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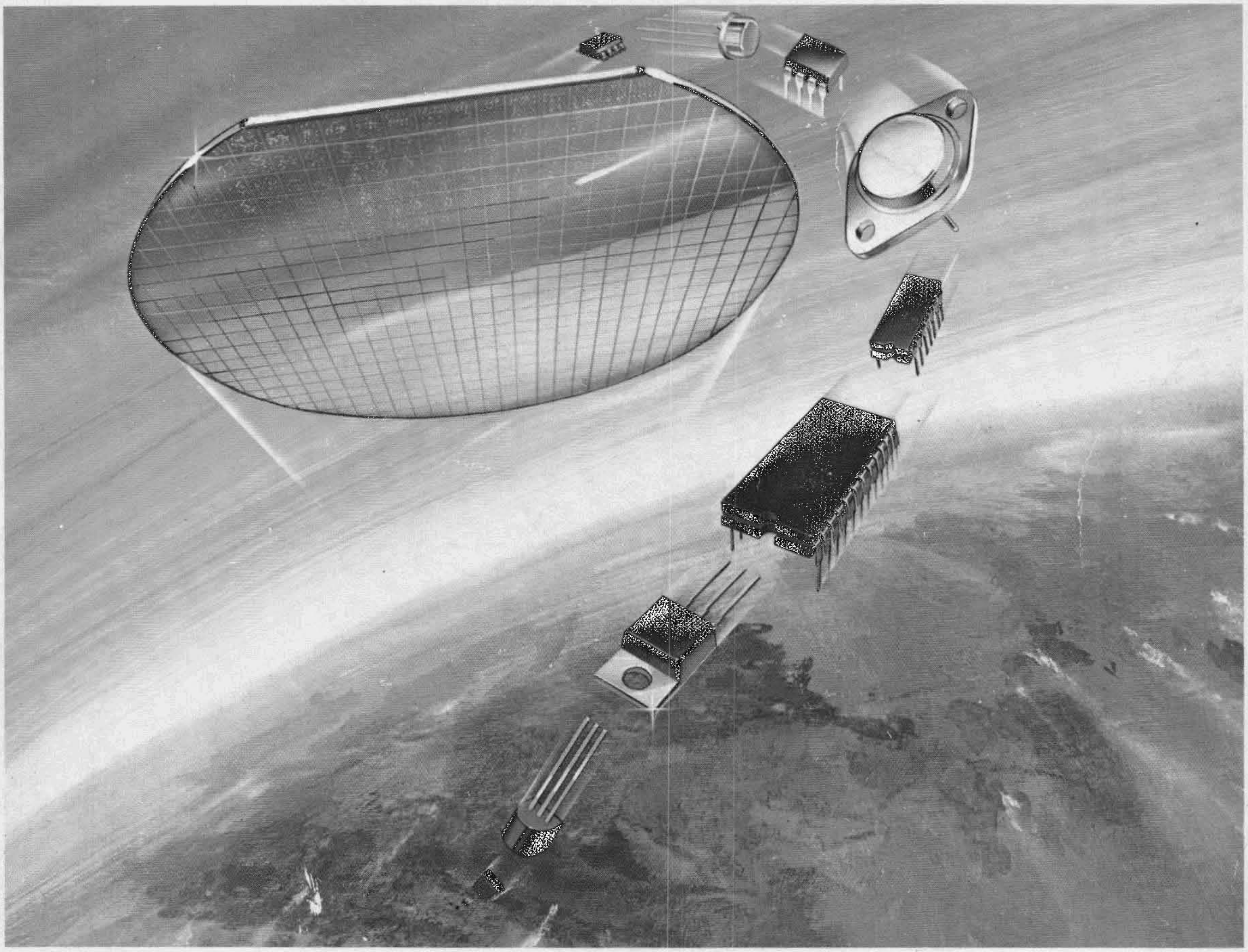
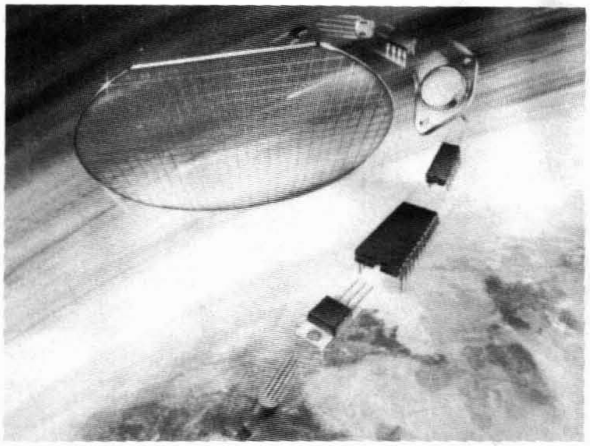


# LINEAR AND INTERFACE INTEGRATED CIRCUITS



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# LINEAR AND INTERFACE INTEGRATED CIRCUITS

This publication presents technical information for the broad line of Linear and Interface Integrated Circuit products. Complete device specifications are provided in the form of **Data Sheets** which are categorized by product type into four chapters for easy reference. **Selector Guides** by product family are provided in Chapter 2 to enable quick comparisons of performance characteristics. A **Cross-Reference** chapter lists Motorola direct replacement and functional equivalent part numbers for other industry products.

A chapter is provided to illustrate **Package Outline** and mounting hardware drawings, and includes information on the new Surface Mount Devices (SMD).

Additionally, chapters are provided with information on **Quality** program concepts, high-reliability processing, and abstracts of available **Technical Literature.**

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

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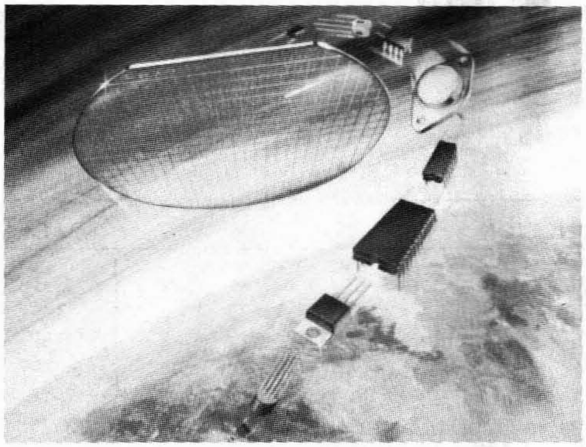

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| MC3505 | Dual Operational Amplifier plus Dual Voltage Comparator | 3-163 |
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| MC3512 | High-Speed 12-Bit D/A Converter | 3-320 |
| MC3517 | Continuously-Variable-Slope Delta Modulator/Demodulator | 3-325 |
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* See Telecommunication Device Data (DL136).

| Device Number | Function | Page |
|---|---|---|
| MC34011A | Electronic Telephone Circuit | * |
| MC34012 Series | Telephone Tone Ringer | * |
| MC34013A | Speech Network and Tone Dialer | * |
| MC34014 | Telephone Speech Network with Dialer Interface | * |
| MC34017 | Telephone Tone Ringer | * |
| MC34018 | Voice Switched Speaker Phone Circuit | * |
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| MC34082,A | Dual High Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC34083 | Dual High Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC34084,A | Quad High Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC34085 | Quad High Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
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| MC35060 | Switchmode Pulse Width Modulation Control Circuits | 4-174 |
| MC35060A | Switchmode Pulse Width Modulation Control Circuits | 4-186 |
| MC35062 | Pin-Programmable Overvoltage Sensing Circuit | 4-304 |
| MC35063 | DC to DC Converter Control Circuits | 4-187 |
| MC35071,A | High Performance Single Supply Operational Amplifiers | 3-206 |
| MC35072,A | Dual High Performance Single Supply Operational Amplifiers | 3-206 |
| MC35074,A | Quad High Performance Single Supply Operational Amplifiers | 3-210 |
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| MC35081 | High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC35082 | Dual High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC35083 | Dual High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC35084,A | Quad High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
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* See Telecommunication Device Data (DL136).

# Cross Reference

A complete interchangeability list linking over 3000 devices are offered by most major Linear Integrated Circuits manufacturers to the nearest equivalent Motorola device. The "Motorola Direct Replacement" column lists devices with identical pin connections and package and the same or better electrical characteristics and temperature range. The "Motorola Similar Replacement" column provides a device which performs the same function but with possible differences in package configurations, pin connections, temperature range or electrical specifications.

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| 8216 | | MC8T26AL |
| 8226 | | MC8T28L |
| 9614DC | | MC75S110L |
| 9614DM | | MC75S110L |
| 9615DC | | MC75108L |
| 9616CDC | | MC1488L |
| 9616EDC | | MC1488L |
| 9616DM | | MC1488L |
| 9617DC | | MC1489AL |
| 9620DC | | MC75S110L |
| 9620DM | | MC75S110L |
| 9621DC | | MC75108L |
| 9627CDC | | MC1489AL |
| 9627DM | | MC1489AL |
| 9636AT | MC3488AP | |
| 9637T | | MC3486P |
| 9638T | | MC3487P |
| 9640DC | MC26S10L | |
| 9640NC | MC3440AP | |
| 9640PC | MC26S10P | |
| 9665DC | MC1411L | |
| 9665PC | MC1411P | |
| 9666DC | MC1412L | |
| 9666PC | MC1412P | |
| 9667DC | MC1413L | |
| 9667PC | MC1413P | |
| 9668DC | MC1416L | |
| 9668PC | MC1416P | |
| 55110DM | | MC75S110L |
| 75107ADC | MC75107L | |
| 75107APC | MC75107P | |
| 75107BDC | | MC75107L |
| 75107BPC | | MC75107P |
| 75108ADC | MC75108L | |
| 75108APC | MC75108P | |
| 75108BDC | | MC75108L |
| 75108BPC | | MC75108P |
| 75110DC | MC75S110L | |
| 75110PC | MC75S110P | |
| 75207DC | | MC75107L |
| 75207PC | | MC75107P |
| 75208DC | | MC75108L |
| 75208PC | | MC75108P |
| AD DAC-08AD | DAC-08AQ | |
| AD DAC-08CD | DAC-08CQ | |
| AD DAC-08D | DAC-08Q | |
| AD DAC-08ED | DAC-08EQ | |
| AD DAC-08HD | DAC-08HQ | |
| AD301AL | | LM301AH |
| AD505J | | MC1776CG |
| AD505K | | MC1776CG |
| AD505S | | MC1776G |
| AD509J | | LM301AH |
| AD509K | | LM301AH |
| AD509S | | LM101AH |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| AD518J | | LM301AH |
| AD518K | | LM301AH |
| AD518S | | LM101AH |
| AD530 | | MC1595L |
| AD531 | | MC1595L |
| AD532L | | MC1595G |
| AD562KD | AD562AKD | |
| AD562SD | AD562ASD | |
| AD563JD | AD563JD | |
| AD563KD | AD563KD | |
| AD563SD | AD563SD | |
| AD563TD | AD563TD | |
| AD565JD | DAC-565JD | |
| AD565KD | | DAC-565JD |
| AD565SD | DAC-565SD | |
| AD565TD | | DAC-565SD |
| AD580J | | MC1403U |
| AD580K | | MC1403P1 |
| AD580M | | MC1403AP1 |
| AD580S | | MC1503U |
| AD580T | | MC1503AU |
| AD589J | | LM385Z-1.2 |
| AD589K | | LM385Z-1.2 |
| AD589L | | LM385Z-1.2 |
| AD589M | | LM385BZ-1.2 |
| AD741CJ | | MC1741CG |
| AD741J | | MC1741G |
| AD741K | | MC1741G |
| AD741L | | MC1741G |
| AD741S | | MC1741SG |
| AD1403AN | | MC1403AU |
| AD1408-7D | MC1408L7 | |
| AD1508-8D | MC1508L8 | |
| AD7520D | | MC3410L |
| AD7520F | | MC3410L |
| AD7520N | | MC3410L |
| AM26LS31CJ | AM26LS31DC | |
| AM26LS31CN | AM26LS31PC | |
| AM26LS31D | AM26LS31D | |
| AM26LS31P | AM26LS31P | |
| AM26LS32ACJ | AM26LS32D | |
| AM26LS32ACN | AM26LS32APC | MC3486L |
| AM26LS32D | AM26LS32D | MC3486P |
| AM26LS32P | AM26LS32PC | |
| AM26LS33DC | | MC3486L |
| AM26LS33PC | | MC3486P |
| AM26S10DC | MC26S10L | |
| AM26S10PC | MC26S10P | |
| AM101 | LM101AH | |
| AM101A | LM101AH | |
| AM101AD | | LM101AH |
| AM101AF | | LM101AH |
| AM101D | | LM101AH |
| AM101F | | LM101AH |
| AM107 | LM111J | MC1741 |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| AM107D | | MC1741 |
| AM107F | | MC1741 |
| AM111D | | MC1741 |
| AM111H | LM111H | |
| AM201 | LM201AH | |
| AM201A | LM201AH | |
| AM201AD | | LM201AN |
| AM201AF | | LM201AH |
| AM201D | | LM201AN |
| AM201F | | LM201AH |
| AM207 | LM211S | MC1741C |
| AM207D | | MC1741C |
| AM207F | | MC1741C |
| AM211D | | MC1741C |
| AM211H | LM211H | |
| AM301 | LM301AH | |
| AM301A | LM301AH | |
| AM301AD | | LM301AJ |
| AM301D | | LM301AJ |
| AM311D | LM311J-8 | |
| AM311H | LM311H | |
| AM592DC | NE592F | |
| AM592DM | SE592F | |
| AM592HC | NE592K | |
| AM592HM | SE592K | |
| AM592PC | NE592N | |
| AM723DC | MC1723CL | |
| AM723DM | MC1723L | |
| AM723HC | MC1723CG | |
| AM723HM | MC1723G | |
| AM723PC | MC1723CP | |
| AM725A31T | | MC1556G |
| AM725HM | MC1556G | |
| AM733DC | MC1733CL | |
| AM733DM | MC1733L | |
| AM733HC | MC1733CG | |
| AM733HM | MC1733G | |
| AM741DC | | MC1741CU |
| AM741DM | | MC1741U |
| AM741HC | MC1741CG | |
| AM741HM | MC1741G | |
| AM747DC | MC1747CL | |
| AM747DM | MC1747L | |
| AM747HC | MC1747CG | |
| AM747HM | MC1747G | |
| AM748DC | | MC1748CU |
| AM748DM | | MC1748U |
| AM748HC | MC1748CG | |
| AM748HM | MC1748G | |
| AN5150 | | MC13002P |
| AN5151 | | MC13001P |
| CA081AE | | TL081ACP |
| CA081AS | | TL081ACJG |
| CA081BE | | TL081BCP |
| CA081CS | | TL081CJG |
| CA081E | | TL081CP |
| CA081S | | TL081MJG |
| CA082AE | | TL082ACP |
| CA082AS | | TL082ACJG |
| CA082BE | | TL082BCP |
| CA082CS | | TL082CJG |
| CA082E | | TL082CP |
| CA082S | | TL082MJG |
| CA084AE | | TL084ACN |
| CA084E | | TL084CN |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| CA084S | | TL082MJ |
| CA101AT | LM101AH | |
| CA101T | LM101AH | |
| CA107T | | MC1741 |
| CA108AS | LM108AJ-8 | |
| CA108AT | LM108AH | |
| CA108S | LM108J-8 | |
| CA108T | LM108H | |
| CA139AG | LM139AJ | |
| CA139G | LM139J | |
| CA201AT | LM201AH | |
| CA201T | | LM201AH |
| CA207T | | MC1741C |
| CA208AT | LM208AH | |
| CA208S | LM208J-8 | |
| CA208T | LM208H | |
| CA239AE | LM239AN | |
| CA239AG | LM239AJ | |
| CA239E | LM239N | |
| CA239G | LM239J | |
| CA301AT | LM301AH | |
| CA308AS | LM308N | |
| CA308AT | LM308AH | |
| CA308S | LM308H | |
| CA339AE | LM339AN | |
| CA339AG | LM339AJ | |
| CA339E | LM339N | |
| CA339G | LM339J | |
| CA723CE | MC1723CP | |
| CA723CT | MC1723CG | |
| CA723E | MC1723L | |
| CA723T | MC1723G | |
| CA741CS | MC1741CP1 | |
| CA741CT | MC1741CG | |
| CA741S | MC1741U | |
| CA741T | MC1741G | |
| CA747CE | MC1747CL | |
| CA747CF | MC1747CL | |
| CA747CT | MC1747CG | |
| CA747E | MC1747L | |
| CA747F | MC1747L | |
| CA747T | MC1747G | |
| CA748CS | MC1748CP1 | |
| CA748CT | MC1748CG | |
| CA748S | MC1748U | |
| CA748T | MC1748G | |
| CA1352E | MC1352P | |
| CA1391E | MC1391P | |
| CA1394E | MC1394P | |
| CA1458S | MC1458CP1 | |
| CA1458T | MC1458G | |
| CA1558S | | MC1558U |
| CA1558T | MC1558G | |
| CA2111AE | MC1357P | |
| CA3008 | | MC1709U |
| CA3008A | | MC1709U |
| CA3010 | | MC1709G |
| CA3010A | | MC1709G |
| CA3011 | | MC1590G |
| CA3012 | | MC1590G |
| CA3013 | | MC1357P |
| CA3014 | | MC1357P |
| CA3015 | | MC1709G |
| CA3015A | | MC1709G |
| CA3016 | | MC1709U |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| CA3016A | | MC1709U |
| CA3020 | | MC1554G |
| CA3020A | | MC1454G |
| CA3021 | | MC1590G |
| CA3022 | | MC1590G |
| CA3023 | | MC1590G |
| CA3026 | | CA3054 |
| CA3029 | | MC1709P1 |
| CA3029A | | MC1709P1 |
| CA3030 | | MC1709P1 |
| CA3030A | | MC1709P1 |
| CA3031 | | MC1733 |
| CA3032 | | MC1733 |
| CA3035 | | MC1352P |
| CA3035V1 | | MC1352P |
| CA3037 | | MC1709U |
| CA3037A | | MC1709U |
| CA3038 | | MC1709U |
| CA3038A | | MC1709U |
| CA3040 | | MC1510G |
| CA3041 | | MC1357P |
| CA3042 | | MC1357P |
| CA3043 | | MC1357P |
| CA3044 | | MC13010P |
| CA3044V1 | | MC13010P |
| CA3045 | | MC3346P |
| CA3045F | | MC3346P |
| CA3046 | MC3346P | |
| CA3048 | | MC3301P |
| CA3052 | | MC3301P |
| CA3054 | CA3054 | |
| CA3056 | MC1741CG | |
| CA3056A | MC1741G | |
| CA3058 | | CA3059 |
| CA3059 | CA3059 | |
| CA3064 | | MC13010P |
| CA3065 | MC1358P | |
| CA3068 | | MC1352P |
| CA3076 | | MC1590G |
| CA3078AS | | MC1776G |
| CA3078AT | | MC1776G |
| CA3078S | | MC1776CG |
| CA3078T | | MC1776CG |
| CA3079 | CA3079 | CA3059 |
| CA3085 | | MC1723G |
| CA3085A | | MC1723G |
| CA3085AF | | MC1723L |
| CA3085AS | | MC1723G |
| CA3085B | | MC1723G |
| CA3085BF | | MC1723L |
| CA3085BS | | MC1723G |
| CA3085F | | MC1723L |
| CA3085S | | MC1723G |
| CA3086 | MC3386P | |
| CA3086F | | MC3346P |
| CA3091D | | MC1594L |
| CA3121E | | TDA3333 |
| CA3136A | | MC3346P |
| CA3139 | | MC13010P |
| CA3145E | | TDA3333 |
| CA3146 | | MC3346P |
| CA3151E | | TDA3333 |
| CA3201E | | TDA3301 |
| CA3210E | | MC13001P |
| CA3217E | | TDA3301 |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| CA3221E | | TDA3333 |
| CA3223E | | MC13002P |
| CA3302E | MC3302P | |
| CA3401E | MC3401P | |
| CA6078AS | | MC1776G |
| CA6078AT | | MC1776G |
| CA6741S | | MC1776G |
| CA6741T | | MC1776G |
| CA7607E | | MC13010P |
| CA7611E | | MC13010P |
| CMP-01CJ | | MC1556G |
| CMP-01CP | | MC1556P |
| CS3471 | MC3471P | |
| D555CJ | | MC1555G |
| D3242 | MC3242AP | |
| D8216 | | MC8T26AL |
| D8226 | | MC8T28L |
| DAC-01 | | MC1506L |
| DAC-08AQ | DAC-08AQ | |
| DAC-08CN | DAC-08CP | |
| DAC-08CP | DAC-08CP | |
| DAC-08CQ | DAC-08CQ | |
| DAC-08EN | DAC-08EP | |
| DAC-08EP | DAC-08EP | |
| DAC-08EQ | DAC-08EQ | |
| DAC-08HN | DAC-08HP | |
| DAC-08HP | DAC-08HP | |
| DAC-08HQ | DAC-08HQ | |
| DAC-08Q | DAC-08Q | |
| DAC-ICC10BC | MC3410L | |
| DAC0800LCJ | DAC-08EQ | |
| DAC0800LCN | DAC-08EP | |
| DAC0800LD | DAC-08Q | |
| DAC0801LCJ | DAC-08CQ | |
| DAC0801LCN | DAC-08CP | |
| DAC0802LCJ | DAC-08HQ | |
| DAC0802LCN | DAC-08HP | |
| DAC0802LD | DAC-08AQ | |
| DAC0806LCJ | MC1408L6 | |
| DAC0806LCN | MC1408P6 | |
| DAC0807LCJ | MC1408L7 | |
| DAC0807LCN | MC1408P7 | |
| DAC0808LCJ | MC1408L8 | |
| DAC0808LCN | MC1408P8 | |
| DAC0808LD | MC1508L8 | |
| DM7822J | | MC1489AL |
| DM7837J | | MC3437L |
| DM8822J | | MC1489AL |
| DM8822N | | MC1489AP |
| DM8837N | MC3437P | |
| DS26LS31J | AM26LS31D | |
| DS26LS31N | AM26LS31P | |
| DS26LS32J | AM26LS32D | |
| DS26LS32N | AM26LS32P | |
| DS26S10CJ | MC26S10L | |
| DS26S10CN | MC26S10P | |
| DS1488J | MC1488L | |
| DS1488N | MC1488P | |
| DS1489AJ | MC1489AL | |
| DS1489AN | MC1489AP | |
| DS1489J | MC1489L | |
| DS1489N | MC1489P | |
| DS3486J | MC3486L | |
| DS3486N | MC3486P | |
| DS3487J | MC3487L | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| DS3487N | MC3487P | |
| DS3612H | | MC1472U |
| DS3612N | | MC1472P1 |
| DS3632H | MC1472U | |
| DS3632J | MC1472U | |
| DS3632N | MC1472P1 | |
| DS3650J | MC3450L | |
| DS3650N | MC3450P | |
| DS3651J | MC3430L | |
| DS3651N | MC3430P | |
| DS3652J | MC3452L | |
| DS3652N | MC3452P | |
| DS3653J | MC3432L | |
| DS3653N | MC3432P | |
| DS7837J | | MC3437L |
| DS7837W | | MC3437L |
| DS8833J | | MC8T28L |
| DS8833N | | MC8T28P |
| DS8834J | | MC8T26AL |
| DS8834N | | MC8T26AP |
| DS8835J | | MC8T26AL |
| DS8835N | | MC8T26AP |
| DS8837J | MC3437L | |
| DS8837N | MC3437P | |
| DS8839J | | MC8T28L |
| DS8839N | | MC8T28P |
| DS55107W | | MC75107L |
| DS55110J | | MC75S110L |
| DS75107J | MC75107L | |
| DS75107N | MC75107P | |
| DS75108J | MC75108L | |
| DS75108N | MC75108P | |
| DS75110J | MC75S110L | |
| DS75110N | MC75S110P | |
| DS75207J | | MC75107L |
| DS75207N | | MC75107P |
| DS75208J | | MC75108L |
| DS75208N | | MC75108P |
| HC5501 | | MC34F19CL |
| HC5502 | | MC34F19CL |
| HI-562-2 | AD562ASD | |
| HI-562-5 | AD562AKD | |
| ICB8000C | | LM111J |
| ICB8001C | | LM111J |
| ICB8741C | | MC1741CG |
| ICH8500ATV | | MC1776CG |
| ICH8500TV | | MC1776CG |
| ICL101ALNDP | | LM101AH |
| ICL101ALNFB | | LM101AH |
| ICL101ALNTY | | LM101AH |
| ICL301ALNPA | | LM301AH |
| ICL301ALNTY | | LM301AH |
| ICL741CLNPA | | MC1741CP1 |
| ICL741CLNTY | | MC1741CP1 |
| ICL8001CTZ | | LM111J |
| ICL8001MTZ | | LM111J |
| ICL8007CTA | | MC1709CG |
| ICL8007MTA | | MC1709CG |
| ICL8008CPA | | LM301AN |
| ICL8008CTY | | LM301AN |
| ICL8013A | | MC1594G |
| ICL8013B | | MC1594G |
| ICL8013C | | MC1594G |
| ICL8017CTW | | LM301AN |
| ICL8017MTW | | LM301AN |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| ICL8021C | | MC1776G |
| ICL8021M | | MC1776G |
| ICL8022C | | MC1776G |
| ICL8022M | | MC1776G |
| ICL8043CDE | | MC1776G |
| ICL8043CPE | | MC1776G |
| ICL8043MDE | | MC1776G |
| ICL8048CDE | | MC1776G |
| ICL8048CPE | | MC1776G |
| ICL8048DPE | | MC1776G |
| ICL8069CCZR | | LM385BZ-1.2 |
| ICL8069DCZR | | LM385BZ-1.2 |
| ITT652 | MC1411P | |
| ITT654 | MC1412P | |
| ITT656 | MC1413P | |
| ITT1330 | MC1330P | |
| ITT1352 | MC1352P | |
| ITT3064 | MC13010P | |
| ITT3065 | MC1358P | |
| ITT3710 | | MC1391P |
| ITT3714 | | MC1394P |
| L144AP | | LM324N |
| L201 | MC1411P | |
| L202 | MC1412P | |
| L203 | MC1413P | |
| L583 | | MC3484V2 |
| LF347BN | LF347BN | |
| LF347N | LF347N | |
| LF347N | MC34004P | |
| LF351AH | MC34001AG | |
| LF351AN | MC34001AP | |
| LF351BH | MC34001BG | |
| LF351BN | MC34001BP | |
| LF351H | MC34001G | |
| LF351N | LF351N | |
| LF351N | MC34001P | |
| LF352D | | LF355J |
| LF353AH | MC34002AG | |
| LF353AN | MC34002AP | |
| LF353BH | MC34002BG | |
| LF353BN | MC34002BP | |
| LF353H | MC34002G | |
| LF353N | LF353N | |
| LF353N | MC34002P | |
| LF355AH | | |
| LF355AJG | | |
| LF355AL | | |
| LF355AP | | |
| LF355BH | LF355BH | |
| LF355BJ | LF355J | |
| LF355H | LF355H | |
| LF355J | LF355J | |
| LF355JG | LF355J | |
| LF355L | LF355H | |
| LF355N | LF355J | |
| LF355P | LF355J | |
| LF356AH | | |
| LF356AL | | |
| LF356AJG | | |
| LF356AP | | |
| LF356BH | LF356BH | |
| LF356BJ | LF356BJ | |
| LF356BN | LF356J | |
| LF356H | LF356H | |
| LF356J | LF356J | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| LF356JG | LF356J | |
| LF356L | LF356H | |
| LF356N | LF356J | |
| LF356P | LF356J | |
| LF357AH | | |
| LF357BH | LF357BH | |
| LF357BJ | LF357BJ | |
| LF357BN | LF357BJ | |
| LF357H | LF357H | |
| LF357J | LF357J | |
| LF357JG | LF357J | |
| LF357L | LF357H | |
| LF357N | LF357J | |
| LF357P | LF357J | |
| LF411CH | | MC34001AG |
| LF11CN | | MC34001AP |
| LF412CH | | MC34002AG |
| LF412CN | | MC34002AP |
| LG351AH | MC34001AG | |
| LG351AN | MC34001AP | |
| LH000ACD | | MC1776CG |
| LH000ACF | | MC1776CG |
| LH000ACH | | MC1776CG |
| LH000AD | | MC1776G |
| LH000AF | | MC1776G |
| LH000AH | | MC1776G |
| LH0004CH | | MC1436G |
| LH0004CHH | | MC1536G |
| LH0004H | | MC1536G |
| LH042CH | | MC1176G |
| LH101H | | MC1741G |
| LH201H | | MC1741G |
| LH740ACH | | LF355H |
| LH2101AD | | MC1537L |
| LH2101AF | | MC1537L |
| LH2201AD | | MC1537L |
| LH2201AF | | MC1537L |
| LH2301AD | | MC1437L |
| LH2301AF | | MC1437L |
| LM11CH | LM11CH | |
| LM11CJ | LM11CJ | |
| LM11CJ-8 | LM11CJ-8 | |
| LM11CLH | LC11CLH | |
| LM11CLJ | LC11CLJ | |
| LM11CLJ-8 | LC11CLJ-8 | |
| LM11CLN | LC11CLN | |
| LM11CLN-14 | LC11CLN-14 | |
| LM11CN | LC11CN | |
| LM11CN-14 | LC11CN-14 | |
| LM11H | LC11H | |
| LM11J | LC11J | |
| LM11J-8 | LC11J-8 | |
| LM101AD | | LM101AH |
| LM101AF | | LM101AH |
| LM101AH | LM101AH | |
| LM101AJ | LM101AJ | |
| LM101AJ-14 | | LM101AJ |
| LM101AJG | LM101AJ | |
| LM101AL | LM101AH | |
| LM101D | | LM101AJ |
| LM101F | | LM101AH |
| LM101H | LM101AH | |
| LM101J-14 | | LM101AJ |
| LM106H | | MC1710G |
| LM107F | | MC1741 |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| LM107H | MC1741 | |
| LM107L | MC1741 | |
| LM108AD | LM108AJ | |
| LM108AF | LM108AF | |
| LM108AH | LM108AH | |
| LM108AJ | LM108AJ | |
| LM108AJ | LM108J-8 | |
| LM108AJ-8 | LM108AJ-8 | |
| LM108D | LM108J | |
| LM108F | LM108F | |
| LM108H | LM108H | |
| LM108J | LM108J | |
| LM108J-8 | LM108J-8 | |
| LM109H | LM109H | |
| LM109K | LM109K | |
| LM109LA | LM109K | |
| LM111D | | |
| LM111H | LM111H | |
| LM111HH | | LM111H |
| LM111J | LM111J | |
| LM111J-8 | LM111J-8 | |
| LM111JG | LM111J-8 | |
| LM112D | | MC1556U |
| LM112F | | MC1556U |
| LM112H | | MC1556U |
| LM117H | LM117H | |
| LM117K | LM117K | |
| LM117LA | LM117H | |
| LM117LH | LM117LH | |
| LM118D | | MC1741SU |
| LM118F | | MC1741SU |
| LM118H | | MC1741SG |
| LM120H-5.0 | | MC7905CK |
| LM120H-5.2 | | MC7905.2CK |
| LM120H-12 | | MC7912CK |
| LM120H-15 | | MC7915CK |
| LM120K-5.0 | | MC7905CK |
| LM120K-5.2 | | MC7905.2CK |
| LM120K-12 | | MC7912CK |
| LM120K-15 | | MC7915CK |
| LM122F | | MC1556G |
| LM122H | | MC1556G |
| LM123AK | LM123AK | |
| LM123K | LM123K | |
| LM124AD | | LM124J |
| LM124AF | | LM124J |
| LM124AJ | | LM124J |
| LM124D | LM124J | |
| LM124F | | LM124J |
| LM124J | LM124J | |
| LM125H | | MC1568G |
| LM126H | | MC1568G |
| LM128H | | MC1568G |
| LM137H | LM137H | |
| LM137K | LM137K | |
| LM139AD | LM139AJ | |
| LM139AJ | LM139AJ | |
| LM139D | LM139J | |
| LM139J | LM139J | |
| LM140AK-5.0 | LM140AK-5.0 | |
| LM140AK-12 | LM140AK-12 | |
| LM140AK-15 | LM140AK-15 | |
| LM140K-5.0 | LM140K-5.0 | |
| LM140K-6.0 | LM140K-6.0 | |
| LM140K-8.0 | LM140K-8.0 | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| LM140K-12 | LM140K-12 | |
| LM140K-15 | LM140K-15 | |
| LM140K-18 | LM140K-18 | |
| LM140K-24 | LM140K-24 | |
| LM140LAH-5.0 | | MC78L05ACG |
| LM140LAH-6.0 | | MC78L05ACG |
| LM140LAH-8.0 | | MC78L08ACG |
| LM140LAH-12 | | MC78L12ACG |
| LM140LAH-15 | | MC78L15ACG |
| LM140LAH-18 | | MC78L18ACG |
| LM140LAH-24 | | MC78L24ACG |
| LM140LAH-50 | | MC78L05ACG |
| LM140LAH-80 | | MC78L05ACG |
| LM143D | | MC1536G |
| LM143F | | MC1536G |
| LM143H | | MC1536G |
| LM145K | | MC7905CK |
| LM148D | LM148J | |
| LM148J | LM148J | |
| LM148F | | MC4741L |
| LM149D | | MC4741L |
| LM149F | | MC4741L |
| LM150K | LM150K | |
| LM158AH | | LM158H |
| LM158H | LM158H | |
| LM158J | LM158J | |
| LM158JG | LM158J | |
| LM158L | LM158H | |
| LM163J | | MC3450L |
| LM171H | | MC1590G |
| LM193AH | LM193AH | |
| LM193H | LM193H | |
| LM193JG | | LM193H |
| LM193U | | LM193H |
| LM201AD | | LM201AJ |
| LM201AF | | LM201AH |
| LM201AH | LM201AH | |
| LM201AJ | | LM201AJ |
| LM201AJG | | LM201AJ |
| LM201AJ-14 | | LM201AJ |
| LM201AL | LM201AH | |
| LM201AN | LM201AN | |
| LM201AND | LM201AND | |
| LM201AP | LM201AN | |
| LM201D | | LM201AJ |
| LM201F | | LM201AH |
| LM201H | LM201AH | |
| LM201J | LM201AJ | |
| LM201J-14 | | LM201AJ |
| LM207F | | MC1741C |
| LM207H | | MC1741C |
| LM208AD | LM208AJ | |
| LM208AF | LM208AF | |
| LM208AH | LM208AH | |
| LM208AJ | LM208AJ-8 | |
| LM208AJ-8 | LM208AJ-8 | |
| LM208AN | LM208AN | |
| LM208D | | LM208J-8 |
| LM208F | LM208J-8 | |
| LM208H | LM208H | |
| LM208J | LM208J | |
| LM208J-8 | LM208J-8 | |
| LM209H | LM209H | |
| LM209K | LM209K | |
| LM209LA | LM209H | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| LM211D | LM211D | |
| LM211H | LM211H | |
| LM211J-8 | LM211J-8 | |
| LM211JG | LM211J-8 | |
| LM212D | | MC1556U |
| LM212F | | MC1556U |
| LM212H | | MC1456U |
| LM217H | LM217H | |
| LM217K | LM217K | |
| LM217KC | | LM217K |
| LM217KD | | LM217H |
| LM217LA | LM217H | |
| LM217LH | LM217LH | |
| LM218D | | MC1741SU |
| LM218F | | MC1741SU |
| LM218H | | MC1741SG |
| LM220H-5.0 | | MC7905CK |
| LM220H-5.2 | | MC7905.2CK |
| LM220H-6.0 | | MC7906CK |
| LM220H-8.0 | | MC7908CK |
| LM220H-12 | | MC7912CK |
| LM220H-15 | | MC7915CK |
| LM220H-18 | | MC7918CK |
| LM220H-24 | | MC7924CK |
| LM220K-5.0 | | MC7905CK |
| LM220K-5.2 | | MC7905.2CK |
| LM220K-6.0 | | MC7906CK |
| LM220K-8.0 | | MC7908CK |
| LM220K-12 | | MC7912CK |
| LM220K-15 | | MC7915CK |
| LM220K-18 | | MC7918CK |
| LM220K-24 | | MC7924CK |
| LM222H | | MC1556G |
| LM223AK | LM223AK | |
| LM223K | LM223K | |
| LM224AD | | LM224J |
| LM224AF | | LM224J |
| LM224AJ | | LM224J |
| LM224D | LM224D | |
| LM224D | LM224J | |
| LM224F | | LM224J |
| LM224J | LM224J | |
| LM224N | LM224N | |
| LM225H | | MC1568G |
| LM226H | | MC1568G |
| LM228H | | MC1568G |
| LM237H | LM237H | |
| LM237K | LM237K | |
| LM239AD | LM239AJ | |
| LM239AJ | LM239AJ | |
| LM239AN | LM239AN | |
| LM239D | LM239D | |
| LM239D | LM239J | |
| LM239J | LM239J | |
| LM239N | LM239N | |
| LM240LAH-5.0 | | MC78L05ACG |
| LM240LAH-6.0 | | MC78L06CG |
| LM240LAH-8.0 | | MC78L08ACG |
| LM240LAH-12 | | MC78L12ACG |
| LM240LAH-15 | | MC78L15ACG |
| LM240LAH-18 | | MC78L18ACG |
| LM240LAH-24 | | MC78L24ACG |
| LM240LAZ-5.0 | | MC78L05ACP |
| LM240LAZ-6.0 | | MC78L06ACP |
| LM240LAZ-8.0 | | MC78L08ACP |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| LM240LAZ-12 | | MC78L12ACP |
| LM240LAZ-15 | | MC78L15ACP |
| LM240LAZ-18 | | MC78L18ACP |
| LM240LAZ-24 | | MC78L24ACP |
| LM243H | | MC1536G |
| LM245K | | MC7905CK |
| LM248D | LM248J | |
| LM248J | LM248J | |
| LM249D | | LMC4741L |
| LM249J | | LMC4741L |
| LM250K | LM250K | |
| LM258AH | | LM258H |
| LM258D | LM258D | |
| LM258H | LM258H | |
| LM258J | LM258J | |
| LM258N | LM258N | |
| LM271H | | MC1590G |
| LM285Z-1.2 | LM285Z-1.2 | |
| LM285Z-2.5 | LM285Z-2.5 | |
| LM293AH | LM293AH | |
| LM293H | LM293H | |
| LM293P | | LM293H |
| LM293U | | LM293H |
| LM301AD | LM301AD | LM301AJ |
| LM301AF | | LM301AH |
| LM301AH | LM301AH | |
| LM301AJ | LM301AJ | |
| LM301AJD | LM301AJD | |
| LM301AJDS | LM301AJDS | |
| LM301AJG | LM301AJ | |
| LM301AJS | LM301AJS | |
| LM301AL | LM301AH | |
| LM301AN | LM301AN | |
| LM301AND | LM301AND | |
| LM301ANDS | LM301ANDS | |
| LM301ANS | LM301ANS | |
| LM301AP | LM301AN | |
| LM307N | LM307N | |
| LM307P | LM307N | |
| LM308AD | LM308AJ | |
| LM308AF | | LM308AJ |
| LM308AH | LM308AH | |
| LM308AH-1 | | LM308AH |
| LM308AH-2 | | LM308AH |
| LM308AJ | LM308AJ | |
| LM308AJ | LM308AJ-8 | |
| LM308AJ-8 | LM308AJ-8 | |
| LM308AJ-8D | LM308AJ-8D | |
| LM308AJ-8DS | LM308AJ-8DS | |
| LM308AJ-8S | LM308AJ-8S | |
| LM308AN | LM308AN | |
| LM308AND | LM308AND | |
| LM308ANDS | LM308ANDS | |
| LM308ANS | LM308ANS | |
| LM308D | LM308D | |
| LM308D | LM308J | |
| LM308H | LM308H | |
| LM308J | LM308J | |
| LM308J-8 | LM308J-8 | |
| LM308J-8D | LM308J-8D | |
| LM308J-8DS | LM308J-8DS | |
| LM308J-8S | LM308J-8S | |
| LM308N | LM308N | |
| LM308ND | LM308ND | |
| LM308NDS | LM308NDS | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| LM308NS | LM308NS | |
| LM309H | LM309H | |
| LM309K | LM309K | |
| LM309KC | LM309K | |
| LM309LA | LM309K | |
| LM311D | LM311D | |
| LM311H | LM311H | |
| LM311J-8 | LM311J-8 | |
| LM311J-8D | LM311J-8D | |
| LM311J-8DS | LM311J-8DS | |
| LM311J-8S | LM311J-8S | |
| LM311JG | LM311J-8 | |
| LM311N | LM311J | |
| LM311N-14 | LM311J | |
| LM311ND | LM311ND | |
| LM311NDS | LM311NDS | |
| LM311NS | LM311NS | |
| LM311P | LM311N | |
| LM312D | | MC1456U |
| LM312F | | MC1456U |
| LM312H | | MC1456G |
| LM317H | LM317H | |
| LM317K | LM317K | |
| LM317KC | LM317T | |
| LM317KD | | LM317T |
| LM317LA | LM317H | |
| LM317LH | LM317LH | |
| LM317LZ | LM317LZ | |
| LM317MP | LM317MT | |
| LM317MT | LM317MT | |
| LM317P | LM317T | |
| LM317T | LM317T | |
| LM318D | | MC1741SCU |
| LM318F | | MC1741SCU |
| LM318H | | MC1741SCG |
| LM318N | | MC1741SCP1 |
| LM320H-5.0 | | MC7905CK |
| LM320H-5.2 | | MC7905.2CK |
| LM320H-12 | | MC7912CK |
| LM320H-15 | | MC7915CK |
| LM320K-5.0 | MC7905CK | |
| LM320K-12 | MC7912CK | |
| LM320K-15 | MC7915CK | |
| LM320LZ-5.0 | MC79L05ACP | |
| LM320LZ-12 | MC79L12ACP | |
| LM320LZ-15 | MC79L15ACP | |
| LM320MP-5.0 | | MC7905CT |
| LM320MP-5.2 | | MC7905.2CT |
| LM320MP-6.0 | | MC7906CT |
| LM320MP-8.0 | | MC7908CT |
| LM320MP-12 | | MC7912CT |
| LM320MP-15 | | MC7915CT |
| LM320MP-18 | | MC7918CT |
| LM320MP-24 | | MC7924CT |
| LM320T-5.0 | MC7905CT | |
| LM320T-5.2 | | MC7905.2CT |
| LM320T-12 | MC7912CT | |
| LM320T-15 | MC7915CT | |
| LM322H | | MC1455G |
| LM322N | | MC1455P1 |
| LM323AK | LM323AK | |
| LM323AT | LM323AT | |
| LM323K | LM323K | |
| LM323T | LM323T | |
| LM324AJ | | LM324J |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| LM324AN | LM324AN | LM324N |
| LM324D | LM324D | |
| LM324J | LM324J | |
| LM324JD | LM324JD | |
| LM324JDS | LM324JDS | |
| LM324JS | LM324JS | |
| LM324N | LM324N | MC3403P |
| LM324ND | LM324ND | |
| LM324NDS | LM324NDS | |
| LM324NS | LM324NS | |
| LM325AN | | MC1468L |
| LM325AS | | MC1468L |
| LM325G | | MC1468L |
| LM325H | | MC1468G |
| LM325N | | MC1468L |
| LM326H | | MC1468G |
| LM326N | | MC1468L |
| LM326S | | MC1468L |
| LM328AN | | MC1468L |
| LM328H | | MC1468G |
| LM328N | | MC1468L |
| LM337H | LM337H | |
| LM337K | LM337K | |
| LM337MP | | LM337MT |
| LM337MT | LM337MT | |
| LM337T | LM337T | |
| LM339AD | LM339AJ | |
| LM339AJ | LM339AJ | |
| LM339AN | LM339AN | |
| LM339D | LM339D | |
| LM339J | LM339J | |
| LM339JD | LM339JD | |
| LM339JDS | LM339JDS | |
| LM339JS | LM339JS | |
| LM339N | LM339N | |
| LM339ND | LM339ND | |
| LM339NDS | LM339NDS | |
| LM339NS | LM339NS | |
| LM339P | LM339N | |
| LM340AK-5.0 | LM340AK-5.0 | |
| LM340AK-12 | LM340AK-12 | |
| LM340AK-15 | LM340AK-15 | |
| LM340AT-5.0 | LM340AT-5.0 | |
| LM340AT-12 | LM340AT-12 | |
| LM340AT-15 | LM340AT-15 | |
| LM340K-5.0 | LM340K-5.0 | |
| LM340K-5.0 | MC7805CK | |
| LM340K-6.0 | LM340K-6.0 | |
| LM340K-6.0 | MC7806CK | |
| LM340K-8.0 | LM340K-8.0 | |
| LM340K-8.0 | MC7808CK | |
| LM340K-12 | LM340K-12 | |
| LM340K-15 | LM340K-15 | |
| LM340K-18 | LM340K-18 | |
| LM340K-24 | LM340K-24 | |
| LM340KC-5 | LM340T-5.0 | |
| LM340KC-6 | LM340T-6.0 | |
| LM340KC-8 | LM340T-8.0 | |
| LM340KC-12 | MC7812CK | |
| LM340KC-15 | MC7815CK | |
| LM340KC-18 | MC7818CK | |
| LM340KC-24 | MC7824CK | |
| LM340LAH-5.0 | | MC78L05ACG |
| LM340LAH-6.0 | | MC78L06ACG |
| LM340LAH-8.0 | | MC78L08ACG |
| LM340LAH-12 | | MC78L12ACG |
| LM340LAH-15 | | MC78L15ACG |
| LM340LAH-18 | | MC78L18ACG |
| LM340LAH-24 | | MC78L24ACG |
| LM340LAZ-5.0 | | MC78L05ACP |
| LM340LAZ-6.0 | | MC78L06ACP |
| LM340LAZ-8.0 | | MC78L08ACP |
| LM340LAZ-12 | | MC78L12ACP |
| LM340LAZ-15 | | MC78L15ACP |
| LM340LAZ-18 | | MC78L18ACP |
| LM340LAZ-24 | | MC78L24ACP |
| LM340T-5.0 | LM340T-5.0 | |
| LM340T-5.0 | MC7805CT | |
| LM340T-6.0 | LM340T-6.0 | |
| LM340T-6.0 | MC7806CT | |
| LM340T-8.0 | LM340T-8.0 | |
| LM340T-8.0 | MC7808CT | |
| LM340T-12 | LM340T-12 | |
| LM340T-12 | MC7812CT | |
| LM340T-15 | LM340T-15 | |
| LM340T-15 | MC7815CT | |
| LM340T-18 | LM340T-18 | |
| LM340T-18 | MC7818CT | |
| LM340T-24 | LM340T-24 | |
| LM340T-24 | MC7824CT | |
| LM341P-5.0 | MC78M05CT | |
| LM341P-6.0 | MC78M06CT | |
| LM341P-8.0 | MC78M08CT | |
| LM341P-12 | MC78M12CT | |
| LM341P-15 | MC78M15CT | |
| LM341P-18 | MC78M18CT | |
| LM341P-24 | MC78M24CT | |
| LM342P-5.0 | MC78M05CT | |
| LM342P-6.0 | MC78M06CT | |
| LM342P-8.0 | MC78M08CT | |
| LM342P-12 | MC78M12CT | |
| LM342P-15 | MC78M15CT | |
| LM342P-18 | MC78M18CT | |
| LM342P-24 | MC78M24CT | |
| LM343D | | MC1436G |
| LM343H | | MC1436G |
| LM345K | | MC7905CK |
| LM348D | LM348D | |
| LM348D | LM348J | |
| LM348J | LM348J | |
| LM348N | LM348N | |
| LM349D | | MC4741CL |
| LM349J | | MC4741CL |
| LM349N | | MC4741CL |
| LM350K | LM350K | |
| LM350T | LM350T | |
| LM358AH | | LM358H |
| LM358AN | | LM358N |
| LM358D | LM358D | |
| LM358H | LM358H | |
| LM358J | LM358J | |
| LM358JD | LM358JD | |
| LM358JDS | LM358JDS | |
| LM358JG | LM358J | |
| LM358JS | LM358JS | |
| LM358L | LM358H | |
| LM358N | LM358N | |
| LM358ND | LM358ND | |
| LM358NDS | LM358NDS | |
| LM358NS | LM358NS | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| LM358P | LM358N | |
| LM363AJ | | MC3450L |
| LM363AN | | MC3450P |
| LM363J | | MC3450L |
| LM363N | | MC3450P |
| LM371H | | MC1590G |
| LM385BZ-1.2 | | LM385BZ-1.2 |
| LM385Z-1.2 | | LM385Z-1.2 |
| LM385BZ-2.5 | | LM385BZ-2.5 |
| LM385Z-2.5 | | LM385Z-2.5 |
| LM393AH | LM393AH | |
| LM393AN | LM393AN | |
| LM393D | LM393D | |
| LM393H | LM393H | |
| LM393J | LM393J | |
| LM393JG | | LM393N |
| LM393N | LM393N | |
| LM393ND | LM393ND | |
| LM393NDS | LM393NDS | |
| LM393NS | LM393NS | |
| LM555CH | MC1455G | |
| LM555CN | MC1455P1 | |
| LM555H | MC1455G | |
| LM556CD | MC3456L | |
| LM556CJ | MC3456L | |
| LM556CN | MC3456P | |
| LM556D | MC3456L | |
| LM556L | MC3456L | |
| LM565CH | | NE565A |
| LM565CN | | NE565A |
| LM565H | | NE565A |
| LM703LN | | MC1350P |
| LM709AH | MC1709AG | |
| LM709CH | MC1709CG | |
| LM709AN-8 | MC1709CP1 | |
| LM709H | MC1709G | |
| LM723CD | LM723CJ | |
| LM723CH | MC1723CG | |
| LM723CJ | MC1723CL | |
| LM723CN | MC1723CP | |
| LM723D | LM723J | |
| LM723H | MC1723G | |
| LM723J | MC1723L | |
| LM733CD | MC1733CL | |
| LM733CH | MC1733CG | |
| LM733CJ | MC1733CL | |
| LM733CN | MC1733CP | |
| LM733D | MC1733L | |
| LM733H | MC1733G | |
| LM733J | MC1733L | |
| LM741AH | | MC1741G |
| LM741CD | LM741CJ | |
| LM741CH | LM741CH | |
| LM741CJ-14 | LC741CJ | |
| LM741CN | LM741CN | |
| LM741EH | | MC1741CG |
| LM741EJ | | MC1741CU |
| LM741EN | | MC1741CP1 |
| LM741H | LM741H | |
| LM747CD | LM747CJ | |
| LM747CH | LM747CH | |
| LM747CJ | LM747CJ | |
| LM747CN | LM747CN | |
| LM747D | LM747J | |
| LM747H | LM747H | |
| LM747J | LM747J | |
| LM748CH | MC1748CG | |
| LM748CJ | MC1748CU | |
| LM748CN | MC1748CP1 | |
| LM748H | MC1748G | |
| LM748J | MC1748U | |
| LM1035 | | TCA5550 |
| LM1351N | | MC1357P |
| LM1391N | MC1391P | |
| LM1394N | MC1394P | |
| LM1408J6 | | LM1408L6 |
| LM1408J7 | | LM1408L7 |
| LM1408J8 | | LM1408L8 |
| LM1408N6 | | LM1408P6 |
| LM1408N7 | | LM1408P7 |
| LM1408N8 | | LM1408P8 |
| LM1414J | MC1414L | |
| LM1414N | MC1414P | |
| LM1458H | MC1458G | |
| LM1458J | MC1458U | |
| LM1458N | MC1458P1 | |
| LM1458N-14 | MC1458P1 | |
| LM1488J | MC1488L | |
| LM1488N | MC1488P | |
| LM1489AJ | MC1489AL | |
| LM1489AN | MC1489AP | |
| LM1489J | MC1489L | |
| LM1489N | MC1489P | |
| LM1496H | MC1496G | |
| LM1496J | MC1496L | |
| LM1496N | MC1496P | |
| LM1514J | MC1514L | |
| LM1558H | MC1558G | |
| LM1558J | MC1558U | |
| LM1596H | MC1596G | |
| LM1596J | MC1596L | |
| LM1822 | | MC13010P |
| LM1841N | | MC1357P |
| LM1849A | | MC3484V2 |
| LM1889 | | MC1374P |
| LM1900D | | MC3301L |
| LM1981 | | MC13020P |
| LM1989 | | MC1372P |
| LM2111N | MC1357P | |
| LM2113N | | MC1357P |
| LM2900N | LM2900N | MC3301P |
| LM2901D | LM2901D | |
| LM2901N | LM2901N | |
| LM2901ND | LM2901ND | |
| LM2901NDS | LM2901NDS | |
| LM2901NS | LM2901NS | |
| LM2902D | LM2902D | |
| LM2902J | LM2902J | |
| LM2902N | LM2902N | |
| LM2903 | LM2903N | |
| LM2903D | LM2903D | |
| LM2903JG | LM2903JG | |
| LM2903N | LM2903N | |
| LM2903P | LM2903N | |
| LM2903U | LM2903U | |
| LM2904D | LM2904D | |
| LM2904H | LM2904H | |
| LM2904J | LM2904J | |
| LM2904N | LM2904N | |
| LM2905N | | MC1455P1 |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| LM3026 | | CA3054 |
| LM3045 | | MC3346P |
| LM3046N | MC3346P | |
| LM3054 | CA3054 | |
| LM3064N | | MC13010P |
| LM3065N | MC1358P | |
| LM3086N | MC3386P | |
| LM3089 | | MC3356P |
| LM3146 | | MC3346P |
| LM3146A | | MC3346P |
| LM3189 | | MC3356P |
| LM3301N | MC3301P | |
| LM3302 | MC3302P | |
| LM3302J | MC3302L | |
| LM3302N | MC3302P | |
| LM3401N | MC3401P | |
| LM3900N | LM3900N | MC3401P |
| LM3905 | | MC1455P1 |
| LM3905N | | MC1455P1 |
| LM4250CH | | MC1776CG |
| LM4250CN | | MC1776CP1 |
| LM4250H | | MC1776G |
| LM4500A | TCA4500A | |
| LM7805CK | MC7805CK | |
| LM7805CT | MC7805CT | |
| LM7805KC | MC7805CK | |
| LM7806KC | MC7806CK | |
| LM7808KC | MC7808CK | |
| LM7812CK | MC7812CK | |
| LM7812CT | MC7812CT | |
| LM7812KC | MC7812CK | |
| LM7815CK | MC7815CK | |
| LM7815CT | MC7815CT | |
| LM7815KC | MC7815CK | |
| LM7818KC | MC7818CK | |
| LM7824KC | MC7824CK | |
| LM7905CK | MC7905CK | |
| LM7905CT | MC7905CT | |
| LM7912CK | MC7912CK | |
| LM7912CT | MC7912CT | |
| LM7915CK | MC7915CK | |
| LM7915CT | MC7915CT | |
| LM78L05ACH | MC78L05ACG | |
| LM78L05ACZ | MC78L05ACP | |
| LM78L05CH | MC78L05CG | |
| LM78L05CZ | MC78L05CP | |
| LM78L08ACH | MC78L08ACG | |
| LM78L08ACZ | MC78L08ACP | |
| LM78L08CH | MC78L08CG | |
| LM78L08CZ | MC78L08CP | |
| LM78L12ACH | MC78L12ACG | |
| LM78L12ACZ | MC78L12ACP | |
| LM78L12CH | MC78L12CG | |
| LM78L12CZ | MC78L12CP | |
| LM78L15ACH | MC78L15ACG | |
| LM78L15ACZ | MC78L15ACP | |
| LM78L15CH | MC78L15CG | |
| LM78L15CZ | MC78L15CP | |
| LM78L18ACH | MC78L18ACG | |
| LM78L18ACZ | MC78L18ACP | |
| LM78L18CH | MC78L18CG | |
| LM78L18CZ | MC78L18CP | |
| LM78L24ACH | MC78L24ACG | |
| LM78L24ACZ | MC78L24ACP | |
| LM78L24CH | MC78L24CG | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| LM78L24CZ | MC78L24CP | |
| LM78M05CP | | MC78M05CT |
| LM78M12CP | | MC78M12CT |
| LM78M15CP | | MC78M15CT |
| LM79L05ACZ | MC79L05ACP | |
| LM79L12ACZ | MC79L12ACP | |
| LM79L15ACZ | MC79L15ACP | |
| LM79M05CP | | MC79M05CT |
| LM79M12CP | | MC79M12CT |
| LM79M15CP | | MC79M15CT |
| LM55109J | | MC75S110L |
| LM55110J | | MC75S110L |
| LM75107AN | MC75107P | |
| LM75108AJ | MC75108L | |
| LM75108AN | MC75108P | |
| LM75110J | MC75S110L | |
| LM75110N | MC75S110P | |
| LM75207L | | MC75107L |
| LM75207N | | MC75107P |
| LM75208J | | MC75108L |
| LM75208N | | MC75108P |
| MB3759 | TL494CN | |
| MB3760 | TL495CN | |
| MC1310A | MC1310P | |
| MC1330A1P | MC1330A1P | |
| MC1330A2P | MC1330A2P | |
| MC1349P | MC1349P | |
| MC1350P | MC1350P | |
| MC1352P | MC1352P | |
| MC1355P | MC1355P | |
| MC1357P | MC1357P | |
| MC1358P | MC1358P | |
| MC1372P | MC1372P | |
| MC1373P | MC1373P | |
| MC1374P | MC1374P | |
| MC1376P | MC1376P | |
| MC1377P | MC1377P | |
| MC1378P | MC1378P | |
| MC1391P | MC1391P | |
| MC1394P | MC1394P | |
| MC1400G2 | MC1400G2 | |
| MC1400G5 | MC1400G5 | |
| MC1400G6 | MC1400G6 | |
| MC1400G10 | MC1400G10 | |
| MC1408B | MC1408P8 | |
| MC1408FB | MC1408L8 | |
| MC1411P | MC1411P | |
| MC1412P | MC1412P | |
| MC1413P | MC1413P | |
| MC1413PD | MC1413PD | |
| MC1413PDS | MC1413PDS | |
| MC1413PS | MC1413PS | |
| MC1416P | MC1416P | |
| MC1416PDS | MC1416PDS | |
| MC1458JG | MC1458U | |
| MC1458L | MC1458G | |
| MC1458P | MC1458P1 | |
| MC1472P1 | MC1472P1 | |
| MC1472U | MC1472U | |
| MC1488L | MC1488L | |
| MC1488LD | MC1488LD | |
| MC1488LDS | MC1488LDS | |
| MC1488LS | MC1488LS | |
| MC1488P | MC1488P | |
| MC1488PD | MC1488PD | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| MC1488PDS | MC1488PDS | |
| MC1488PS | MC1488PS | |
| MC1489AL | MC1489AL | |
| MC1489ALD | MC1489ALD | |
| MC1489ALDS | MC1489ALDS | |
| MC1489ALS | MC1489ALS | |
| MC1489AP | MC1489AP | |
| MC1489APD | MC1489APD | |
| MC1489APDS | MC1489APDS | |
| MC1489APS | MC1489APS | |
| MC1489L | MC1489L | |
| MC1489LD | MC1489LD | |
| MC1489LDS | MC1489LDS | |
| MC1489LS | MC1489LS | |
| MC1489N | MC1489P | |
| MC1489N3 | MC1489PDS | |
| MC1489P | MC1489P | |
| MC1489PD | MC1489PD | |
| MC1489PDS | MC1489PDS | |
| MC1489PS | MC1489PS | |
| MC1545J | MC1545L | |
| MC3446J | | MC3446AP |
| MC3446N | MC3446AP | |
| MC3460P | DS3674N | |
| MC3470N | MC3470P | MC3470AP |
| MC3481J | MC3481L | |
| MC3481N | MC3481P | |
| MC3485J | MC3485L | |
| MC3485N | MC3485P | |
| MC3486J | MC3486L | |
| MC3486N | MC3486P | |
| MC3487J | MC3487L | |
| MC3487N | MC3487P | |
| MP562KD | AD562AKD | |
| MP562SD | AD562ASD | |
| MP5531AJ | MC1500AG5 | |
| MP5531BJ | MC1500G5 | |
| MP5531CP | MC1404U5 | |
| MP5531DP | MC1404U5 | |
| MP5531EJ | MC1400AG5 | |
| MP5531HJ | MC1400G5 | |
| MP5532AJ | MC1500AG10 | |
| MP5532BJ | MC1500G10 | |
| MP5532CP | MC1404U10 | |
| MP5532DP | MC1404U10 | |
| MP5532EJ | MC1400AG10 | |
| MP5532HJ | MC1400G10 | |
| N8T15A | | MC1488L |
| N8T15F | | MC1488L |
| N8T16A | | MC1489L |
| N8T26AB | MC8T26AP | |
| N8T26AE | MC8T26AL | |
| N8T26AJ | MC8T26AL | |
| N8T26AN | MC8T26AP | |
| N8T26B | MC8T26AP | |
| N8T26J | MC8T26AL | |
| N8T26N | MC8T26AP | |
| N8T28B | MC8T28P | |
| N8T37A | MC3437P | |
| N8T95B | MC8T95P | |
| N8T95F | MC8T95L | |
| N8T96B | MC8T96P | |
| N8T96F | MC8T96L | |
| N8T97B | MC8T97P | |
| N8T97F | MC8T97L | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| N8T98B | MC8T98P | |
| N8T98F | MC8T98L | |
| N5065A | MC1358P | |
| N5556T | MC1456G | |
| N5556V | MC1456P1 | |
| N5558F | MC1458L | |
| N5558T | MC1458G | |
| N5558V | MC1458P1 | |
| N5595A | MC1495L | |
| N5595F | MC1495L | |
| N5596A | MC1496L | |
| N5596K | MC1496G | |
| N5709A | | MC1709CP1 |
| N5709G | | MC1709CU |
| N5709T | MC1709CG | |
| N5709V | MC1709CP1 | |
| N5723A | | MC1723CP |
| N5723T | MC1723CG | |
| N5723K | MC1733CG | |
| N5741A | | MC1741CP1 |
| N5741T | MC1741CG | |
| N5741V | MC1741CP1 | |
| N5747A | MC1747CL | |
| N5747F | MC1747CL | |
| N5748A | | MC1747CG |
| N5748T | MC1748CG | |
| NE501A | | MC1733CL |
| NE501K | | MC1733CG |
| NE531G | | MC1439G |
| NE531T | | MC1439G |
| NE531V | | MC1439P |
| NE533G | | MC1776CG |
| NE533T | | MC1776CG |
| NE533V | | MC1776CG |
| NE537G | | MC1456G |
| NE537T | | MC1456G |
| NE540L | | MC1554G |
| NE550A | | MC1723CP |
| NE550L | | MC1723CG |
| NE555JG | MC1455U | |
| NE555L | MC1455G | |
| NE555P | MC1455P1 | |
| NE555T | MC1455G | |
| NE555V | MC1455P1 | |
| NE556A | MC3456P | |
| NE556I | MC3456L | |
| NE565A | | NE565A |
| NE565K | | NE565A |
| NE592A | NE592A | |
| NE592K | NE592K | |
| NE5118F | | MC6890L |
| NE5118N | | MC6890L |
| NE5410F | MC3410L | |
| NE5561FE | | MC34060L |
| NE5561N | | MC34060P |
| OP-01C | | MC1536 |
| OP-01G | | MC1536 |
| OP-01H | | MC1536 |
| OP-01J | | MC1536G |
| OP-01L | | MC1536G |
| OP-01P | | MC1436P |
| OP-08 | | MC1776 |
| OP-08A | | MC1776 |
| OP-08B | | MC1776 |
| OP-08C | | MC1776 |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| OP-08E | | MC1776 |
| OP-27AJ | | OP-27AZ |
| OP-27AZ | OP-27AZ | |
| OP-27BJ | | OP-27BZ |
| OP-27BZ | OP-27BZ | |
| OP-27CJ | | OP-27CZ |
| OP-27CZ | OP-27CZ | |
| OP-27EJ | | OP-27EZ |
| OP-27EP | OP-27EP | |
| OP-27EZ | OP-27EZ | |
| OP-27FJ | | OP-27FZ |
| OP-27FP | OP-27FP | |
| OP-27FZ | OP-27FZ | |
| OP-27GJ | | OP-27GZ |
| OP-27GP | OP-27GP | |
| OP-27GZ | OP-27GZ | |
| OP-37AJ | | OP-37AZ |
| OP-37AZ | OP-37AZ | |
| OP-37BJ | | OP-37BZ |
| OP-37BZ | OP-37BZ | |
| OP-37CJ | | OP-37CZ |
| OP-37CZ | OP-37CZ | |
| OP-37EJ | | OP-37EZ |
| OP-37EP | OP-37EP | |
| OP-37EZ | OP-37EZ | |
| OP-37FJ | | OP-37FZ |
| OP-37FP | OP-37FP | |
| OP-37FZ | OP-37FZ | |
| OP-37GJ | | OP-37GZ |
| OP-37GP | OP-37GP | |
| OP-37GZ | OP-37GZ | |
| PWM125AK | SG1525AJ | |
| PWM125BK | SG2525AJ | |
| PWM125CK | SG3525AJ | |
| RC702T | | MC1733C |
| RC709DN | MC1709CP1 | |
| RC709T | MC1709CG | |
| RC723D | MC1723CL | |
| RC723DB | MC1723CP | |
| RC723DC | MC1723CL | |
| RC723T | MC1723CG | |
| RC733D | MC1733CL | |
| RC733T | MC1733CG | |
| RC741DN | MC1741CP1 | |
| RC741T | MC1741CG | |
| RC747D | MC1747CL | |
| RC747T | MC1747CG | |
| RC748T | MC1748CG | |
| RC1414DC | MC1414L | |
| RC1414DP | MC1414P | |
| RC1488DC | MC1488L | |
| RC1489ADC | MC1489AL | |
| RC1489DC | MC1489L | |
| RC1437D | MC1437L | |
| RC1437DP | MC1437P | |
| RC1458DN | MC1458P1 | |
| RC1458T | MC1458G | |
| RC1556T | MC1456CG | |
| RC1558T | MC1558G | |
| RC3302DB | MC3302P | |
| RC4131DP | | MC1471SCP1 |
| RC4131T | | MC1741SG |
| RC4136D | | MC3403L |
| RC4136DP | | MC3403P |
| RC4136J | | MC3403L |
| RC4136N | | MC3403P |
| RC4194DC | | MC1468L |
| RC4195NB | | MC1468L |
| RC4195T | | MC1468G |
| RC4444R | MC3416L | |
| RC4558DN | MC4558CP1 | |
| RC4558JG | MC4558CU | |
| RC4558L | MC4558CG | |
| RC4558P | MC4558CP1 | |
| RC4558T | MC4558CG | |
| RC75107AD | MC75107L | |
| RC75107ADP | MC75107P | |
| RC75108AD | MC75108L | |
| RC75108ADP | MC75108P | |
| RC75109D | | MC75S110L |
| RC75109DP | | MC75S110P |
| RC75110D | MC75S110L | |
| RC75110DP | MC75S110P | |
| REF-01AJ | MC1500AG10 | |
| REF-01AZ | | MC1500AG10 |
| REF-01CJ | | MC1404U10 |
| REF-01CP | MC1404U10 | |
| REF-01CZ | MC1404U10 | |
| REF-01DJ | | MC1404U10 |
| REF-01DP | MC1404U10 | |
| REF-01DZ | MC1404U10 | |
| REF-01EJ | MC1400AG10 | |
| REF-01EZ | | MC1400AG10 |
| REF-01HJ | MC1400G10 | |
| REF-01HP | | MC1400G10 |
| REF-01HZ | | MC1400G10 |
| REF-01J | MC1500G10 | |
| REF-01Z | | MC1500G10 |
| REF-02AJ | MC1500AG5 | |
| REF-02AZ | | MC1500AG5 |
| REF-02CJ | | MC1404U5 |
| REF-02CP | MC1404U5 | |
| REF-02CZ | MC1404U5 | |
| REF-02DJ | | MC1404U5 |
| REF-02DP | MC1404U5 | |
| REF-02DZ | MC1404U5 | |
| REF-02EJ | MC1400AG5 | |
| REF-02EZ | | MC1400AG5 |
| REF-02HJ | MC1400G5 | |
| REF-02HP | | MC1400G5 |
| REF-02HZ | | MC1400G5 |
| REF-02J | MC1500G5 | |
| REF-02Z | | MC1500G5 |
| RM702T | | MC1733 |
| RM709T | MC1709G | |
| RM723D | MC1723L | |
| RM723DC | MC1723L | |
| RM723T | MC1723G | |
| RM733D | MC1733L | |
| RM733T | MC1733G | |
| RM741DP | MC1741P | |
| RM741T | MC1741G | |
| RM747D | MC1747L | |
| RM747T | MC1747G | |
| RM748T | MC1748G | |
| RM1514DC | MC1514L | |
| RM1537D | MC1537L | |
| RM4136D | | MC3503L |
| RM4136J | | MC3503L |
| RM4194DC | | MC1568L |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| RM4195T | | MC1568G |
| RM4558D | MC4558U | |
| RM4558JG | MC4558U | |
| RM4558L | MC4558G | |
| RM4558T | MC4558G | |
| RV3301DB | MC3301P | |
| S5556T | MC1556G | |
| S5558E | MC1558L | |
| S5558T | MC1558G | |
| S5596F | MC1596L | |
| S5596K | MC1596G | |
| S5709G | MC1709U | |
| S5709T | MC1709G | |
| S5723T | MC1723G | |
| S5733K | MC1733G | |
| S5741T | MC1741G | |
| SE501K | | MC1733G |
| SE531G | | MC1539G |
| SE531T | | MC1539G |
| SE533G | | MC1776G |
| SE533T | | MC1776G |
| SE537G | | MC1556G |
| SE537T | | MC1556G |
| SE550L | | MC1723G |
| SE555JG | MC1555U | |
| SE555L | MC1555G | |
| SE555T | MC1555G | |
| SE556A | MC3556L | |
| SE565A | | MLM565CP |
| SE565K | | MLM565CP |
| SE592A | SE592L | |
| SE592K | SE592G | |
| SE5118F | MC6890AL | MC6890AL |
| SE5410F | MC3510L | |
| SE5561FE | | MC35060L |
| SG100T | | MC1723G |
| SG101AD | | LM101AH |
| SG101AT | LM101AH | |
| SG101J | | LM101AH |
| SG101T | LM101AH | |
| SG104T | LM104H | |
| SG105N | | LM105H |
| SG105T | LM105H | |
| SG107J | | MC1741 |
| SG107T | | MC1741 |
| SG108AJ | LM108AJ | |
| SG108AT | LM108AH | |
| SG108J | LM108J | |
| SG108T | LM108H | |
| SG109K | LM109K | |
| SG109R | | MC109K |
| SG109T | LM109H | |
| SG111D | LM111J | |
| SG111T | LM111H | |
| SG117K | LM117K | |
| SG117R | | LM117K |
| SG117T | LM117H | |
| SG118T | | MC1741SG |
| SG123K | LM123K | |
| SG124J | LM124J | |
| SG137K | LM137K | |
| SG137R | | LM137K |
| SG137T | LM137H | |
| SG140K-05 | LM140K-5.0 | |
| SG140K-06 | LM140K-6.0 | |
| SG140K-08 | LM140K-8.0 | |
| SG140K-12 | LM140K-12 | |
| SG140K-15 | LM140K-15 | |
| SG140K-18 | LM140K-18 | |
| SG140K-24 | LM140K-24 | |
| SG150K | LM150K | |
| SG200T | | MC1723G |
| SG201AD | | LM201AH |
| SG201AM | LM201AN | |
| SG201AN | | LM201AN |
| SG201AT | LM201AH | |
| SG201J | | LM201AH |
| SG201M | LM201AN | |
| SG201N | | LM201AN |
| SG201T | LM201AH | |
| SG207J | | MC1741C |
| SG207M | | MC1741C |
| SG207N | | MC1741C |
| SG207T | | MC1741C |
| SG208AJ | LM208AJ | |
| SG208AM | LM208AJ-8 | |
| SG208AT | LM208AH | |
| SG208J | LM208J | |
| SG208M | LM208J-8 | |
| SG208T | LM208H | |
| SG209K | LM209K | |
| SG209R | | MC209K |
| SG209T | LM209H | |
| SG211D | LM211J | |
| SG211M | LM211N | |
| SG211T | LM211H | |
| SG217K | LM217K | |
| SG217R | | LM217K |
| SG217T | LM217H | |
| SG218J | | MC1741SL |
| SG218M | | MC1741SL |
| SG218T | | MC1741SG |
| SG223K | LM223K | |
| SG224J | LM224J | |
| SG224N | LM224N | |
| SG237K | LM237K | |
| SG237R | | LM237K |
| SG237T | LM237H | |
| SG250K | LM250K | |
| SG300N | | MC1723CP |
| SG300T | | MC1723CG |
| SG301AD | | LM301AH |
| SG301AM | LM301AN | |
| SG301AN | | LM301AN |
| SG301AT | LM301AH | |
| SG307J | | LM307N |
| SG307M | LM307N | |
| SG307N | | LM307N |
| SG308AJ | LM308AJ | |
| SG308AM | LM308AN | |
| SG308AT | LM308AH | |
| SG308J | LM308J | |
| SG308M | LM308N | |
| SG308T | LM308H | |
| SG309K | LM309K | |
| SG309P | | LM309K |
| SG309R | | MC309K |
| SG309T | LM309H | |
| SG311D | LM311J | |
| SG311M | LM311N | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| SG311T | LM311H | |
| SG317K | LM317K | |
| SG317P | LM317T | |
| SG317R | | LM317T |
| SG317T | LM317H | |
| SG318J | | MC1741SCL |
| SG318M | | MC1741CP1 |
| SG318T | | MC1741CG |
| SG324J | LM324J | |
| SG324N | LM324N | |
| SG337K | LM337K | |
| SG337P | LM337T | |
| SG337R | | LM337T |
| SG337T | LM337H | |
| SG340K-05 | LM340K-5.0 | |
| SG340K-06 | LM340K-6.0 | |
| SG340K-08 | LM340K-8.0 | |
| SG340K-12 | LM340K-12 | |
| SG340K-15 | LM340K-15 | |
| SG340K-18 | LM340K-18 | |
| SG340K-24 | LM340K-24 | |
| SG350K | LM350K | |
| SG501AJ | | MC1468G |
| SG555CM | MC1455P1 | |
| SG555CT | MC1455G | |
| SG555T | MC1555G | |
| SG556CJ | MC3456L | |
| SG556CN | MC3456P | |
| SG556J | MC3556L | |
| SG556N | MC3556L | |
| SG723CD | MC1723CL | |
| SG723CJ | MC1723CL | |
| SG723CN | MC1723CP | |
| SG723CT | MC1723CG | |
| SG723D | MC1723L | |
| SG723J | MC1723L | |
| SG723T | MC1723G | |
| SG733CD | MC1733CL | |
| SG733CN | | MC1733CP |
| SG733CT | MC1733CG | |
| SG733D | MC1733L | |
| SG733N | | MC1733L |
| SG733T | MC1733G | |
| SG741CM | MC1741CP1 | |
| SG741CT | MC1741CG | |
| SG741SCM | MC1741SCP1 | |
| SG741SCT | MC1741SCG | |
| SG741ST | MC1741SG | |
| SG741T | MC1741G | |
| SG747CJ | MC1747CL | |
| SG747CN | MC1747CP2 | |
| SG747CT | MC1747CG | |
| SG747J | MC1747L | |
| SG747T | MC1747G | |
| SG748CD | | MC1748CP1 |
| SG748CM | | MC1748CP1 |
| SG748CN | | MC1748CP1 |
| SG748CT | MC1748CG | |
| SG748D | | MC1748G |
| SG748T | MC1748G | |
| SG777CJ | | LM308AJ |
| SG777CM | | LM308AN |
| SG777CN | | LM308AN |
| SG777CT | | LM308AH |
| SG777J | | LM108AJ |
| SG777T | | LM108AH |
| SG1118AJ | | LM108AJ |
| SG1118AT | | LM108AH |
| SG1118J | | LM108J |
| SG1118T | | LM108H |
| SG1217 | | MC1741G |
| SG1217T | | MC1741SG |
| SG1250T | | MC1776G |
| SG1402N | | MC1594L |
| SG1402T | | MC1594L |
| SG1436CT | MC1436CG | |
| SG1436M | MC1436U | |
| SG1436T | MC1436G | |
| SG1456CT | MC1456CG | |
| SG1456T | MC1456G | |
| SG1458M | MC1458P1 | |
| SG1458T | MC1458G | |
| SG1468J | MC1468L | |
| SG1468N | | MC1468L |
| SG1468T | MC1468G | |
| SG1495D | MC1495L | |
| SG1495N | MC1495L | |
| SG1496D | MC1496L | |
| SG1496N | | MC1496L |
| SG1496T | MC1496G | |
| SG1501AD | | MC1568L |
| SG1501AJ | | MC1568L |
| SG1501AT | | MC1568G |
| SG1501J | MC1568L | |
| SG1501T | MC1568G | |
| SG1502D | | MC1568L |
| SG1502J | | MC1568L |
| SG1502N | | MC1568L |
| SG1503 | MC1503U | |
| SG1503T | | MC1503U |
| SG1503Y | | MC1503U |
| SG1524J | | TL494MJ |
| SG1525AJ | SG1525AJ | |
| SG1526J | SG1526J | |
| SG1527AJ | SG1527AJ | |
| SG1536T | MC1536G | |
| SG1542J | | MC3524L |
| SG1543J | | MC3524L |
| SG1544J | | MC3424AL |
| SG1556T | MC1556G | |
| SG1558T | MC1558G | |
| SG1568J | MC1568L | |
| SG1568T | MC1568G | |
| SG1595D | MC1595L | |
| SG1596D | MC1596L | |
| SG1596T | MC1596G | |
| SG1660D | | LM301AH |
| SG1660J | | LM308J |
| SG1660M | | LM308N |
| SG1660T | | LM308H |
| SG1760J | | LM308J |
| SG1760M | | LM308N |
| SG1760T | | LM308H |
| SG2118AJ | | LM208AJ |
| SG2118AM | | LM208AJ-8 |
| SG2118AT | | LM208AH |
| SG2118J | | LM208J |
| SG2118M | | LM208J-8 |
| SG2118T | | LM208H |
| SG2250T | | MC1776G |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| SG2402N | | MC1494L |
| SG2402T | | MC1494L |
| SG2501AD | | MC1468L |
| SG2501AT | | |
| SG2501D | MC1468L | |
| SG2501J | MC1468L | |
| SG2501N | MC1468L | |
| SG2501T | MC1468G | |
| SG2502J | | MC1468L |
| SG2502N | | MC1468L |
| SG2503 | MC1403AU | |
| SG2503M | | MC1403AU |
| SG2503T | | MC1403AU |
| SG2503Y | | MC1403AU |
| SG2524J | | TL494IJ |
| SG2525AJ | SG2525AJ | |
| SG2526J | SG2526J | |
| SG2527AJ | SG2527AJ | |
| SG2542J | | MC3324L |
| SG2542N | | MC3324P |
| SG2543J | | MC3324L |
| SG2544J | | MC3324AL |
| SG3118AJ | | LM308AJ |
| SG3118AM | | LM308AN |
| SG3118AT | | LM308AH |
| SG3118J | | LM308J |
| SG3118M | | LM308N |
| SG3118T | | LM308H |
| SG3250T | | MC1776G |
| SG3402N | | MC1494L |
| SG3402T | | MC1494L |
| SG3423M | | MC3423P1 |
| SG3423Y | | MC3423U |
| SG3501AD | MC1468L | |
| SG3501AJ | MC1468L | |
| SG3501AN | | MC1468L |
| SG3501AT | MC1468G | |
| SG3501J | MC1468L | |
| SG3501D | MC1468L | |
| SG3501N | MC1468L | |
| SG3501T | MC1468G | |
| SG3502D | | MC1468L |
| SG3502G | | MC1468G |
| SG3502J | | MC1468L |
| SG3502N | | MC1468L |
| SG3503 | MC1403U | |
| SG3503M | | MC1403U |
| SG3503T | | MC1403U |
| SG3503Y | MC1403U | |
| SG3523Y | | MC3523U |
| SG3524J | | MC3420L |
| SG3525AJ | SG3525AJ | |
| SG3525AN | SG3525AN | |
| SG3526J | SG3526J | |
| SG3527AJ | SG3527AJ | |
| SG3527AN | SG3527AN | |
| SG3542J | | MC3424L |
| SG3542N | | MC3424P |
| SG3543J | | MC3424L |
| SG3544J | | MC3424AL |
| SG4194CJ | | MC1468L |
| SG4194J | | MC1568L |
| SG4250CM | | MC1776CP1 |
| SG4250CT | | MC1776CG |
| SG4250T | | MC1776G |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| SG4501D | MC1468L | |
| SG4501J | | MC1468L |
| SG4501N | | MC1468L |
| SG4501T | | MC1468G |
| SG7805ACK | MC7805ACK | |
| SG7805ACP | MC7805ACT | |
| SG7805ACR | | MC7805ACT |
| SG7805ACT | | MC7805ACT |
| SG7805AK | MC7805AK | |
| SG7805AR | | MC7805AK |
| SG7805AT | | MC7805AK |
| SG7805CK | MC7805CK | |
| SG7805CP | MC7805CT | |
| SG7805CR | | MC7805CT |
| SG7805CT | | MC78M05CG |
| SG7805K | MC7805K | |
| SG7805R | | MC7805K |
| SG7805T | | MC7805K |
| SG7806ACK | MC7806ACK | |
| SG7806ACP | MC7806ACT | |
| SG7806ACR | | MC7806ACT |
| SG7806ACT | | MC7806ACT |
| SG7806AK | MC7806AK | |
| SG7806AR | | MC7806AK |
| SG7806AT | | MC7806AK |
| SG7806CK | MC7806CK | |
| SG7806CP | MC7806CT | |
| SG7806CR | | MC7806CT |
| SG7806CT | | MC78M06CG |
| SG7806K | MC7806K | |
| SG7806R | | MC7806K |
| SG7806T | | MC7806K |
| SG7808ACK | MC7808ACK | |
| SG7808ACP | MC7808ACT | |
| SG7808ACR | | MC78M08ACT |
| SG7808ACT | | MC7808ACT |
| SG7808AK | MC7808AK | |
| SG7808AR | | MC7808AK |
| SG7808AT | | MC7808AK |
| SG7808CK | MC7808CK | |
| SG7808CP | MC7808CT | |
| SG7808CR | | MC7808CT |
| SG7808CT | | MC7808CG |
| SG7808K | MC7808K | |
| SG7808R | | MC7808K |
| SG7808T | | MC7808K |
| SG7812ACK | MC7812ACK | |
| SG7812ACP | MC7812ACT | |
| SG7812ACR | | MC7812ACT |
| SG7812ACT | | MC7812ACT |
| SG7812AK | MC7812AK | |
| SG7812AR | | MC7812AK |
| SG7812AT | | MC7812AK |
| SG7812CK | MC7812CK | |
| SG7812CP | MC7812CT | |
| SG7812CR | | MC7812CT |
| SG7812CT | | MC78M12CG |
| SG7812K | MC7812K | |
| SG7815ACK | MC7815ACK | |
| SG7815ACP | MC7815ACT | |
| SG7815ACR | | MC7815ACT |
| SG7815ACT | | MC7815ACT |
| SG7815AK | MC7815AK | |
| SG7815AR | | MC7815AK |
| SG7815AT | | MC7815AK |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| SG7815CK | MC7815CK | |
| SG7815CP | MC7815CT | |
| SG7815CR | | MC7815CT |
| SG7815CT | | MC78M15CG |
| SG7815K | MC7815K | |
| SG7815R | | MC7815K |
| SG7815T | | MC7815K |
| SG7818ACK | MC7818ACK | |
| SG7818ACP | MC7818ACT | |
| SG7818ACR | | MC7818ACT |
| SG7818ACT | | MC7818ACT |
| SG7818AK | MC7818AK | |
| SG7818AR | | MC7818AK |
| SG7818AT | | MC7818AK |
| SG7818CK | MC7818CK | |
| SG7818CP | MC7818CT | |
| SG7818CR | | MC7818CT |
| SG7818CT | | MC7818CG |
| SG7818K | MC7818K | |
| SG7818R | | MC7818K |
| SG7818T | | MC7818K |
| SG7824ACK | MC7824ACK | |
| SG7824ACP | MC7824ACT | |
| SG7824ACR | | MC7824ACT |
| SG7824ACT | | MC7824ACT |
| SG7824AK | MC7824AK | |
| SG7824AR | | MC7824AK |
| SG7824AT | | MC7824AK |
| SG7824CK | MC7824CK | |
| SG7824CP | MC7824CT | |
| SG7824CR | | MC7824CT |
| SG7824CT | | MC78M24CG |
| SG7824K | MC7824K | |
| SG7824R | | MC7824K |
| SG7824T | | MC7824K |
| SG7905ACK | MC7905ACK | |
| SG7905ACP | MC7905ACT | |
| SG7905ACR | | MC7905ACT |
| SG7905ACT | | MC7905ACT |
| SG7905CK | | MC7905CK |
| SG7905CP | MC7905CT | |
| SG7905CR | | MC7905CT |
| SG7905CT | | MC7905CT |
| SG7905.2CK | MC7905.2CK | |
| SG7905.2CP | MC7905.2CT | |
| SG7905.2CR | | MC7905.2CT |
| SG7905.2CT | | MC7905.2CT |
| SG7908CK | MC7908CK | |
| SG7908CP | MC7908CT | |
| SG7908CR | | MC7908CT |
| SG7908CT | | MC7908CT |
| SG7912ACK | MC7912ACK | |
| SG7912ACP | MC7912ACT | |
| SG7912ACR | | MC7912ACT |
| SG7912ACT | | MC7912ACT |
| SG7912CK | MC7912CK | |
| SG7912CP | MC7912CT | |
| SG7912CR | | MC7912CT |
| SG7912CT | | MC7912CT |
| SG7915ACK | MC7915ACK | |
| SG7915ACP | MC7915ACT | |
| SG7915ACR | | MC7915ACT |
| SG7915ACT | | MC7915ACT |
| SG7915CK | MC7915CK | |
| SG7915CP | MC7915CT | |
| SG7915CR | | MC7915CT |
| SG7915CT | | MC7915CT |
| SG7918CK | MC7918CK | |
| SG7918CP | MC7918CT | |
| SH323SKC | LM323K | |
| SH8090FM | | MC1508L8 |
| SN52101AL | LM101AH | |
| SN52104L | LM101H | |
| SN52107L | | MC1741 |
| SN52108AL | LM108AH | |
| SN52108L | LM108H | |
| SN52109L | LM109H | |
| SN52514J | MC1514L | |
| SN52555L | MC1555G | |
| SN52558L | MC1558G | |
| SN52702AJ | | MC1733 |
| SN52702AL | | MC1733 |
| SN52702FA | | MC1733 |
| SN52702J | | MC1733 |
| SN52702L | | MC1333 |
| SN52709AL | MC1709AG | |
| SN52709L | MC1709G | |
| SN52723J | MC1723L | |
| SN52723L | MC1723G | |
| SN52733J | MC1733L | |
| SN52733L | MC1733G | |
| SN52741L | MC1741G | |
| SN52747J | MC1747L | |
| SN52747L | MC1747G | |
| SN52748L | MC1748G | |
| SN52770L | | MC1556G |
| SN52771L | | MC1556G |
| SN55108BJ | | MC75108L |
| SN55109J | | MC75S110L |
| SN55110J | | MC75S110L |
| SN55244J | MC1544L | |
| SN72L022P | | LM358N |
| SN72L044JA | | LM324N |
| SN72L044N | | LM324N |
| SN72301AL | LM301AH | |
| SN72301AP | LM301AN | |
| SN72308AL | LM308AH | |
| SN72308L | LM308H | |
| SN72309L | LM309H | |
| SN72311L | LM311H | |
| SN72311P | LM311N | |
| SN72514J | | MC1414L |
| SN72514N | | MC1414P |
| SN72555L | MC1455G | |
| SN72555P | MC1455P1 | |
| SN72558L | MC1458G | |
| SN72558P | MC1458P1 | |
| SN72702J | | MC1733C |
| SN72702L | | MC1733C |
| SN72709L | MC1709CG | |
| SN72709P | MC1709CP1 | |
| SN72723J | MC1723CL | |
| SN72723L | MC1723CG | |
| SN72733J | MC1733CL | |
| SN72733L | MC1733CG | |
| SN72741L | MC1741CG | |
| SN72741P | MC1741CP1 | |
| SN72747J | MC1747CL | |
| SN72747L | MC1747CG | |
| SN72747N | MC1747CP2 | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| SN72748L | MC1748CG | |
| SN72748P | MC1748CP1 | |
| SN72770L | | MC1456G |
| SN72771L | | MC1456G |
| SN72905 | MC7905CT | |
| SN72906 | MC7906CT | |
| SN72908 | MC7908CT | |
| SN72912 | MC7912CT | |
| SN72915 | MC7915CT | |
| SN75107AJ | MC75107L | |
| SN75107AN | MC75107P | |
| SN75107BJ | | MC75107L |
| SN75107BN | | MC75107P |
| SN75108AJ | MC75108L | |
| SN75108AN | MC75108P | |
| SN75108BJ | | MC75108L |
| SN75108BN | | MC75108P |
| SN75110AJ | MC75S110L | |
| SN75110AN | MC75S110P | |
| SN75121J | | MC3481/5L |
| SN75121N | | MC3481/5P |
| SN75122J | | SN75125-9L |
| SN75122N | | SN75125-9P |
| SN75125J | MC75125L | |
| SN75125N | MC75125P | |
| SN75126J | | MC3481/5L |
| SN75126N | | MC3481/5P |
| SN75127J | MC75127L | |
| SN75127N | MC75127P | |
| SN75128J | MC75128L | |
| SN75128N | MC75128P | |
| SN75129J | MC75129L | |
| SN75129N | MC75129P | |
| SN75150J | | MC1488L |
| SN75150N | | MC1488P |
| SN75154J | | MC1489L |
| SN75154N | | MC1489P |
| SN75160J | | MC3447L |
| SN75160N | | MC3447P/P3 |
| SN75172J | SN75172J | |
| SN75172NG | SN75172NG | |
| SN75173J | SN75173J | |
| SN75173N | SN75173N | |
| SN75174J | SN75174J | |
| SN75174NG | SN75174NG | |
| SN75175J | SN75175J | |
| SN75175N | SN75175N | |
| SN75176JG | SN75176JG* | |
| SN75176P | SN75176P* | |
| SN75177JG | SN75177JG* | |
| SN75177P | SN75177P* | |
| SN75178JG | SN75178JG* | |
| SN75178P | SN75178P* | |
| SN75188J | MC1488L | |
| SN75188N | MC1488P | |
| SN75188N3 | MC1488PDS | |
| SN75189AJ | MC1489AL | |
| SN75189AJ4 | MC1489ALDS | |
| SN75189AN | MC1489AP | |
| SN75189J | MC1489L | |
| SN75189J4 | MC1489LDS | |
| SN75189N | MC1489P | |
| SN75189N3 | MC1489PDS | |
| SN75207J | | MC75107L |
| SN75207N | | MC75107P |
| SN75208J | | MC75108L |
| SN75208N | | MC75108P |
| SN75251N | | MC3471P |
| SN75466J | MC1411L | |
| SN75466N | MC1411P | |
| SN75467J | MC1412L | |
| SN75467N | MC1412P | |
| SN75468J | MC1413L | |
| SN75468N | MC1413P | |
| SN75475JG | MC1472U | |
| SN75475P | MC1472P1 | |
| SN75491AN | MC75491P | |
| SN75491N | MC75491P | |
| SN75492AN | MC75492P | |
| SN75492N | MC75492P | |
| SN76298N | MC1398P | |
| SN76514L | | MC1496G |
| SN76514N | MC1496P | |
| SN76564N | | MC13010P |
| SN76565N | | MC13010P |
| SN76591P | MC1391P | |
| SN76594P | MC1394P | |
| SN76600P | MC1350P | |
| SN76642N | MC1357P | |
| SN76644N | | MC1352P |
| SN76650N | MC1352P | |
| SN76651N | | MC1357P |
| SN76653N | | MC1352P |
| SN76660N | | MC1357P |
| SN76665N | | MC13010P |
| SN76666N | MC1358P | |
| SN76669N | | MC1357P |
| SN76678P | | MC1355P |
| SSS101AL | | LM101AH |
| SSS101AJ | LM101AH | |
| SSS107J | | MC1741 |
| SSS107P | | MC1741 |
| SSS201AJ | LM201AH | |
| SSS201AL | | LM201AH |
| SSS201AP | | LM201AN |
| SSS207J | | MC1741C |
| SSS207P | | MC1741C |
| SSS301AJ | LM301AH | |
| SSS301AL | | LM301AH |
| SSS301AP | LM301AN | |
| SSS741BJ | | MC1741G |
| SSS741CJ | | MC1741CG |
| SSS741GJ | MC1741SG | |
| SSS741GP | | MC1741SG |
| SSS741J | | MC1741G |
| SSS747BP | | MC1747L |
| SSS747CK | | MC1747CG |
| SSS747CM | | MC1747CF |
| SSS747CP | | MC1747CL |
| SSS747GK | | MC1747G |
| SSS747GP | | MC1747L |
| SSS747P | | MC1747L |
| SSS1408A-6Z | MC1408L6 | |
| SSS1408A-7Z | MC1408L7 | |
| SSS1408A-8Z | MC1408L8 | |
| SSS1458J | MC1458G | |
| SSS1508A-8Z | MC1508L8 | |
| SSS1558J | MC1558G | |
| TBA120 | | TBA120C |
| TBA440 | | MC13010P |

*To be introduced.

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| TBA920 | | MC1391P |
| TBA920S | | MC1391P |
| TBA1440 | | MC13010P |
| TCA4500A | TCA4500A | |
| TDA1085 | TDA1085 | |
| TDA1524 | | TCA5550 |
| TDA2540 | | MC13010P |
| TDA2544 | | MC13010P |
| TDA3780 | | MC1376P |
| TDA4420 | | MC13010P |
| TDA4600 | TDA4600 | |
| TDA5600 | | MC13010P |
| TDC1027J7 | | MC10315L |
| TL022CJG | | LM358J |
| TL022CL | | LM358H |
| TL022CP | | LM358N |
| TL022MJG | | LM158J |
| TL022ML | | LM158H |
| TL044CJ | | LM324J |
| TL044CN | | LM324N |
| TL044MJ | | LM124J |
| TL071ACJG | TL071ACJG | |
| TL071ACP | TL071ACP | |
| TL071BCJG | TL071BCJG | |
| TL071BCP | TL071BCP | |
| TL071CJG | TL071CJG | |
| TL071CP | TL071CP | |
| TL072ACJG | TL072ACJG | |
| TL072ACP | TL072ACP | |
| TL072BCJG | TL072BCJG | |
| TL072BCP | TL072BCP | |
| TL072CJG | TL072CJG | |
| TL072CP | TL072CP | |
| TL074ACJ | TL074ACJ | |
| TL074ACN | TL074ACN | |
| TL074BCJ | TL074BCJ | |
| TL074BCN | TL074BCN | |
| TL074CJ | TL074CJ | |
| TL074CN | TL074CN | |
| TL081ACJG | TL081ACJG | |
| TL081ACP | TL081ACP | |
| TL081BCJG | TL081BCJG | |
| TL081BCP | TL081BCP | |
| TL081CJG | TL081CJG | |
| TL081CP | TL081CP | |
| TL082ACJG | TL082ACJG | |
| TL082ACP | TL082ACP | |
| TL082BCJG | TL082BCJG | |
| TL082BCP | TL082BCP | |
| TL082CJG | TL082CJG | |
| TL082CP | TL082CP | |
| TL084ACJ | TL084ACJ | |
| TL084ACN | TL084ACN | |
| TL084BCJ | TL084BCJ | |
| TL084BCN | TL084BCN | |
| TL084CJ | TL084CJ | |
| TL084CN | TL084CN | |
| TL431CJG | TL431CJG | |
| TL431CLP | TL431CLP | |
| TL431CP | TL431CP | |
| TL431IJG | TL431IJG | |
| TL431IP | TL431IP | |
| TL431ILP | TL431ILP | |
| TL431MJG | TL431MJG | |
| TL494CJ | TL494CJ | |
| TL494CN | TL494CN | |
| TL494IJ | TL494IJ | |
| TL494IN | TL494IN | |
| TL494MJ | TL494MJ | |
| TL495CJ | TL495CJ | |
| TL495CN | TL495CN | |
| TL495IJ | TL495IJ | |
| TL495IN | TL495IN | |
| TL497CJ | | MC34063U |
| TL497CN | | MC34063P1 |
| TL497MJ | | MC35063U |
| TL514MJ | MC1514L | |
| TL780-05CKC | TL780-05CKC | |
| TL780-12CKC | TL780-12CKC | |
| TL780-15CKC | TL780-15CKC | |
| TL7805ACKC | MC7805ACT | |
| UC117K | LM117K | |
| UC137K | LM137K | |
| UC150K | LM150K | |
| UC217K | LM217K | |
| UC237K | LM237K | |
| UC250K | LM250K | |
| UC317K | LM317K | |
| UC317T | LM317T | |
| UC337K | LM337K | |
| UC337T | LM337T | |
| UC350K | LM350K | |
| UC1525AJ | SG1525AJ | |
| UC1526J | SG1526J | |
| UC1527AJ | SG1527AJ | |
| UC2525AJ | SG2525AJ | |
| UC2526J | SG2526J | |
| UC2526N | SG2526N | |
| UC2527AJ | SG2527AJ | |
| UC3525AJ | SG3525AJ | |
| UC3525AN | SG3525AN | |
| UC3526J | SG3526J | |
| UC3526N | SG3526N | |
| UC3527AJ | SG3527AJ | |
| UC3527AN | SG3527AN | |
| UDN5711M | MC1471P1 | |
| UDN5712M | MC1472P1 | |
| UDN5713M | MC1473P1 | |
| UDN5714M | MC1474P1 | |
| ULN2001A | ULN2001A | |
| ULN2001AN | MC1411P | |
| ULN2002A | ULN2002A | |
| ULN2002AJ | MC1412L | |
| ULN2002AN | MC1412P | |
| ULN2003A | ULN2003A | |
| ULN2003AJ | MC1413L | |
| ULN2003AJ4 | MC1413LDS | |
| ULN2003AN | MC1413P | |
| ULN2003AN3 | MC1413PDS | |
| ULN2004A | ULN2004A | |
| ULN2004AJ | MC1416L | |
| ULN2004AJ4 | MC1416LDS | |
| ULN2004AN | MC1416P | |
| ULN2004AN3 | MC1416PDS | |
| ULN2064NE | ULN2064B | |
| ULN2065NE | ULN2065B | |
| ULN2066NE | ULN2065B | |
| ULN2067NE | ULN2066B | |
| ULN2068B | ULN2068B | |
| ULN2068NE | ULN2068B | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| ULN2069NE | ULN2069B | |
| ULN2074B | ULN2074B | |
| ULN2074NE | ULN2074B | |
| ULN2111A | MC1357P | |
| ULN2113A | | MC1357P |
| ULN2113N | | MC1357P |
| ULN2136A | | MC1357P |
| ULN2139D | | MC1439G |
| ULN2139G | | MC1439G |
| ULN2139H | | MC1439P2 |
| ULN2139M | | MC1439P1 |
| ULN2151D | | MC1741CG |
| ULN2151G | | MC1741CF |
| ULN2151H | | MC1741CP1 |
| ULN2151M | | MC1741CP1 |
| ULN2156D | | MC1456G |
| ULN2156G | | MC1456G |
| ULN2156H | | MC1456G |
| ULN2156M | | MC1456G |
| ULN2157K | | MC1458G |
| ULN2165A | MC1358P | |
| ULN2209A | | MC1357P |
| ULN2244A | | MC1310P |
| ULN2264A | | MC13010P |
| ULN2741D | | M 1741CG |
| ULN2747A | | MC1747CL |
| ULN2801A | ULN2801A | |
| ULN2802A | ULN2802A | |
| ULN2803A | ULN2803A | |
| ULN2804A | ULN2804A | |
| ULN8126A | SG3526N | |
| ULN8126R | SG3526J | |
| ULQ8126A | SG2526N | |
| ULQ8126R | SG2526J | |
| ULS2139D | | MC1539G |
| ULS2139G | | MC1539G |
| ULS2139H | | MC1539L |
| ULS2139M | | MC1439P1 |
| ULS2151D | | MC1741G |
| ULS2151M | | MC1741CP1 |
| ULS2156D | | MC1556G |
| ULS2156G | | MC1556G |
| ULS2156H | | MC1556G |
| ULS2156M | | MC1556G |
| ULS2157A | | MC1558L |
| ULS2157H | | MC1558L |
| ULS2157K | | MC1558G |
| ULS8126R | SG1526J | |
| ULX8161M | | MC34060P |
| XR082CN | TL082CJG | |
| XR082CP | TL082CP | |
| XR082M | TL082MJG | |
| XR084CN | TL084CJ | |
| XR084CP | TL084CN | |
| XR084M | TL084MJ | |
| XR3470A | MC3470AP | |
| μA0802DC-1 | MC1408L8 | |
| μA0802DC-2 | MC1408L7 | |
| μA0802DC-3 | MC1408L6 | |
| μA0802DM-1 | MC1508L8 | |
| μA0802PC-1 | MC1408P8 | |
| μA0802PC-2 | MC1408P7 | |
| μA0802PC-3 | MC1408P6 | |
| μA78GHM | | LM117K |
| μA78GKC | | LM117K |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| μA78GKM | | LM117K |
| μA78GUC | | LM317T |
| μA78GU1C | | LM317T |
| μA78H05KC | | MC7805CK |
| μA78L02ACJG | | MC78L02ACG |
| μA78L05ACJG | | MC78L05ACG |
| μA78L05ACLP | MC78L05ACP | |
| μA78L05AHC | MC78L05ACG | |
| μA78L05AWC | MC78L05ACP | |
| μA78L05CJG | | MC78L05CG |
| μA78L05CLP | MC78L05CP | |
| μA78L05HC | MC78L05CG | |
| μA78L05WC | MC78L05CP | |
| μA78L06ACJG | | MC78L06ACG |
| μA78L06ACLP | MC78L06ACP | |
| μA78L06CJG | | MC78L06CG |
| μA78L06CLP | MC78L06CP | |
| μA78L08ACJG | | MC78L08ACG |
| μA78L08ACLP | | MC78L08ACP |
| μA78L08AWC | MC78L08ACP | |
| μA78L08CJG | | MC78L08CG |
| μA78L08CLP | MC78L08CP | |
| μA78L12ACJG | | MC78L12ACG |
| μA78L12ACLP | MC78L12ACP | |
| μA78L12AHC | MC78L12ACG | |
| μA78L12AWC | MC78L12ACP | |
| μA78L12CJG | | MC78L12CG |
| μA78L12CLP | MC78L12CP | |
| μA78L12HC | MC78L12CG | |
| μA78L12WC | MC78L12CP | |
| μA78L15ACJG | | MC78L15ACG |
| μA78L15ACLP | MC78L15ACP | |
| μA78L15AHC | MC78L15ACG | |
| μA78L15AWC | MC78L15ACP | |
| μA78L15CJG | | MC78L15CG |
| μA78L15CLP | MC78L15CP | |
| μA78L15HC | MC78L15CG | |
| μA78L15WC | MC78L15CP | |
| μA78L18AHC | MC78L18ACG | |
| μA78L18AWC | MC78L18ACP | |
| μA78L24AHC | MC78L24ACG | |
| μA78L24AWC | MC78L24ACP | |
| μA78L26AWC | MC7802ACP | |
| μA78MGT2C | | LM317T |
| μA78MGU1C | | LM317T |
| μA78MGUC | | LM317MT |
| μA78M05CKC | MC78M05CT | |
| μA78M05CKD | | MC78M05CT |
| μA78M05CLA | MC78M05CG | |
| μA78M05HC | MC78M05CG | |
| μA78M05HM | | MC78M05CG |
| μA78M05UC | MC78M05CT | |
| μA78M06CKC | MC78M06CT | |
| μA78M06CKD | | MC78M06CT |
| μA78M06CLA | MC78M06CG | |
| μA78M06HC | MC78M06CG | |
| μA78M06HM | | MC78M06CG |
| μA78M06UC | MC78M06CT | |
| μA78M08CKC | MC78M08CT | |
| μA78M08CKD | | MC78M08CT |
| μA78M08CLA | MC78M08CG | |
| μA78M08HC | MC78M08CG | |
| μA78M08HM | | MC78M08CG |
| μA78M08UC | MC78M08CT | |
| μA78M12CKC | MC78M12CT | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| µA78M12CKD | | MC78M12CT |
| µA78M12CLA | MC78M12CG | |
| µA78M12HC | MC78M12CG | |
| µA78M12HM | | MC78M12CG |
| µA78M12UC | MC78M12CT | |
| µA78M15CKC | MC78M15CT | |
| µA78M15CKD | | MC78M15CT |
| µA78M15CLA | MC78M15CG | |
| µA78M15HC | | MC78M15CG |
| µA78M15HM | | MC78M15CG |
| µA78M15UC | MC78M15CT | |
| µA78M18HC | MC78M18CG | |
| µA78M18HM | | MC78M18CG |
| µA78M18UG | MC78M18CT | |
| µA78M20CKC | MC78M20CT | |
| µA78M20CKD | | MC78M20CT |
| µA78M20CLA | MC78M20CG | |
| µA78M20HC | MC78M20CG | |
| µA78M20HM | | MC78M20CG |
| µA78M20UG | MC78M20CT | |
| µA78M24CKC | MC78M24CT | |
| µA78M24CKD | | MC78M24CT |
| µA78M24CLA | MC78M24CG | |
| µA78M24HC | MC78M24CG | |
| µA78M24HM | | MC78M24CG |
| µA78M24UC | MC78M24CT | |
| µA78S40DC | µA78S40DC | |
| µA78S40DM | µA78S40DM | |
| µA78S40PC | µA78S40PC | |
| µA79L05AHC | MC79L05ACG | |
| µA79L05AWC | MC79L05ACP | |
| µA79L05HC | MC79L05CG | |
| µA79L05WC | MC79L05CP | |
| µA79L12AHC | MC79L12ACG | |
| µA79L12AWC | MC79L12ACP | |
| µA79L12HC | MC79L12CG | |
| µA79L12WC | MC79L12CP | |
| µA79L15AHC | MC79L15ACG | |
| µA79L15AWC | MC79L15ACP | |
| µA79L15HC | MC79L15CG | |
| µA79L15WC | MC79L15CP | |
| µA79M05AUC | MC79M05CT | |
| µA79M05CKC | MC79M05CT | |
| µA79M06AHM | | MC7906CK |
| µA79M06AUC | | MC7906CT |
| µA79M06CKC | | MC7806CT |
| µA79M06HM | | MC7906CK |
| µA79M06UC | | MC7906CT |
| µA79M08AHM | | MC7908CK |
| µA79M08AUC | | MC7908CT |
| µA79M08CKC | | MC7908CT |
| µA79M08HM | | MC7908C |
| µA79M08UC | | MC7908CT |
| µA79M12AUC | MC79M12CT | |
| µA79M12CKC | MC79M12CT | |
| µA79M15AUC | MC79M15CT | |
| µA79M15CKC | MC79M15CT | |
| µA79M18AHM | | MC7918CK |
| µA79M18AUC | | MC7918CT |
| µA79M18HM | | MC7918CK |
| µA79M18UC | | MC7918CT |
| µA79M24AHM | | MC7924CK |
| µA79M24AUC | | MC7924CT |
| µA79M24CKC | | MC7924CT |
| µA79M24HM | | MC7924CK |

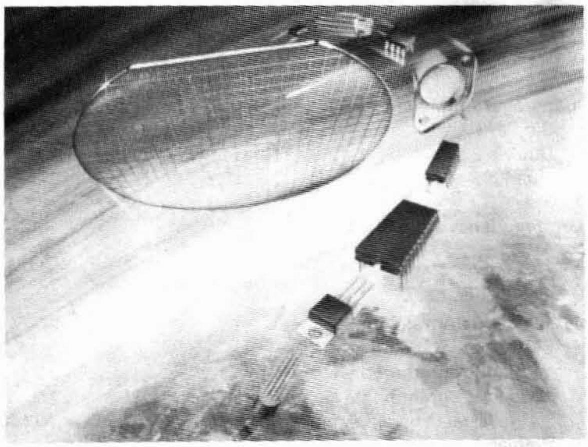
| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| µA79M24UC | | MC7924CT |
| µA101AD | | LM101AJ |
| µA101AF | | LM101AJ |
| µA101AH | LM101AH | |
| µA101D | | LM101AJ |
| µA101F | | LM101AJ |
| µA101H | LM101AH | |
| µA107H | | MC1741 |
| µA108AD | LM108AJ | |
| µA108AF | | LM108AH |
| µA108AH | LM108AH | |
| µA108D | LM108J | |
| µA108F | LM108F | |
| µA108H | LM108H | |
| µA109KM | LM109K | |
| µA117KM | LM117K | |
| µA201AD | | LM201AJ |
| µA201AF | | LM201AJ |
| µA201AH | LM201AH | |
| µA201D | | LM201AJ |
| µA201F | | LM201AJ |
| µA201H | LM201AH | |
| µA207H | | MC1741C |
| µA208AD | LM208AJ | |
| µA208AF | | LM208AH |
| µA208AH | LM208AH | |
| µA208D | LM208J | |
| µA208F | LM208F | |
| µA208H | LM208H | |
| µA209KM | LM209K | |
| µA217UV | | LM217K |
| µA301AD | | LM301AJ |
| µA301AH | LM301AH | |
| µA301AT | LM301AN | |
| µA307T | LM307N | |
| µA308AD | LM308AJ | |
| µA308AH | LM308AH | |
| µA308D | LM308J | |
| µA308H | LM308H | |
| µA309KC | LM309K | |
| µA311T | LM311N | |
| µA317KC | LM317K | |
| µA317UC | LM317T | |
| µA431AWC | TL431CP | |
| µA494DC | TL494CJ | |
| µA494DM | TL494MJ | |
| µA494PC | TL494CN | |
| µA555HC | MC1455G | |
| µA555HM | MC1555G | |
| µA555TC | MC1455P1 | |
| µA556DC | MC3456L | |
| µA556DM | MC3556L | |
| µA556PC | MC3456P | |
| µA565JJC | DAC-565JD | |
| µA565KJC | | DAC-565JD |
| µA565SJM | DAC-565SD | |
| µA565TJM | | DAC-565SD |
| µA702DC | | MC1733C |
| µA702DM | | MC1733 |
| µA702FM | | MC1733 |
| µA702HC | | MC1733C |
| µA702HM | | MC1733 |
| µA702MJ | | MC1733 |
| µA702ML | | MC1733 |
| µA709AHM | MC1709AG | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| µA709AMJG | MC1709AU | |
| µA709AML | MC1709AG | |
| µA709CJG | MC1709CU | |
| µA709CL | MC1709CG | |
| µA709CP | MC1709CP1 | |
| µA709HC | MC1709CG | |
| µA709HM | MC1709G | |
| µA709MJG | MC1709U | |
| µA709ML | MC1709G | |
| µA709TC | MC1709CP1 | |
| µA715DC | | MC1741SCU |
| µA715DM | | MC1741SU |
| µA715HC | | MC1741SCG |
| µA715HM | | MC1741SG |
| µA723CF | MC1723CL | |
| µA723CJ | MC1723CL | |
| µA723CL | MC1723CG | |
| µA723CN | MC1723CP | |
| µA723DC | MC1723CL | |
| µA723DM | MC1723L | |
| µA723F | MC1723L | |
| µA723HC | MC1723CG | |
| µA723HM | MC1723G | |
| µA723MJ | MC1723L | |
| µA723ML | MC1723G | |
| µA723PC | MC1723CP | |
| µA725AHM | | LM108AH |
| µA725EHC | | LM308AH |
| µA725HC | | LM308AH |
| µA725HM | | LM108AH |
| µA733CJ | MC1733CL | |
| µA733CL | MC1733CG | |
| µA733CN | MC1733CP | |
| µA733DC | MC1733CL | |
| µA733DM | MC1733L | |
| µA733FM | MC1733F | |
| µA733HC | MC1733CG | |
| µA733HM | MC1733G | |
| µA733MJ | MC1733L | |
| µA733ML | MC1733G | |
| µA734DC | | LM311J |
| µA734DM | | LM311J |
| µA734HC | | LM311H |
| µA734HM | | LM311H |
| µA740HC | | LF355H |
| µA741ADM | | MC1741L |
| µA741AHM | | MC1741G |
| µA741CJG | MC1741CU | |
| µA741CL | MC1741CG | |
| µA741CP | MC1741CP1 | |
| µA741DC | µA741DC | |
| µA741EHC | | MC1741G |
| µA741HC | µA741HC | |
| µA741HM | MC1741G | |
| µA741MJG | MC1741U | |
| µA741ML | MC1741G | |
| µA741RC | MC1741CU | |
| µA741RM | MC1741U | |
| µA741TC | µA741TC | |
| µA742DC | | CA3059 |
| µA747ADM | | MC1747L |
| µA747AHM | | MC1747G |
| µA747CL | MC1747CG | |
| µA747CN | MC1747CP2 | |
| µA747DC | MC1747CL | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| µA747DM | MC1747L | |
| µA747EDC | MC1747CL | |
| µA747EHC | MC1747CG | |
| µA747HC | MC1747CG | |
| µA747HM | MC1747G | |
| µA747MJ | MC1747L | |
| µA747ML | MC1747G | |
| µA747PC | MC1747CP2 | |
| µA748AHM | | MC1748G |
| µA748CJG | MC1748CU | |
| µA748CL | MC1748CG | |
| µA748CP | MC1748CP1 | |
| µA748HC | MC1748CG | |
| µA748HM | MC1748G | |
| µA748MJG | MC1748U | |
| µA748ML | MC1748G | |
| µA748TC | MC1748CP1 | |
| µA753TC | | MC1357P |
| µA754HC | | MC1355P |
| µA754TC | | MC1355P |
| µA757DC | | MC1350P |
| µA757DM | | MC1350P |
| µA772 | | MC1741S |
| µA775DC | LM339J | |
| µA775DM | LM339J | |
| µA775PC | LM339N | |
| µA776DC | | MC1776CG |
| µA776DM | | MC1776G |
| µA776HC | MC1776CG | |
| µA776HM | MC1776G | |
| µA776TC | MC1776CP1 | |
| µA777CJ | | LM308AJ-8 |
| µA777CJG | | LM308AJ-8 |
| µA777CL | | LM308AH |
| µA777CN | | LM308AN |
| µA777CP | | LM308AN |
| µA777DC | | LM308AJ-8 |
| µA777HC | | LM308AH |
| µA777MJ | | LM108AJ-8 |
| µA777MJG | | LM108AJ-8 |
| µA777ML | | LM108AH |
| µA777TC | | LM308AN |
| µA796DC | MC1496L | |
| µA796DM | MC1596L | |
| µA796HC | MC1496G | |
| µA796HM | MC1596G | |
| µA798HC | MC3458G | |
| µA798HM | MC3558G | |
| µA798RC | MC3458U | |
| µA798RM | MC3558U | |
| µA798TC | MC3458P1 | |
| µA799HC | | MC1741G |
| µA799HM | | MC1741G |
| µA1391PC | MC1391P | |
| µA1394PC | MC1394P | |
| µA1458CHC | MC1458CG | |
| µA1458CP | MC1458CP1 | |
| µA1458CRC | MC1458CU | |
| µA1458CTC | MC1458CP1 | |
| µA1458E | MC1458G | |
| µA1458HC | MC1558G | |
| µA1458P | MC1458P1 | |
| µA1458RC | MC1458U | |
| µA1458TC | MC1458P1 | |
| µA1558E | MC1558G | |

| PART NO. | MOTOROLA DIRECT REPLACEMENT | MOTOROLA SIMILAR REPLACEMENT |
|---|---|---|
| μA1558HM | MC1558G | |
| μA2136PC | | MC1357P |
| μA2240DC | | MC1455U |
| μA2240DM | | MC1555G |
| μA2240PC | | MC1455P1 |
| μA3026HM | | CA3054 |
| μA3045 | | MC3346P |
| μA3046DC | MC3346P | |
| μA3054DC | CA3054P | |
| μA3064PC | | MC13010P |
| μA3065PC | MC1358P | |
| μA3086DM | MC3386P | |
| μA3301P | MC3301P | |
| μA3302P | MC3302P | |
| μA3303P | MC3303P | |
| μA3401P | MC3401P | |
| μA3403D | MC3403L | |
| μA3403P | MC3403P | |
| μA4136DC | | MC4741CL |
| μA4136DM | | MC4741L |
| μA4136PC | | MC4741CP |
| μA4558HC | MC4558CG | |
| μA4558HM | MC4558G | |
| μA4558TC | MC4558CP1 | |
| μA7805CKC | MC7805CT | |
| μA7805KC | MC7805CK | |
| μA7805KM | MC7805K | |
| μA7805UC | MC7805CT | |
| μA7805UV | MC7805BT | |
| μA7806CKC | MC7806CT | |
| μA7806KC | MC7806CK | |
| μA7806KM | MC7806K | |
| μA7806UC | MC7806CT | |
| μA7806UV | MC7806BT | |
| μA7808CKC | MC7808CT | |
| μA7808KC | MC7808K | |
| μA7808KM | MC7808K | |
| μA7808UC | MC7808CT | |
| μA7808UV | MC7808BT | |
| μA7812CKC | MC7812CT | |
| μA7812KC | MC7812CK | |
| μA7812KM | MC7812K | |
| μA7812UC | MC7812CT | |
| μA7812UV | MC7812BT | |
| μA7815CKC | MC7815CT | |
| μA7815KC | MC7815CK | |
| μA7815KM | MC7815K | |
| μA7815UC | MC7815CT | |
| μA7815UV | MC7815BT | |
| μA7818CKC | MC7818CT | |
| μA7818KC | MC7818CK | |
| μA7818KM | MC7818K | |
| μA7818UC | MC7818CT | |
| μA7818UV | MC7818BT | |
| μA7824CKC | MC7824CT | |
| μA7824KC | MC7824CK | |
| μA7824KM | MC7824K | |
| μA7824UC | MC7824CT | |
| μA7824UV | MC7824BT | |
| μA7902KC | MC7902K | |
| μA7902KM | MC7902K | |
| μA7902UC | MC7902CT | |
| μA7905CKC | MC7905CT | |
| μA7905KC | MC7905CK | |
| μA7905KM | | MC7905CK |
| μA7905UC | MC7905CT | |
| μA7905.2CKC | MC7905.2CT | |
| μA7906CKC | MC7906CT | |
| μA7906KC | MC7906CK | |
| μA7906KM | | MC7906CK |
| μA7906UC | MC7906CT | |
| μA7908CKC | MC7908CT | |
| μA7908KC | MC7908CT | |
| μA7908KM | | MC7908CK |
| μA7908UC | | MC7908CT |
| μA7912CKC | MC7912CT | |
| μA7912KC | MC7912CK | |
| μA7912KM | | MC7912CK |
| μA7912UC | MC7912CT | |
| μA7915CKC | MC7915CT | |
| μA7915KC | MC7915CK | |
| μA7915KM | | MC7915CK |
| μA7915UC | MC7915CT | |
| μA7918CKC | MC7918CT | |
| μA7918KC | MC7918CK | |
| μA7918KM | | MC7918CK |
| μA7918UC | MC7918CT | |
| μA7924CKC | MC7924CT | |
| μA7924KC | MC7924CK | |
| μA7924KM | | MC7924CK |
| μA7924UC | MC7924CT | |
| μA9636ACJG | * | |
| μA9636ACP | * | |
| μPC1373 | | MC3373P |

*To be introduced.



*As with other integrated circuit technologies, analog circuit design techniques and processes have been continually refined and updated to meet the needs of an ever-expanding marketplace. Operational amplifiers have utilized JFET inputs for improved performance, CMOS for low power applications, and innovative design concepts for improved high performance and precision characteristics. Basic voltage regulators have been refined to include three-terminal fixed and adjustable voltages, and with the advent of switching regulators, power supply control and supervisory circuits.*

*The original bipolar A-D and D-A converters have been augmented with high performance video speed and multiplying designs. CMOS converters have provided A-D and D-A functions for low power applications, and linear circuit technology has provided precision low-voltage references for use in data conversion and other low temperature drift applications.*

*Bipolar linear designs offer a wide array of receivers, drivers and transceivers for the popular RS-232C and the new RS-485 interface specifications. In addition to these key interface functions, a spectrum of magnetic and semiconductor memory read, write, sense and RAM control circuits are also available.*

*A host of other special purpose devices have been developed using analog designs in both bipolar and CMOS technologies. These circuits find applications in motor control, radio television, automotive, high frequency, and data transmission.*

# Selector Guide

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# Analog Circuits
# Amplifiers

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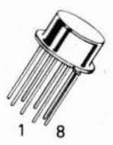
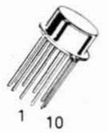
## Operational Amplifiers

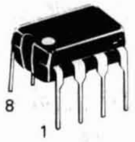
Motorola offers a broad line of bipolar operational amplifiers to meet a wide range of applications. From low-cost industry-standard types to high precision circuits, the span encompasses a large range of performance capabilities. These linear integrated circuits are available as single, dual, and quad monolithic devices in a variety of temperature ranges and package styles. Most devices may be obtained in unencapsulated "chip" form as well. For price and delivery information on chips, please contact your Motorola Sales Representative or Distributor.



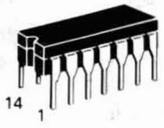
CASE 601
METAL



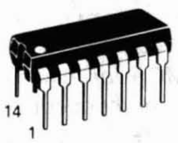
CASE 603
METAL
(TO-100)



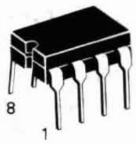
CASE 626
PLASTIC



CASE 632
CERAMIC
(MO-001AA)



CASE 646
PLASTIC



CASE 693
CERAMIC

## Single Operational Amplifiers

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $TC_{VIO}$ μV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V = 1$) MHz Typ | SR ($A_V = 1$) V/μs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Noncompensated** | | | | | | | | | | | |
| **Commercial Temperature Range (0°C to +70°C)** | | | | | | | | | | | |
| LM301A | 0.25 | 7.5 | 10 | 50 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | General Purpose | 601,626,693 |
| LM308 | 7.0 | 7.5 | 15 | 1.0 | 25 | 1.0 | 0.3 | ±3.0 | ±18 | Precision | 601,626,693 |
| LM308A | 7.0 | 0.5 | 5.0 | 1.0 | 80 | 1.0 | 0.3 | ±3.0 | ±18 | Precision | 601,626,693 |
| MC1439 | 1.0 | 7.5 | 15 | 100 | 15 | 2.0 | 4.2 | ±6.0 | ±18 | High Slew Rate | 601,626 |
| MC1709C | 1.5 | 7.5 | 15 | 500 | 15 | 1.0 | 0.3 | ±3.0 | ±18 | General Purpose | 601,626,693 |
| MC1748C | 0.5 | 6.0 | 15 | 200 | 20 | 1.0 | 0.5 | ±3.0 | ±18 | General Purpose | 601,626,693 |
| **Industrial Temperature Range (−25°C to +85°C)** | | | | | | | | | | | |
| LM201A | 0.075 | 2.0 | 10 | 10 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | General Purpose | 601,626,693 |
| LM208 | 0.002 | 2.0 | 3.0 | 0.2 | 50 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | 601,632,693 |
| LM208A | 0.002 | 0.5 | 1.0 | 0.2 | 80 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | 601,632,693 |
| **Military Temperature Range (−55°C to +125°C)** | | | | | | | | | | | |
| LM101A | 0.075 | 2.0 | 10 | 10 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | General Purpose | 601,693 |
| LM108 | 0.002 | 2.0 | 3.0 | 0.2 | 50 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | 601,693 |
| LM108A | 0.002 | 0.5 | 1.0 | 0.2 | 80 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | 601,693 |
| MC1539 | 0.5 | 3.0 | 15 | 60 | 50 | 2.0 | 4.2 | ±4.0 | ±18 | High Slew Rate | 601 |
| MC1709 | 0.5 | 5.0 | 15 | 200 | 25 | 1.0 | 0.3 | ±3.0 | ±18 | General Purpose | 601,693 |
| MC1709A | 0.6 | 3.0 | 5.0 | 100 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | High Performance MC1709 | 601 |
| MC1748 | 0.5 | 5.0 | 15 | 200 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | General Purpose | 601,693 |

## Single Operational Amplifiers (continued)

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $TC_{VIO}$ μV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V = 1$) MHz Typ | SR ($A_V = 1$) V/μs Typ | Supply Voltage V Min | Max | Description | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Internally Compensated** | | | | | | | | | | | |
| **Commercial Temperature Range (0°C to +70°C)** | | | | | | | | | | | |
| LF351 | 200 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 626 |
| LF355 | 200 pA | 10 | 5.0 | 50 pA | 50 | 1.0 | 5.0 | ±5.0 | ±18 | JFET Input | 601,693 |
| LF355B | 100 pA | 5.0 | 5.0 | 20 pA | 50 | 2.5 | 5.0 | ±5.0 | ±22 | JFET Input | 601,693 |
| LF356 | 200 pA | 10 | 5.0 | 50 pA | 50 | 2.0 | 15 | ±5.0 | ±18 | JFET Input | 601,693 |
| LF356B | 100 pA | 5.0 | 5.0 | 20 pA | 50 | 5.0 | 12 | ±5.0 | ±22 | JFET Input | 601,693 |
| LF357 | 200 pA | 10 | 5.0 | 50 pA | 50 | 3.0 | 75 | ±5.0 | ±18 | Wideband FET Input | 601,693 |
| LF357B | 100 pA | 5.0 | 5.0 | 20 pA | 50 | 20 | 50 | ±5.0 | ±22 | JFET Input | 601,693 |
| LM11C | 100 pA | 0.6 | 2.0 | 10 pA | 250 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | 626,632,646,601 |
| LM11CL | 200 pA | 5.0 | 3.0 | 25 pA | 50 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | 693 |
| LM307 | 0.25 | 7.5 | 10 | 50 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | General Purpose | 626 |
| MC1436 | 0.04 | 10 | 12 | 10 | 70 | 1.0 | 2.0 | ±15 | ±34 | High Voltage | 626,601,693 |
| MC1456 | 0.03 | 10 | 12 | 10 | 70 | 1.0 | 2.5 | ±3.0 | ±18 | High Performance | 601,626,693 |
| MC1733C | 30 | — | — | 5.0 μA | 80 | 90 | — | ±4.0 | ±8.0 | Differential Wideband Video Amp | 601,632,646 |
| MC1741C | 0.5 | 6.0 | 15 | 200 | 20 | 1.0 | 0.5 | ±3.0 | ±18 | General Purpose | 601,626,693 |
| MC1741SC | 0.5 | 6.0 | 15 | 200 | 20 | 1.0 | 10 | ±3.0 | ±18 | High Slew Rate | 601,626,693 |
| MC1776C | 0.003 | 6.0 | 15 | 3.0 | 100 | 1.0 | 0.2 | ±1.5 | ±18 | μPower, Programmable | 693,626,601 |
| MC3476 | 0.05 | 6.0 | 15 | 25 | 50 | 1.0 | 0.2 | ±1.5 | ±18 | Low Cost μPower, Programmable | 601,626,693 |
| MC34001 | 200 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 601,626,693 |
| MC34001A | 100 pA | 2.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 601,626,693 |
| MC34001B | 200 pA | 5.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 601,626,693 |
| OP-27EP | 0.040 | 0.025 | 0.2 | 35 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | 626 |
| OP-27FP | 0.055 | 0.060 | 0.3 | 50 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | 626 |
| OP-27GP | 0.080 | 0.100 | 0.4 | 75 | 700 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | 626 |
| OP-37EP | 0.040 | 0.025 | 0.2 | 35 | 1000 | 40 | 17 | ±4.0 | ±22 | Low Noise, Precision | 626 |
| OP-27FP | 0.055 | 0.060 | 0.3 | 50 | 1000 | 40 | 17 | ±4.0 | ±22 | Decompensated for | 626 |
| OP-27GP | 0.080 | 0.100 | 0.4 | 75 | 700 | 40 | 17 | ±4.0 | ±22 | $A_V \geqslant 5$ | 626 |
| TL071AC | 200 pA | 6.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | 626,693 |
| TL071BC | 200 pA | 3.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | 626,693 |
| TL071C | 200 pA | 10 | 10 | 50 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | 626,693 |
| TL081AC | 200 pA | 6.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 626,693 |
| TL081BC | 200 pA | 3.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 626,693 |
| TL081C | 400 pA | 15 | 10 | 200 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 626,693 |
| **Industrial Temperature Range (−25°C to +85°C)** | | | | | | | | | | | |
| OP-27E | 0.040 | 0.025 | 0.2 | 35 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | 693 |
| OP-27F | 0.055 | 0.060 | 0.3 | 50 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | 693 |
| OP-27G | 0.080 | 0.100 | 0.4 | 75 | 700 | 8.0 | 2.8 | ±4.0 | ±22 | Low, Noise, Precision | 693 |
| OP-37E | 0.040 | 0.025 | 0.2 | 35 | 1000 | 40 | 17 | ±4.0 | ±22 | Low Noise, Precision, | 693 |
| OP-37F | 0.055 | 0.060 | 0.3 | 50 | 1000 | 40 | 17 | ±4.0 | ±22 | Decompensated for | 693 |
| OP-37G | 0.080 | 0.100 | 0.4 | 75 | 700 | 40 | 17 | ±4.0 | ±22 | $A_V \geqslant 5$ | 693 |
| **Military Temperature Range (−55°C to +125°C)** | | | | | | | | | | | |
| LM11 | 50 pA | 0.3 | 1.0 | 10 pA | 250 | 1.0 | 0.3 | ±3.0 | ±20 | Precision | 601,632,693 |
| MC1536 | 0.02 | 5.0 | 10 | 3.0 | 100 | 1.0 | 2.0 | ±15 | ±40 | High Voltage | 693,601 |
| MC1556 | 0.015 | 4.0 | 10 | 2.0 | 100 | 1.0 | 2.5 | ±3.0 | ±22 | High Performance | 601,693 |
| MC1733 | 0.20 | — | — | 3.0 μA | 90 | 90 | — | ±4.0 | ±8.0 | Differential Wideband Video Amp | 603,632 |
| MC1741 | 0.5 | 5.0 | 15 | 200 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | General Purpose | 601,693 |
| MC1741S | 0.5 | 5.0 | 15 | 200 | 50 | 1.0 | 10 | ±3.0 | ±22 | High Slew Rate | 601,693 |
| MC1776 | 0.0075 | 5.0 | 15 | 3.0 | 200 | 1.0 | 0.2 | ±1.5 | ±18 | μPower, Programmable | 601,632 |
| MC35001 | 100 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | 601,693 |
| MC35001A | 75 pA | 2.0 | 10 | 25 pA | 50 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | 601,693 |
| MC35001B | 100 pA | 5.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | 601,693 |
| OP-27A | 0.040 | 0.025 | 0.2 | 35 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | 693 |
| OP-27B | 0.055 | 0.060 | 0.3 | 50 | 1000 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | 693 |
| OP-27C | 0.080 | 0.100 | 0.4 | 75 | 700 | 8.0 | 2.8 | ±4.0 | ±22 | Low Noise, Precision | 693 |
| OP-37A | 0.040 | 0.025 | 0.2 | 35 | 1000 | 40 | 17 | ±4.0 | ±22 | Low Noise, Precision, | 693 |
| OP-37B | 0.055 | 0.060 | 0.3 | 50 | 1000 | 40 | 17 | ±4.0 | ±22 | Decompensated for | 693 |
| OP-37C | 0.080 | 0.100 | 0.4 | 75 | 700 | 40 | 17 | ±4.0 | ±22 | $A_V \geqslant 5$ | 693 |
| TL071M | 200 pA | 6.0 | 10 | 50 pA | 35 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | 693 |
| TL081M | 200 pA | 9.0 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 693 |

# Dual Operational Amplifiers

| Device | $I_{IB}$ μA Max | $V_{IO}$ mV Max | $TC_{VIO}$ μV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V = 1$) MHz Typ | SR ($A_V = 1$) V/μs Typ | Supply Voltage V | | Description | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Min | Max | | |
| **Noncompensated** | | | | | | | | | | | |
| **Commercial Temperature Range (0°C to +70°C)** | | | | | | | | | | | |
| MC1437 | 1.5 | 7.5 | 10 | 500 | 15 | 1.0 | 0.25 | ±3.0 | ±18 | Dual MC1709 | 632,646 |
| **Military Temperature Range (−55°C to +125°C)** | | | | | | | | | | | |
| MC1537 | 0.5 | 5.0 | 10 | 200 | 25 | 1.0 | 0.25 | ±3.0 | ±18 | Dual MC1709 | 632 |
| **Internally Compensated** | | | | | | | | | | | |
| **Commercial Temperature Range (0°C to +70°C)** | | | | | | | | | | | |
| LF353 | 200 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 626 |
| LM358 | 0.25 | 6.0 | 7.0 | 50 | 25 | 1.0 | 0.6 | ±1.5<br>+3.0 | ±18<br>+36 | Single Supply (Low Power Consumption) | 601,626,693 |
| MC1458 | 0.5 | 6.0 | 10 | 200 | 20 | 1.1 | 0.8 | ±3.0 | ±18 | Dual MC1741 | 601,626,693 |
| MC1458C | 0.70 | 10 | 10 | 300 | 20 | 1.1 | 0.8 | ±3.0 | ±18 | Dual General Purpose | 601,626 |
| MC1458S | 0.5 | 6.0 | 10 | 200 | 20 | 1.0 | 10 | ±3.0 | ±18 | High Slew Rate | 601,626,693 |
| MC1747C | 0.5 | 6.0 | 10 | 200 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | Dual MC1741 | 603,632,646 |
| MC3458 | 0.5 | 10 | 7.0 | 50 | 20 | 1.0 | 0.6 | ±1.5<br>+3.0 | ±18<br>+36 | Split Supplies<br>Single Supply (Low Crossover Distortion) | 601,626,693 |
| MC4558C | 0.5 | 6.0 | 10 | 200 | 20 | 3.0 | 1.5 | ±3.0 | +18 | High Frequency | 601,626,693 |
| MC34002 | 100 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 601,626,693 |
| MC34002A | 75 pA | 2.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 601,626,693 |
| MC34002B | 100 pA | 5.0 | 10 | 70 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 601,626,693 |
| TL072AC | 200 pA | 6.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | 626,693 |
| TL072BC | 200 pA | 3.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | 626,693 |
| TL072C | 200 pA | 10 | 10 | 50 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | 626,693 |
| TL082AC | 200 pA | 6.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 626,693 |
| TL082BC | 200 pA | 3.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 626,693 |
| TL082C | 400 pA | 15 | 10 | 200 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 626,693 |
| **Industrial Temperature Range (−25°C to +85°C)** | | | | | | | | | | | |
| LM258 | 0.15 | 5.0 | 10 | 30 | 50 | 1.0 | 0.6 | ±1.5<br>±3.0 | ±18<br>±36 | Split or Single Supply OP Amp | 601,626,693 |
| **Automotive Temperature Range (−40°C to +85°C)** | | | | | | | | | | | |
| MC3358 | 5.0 | 8.0 | 10 | 75 | 20 | 1.0 | 0.6 | ±1.5<br>+3.0 | ±18<br>+36 | Split Supplies<br>Single Supply | 626 |
| LM2904 | 0.25 | 7.0 | 7.0 | 50 | 100 typ | 1.0 | 0.6 | ±1.5<br>±3.0 | ±13<br>±26 | Split or Single Supply OP Amp | 626 |
| **Military Temperature Range (−55°C to +125°C)** | | | | | | | | | | | |
| LM158 | 0.15 | 5.0 | 10 | 30 | 50 | 1.0 | 0.6 | ±1.5<br>+3.0 | ±18<br>+36 | Split Supplies<br>Single Supply (Low Power Consumption) | 601,632,693 |
| MC1558 | 0.5 | 5.0 | 10 | 200 | 50 | 1.1 | 0.8 | ±3.0 | ±22 | Dual MC1741 | 601,693 |
| MC1558S | 0.5 | 5.0 | 10 | 200 | 50 | 1.0 | 10 | ±3.0 | ±22 | High Slew Rate | 601,693 |
| MC1747 | 0.5 | 5.0 | 10 | 200 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | Dual MC1741 | 601,632 |
| MC3558 | 0.5 | 5.0 | 10 | 50 | 50 | 1.0 | 0.6 | ±1.5<br>+3.0 | ±18<br>+36 | Split Supplies<br>Single Supply | 601,693 |
| MC4558 | 0.5 | 5.0 | 10 | 200 | 50 | 4.0 | 1.5 | ±3.0 | ±22 | High Frequency | 601,693 |
| MC35002 | 100 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | 601,693 |
| MC35002A | 75 pA | 2.0 | 10 | 25 pA | 50 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | 601,693 |
| MC35002B | 100 pA | 5.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | 601,693 |
| TL072M | 200 pA | 6.0 | 10 | 50 pA | 35 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | 693 |
| TL082M | 200 pA | 6.0 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 693 |

# Quad Operational Amplifiers

## Internally Compensated

### Commercial Temperature Range (0°C to +70°C)

| Device | $I_{IB}$ µA Max | $V_{IO}$ mV Max | $TC_{VIO}$ µV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V = 1$) MHz Typ | SR ($A_V = 1$) V/µs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LF347 | 200 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 646 |
| LF347B | 200 pA | 5.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 646 |
| LM324 | 0.25 | 6.0 | 7.0 | 50 | 25 | 1.0 | 0.6 | ±1.5 | ±16 | Low Power | 632,646 |
| | | | | | | | | +3.0 | +32 | Consumption | |
| LM348 | 0.20 | 6.0 | — | 50 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | Quad MC1741 | 632,646 |
| MC3401 | 0.3 | — | — | — | 1.0 | 5.0 | 0.6 | ±1.5 | ±18 | Norton Input | 632,646 |
| LM3900 | | | | | | | | +3.0 | +36 | | |
| MC3403 | 0.5 | 10 | 7.0 | 50 | 20 | 1.0 | 0.6 | ±1.5 | ±18 | No Crossover | 632,646 |
| | | | | | | | | +3.0 | +36 | Distortion | |
| MC4741C | 0.5 | 6.0 | 15 | 200 | 20 | 1.0 | 0.5 | ±3.0 | ±18 | Quad MC1741 | 632,646 |
| MC34004 | 200 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 632,646 |
| MC34004B | 200 pA | 5.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 632,646 |
| MC34074 | 0.50 | 4.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, | 632,646 |
| MC34074A | 0.50 | 2.0 | 10 | 50 | 50 | 4.5 | 10 | +3.0 | +44 | Single Supply | 632,646 |
| MC34084 | 200 pA | 12 | 10 | 100 pA | 25 | 8 | 30 | ±5.0 | ±18 | Hi-Speed, JFET Input | 646 |
| MC34084A | 200 pA | 6 | 10 | 100 pA | 50 | 8 | 30 | ±5.0 | ±18 | Hi-Speed, JFET Input | 646 |
| MC34085 | 200 pA | 12 | 10 | 100 pA | 25 | 16 | 55 | ±5.0 | ±18 | Decompensated | 646 |
| MC34085A | 200 pA | 6 | 10 | 100 pA | 50 | 16 | 55 | ±5.0 | ±18 | MC34084 for $A_V \geq 2$ | 646 |
| TL074AC | 200 pA | 6.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | 632,646 |
| TL074C | 200 pA | 10 | 10 | 50 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | 632,646 |
| TL084AC | 200 pA | 6.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 632,646 |
| TL084BC | 200 pA | 3.0 | 10 | 100 pA | 50 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 632,646 |
| TL084C | 400 pA | 15 | 10 | 200 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 632,646 |

### Industrial Temperature Range (−25°C to +85°C)

| Device | $I_{IB}$ µA Max | $V_{IO}$ mV Max | $TC_{VIO}$ µV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V = 1$) MHz Typ | SR ($A_V = 1$) V/µs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM224 | 0.15 | 5.0 | 7.0 | 30 | 50 | 1.0 | 0.6 | ±1.5 | ±16 | Split or Single | 632,646 |
| | | | | | | | | ±3.0 | ±32 | Supply OP Amp | |
| LM248 | 0.20 | 6.0 | — | 50 | 25 | 1.0 | 0.5 | ±3.0 | ±18 | Quad MC1741 | 632,646 |

### Automotive Temperature Range (−40°C to +85°C)

| Device | $I_{IB}$ µA Max | $V_{IO}$ mV Max | $TC_{VIO}$ µV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V = 1$) MHz Typ | SR ($A_V = 1$) V/µs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM2902 | 0.5 | 10 | — | 50 | — | 1.0 | 0.6 | ±1.5 | ±13 | Differential | 646 |
| | | | | | | | | +3.0 | +26 | Low Power | |
| MC3301 | 0.3 | — | — | — | 1.0 | 4.0 | 0.6 | ±2.0 | ±15 | Norton Input | 646 |
| LM2900 | | | | | | | | +4.0 | +28 | | |
| MC3303 | 0.5 | 8.0 | 10 | 75 | 20 | 1.0 | 0.6 | ±1.5 | ±18 | Differential | 646 |
| | | | | | | | | +3.0 | +36 | General Purpose | |
| MC33074 | 0.50 | 4.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, | 632,646 |
| MC33074A | 0.50 | 2.0 | 10 | 50 | 50 | 4.5 | 10 | +3.0 | +44 | Single Supply | 632,646 |

### Telecommunications Temperature Range (−40°C to +85°C)

| Device | $I_{IB}$ µA Max | $V_{IO}$ mV Max | $TC_{VIO}$ µV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V = 1$) MHz Typ | SR ($A_V = 1$) V/µs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MC143403 | 1.0 nA | 30 | — | 200 pA | 45 dB | 0.8 | 1.5 | 4.75 | 12.6 | CMOS, Low Power, Drives Low-Impedance Loads | 632,646 |
| MC143404 | 1.0 nA | 30 | — | 200 pA | 60 dB | 0.8 | 1.0 | 4.75 | 12.6 | CMOS, Very Low Power | 632,646 |

### Military Temperature Range (−55°C to +125°C)

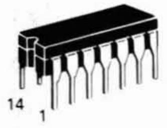
| Device | $I_{IB}$ µA Max | $V_{IO}$ mV Max | $TC_{VIO}$ µV/°C Typ | $I_{IO}$ nA Max | $A_{vol}$ V/mV Min | BW ($A_V = 1$) MHz Typ | SR ($A_V = 1$) V/µs Typ | Supply Voltage V Min | Supply Voltage V Max | Description | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM124 | 0.15 | 5.0 | 7.0 | 30 | 50 | 1.0 | 0.6 | ±1.5 | ±16 | Low Power | 632,646 |
| | | | | | | | | +3.0 | +32 | Consumption | |
| LM148 | 0.10 | 5.0 | — | 25 | 50 | 1.0 | 0.5 | ±3.0 | ±18 | Quad MC1741 | 632 |
| MC3503 | 0.5 | 5.0 | 7.0 | 50 | 50 | 1.0 | 0.6 | ±1.5 | ±18 | General Purpose | 632,646 |
| | | | | | | | | +3.0 | +36 | Low Power | |
| MC4741 | 0.5 | 5.0 | 15 | 200 | 50 | 1.0 | 0.5 | ±3.0 | ±22 | Quad MC1741 | 632,646 |
| MC35004 | 100 pA | 10 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | 632 |
| MC35004B | 100 pA | 5.0 | 10 | 50 pA | 50 | 4.0 | 13 | ±5.0 | ±22 | JFET Input | 632 |
| MC35074 | 0.50 | 4.5 | 10 | 75 | 25 | 4.5 | 10 | +3.0 | +44 | High Performance, | 632 |
| MC35074A | 0.50 | 2.0 | 10 | 50 | 50 | 4.5 | 10 | +3.0 | +44 | Single Supply | 632 |
| MC35084 | 200 pA | 12 | 10 | 100 pA | 25 | 8 | 30 | ±5.0 | ±18 | Hi-Speed, JFET Input | 632 |
| MC35084A | 200 pA | 6 | 10 | 100 pA | 50 | 8 | 30 | ±5.0 | ±18 | Hi-Speed, JFET Input | 632 |
| MC35085 | 200 pA | 12 | 10 | 100 pA | 25 | 16 | 55 | ±5.0 | ±18 | Decompensated | 632 |
| MC35085A | 200 pA | 6 | 10 | 100 pA | 50 | 16 | 55 | ±5.0 | ±18 | MC35084 for $A_V \geq 2$ | 632 |
| TL074M | 200 pA | 9.0 | 10 | 50 pA | 35 | 4.0 | 13 | ±5.0 | ±18 | Low Noise, JFET Input | 632 |
| TL084M | 200 pA | 9.0 | 10 | 100 pA | 25 | 4.0 | 13 | ±5.0 | ±18 | JFET Input | 632 |

# High Frequency Amplifiers

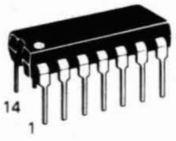
A variety of high-frequency circuits with features ranging from low-cost simplicity to multi-function versatility marks Motorola's line of integrated amplifiers. Devices described here are intended for industrial and communications applications. For devices especially dedicated to consumer products, i.e., TV and entertainment radio, see "Consumer and Automotive Circuits."

CASE 601
METAL

CASE 603
METAL
(TO-100)



CASE 632
CERAMIC
(MO-001AA)



CASE 646
PLASTIC

## AGC Amplifiers

### MC1590G — Wide-Band General Purpose

Has differential inputs and outputs with unneutralized power gain as high as 35 dB typical at 100 MHz in tuned amplifier service. Effective AGC voltage range from 5.0 to 7.0 volts for a 60 dB gain reduction.

### MC1545/1445 — Gated 2-Channel Input

Differential input and output amplifier with gated 2-channel input for a wide variety of switching purposes. Typical 75 MHz bandwidth makes it suitable for high-frequency applications such as video switching, FSK circuits, multiplexers, etc. Gating circuit is useful for AGC control.

## Non-AGC Amplifiers

### SE/NE592 — Differential Two Stage Video Amplifier

A monolithic, two state differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems.

### MC1733/MC1733C — Video Amplifier

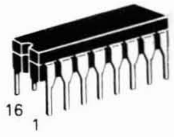
Differential input and output amplifier provides three fixed gain options with bandwidth to 120 MHz. External resistor permits any gain setting from 10 to 400 V/V. Extremely fast rise time (2.5 ns typ) and propagation delay time (3.6 ns typ) makes this unit particularly useful as pulse amplifier in tape, drum, or disc memory read applications.

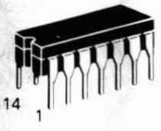
| **Operating Temperature Range** | | | | | | |
|---|---|---|---|---|---|---|
| **−55 to +125°C** | **0 to +70°C** | **$A_V$ dB** | @ | **Bandwidth MHz** | **$V_{CC}/V_{EE}$ Vdc** | **Case** |
| MC1590G | — | 44 Typ<br>4.0 Typ | | 10<br>100 | +12/− | 601 |
| MC1545 | MC1445 | 19 Typ | | 75 | +5/−5 | 603, 632 |
| SE592 | NE592 | 55<br>45 | | 40<br>90 | +6/−6 | 603, 632<br>646 |
| MC1733 | MC1733C | 52<br>40<br>20 | | 40<br>90<br>120 | +6/−6 | 602, 632,<br>646 |

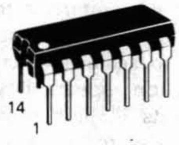
# Miscellaneous Amplifiers

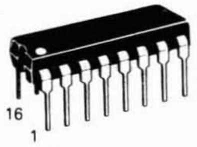
Motorola provides several bipolar and CMOS special purpose amplifiers which fill specific needs. These devices range from low-power CMOS programmable amplifiers and comparators to bipolar variable gain-power amplifiers.

CASE 603C
METAL


CASE 620
CERAMIC


CASE 632
CERAMIC
(MO-001AA)

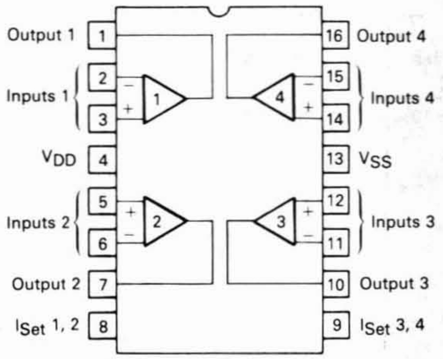

CASE 646
PLASTIC


CASE 648
PLASTIC

## CMOS

These low power devices are designed for applications such as active filters, voltage reference circuits, function generators, oscillators, and limit set alarms.

**MC14573: Quad Programmable Operational Amplifier**
**MC14574: Quad Programmable Comparator**
**MC14575: Dual/Dual Programmable Operational Amplifier — Comparator**


Output 1
1
2
3
Inputs 1
V<sub>DD</sub>
4
5
6
Inputs 2
Output 2
7
I<sub>Set</sub> 1, 2
8
16
Output 4
15
14
Inputs 4
13
V<sub>SS</sub>
12
11
Inputs 3
10
Output 3
9
I<sub>Set</sub> 3, 4
1
2
3
4
+
−

CASE 620, CASE 648

| Supply Voltage Range | | Frequency Range MHz |
|---|---|---|
| Single | Dual | |
| 3.0 to 15 | ±1.5 to ±7.5 | dc to ~1.0 |

## Power Amplifiers Variable Gain

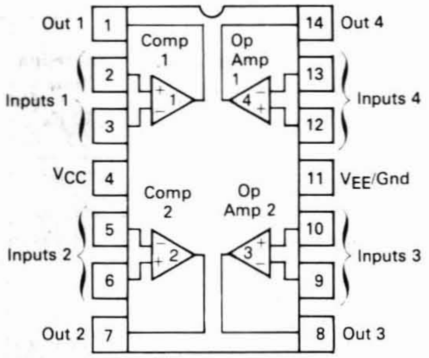
One-watt Power Amplifier for single or split supply operation. Typical voltage gain of 10, 18, or 33 V/V with 0.4% THD.

**MC1554G** ($T_A = -55$ to $+125°C$)
**MC1454G** ($T_A = 0$ to $+70°C$)
**CASE 603C**

## Bipolar

This device contains two Differential Input Operational Amplifiers and two Comparators each set capable of single supply operation. This operational amplifier-comparator circuit will find its applications as a general purpose product for automotive circuits and as an industrial "building block."

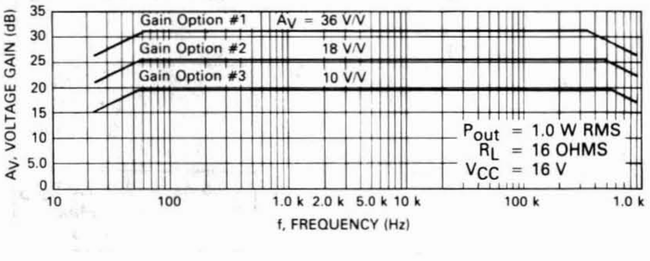
**MC3505L Dual/Dual Operational**
**MC3405L,P Amplifier/Comparator**


Out 1
1
2
3
Inputs 1
V<sub>CC</sub>
4
5
6
Inputs 2
Out 2
7
14
Out 4
13
12
Inputs 4
11
V<sub>EE</sub>/Gnd
10
9
Inputs 3
8
Out 3
Comp 1
Op Amp 1
Comp 2
Op Amp 2
1
2
3
4
+
−

CASE 632, CASE 646

| Supply Voltage Range | | Frequency Range MHz |
|---|---|---|
| Single | Dual | |
| 3.0 to 36 | ±1.5 to ±18 | dc to ~1.0 |

VOLTAGE GAIN versus FREQUENCY ($R_L$ = 16 OHMS)



# Analog Circuits
# Data Converters

The line of data conversion products which Motorola offers, span a wide spectrum of speed and resolution/accuracy. Features including bus compatibility minimize external parts count and provide easy interface to microprocessor systems. Various technologies, such as Bipolar and CMOS, are utilized to achieve functional capability, accuracy and production repeatability. Bipolar technology generally results in higher speed, while CMOS devices offer greatly reduced power consumption.

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## A-D/D-A Converters

### CMOS — For Telecommunications

| Resolution (Bits) | Device | Monotonicity (Bits) | Conversion Time | Input Voltage Range | Supplies (V) | Temperature Range | Package | Comments |
|---|---|---|---|---|---|---|---|---|
| 13 | MC145402* | 13 | 31.25 µs | ±3.28 V peak | ±5 to 6 | −40 to +85°C | Case 620 | Digital signal processing (e.g., echo cancelling, high-speed modems, phone systems with conferencing) |

*To Be Introduced

## A-D Converters

### CMOS

| Resolution (Bits) | Device | Nonlinearity (Max) | Conversion Time | Input Voltage Range | Supplies (V) | Temperature Range | Package (Suffix) | Comments |
|---|---|---|---|---|---|---|---|---|
| 8 | MC145040 | ±1/2 LSB | 10 µs | 0 to $V_{DD}$ | +5.0, ±10% | −55°C to +125°C<br>−40°C to +85°C | Case 732<br>Case 738 | Requires External Clock |
| | MC145041 | | 20 µs | | | | | Includes Internal Clock |
| | MC14442 | | 32 µs | | | −40°C to +85°C | Case 733<br>Case 710 | µP Compatible<br>11-Channel MUX<br>S.A.R. |
| | MC14444 | | | | | | Case 711<br>Case 734 | µP Compatible<br>15-Channel MUX<br>S.A.R. |
| 8–10 | MC14443/47 | ±0.5% Full Scale | 300 µs | Variable w/Supply | +5.0 to +18 | −40°C to +85°C | Case 620<br>Case 648 | µP Compatible,<br>Single Slope,<br>6-Channel MUX |
| 3-1/2 Digit | MC14433 | ±0.05%<br>±1 Count | 40 ms | ±2.0 V<br>±200 mV | +5.0, +8.0 | −40°C to +85°C | Case 623<br>Case 709 | Dual Slope |

### Bipolar

| Resolution (Bits) | Device | Nonlinearity (Max) | Conversion Time | Input Voltage Range | Supplies (V) | Temperature Range | Package (Suffix) | Comments |
|---|---|---|---|---|---|---|---|---|
| 7 | MC10315L | ±1/2 LSB | 66 ns | 1 to 2 $V_{p-p}$ | +5.0, −5.2 | 0°C to +70°C | Case 623 | Video Speed Flash, ECL Logic Levels |
| | MC10317L | | | | | | | Expandable to 8 Bits |
| 8 | MC6108 | | 2.0 µs** | ±5.0 V<br>0 to 5.0 V<br>0 to 10 V | | | Case 719 | µP Compatible, Three-State Outputs, includes Reference |
| 8 | MC10319 | | 50 ns | 0 to 2.0 $V_{p-p}$ Max | +5.0 V and −5.0 V or −5.2 V | | Case 623<br>Case 777 | Video Speed Flash Converter Internal Grey Code |

# D-A Converters

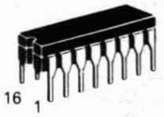
## CMOS

| Resolution (Bits) | Device | Suffix | Accuracy @ 25°C (Max) | Settling Time (±1/2 LSB) | Internal Reference | Supplies (V) | Temperature Range | Package | Comments |
|---|---|---|---|---|---|---|---|---|---|
| 6 | MC144110 | | — | — | — | +5.0 to +15 | 0°C to +85°C | Case 707 | Serial input, Hex DAC, 6 outputs |
| | MC144111 | | | | | | | Case 646 | Serial input, Quad DAC, 4 outputs |
| 8 | MC14549B<br>MC14559B | A<br>C | — | — | — | +3.0 to +18 | −55°C to +125°C<br>−40°C to +85°C | Case 620<br>Case 648 | Compatible with MC1408 (SAR) 8-Bit D-A Converter |

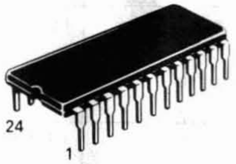
## Bipolar

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 6 | MC1406 | | ±1/2 LSB | 300 ns | — | +5.0, −15 | 0°C to +70°C | Case 632 | Multiplying |
| | MC1506 | | | | | | −55°C to +125°C | | |
| 8 | DAC-08 | | ±1/2 LSB | 150 ns | — | ±5.0 to ±15 | −55°C to +125°C | Case 620 | High-Speed Multiplying |
| | | A | ±1/4 LSB | 135 ns | | | | Case 648 | |
| | | C | ±1 LSB | 150 ns | | | 0°C to +70°C | | |
| | | E | ±1/2 LSB | | | | | | |
| | | H | ±1/4 LSB | 135 ns | | | | | |
| | MC1408 | L6/P6 | ±2 LSB | 300 ns Typ | — | +5.0, −15 | 0°C to +70°C | Case 620 | Multiplying |
| | | L7/P7 | ±1 LSB | | | | | Case 648 | |
| | | L8/P8 | ±1/2 LSB | | | | | | |
| | MC1508 | L8 | ±1/2 LSB | 300 ns | — | +5.0, −15 | −55°C to +125°C | | |
| | MC6890 | | ±1/2 LSB | 300 ns | 2.5 V | ±5.0 to ±15 | 0°C to +70°C | Case 732 | μP Compatible Double Buffered. Includes Application Resistors |
| | | A | | | | | −55°C to +125°C | | |
| | MC10318 | CL6 | ±2 LSB | 10 ns Typ | — | −5.2 | 0°C to +70°C | Case 620 | ECL input Logic Levels |
| | | CL7 | ±1 LSB | | | | | | |
| | | L | ±1/2 LSB | | | | | Case 690 | |
| | | L9 | ±1/4 LSB | | | | | | |
| 10 | MC3410 | | ±1/2 LSB | 250 ns Typ | — | +5.0, −15 | 0°C to +70°C | Case 690 | Multiplying |
| | | C | ±1 LSB | | | | | | |
| | MC3510 | | ±1/2 LSB | | | | −55°C to +125°C | | |
| 12 | AD562A | A | ±1/2 LSB | 400 ns | — | +15, −15 | | Case 716 | High-speed Multiplying, includes Applications Resistors |
| | | K | ±1/2 LSB | | | | 0°C to +70°C | | |
| | | S | ±1/4 LSB | | | | −55°C to +125°C | | |
| | AD563 | J | ±1/2 LSB | 1.2 μs | 2.5 V | +5.0, −15 | 0°C to +70°C | | Includes Applications Resistors. Suffix variations represent variations in *Gain TC.* |
| | | K | ±1/4 LSB | | | | | | |
| | | S | | | | | −55°C to +125°C | | |
| | MC3412 | | ±1/2 LSB | 400 ns | 10 V | +15, −15 | 0°C to +70°C | Case 716 | High-speed, includes Applications Resistors |
| | MC3512 | | | | | | −55°C to +125°C | | |

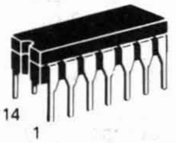
# Package Overview



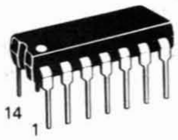
CASE 620
CERAMIC



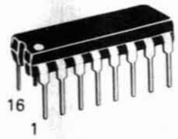
CASE 623
CERAMIC



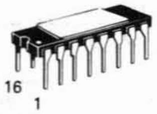
CASE 632
CERAMIC



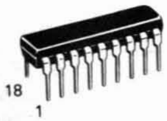
CASE 646
PLASTIC



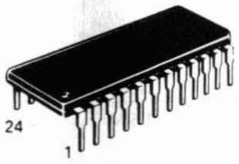
CASE 648
PLASTIC



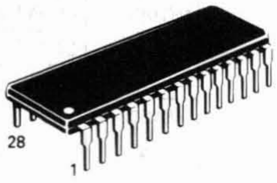
CASE 690
CERAMIC



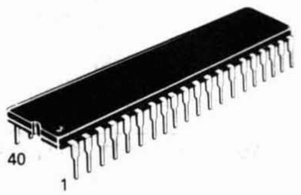
CASE 707
PLASTIC



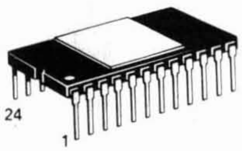
CASE 709
PLASTIC



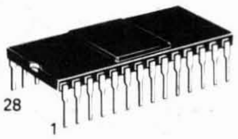
CASE 710
PLASTIC



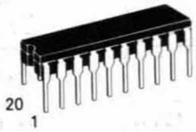
CASE 711
PLASTIC



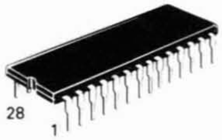
CASE 716
CERAMIC



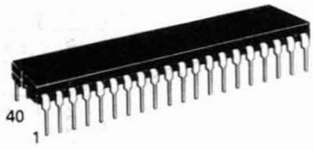
CASE 719
CERAMIC



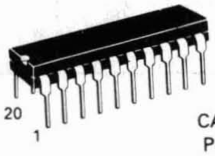
CASE 732
CERAMIC



CASE 733
CERDIP



CASE 734
CERAMIC



CASE 738
PLASTIC

# Analog Circuits
# Comparators

Motorola offers a broad line of comparators that encompasses a large range of performance capabilities. These Linear Integrated Circuits are available as single, dual and quad monolithic devices in a variety of package styles and as standard "chips" for hybrid circuit manufacture.

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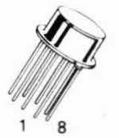
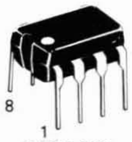
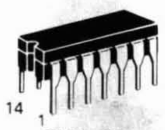


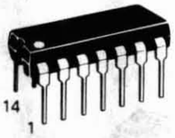
CASE 601
METAL



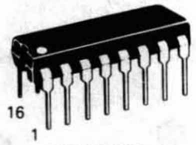
CASE 626
PLASTIC



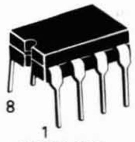
CASE 632
CERAMIC
(MO-001AA)



CASE 646
PLASTIC



CASE 648
PLASTIC



CASE 693
CERAMIC

## Comparators

| Device | $I_{IB}$ µA Max | $V_{IO}$ mV Max | $I_{IO}$ µA Max | $A_V$ V/V Typ | Output Current mA Min | Response Time ns | Supply Voltage V | Description | Temperature Range (°C) | Packages |
|---|---|---|---|---|---|---|---|---|---|---|
| **Single** | | | | | | | | | | |
| LM111 | 0.10 | 3.0 | 0.01 | 200K | 8.0 | 200 | +15, −15 | With strobe, will operate from single supply | −55 to +125 | 601,693 |
| LM211 | 0.10 | 3.0 | 0.01 | 200K | 8.0 | 200 | +15, −15 | | −25 to +85 | 601,693 |
| LM311 | 0.25 | 7.5 | 0.05 | 200K | 8.0 | 200 | +15, −15 | | 0 to +70 | 601,626,693 |
| **Dual** | | | | | | | | | | |
| LM193 | 0.10 | 5.0 | 0.025 | 200K | 6.0 | 1300 | ±1.5 to ±18 or +3.0 to +36 | Designed for single or split supply operation, input commonmode includes ground (negative supply) | −55 to +125 | 601 |
| LM193A | 0.10 | 2.0 | 0.025 | 200K | 6.0 | 1300 | | | −55 to +125 | 601 |
| LM293 | 0.25 | 5.0 | 0.050 | 200K | 6.0 | 1300 | | | −25 to +85 | 601 |
| LM293A | 0.25 | 2.0 | 0.050 | 200K | 6.0 | 1300 | | | −25 to +85 | 601 |
| LM393 | 0.25 | 5.0 | 0.050 | 200K | 6.0 | 1300 | | | 0 to +70 | 601,626 |
| LM393A | 0.25 | 2.0 | 0.050 | 200K | 6.0 | 1300 | | | 0 to +70 | 601,626 |
| LM2903 | 0.25 | 7.0 | 0.050 | 200K | 6.0 | 1500 | | | −40 to +85 | 626 |
| MC3324 | 0.25 | 10 | 0.025 | — | 200 | 1000 | +4.5 to +40 | Dual comparator/power supply supervisory circuit. | −40 to +85 | 620,648 |
| MC3324A | 0.25 | 8.0 | 0.025 | — | 200 | 1000 | +4.5 to +40 | | −40 to +85 | 620,648 |
| MC3424 | 0.25 | 10 | 0.025 | — | 200 | 1000 | +4.5 to +40 | | 0 to +70 | 620,648 |
| MC3424A | 0.25 | 8.0 | 0.025 | — | 200 | 1000 | +4.5 to +40 | | 0 to +70 | 620,648 |
| MC3524 | 0.25 | 10 | 0.025 | — | 200 | 1000 | +4.5 to +40 | | −55 to +125 | 620 |
| MC3524A | 0.25 | 8.0 | 0.025 | — | 200 | 1000 | +4.5 to +40 | | −55 to +125 | 620 |
| **Quad** | | | | | | | | | | |
| LM139 | 0.25 | 5.0 | 0.025 | 200K | 6.0 | 1300 | ±1.5 to ±18 or +3.0 to +36 | Designed for single or split supply operation, input commonmode includes ground (negative supply) | −55 to +125 | 632 |
| LM139A | 0.10 | 2.0 | 0.025 | 200K | 6.0 | 1300 | | | −55 to +125 | 632 |
| LM239 | 0.25 | 5.0 | 0.050 | 200K | 6.0 | 1300 | | | −25 to +85 | 632,646 |
| LM239A | 0.25 | 2.0 | 0.050 | 200K | 6.0 | 1300 | | | −25 to +85 | 632,646 |
| LM339 | 0.25 | 5.0 | 0.050 | 200K | 6.0 | 1300 | | | 0 to +70 | 632,646 |
| LM339A | 0.25 | 2.0 | 0.050 | 200K | 6.0 | 1300 | | | 0 to +70 | 632,646 |
| LM2901 | 0.25 | 7.0 | 0.050 | 100K | 6.0 | 1300 | | | −40 to +85 | 646 |
| MC3302 | 0.50 | 20 | 0.500 | 30K | 6.0 | 1300 | | | −40 to +85 | 646 |
| MC3430 | 40 | 6.0 | 1.0 Typ | 1.2K | 16 | 33 | +5.0, −5.0 | High speed comparator/ sense-amplifier | 0 to +70 | 620,648 |
| MC3431 | 40 | 10 | 1.0 Typ | 1.2K | 16 | 33 | +5.0, −5.0 | | 0 to +70 | 620,648 |
| MC3432 | 40 | 6.0 | 1.0 Typ | 1.2K | 16 | 40 | +5.0, −5.0 | | 0 to +70 | 620,648 |
| MC3433 | 40 | 10 | 1.0 Typ | 1.2K | 16 | 40 | +5.0, −5.0 | | 0 to +70 | 620,648 |

### Bipolar Dual/Dual Operational Amplifier/Comparator
### MC3405L,P/MC3505L — See Miscellaneous Amplifiers Section.

### CMOS Comparators
### MC14574/MC14575 — See Miscellaneous Amplifiers Section.

# Analog Circuits
# Special Circuits

A variety of special function analog circuits are provided in both bipolar and CMOS technologies. These products provide key functions in a wide range of applications including PCM, TV receivers, data transmission, industrial controls, smoke detectors, and automobiles.

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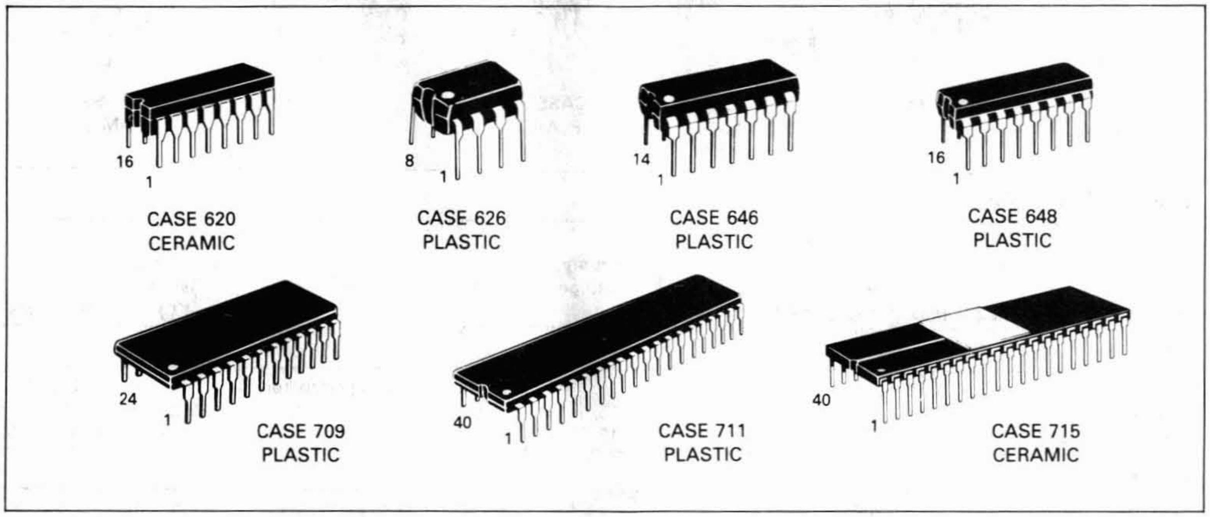
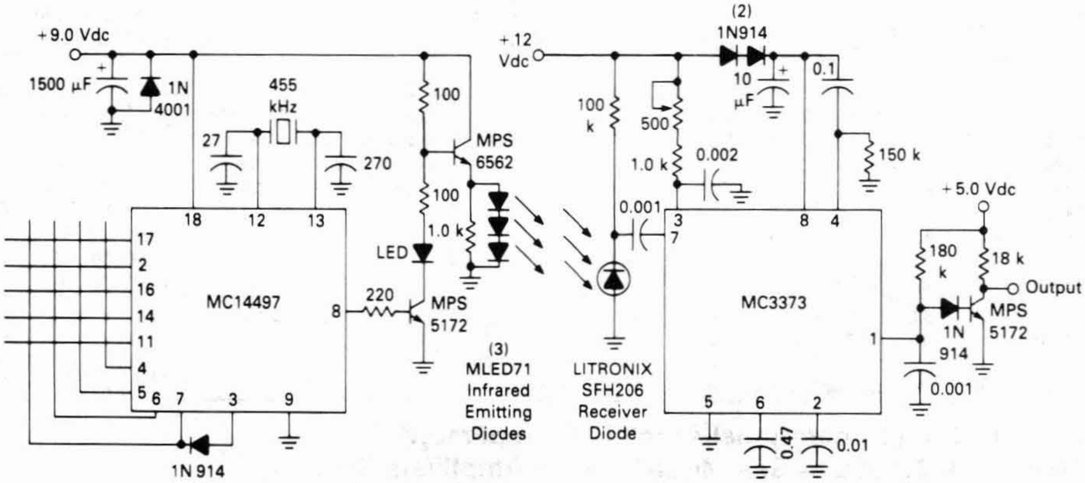
Balanced Mod/Demod . . . . . . . . . . . . . . . . . . . . . 2-15
CMOS Miscellaneous. . . . . . . . . . . . . . . . . . . . . . 2-16


16
1
CASE 620
CERAMIC
8
1
CASE 626
PLASTIC
14
1
CASE 646
PLASTIC
16
1
CASE 648
PLASTIC
24
1
CASE 709
PLASTIC
40
1
CASE 711
PLASTIC
40
1
CASE 715
CERAMIC

## Remote Control

### MC14497 Transmitter (CMOS)
### MC3373 Amplifiers/Detector (Bipolar)

Amplifier/Receiver pair designed for infrared remote-control PCM applications. Receiver incorporates high-gain preamplifier and pulse shaping required to transfer signal from IR diode to tuning control system logic. This reduces external component count to a minimum.

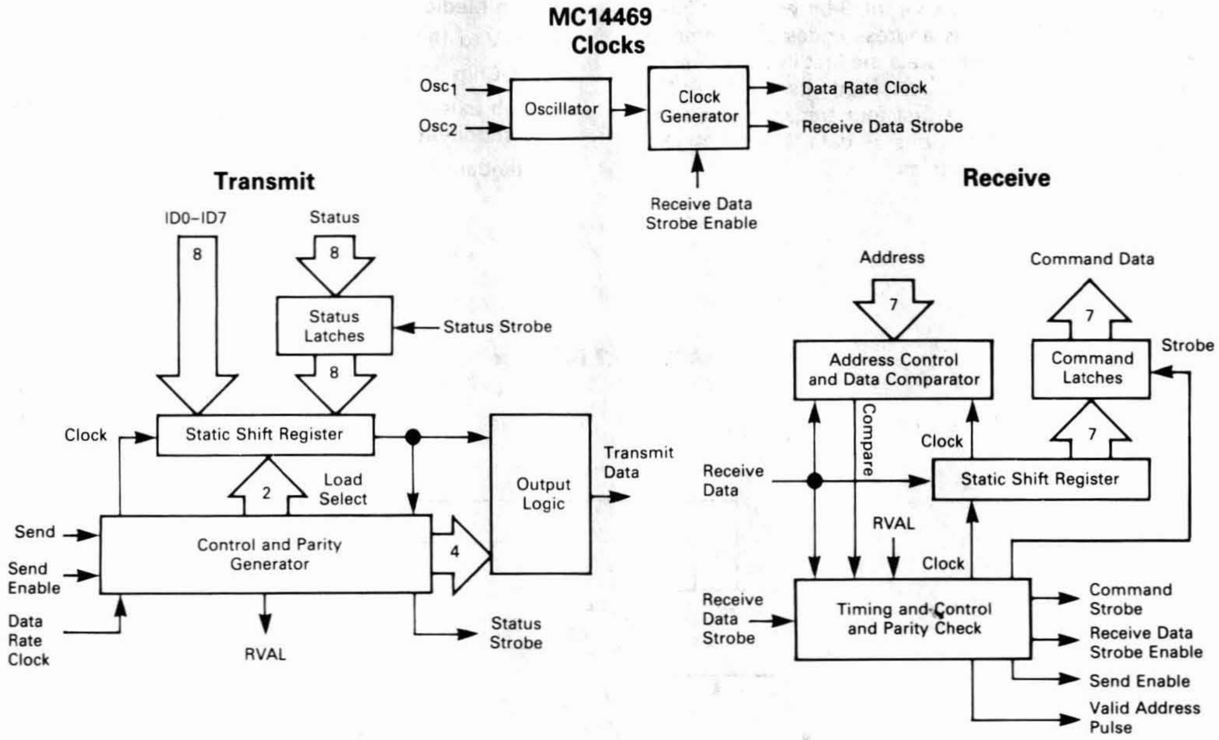

+9.0 Vdc
1500 µF
1N 4001
455 kHz
27
270
100
MPS 6562
100
1.0 k
LED
220
MPS 5172
18
12
13
17
2
16
14
11
4
5
6
7
3
9
8
MC14497
1N 914
(3) MLED71 Infrared Emitting Diodes
+12 Vdc
(2) 1N914
10 µF
0.1
100 k
500
1.0 k
0.002
150 k
0.001
LITRONIX SFH206 Receiver Diode
3
7
8
4
MC3373
1
5
6
2
0.47
0.01
+5.0 Vdc
180 k
18 k
Output
1N 914
MPS 5172
0.001

## Addressable Asynchronous System

### MC14469 Receiver/Transmitter (CMOS)

For application in transmitting data from remote A-to-D converters, remote MPUs or remote digital transducers to the master computer or MPU. Features:

- Supply Voltage Range — 4.5 Vdc to 18 Vdc
- Low Quiescent Current — 75 $\mu$Adc maximum @ 5 Vdc
- Data Rates to 4800 Baud @ 5 V, to 9600 Baud @ 12 V
- Receive — Serial to Parallel
  Transmit — Parallel to Serial
- Transmit and Receive Simultaneously in Full Duplex
- Crystal or Resonator Operation for On-Chip Oscillator

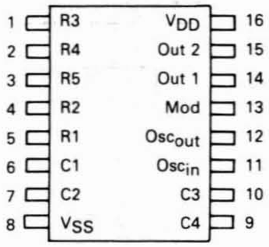

MC14469
Clocks
Osc1
Osc2
Oscillator
Clock Generator
Data Rate Clock
Receive Data Strobe
Receive Data Strobe Enable
Transmit
ID0–ID7
Status
8
8
8
Status Latches
Status Strobe
Clock
Static Shift Register
2
Load Select
Output Logic
Transmit Data
Send
Send Enable
Control and Parity Generator
4
Data Rate Clock
RVAL
Status Strobe
Receive
Address
7
Command Data
7
Address Control and Data Comparator
Command Latches
Strobe
Compare
Clock
7
Receive Data
Static Shift Register
RVAL
Clock
Receive Data Strobe
Timing and Control and Parity Check
Command Strobe
Receive Data Strobe Enable
Send Enable
Valid Address Pulse

## Transmitter-Receiver

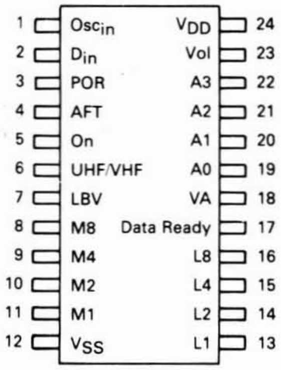
### MC14457 Transmitter
### MC14458 Receiver

Constructed in CMOS technology, this Transmitter-Receiver pair is designed for ultrasonic or infrared remote control of TV receivers, converters, communications receivers and games. Channel selection up to 16 channels can be done single entry; or, up to 256 channels with double entry.

**MC14457**
**TRANSMITTER**


1 R3
2 R4
3 R5
4 R2
5 R1
6 C1
7 C2
8 VSS
16 VDD
15 Out 2
14 Out 1
13 Mod
12 Oscout
11 Oscin
10 C3
9 C4

**MC14458**
**RECEIVER**


1 Oscin
2 Din
3 POR
4 AFT
5 On
6 UHF/VHF
7 LBV
8 M8
9 M4
10 M2
11 M1
12 VSS
24 VDD
23 Vol
22 A3
21 A2
20 A1
19 A0
18 VA
17 Data Ready
16 L8
15 L4
14 L2
13 L1

## Encoder/Decoder Pairs (CMOS)

### MC145026 Encoder
### MC145027 Decoder
### MC145028 Decoder
### MC145029 Decoder

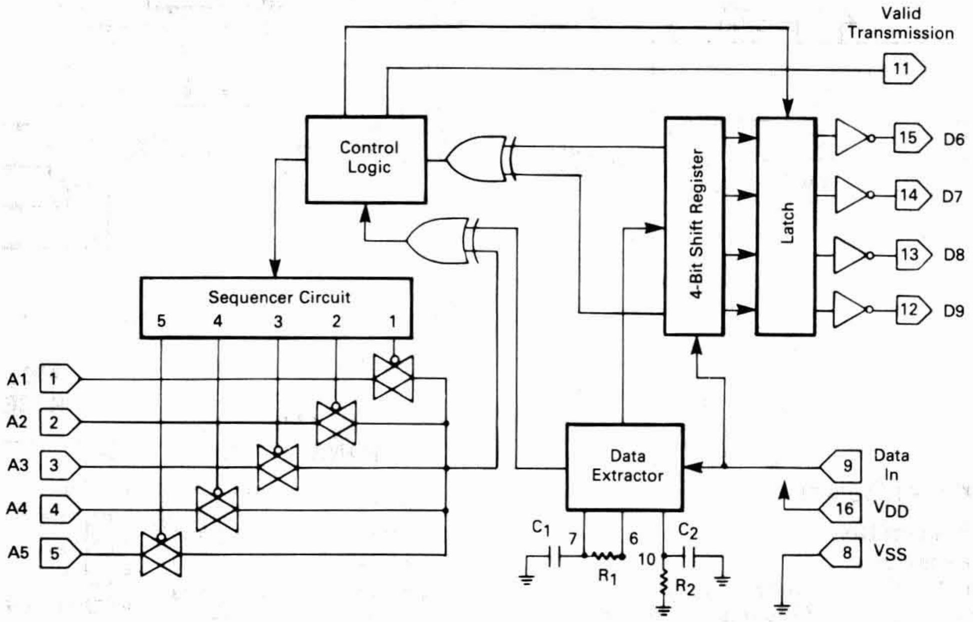
The MC145026 encodes nine bits of information and serially transmits this information. The nine inputs may be encoded with trinary data (0, 1, open) allowing 19,683 different codes.

The three decoders receive the 9-bit word and interpret some of the bits as address codes and some as data. The MC145027 interprets the first five transmitted bits as address and the last four bits as data. The MC145029 interprets the first four transmitted bits as address and the last five bits as data. The MC145028 treats all nine bits as address.

Features:

- Interfaces with RF, Ultrasonic, or Infrared Transmission Media
- 4.5 V to 18 V Operation
- On-Chip RC Oscillator; No Crystal Required
- High External Component Tolerance; Can use ±5% Components
- Standard B-Series Input and Output Characteristics

**MC145027 Decoder**



Valid Transmission
11
Control Logic
4-Bit Shift Register
Latch
15
D6
14
D7
13
D8
12
D9
Sequencer Circuit
5
4
3
2
1
A1
1
A2
2
A3
3
A4
4
A5
5
Data Extractor
9
Data In
16
$V_{DD}$
8
$V_{SS}$
$C_1$
7
6
$C_2$
10
$R_1$
$R_2$

## Timing Circuits

These highly stable timers are capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The output structure can source or sink up to 200 mA or drive TTL circuits. Timing intervals from microseconds through hours can be obtained. The typical timing error for the MC1555 is 0.5%, for the MC1455, 1.0%.

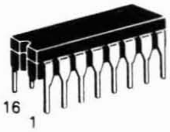
### Singles

**MC1555G,U** ($T_A$ = −55 to +125°C)
**MC1455G, P1,U** ($T_A$ = 0 to +70°C)
Case 601, Case 626, Case 693

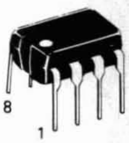
### Duals

**MC3556L** ($T_A$ = −55 to +125°C)
**MC3456L,P** ($T_A$ = 0 to +70°C)
Case 632, Case 646

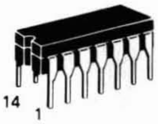
CASE 601
METAL



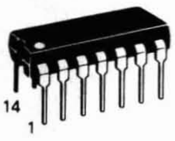
CASE 620
CERAMIC



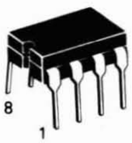
CASE 626
PLASTIC



CASE 632
CERAMIC
(MO-001AA)



CASE 646
PLASTIC



CASE 693
CERAMIC

## Multipliers

Multipliers are designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square, root-mean-square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/MC1494 is a Variable Transconductance Multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

**MC1594L** ($T_A$ = −55 to +125°C)
**MC1494L** ($T_A$ = 0 to +70°C)
Case 620

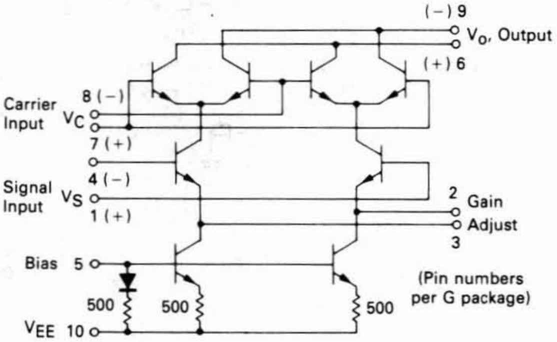
The MC1595L/1495L is similar to the above, but without internal level shift and voltage regulator circuits.

**MC1595L** ($T_A$ = −55 to +125°C)
**MC1495L** ($T_A$ = 0 to +70°C)
Case 632

## Balanced Modulator-Demodulator

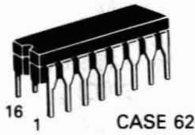
Balanced Modulator-Demodulators are designed for use in circuits where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection and chopper application.

**MC1596G,L** ($T_A$ = −55 to +125°C)
**MC1496G,L,P** ($T_A$ = 0 to +70°C)
Case 603, Case 632, Case 646

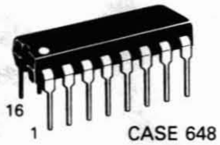


# CMOS Miscellaneous

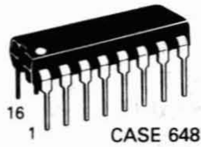
Additional CMOS devices provide specialized analog functions for smoke detectors, automotive and industrial control applications. As with other analog devices, designs are greatly simplified by providing many key functions in a single package.



CASE 620
CERAMIC



CASE 648
PLASTIC



CASE 648B*
PLASTIC

*Pins 15 and 16 are connected via a metal shorting bar.

## Smoke Detectors

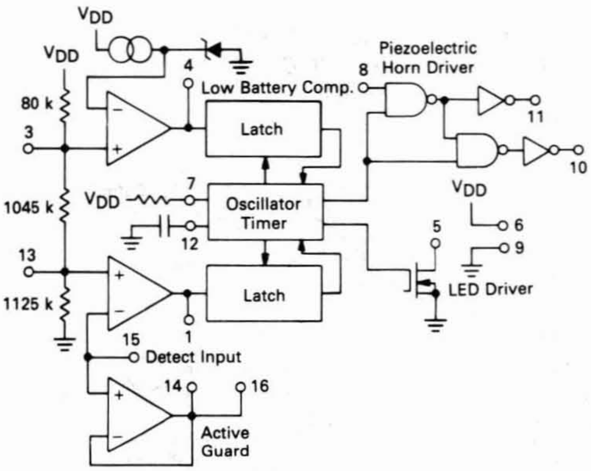
These ionization-type smoke detector ICs require a minimum number of external components. When smoke is sensed or a low battery level is detected, an alarm is sounded via an external piezoelectric transducer. These devices are designed to comply with the UL specification.

**MC14466P1** — Lowest cost version. Requires clipping of external shorting bar on the package after assembly in the PC board. Special handling required to avoid damage due to electrostatic discharge. In Case 648B.

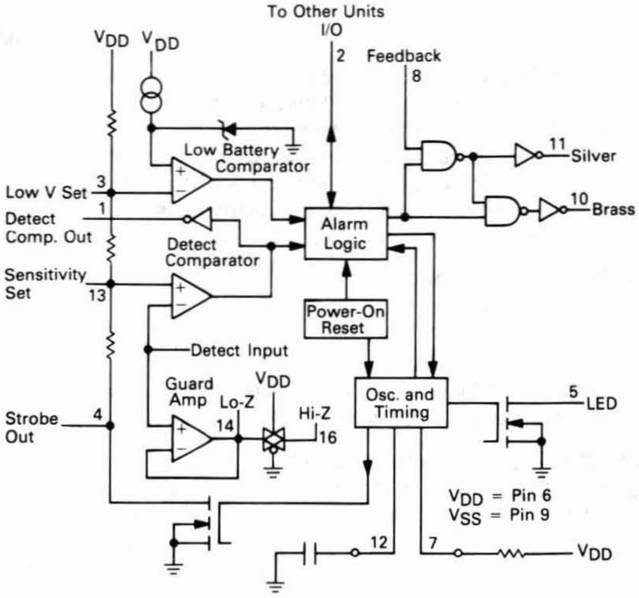
**MC14467P1** — Has protection network on the Detect input. Standard package, with no shorting bar. More immune to electrostatic discharge damage than MC14466P1. In Case 648.

**MC14468P** — Allows up to 40 units to be interconnected for common signalling. Electrostatic discharge protection similar to that of the MC14467P1. In Case 648.

**MC14466P1/MC14467P1**


$V_{DD}$
$V_{DD}$
80 k
3
1045 k
13
1125 k
4
Low Battery Comp.
8
Piezoelectric Horn Driver
11
10
Latch
7
$V_{DD}$
Oscillator Timer
12
Latch
$V_{DD}$
5
6
9
LED Driver
15
1
Detect Input
14
16
Active Guard

**MC14468P**


To Other Units
I/O
2
Feedback
8
$V_{DD}$
$V_{DD}$
Low Battery Comparator
Low V Set
3
1
Detect Comp. Out
Detect Comparator
Sensitivity Set
13
Alarm Logic
11
Silver
10
Brass
Power-On Reset
Detect Input
Guard Amp
Lo-Z
$V_{DD}$
Hi-Z
14
16
Strobe Out
4
Osc. and Timing
5
LED
$V_{DD}$ = Pin 6
$V_{SS}$ = Pin 9
12
7
$V_{DD}$

## Automotive Speed Control Processor

**MC14460,** Case 648

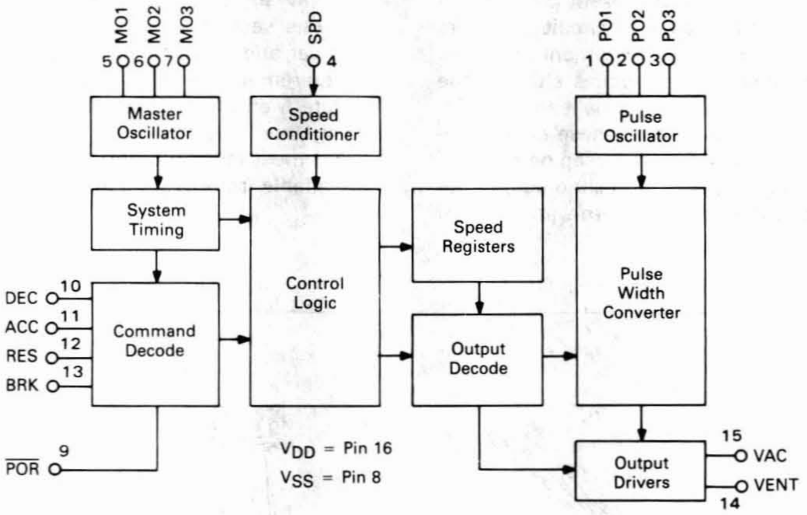
This device is designed to measure vehicle speed and provide pulse-width modulated outputs to trim a throttle positioning servo to maintain an internally stored reference speed.

The stored reference speed can be altered by the DECEL and ACCEL driver commands. The DECEL command trims down the speed, while ACCEL trims up the speed.

A BRAKE input is provided to turn off the outputs with a RESUME driver command to return the vehicle to the last stored speed. Features:

- Internal Redundant Brake and Minimum Speed Checks
- Acceleration Rates Controlled During ACCEL and RESUME Modes of Operation
- Low Frequency Speed Sensors Used
- No Throttle Position Feedback Required
- Power-On Reset
- Low Power Dissipation

**MC14460**



MO1
MO2
MO3
5
6
7
SPD
4
PO1
PO2
PO3
1
2
3
Master Oscillator
Speed Conditioner
Pulse Oscillator
System Timing
Control Logic
Speed Registers
Pulse Width Converter
DEC
ACC
RES
BRK
10
11
12
13
Command Decode
Output Decode
POR
9
VDD = Pin 16
VSS = Pin 8
Output Drivers
15
VAC
VENT
14

## Relay-Contact Bounce Eliminator

**MC14490,** Case 648

. . . designed to eliminate the extraneous signal variations resulting from interfacing with mechanical contacts.

The circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. It removes bounce on both the "make" and the "break" of a contact closure. The clock for operation of the MC14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay).

## Industrial Control Unit

**MC14500B,** Case 620, Case 648

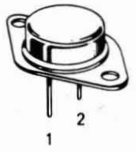
The MC14500B Industrial Control Unit is a one-bit processor that operates over a full voltage and temperature range of CMOS JEDEC B-Series parts, and has a peripheral family including over 100 parts. It can be applied in a multitude of systems, for example as a PLC (low cost) programmable logic controls, control systems, or as an MPU companion for unloading overtaxed microprocessors.

# Power Supply Circuits

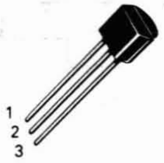
Page
Fixed Output Voltage . . . . . . . . . . . . . . . . . . . . . . . 2-19
Adjustable Output Voltage . . . . . . . . . . . . . . . . . . 2-22
Switching Regulators . . . . . . . . . . . . . . . . . . . . . . . 2-23
Special Regulators . . . . . . . . . . . . . . . . . . . . . . . . 2-24

Power Supplies have changed . . . and are still changing. Today's sophisticated computing equipment no longer tolerates the output voltage and current swings that were acceptable to the less demanding applications of yesteryear. The shrinking space requirements for electronic equipment, made possible by LSI and VLSI circuitry, demand equivalent size and weight reductions for power supplies, and the ever-present pressure on costs poses a continual challenge to circuit designers and component suppliers. The development and rapid penetration of switching power supplies attest to the success of designers in meeting the challenge. The increased component complement for these designs indicates that component suppliers are keeping pace.

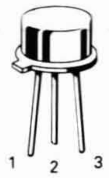
Since the inception of solid-state technology, Motorola's product portfolio supported the advance of power-supply design trends. From the first press-fit rectifiers (whose low cost precipitated the conversion from the generator to the alternator in automotive applications) to the Switchmode and Power BIMOS regulator and control components, Motorola has provided the means with which to implement the designers' plans. The wealth of integrated circuits dedicated to power-supply and power conversion applications is detailed in this section. The accompanying rectifiers, zeners, power and small-signal transistors that round out the requirements for today's designs are listed in their separate Motorola Discrete Components selector guides. Together, these products represent the most complete and most competitive power-supply component lines available from the industry.



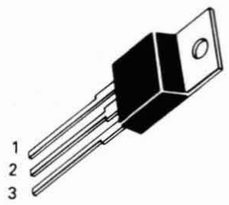
CASE 1
METAL



CASE 29
PLASTIC



CASE 79
METAL



CASE 221A
PLASTIC POWER

# Power Supply Voltage Regulators

## Fixed Output Voltage Regulators

These low-cost monolithic circuits have a positive and/or negative regulation at currents from 100 mA to 3.0 A. They are ideal for on-card regulation of subsystems. They employ current limiting, thermal shutdown, and safe-area compensation.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

### Fixed/Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies

| $V_{out}$ Volts | Tol.† Volts | $I_O$ mA Max | Device Positive Output | Device Negative Output | $V_{in}$ Min/Max | $Reg_{line}$ mV | $Reg_{load}$ mV | $\Delta V_O/\Delta T$ mV/°C Typ | Case |
|---|---|---|---|---|---|---|---|---|---|
| 2 | ±0.1 | 1500 | — | MC7902C | 5.5/35 | 40 | 120 | 1.0 | 1, 221A |
| 5 | ±0.5 | 100 | MC78L05C | MC79L05C | 6.7/30 | 200 | 60 | — | 29, 79 |
| | ±0.25 | | MC78L05AC | MC79L05AC | | 150 | | | |
| | | 500 | MC78M05C | MC79M05C | 7/35 | 100 | 100 | 1.0 | 79, 221A |
| | ±0.4 | 1500 | LM109 | — | | | | 1.1 | 1, 79 |
| | | | LM209 | — | | | | | |
| | ±0.25 | | LM309 | — | | 50 | | 1.0 | |
| | ±0.35 | | MC7805* | — | 8.0/35 | | | 0.6 | 1 |
| | ±0.25 | | MC7805B# | — | 8/35 | 100 | | 1.0 | 1, 221A |
| | | | MC7805C | MC7905C | 7/35 | | | | |
| | ±0.2 | | MC7805A* | — | 7.5/35 | 10 | 50 | 0.6 | 1 |
| | | | MC7805AC | MC7905AC | | | 100 | | 1, 221A |
| | ±0.25 | | LM140-5* | — | 7.0/35 | 50 | 50 | | 1 |
| | ±0.2 | | LM140A-5* | — | | 10 | 25 | | |
| | ±0.25 | | LM340-5 | — | | 50 | 50 | | 1, 221A |
| | ±0.2 | | LM340A-5 | — | | 10 | 25 | | |
| | ±0.1 | | TL780-05C | — | 7.0/35 | 5.0 | 25 | 0.06 | 221A |
| | ±0.25 | 3000 | MC78T05* | — | 7.3/35 | 25 | 30 | 0.1 | 1 |
| | | | MC78T05C | — | | | | | |
| | ±0.2 | | | | | | | | 1, 221A |
| | | | MC78T05A* | — | | 10 | 25 | | 1 |
| | | | MC78T05AC | — | | | | | 1, 221A |
| | ±0.4 | | LM123* | — | 7.5/20 | 25 | 100 | | 1 |
| | | | LM223 | — | | | | | |
| | ±0.25 | | LM323 | — | | | | | 221A |
| | ±0.2 | | LM123A | — | | | | | 1 |
| | | | LM223A | — | | 15 | 50 | | |
| | | | LM323A | — | | | | | 221A |
| 5.2 | ±0.26 | 1500 | — | MC7905.2C | 7.2/35 | 105 | 105 | 1.0 | 1, 221A |

#$T_J$ = −40 to +125°C †Output Voltage Tolerance for Worst Case

*$T_J$ = −55 to +150°C

(continued)

## Fixed Output Voltage Regulators (continued)

| $V_{out}$ Volts | Tol.† Volts | $I_O$ mA Max | Device Positive Output | Device Negative Output | $V_{in}$ Min/Max | $Reg_{line}$ mV | $Reg_{load}$ mV | $\Delta V_O/\Delta T$ mV/°C Typ | Case |
|---|---|---|---|---|---|---|---|---|---|
| 6 | ±0.3 | 500 | MC78M06C | | 8/35 | 100 | 120 | 1.0 | 79, 221A |
| | ±0.35 | 1500 | MC7806* | — | 9/35 | 60 | 100 | 0.7 | 1 |
| | ±0.3 | | MC7806B# | — | 9/35 | 120 | 120 | | 1, 221A |
| | | | MC7806C | MC7906C | 8/35 | | | | |
| | ±0.24 | | MC7806A* | — | 8.6/35 | 11 | 50 | | 1 |
| | | | MC7806AC | — | | | 100 | | 1, 221A |
| | ±0.3 | | LM140-6* | — | 8/35 | 60 | 60 | | 1 |
| | | | LM340-6 | — | | | | | 1, 221A |
| | | 3000 | MC78T06* | — | 8.3/35 | 30 | 30 | 0.12 | 1 |
| | | | MC78T06C | — | | | | | 1, 221A |
| 8 | ±0.8 | 100 | MC78L08C | — | 9.7/30 | 200 | 80 | — | 29, 79 |
| | | | MC78L08AC | — | | 175 | | | |
| | ±0.4 | 500 | MC78M08C | — | 10/35 | 100 | 160 | 1.0 | 79, 221A |
| | | 1500 | MC7808* | — | 11.5/35 | 80 | 100 | | 1 |
| | | | MC7808B# | — | 11.5/35 | 160 | 160 | | 1, 221A |
| | | | MC7808C | MC7908C | 10.5/35 | | | | |
| | ±0.3 | | MC7808A* | — | 10.6/35 | 13 | 50 | | 1 |
| | | | MC7808AC | — | | | 100 | | 1, 221A |
| | ±0.4 | | LM140-8* | — | 10.5/35 | 80 | 80 | | 1 |
| | | | LM340-8 | — | | | | | 1, 221A |
| | | 3000 | MC78T08* | — | 10.4/35 | 35 | 30 | 0.16 | 1 |
| | | | MC78T08C | — | | | | | 1, 221A |
| 12 | ±1.2 | 100 | MC78L12C | MC79L12C | 13.7/35 | 250 | 100 | — | 29, 79 |
| | ±0.6 | | MC78L12AC | MC79L12AC | | | | | |
| | | 500 | MC78M12C | MC79M12C | 14/35 | 100 | 240 | 1.0 | 79, 221A |
| | | 1500 | MC7812* | — | 15.5/35 | 120 | 120 | 1.5 | 1 |
| | | | MC7812B# | — | | 240 | 240 | | 1, 221A |
| | | | MC7812C | MC7912C | 14.5/35 | | | | |
| | ±0.5 | | MC7812A* | — | 14.8/35 | 18 | 50 | | 1 |
| | | | MC7812AC | — | | | 100 | | 1, 221A |
| | ±0.6 | | LM140-12* | — | 14.5/35 | 120 | 120 | 1.5 | 1 |
| | ±0.5 | | LM140A-12* | — | | 18 | 32 | | |
| | ±0.6 | | LM340-12 | — | | 120 | 120 | | 1, 221A |
| | ±0.5 | | LM340A-12 | — | | 18 | 32 | | |
| | ±0.24 | | TL780-12C | — | | 5.0 | | 0.15 | 221A |
| | ±0.6 | 3000 | MC78T12* | — | 14.5/35 | 45 | 30 | 0.24 | 1 |
| | | | MC78T12C | — | | | | | 1, 221A |
| | ±0.5 | | MC78T12A* | — | | 18 | 25 | | 1 |
| | | | MC78T12AC | — | | | | | 1, 221A |

#$T_J$ = −40 to +125°C    †Output Voltage Tolerance for Worst Case    (continued)

*$T_J$ = −55 to +150°C

## Fixed Output Voltage Regulators (continued)

| $V_{out}$ Volts | Tol.† Volts | $I_O$ mA Max | Device Positive Output | Device Negative Output | $V_{in}$ Min/Max | $Reg_{line}$ mV | $Reg_{load}$ mV | $\Delta V_O/\Delta T$ mV/°C Typ | Case |
|---|---|---|---|---|---|---|---|---|---|
| 15 | ±1.5 | 100 | MC78L15C | MC78L15C | 16.7/35 | 300 | 150 | — | 29, 79 |
| | ±0.75 | | MC78L15AC | MC78L15A | | | | | |
| | | 500 | MC78M15C | MC79M15C | 17/35 | 100 | 300 | 1.0 | 79, 221A |
| | | 1500 | MC7815* | — | 18.5/35 | 150 | 150 | 1.8 | 1 |
| | | | MC7815B# | — | | 300 | 300 | | 1, 221A |
| | | | MC7815C | MC7915C | 17.5/35 | | | | |
| | ±0.6 | | MC7815A* | — | 17.9/35 | 22 | 50 | | 1 |
| | | | MC7815AC | — | | | 100 | | 1, 221A |
| | ±0.75 | | LM140-15* | — | 17.5/35 | 150 | 150 | | 1 |
| | ±0.6 | | LM140A-15* | — | | 22 | 35 | | |
| | ±0.75 | | LM340-15 | — | | 150 | 150 | | 1, 221A |
| | ±0.6 | | LM340A-15 | | | 22 | 35 | | |
| | ±0.3 | | TL780-15C | — | | 15 | 60 | 0.18 | 221A |
| | ±0.75 | 3000 | MC78T15* | — | 17.5/40 | 55 | 30 | 0.3 | 1 |
| | | | MC78T15C | — | | | | | 1, 221A |
| | ±0.6 | | MC78T15A* | — | | 22 | 25 | | 1 |
| | | | MC78T15AC | — | | | | | 1, 221A |
| 18 | ±1.8 | 100 | MC78L18C | MC79L18C | 19.7/35 | 325 | 170 | — | 29, 79 |
| | ±0.9 | | MC78L18AC | MC79L18AC | | | | | |
| | | 500 | MC78M18C | — | 20/35 | 100 | 360 | 1.0 | 79, 221A |
| | | 1500 | MC7818* | — | 22/35 | 180 | 180 | 2.3 | 1 |
| | | | MC7818B# | — | | 360 | 360 | | 1, 221A |
| | | | MC7818C | MC7918C | 21/35 | | | | |
| | ±0.7 | | MC7818A* | — | | 31 | 50 | | 1 |
| | | | MC7818AC | — | | | 100 | | 1, 221A |
| | ±0.9 | | LM140-18* | — | | 180 | 180 | | 1 |
| | | | LM340-18 | — | | | | | 1, 221A |
| | | 3000 | MC78T18* | — | 20.6/40 | 80 | 30 | 0.36 | 1 |
| | | | MC78T18C | — | | | | | 1, 221A |
| 20 | ±1.0 | 500 | MC78M20C | — | 22/40 | 10 | 400 | 1.1 | 79, 221A |
| 24 | ±2.4 | 100 | MC78L24C | MC79L24C | 25.7/40 | 350 | 200 | — | 29, 79 |
| | ±1.2 | | MC78L24AC | MC79L24AC | | 300 | | | |
| | | 500 | MC78M24C | | 26/40 | 100 | 480 | 1.2 | 79, 221A |
| | | 1500 | MC7824* | — | 28/40 | 240 | 240 | 3.0 | 1 |
| | | | MC7824B# | — | | 480 | 480 | | 1, 221A |
| | | | MC7824C | MC7924C | 27/40 | | | | |
| | ±1.0 | | MC7824A* | — | 27.3/40 | 36 | 50 | | 1 |
| | | | MC7824AC | — | | | 100 | | 1, 221A |
| | ±1.2 | | LM140-24* | — | | 240 | 240 | | 1 |
| | | | LM340-24 | — | | | | | 1, 221A |
| | | 3000 | MC78T24* | | 26.7/40 | 90 | 30 | 0.48 | 1 |
| | | | MC78T24C | | | | | | 1, 221A |

#$T_J$ = −40 to +125°C  *$T_J$ = −55 to +150°C  †Output Voltage Tolerance for Worst Case

# Adjustable Output Voltage Regulators

Motorola offers a broad line of adjustable output voltage regulators with a variety of output current capabilities. Adjustable voltage regulators provide users the capability of stocking a single integrated circuit providing a wide range of output voltages for industrial and communications applications. The three-terminal devices require only two external resistors to set the output voltage.

## Positive Output Regulators

| $I_O$ mA Max | Device | Suffix | $V_{out}$ Volts |  | $V_{in}$ Volts |  | $V_{in}$ — $V_{out}$ Differential Volts Min | $P_D$ Watts Max |  | Regulation % $V_{out}$ @ $T_A$ = 25°C Max |  | TC $V_{out}$ Typ %/°C | $T_J$ = °C Max | Case |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  |  |  | Min | Max | Min | Max |  | $T_A$ = 25°C | $T_C$ = 25°C | Line | Load |  |  |  |
| 100 | LM317L | H,Z | 1.2 | 37 | 5.0 | 40 | 3.0 | Internally Limited |  | 0.04 | 0.5 | 0.006 | 125 | 29, 79 |
|  | LM217L# |  |  |  |  |  |  |  |  | 0.02 | 0.3 | 0.004 | 150 |  |
|  | LM117L* |  |  |  |  |  |  |  |  |  |  | 0.003 |  |  |
| 150 | MC1723 | CP | 2.0 | 37 | 9.5 | 40 | 3.0 | 1.25 | — | 0.1 | 0.3 | 0.003 | 150 | 646 |
|  |  | CG |  |  |  |  |  | 1.0 | 2.1 |  |  | 0.003 |  | 603C |
|  |  | G |  |  |  |  |  |  |  |  |  | 0.002 |  |  |
|  |  | CL |  |  |  |  |  | 1.5 | — |  |  | 0.003 | 175 | 632 |
|  |  | L |  |  |  |  |  |  | — |  |  | 0.002 |  |  |
| 500 | LM317M | T | 1.2 | 37 | 5.0 | 40 | 3.0 | Internally Limited |  | 0.04 | 0.5 | 0.0056 | 125 | 221A |
| 1500 | LM317 | T | 1.2 | 37 | 5.0 | 40 | 3.0 | Internally Limited |  | 0.04 | 0.5 | 0.006 | 125 | 221A |
|  | LM317 | H, K |  |  |  |  |  |  |  |  |  |  |  | 79, 1 |
|  | LM217# |  |  |  |  |  |  |  |  |  |  | 0.004 |  |  |
|  | LM117* |  |  |  |  |  |  |  |  | 0.02 | 0.3 | 0.003 | 150 |  |
| 3000 | LM350 | T | 1.2 | 33 | 5.0 | 36 | 3.0 | Internally Limited |  | 0.03 | 0.5 | 0.008 | 125 | 221A |
|  | LM350 | K |  |  |  |  |  |  |  |  |  |  |  | 1 |
|  | LM250# |  |  |  |  |  |  |  |  | 0.01 | 0.3 | 0.0057 | 150 |  |
|  | LM150* |  |  |  |  |  |  |  |  |  |  | 0.0051 |  |  |

## Negative Output Regulators

| $I_O$ mA Max | Device | Suffix | $V_{out}$ Volts |  | $V_{in}$ Volts |  | $V_{in}$ — $V_{out}$ Differential Volts Min | $P_D$ Watts Max |  | Regulation % $V_{out}$ @ $T_A$ = 25°C Max |  | TC $V_{out}$ Typ %/°C | $T_J$ = °C Max | Case |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  |  |  | Min | Max | Min | Max |  | $T_A$ = 25°C | $T_C$ = 25°C | Line | Load |  |  |  |
| 500 | LM337M | T | −1.2 | −37 | 5.0 | 40 | 3.0 | Internally Limited |  | 0.04 | 1.0 | 0.0048 | 125 | 221A |
| 1500 | LM337 | T | −1.2 | −37 | 5.0 | 40 | 3.0 | Internally Limited |  | 0.04 | 1.0 | 0.0048 | 125 | 221A |
|  | LM337 | H, K |  |  |  |  |  |  |  |  |  |  |  | 79, 1 |
|  | LM237# |  |  |  |  |  |  |  |  | 0.02 | 0.5 | 0.0034 | 150 |  |
|  | LM137* |  |  |  |  |  |  |  |  |  |  | 0.0031 |  |  |

#$T_J$ = −25 to +150°C
*$T_J$ = −55 to +150°C

## Switching Regulators

Used as control circuit in PWM, push-pull, bridge and series type switchmode supplies. The devices include the reference, oscillator, pulse-width modulator, phase splitter and output sections. Frequency and duty cycle are independently adjustable.

| $I_O$ mA Max | $V_{CC}$ Volts | | $f_o$ kHz | | Device | Suffix | $T_A$ °C | Case |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | | | |
| 40 | 1 | 30 | 2.0 | 100 | MC3420 | P | 0 to +70 | 648 |
| | | | | | | L | | 620 |
| | | | | | MC3520 | L | −55 to +125 | 620 |
| 250* | 7.0 | 40 | 1.0 | 300 | MC34060 | P | 0 to +70 | 646 |
| | | | | | | L | | 632 |
| | | | | | MC35060 | L | −55 to +125 | 632 |
| 250 | 7.0 | 40 | 1.0 | 300 | TL494 | CN | 0 to +70 | 648 |
| | | | | | | CJ | | 620 |
| | | | | | | IN | −25 to + 85 | 648 |
| | | | | | | IJ | | 620 |
| | | | | | | MJ | −55 to +125 | 620 |
| 250 | | >40 | 1.0 | 300 | TL495** | CN | 0 to +70 | 707 |
| | | | | | | CJ | | 726 |
| | | | | | | IN | −25 to +85 | 707 |
| | | | | | | IJ | −25 to +85 | 726 |
| ±400 | 8 | 40 | 0.1 | 400 | SG3525A | N | 0° to +70 | 648 |
| | | | | | | J | | 620 |
| | | | | | SG2525A | N | −25 to +85 | 648 |
| | | | | | | J | | 620 |
| | | | | | SG1525A | J | −55 to +125 | 620 |
| ±400 | 8 | 40 | 0.1 | 400 | SG3527A | N | 0 to +70 | 648 |
| | | | | | | J | | 620 |
| | | | | | SG2527A | N | −25 to +85 | 648 |
| | | | | | | J | | 620 |
| | | | | | SG1527A | J | −55 to +125 | 620 |
| ±200 | 8 | 40 | 0.001 | 400 | SG3526 | N | † 0 to +125 | 707 |
| | | | | | | J | | 726 |
| | | | | | SG2526 | N | † −40 to +150 | 707 |
| | | | | | | J | | 726 |
| | | | | | SG1526 | J | † −55 to +150 | 726 |
| 1500* | 2.5 | 40 | 0.1 | 100 | µA78S40 | PC | 0 to +70 | 648 |
| | | | | | | DC | | 620 |
| | | | | | | DM | −55 to +125 | |
| 1500* | 2.5 | 40 | 0.1 | 100 | MC34063 | P1 | 0 to +70 | 626 |
| | | | | | | U | | 693 |
| | | | | | MC33063 | P1 | −40 to +85 | 626 |
| | | | | | | U | | 693 |
| | | | | | MC35063 | U | −55 to +125 | 693 |

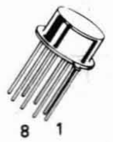
*Single output device

**Internal 39 V zener for < 40 volt operation

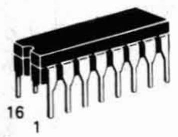
†Junction Temperature Range

## Special Regulators

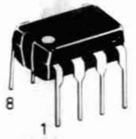
Special voltage regulators are available to provide floating voltage and current regulation, and dual tracking plus and minus voltage regulation.



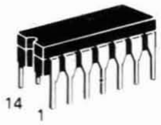
CASE 601
METAL



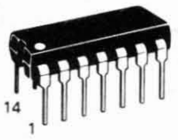
CASE 620
CERAMIC



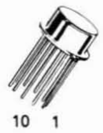
CASE 626
PLASTIC



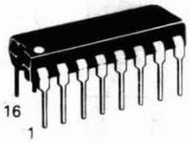
CASE 632
CERAMIC
(MO-001AA)



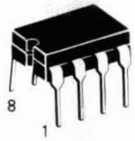
CASE 646
PLASTIC



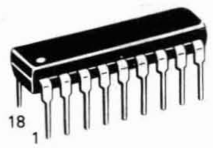
CASE 603C
METAL
(TO-100)



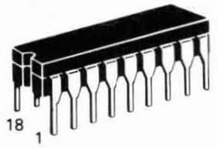
CASE 648
PLASTIC



CASE 693
CERAMIC



CASE 707
PLASTIC



CASE 726
CERAMIC

### Floating Voltage and Current Regulators

Designed for laboratory type power supplies. Voltage is limited only by the break down voltage of associated, external, series-pass transistors.

| $V_{out}$ Volts | | $I_O$ mA | | | $V_{aux}$ Volts | | $P_D$ Watts | $\Delta V_{ref}/V_{ref}$ % | | $\Delta I_L/L_L$ % | TC $V_{out}$ %/°C | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min | Max | Max | Device | Suffix | Min | Max | Max | Line | Load | Max | Typ | Case |
| 0 | * | * | MC1466 | L | 21 | 30 | 0.75 | 0.015 | 0.015 | 0.2 | 0.001 | 632 |
| | | | MC1566 | L | 20 | 35 | | 0.004 | 0.004 | 0.1 | 0.006 | |

*Dependent on characteristics of external series-pass elements.

### Dual ± 15 V Tracking Regulators

Internally, the device is set for ±15 V, but an external adjustment can change both outputs simultaneously, from 8.0 V to 20 V.

| $V_{out}$ Volts | | $I_O$ mA | $V_{in}$ Volts | | | | $P_D$ Watts | $Reg_{line}$ | $Reg_{load}$ | TC %/°C ($T_{low}$ to $T_{high}$) | $T_A$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min | Max | Max | Min | Max | Device | Suffix | Max | mV | mV | Typ | °C | Case |
| 14.8 | 15.2 | ±100 | 17 | 30 | MC1468 | G | 0.8 | 10 | 10 | 3.0 | 0 to +75 | 603C |
| | | | | | | L | 1.0 | | | | | 632 |
| | | | | | MC1568 | G | 0.8 | | | | −55 to +125 | 603C |
| | | | | | | L | 1.0 | | | | | 632 |

# Power Supply Voltage References

## Precision Low-Voltage References

A family of precision low-voltage bandgap reference devices designed for applications requiring low temperature drift.

| $V_{out}$ Volts Typ | $I_O$ mA Max | $\Delta V_{out}/\Delta T$ ppm/°C Max | Device | $Reg_{line}$ mV Max | $Reg_{load}$ mV Max | $T_A$ °C | Case |
|---|---|---|---|---|---|---|---|
| 1.235 ± 12 mV | 20 | 20 Typ | LM385BZ-1.2 | (Note 1) | 1.0 (Note 2) | 0 to +70 | 29 |
| | | | LM285Z-1.2 | | | −40 to +85 | |
| 1.235 ± 25 mV | | | LM385Z-1.2 | | | 0 to +70 | |
| 2.5 ± 38 mV | | | LM385BZ-2.5 | | 2.0 (Note 3) | | |
| | | | LM285Z-2.5 | | | −40 to +85 | |
| 2.5 ± 75 mV | | | LM385Z-2.5 | | | 0 to +70 | |
| 2.5 ± 5.0 mV | ±10 | 25 | MC1400G2 | 3.0 (Note 4) | 10 (Note 7) | 0 to +70 | 601 |
| | | 10 | MC1400AG2 | | | | |
| | | 40 | MC1500G2 | | | −55 to +125 | |
| | | 10 | MC1500AG2 | | | | |
| 2.5 ± 25 mV | 10 | 40 | MC1403 | 3.0/4.5 (Note 5) | 10 (Note 8) | 0 to +70 | 693, 79 |
| | | 25 | MC1403A | | | | 693, 79 |
| | | 55 | MC1503 | | | −55 to +125 | |
| | | 25 | MC1503A | | | | |
| 5.0 ± 10 mV | ±10 | 25 | MC1400G5 | 4.0 (Note 4) | 20 (Note 7) | 0 to +70 | 693 |
| | | 10 | MC1400AG5 | | | | |
| | | 40 | MC1500G5 | | | −55 to +125 | |
| | | 10 | MC1500AG5 | | | | |
| 5.0 ± 50 mV | 10 | 40 | MC1404U5 | 6.0 (Note 6) | 10 (Note 8) | 0 to +70 | |
| | | 25 | MC1404AU5 | | | | |
| | | 55 | MC1504U5 | | | −55 to +125 | |
| | | 25 | MC1504AU5 | | | | |
| 6.25 ± 10 mV | ±10 | 25 | MC1400G6 | 4.0 (Note 4) | 20 (Note 7) | 0 to +70 | 601 |
| | | 10 | MC1400AG6 | | | | |
| | | 40 | MC1500G6 | | | −55 to +125 | |
| | | 10 | MC1500AG6 | | | | |
| 6.25 ± 60 mV | 10 | 40 | MC1404U6 | 6.0 (Note 6) | 10 (Note 8) | 0 to +70 | 693 |
| | | 25 | MC1404AU6 | | | | |
| | | 55 | MC1504U6 | | | −55 to +125 | |
| | | 25 | MC1504AU6 | | | | |
| 10 ± 20 mV | ±10 | 25 | MC1400G10 | 4.0 (Note 4) | 20 (Note 7) | 0 to +70 | 601 |
| | | 10 | MC1400AG10 | | | | |
| | | 40 | MC1500G10 | | | −55 to +125 | |
| | | 10 | MC1500AG10 | | | | |
| 10 ± 100 mV | 10 | 40 | MC1404U10 | 6.0 (Note 6) | 10 (Note 8) | 0 to +70 | 693 |
| | | 25 | MC1404AU10 | | | | |
| | | 55 | MC1504U10 | | | −55 to +125 | |
| | | 25 | MC1504AU10 | | | | |
| 2.5 to 37 | 100 | 50 Typ | TL431C | Shunt Reference Dynamic Impedance $z \leq 0.5\ \Omega$ | | 0 to +70 | 29,626,693 |
| | | | TL431I | | | −40 to +85 | |
| | | | TL431M | | | −55 to +125 | 693 |

Notes:
1. Micro-Power Reference Diode Dynamic Impedance (z) ≤ 1.0 Ω at $I_R$ = 100 μA
2. 10 μA ≤ $I_R$ ≤ 1.0 mA
3. 20 μA ≤ $I_R$ ≤ 1.0 mA
4. ($V_{out}$ + 1.0 V) ≤ $V_{in}$ ≤ 40 V
5. 4.5 V ≤ $V_{in}$ ≤ 15 V 15 V ≤ $V_{in}$ ≤ 40 V
6. ($V_{out}$ + 2.5 V) ≤ $V_{in}$ ≤ 40 V
7. −10 mA ≤ $I_L$ ≤ + 10 mA
8. 0 mA ≤ $I_L$ ≤ 10 mA

# Power Supply Supervisory Circuits

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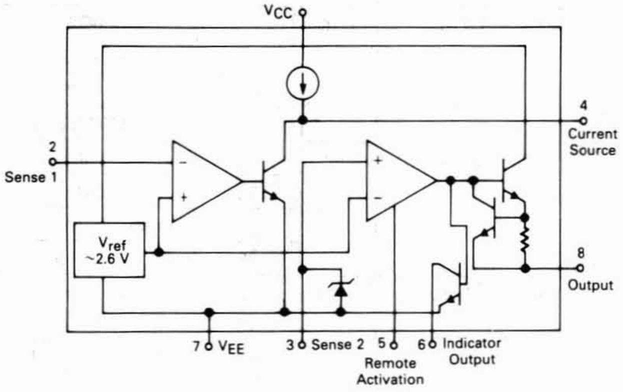
## Overvoltage "Crowbar" Sensing Circuit

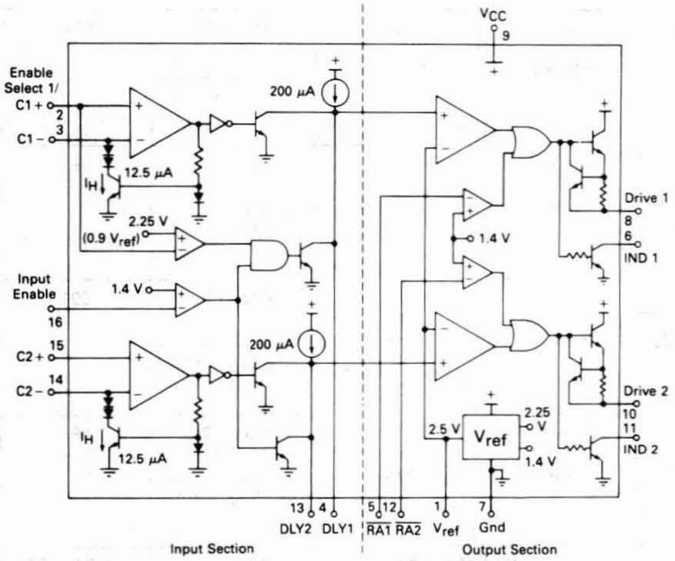
This device can protect sensitive circuitry from power supply transients or regulator failure when used with an external "Crowbar" SCR. The device senses voltage and compares it to an internal 2.6 V reference. Overvoltage trip is adjustable by means of an external resistive voltage divider. A minimum duration before trip is programmable with an external capacitor. Other features include a 300 mA high current output for driving the gate of a "Crowbar" SCR, an open-collector indicator output and remote activation capability.

**MC3523U** ($T_A$ = −55 to +125°C)
**MC3423P1,U** ($T_A$ = 0 to +70°C)

Packages: P1 Suffix, Case 626 (Plastic)
U Suffix, Case 693 (Ceramic)


VCC
4
Current Source
2
Sense 1
Vref ~2.6 V
8
Output
7 VEE
3 Sense 2
5 Remote Activation
6 Indicator Output

## Dual Voltage Comparator


VCC
9
Enable Select 1/
C1+
2
3
C1−
200 µA
12.5 µA
IH
2.25 V
(0.9 Vref)
Input Enable
16
1.4 V
15
C2+
14
C2−
200 µA
IH
12.5 µA
Drive 1
8
6
IND 1
1.4 V
Drive 2
10
11
IND 2
2.5 V
Vref
2.25 V
1.4 V
13
4
5
12
1
7
DLY2
DLY1
RA1
RA2
Vref
Gnd
Input Section
Output Section

**MC3524L,AL** ($T_A$ = −55 to +125°C)
**MC3424L,P,AL,AP** ($T_A$ = 0 to +70°C)
**MC3324P,AP,L,AL** ($T_A$ = −40 to +85°C)

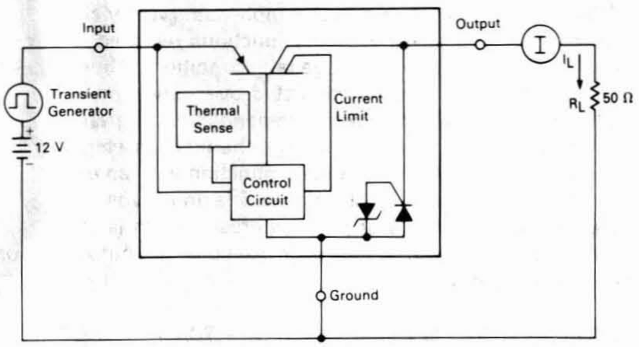
Packages: L Suffix, Case 620 (Ceramic)
P Suffix, Case 648 (Plastic)

This Dual Channel Supervisory Circuit consists of uncommitted differential inputs, an internal reference, and high current outputs. The two differential input channels and the pinned-out reference permit monitoring for over- and under-voltage faults. Three hundred mA of output current for each channel provides sufficient gate drive for "Crowbar" SCR's and 30 mA are available to drive indicator devices. Other features include, programmable hysteresis, activation delay, and remote activation.

## Series Switch Transient Protection Circuit

**MC33031T** $T_J = -40$ to $+125°C$, Case 221A

This device acts as a saturated series pass element with a very low voltage drop for load currents in excess of 750 mA. In the event of an over voltage condition (≥31 V typically) or high voltage transient of either positive or negative polarity, the MC33031T instantaneously switches to an open circuit (OFF) state, interrupting power to the load and protecting the load during this potentially destructive condition. The device will immediately recover to an ON state when supply voltages fall within the normal operating range.


Input
Output
Transient Generator
12 V
Thermal Sense
Current Limit
Control Circuit
$I_L$
$R_L$
50 Ω
Ground

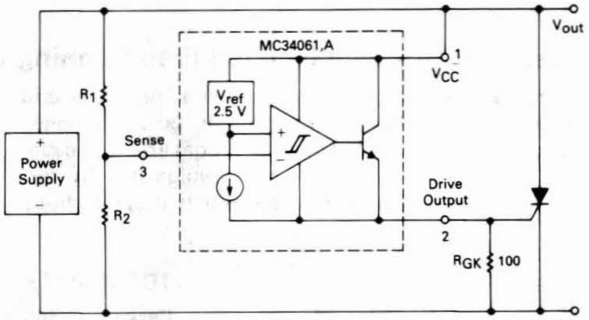
## Over-Voltage Protection Circuits

**MC34061P,AP** ($T_A = 0$ to $+70°C$)

Package: P Suffix, Case 29 (Plastic)

The MC34061,A, overvoltage protection (OVP) circuit, in combination with two external programming resistors and a "crow-bar" SCR protects sensitive electronic circuitry from overvoltage damage. It senses an overvoltage condition and quickly "crow-bars," or short circuits, the supply. An external capacitor may be used to program a minimum overvoltage duration before tripping, thus providing noise immunity.

This three-terminal circuit provides a cost-effective means of protecting either positive or negative power supplies. The unique design of the MC34061,A eliminates trip voltage and temperature drift errors due to SCR gate variations.

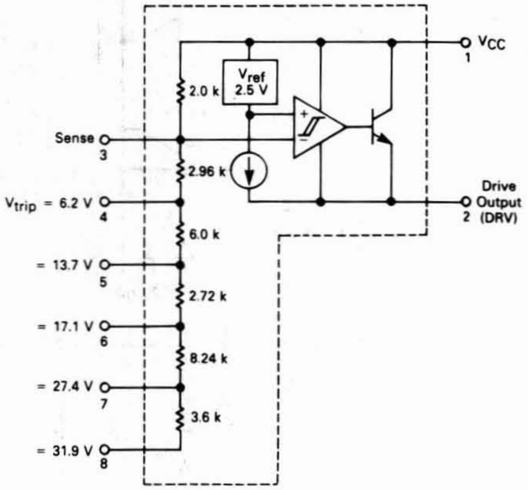

MC34061,A
$V_{out}$
1
$V_{CC}$
$R_1$
$V_{ref}$ 2.5 V
Power Supply
Sense
3
$R_2$
Drive Output
2
$R_{GK}$
100
Gnd

$$V_{trip} = \frac{R_1 + R_2}{R_1}(2.5\ V)$$

**MC34062P1,U** ($T_A = 0$ to $+70°C$)
**MC35062U** ($T_A = -55$ to $+125°C$)

Packages: P1 Suffix, Case 626 (Plastic)
U Suffix, Case 693 (Ceramic)

The MC34062/35062 overvoltage protection (OVP) circuits require only an external "crowbar" SCR to protect sensitive electronic circuitry from overvoltage damage. They sense an overvoltage condition and quickly "crowbar," or short circuit the supply.

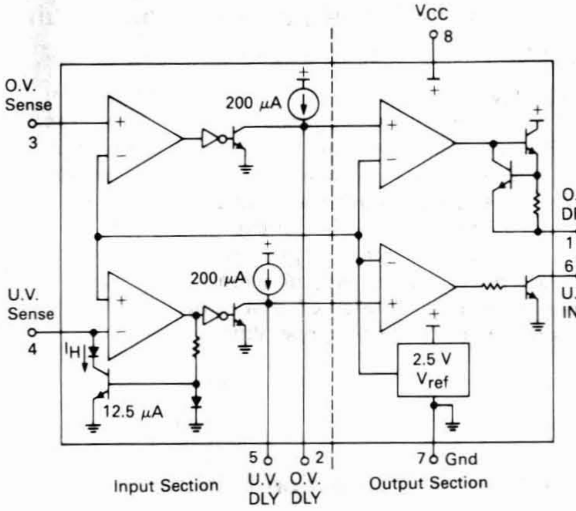

$V_{CC}$
1
2.0 k
$V_{ref}$ 2.5 V
Sense
3
2.96 k
$V_{trip}$ = 6.2 V
4
6.0 k
= 13.7 V
5
2.72 k
= 17.1 V
6
8.24 k
= 27.4 V
7
3.6 k
= 31.9 V
8
Drive Output
2 (DRV)

## Over-Under Voltage Protection Circuit

The MC3425/3525 is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. These integrated circuits contain dedicated over- and under-voltage sensing channels with independently programmable time delays. The over-voltage channel has a high current Drive Output for use in conjunction with an external SCR "Crowbar" for shutdown. The under-voltage channel input comparator has hysteresis which is externally programmable, and an open-collector output for fault indication.

**MC3425P1, AP1,U,AU** ($T_A$ = 0 to +70°C)
**MC3525U,AU** ($T_A$ = −55 to +125°C)

Packages: P1 Suffix, Case 626 (Plastic)
U Suffix, Case 693 (Ceramic)


VCC
8
O.V. Sense
3
200 µA
200 µA
U.V. Sense
4
IH
12.5 µA
O.V. DRV
1
6
U.V. IND
2.5 V Vref
5
2
7 Gnd
Input Section
U.V. DLY
O.V. DLY
Output Section

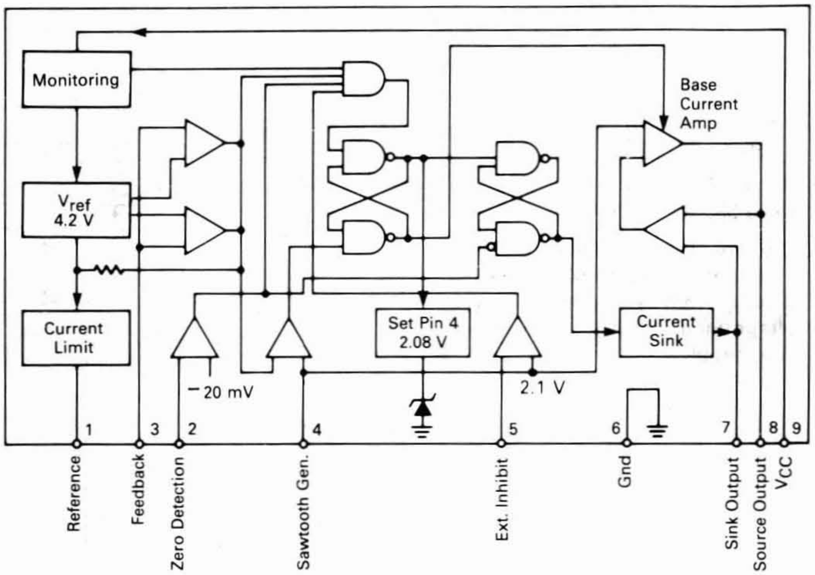
## Control IC for Line Isolated Free Running Flyback Converter

This bipolar integrated circuit drives, regulates and monitors the switching transistor in power supplies based on the free oscillating flyback converter principle.

Wide regulating range and high voltage stability during large load changes provide excellent switchmode performance in Hi-Fi equipment, active loudspeakers, as well as applications in TV receivers and video recorders.

The TDA4600 is available in a 9-pin SIP plastic medium-power package.

**TDA4600** ($T_A$ = −15 to +85°C)
Package P Suffix — Case 762 (Plastic)

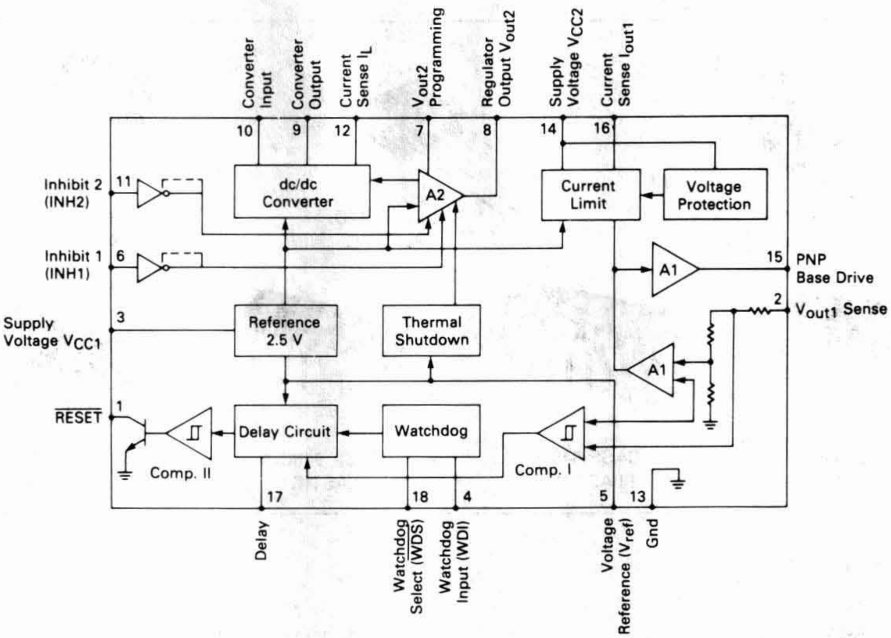

Monitoring
Vref 4.2 V
Current Limit
Base Current Amp
Set Pin 4 2.08 V
Current Sink
−20 mV
2.1 V
1
3
2
4
5
6
7
8
9
Reference
Feedback
Zero Detection
Sawtooth Gen.
Ext. Inhibit
Gnd
Sink Output
Source Output
VCC

## Universal Microprocessor Power Supply Controller

This device is a versatile power supply control circuit for microprocessor based systems and mainly intended for automotive applications and battery powered instruments. To cover a wide range of applications, the device offers high circuit flexibility with minimum of external components.

Functions included in this IC are a temperature compensated voltage reference, on-chip dc/dc converter, programmable and remote controlled voltage regulator, fixed 5.0 V supply voltage regulator with external PNP power device, undervoltage detection circuit, power-on RESET delay and watchdog feature for orderly microprocessor operations.

**TCA5600/TCF5600** ($T_A$ = 0 to +125°C)
Package P Suffix — Case 707 (Plastic)



Converter Input
Converter Output
Current Sense $I_L$
$V_{out2}$ Programming
Regulator Output $V_{out2}$
Supply Voltage $V_{CC2}$
Current Sense $I_{out1}$
10
9
12
7
8
14
16
Inhibit 2 (INH2)
11
dc/dc Converter
A2
Current Limit
Voltage Protection
Inhibit 1 (INH1)
6
15
PNP Base Drive
A1
2
$V_{out1}$ Sense
Supply Voltage $V_{CC1}$
3
Reference 2.5 V
Thermal Shutdown
A1
RESET
1
Delay Circuit
Watchdog
Comp. II
Comp. I
17
18
4
5
13
Delay
Watchdog Select (WDS)
Watchdog Input (WDI)
Voltage Reference ($V_{ref}$)
Gnd

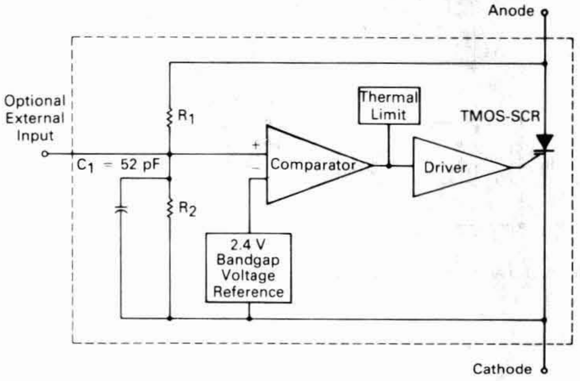
## SMARTpower II Overvoltage and Over Temperature Protector Circuit

### MPC2004/2005/2006/2011/2012/2014/2015

SMARTpower II combines the best qualities of high speed CMOS logic and high current TMOS vertical power structuring on a single chip.

The MPC2000 family of overvoltage and temperature protection circuits are the first family of devices to utilize this new technology. These devices sense and protect sensitive electronics from overvoltage transients or an extreme temperature environment. The circuits sense a fault condition and quickly "crowbar" or short circuit the supply, forcing the supply to current limit/foldback, or they can open a fuse or a circuit breaker.

The devices are available for 5, 12 and 15 volt bus voltages with continuous current ratings of 7.5, 15 and 35 amperes. Depending on the device selected, peak currents up to 350 amperes can be used to discharge capacitors. All devices are housed in the TO-220 package except for the MPC2006.



Anode
Optional External Input
$R_1$
$C_1$ = 52 pF
$R_2$
Thermal Limit
TMOS-SCR
+
−
Comparator
Driver
2.4 V Bandgap Voltage Reference
Cathode

| Continuous Current (Amps) \ Nominal Bus Voltage (Volts) | 5.0 | 12 | 15 |
|---|---|---|---|
| 7.5 | MPC2004 | MPC2011 | MPC2014 |
| 15 | MPC2005 | MPC2012 | MPC2015 |
| 35 | MPC2006* | — | — |

*Indicates TO-204AE Package.

# Power Supply
# Power Controllers

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Motor Control . . . . . . . . . . . . . . . . . . . . . . . . . 2-32
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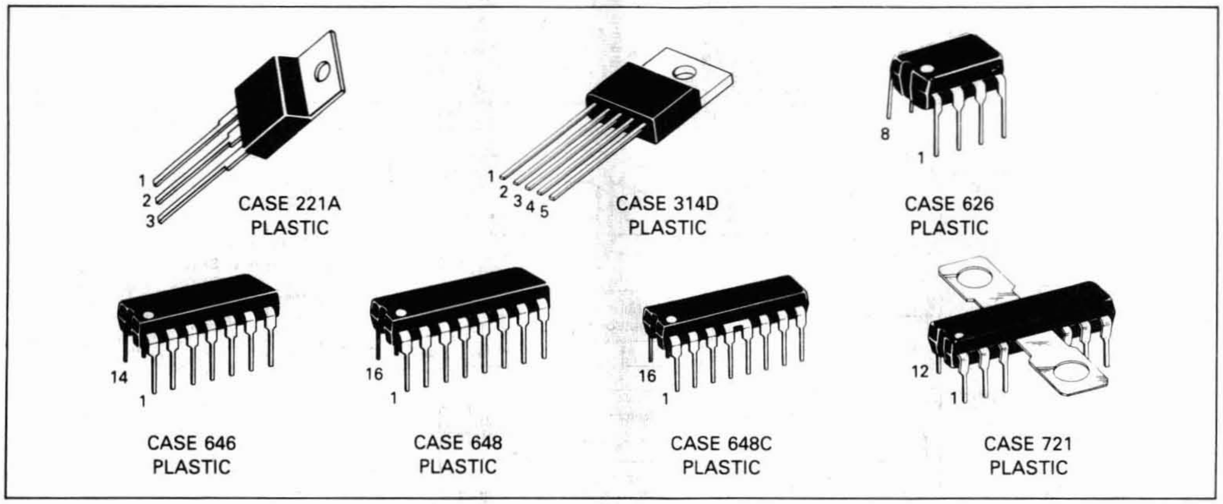
  Universal Motor Speed Controllers . . . . . . . . . . 2-32
  DC Servo Motor Controller/Driver . . . . . . . . . . . 2-33

Several power control circuits are available for zero voltage switching, driving solenoids, and driving loads from a power supply high-side line.

## Power Control



1
2
3
CASE 221A
PLASTIC
1
2
3
4
5
CASE 314D
PLASTIC
8
1
CASE 626
PLASTIC
14
1
CASE 646
PLASTIC
16
1
CASE 648
PLASTIC
16
1
CASE 648C
PLASTIC
12
1
CASE 721
PLASTIC

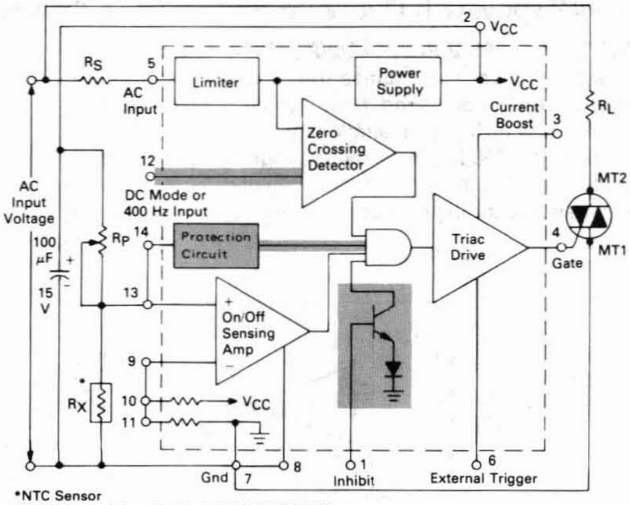
## Zero Voltage Switches

### CA3079P/CA3059P

$T_A = -40$ to $+85°C$, Case 646

. . . designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V @ 50/60 Hz. Features include:

- **Limiter-Power Supply** — Allows operation directly from an ac line.
- **Differential On/Off Sensing Amplifier** — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented.
- **Zero-Crossing Detector** — Synchronizes the output pulses to the zero voltage point of the ac cycle. Eliminates RFI when used with resistive loads.
- **Triac Drive** — Supplies high-current pulses to the external power controlling thyristor.
- **Protection Circuit (CA3059 only)** — A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive circuit from the external triac.
- **Inhibit Capability (CA3059 only)** — Thyristor firing may be inhibited by the action of an internal diode gate.
- **High Power DC Comparator Operation (CA3059 only)** — Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector).



2
VCC
RS
5
AC
Input
Limiter
Power
Supply
VCC
Current
Boost
3
RL
Zero
Crossing
Detector
12
DC Mode or
400 Hz Input
AC
Input
Voltage
MT2
100
μF
15
V
RP
14
Protection
Circuit
Triac
Drive
4
Gate
MT1
13
+
On/Off
Sensing
Amp
−
9
*
RX
10
VCC
11
Gnd
7
8
1
Inhibit
6
External Trigger

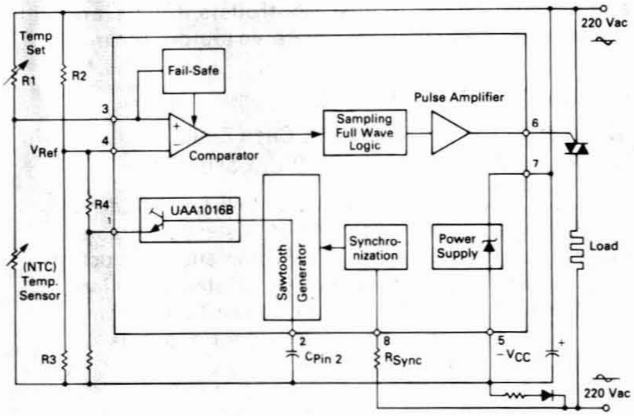
*NTC Sensor
NOTE: Shaded Area Not Included With CA3079.

## Zero Voltage Controller

**UAA1016B** ($T_A$ = −20 to +100°C, Case 626)

. . . designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. They provide the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail-Safe
- No dc Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triacs Quadrants 2 and 3)
- Direct ac Line Operation
- Low External Components Count

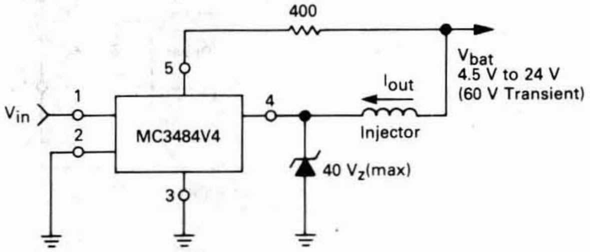


Temp Set
R1
R2
Fail-Safe
Pulse Amplifier
3
4
VRef
Comparator
Sampling Full Wave Logic
6
7
220 Vac
R4
1
UAA1016B
Sawtooth Generator
Synchro-nization
Power Supply
Load
(NTC) Temp. Sensor
R3
2
CPin 2
8
RSync
5
−VCC
220 Vac

## Integrated Solenoid Driver

**MC3484V2,V4** $T_J$ = −40 to +125°C, Case 314D

The MC3484 is an integrated monolithic solenoid driver. Its typical function is to apply full battery voltage to fuel injector(s) for rapid current rise, in order to produce positive injector opening. When load current reaches a preset level (4.0 A in MC3484V4 or 2.4 A in MC3484V2) the injector driver reduces the load current by a 4-to-1 ratio and operates as a constant current supply. This condition holds the injector open and reduces system dissipation.

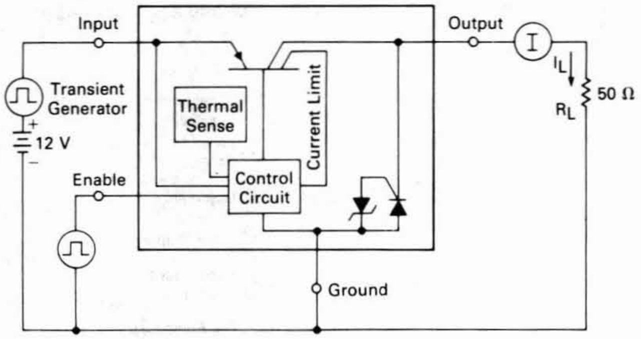


400
Vbat
4.5 V to 24 V
(60 V Transient)
5
Iout
Vin
1
2
MC3484V4
4
Injector
40 Vz(max)
3

## High-Side Driver Switch

**MC33038T** $T_J$ = −40 to +125°C, Case 314D

. . . designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive or negative going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.



Input
Output
Transient Generator
12 V
Thermal Sense
Current Limit
Enable
Control Circuit
IL
RL
50 Ω
Ground

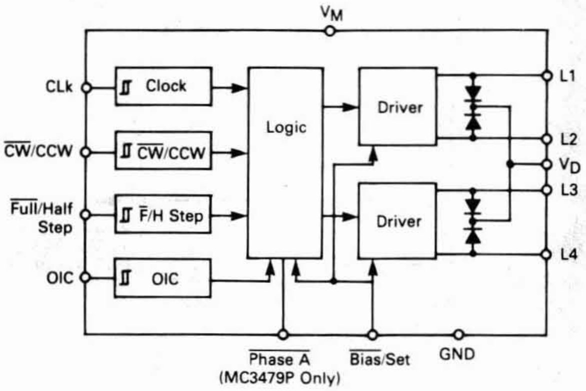
# Motor Control

Motorola offers a variety of motor control bipolar analog integrated circuits. Controllers/drivers are available for stepper motors, dc servo motors and motor speed. Circuits are also offered for generating controlled triac triggering pulses and for protecting loads from transients.

## Stepper Motor Drivers

**MC3479P** $T_A$ = 0° to +70°C, Case 648C
**SAA1042P,AP** $T_A$ = 0 to +70°C, Case 721

Stepper Motor Drivers provide up to 500 mA of drive per coil for two phase 6.0 V to 24 V stepper motors. Control logic is provided to accept commands for clockwise, counter clockwise and half or full step operation. MC3479P has added Output Impedance Control (OIC) and Phase A drive state indicator (not available on SAA1042 devices).



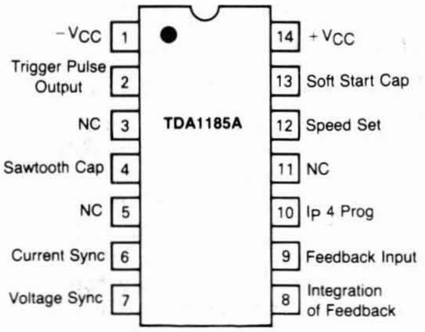
$V_M$
CLk
Clock
$\overline{CW}$/CCW
$\overline{CW}$/CCW
$\overline{Full}$/Half Step
$\overline{F}$/H Step
OIC
OIC
Logic
Driver
Driver
L1
L2
$V_D$
L3
L4
$\overline{Phase\ A}$ (MC3479P Only)
$\overline{Bias}$/Set
GND

## Triac Phase Angle Controller

**TDA1185A,P** $T_A$ = 0 to +70°C, Case 646

. . . generates controlled triac triggering pulses and allows tacholess speed stabilization of universal motors by an integrated positive feedback function.

- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses When Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft Start
- Power Failure Detectiion and General Circuit Reset
- Low Power Consumption: 1.0 mA



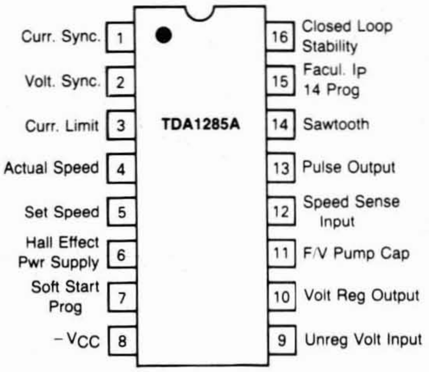
TDA1185A
$-V_{CC}$ 1
Trigger Pulse Output 2
NC 3
Sawtooth Cap 4
NC 5
Current Sync 6
Voltage Sync 7
14 $+V_{CC}$
13 Soft Start Cap
12 Speed Set
11 NC
10 Ip 4 Prog
9 Feedback Input
8 Integration of Feedback

## Universal Motor Speed Controllers

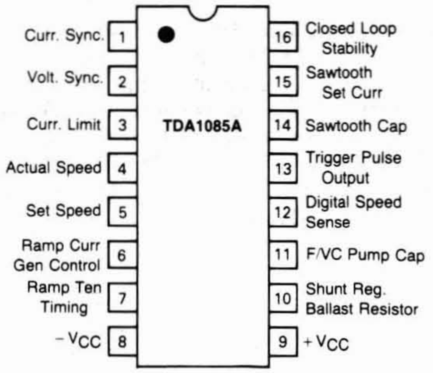
**TDA1285AP/TDA1085AP,BP**
$T_A$ = 0 to +70°C, Case 648

. . . all the necessary functions for the speed control of universal (ac/dc) motors in an open or closed loop configuration. Facility for defining the initial speed/time characteristic. The circuits provide a phase angle varied trigger pulse to the motor control triac.

- Guaranteed Full Wave Triac Drive
- Soft Start from Power-up
- On-Chip Frequency/Voltage Converter and Ramp Generator
- Current Limiting Incorporated
- Direct Drive from ac Line



TDA1285A
Curr. Sync. 1
Volt. Sync. 2
Curr. Limit 3
Actual Speed 4
Set Speed 5
Hall Effect Pwr Supply 6
Soft Start Prog 7
$-V_{CC}$ 8
16 Closed Loop Stability
15 Facul. Ip 14 Prog
14 Sawtooth
13 Pulse Output
12 Speed Sense Input
11 F/V Pump Cap
10 Volt Reg Output
9 Unreg Volt Input

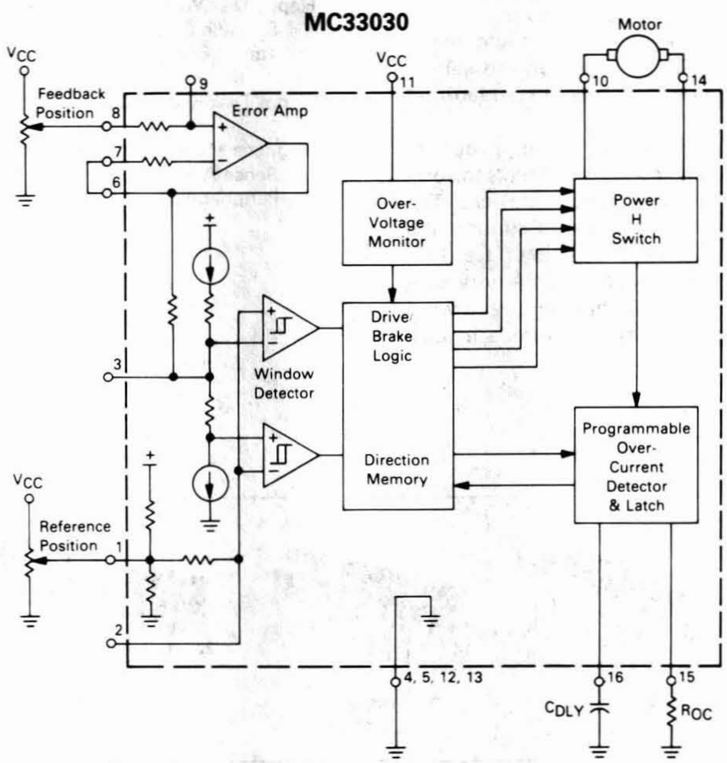


TDA1085A
Curr. Sync. 1
Volt. Sync. 2
Curr. Limit 3
Actual Speed 4
Set Speed 5
Ramp Curr Gen Control 6
Ramp Ten Timing 7
$-V_{CC}$ 8
16 Closed Loop Stability
15 Sawtooth Set Curr
14 Sawtooth Cap
13 Trigger Pulse Output
12 Digital Speed Sense
11 F/VC Pump Cap
10 Shunt Reg. Ballast Resistor
9 $+V_{CC}$

## DC Servo Motor Controller/Driver

**MC33030** $T_A = -40$ to $+85°C$, Case 648C

A monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on-chip op amp and window comparator with wide input common-mode range, drive and brake logic with direction memory, power H switch driver capable of 1.0 A, independently programmable over-current monitor and shutdown delay, and over-voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.


MC33030
Motor
$V_{CC}$
Feedback Position
8
9
Error Amp
7
6
$V_{CC}$
11
10
14
Over-Voltage Monitor
Power H Switch
Drive/Brake Logic
Window Detector
3
Direction Memory
Programmable Over-Current Detector & Latch
$V_{CC}$
Reference Position
1
2
4, 5, 12, 13
16
15
$C_{DLY}$
$R_{OC}$

# Interface Circuits
# Memory Interface and Control

To a significant degree, the economics of semiconductors prohibits the specific tailoring of integrated circuits — except custom and semicustom circuits — to the vast variety of potential end uses. Most commonly, off-the-shelf circuits, even MSI and LSI circuits, are designed to perform a major generic function that can be adapted to numerous applications. Direct adaptation to specific peripherals or ancillary circuits are then accomplished through appropriate interface circuits.

A few potential interface requirements may demand custom interface designs. Most, however, are served adequately by Motorola's large variety of standardized Interface ICs.

Motorola's broad spectrum of interface products ranges from basic drivers and receiver products to complex bus and magnetic memory support devices. The driver, receiver and transceiver products support the application requirements of peripheral interface, EIA, IEE and 360/370 I/O standards. Magnetic memory support products include sense amplifiers and read/write control circuits which provide easy interface in disk drive systems.

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  Tunnel Erase Controller . . . . . . . . . . . . . . . . . 2-35

Floppy Disk Read Amplifier Systems . . . . . . . . . . . . 2-35

Magnetic Memories to TTL Systems . . . . . . . . . . . . 2-36
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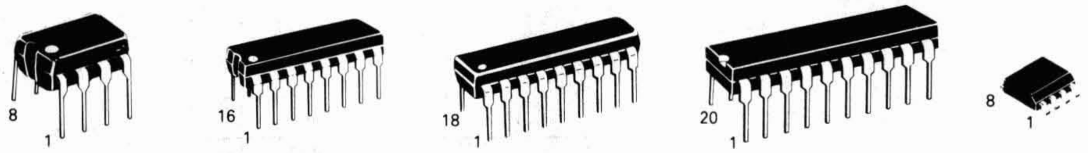
  Peripheral Clamping Array. . . . . . . . . . . . . . . . 2-36



CASE 626
PLASTIC

CASE 648
PLASTIC

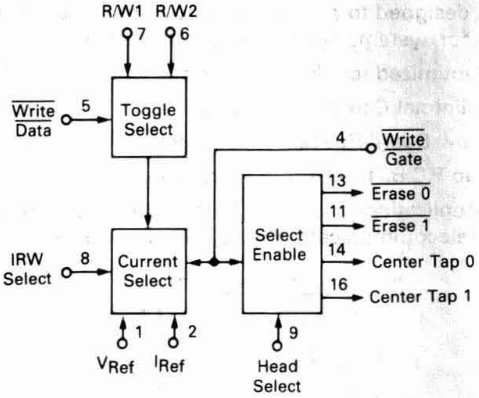
CASE 707
PLASTIC

CASE 738
PLASTIC

CASE 751
PLASTIC

# Floppy Disk Write Controller/Head Driver Systems

## MC3469P Straddle Erase Controller

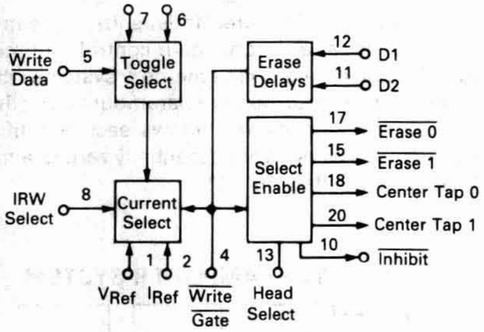

R/W1 R/W2
7
6
Write Data
5
Toggle Select
4
Write Gate
13
Erase 0
11
Erase 1
Select Enable
14
Center Tap 0
16
Center Tap 1
IRW Select
8
Current Select
1
2
9
VRef
IRef
Head Select

Designed to provide the entire interface between floppy disk heads and the head control and write data signals for straddle-erase heads.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer track compensation.

Packages:
MC3469P — Case 648
MC3471P — Case 738
$T_A$ = 0 to +70°C

## MC3471P Tunnel Erase Controller


R/W1 R/W2
7
6
Write Data
5
Toggle Select
Erase Delays
12
D1
11
D2
17
Erase 0
15
Erase 1
Select Enable
18
Center Tap 0
IRW Select
8
Current Select
20
Center Tap 1
10
Inhibit
1
2
4
13
VRef
IRef
Write Gate
Head Select

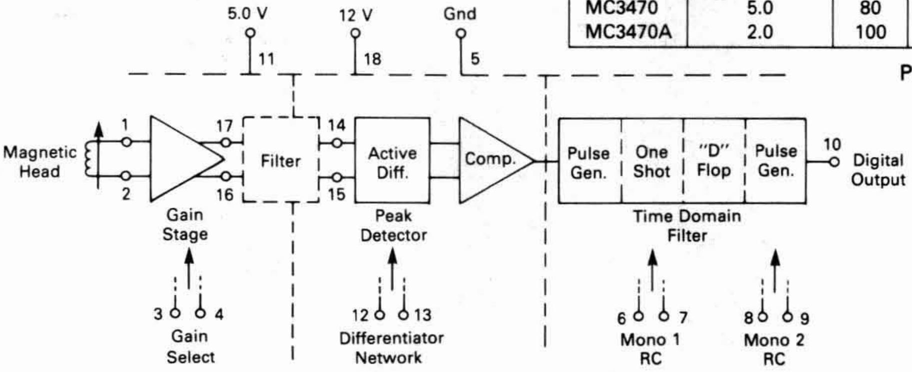
Designed to provide the entire interface between the write data and head control signals and the heads (write and erase) for either tunnel or straddle-erase floppy disk systems.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off. An Inhibit output is provided which indicates that the heads are active during write, degauss, or erase.

# Floppy Disk Read Amplifier System

## MC3470,A Floppy Disk Read Amplifier

Designed as monolithic Read Amplifier Systems for obtaining digital information from floppy disk storage. These devices accept differential ac signals produced by the magnetic head and provides a digital output pulse that corresponds to each peak of the input signal. A gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output. These devices provide all the active circuitry to perform the floppy disk Read amplifier function, and guarantee to have a maximum peak shift of 5.0%, adjustable to zero, for the MC3470P and 2.0%, adjustable to zero, for the MC3470AP.


5.0 V
12 V
Gnd
11
18
5
Magnetic Head
1
2
17
16
Filter
14
15
Active Diff.
Comp.
Pulse Gen.
One Shot
"D" Flop
Pulse Gen.
10
Digital Output
Gain Stage
Peak Detector
Time Domain Filter
3
4
Gain Select
12
13
Differentiator Network
6
7
Mono 1 RC
8
9
Mono 2 RC

| Device Number | Peak Shift (f = 250 kHz, $V_{ID}$ = 1.0 Vpp) | Differential Input Voltage Gain (f = 200 kHz, $V_{ID}$ = 5.0 mV [RMS]) | | Input Common Mode Range (5% Max THD) | |
|---|---|---|---|---|---|
| | | V/V | | V | |
| | % Max | Min | Max | Min | Max |
| MC3470 | 5.0 | 80 | 130 | −0.1 | 1.5 |
| MC3470A | 2.0 | 100 | 130 | | |

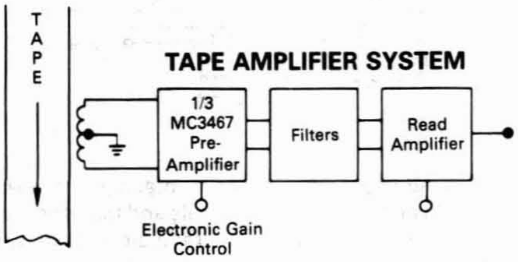
Package:
P Suffix — Case 707
$T_A$ = 0 to +70°C

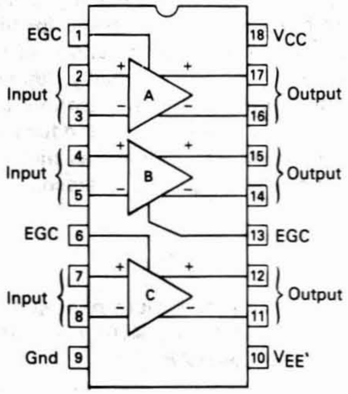
# Magnetic Memories to TTL Systems

## MC3467 Sense Amplifier . . . for Magnetic Tape Memories

The MC3467 provides three independent preamplifiers with individual electronic gain control, optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V.


TAPE AMPLIFIER SYSTEM
T A P E
1/3 MC3467 Pre-Amplifier
Filters
Read Amplifier
Electronic Gain Control

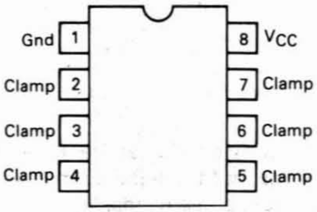

EGC 1
Input 2
Input 3
Input 4
Input 5
EGC 6
Input 7
Input 8
Gnd 9
A
B
C
18 VCC
17 Output
16 Output
15 Output
14 Output
13 EGC
12 Output
11 Output
10 VEE

| Device Number | Small-Signal Bandwidth MHz Min | Input Common Mode Range Volts Min | Temperature Range °C | Package |
|---|---|---|---|---|
| MC3467L | 10 | +1.5 | 0 to +70 | Ceramic Case 726 |
| MC3467P | | | | Plastic Case 707 |

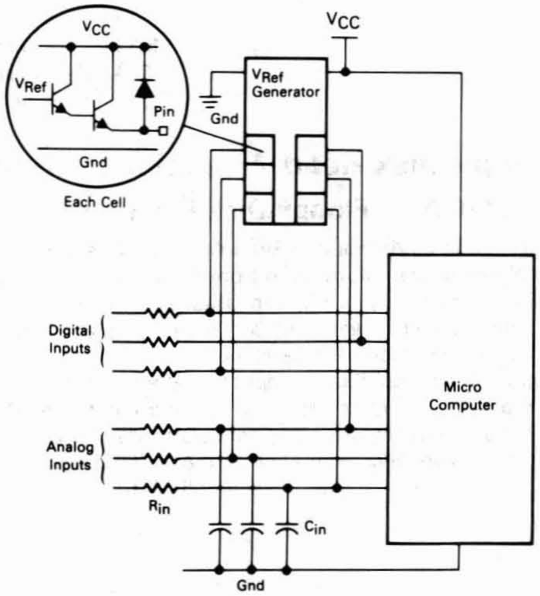
## TCF6000 Peripheral Clamping Array

. . . designed to protect input/output lines of microprocessor systems against voltage transients.

- Optimized for HMOS System
- Minimal Component Count
- Low Board Space Requirement
- No P.C.B. Track Crossovers Required
- Applications Areas Include Automotive, Industrial, Telecommunications and Consumer Goods


Gnd 1
Clamp 2
Clamp 3
Clamp 4
8 VCC
7 Clamp
6 Clamp
5 Clamp

$T_A = -40$ to $+85°C$


VCC
VRef
Pin
Gnd
Each Cell
VCC
VRef Generator
Gnd
Digital Inputs
Analog Inputs
Rin
Cin
Gnd
Micro Computer

# Interface Circuits
# Bus Interface

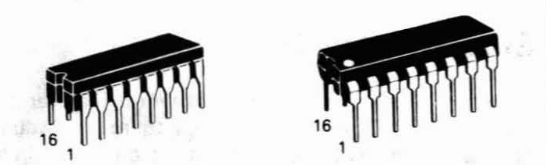
Motorola's bus interface circuits extend the drive capabilities of microprocessor data, address and control buses.

Page
Microprocessor Bus Extenders . . . . . . . . . . . . . . . . 2-37
Address and Control Bus Extenders . . . . . . . . . . . . 2-37

## Microprocessor Bus Extenders

These devices are designed to extend the drive capabilities of today's standard microprocessors. All devices are fabricated with Schottky TTL technology for high speed.

- Single +5.0 V Power Supply Requirement
- Three-State Logic Output
- Low Input Loading — 200 μA Max



CASE 620
CERAMIC

CASE 648
PLASTIC

## Address and Control Bus Extenders

### Hex 3-State Buffers/Inverters

**MC8T95/MC6885#** — Noninverting
**MC8T96/MC6886#** — Inverting

**MC8T97/MC6887#** — Noninverting
**MC8T98/MC6888#** — Inverting

These devices differ in that the non-inverting MC8T95/MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the non-inverting MC8T97/MC6887 and inverting MC8T98/MC6888 provide two Enable inputs — one controlling four buffers and the other controlling the remaining two buffers.

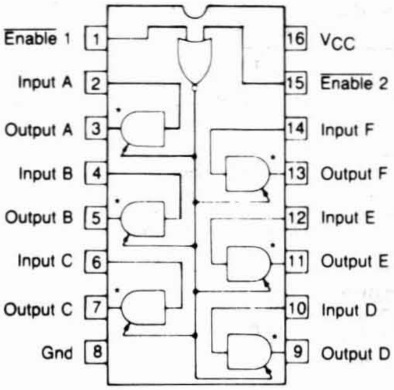
#These devices may be ordered by either of the paired numbers.

$T_A$ = 0 to +75°C

Packages:
L Suffix — Case 620
P Suffix — Case 648

| $V_{OL}$ @ $I_{OL}$ = 48 mA Volts Max | $V_{OH}$ @ $I_{OH}$ = −5.2 mA Volts Min | $I_{OS}$ mA Typ | $t_{PLH}$ ns Typ | $t_{PZH/L(E)}$ ns Typ |
|---|---|---|---|---|
| 0.5 | 2.4 | −80 | 6.0 | 11/15 |

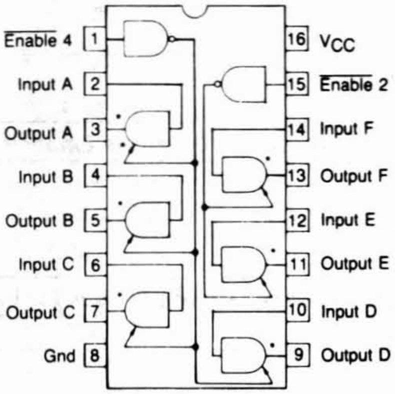
**MC8T95/MC6885#** — Noninverting
**MC8T96/MC6886#** — Inverting
Two-input Enable controls all six buffers.



Enable 1
1
Input A
2
Output A
3
Input B
4
Output B
5
Input C
6
Output C
7
Gnd
8
16
VCC
15
Enable 2
14
Input F
13
Output F
12
Input E
11
Output E
10
Input D
9
Output D

*Add inverter for MC6886/MC8T96.

**MC8T97/MC6887#** — Noninverting
**MC8T98/MC6888#** — Inverting
Two Enable inputs, one controlling four buffers and the other controlling the remaining two buffers.



Enable 4
1
Input A
2
Output A
3
Input B
4
Output B
5
Input C
6
Output C
7
Gnd
8
16
VCC
15
Enable 2
14
Input F
13
Output F
12
Input E
11
Output E
10
Input D
9
Output D

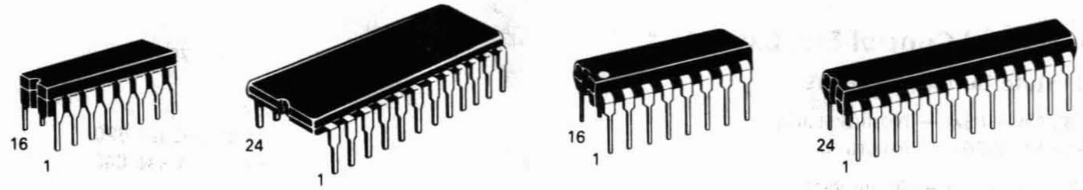
*Add inverter for MC6888/MC8T98.

# Interface Circuits Line Drivers and Receivers for Computer/Terminal Applications

## Single-Ended Transceivers

Motorola offers a spectrum of line drivers and receivers which provide interfaces to many industry standard specifications. Many of the devices add key operational features, such as hysteresis, short circuit protection, clamp diode protection, or special control functions.

Page
Single-Ended Transceivers . . . . . . . . . . . . . . . . . . 2-38
Line Receivers . . . . . . . . . . . . . . . . . . . . . . . . . . 2-39
Line Drivers. . . . . . . . . . . . . . . . . . . . . . . . . . . 2-39
Peripheral. . . . . . . . . . . . . . . . . . . . . . . . . . . . 2-40



CASE 620
CERAMIC

CASE 623
CERAMIC

CASE 648
PLASTIC

CASE 724
PLASTIC

### For Instrumentation Bus, Meets GPIB — IEEE Standard 488

| **Driver Characteristics** | | **Receiver Characteristics** | | | | |
|---|---|---|---|---|---|---|
| **Output Current (mA)** | **Propagation Delay Max (ns)** | **Propagation Delay Max (ns)** | **Transceivers Per Package** | **Device** | **Package Suffix** | **Comments** |
| 48 | 50 | 50 | 4 | MC3446A | P | MOS Compatible Input Hysteresis |
| 48 | 30 | 50 | 8 | MC3447 | P3,L | Input Hysteresis Open Collector, 3-State Outputs with Terminations |
| 48 | 30 | 30 | 4 | MC3448A | P,L | Input Hysteresis Open Collector 3-State Outputs |
| 100 | 30 | 30 | 4 | MC3440A | P,L | Input Hysteresis |
| | | | | MC3441A | | Common Enable Input Hysteresis |

### For Microprocessor Data Bus Extension

| | | | | | | |
|---|---|---|---|---|---|---|
| 48 | 14 | 14 | 4 | MC8T26A<br>(MC6880A) | P,L | Inverting Logic |
| 48 | 17 | 17 | 4 | MC8T28<br>(MC6889) | P,L | Non-Inverting Logic |

### For High-Current Party-Line Bus for Industrial and Data Communications

| | | | | | | |
|---|---|---|---|---|---|---|
| 100 | 15 | 15 | 4 | MC26S10 | P,L | Open Collector Outputs |

# Line Receivers

## General-Purpose

| S = Single Ended<br>D = Differential | Type* Of Output | $t_{prop}$ Delay Time Max (ns) | Party-Line Operation | Strobe Or Enable | Power Supplies (V) | Device | Package Suffix(s) | Receivers Per Package | Companion Drivers | Comments |
|---|---|---|---|---|---|---|---|---|---|---|
| D | TP | 25 | Yes | Yes | ±5 | MC3450 | P,L | 4 | MC3453 | |
| D | OC | 25 | Yes | Yes | ±5 | MC3452 | P,L | 4 | | |
| D | TP | 25 | Yes | Yes | ±5 | MC75107 | P,L | 2 | MC75S110 | |
| D | OC | 25 | Yes | Yes | ±5 | MC75108 | P,L | 2 | | |
| S | TP | 30 | — | Yes | +5 | MC3437 | P,L | 6 | | Input Hysteresis |

## 360/370 I/O Interface

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| S | TP | 30 | Yes | No | +5 | MC75125<br>MC75127 | P,L | 7 | MC3481<br>MC3485 | Schottky Circuitry |
| S | TP | 30 | Yes | Yes | +5 | MC75128<br>MC75129 | P,L | 8 | MC3481<br>MC3485 | Schottky Circuitry |

*OC = Open Collector, TP = Totem-pole output

## EIA Standard

| S = Single Ended<br>D = Differential | Type* Of Output | $t_{prop}$ Delay Time Max (ns) | Party-Line Operation | Strobe Or Enable | Power Supplies (V) | Device | Package Suffix(s) | Receivers Per Package | Companion Drivers | EIA Standard |
|---|---|---|---|---|---|---|---|---|---|---|
| S | R | 85 | No | No | +5 | MC1489<br>MC1489A | P,L | 4 | MC1488 | RS232C |
| S, D | TP | 30 | Yes | Yes | +5 | AM26LS32 | P,D | 4 | AM26LS31 | RS422/423 |
| S, D | TP | 30 | Yes | Yes | +5 | MC3486 | P,L | 4 | MC3487 | |
| S, D | TP | 35 | Yes | Yes | +5 | SN75173 | N,J | 4 | SN75172 | RS422/423/485 |
| S, D | TP | 35 | Yes | Yes | +5 | SN75175 | N,J | 4 | SN75174 | |

*R = Resistor Pull-up, TP = Totem-pole output

# Line Drivers

## Current Mode

| Output Current Capability (mA) | $t_{prop}$ Delay Time Max (ns) | S = Single Ended<br>D = Differential | Party-Line Operation | Strobe Or Enable | Power Supplies (V) | Device | Package Suffix(s) | Drivers Per Package | Companion Receivers | Comments |
|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 15 | D | Yes | Yes | ±5 | MC3453 | P,L | 4 | MC3450<br>MC3452 | |
| 15 | 15 | D | Yes | Yes | ±5 | MC75S110 | P,L | 2 | MC75107<br>MC75108 | |

## 360/370 I/O Interface

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 60 | 20† | S | Yes | Yes | +5 | MC3481 | P,L | 4 | MC75125<br>MC75127 | |
| 60 | 20† | S | Yes | Yes | +5 | MC3485 | P,L | 4 | MC75128<br>MC75128 | Common Enable |

† = Typical value.

## Line Drivers (continued)

### EIA Standard

| Output Current Capa-bility (mA) | $t_{prop}$ Delay Time Max (ns) | S = Single Ended D = Differ-ential | Party-Line Opera-tion | Strobe Or Enable | Power Supplies (V) | Device | Package Type | Drivers Per Package | Companion Receivers | EIA Standard |
|---|---|---|---|---|---|---|---|---|---|---|
| 85 | 35 | D | Yes | Yes | +5 | SN75172 | N,J | 4 | SN75173 | RS485 |
| 85 | 35 | D | Yes | Yes | +5 | SN75174 | N,J | 4 | SN75175 | |
| 48 | 20 | D | Yes | Yes | +5 | MC3487 | P,L | 4 | MC3486 | RS422 with 3-State Outputs |
| 20 | 20 | D | Yes | Yes | +5 | AM26LS31 | P,D | 4 | AM26LS32 | |
| 20 | — | S | No | No | ±12 | MC3488A<br>(μA9636A) | P1,U | 2 | | RS423/232C |
| 6 | 350 | S | No | Yes | ±12 | MC1488 | P,L | 4 | MC1489<br>MC1489A | RS232C |

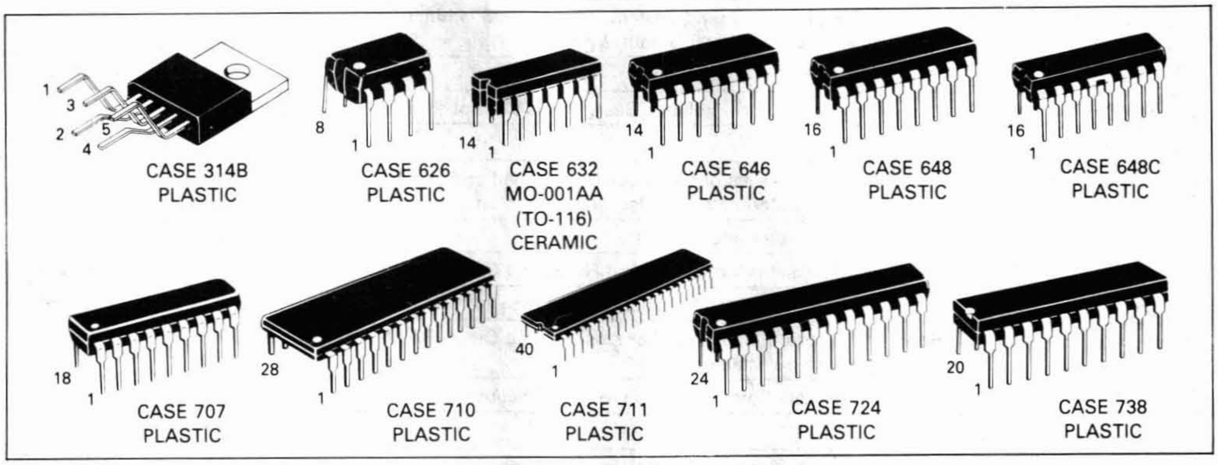
## Peripheral Drivers

| Output Current Capability (mA) | Input Capability | Propagation Delay Time Max (μs) | Output Clamp Diode | Off State Voltage Max (V) | Device | Package Suffix | Logic Function |
|---|---|---|---|---|---|---|---|
| 300 | TTL, DTL | 1.0 | Yes | 70 | MC1472 | P1,U | NAND |
| 500 | TTL, CMOS, PMOS | 1.0 | Yes | 50 | ULN2801 | A | Invert |
| 500 | 14 V to 25 V PMOS | 1.0 | Yes | 50 | ULN2802 | A | Invert |
| 500 | TTL | 1.0 | Yes | 50 | ULN2803 | A | Invert |
| 500 | 6.0 V to 15 V MOS | 1.0 | Yes | 50 | ULN2804 | A | Invert |
| 500 | TTL, CMOS PMOS | 1.0 | Yes | 50 | MC1411<br>(ULN2001A) | P | Invert |
| 500 | 14 V to 25 V PMOS | 1.0 | Yes | 50 | MC1412<br>(ULN2002A) | P | Invert |
| 500 | TTL, 5.0 V CMOS | 1.0 | Yes | 50 | MC1413<br>(ULN2003A) | P | Invert |
| 500 | 8.0 V to 18 V MOS | 1.0 | Yes | 50 | MC1416<br>(ULN2004A) | P | Invert |
| 1500 | TTL, 5.0 V CMOS | 1.0 | Yes | 50 | ULN2068 | B | Invert |
| 1500 | TTL, 5.0 V CMOS | 1.0 | No | 50 | ULN2074 | B | Invert |

# Consumer and Automotive Circuits

. . . reflecting Motorola's continuing commitment to semiconductor products necessary for consumer system designs. This tabulation is arranged to simplify first-order selection of consumer integrated circuit devices that satisfy the primary functions for Television, Audio, Radio, TV Games, Cordless Telephone and Automotive Applications.

Page
Consumer Circuits . . . . . . . . . . . . . . . . . . . . . . 2-41
Automotive Circuits. . . . . . . . . . . . . . . . . . . . . . 2-43



1
3
2
5
4
CASE 314B
PLASTIC
8
1
CASE 626
PLASTIC
14
1
CASE 632
MO-001AA
(TO-116)
CERAMIC
14
1
CASE 646
PLASTIC
16
1
CASE 648
PLASTIC
16
1
CASE 648C
PLASTIC
18
1
CASE 707
PLASTIC
28
1
CASE 710
PLASTIC
40
1
CASE 711
PLASTIC
24
1
CASE 724
PLASTIC
20
1
CASE 738
PLASTIC

## Consumer circuits

### Television Subsystems

| Function | Features | Case | Device |
|---|---|---|---|
| MONOMAX — 1-Chip Black and White TV Subsystem | Video IF, Detector, AGC, Video Amplifier, Horizontal Processor, Vertical Processor, and Sync For 525 Line Systems | 710 | MC13001 |
| | Same as Above Except For 625 Line Systems | 710 | MC13002 |
| Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier, Power Amplifier | Complete TV Sound System; 100 $\mu$V, 3 dB Limiting Sensitivity; 4 Watts Output; $V_{CC}$ = 24 V; $R_L$ = 16 Ω | 648C | TDA3190P |
| | Same as TDA1190Z Except for 750 mW Output | 648C | TDA1190P |
| MONOMAX Audio/Vertical Output | High Level 750 mW Audio Output — Vertical Yoke Driver | 648C | MC13014P |

### Video

| Function | Features | Case | Device |
|---|---|---|---|
| 1st and 2nd Video IF Amplifier | IF Gain @ 45 MHz = 60 dB typ, AGC Range = 70 dB min | 626 | MC1349 |
| | IF Gain @ 45 MHz = 50 dB typ, AGC Range = 60 dB min | 626 | MC1350 |
| 1st and 2nd Video IF, AGC Keyer and Amplifier | IF Gain @ 45 MHz = 53 dB typ, AGC Range = 75 dB min, "Forward AGC" Provided for Tuner | 646 | MC1352 |
| 3rd IF, Video Detector, Video Buffer, and AFC Buffer | Low-Level Detection, Low Harmonic Generation, Zero Signal dc Output Voltage of 7.0 to 8.2 V | 626 | MC1330A1 |
| | Same as MC1330A1 Except Zero Signal dc Output Voltage of 7.8 to 9.0 V | 626 | MC1330A2 |
| SAW Preamp, IF Amplifier, Detector, AGC, AFC | Complete Video IF or Parallel Sound IF System Complete AFT System with Simple Quadrature Detector | 707 | MC13010 |

### Chroma

| Function | Features | Case | Device |
|---|---|---|---|
| Color Processor | PAL/NTSC Input, RGB Output, also RGB Inputs, Plus Fast Blanking Input. Ideal for Text, Graphics, Overlays | 711 | TDA3301<br>TDA3303 |
| Color Processor | PAL/NTSC Input, RGB Outputs, on-Chip Hue Control | 724 | TDA3330 |
| Color Processor | PAL/NTSC Input, Color Difference Outputs on-Chip Hue Control | 707 | TDA3333 |

### Deflection

| Function | Features | Case | Device |
|---|---|---|---|
| Horizontal Processor | Linear Balanced Phase Detector, Oscillator and Predriver, Adjustable dc Loop Gain, Adjustable Duty Cycle | 626 | MC1391 |
| | Same as MC1391 except designed to accept negative Flyback Input Pulse | 626 | MC1394 |

### Sound

| | | | |
|---|---|---|---|
| Sound IF Detector | Interchangeable with ULN2111A | 646 | MC1357 |
| Sound IF Detector, dc Volume Control, Preamplifier | Excellent AMR, Interchangeable with CA3065 | 646 | MC1358 |
| | 30 $\mu$V, 3.0 dB Limiting, Excellent AMR | 646 | TBA120C |
| Sound IF, Low Pass Filter, Detector, dc Volume Control, Preamplifier | Complete TV Sound System; 100 $\mu$V, 3 dB Limiting Sensitivity; 4 Watts Output; $V_{CC}$ = 24 V; $R_L$ = 16 Ω | 648C | TDA3190P |
| | 750 mW Output | 648C | TDA1190P |
| Stereo Sound Control System | Stereo Balance, Volume, Bass, Treble Control | 707 | TCA5550 |

### Modulators

| | | | |
|---|---|---|---|
| Color TV Video Modulator | Chroma Oscillator and Clock Driver, Lead and Lag Network, Chroma Modulator, RF Oscillator, and Modulator | 646 | MC1372 |
| | RF Oscillator and Modulator | 626 | MC1373 |
| TV Modulator (Hi Quality) | RF Oscillator/Modulator, and FM Sound Oscillator/Modulator | 646 | MC1374 |
| FM Modulator | FM Oscillator and Modulator 1.4 MHz to 14 MHz Applications | 626 | MC1376 |
| Video RGB to PAL/NTSC Encoder | RGB and Sync Inputs, Composite Video Out — PAL/NTSC Switch Selectable | 738 | MC1377 |
| Video Synchronizer | Complete Color TV Video Overlay Synchronizer | 711 | MC1378 |

### Tuning System Circuits

| | | | |
|---|---|---|---|
| Tuner Control | Interface Between Synthesizer and Tuner | 707 | MC2801 |
| Two Modulus Prescaler | Divide-by-15 and 16. Toggle Frequency = 140 MHz | 626 | MC3393 |
| Divide-by-20 Prescaler | 200 MHz Toggle Frequency | 626 | MC3396 |
| Remote Control Amplifier | Infrared Diode Signal Amplifier Shaper | 626 | MC3373 |

### IF Amplifiers Radio

| Function | Recommended Frequency, $\frac{IF}{RF*}$ MHz | 3 dB Limiting @ 10.7 MHz $\mu$V (RMS) Typ | AMR dB Typ | Recovered Audio Output $\Delta f = \pm 75$ kHz $\Delta f = \pm 3$ kHz* mV (RMS) | Power Supply Volts Max | Case | Device |
|---|---|---|---|---|---|---|---|
| AGC IF Amplifier | 0.5–50 | — | — | — | 18 | 626 | MC1350 |
| Limiting FM-IF Amplifier | 10.7 | 600 | 45 | 480 | 18 | 646 | MC1355 |
| Limiting IF Amplifier/Quad Detector | 1–70 | 400 | 45 | 480 | 16 | 646 | MC1357 |
| Wideband FSK Receiver Oscillator/Mixer, FM, IF Detector, Meter Drive, Data Shaper | $\frac{10.7}{200*}$ | 30 | 50 | 500 | 15 | 738 | MC3356 |
| Low-Power FM-IF for Dual Conversion Scanning Receivers | $\frac{0.5}{10.7*}$ | 5.0 | 40 | 350* | 8.0 | 648 | MC3357 |
| Narrow Band FM, Oscillator Mixer IF, AFT, Squelch | $\frac{0.5}{10.7*}$ | 2.0 | 40 | 700* | 12 | 707 | MC3359 |
| Low Voltage Version of MC3357 | $\frac{0.5}{10.7*}$ | 2.0 | 40 | 150* | 8 | 648 | MC3361 |

### Modulators

| | | | |
|---|---|---|---|
| FM Transmitter | Low-Power VHF FM Transmitter-Cordless Telephones | 648 | MC2831 |
| UHF/VHF Video Modulator | RF Video/Audio Modulator Oscillator — Operates to 600 MHz | 646 | MC13024 |

### FM Stereo Decoders

| Function | Channel Separation dB Typ | THD % Typ | Stereo/Indicator Lamp Driver mA Max | Features | Case | Device |
|---|---|---|---|---|---|---|
| FM Multiplex Stereo Decoder Coiless Operation | 41 | 0.1 | 50 | Low $V_{CC}$ Automotive | 646 | MC1309 |
| PLL Designs | 41 | 0.1 | 75 | High Input Signal Handling | 646 | MC1310 |
| | 62 | 0.1 | 100 | Low Signal Blend for Noise Reduction | 648 | TCA4500A |

### AM Stereo Decoder

| Features | Function | Case | Device |
|---|---|---|---|
| CQUAM® AM Stereo Decoder | Monaural/Stereo AM Detector, Indicator | 738 | MC13020 |

### Attenuators

| Function | $V_{CC}$ Range Vdc | THD % Typ | V dB Typ | Attenuation Range dB Typ | Case | Device |
|---|---|---|---|---|---|---|
| Electronic Attenuator | 9.0–18 | 0.6 | 13 | 90 | 626 | MC3340 |
| Stereo, Volume, Bass, Treble, Balance | 8.5–18 | 0.1 | 10 | 80 | 707 | TCA5550 |

### Audio

| Features | (System) $P_O$ Watts | $V_{CC}$ Vdc Max | $V_{in}$ @ rated $P_O$ mV Typ | $I_D$ mA Typ | $R_L$ Ohms | Case | Type |
|---|---|---|---|---|---|---|---|
| Class B Audio Driver | 10.0 | 35 | 89 | 10 | 165 | 626 | MC3320 |
| | 10.0 | 20 | 32 | 7.0 | 65 | 626 | MC3321 |

### Transistor Arrays

| Function | $I_{C(max)}$ mA | $V_{CEO}$ Volts Max | $V_{CBO}$ Volts Max | $V_{EBO}$ Volts Max | Case | Device |
|---|---|---|---|---|---|---|
| One Differentially Connected Pair and Three Isolated Transistors | 50 | 15 | 20 | 5.0 | 646 | MC3346<br>MC3386 |
| Dual Independent Differential Amplifiers with Associated Constant Current Transistors | 50 | 15 | 20 | 5.0 | 646 | CA3054 |
| Three Differentially Connected Pairs | 50 | 35 | 40 | 5.0 | 648 | MC3350 |

## Automotive Circuits

### Voltage Regulator

| Function | Features | Case | Device |
|---|---|---|---|
| Automotive Voltage Regulator | Designed for use with NPN Darlington, Overvoltage Protection; "Open Sense" Shut Down; Selectable Temperature Coefficient for Use in a Floating Field<br>Alternator Charging System | 646 | MC3325 |

### Electronic Ignition

| | | | |
|---|---|---|---|
| Electronic Ignition Circuit | Designed for Use in High Energy Variable Dwell Electronic Ignition Systems with Variable Reluctance Sensors. Dwell and Spark Energy are Externally Adjustable | 626 | MC3334 |
| Flip-Chip Electronic Ignition Circuit | Same as MC3334 — Mirror Image Die for Inverted "Bumped" Mounting to Substrate | — | MCCF3334 |

### Special Function — Automotive

| | | | |
|---|---|---|---|
| Programmable Frequency Switch (Engine RPM Switch) | Wide Input Frequency Range (10 Hz to 100 kHz)<br>Adjustable Hysteresis<br>Wide Supply Operating Range (7 to 24 V) | 646, 632 | MC3344 |
| Injector Driver | Power Driver for Automotive Fuel Injection Systems, Reduced Hold Current | 314B | MC3484 |

# Communication Circuits

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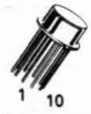
Phase-Locked-Loop Components . . . . . . . . . . . . . . 2-53

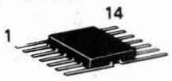
Traditionally, an office environment has utilized two distinctly separate wired communications systems — Telecommunications and Datacommunications. Each had its individual hardware components complement and each required its own independent transmission line system: twisted wire pairs for Telecom and relatively high-priced coax cable for Datacom. But times have changed. Today, Telecom and Datacom coexist comfortably on inexpensive twisted wire pairs and utilize a significant number of components in common. This has led to the development and enhancement of PBX (Private Branch Exchanges) to the point where the long heralded "office of the future," with simultaneous voice and data communications capability at each station, is no longer of the future at all. The capability is here today!

The keys to this communications explosion are the recent advances in semiconductor technology and the resultant dedicated VLSI products. These new products not only permit the implementation of combined voice/data communications, but materially improve the performance and cost-effectiveness of each major segment of the total system.

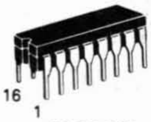
Motorola semiconductor components serve a wide range of requirements for the voice/data marketplace. They encompass both CMOS and bipolar linear technologies, each to its best advantage, and upgrade the conventional analog voice systems and establish new capabilities in digital communications. Early products, such as the solid-state single-chip crosspoint switch, the more recent monolithic Subscriber-Loop-Interface Circuit (SLIC), a single-chip Codec/Filter Mono-circuit) the latest Universal Digital Loop Transceivers (UDLT), and single-chip telephone circuits are just a few examples of Motorola leadership in the voice/data area. A large-scale R & D effort dedicated to this market assures a continuance of this position.



CASE 603
METAL



CASE 607
CERAMIC



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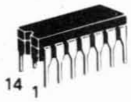
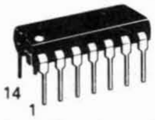
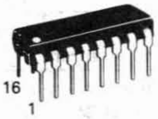
CERAMIC



CASE 632
CERAMIC



CASE 646
PLASTIC



CASE 648
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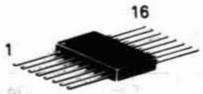

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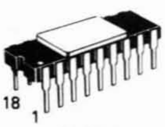
CERAMIC



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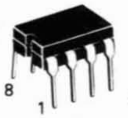

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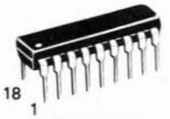

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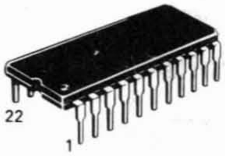

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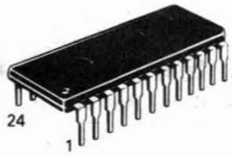

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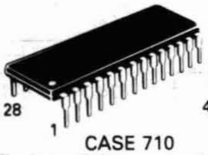
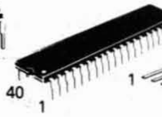


CASE 710
PLASTIC



CASE 711
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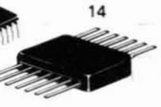

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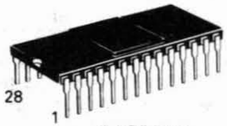

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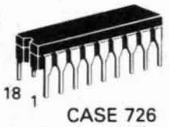
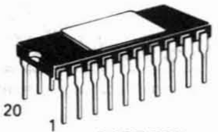
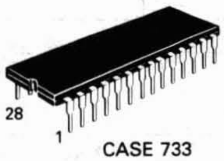
CERAMIC



CASE 726
CERAMIC



CASE 729
CERAMIC



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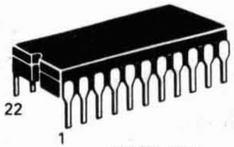
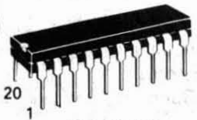
CERAMIC



CASE 736
CERAMIC



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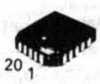

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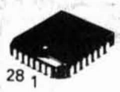

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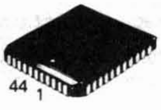
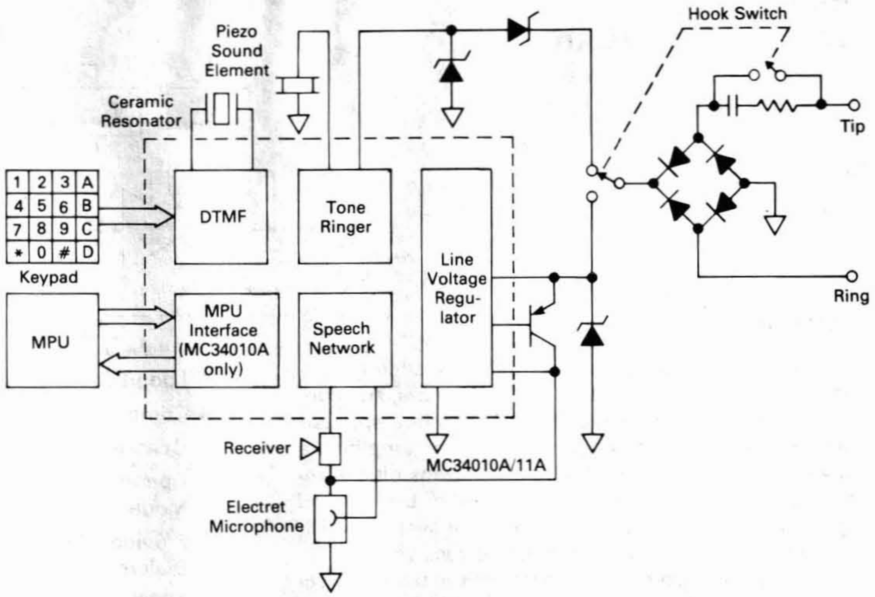


CASE 777
PLASTIC

# Electronic Telephone Circuits

## The Complete Electronic Telephone Circuit

### MC34010A/11A



The conventional transformer-driven telephone handset is slated for major innovations. The bulky transformer is destined to disappear. So are many of its discrete components, including the familiar telephone bell. They are being replaced with integrated circuits that perform all the major handset functions simply, reliably and inexpensively . . . functions such as 2-to-4 wire conversion, DTMF dialing, tone ringing, and a variety of related activites.

The culmination of these capabilities is the recently introduced Electronic Telephone Circuit, the MC34010A/11A. This IC places all of the above-mentioned functions on a single monolithic chip.

These telephone circuits utilize advanced bipolar linear ($I^2L$) technology and provide all the necessary elements of a modern tone-dialing telephone. The MC34010A even incorporates an MPU interface circuit for the potential inclusion of automatic dialing in the final system.

Available in Case 711 (Plastic) and the 44-pin plastic chip carrier Case 777.

### Features

- Provides All Basic Telephone Functions, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA RS-470 Requirements
- Speech Network Provides Two–Four Wire Conversion with Adjustable sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- $I^2L$ Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- MC34010A Provides Microprocessor Interface Port for Automatic Dialing Features

## Also Available — a broad line of additional telephone components for customizing systems design.

### Ringer Circuits

**MC34012.** Telephone bell replacement circuit available with 500 Hz, 1.0 kHz and 2.0 kHz tone options.

**MC34017.** Same as above, but has push-pull output for greater power.

**MC34013.** Speech network and tone dialer provides 2–4 wire conversion and DTMF tone generation.

### Dialer Circuits

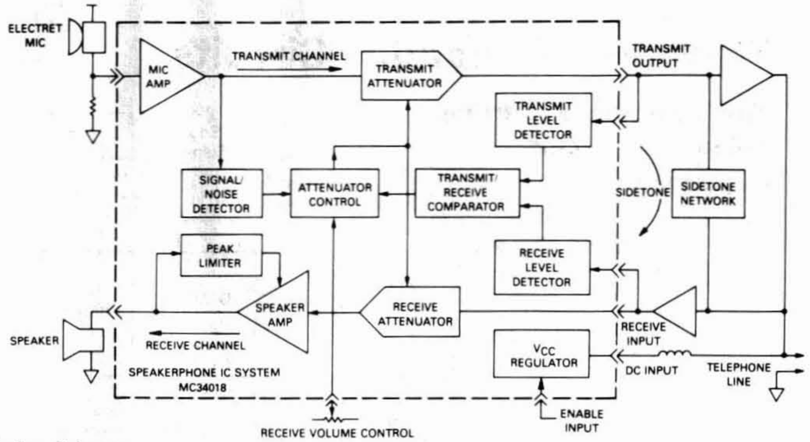
**MC14408/9.** Binary-to-phone pulse converter changes 4-bit binary input code to corresponding serial output pulses.

**MC14410.** 2-of-8 tone encoder converts digital input code to corresponding high- and low-band sine waves.

**MC14419.** 2-of-8 key pad-to-binary encoder accepts inputs from 16-key switches arranged in a 4 x 4 matrix. Contains illegal-state detector to eliminate false data outputs.

**MC145409.** Integrated pulse dialer with 17-digit redial. Operates at 2.5 to 6 volt range and uses an RC oscillator instead of a crystal.

# Two-Chip Switchable Hands-Free Telephone System


ELECTRET MIC
MIC AMP
TRANSMIT CHANNEL
TRANSMIT ATTENUATOR
TRANSMIT OUTPUT
TRANSMIT LEVEL DETECTOR
SIGNAL/ NOISE DETECTOR
ATTENUATOR CONTROL
TRANSMIT/ RECEIVE COMPARATOR
SIDETONE
SIDETONE NETWORK
PEAK LIMITER
RECEIVE LEVEL DETECTOR
SPEAKER AMP
RECEIVE ATTENUATOR
RECEIVE INPUT
SPEAKER
RECEIVE CHANNEL
V<sub>CC</sub> REGULATOR
DC INPUT
TELEPHONE LINE
SPEAKERPHONE IC SYSTEM MC34018
ENABLE INPUT
RECEIVE VOLUME CONTROL

## Speaker Phone

### MC34018

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a viable hands-free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line-powered operation (no additional power supplies required). The MC34018 is designed to be interfaced with a speech network (below) which provides the necessary 2-to-4 wire conversion.

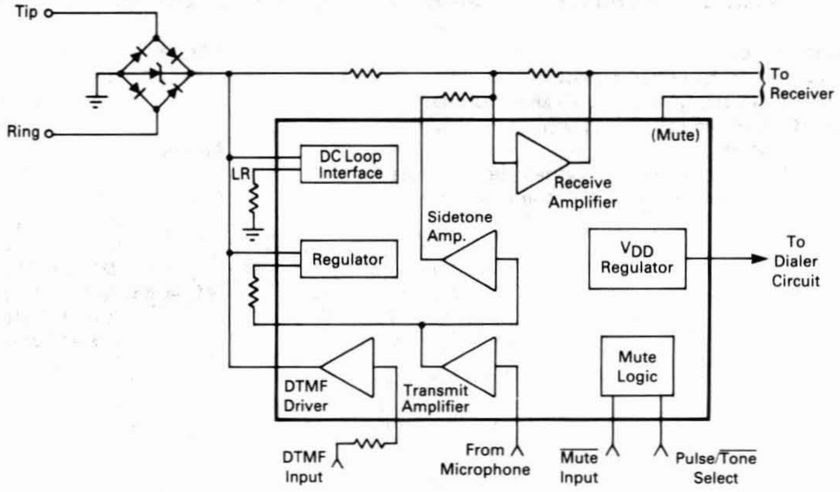
- Adjustable Transmit, Receive and Sidetone Gains
- Loop Length Equalization for Transmit and Receive
- Compatible with 150–300 Ohm Receivers
- Operates Down to 1.4 Volts (V+) in Speech Mode
- Operates Down to 8.0 mA Loop Current in DTMF Mode
- Provides Adjustable, Regulated Voltage for CMOS Dialers
- Speech Amplifiers Muted During Dialing (Tone or Pulse)
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Available in Case 710 (Plastic) and the 28-pin Plastic Chip Carrier Case 776.

## Speech Network with Dialer Interface

### MC34014

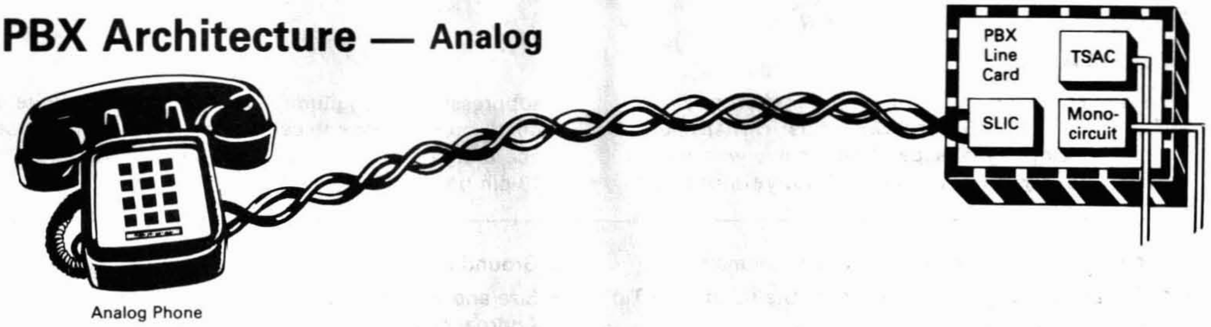
The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, a dc loop interface circuit, tone dialer interface, and a regulated output voltage for a pulse/tone dialer. Also included is an equalization circuit which compensates gains for line length variations, and the conversion from 2-to-4 wire is accomplished with a supply voltage as low as 1.5 volts. The MC34014 is packaged in a standard 18-pin (0.3″ wide) plastic DIP Case 707, and a 20-pin surface mount PLCC package, Case 775.

- Transmit, Receive, and Sidetone Gains Set By External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 Volts (V+) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Compatible with Receiver Impedances of 150 Ω and Higher


Tip
Ring
To Receiver
(Mute)
DC Loop Interface
LR
Receive Amplifier
Sidetone Amp.
Regulator
V<sub>DD</sub> Regulator
To Dialer Circuit
Mute Logic
DTMF Driver
Transmit Amplifier
DTMF Input
From Microphone
Mute Input
Pulse/Tone Select

# Communication Circuits

## PBX Architecture — Analog



### PCM Mono-Circuits Codec-Filters (CMOS LSI)

The Mono-circuits perform the digitizing and restoration of the analog signals. In addition to these important functions, Motorola's family of pulse-code modulation mono-circuits also provides the band-limiting filter functions — all on a single monolithic CMOS chip with extremely low power dissipation.

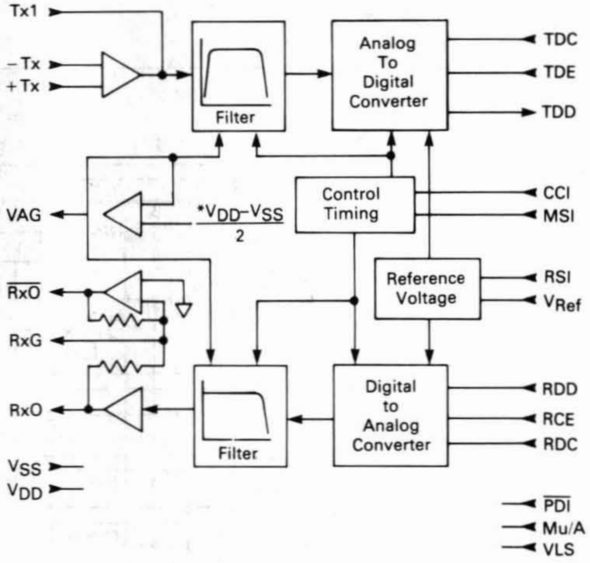
The Mono-circuits require no external components. They incorporate the bandpass filter required for anti-aliasing and 60 Hz rejection, the A/D–D/A conversion functions for either U.S. Mu-Law or European A Law companding formats, the lowpass filter required for reconstruction smoothing, an on-board precision voltage reference, and a variety of options that lend flexibility to circuit implementations. Unique features of Motorola's Mono-circuit family include wide power supply range (6.0 to 13 V) selectable on-board voltage reference (2.5, 3.1, or 3.8 V), and TTL or CMOS I/O interface.

Motorola supplies five versions of the PCM Mono-circuit. The MC14400, MC14403 and MC14405 are general-purpose devices in Case 620 16-pin packages designed to operate in synchronous applications. The MC14401 is the same device (in Case 726 18-pin package) that offers the capability of selecting from three peak overload voltages (2.5, 3.15 and 3.78 V). The MC14402 is the full-feature device that presents all of the options available on the chip. This device is packaged in Case 736 22-pin DIP.

**For 13-Bit Linear Codec see "Analog Circuits — Data Converters."**

**Also Available — separate integrated circuit filters:**

| | |
|---|---|
| MC14413 | PCM Filter with Transmit Bandpass and RCV Lowpass |
| MC14414 | PCM Filter with Transmit and RCV Lowpass |
| MC145414 | Dual Tuneable Lowpass Filter |
| MC145415 | Dual Tuneable Linear Phase Lowpass Filter |
| MC145432 | 2600 Hz Tone Signalling Filter |
| MC145433 | Tuneable Notch/Bandpass Filter |
| MC145440 | 300 Baud Modem Filter-Bell 103 |
| MC145441 | 300 Baud Modem Filter-CCITT V.21 |



### Time Slot Assigner Circuit (TSAC)

Under external MPU control, the TSAC permits time-multiplexed interaction between the various phones in a PBX system.

The TSAC associated with each UDLT in a typical PBX system provides a unique time-slot identity for each of the 32 digital telephones associated with a typical PBX bank. Each TSAC in the system is assigned a specific address, permitting the 32 telephones to be selectively interconnected by means of an 8-bit control bus associated with the MPU.

**MC14416/14418** allows variable codec time slot assignments to be programmed through a *serial* MPU port. MC14416 provides the ability to multiplex off-hook signals for an entire bank of TSACs.

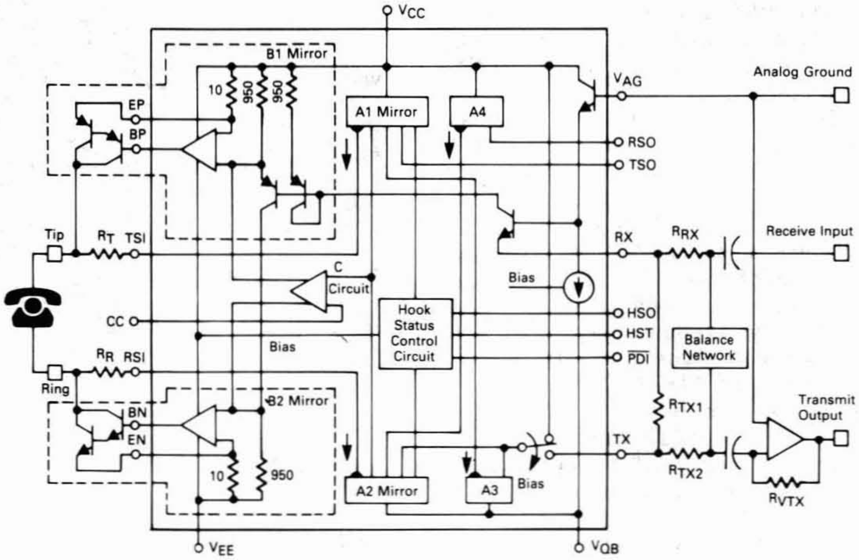
**MC14417** provides for 8-bit parallel signal programming.

# The Subscriber Loop Interface Circuit Family (SLIC)

## MC34F19,A

. . . designed to replace the hybrid transformer circuit in Central Office, PABX and Subscriber carrier equipment, providing signal separation for two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input. It provides dc line current for powering the telset, operating from up to a 56 V supply. Case 726 (Ceramic 18-pin package.)

- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Power Down Input
- Ground Fault Protection
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under patent No. 4,004,109. All royalties related to this patent are included in the unit price.


VCC
B1 Mirror
10
950
950
EP
BP
A1 Mirror
A4
VAG
Analog Ground
RSO
TSO
Tip
RT
TSI
RX
RRX
Receive Input
C
Circuit
Bias
Hook
Status
Control
Circuit
CC
HSO
HST
PDI
Balance
Network
Bias
RR
RSI
Ring
B2 Mirror
BN
EN
RTX1
Transmit
Output
TX
10
950
A2 Mirror
A3
Bias
RTX2
RVTX
VEE
VQB

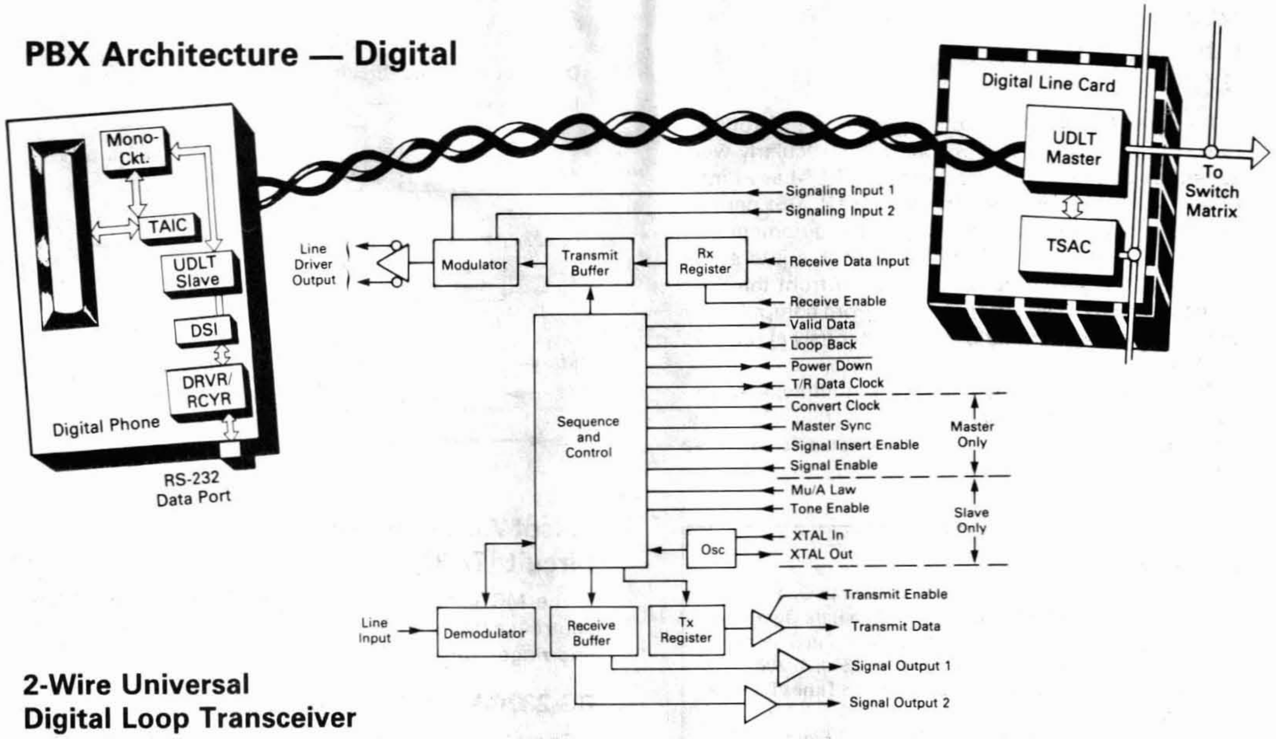
## Crosspoint Switches

Today's semiconductor Crosspoint switches, implemented with semiconductor technology, take the place of the huge banks of mechanical relay matrices one utilized in Central Offices and PBXs. Motorola provides a choice of three configurations and two different technologies to meet specific system design goals.

| Device | Description | Pins | Suffix |
|---|---|---|---|
| MC3416 | Bipolar 4x4x2 Matrix; SCR cells | 24 | L,P |
| MC142100/<br>145100 | CMOS 4x4x1 Matrix; Complementary Transistor Cells | 16 | L,P |

Note: L = Ceramic, P = Plastic

## PBX Architecture — Digital


Mono-Ckt.
TAIC
UDLT Slave
DSI
DRVR/RCYR
Digital Phone
RS-232 Data Port
Digital Line Card
UDLT Master
TSAC
To Switch Matrix
Signaling Input 1
Signaling Input 2
Line Driver Output
Modulator
Transmit Buffer
Rx Register
Receive Data Input
Receive Enable
Valid Data
Loop Back
Power Down
T/R Data Clock
Convert Clock
Master Sync
Signal Insert Enable
Signal Enable
Master Only
Mu/A Law
Tone Enable
Slave Only
XTAL In
XTAL Out
Osc
Sequence and Control
Line Input
Demodulator
Receive Buffer
Tx Register
Transmit Enable
Transmit Data
Signal Output 1
Signal Output 2

## 2-Wire Universal Digital Loop Transceiver (UDLT)

The UDLT family of transceivers allows the use of existing twisted-pair telephone lines (between conventional telephones and a PBX) for the transmission of digital data. With the UDLT, every voice-only telephone station in a PBX system can be upgraded to a digital telephone station that handles the complex voice/data communications with no increase in cabling costs.

In implementing a UDLT-based system the A/D — D/A conversion function associated with each telset is relocated from the PBX directly to the teleset. The SLIC (or its equivalent circuits) is eliminated since its signaling information is transmitted digitally between two UDLTs.

The UDLT master-slave system incorporates the modulation/demodulation functions that permit data communications over a distance up to 2 kilometers. It also provides the sequence control that governs the exchange of information between master and slave. Specifically, the master resides on the PBX line card where it transmits and receives data over the wire pair to the telset. The slave is located in the telset and interfaces the mono-circuit to the wire pair. Data transfer occurs in 10-bit bursts (8 bits of data and 2 signaling bits), with the master transmitting first, and the slave responding in a synchronized half-duplex transmission format.

UDLTs utilize a 256 kilobaud modified differential phase shift keyed (MDPSK) burst modulation technique for transmission to minimize radio frequency, electromagnetic, and crosstalk interference. Implementation through CMOS technology takes advantage of low-power operation, increased reliability, and the proven capability to perform complex telecommunications functions.

### Functional Features

- Provides Synchronous Duplex 64 Kilobits/Second Voice/Data Channel and Two 8 Kilobits/Second Signaling Data Channels Over One 26 AWG Wire Pair Up to 2 Kilometers
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Automatic Detection Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single 5.0 V to 8.0 V Power Supply

### MC145422 Master UDLT

- 2.048 MHz Master and Data Clock
- Pin Controlled Power-Down and Loop-Back Features
- Variable Data Clock — 64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of 8 Kilobits/Seconds Channel into LSB of 64 Kilobits/Second Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

### MC145426 Slave UDLT

- Compatible with MC14400 Series PCM Mono-Circuits
- Automatic Power-Up/Down Feature
- On-Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications

## Digital Loop Transceiver (DLT)

The MC145418/MC145419 DLTs are similar to the MC145422/MC145426 UDLTs. However, the DLTs allow interface flexibility by using external drivers and limiters.

## Data Set Interface Circuit (DSI)

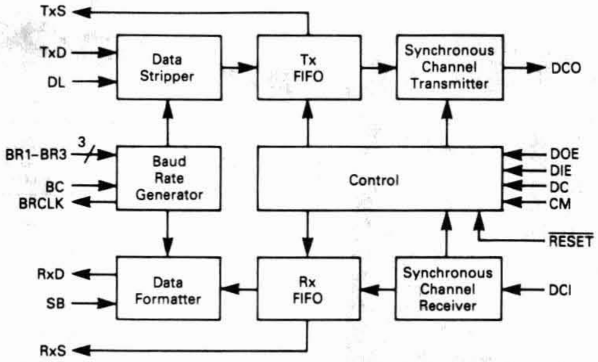
This new CMOS LSI circuit provides asynchronous-to-synchronous data conversion. It is particularly well-suited for use in conjunction with a UDLT-based integrated voice/data system. The **MC145428** DSI permits direct interface between existing data equipment and the UDLT without modifications. With this interactive component, digitized voice information from the PCM Monocircuit and asynchronous data from computers or terminals can be transmitted simultaneously at rates up to 56 K bits/s.

DSI circuits are also used for data multiplexers, concentrators and deconcentrators, data rate changers, data-only switching, and PBX-based local area networks.

**Features**

- Up to 128 kbps Asynchronous Data Rate Operation
- −0 Up to 2.1 Mbps Synchronous Data Rate Operation
- On-board Bit Rate Clock Generator with Pin Selectable Bit Rates of 300, 1200, 2400, 4800, 9600, 19200, and 38400 bps or an Externally Supplied 16 Times Bit Rate Clock May Be Used
- Accepts Asynchronous Data Words of Eight or Nine Bits
- False Start Detection Provided
- Automatic Sync Insertion and Checking

**Data Set Interface Circuit**


TxS
TxD
DL
Data Stripper
Tx FIFO
Synchronous Channel Transmitter
DCO
BR1–BR3
3
BC
BRCLK
Baud Rate Generator
Control
DOE
DIE
DC
CM
RESET
RxD
SB
Data Formatter
Rx FIFO
Synchronous Channel Receiver
DCI
RxS

## Telset Audio Interface Circuit (TAIC)

The MC145429 is an audio control circuit for MPU-controlled independent adjustment of earpiece, speaker and ringer volume.

### RS-232C/V.28 Driver/Receiver

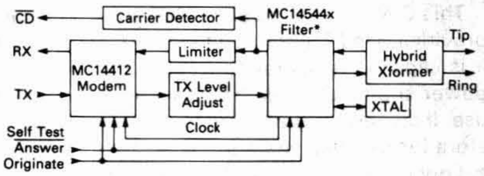
The MC145406 is a silicon-gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of EIA Standard RS-232C and CCITT V.28. Using ±12 volt supplies and a +5.0 volt supply, this 16-pin device consumes a maximum of 15 mW.

# Communication Circuits
# Modem/Filter Circuits

While the modulator/demodulator/filter functions required for data transmission over telephone lines are built into some of the dedicated LSI voice/data transmission circuits — e.g. UDLT (Page 51) — many applications require the modem capabilities separately. Motorola offers a wide choice of system design alternatives by making a variety of such circuits available.

## 300/600 Baud

### MC14412/MC14544x Set



CD
Carrier Detector
MC14544x Filter*
RX
Limiter
Tip
MC14412 Modem
Hybrid Xformer
TX
TX Level Adjust
Ring
XTAL
Clock
Self Test
Answer
Originate

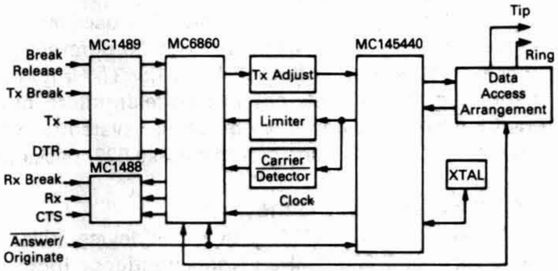
*MC145440 for Bell 103
MC145441 for CCITT V.21

This CMOS subsystem provides the necessary modulation, demodulation and supervisory control functions to implement a serial data communications link at bit rates up to 600 bps.

An accompanying switched capacitor bandpass filter may be selected to meet Bell 103 specifications (MC145440) or CCITT V.21 specifications (MC145441).

- Originate and Answer Modes
- Simplex, Half-Duplex, and Full-Duplex Operation
- On-Chip Sine Wave Generator
- Modem Self Test Mode
- Single Supply
  - $V_{DD}$ = 4.75 to 15 Vdc MC14412FP, MC14412FL
  - $V_{DD}$ = 4.75 to 6.0 Vdc MC14412VP, MC14412VL
- Post Detection Filter
- TTL or CMOS Compatible Inputs and Outputs

### MC6860/MC145440 Set



Tip
Ring
Break Release
MC1489
MC6860
MC145440
Tx Adjust
Data Access Arrangement
Tx Break
Tx
Limiter
DTR
Carrier Detector
MC1488
XTAL
Rx Break
Rx
Clock
CTS
Answer/ Originate

This N-channel MOS Modem adds a telephone interface feature, with automatic answering of a Ring Indicator signal.

The modem is compatible with the M6800 microprocessor family and interfaces directly with the Asynchronous Communications Interface Adapter (ACIA) of this Family.

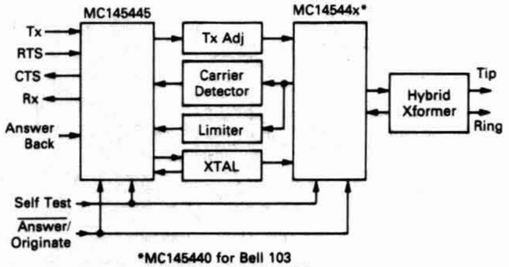
- Originate and Answer Mode
- Crystal or External Reference Control
- Modem Self Test
- Terminal Interfaces TTL-Compatible
- Full-Duplex or Half-Duplex Operation
- Automatic Answer and Disconnect

### MC145445/MC14544x Set

The MC145445 CMOS Modem circuit configuration is similar to that of the MC14412, above, but adds Request to Send ($\overline{RTS}$) and Clear to Send ($\overline{CTS}$) handshake functions with eight selectable $\overline{RTS}$ and $\overline{CTS}$ options. It operates from a single-voltage supply between 4.5 and 7.0 volts.

- Bell 103/113 Answer and Originate Compatible
- CCITT V.21 Modes 1 and 2 Compatible
- Eight Selectable $\overline{RTS}$ to $\overline{CTS}$ Delay Options
- Answer-Back Tone Generator (U.S. and CCITT Tones)
- Carrier Detect Input
- TTL Compatible
- 22-Pin Package

**300 BAUD MODEM BLOCK DIAGRAM**
**MC145445/MC14544x***



MC145445
MC14544x*
Tx
RTS
Tx Adj
CTS
Carrier Detector
Tip
Rx
Hybrid Xformer
Answer Back
Limiter
Ring
XTAL
Self Test
Answer/ Originate

*MC145440 for Bell 103
MC145441 for CCITT V.21

## 1200/2400 Baud

### MC6172 Modulator/MC6173 Demodulator

These components are N-channel, silicon-gate subsystems designed to be integrated into a wide range of equipment utilizing serial data communications. They provide the necessary modem and control functions to communicate over a voice-grade channel, using differential phase shift keying (DPSK) at bit rates of 1200 or 2400 bps. Phase options are provided for both U.S. (Bell) and international (CCITT) markets. Modulator features Clear-to-Send delay options and Answer-Back tone. Both devices are available in the 24-pin plastic (Case 709) and ceramic (Case 623) packages.

### MC14411 Bit Rate Generator

Internal (crystal controlled) 1.843 MHz oscillator and subsequent divider networks provide 16 different output clock rates ranging from 75 Hz to 1.843 MHz for data communications equipment such as teleprinters, printers, CRT terminals and microprocessor systems. In 24-pin plastic (Case 709) and ceramic (Case 623) packages.

### MC145411 Bit Rate Generator

Similar to the MC14411, above, this device utilizes a 1.843 MHz or 3.6864 MHz crystal frequency input divided to provide nine different output clock rates from 150 Hz to 1.843 MHz, or 300 Hz to 3.6864 MHz, respectively. In 16-pin plastic package (Case 648).

### MC145450 1200 Baud FSK Modem

This CMOS modem is intended for use in Bell 202 and CCITT V.23 applications. Features include eight selectable handshake (RTS-CTS) options, soft turn-off capability, Answer-Back tone generator and Carrier-Detect input.

Operates from a single-voltage supply between 4.5 and 6.5 volts for TTL compatibility. On-board crystal oscillator operates with 3.6864 MHz external crystal. The device is available in a 22-pin plastic (Case 708) and ceramic (Case 736) package.

### MC145415 Dual Tunable Linear Phase Low-Pass Sampled Data Filters

This CMOS sampled data, switched capacitor filter IC provides band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two uncommitted comparators for use elsewhere in the system.

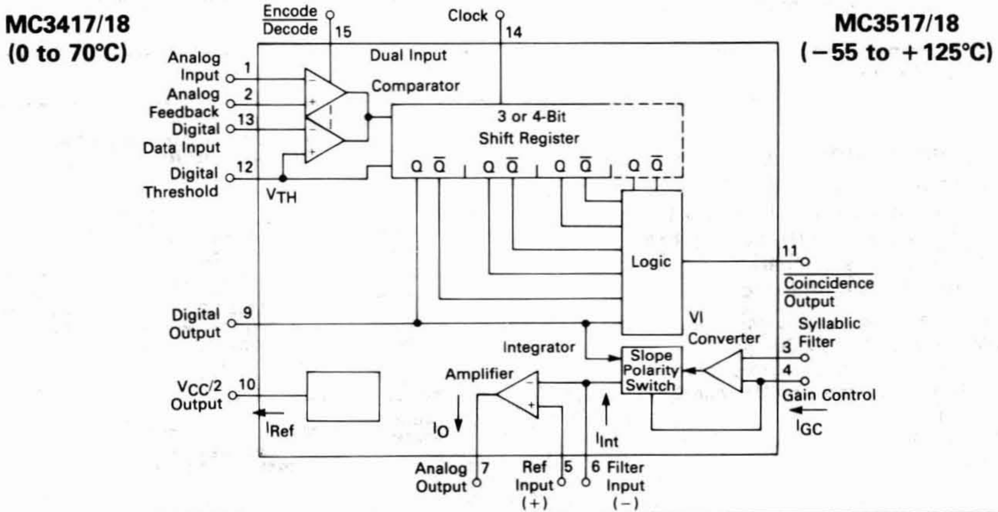
- Low Operating Power Consumption — 20 mW (Typical)
- ±2.5 to ±8.0 Volt Power Supply Ranges
- Useful in High Speed Data Modem Applications
- Pass-Band Edges Tunable With Clock Frequency from 1.25 kHz to 10 kHz

## Continuously Variable Slope Delta Modulator/Demodulator

Provides the A/D-D/A function of voice communications by digital transmission.

The MC3517/18 series of CVSDs is designed for military secure communications and commercial telephone applications. A single IC provides both encoding and decoding functions.

- Encode and Decode functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I$^2$L — Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- MC3417/MC3517 has a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 has a 4-Bit Algorithm (Commercial Telephone)


MC3417/18
(0 to 70°C)
MC3517/18
(−55 to +125°C)
Encode
Decode
15
Clock
14
Analog Input 1
Analog Feedback 2
Digital Data Input 13
Digital Threshold 12
Dual Input
Comparator
3 or 4-Bit
Shift Register
Q Q̄ Q Q̄ Q Q̄ Q Q̄
V_TH
Logic
11
Coincidence Output
Digital Output 9
VI
Converter
Syllabic Filter 3
Integrator
Slope Polarity Switch
4
Gain Control
I_GC
Amplifier
V_CC/2 Output 10
I_Ref
I_O
I_Int
Analog Output 7
Ref Input (+) 5
6 Filter Input (−)

# Communication Circuits
# Phase-Locked-Loop Components

Motorola offers a choice of phase-locked loop components ranging from complete, functional PLL circuits for dedicated applications to a wide selection of basic PLL circuit elements. Full-function phase-locked loops include devices having serial and parallel inputs, as well as 4-bit data inputs for MPU data-bus interfacing. Options include single or dual-modulus capability, transmit/receive offsets, choice of phase detectors and choice of reference-divider integer values. Basic PLL building-block circuits include a large variety of counters and prescalers and other integral functions such as oscillators, phase detectors and control circuits.

## Frequency Synthesizers

### . . . For General Purpose Applications

This family of PLL frequency synthesizers is fabricated with Motorola CMOS technology for very low power consumption. Designed for a wide variety of applications, the family consists of individual devices with a wide range of inputs and divider options that make each device uniquely qualified for a specific end use. Typical applications include:

CATV
AM/FM Radio
Two-Way Radio
TV Tuning
Scanning Receivers
Amateur Radio

Common characteristics for the family include:

- 3.0 to 9.0 Vdc Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- Single-Ended or Double-Ended Error Signal Option

The specific variations for the individual family members are given in the following table:

| | MC145145-1 | MC145146-1 | MC145151-1 | MC145152-1 | MC145155-1 | MC145156-1 | MC145157-1 | MC145158-1 | MC145159-1 |
|---|---|---|---|---|---|---|---|---|---|
| Divider Programming | 4-Bit Data Bus | | Parallel | | Serial | | | | |
| Modulus | Single | Dual | Single | Dual | Single | Dual | Single | Dual | |
| N (N/A) Divider Bits | 14 | (10/7) | 14 | (10/6) | 14 | (10/7) | 14 | (10/7) | |
| Programmable Reference Divider Bits | 12 | | 12** | | 12** | 12** | 14 | | |
| Single-Ended PD(out) (Three-State) | Yes | | | No | Yes | | | | * |
| Double-Ended PD(out) | Yes | | | | | | | | No |
| Lock Detect Output | Yes | | | | | | | | |
| Band-Switch Outputs | No | | | | Yes | | No | | |
| Package (pins) | 18 | 20 | 28 | 28 | 18 | 20 | 16 | 16 | 20 |

Notes: *sample & hold analog phase detector
**8 limited number of selectable values

## . . . For TV/CATV Tuning Systems

Dedicated to TV/CATV applications, these NMOS silicon-gate frequency synthesizers offer the following features:

MC6195/MC6196

- Single 5 V Supply
- Low External Parts Count
- Remote Control Capability
- Scan Up/Scan Down Channel Selection
- Automatic Switching to AFT Mode
- Channel Information Output Interfaces to LEDs
- On-Chip Reference Oscillator Uses External Crystal

**Specific Characteristics**

| Device Type | MC6195* | MC6196* |
|---|---|---|
| Channels | CATV | TV |
| IF Frequency (MHz) | 612.75 | 45.75 |
| Ref. Osc. Freq. (MHz) | 4 | |
| Phase Det. Freq. (kHz) | 7.8125 | 3.90625 |
| Video Coincidence Input | Yes | |
| Band Switch Outputs | Yes | |
| Prescaler Requirements | 256 | |
| Package (pins) | 20 | |

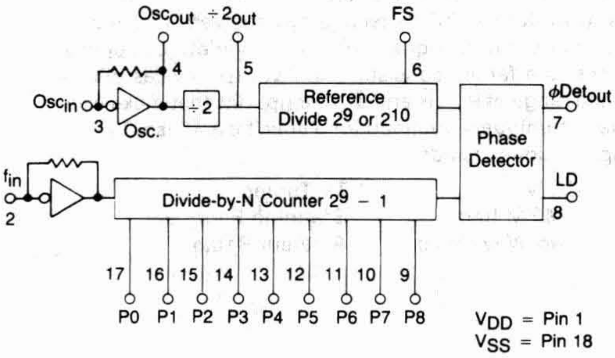
*Closest equivalent for MC6190 through MC6194, which are being phased out and are not recommended for new designs.

## . . . For CB and FM Transceivers

MC145106† CMOS frequency synthesizer contains an oscillator/amplifier, a $2^{10}$ divider chain for that oscillator signal, a programmable divider chain for the input signal and a phase detector. The MC145106 has circuitry for a 10.24 MHz oscillator or may operate with an external signal. A 5.12 MHz output signal can be used for frequency tripling. A $2^9$ programmable divider divides the input signal frequency for channel selection.

†Closest equivalent for MC145104, MC145107, MC145109, MC145112, and MC145143, which are being phased out and are not recommended for new designs.

**MC145106**

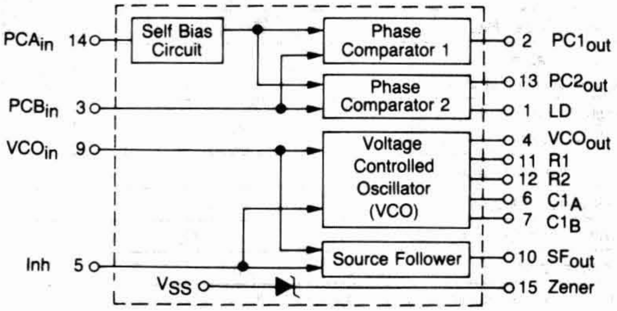


Osc$_{out}$
÷ 2$_{out}$
FS
4
5
6
Osc$_{in}$
3
Osc.
÷ 2
Reference Divide $2^9$ or $2^{10}$
Phase Detector
φDet$_{out}$
7
f$_{in}$
2
Divide-by-N Counter $2^9$ − 1
LD
8
17 16 15 14 13 12 11 10 9
P0 P1 P2 P3 P4 P5 P6 P7 P8
V$_{DD}$ = Pin 1
V$_{SS}$ = Pin 18

## . . . For FM/FSK Modulation and Demodulation

MC14046B CMOS Phase-Locked Loop contains a voltage-controlled oscillator and two phase comparators. Ideal for frequency synthesis, frequency discrimination, tone decoding, voltage-to-frequency conversion and motor speed control.

**MC14046B**



PCA$_{in}$ 14
Self Bias Circuit
Phase Comparator 1
2 PC1$_{out}$
13 PC2$_{out}$
PCB$_{in}$ 3
Phase Comparator 2
1 LD
VCO$_{in}$ 9
Voltage Controlled Oscillator (VCO)
4 VCO$_{out}$
11 R1
12 R2
6 C1$_A$
7 C1$_B$
Inh 5
Source Follower
10 SF$_{out}$
V$_{SS}$
15 Zener

# Components for PLL Circuit Development

The following functions are given in order of decreasing frequency within each category.

| Function | Family | Frequency MHz typ | Power Dissipation mW typ/pkg | Type |  | Case① |
|---|---|---|---|---|---|---|
|  |  |  |  | −55 to +125°C | 0 to +75°C |  |
| **Combination Functions** |  |  |  |  |  |  |
| Phase-Locked Loop | LINEAR | 0.5 | 825 | — | NE565C | 646 |
| **Oscillators** |  |  |  |  |  |  |
| Crystal Oscillator | MECL | 2.0 to 20 | 210 | MC12561 | MC12061 | 620, 648 |
| Voltage-Controlled Oscillator | MECL | 225 | 150 | MC1648M | MC1648# | 607, 632, 646 |
| Voltage-Controlled Multivibrator | MECL | 150 | 150 | — | MC1658# | 620, 648, 650 |
| Dual Voltage-Controlled Multivibrator | TTL | 30 | 150 | MC4324 | MC4024 | 607, 632, 646 |
| Voltage Controlled Oscillator | TTL | 16 | — | — | SN74LS724 | 626, 693 |
| **Phase Detectors** |  |  |  |  |  |  |
| Digital |  |  |  |  |  |  |
| Phase-Frequency Detector | MECL | 70 | 520 | MC12540 | MC12040 | 607, 632, 646 |
| Phase-Frequency Detector | MTTL | 8.0 | 85 | MC4344 | MC4044 | 607, 632, 646 |
| Analog |  |  |  |  |  |  |
| Analog Mixer — Double Balanced | MECL | 100 | 60 | MC12502 | MC12002# | 632, 646 |
| Modulator/Demodulator | LINEAR | 10 | 575 | MC1596 | MC1496 | 603, 632, 646 |
| Modulator/Demodulator | LINEAR | 1.0 | 750 | MC1594 | MC1494 | 620 |
| Modulator/Demodulator | LINEAR | 1.0 | 135 | MC1595 | MC1495 | 632 |
| **Control Functions** |  |  |  |  |  |  |
| Counter Control Logic | MECL | 25 | 150 | MC12514 | MC12014 | 620, 648 |
| TV Interface Control | LINEAR | — | 360 | MC2801P |  | 707 |
| **Prescalers** |  |  |  |  |  |  |
| High-Speed Prescaler (÷256/64) | MECL | 950 | 350 | — | MC12071** | 646 |
| ÷2 Counter | MECL | 750 | — | — | MC12090 | 620, 648 |
| ÷4 Counter | MECL | 1100 | 322 | — | MC1697 | 626, 693 |
| ÷4 Counter | MECL | 1100 | 322 | — | MC1699# | 620, 650 |
| Two-Modulus Prescaler (÷5/÷6) | MECL | 500 | 350 | MC12509 | MC12009 | 620, 648 |
| Two-Modulus Prescaler (÷8/÷9) | MECL | 550 | 350 | MC12511 | MC12011 | 620, 648 |
| Two-Modulus Prescaler (÷10/11) | MECL | 600 | 350 | MC12513 | MC12013# | 620, 648, 650 |
| UHF Type D Prescaler (÷2) | MECL | 500 | — | — | MC1690# | 620, 650 |
| Two-Modulus Prescaler (÷32/33) | MECL | 225 | 7.0 mA‡ | — | MC12015§ | 626 |
| Two-Modulus Prescaler (÷40/41) | MECL | 225 | 7.0 mA‡ | — | MC12016§ | 626 |
| Two-Modulus Prescaler (÷64/65) | MECL | 225 | 7.0 mA‡ | — | MC12017§ | 626 |
| Divide-by-20 Prescaler | LINEAR | 200 | 150 | MC3396§ |  | 626 |
| Two-Modulus Prescaler (÷15/16) | LINEAR | 140 | 200 | MC3393§ |  | 626 |
| Dual Type D | LS TTL | 45 | 20 | SN54LS74 | SN74LS74 | 717, 632, 646 |
| Dual Type D | CMOS | 27* | — | MC54HC74 | MC74HC74§ | 632, 646 |

① Plastic package available for commercial-temperature devices only.

* @ 4.5 V, 25°C

** $T_A$ = 0 to +70°C

§ $T_A$ = −40 to +85°C

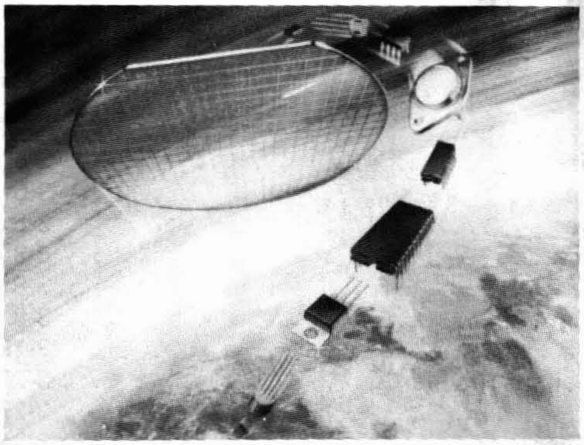
# $T_A$ = −30 to +85°C

‡ 7.0 mA @ 6.8 V = 47.6 mW

The following functions are given in order of decreasing frequency within each category.

| Function | Family | Frequency MHz typ | Power Dissipation mW typ/pkg | Type | | Case① |
|---|---|---|---|---|---|---|
| | | | | −55 to +125°C | 0 to +75°C | |
| **Counters** | | | | | | |
| Binary | MECL | 325 | 750 | — | MC1654# | 620 |
| Bi-Quinary (÷2, ÷5, ÷10) | MECL | 325 | 750 | — | MC1678# | 620 |
| Universal Hexadecimal (÷0–15) | MECL | 150 | 625 | — | — | 620, 648 |
| Universal Decade | MECL | 150 | 625 | — | — | 620, 648, 650 |
| Bi-Quinary | MECL | 150 | 370 | MC10538 | MC10138# | 620, 648, 650 |
| Binary | MECL | 150 | 370 | MC10578 | MC10178# | 620, 648, 650 |
| Presettable Binary (÷2, ÷8) | LS TTL | 60 | 60 | SN54LS197 | SN74LS197 | 717, 632, 646 |
| Presettable Decade (÷2, ÷5) | LS TTL | 60 | 60 | SN54LS196 | SN74LS196 | 717, 632, 646 |
| Presettable Up/Down Decade | LS TTL | 40 | 95 | SN54LS192 | SN74LS192 | 620, 648, 650 |
| Presettable Up/Down Binary | LS TTL | 40 | 95 | SN54LS193 | SN74LS193 | 620, 648, 650 |
| Presettable Decade | LS TTL | 35 | 95 | SN54LS160 | SN74LS160 | 620, 648, 650 |
| Presettable Binary | LS TTL | 35 | 95 | SN54LS161 | SN74LS161 | 620, 648, 650 |
| Presettable Decade | LS TTL | 35 | 95 | SN54LS162 | SN74LS162 | 620, 648, 650 |
| Presettable Binary | LS TTL | 35 | 95 | SN54LS163 | SN74LS163 | 620, 648, 650 |
| Presettable Up/Down Decade | LS TTL | 35 | 95 | SN54LS190 | SN74LS190 | 620, 648, 650 |
| Presettable Up/Down Binary | LS TTL | 35 | 95 | SN54LS191 | SN74LS191 | 620, 648, 650 |
| Decade (÷2, ÷5) | LS TTL | 32** | 45 | SN54LS90 | SN74LS90 | 717, 632, 646 |
| Binary (÷2, ÷8) | LS TTL | 32** | 45 | SN54LS93 | SN74LS93 | 717, 632, 646 |
| Universal (÷2–12 except 7 and 11) | MTTL | 30 | 200 | MC4323 | MC4023 | 607, 632, 646 |
| Presettable BCD Counter with Asynchronous Reset | CMOS | 27* | — | MC54HC160 | MC74HC160§ | 620, 648 |
| Presettable 4-Bit Binary Counter with Asynchronous Reset | CMOS | 27* | — | MC54HC161 | MC74HC161§ | 620, 648 |
| Presettable BCD Counter with Synchronous Reset | CMOS | 27* | — | MC54HC162 | MC74HC162§ | 620, 648 |
| Presettable 4-Bit Binary Counter with Synchronous Reset | CMOS | 27* | — | MC54HC163 | MC74HC163§ | 620, 648 |
| Presettable BCD Up/Down Counter | CMOS | — | — | MC54HC190 | MC74HC190§ | 620, 648 |
| Presettable 4-Bit Binary Up/Down Counter | CMOS | — | — | MC54HC191 | MC74HC191§ | 620, 648 |
| Dual 4-Stage Binary Ripple Counter (÷2 and ÷5) | CMOS | 27* | — | MC54HC390 | MC74HC390§ | 620, 648 |
| Dual 4-Stage Binary Ripple Counter | CMOS | 27* | — | MC54HC393 | MC74HC393§ | 632 |
| Decade Counter/Divider | CMOS | 20* | — | MC54HC4017 | MC74HC4017§ | 620, 648 |
| 14-Stage Binary Ripple Counter | CMOS | — | — | MC54HC4020 | MC74HC4020§ | 620, 648 |
| 7-Stage Binary Ripple Counter | CMOS | 27* | — | MC54HC4024 | MC74HC4024§ | 632, 646 |
| 12-Stage Binary Ripple Counter | CMOS | 20* | — | MC54HC4040 | MC74HC4040§ | 620, 648 |
| 14-Stage Binary Ripple Counter with Oscillator | CMOS | 20* | — | MC54HC4060 | MC74HC4060§ | 620, 648 |
| Decade (÷2, ÷5, ÷10) | MTTL | 20 | 160 | — | — | 607, 632, 646 |
| Programmable ÷N Decade (÷0–9) | MTTL | 10 | 250 | MC4316 | MC4016 | 620, 648, 650 |
| Two Programmable ÷N (÷0–1, ÷0–4) | MTTL | 10 | 250 | MC4317 | MC4017 | 620, 648, 650 |
| Programmable ÷N Hexadecimal (÷0–15) | MTTL | 10 | 250 | MC4318 | MC4018 | 620, 648, 650 |
| Two Programmable ÷N (÷0–3, ÷0–3) | MTTL | 10 | 250 | MC4319 | MC4019 | 620, 648, 650 |

① Plastic package available for commercial-temperature devices only.
* @ 4.5 V, 25°C
** $T_A$ = 0 to +70°C
§ $T_A$ = −40 to +85°C
# $T_A$ = −30 to +85°C
‡ 7.0 mA @ 6.8 V = 47.6 mW



# Analog Circuits

Amplifiers

Data Converters

Comparators

Special Circuits

# ANALOG CIRCUITS

## Amplifiers

| Device | Function | Page |
|---|---|---|
| LF347 | Family of BIFET Operational Amplifiers | 3-6 |
| LF351 | Family of BIFET Operational Amplifiers | 3-6 |
| LF353 | Family of BIFET Operational Amplifiers | 3-6 |
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| LF356,B | Monolithic JFET Operation Amplifier | 3-8 |
| LF357,B | Monolithic JFET Operational Amplifier | 3-8 |
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| LM248 | Quad MC1741 Operational Amplifier | 3-40 |
| LM258 | Dual Low-Power Operational Amplifier | 3-46 |
| LM301A | General Purpose Adjustable Operational Amplifier | 3-25 |
| LM307 | Internally Compensated Monolithic Operational Amplifier | 3-52 |
| LM308,A | Precision Operational Amplifiers | 3-25 |
| LM324,A | Quad Low-Power Operational Amplifier | 3-34 |
| LM348 | Quad MC1741 Operational Amplifier | 3-40 |
| LM358 | Dual Low-Power Operational Amplifier | 3-46 |
| LM2900 | Quad Single-Supply Operational Amplifier | 3-147 |
| LM2902 | Quad Low-Power Operational Amplifier | 3-34 |
| LM2904 | Dual Low-Power Operational Amplifier | 3-46 |
| LM3900 | Quad Single-Supply Operational Amplifier | 3-147 |
| MC1436,C | High-Voltage Operational Amplifier | 3-56 |
| MC1437 | Dual Operational Amplifier | 3-60 |
| MC1439 | High-Slew-Rate Operational Amplifier | 3-64 |
| MC1445 | Wideband Amplifier | 3-72 |
| MC1454G | 1-Watt Power Amplifier | 3-78 |
| MC1456,C | High-Performance Operational Amplifier | 3-82 |
| MC1458,C | Dual Operational Amplifiers | 3-88 |
| MC1458S | High-Slew-Rate Dual Operational Amplifier | 3-93 |
| MC1536 | High-Voltage Operational Amplifiers | 3-56 |
| MC1537 | Dual Operational Amplifier | 3-60 |
| MC1539 | High-Slew-Rate Operational Amplifier | 3-64 |
| MC1545 | Wideband Amplifier | 3-72 |
| MC1554G | 1-Watt Power Amplifier | 3-78 |
| MC1556 | High-Performance Operational Amplifier | 3-82 |
| MC1558 | Low-Noise Dual Operational Amplifier | 3-88 |
| MC1558S | High-Slew-Rate Dual Operational Amplifier | 3-93 |
| MC1590G | Wideband Amplifier with AGC | 3-99 |
| MC1709,A,C | General-Purpose Operational Amplifier | 3-107 |
| MC1733,C | Differential Video Amplifier | 3-111 |
| MC1741,C | General-Purpose Operational Amplifier | 3-119 |
| MC1741S,SC | High-Slew-Rate Operational Amplifier | 3-124 |
| MC1747,C | Dual MC1741 Operational Amplifier | 3-130 |
| MC1748,C | General-Purpose Operational Amplifier | 3-134 |
| MC1776,C | Programmable Operational Amplifier | 3-138 |
| MC3301 | Quad Operational Amplifier | 3-147 |
| MC3303 | Quad Differential-Input Operational Amplifier | 3-157 |

## Amplifiers (con't)

| Device | Function | Page |
|---|---|---|
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| MC3401 | Quad Operational Amplifier | 3-147 |
| MC3403 | Quad Differential-Input Operational Amplifier | 3-157 |
| MC3405 | Dual Operational Amplifier plus Dual Voltage Comparator | 3-163 |
| MC3458 | Dual Low-Power Operational Amplifier | 3-171 |
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| MC3503 | Quad Differential-Input Operational Amplifier | 3-157 |
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| MC34081 | High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC34082 | Dual High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC34083 | Dual High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC34084 | Quad High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC34085 | Quad High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC35071 | High-Performance Single-Supply Operational Amplifier | 3-226 |
| MC35072 | Dual High-Performance Single-Supply Operational Amplifier | 3-226 |
| MC35074,A | Quad High-Performance Single-Supply Operational Amplifier | 3-210 |
| MC35080 | High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC35081 | High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC35082 | Dual High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
| MC35083 | Dual High-Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier | 3-226 |
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# ANALOG CIRCUITS (con't)

## Amplifiers (con't)

| Device | Function | Page |
|---|---|---|
| MC35171 | Low-Power, Single-Supply Operational Amplifier | 3-192 |
| MC35172 | Dual Low-Power, Single-Supply Operational Amplifier | 3-192 |
| MC35174 | Quad Low-Power, Single Supply Operational Amplifier | 3-192 |
| NE592 | Video Amplifier | 3-237 |
| OP-27 | Ultra-Low Noise Precision, High Speed Operational Amplifiers | 3-242 |
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| AD563 | Complete 12-Bit High-Speed Monolithic D/A Converter | 3-270 |
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| MC1506L | 6-Bit Multiplying Digital-to-Analog Converter | 3-285 |
| MC1508 | 8-Bit Multiplying Digital-to-Analog Converter | 3-297 |
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| MC3417 | Continuously Variable Slope Delta Modulator/Demodulator | 3-325 |
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| MC3512 | High-Speed 12-Bit D/A Converter | 3-320 |
| MC3517 | Continuously Variable Slope Delta Modulator/Demodulator | 3-325 |
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| MC6890 | 8-Bit Bus-Compatible MPU D/A Converter | 3-345 |
| MC10315L | Seven-Bit Parallel High-Speed A/D Converter | 3-352 |
| MC10317L | Seven-Bit Parallel High-Speed A/D Converter | 3-352 |
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|---|---|---|
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| LM139,A | Quad Single-Supply Comparators | 3-399 |
| LM193,A | Dual Comparators | 3-403 |
| LM211 | High Performance Voltage Comparator | 3-393 |
| LM239,A | Quad Single-Supply Comparators | 3-399 |
| LM293,A | Dual Comparators | 3-403 |
| LM311 | High Performance Voltage Comparator | 3-393 |
| LM339,A | Quad Single-Supply Comparators | 3-399 |
| LM393,A | Dual Comparators | 3-403 |
| LM2901 | Quad Single-Supply Comparators | 3-399 |
| LM2903 | Dual Comparators | 3-403 |
| MC3302 | Quad Single-Supply Comparators | 3-399 |
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| MC3424,A | Power Supply Supervisory Circuit/Dual-Voltage Comparator | 3-408 |
| MC3430 | High-Speed Quad Comparator | 3-409 |
| MC3431 | High-Speed Quad Comparator | 3-409 |
| MC3432 | High-Speed Quad Comparator | 3-409 |
| MC3433 | High-Speed Quad Comparator | 3-409 |
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## Special Circuits

| Device | Function | Page |
|---|---|---|
| MC1455 | Timing Circuit | 3-417 |
| MC1494L | Four-Quadrant Multiplier | 3-424 |
| MC1495L | Four-Quadrant Multiplier | 3-438 |
| MC1496 | Balanced Modulator-Demodulator | 3-453 |
| MC1555 | Timing Circuit | 3-417 |
| MC1594L | Four-Quadrant Multiplier | 3-424 |
| MC1595L | Four-Quadrant Multiplier | 3-438 |
| MC1596 | Balanced Modulator-Demodulator | 3-453 |
| MC3373 | Remote Control Amplifier-Detector | 3-463 |
| MC3456 | Dual Timing Circuit | 3-467 |
| MC3556 | Dual Timing Circuit | 3-467 |

# LF347
# LF351
# LF353

## FAMILY OF BIFET OPERATIONAL AMPLIFIERS

### SILICON MONOLITHIC INTEGRATED CIRCUITS

**ODERING INFORMATION**

| Op Amp Function | Device | Package |
|---|---|---|
| Single | LF351D | SO-8 |
| Single | LF351N | Plastic DIP |
| Dual | LF353D | SO-8 |
| Dual | LF353N | Plastic DIP |
| Quad | LF347D | SO-14 |
| Quad | LF347BN | Plastic DIP |
| Quad | LF347N | Plastic DIP |

## JFET INPUT OPERATIONAL AMPLIFIERS

These low-cost JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices.

- Input Offset Voltage of 5.0 mV Max (LF347B)
- Low Input Bias Current – 50 pA
- Low Input Noise Voltage – 16 nV/$\sqrt{\text{Hz}}$
- Wide Gain Bandwidth – 4.0 MHz
- High Slew Rate – 13 V/µs
- Low Supply Current – 1.8 mA per Amplifier
- High Input Impedance – $10^{12}$ Ω
- High Common-Mode and Supply Voltage Rejection Ratios – 100 dB

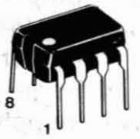
**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>−18 | V |
| Differential Input Voltage | $V_{ID}$ | ±30 | V |
| Input Voltage Range (Note 1) | $V_{IDR}$ | ±15 | V |
| Output Short Circuit Duration (Note 2) | $t_S$ | Continuous | |
| Power Dissipation at $T_A = +25°C$ | $P_D$ | 900 | mW |
| Derate above $T_A = +25°C$ | $1/\theta_{JA}$ | 10 | mW/°C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Operating Junction Temperature Range | $T_J$ | 115 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**NOTES:**

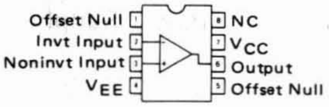
1. Unless otherwise specified, the absolute maximum negative input voltage is limited to the negative power supply.

2. Any amplifier output can be shorted to ground indefinitely. However, if more than one amplifier output is shorted simultaneously, maximum junction temperature ratings may be exceeded.

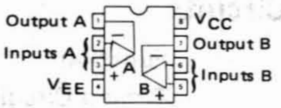


**N SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(LF351, LF353 only)

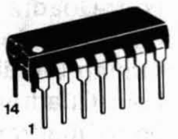
**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8
(LF351, LF353 Only)



LF351
(Top View)

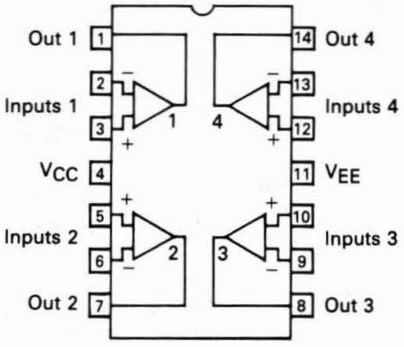


LF353
(Top View)



**N SUFFIX**
PLASTIC PACKAGE
CASE 646-05
(LF347 only)

**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14



(Top View)

**NOTES:** (continued)

3. Input bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature. To maintain junction temperatures as close to ambient as is possible, pulse techniques are utilized during test.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = 25°C unless otherwise noted).

| Characteristic | Symbol | LF347B Min | LF347B Typ | LF347B Max | LF347, LF351, LF353 Min | LF347, LF351, LF353 Typ | LF347, LF351, LF353 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage ($R_S \leq$ 10 k, $V_{CM}$ = 0) | $V_{IO}$ | | | | | | | mV |
| $T_A$ = +25°C | | — | 1.0 | 5.0 | — | 5.0 | 10 | |
| 0°C ≤ $T_A$ ≤ +70°C | | — | — | 8.0 | — | — | 13 | |
| Average Temperature Coefficient of Input Offset Voltage<br>$R_S \leq$ 10 k, 0°C ≤ $T_A$ ≤ +70°C | $\Delta V_{IO}/\Delta T$ | — | 10 | — | — | 10 | — | μV/°C |
| Input Offset Current ($V_{CM}$ = 0, Note 3) | $I_{IO}$ | | | | | | | |
| $T_A$ = +25°C | | — | 25 | 100 | — | 25 | 100 | pA |
| 0°C ≤ $T_A$ ≤ +70°C | | — | — | 4.0 | — | — | 4.0 | nA |
| Input Bias Current ($V_{CM}$ = 0, Note 3) | $I_{IB}$ | | | | | | | |
| $T_A$ = +25°C | | — | 50 | 200 | — | 50 | 200 | pA |
| 0°C ≤ $T_A$ ≤ +70°C | | — | — | 8.0 | — | — | 8.0 | nA |
| Input Resistance | $r_i$ | — | $10^{12}$ | — | — | $10^{12}$ | — | Ω |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±11 | +15<br>−12 | — | ±11 | +15<br>−12 | — | V |
| Large-Signal Voltage Gain ($V_O$ = ±10 V, $R_L$ = 2.0 k) | $A_{VOL}$ | | | | | | | V/mV |
| $T_A$ = +25°C | | 50 | 100 | — | 25 | 100 | — | |
| 0°C ≤ $T_A$ ≤ +70°C | | 25 | — | — | 15 | — | — | |
| Output Voltage Swing ($R_L$ = 10 k) | $V_O$ | ±12 | ±14 | — | ±12 | ±14 | — | V |
| Common Mode Rejection Ratio ($R_S \leq$ 10 k) | CMRR | 80 | 100 | — | 70 | 100 | — | dB |
| Supply Voltage Rejection Ratio ($R_S \leq$ 10 k) | PSRR | 80 | 100 | — | 70 | 100 | — | dB |
| Supply Current | $I_D$ | | | | | | | mA |
| LF347 | | — | 7.2 | 11 | — | 7.2 | 11 | |
| LF351 | | — | — | — | — | 1.8 | 3.4 | |
| LF353 | | — | — | — | — | 3.6 | 6.5 | |
| Slew Rate ($A_V$ = +1) | SR | — | 13 | — | — | 13 | — | V/μs |
| Gain-Bandwidth Product | $BW_p$ | — | 4.0 | — | — | 4.0 | — | MHz |
| Equivalent Input Noise Voltage<br>($R_S$ = 100 Ω, f = 1000 Hz) | $e_n$ | — | 16 | — | — | 16 | — | nV/√Hz |
| Equivalent Input Noise Current (f = 1000 Hz) | $i_n$ | — | 0.01 | — | — | 0.01 | — | pA/√Hz |
| Channel Separation (LF347, LF353)<br>1.0 Hz ≤ f ≤ 20 kHz (Input Referred) | — | — | −120 | — | — | −120 | — | dB |

**For Typical Characteristic Performance Curves, refer to MC34001/34002/34004 data sheet.**

**MOTOROLA**

# LF355, LF356, LF357* LF355B, LF356B, LF357B*

## Specifications and Applications Information

### MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS

These internally compensated operational amplifiers incorporate highly matched JFET devices on the same chip with standard bipolar transistors. The JFET devices enhance the input characteristics of these operational amplifiers by more than an order of magnitude over conventional amplifiers.

This series of op amps combines the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Also, nulling the offset voltage does not degrade the drift or common mode rejection.

- Low Input Bias Current – 30 pA
- Low Input Offset Current – 3.0 pA
- Low Input Offset Voltage – 1.0 mV
- Temperature Compensation of Input Offset Voltage – 3.0 $\mu$V/°C
- Low Input Noise Current – 0.01 pA/$\sqrt{\text{Hz}}$
- High Input Impedance – $10^{12}\Omega$
- High Common-Mode Rejection Ratio – 100 dB
- High DC Voltage Gain – 106 dB

### SERIES FEATURES

- LF355/355B — Low Power Supply Current
- LF356/356B — Wide Bandwidth
- LF357/357B — **Wider** Bandwidth Decompensated ($A_{V_{min}} = 5$)

| | LF355/355B | LF356/356B | LF357/357B |
|---|---|---|---|
| Fast Settling Time to 0.01% | 4.0 $\mu$s | 1.5 $\mu$s | 1.5 $\mu$s |
| Fast Slew Rate | 5.0 V/$\mu$s | 12 V/$\mu$s | 50 V/$\mu$s |
| Wide Gain Bandwidth | 2.5 MHz | 5.0 MHz | 20 MHz |
| Low Input Noise Voltage | 20 nV/$\sqrt{\text{Hz}}$ | 12 nV/$\sqrt{\text{Hz}}$ | 12 nV/$\sqrt{\text{Hz}}$ |

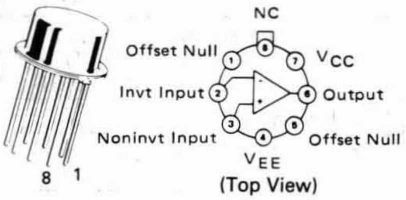
**ORDERING INFORMATION**

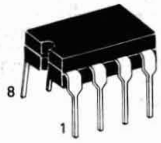
| Device | Temperature Range | Package |
|---|---|---|
| LF355BH,H<br>LF355BJ,J | 0 to +70°C<br>0 to +70°C | Metal Can<br>Ceramic DIP |
| LF356BH,H<br>LF356BJ,J | 0 to +70°C<br>0 to +70°C | Metal Can<br>Ceramic DIP |
| LF357BH,H<br>LF357BJ,J | 0 to +70°C<br>0 to +70°C | Metal Can<br>Ceramic DIP |

### MONOLITHIC JFET OPERATIONAL AMPLIFIERS

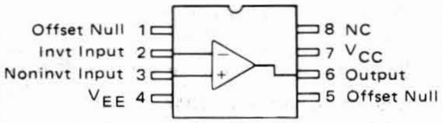
**SILICON MONOLITHIC INTEGRATED CIRCUITS**

**H SUFFIX**
METAL PACKAGE
CASE 601-04





**J SUFFIX**
CERAMIC PACKAGE
CASE 693-02



(Top View)

### APPLICATIONS

The LF series is suggested for all general purpose FET input amplifier requirements where precision and frequency response flexibility are of prime importance.

Specific applications include:

- Sample and Hold Circuits
- High Impedance Buffers
- Fast D/A and A/D Converters
- Precision High-Speed Integrators
- Wideband, Low Noise, Low Drift Amplifiers

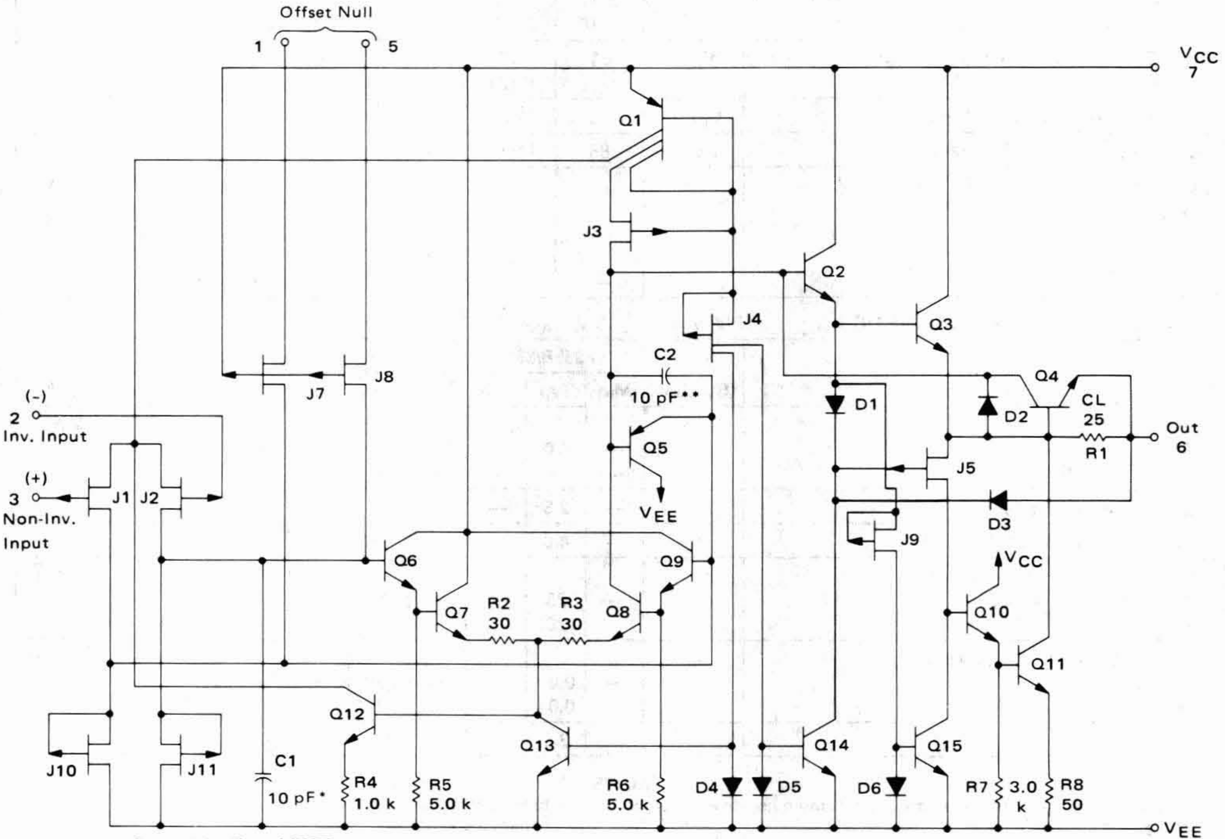
***NOTE:** The LF357/357B are designed for wider bandwidth applications. They are decompensated ($A_{V_{min}} = 5$).

## MAXIMUM RATINGS

| Rating | Symbol | LF355B/ 356B/357B | LF355/356/357 | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +22<br>−22 | +18<br>−18 | V |
| Differential Input Voltage | $V_{ID}$ | ±40 | ±30 | V |
| Input Voltage Range (Note 1) | $V_{IDR}$ | ±20 | ±16 | V |
| Output Short-Circuit Duration | $T_S$ | Continuous | | |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | | °C |
| Operating Junction Temperature<br>Metal and Ceramic Packages<br>Plastic Package | $T_J$ | <br>115<br>100 | | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | | °C |

Note 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

## CIRCUIT SCHEMATIC


Offset Null
1
5
VCC
7
Q1
J3
Q2
J4
Q3
C2
10 pF**
J8
J7
Q4
D1
D2
CL
25
R1
Out
6
(−)
2
Inv. Input
(+)
3
Non-Inv.
Input
J1
J2
Q5
VEE
J5
D3
J9
Q6
Q9
VCC
Q7
R2
30
R3
30
Q8
Q10
Q11
Q12
Q13
Q14
Q15
J10
J11
C1
10 pF*
R4
1.0 k
R5
5.0 k
R6
5.0 k
D4
D5
D6
R7
3.0 k
R8
50
VEE

*C1 = 5.0 pF on LF357.
**C2 = 2.0 pF on LF357.

**DC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 to 20 V, $V_{EE}$ = −15 to −20 V for LF355B/356B/357B; $V_{CC}$ = 15 V, $V_{EE}$ = −15 V for LF355/356/357; $T_A$ = 0°C to +70°C unless otherwise noted)

| Characteristic | Symbol | LF355B/6B/7B | | | LF355/6/7 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($R_S$ = 50 Ω, $V_{CM}$ = 0)<br>($T_A$ = 25°C)<br>(Over Temperature) | $V_{IO}$ | —<br>— | 3.0<br>— | 5.0<br>6.5 | —<br>— | 3.0<br>— | 10<br>13 | mV |
| Average Temperature Coefficient of Input Offset Voltage ($R_S$ = 50 Ω) | $\Delta V_{IO}/\Delta T$ | — | 5.0 | — | — | 5.0 | — | μV/°C |
| Change in Average TC with $V_{IO}$ Adjust ($R_S$ = 50 Ω) (Note 2) | $\Delta TC/\Delta V_{IO}$ | — | 0.5 | — | — | 0.5 | — | μV/°C per mV |
| Input Offset Current ($V_{CM}$ = 0) (Note 3)<br>($T_J$ = 25°C)<br>($T_J \leq$ 70°C) | $I_{IO}$ | —<br>— | 3.0<br>— | 20<br>1.0 | —<br>— | 3.0<br>— | 50<br>2.0 | pA<br>nA |
| Input Bias Current ($V_{CM}$ = 0) (Note 3)<br>($T_J$ = 25°C)<br>($T_J \leq$ 70°C) | $I_{IB}$ | —<br>— | 30<br>— | 100<br>5.0 | —<br>— | 30<br>— | 200<br>8.0 | pA<br>nA |
| Input Resistance ($T_J$ = 25°C) | $r_i$ | — | $10^{12}$ | — | — | $10^{12}$ | — | Ω |
| Large Signal Voltage Gain ($V_O$ = ±10 V, $R_L$ = 2.0 k, $V_{CC}$ = 15 V, $V_{EE}$ = −15 V)<br>($T_A$ = 25°C)<br>(0°C ≤ $T_A$ ≤ +70°C) | $A_{VOL}$ | 50<br>25 | 200<br>— | —<br>— | 25<br>15 | 200<br>— | —<br>— | V/mV |
| Output Voltage Swing<br>($V_{CC}$ = 15 V, $V_{EE}$ = −15 V, $R_L$ = 10 kΩ)<br>($V_{CC}$ = 15 V, $V_{EE}$ = −15 V, $R_L$ = 2 kΩ) | $V_O$ | ±12<br>±10 | ±13<br>±12 | —<br>— | ±12<br>±10 | ±13<br>±12 | —<br>— | V |
| Input Common-Mode Voltage Range ($V_{CC}$ = 15 V, $V_{EE}$ = −15 V) | $V_{ICR}$ | ±11 | +15.1<br>−12.0 | — | ±10 | +15.1<br>−12.0 | — | V |
| Common-Mode Rejection Ratio | CMRR | 85 | 100 | — | 80 | 100 | — | dB |
| Supply Voltage Rejection Ratio (Note 4) | PSRR | 85 | 100 | — | 80 | 100 | — | dB |
| Supply Current ($T_A$ = 25°C, $V_{CC}$ = 15 V, $V_{EE}$ = −15 V)<br>LF355B/355<br>LF356B/357B<br>LF356/357 | $I_D$ | —<br>—<br>— | 2.0<br>5.0<br>— | 4.0<br>7.0<br>— | —<br>—<br>— | 2.0<br>—<br>5.0 | 4.0<br>—<br>10 | mA |

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $V_{EE}$ = −15 V, $T_A$ = 25°C)

| Characteristic | Symbol | LF355B/355 | | | LF356B/356 | | | LF357B/357 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Slew Rate (Note 5)<br>($A_V$ = 1) LF355/356<br>($A_V$ = 5) LF357 | SR | —<br>— | 5.0<br>— | —<br>— | 7.5<br>— | 12<br>— | —<br>— | —<br>30 | —<br>50 | —<br>— | V/μs |
| Gain-Bandwidth Product | GBW | — | 2.5 | — | — | 5.0 | — | — | 20 | — | MHz |
| Settling Time to 0.01% (Note 6) | $t_s$ | — | 4.0 | — | — | 1.5 | — | — | 1.5 | — | μs |
| Equivalent Input Noise Voltage<br>($R_S$ = 100 Ω, f = 100 Hz)<br>($R_S$ = 100 Ω, f = 1000 Hz) | $e_n$ | —<br>— | 25<br>20 | —<br>— | —<br>— | 15<br>12 | —<br>— | —<br>— | 15<br>12 | —<br>— | nV/√Hz |
| Equivalent Input Noise Current<br>(f = 100 Hz)<br>(f = 1000 Hz) | $i_n$ | —<br>— | 0.01<br>0.01 | —<br>— | —<br>— | 0.01<br>0.01 | —<br>— | —<br>— | 0.01<br>0.01 | —<br>— | pA/√Hz |
| Input Capacitance | $C_i$ | — | 3.0 | — | — | 3.0 | — | — | 3.0 | — | pF |

**NOTES**

(1) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

(2) The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

(3) The input bias currents approximately double for every 10°C rise in junction temperature, $T_J$. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

(5) The Min. slew rate limits apply for the LF356B and the LF357B, but do not apply for the LF356 or LF357.

(6) Settling time is defined here, for a unity gain inverter connection using 2.0 k resistors for the LF355/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10 V step input is applied to the inverter. For the LF357, $A_V$ = −5.0, the feedback resistor from output to input is 2.0 k and the output step is 10 V (see settling time test circuit).

## TYPICAL DC PERFORMANCE CHARACTERISTICS
(Curves are for LF355, LF356, and LF357 series unless otherwise specified)

### INPUT BIAS CURRENT versus CASE TEMPERATURE

FIGURE 1 — (LF355 SERIES)

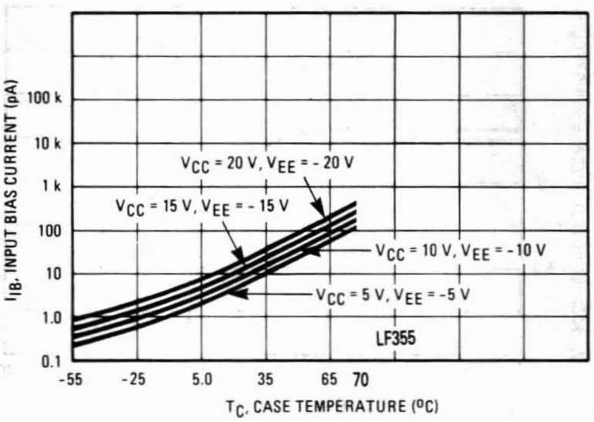


FIGURE 2 — (LF356 AND LF357 SERIES)

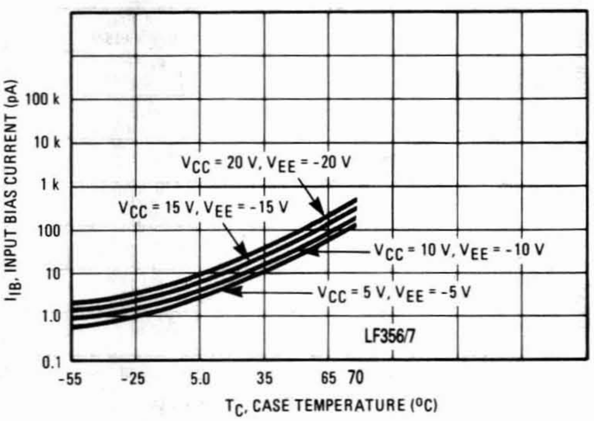


FIGURE 3 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

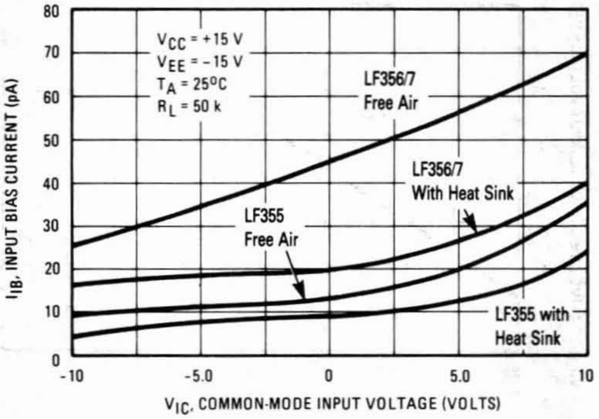
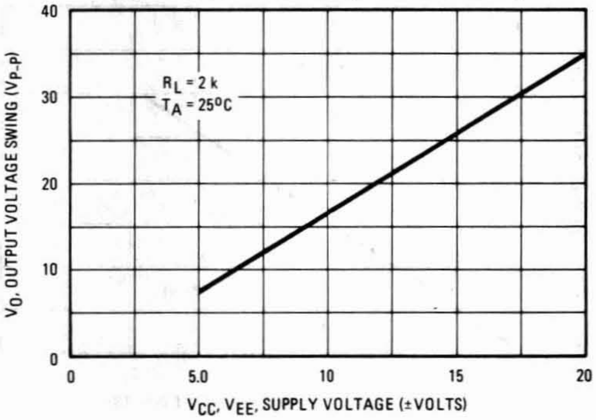


FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE (LF355B/356B/357B)



### SUPPLY CURRENT versus SUPPLY VOLTAGE

FIGURE 5 — (LF355 SERIES)

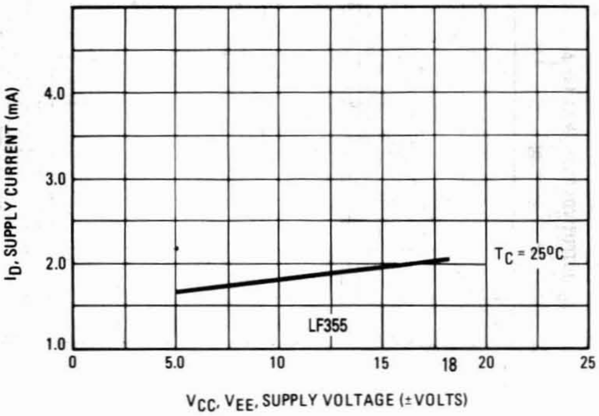
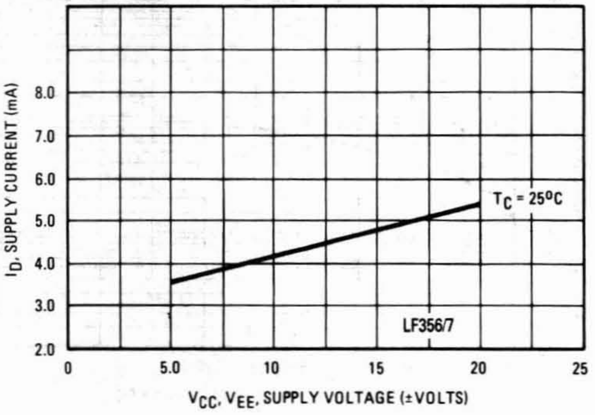


FIGURE 6 — (LF356 AND LF357 SERIES)



## TYPICAL DC PERFORMANCE CHARACTERISTICS (continued)

FIGURE 7 — NEGATIVE CURRENT LIMIT

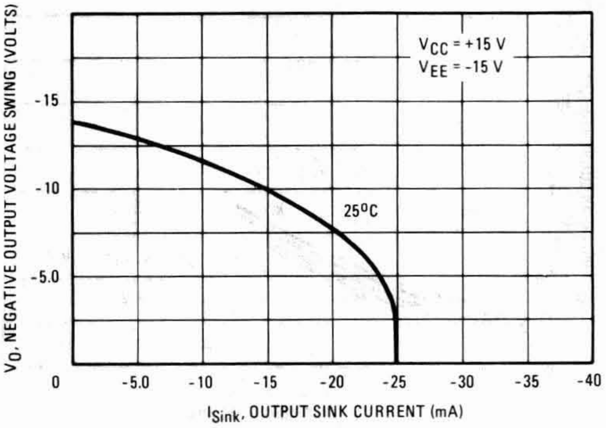


FIGURE 8 — POSITIVE CURRENT LIMIT

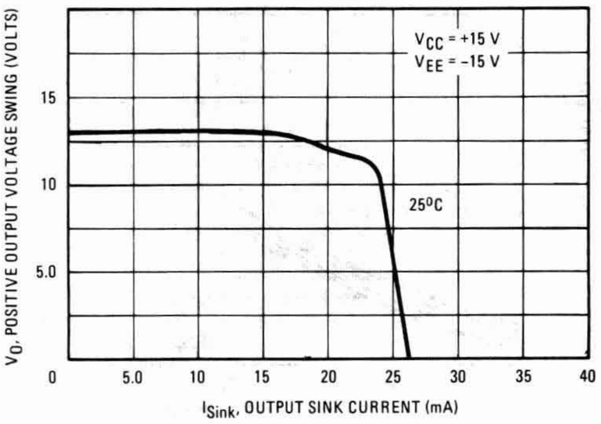


FIGURE 9 — POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT

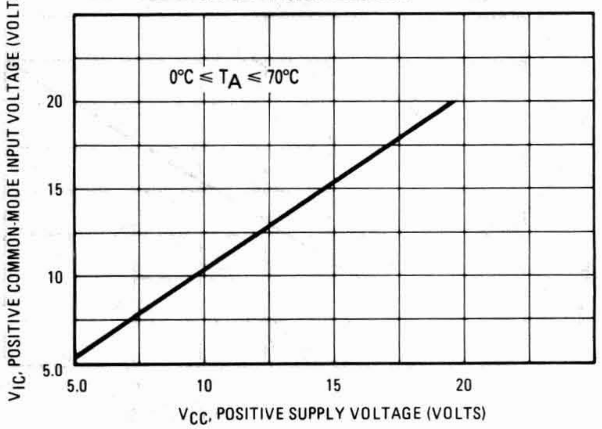


FIGURE 10 — NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT

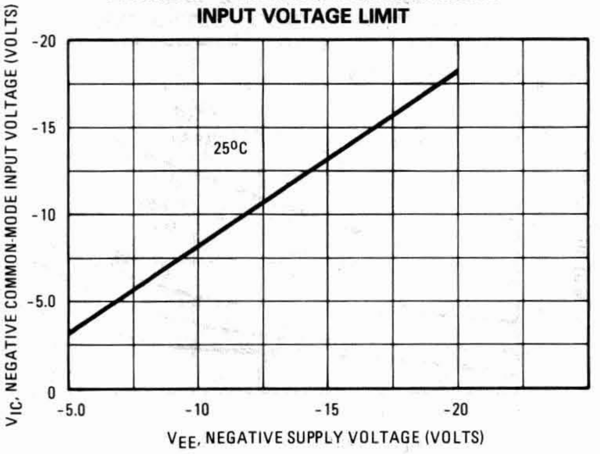


FIGURE 11 — OPEN LOOP VOLTAGE GAIN

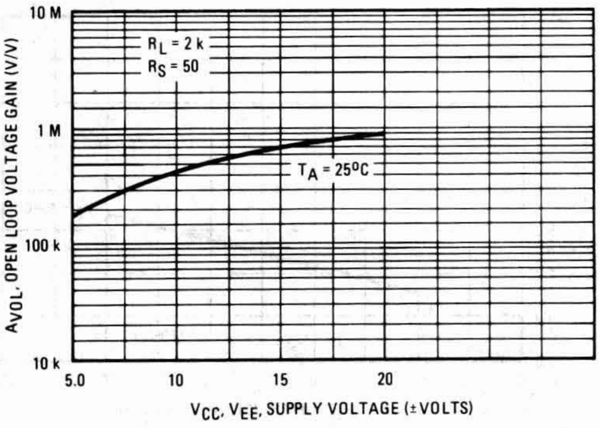
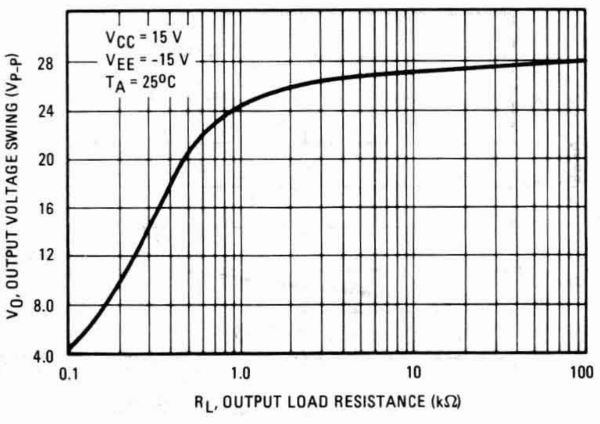


FIGURE 12 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



## TYPICAL AC PERFORMANCE CHARACTERISTICS

### GAIN BANDWIDTH PRODUCT

FIGURE 13 — (LF355 SERIES)

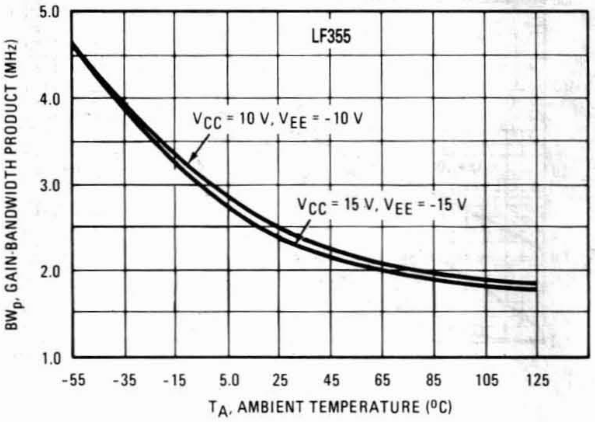
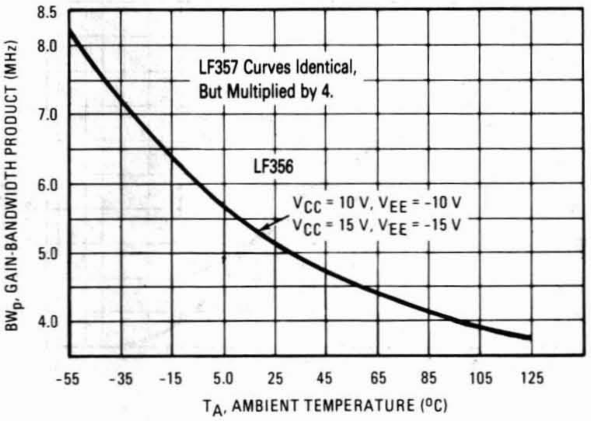


FIGURE 14 — (LF356/357 SERIES)



### INVERTER SETTLING TIME

FIGURE 15 — (LF355 SERIES)

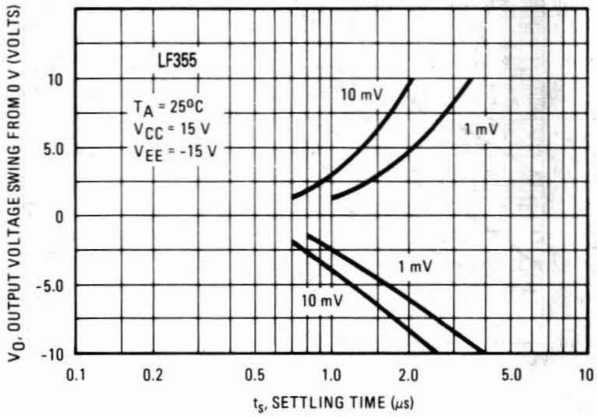


FIGURE 16 — (LF356 AND LF357 SERIES)

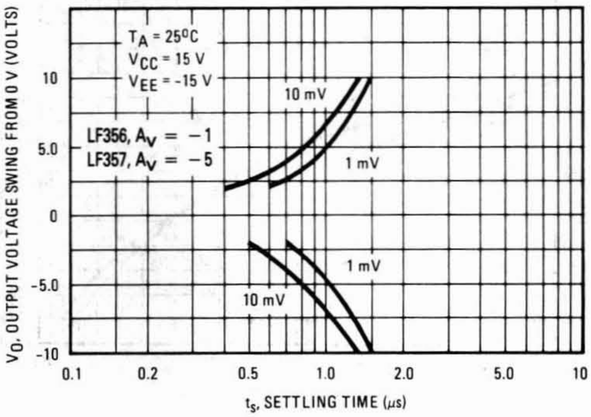


FIGURE 17 — NORMALIZED SLEW RATE

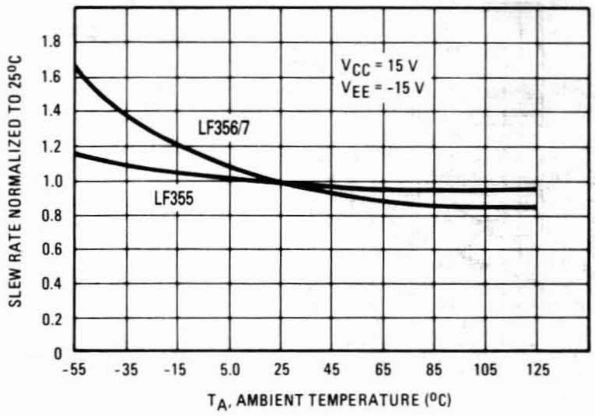
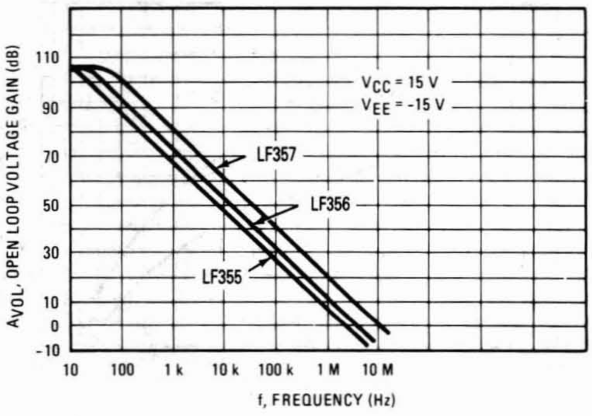


FIGURE 18 — OPEN LOOP FREQUENCY RESPONSE



## TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

### BODE PLOT

FIGURE 19 — (LF355 SERIES)

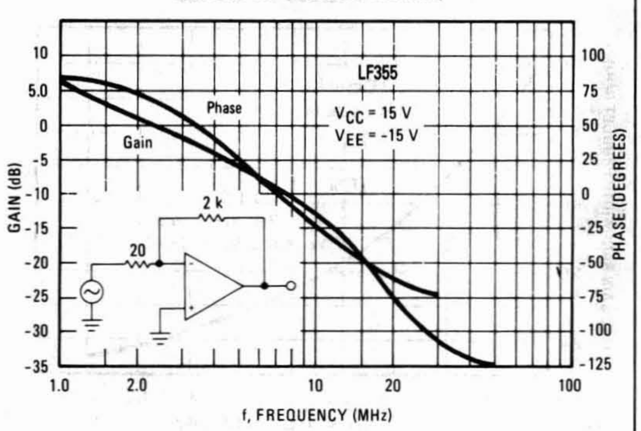


FIGURE 20 — (LF356 SERIES)

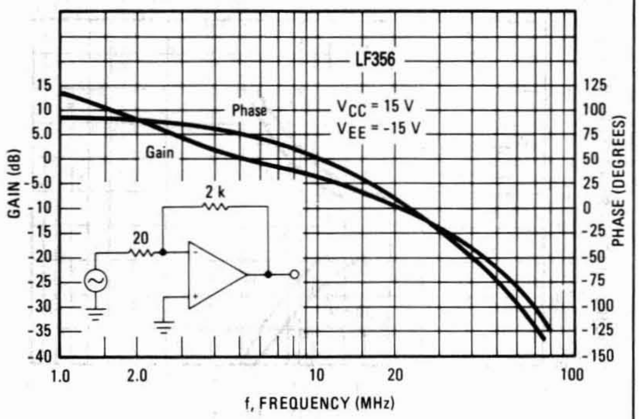
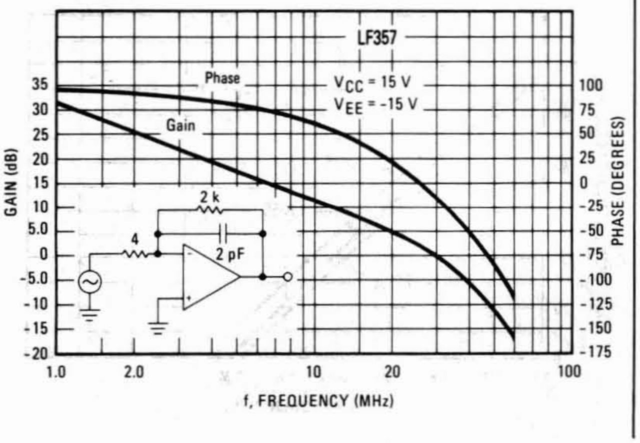


FIGURE 21 — (LF357 SERIES)



### OUTPUT IMPEDANCE

FIGURE 22 — (LF355 SERIES)

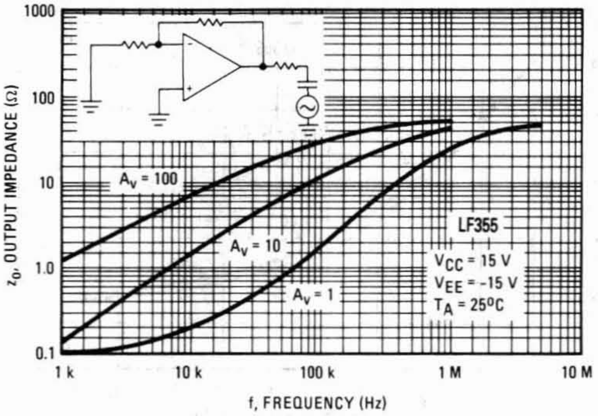


FIGURE 23 — (LF356 SERIES)

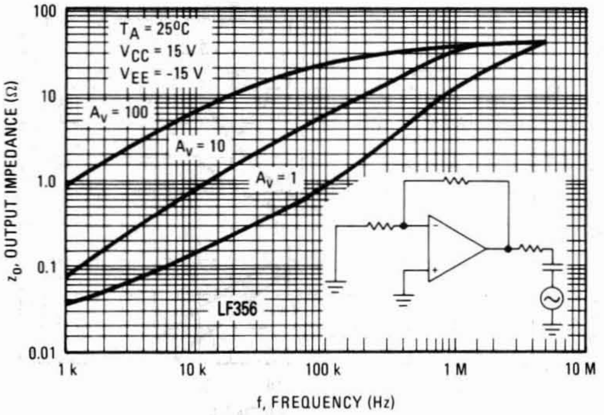
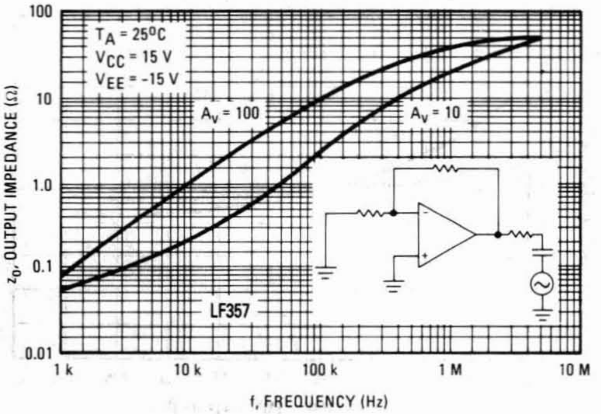


FIGURE 24 — (LF357 SERIES)



## TYPICAL AC PERFORMANCE CHARACTERISTICS (continued)

**FIGURE 25 — COMMON-MODE REJECTION RATIO**

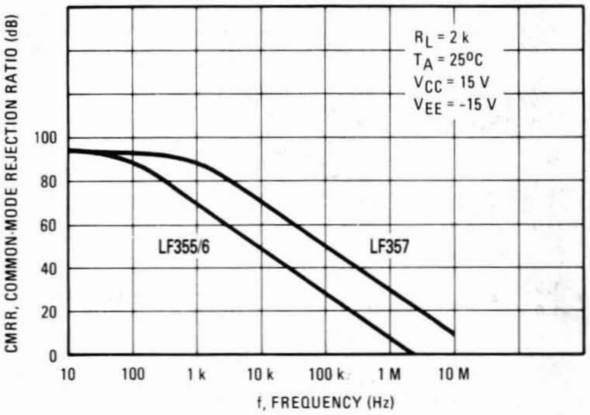
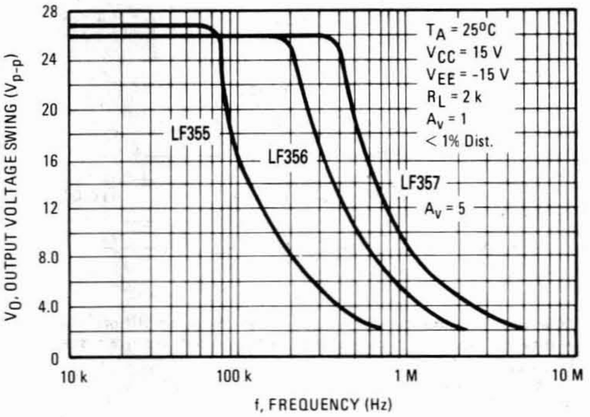


**FIGURE 26 — UNDISTORTED OUTPUT VOLTAGE SWING**



## POWER SUPPLY VOLTAGE REJECTION RATIO

**FIGURE 27 — (LF355 SERIES)**

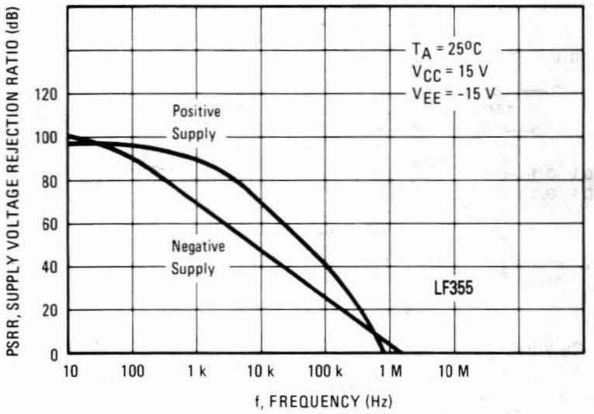
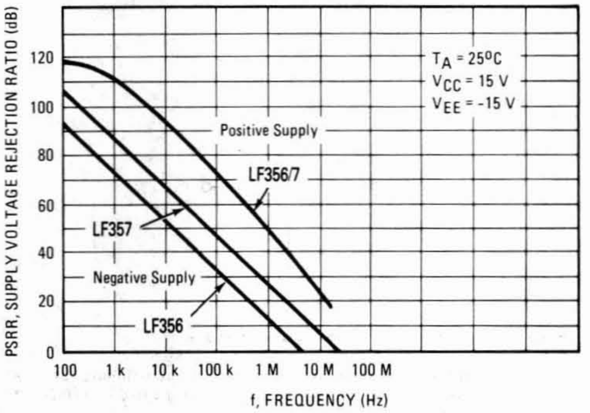


**FIGURE 28 — (LF356 AND LF357 SERIES)**



## EQUIVALENT NOISE VOLTAGE

**FIGURE 29 — (LF355/356/357 SERIES)**

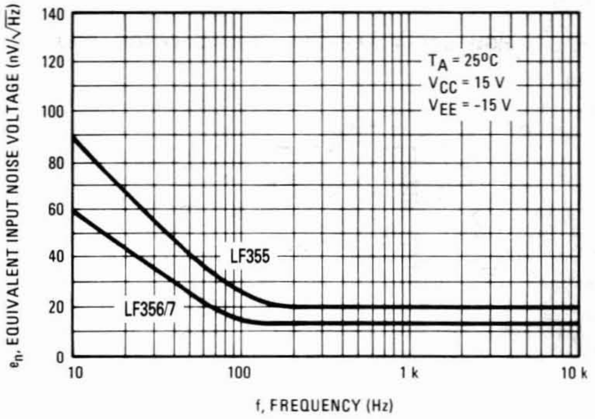
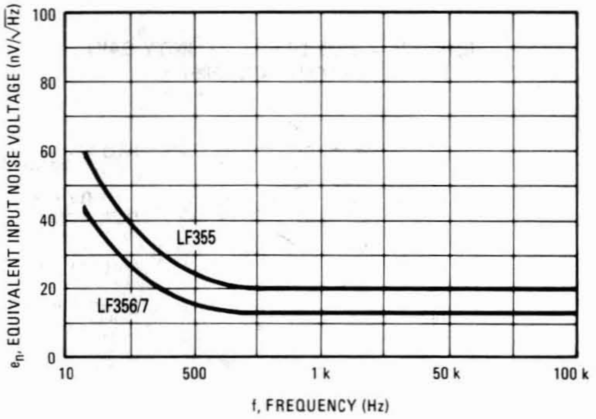
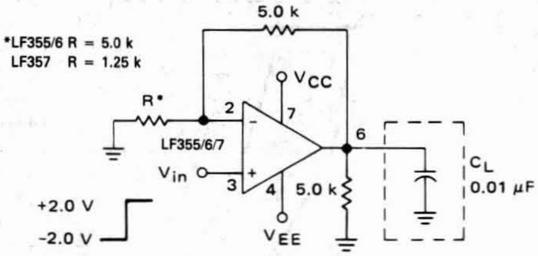


**FIGURE 30 (EXPANDED SCALE)**



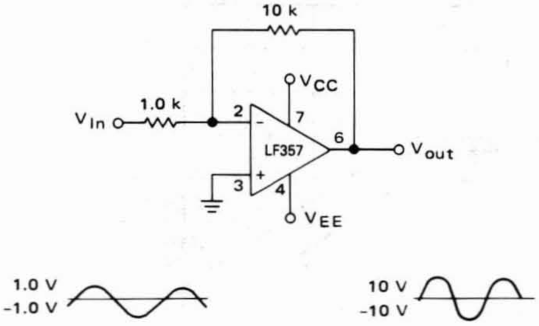
## TYPICAL CIRCUIT CONNECTIONS

### FIGURE 31 — DRIVING CAPACITIVE LOADS


*LF355/6 R = 5.0 k
LF357 R = 1.25 k
5.0 k
R*
$V_{CC}$
LF355/6/7
$V_{in}$
2
7
6
3
4
5.0 k
$C_L$
0.01 µF
+2.0 V
-2.0 V
$V_{EE}$

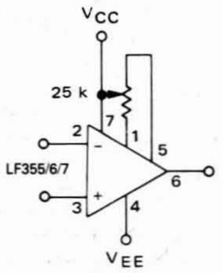
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.
$C_{L(max)} \cong 0.01\ \mu F$.
Overshoot $\leqslant$ 20%
Settling time $(t_s) \cong 5.0\ \mu s$

### FIGURE 32 — LARGE POWER BANDWIDTH AMPLIFIER


10 k
1.0 k
$V_{in}$
$V_{CC}$
2
7
6
3
4
LF357
$V_{out}$
$V_{EE}$
1.0 V
-1.0 V
10 V
-10 V

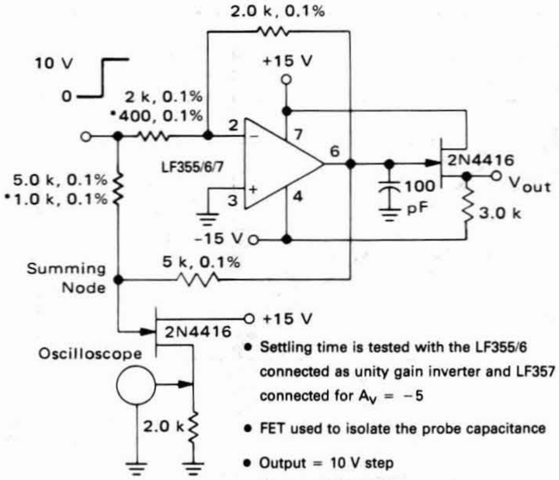
For distortion < 1% and a 20 Vp-p $V_{Out}$ swing, power bandwidth is: 500 kHz.

### FIGURE 33 — INPUT OFFSET VOLTAGE ADJUSTMENT


$V_{CC}$
25 k
7
1
5
2
6
3
4
LF355/6/7
$V_{EE}$

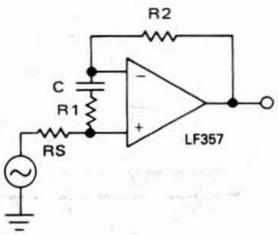
- $V_{IO}$ is adjusted with a 25 k potentiometer
- The potentiometer wiper is connected to $V_{CC}$
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 µV/°C/mV of adjustment.
- Typical overall drift: 5.0 µV/°C ±(0.5 µV/°C/mV of adjustment.)

### FIGURE 34 — SETTLING TIME TEST CIRCUIT


2.0 k, 0.1%
10 V
0
+15 V
2 k, 0.1%
*400, 0.1%
2
7
6
LF355/6/7
3
4
2N4416
100 pF
$V_{out}$
3.0 k
5.0 k, 0.1%
*1.0 k, 0.1%
-15 V
5 k, 0.1%
Summing Node
+15 V
2N4416
Oscilloscope
2.0 k

- Settling time is tested with the LF355/6 connected as unity gain inverter and LF357 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10 V step
- $^*A_V = -5$ for LF357

### FIGURE 35 — NONINVERTING UNITY GAIN OPERATION FOR LF357


R2
C
R1
RS
LF357

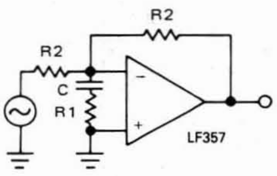
$R1C \geqslant \frac{1}{(2\pi)(5\ MHz)}$

$R1 = \frac{R2 + R_S}{4}$

$A_{V(DC)} = 1$

$f_{-3dB} \approx 5\ MHz$

### FIGURE 36 — INVERTING UNITY GAIN FOR LF357


R2
R2
C
R1
LF357

$R1C \geqslant \frac{1}{(2\pi)(5\ MHz)}$

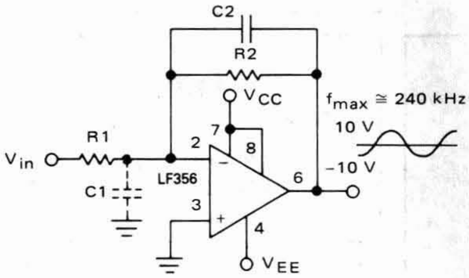
$R1 = \frac{R2}{4}$

$A_{V(DC)} = -1$

$f_{-3dB} \approx 5\ MHz$

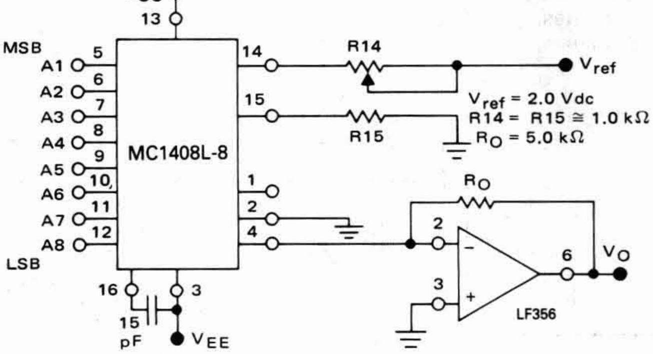
## TYPICAL APPLICATIONS

### FIGURE 37 — WIDE BW, LOW NOISE, LOW DRIFT AMPLIFIER


C2
R2
VCC
$f_{max} \cong 240$ kHz
10 V
−10 V
R1
Vin
C1
LF356
2
3
7
8
6
4
VEE

- Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \cong 240$ kHz
- Parasitic input capacitance (C1 ≅ 3 pF for LF355, LF356, and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

### FIGURE 39 — 8-BIT D/A WITH OUTPUT CURRENT TO VOLTAGE CONVERSION


VCC
13
MSB
A1
A2
A3
A4
A5
A6
A7
A8
LSB
5
6
7
8
9
10
11
12
MC1408L-8
14
15
1
2
4
16
3
15 pF
VEE
R14
R15
Vref
RO
2
3
6
VO
LF356

$V_{ref} = 2.0$ Vdc
R14 = R15 ≅ 1.0 kΩ
$R_O = 5.0$ kΩ

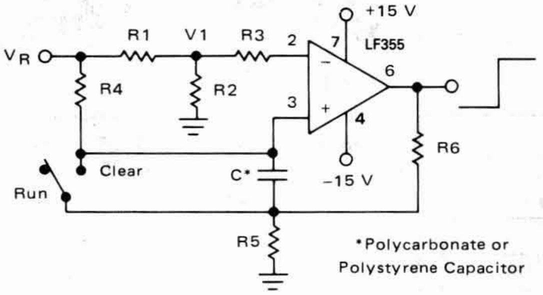
Theoretical $V_O$

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust $V_{ref}$, R14 or $R_O$ so that $V_O$ with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2V}{1\,k}(5\,k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$
$$= 10\,V\left[\frac{255}{256}\right] = 9.961\,V$$

### FIGURE 41 — LONG INTERVAL RC TIMER


+15 V
R1
V1
R3
2
7
LF355
6
VR
R4
R2
3
4
R6
Clear
Run
C*
−15 V
R5

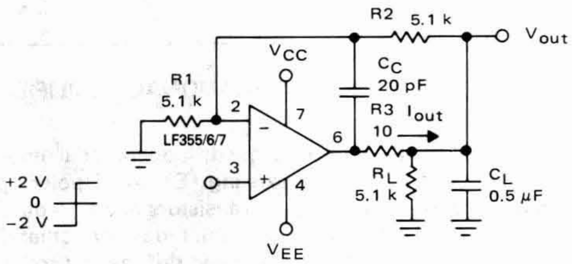
*Polycarbonate or Polystyrene Capacitor

Time (t) = R4Cℓn$(V_R/V_R - V_I)$, $R_3 = R_4$, $R_5 = 0.1$ R6
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer

| | | |
|---|---|---|
| $V_R$ = 10 V | C = 1 μF | R3 = R4 = 144 M |
| R6 = 20 k | R5 = 2 k | R1 = R2 = 1 k |

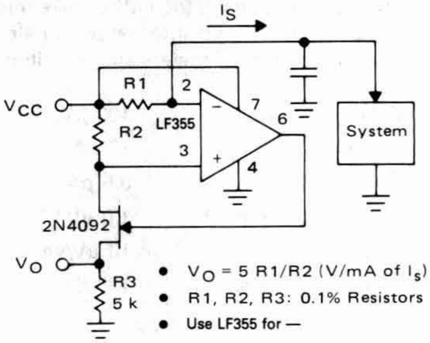
### FIGURE 38 — ISOLATING LARGE CAPACITIVE LOADS


R2 5.1 k
Vout
VCC
CC 20 pF
R1 5.1 k
2
7
R3 10
Iout
LF355/6/7
6
3
4
RL 5.1 k
CL 0.5 μF
+2 V
0
−2 V
VEE

- Overshoot 6%
- $t_s = 10$ μs
- When driving large $C_L$, the $V_{out}$ slew rate is determined by $C_L$ and $I_{out(max)}$:

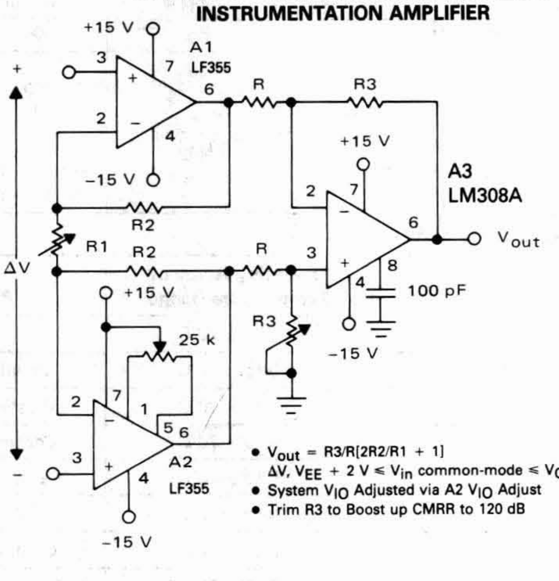
$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \cong \frac{0.02}{0.5}\ \text{V/μs} = 0.04\ \text{V/μs (with } C_L \text{ shown)}$$

### FIGURE 40 — PRECISION CURRENT MONITOR


IS
VCC
R1
2
7
6
R2
LF355
3
4
System
2N4092
VO
R3 5 k

- $V_O$ = 5 R1/R2 (V/mA of $I_s$)
- R1, R2, R3: 0.1% Resistors
- Use LF355 for —
    - ▲ Common-Mode Range to Supply Range
    - ▲ Low $I_{IB}$
    - ▲ Low $V_{IO}$
    - ▲ Low Supply Current

### FIGURE 42 — HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER


+15 V
A1
LF355
3
7
6
2
4
−15 V
R
R3
+15 V
A3
LM308A
2
7
6
3
8
Vout
100 pF
R2
R1
R2
R
R3
−15 V
ΔV
+
−
+15 V
25 k
2
7
1
5
6
3
4
A2
LF355
−15 V

- $V_{out}$ = R3/R[2R2/R1 + 1]
  ΔV, $V_{EE}$ + 2 V ≤ $V_{in}$ common-mode ≤ $V_{CC}$
- System $V_{IO}$ Adjusted via A2 $V_{IO}$ Adjust
- Trim R3 to Boost up CMRR to 120 dB

**MOTOROLA**

# LM11
# LM11C
# LM11CL

## PRECISION OPERATIONAL AMPLIFIERS

The LM11 is a precision, low drift operational amplifier providing the best features of existing FET and Bipolar op amps. Implementation of super gain transistors allows reduction of input bias currents by an order of magnitude over earlier devices such as the LM108A. Offset voltage and drift have also been reduced. Although bandwidth and slew rate are not as great as FET devices, input offset voltage, drift and bias current are inherently lower, particularly over temperature. Power consumption is also much lower, eliminating warm-up stabilization time in critical applications.

Offset balancing is provided, with the range determined by an external low resistance potentiometer. Compensation is provided internally, but external compensation can be added for improved stability when driving capacitive loads.

The precision characteristics of the LM11 make this device ideal for applications such as charge integrators, analog memories, electrometers, active filters, light meters and logarithmic amplifiers.

| | |
|---|---|
| • Low Input Offset Voltage: | 100 µV |
| • Low Input Bias Current: | 17 pA |
| • Low Input Offset Current: | 0.5 pA |
| • Low Input Offset Voltage Drift: | 1.0 µV/°C |
| • Long-Term Stability: | 10 µV/year |
| • High Common Mode Rejection: | 130 dB |

### MAXIMUM RATINGS

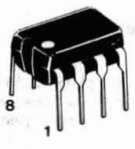
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ to $V_{EE}$ | 40 | Vdc |
| Differential Input Current (Note 1) | $I_{ID}$ | ± 10 | mA |
| Output Short-Circuit Duration (Note 2) | $t_s$ | Indefinite | |
| Power Dissipation (Note 3) | $P_D$ | 500 | mW |
| Operating Junction Temperature<br>LM11<br>LM11C/CL | $T_J$ | <br>150<br>85 | °C |
| Storage Temperature Range<br>Metal and Ceramic Packages<br>Plastic Packages | $T_{stg}$ | <br>− 65 to + 150<br>− 55 to + 125 | °C |

### ORDERING INFORMATION

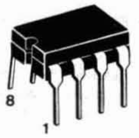
| Device | Operating Ambient Temperature Range | Package |
|---|---|---|
| LM11CD,CLD | 0 to +70°C | SO-8 |
| LM11CLN,CN | 0 to +70°C | Plastic 8-Pin DIP |
| LM11CLN-14, CN-14 | 0 to +70°C | Plastic 14-Pin DIP |
| LM11CLJ-8, CJ-8 | 0 to +70°C | Ceramic 8-Pin DIP |
| LM11CLJ, CJ | 0 to +70°C | Ceramic 14-Pin DIP |
| LM11CLH, CH | 0 to +70°C | Metal Can |
| LM11J-8 | −55 to +125°C | Ceramic 8-Pin DIP |
| LM11J | −55 to +125°C | Ceramic 14-Pin DIP |
| LM11H | −55 to +125°C | Metal Can |

## PRECISION OPERATIONAL AMPLIFIERS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

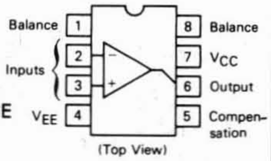


**N SUFFIX**
PLASTIC PACKAGE
CASE 626-04

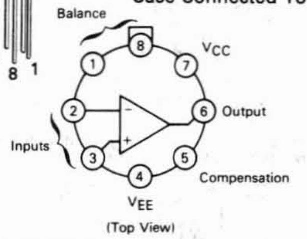


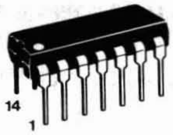
**J-8 SUFFIX**
CERAMIC PACKAGE
CASE 693-02

**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8

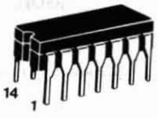


**H SUFFIX**
METAL CAN
CASE 601-04
Case Connected To $V_{EE}$

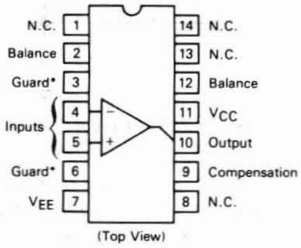




**N-14 SUFFIX**
PLASTIC PACKAGE
CASE 646-05



**J SUFFIX**
CERAMIC PACKAGE
CASE 632-02



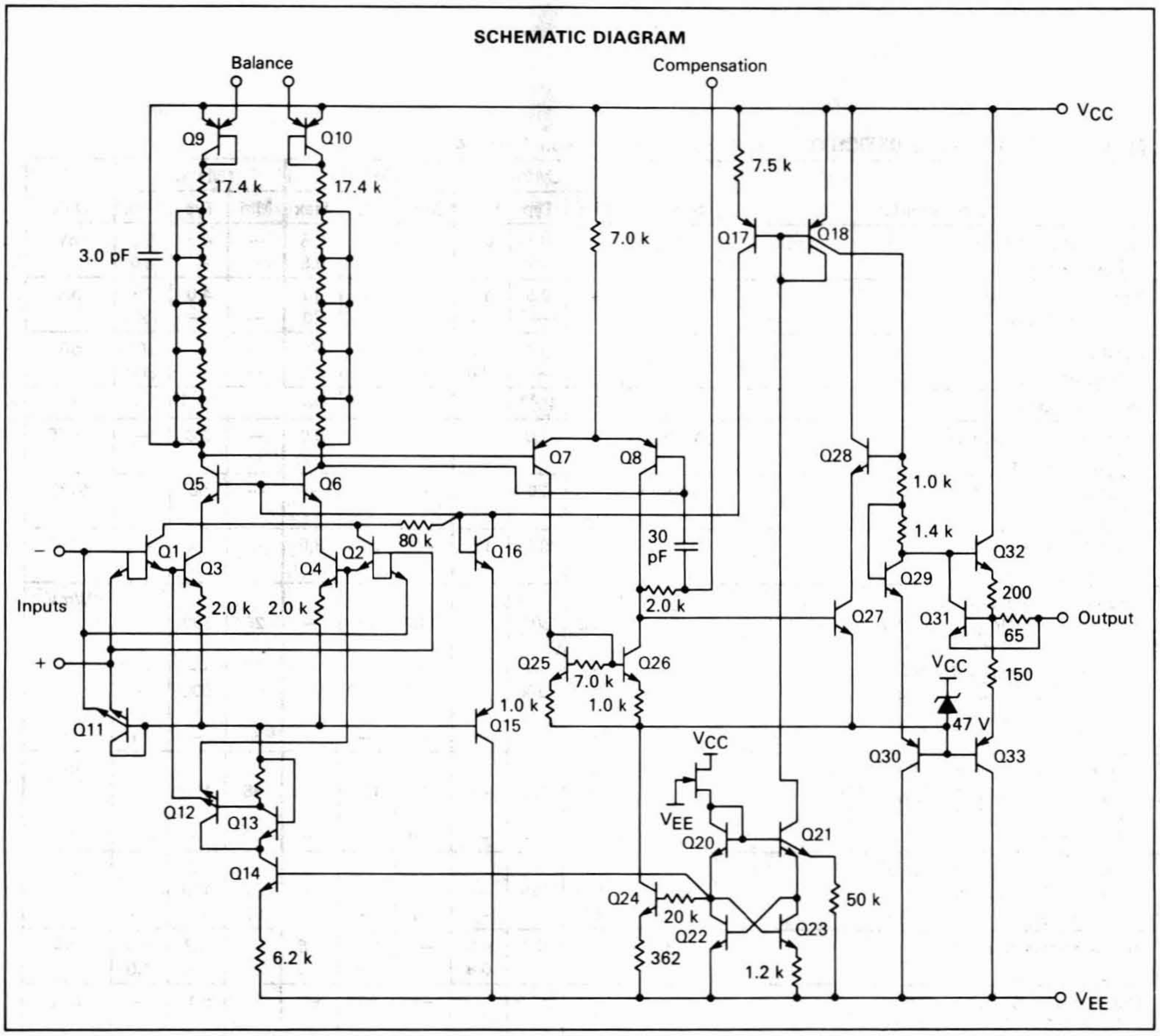
*Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted [Note 4])

| Characteristics | Symbol | LM11 | | | LM11C | | | LM11CL | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{IO}$ | — | 0.1 | 0.3 | — | 0.2 | 0.6 | — | 0.5 | 5.0 | mV |
| $T_{low}$ to $T_{high}$ | | — | — | 0.6 | — | — | 0.8 | — | — | 6.0 | |
| Input Offset Current | $I_{IO}$ | — | 0.5 | 10 | — | 1.0 | 10 | — | 4.0 | 25 | pA |
| $T_{low}$ to $T_{high}$ | | — | — | 30 | — | — | 20 | — | — | 50 | |
| Input Bias Current | $I_{IB}$ | — | 17 | 50 | — | 17 | 100 | — | 17 | 200 | pA |
| $T_{low}$ to $T_{high}$ | | — | — | 150 | — | — | 150 | — | — | 300 | |
| Input Resistance | $r_i$ | — | $10^{11}$ | — | — | $10^{11}$ | — | — | $10^{11}$ | — | Ω |
| Input Offset Voltage Drift<br>$T_{low}$ to $T_{high}$ | $\Delta V_{IO}/\Delta T$ | — | 1.0 | 3.0 | — | 2.0 | 5.0 | — | 3.0 | — | μV/°C |
| Input Offset Current Drift<br>$T_{low}$ to $T_{high}$ | $\Delta I_{IO}/\Delta T$ | — | 20 | — | — | 10 | — | — | 50 | — | fA/°C |
| Input Bias Current Drift<br>$T_{low}$ to $T_{high}$ | $\Delta I_{IB}/\Delta T$ | — | 0.5 | 1.5 | — | 0.8 | 3.0 | — | 1.4 | — | pA/°C |
| Large Signal Voltage Gain | $A_{VOL}$ | | | | | | | | | | V/mV |
| $V_S$ = ±15 V, $V_{out}$ = ±12 V, $I_{out}$ = ±2.0 mA | | 100 | 300 | — | 100 | 300 | — | 25 | 300 | — | |
| $T_{low}$ to $T_{high}$ (Note 5) | | 50 | — | — | 50 | — | — | 15 | — | — | |
| $V_S$ = ±15 V, $V_{out}$ = ±12 V, $I_{out}$ = ±0.5 mA | | 250 | 1200 | — | 250 | 1200 | — | 50 | 800 | — | |
| $T_{low}$ to $T_{high}$ | | 100 | — | — | 100 | — | — | 30 | — | m | |
| Common Mode Rejection Ratio | CMRR | | | | | | | | | | dB |
| $V_S$ = ±15 V, $-13\ V \leq V_{CM} \leq 14$ V | | 110 | 130 | — | 110 | 130 | — | 96 | 110 | — | |
| $V_S$ = ±15 V, $-12.5\ V \leq V_{CM} \leq 14$ V, $T_{low}$ to $T_{high}$ | | 100 | — | — | 100 | — | — | 90 | — | — | |
| Power Supply Rejection Ratio | PSRR | | | | | | | | | | dB |
| $\pm 2.5\ V \leq V_S \leq \pm 20$ V | | 100 | 118 | — | 100 | 118 | — | 84 | 100 | — | |
| $T_{low}$ to $t_{high}$ | | 96 | — | — | 96 | — | — | 80 | — | — | |
| Power Supply Current | $I_D$ | — | 0.3 | 0.6 | — | 0.3 | 0.8 | — | 0.3 | 0.8 | mA |
| $T_{low}$ to $T_{high}$ | | — | — | 0.8 | — | — | 1.0 | — | — | 1.0 | |
| Output Short-Circuit Current<br>$T_J$ = 150°C, Output Shorted to Ground | $I_{os}$ | — | ±10 | — | — | ±10 | — | — | ±10 | — | mA |

Notes:

1. The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow if the input differential voltage is in excess of 1.0 V if no limiting resistance is used. Additionally, a 2 kΩ resistance in each input is suggested to prevent possible latch-up initiated by supply reversals.
2. The output is current limited when shorted to ground or any voltages less than the supplies. Continuous overloads will require package dissipation to be considered and heat sinking should be provided when necessary.
3. Devices must be derated based on package thermal resistance (see package outline dimensions).
4. These specifications apply for $V_{EE} + 2.0\ V \leq V_{CM} \leq V_{CC} - 1.0$ V ($V_{EE} + 2.5\ V \leq V_{CM} \leq V_{CC} - 1.0$ V for $T_{low}$ to $T_{high}$) and $\pm 2.5\ V \leq V_S \leq \pm 20$ V
   $T_{low}$ to $T_{high}$: $-55°C \leq T_J \leq +125°C$ for LM11
   $0°C \leq T_J \leq +70°C$ for LM11C and LM11CL
5. $V_{out}$ = ±11.5 V, all other conditions unchanged.



SCHEMATIC DIAGRAM

Balance
Compensation
VCC
Q9
Q10
17.4 k
17.4 k
3.0 pF
7.0 k
7.5 k
Q17
Q18
Q7
Q8
Q28
1.0 k
1.4 k
Q5
Q6
80 k
Q16
30 pF
Q32
Q1
Q2
Q3
Q4
Q29
200
Inputs
2.0 k
2.0 k
2.0 k
Q27
Q31
Output
65
Q25
Q26
7.0 k
VCC
150
1.0 k
1.0 k
47 V
Q11
Q15
VCC
Q30
Q33
VEE
Q12
Q13
Q20
Q21
Q14
Q24
20 k
50 k
Q22
Q23
6.2 k
362
1.2 k
VEE

**FIGURE 1 — INPUT BIAS CURRENT versus CASE TEMPERATURE**

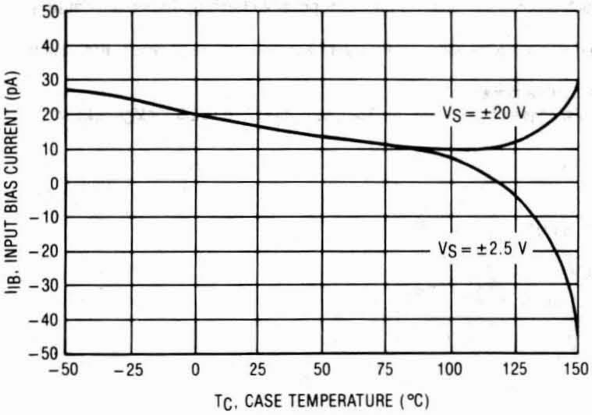


**FIGURE 2 — INPUT OFFSET CURRENT versus CASE TEMPERATURE**

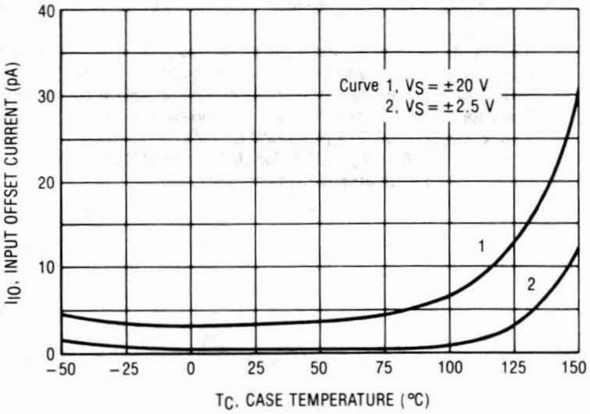


**FIGURE 3 — TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE versus INPUT OFFSET VOLTAGE**

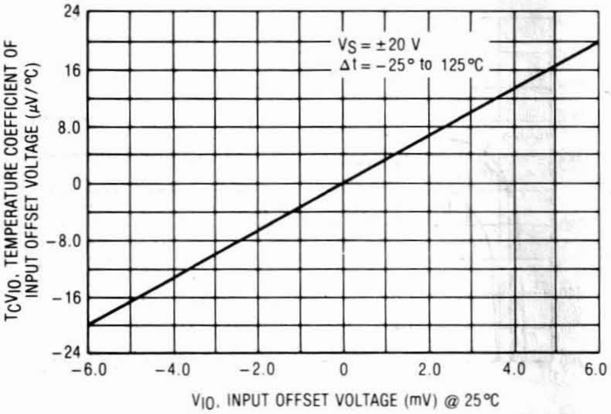


**FIGURE 4 — SPECTRAL NOISE DENSITY**

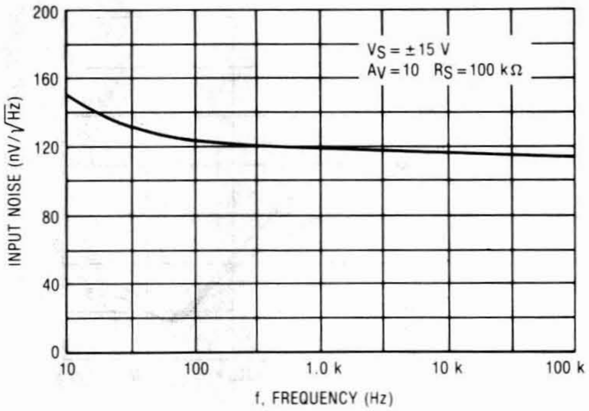


**FIGURE 5 — COMMON-MODE LIMITS versus TEMPERATURE**

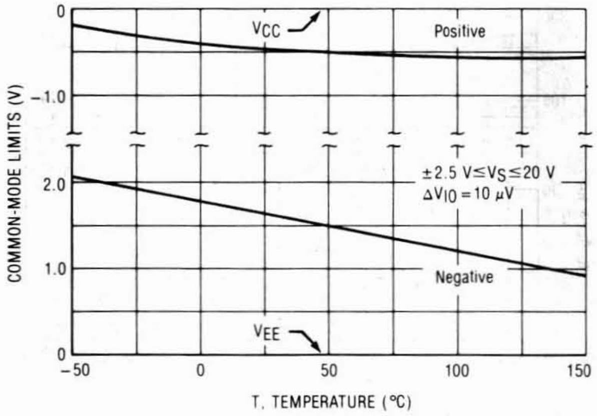


**FIGURE 6 — COMMON-MODE REJECTION AND SLEW LIMIT versus FREQUENCY**

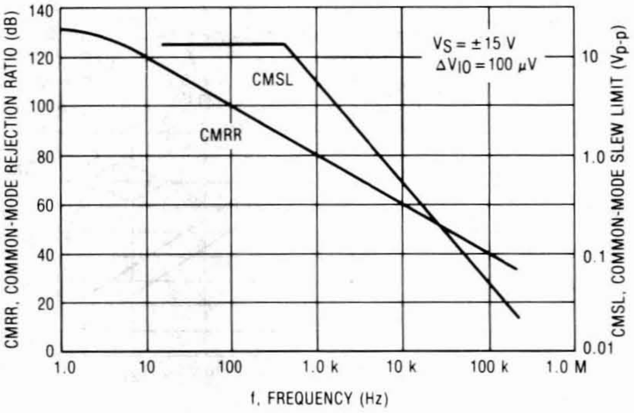


**FIGURE 7 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE**

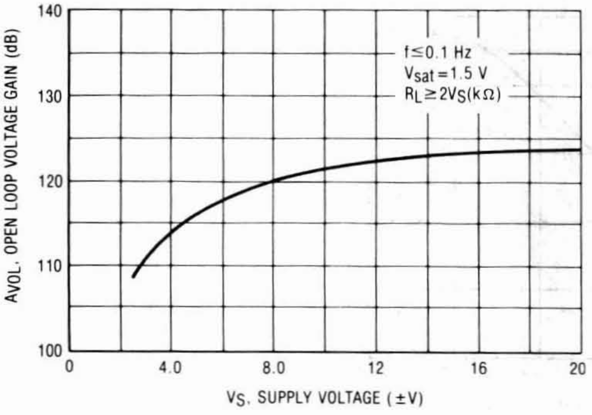


**FIGURE 8 — OUTPUT SATURATION versus LOAD CURRENT**

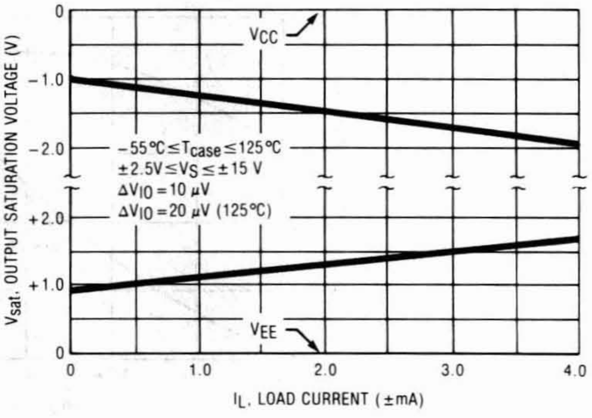


FIGURE 9 — POWER SUPPLY REJECTION RATIO versus FREQUENCY

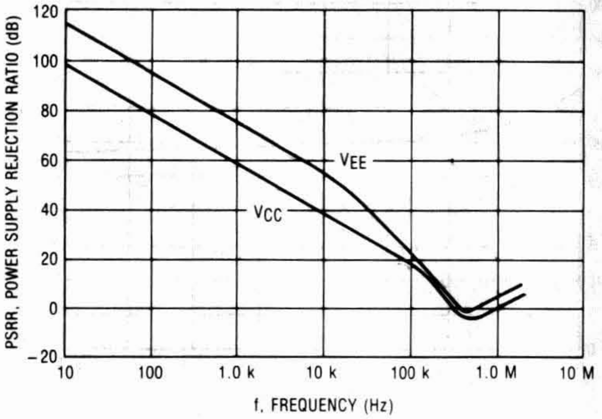


FIGURE 10 — SUPPLY CURRENT versus SUPPLY VOLTAGE

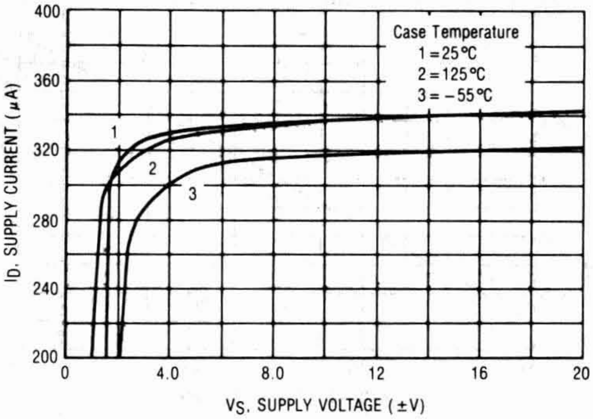


FIGURE 11 — OPEN LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

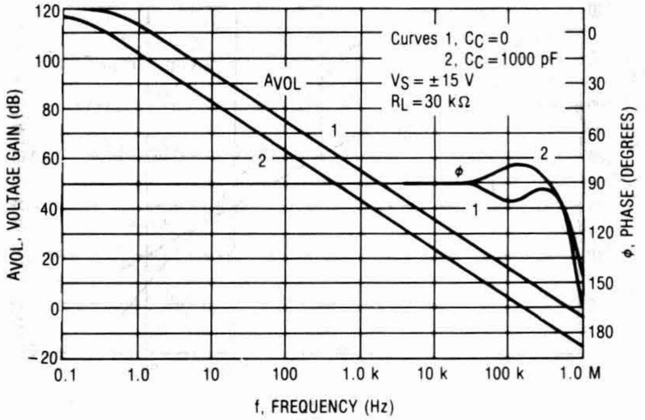


FIGURE 12 — SLEW RATE versus EXTERNAL COMPENSATION CAPACITOR

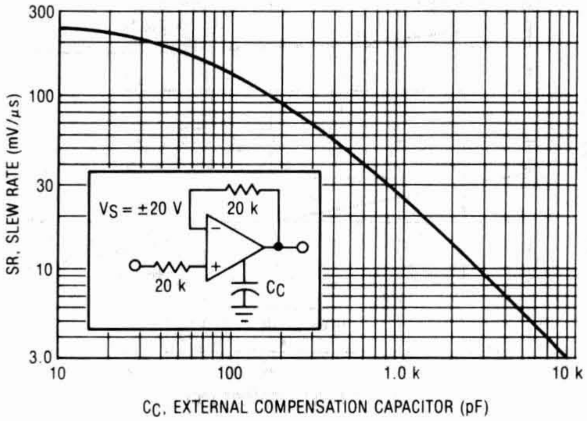
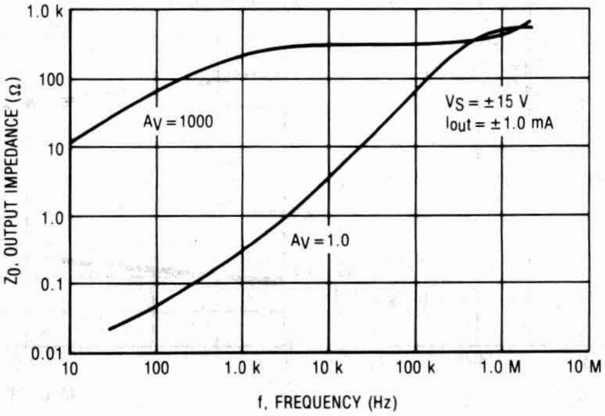


FIGURE 13 — CLOSED LOOP OUTPUT IMPEDANCE versus FREQUENCY



## APPLICATIONS INFORMATION

Due to the extremely low input bias currents of this device, it may be tempting to remove the bias current compensation resistor normally associated with a summing amplifier configuration. Direct connection of the inputs to a low impedance source or ground should be avoided when supply voltages greater than approximately 3 volts are used. The potential problem involves reversal of one supply which can cause excessive current to flow in the second supply. Possible destruction of the IC could result if the second supply is not current limited to approximately 100 mA or if bypass capacitors greater than 1.0 μF are used in the supply bus.

Disconnecting one supply will generally cause reversal due to loading of the other supply within the IC and in external circuitry. Although the problem can usually be avoided by placing clamp diodes across the power supplies of each printed circuit board, a careful design will include sufficient resistance in the input leads to limit the current to 10 mA if the input leads are pulled to either supply by internal currents. This precaution is not limited to only the LM11.

The LM11 is capable of resolving picoampere level signals. Leakage currents external to the IC can severely impair the performance of the device. It is important that high quality insulating materials such as teflon be employed. Proper cleaning to remove fluxes and other residues from printed circuit boards, sockets and the device package are necessary to minimize surface leakage.

When operating in high humidity environments or temperatures near 0°C, a surface coating is suggested to set up a moisture barrier.

Leakage effects on printed circuit boards can be reduced by encircling the inputs (both sides of p.c. board) with a conductive guard ring connected to a low impedance potential nearly the same as that of the inputs.

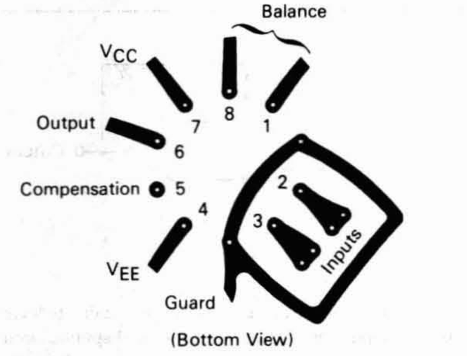
The suggested printed circuit board layout for input guarding is shown in Figure 14. Guard ring electrical connections for common operational amplifier configurations are illustrated in Figure 15. For critical applications, a 14-pin dual in-line package is available with guard pins (internally unconnected) adjacent to the inputs for minimal package leakage effects.

Electrostatic shielding is suggested in high-impedance circuits.

Error voltages in external circuitry can be generated by thermocouple effects. Dissimilar metals along with temperature gradients can set up an error voltage ranging in the hundreds of microvolts. Some of the best thermocouples are junctions of dissimilar metals made up of IC package pins and printed circuit boards. Problems can be avoided by keeping low level circuitry away from heat generating elements.

The LM11 is internally compensated, but external compensation can be added to improve stability, particularly when driving capacitive loads.

FIGURE 14 — SUGGESTED PRINTED CIRCUIT BOARD LAYOUT FOR INPUT GUARDING USING METAL PACKAGED DEVICE



The above guard ring, required on both sides of the board, is connected to a low impedance point of the same potential as the sensitive inputs to reduce surface leakage paths. Bulk leakage is reduced less, and depends more on guard ring width.

FIGURE 15 — GUARD RING ELECTRICAL CONNECTIONS FOR COMMON AMPLIFIER CONFIGURATIONS

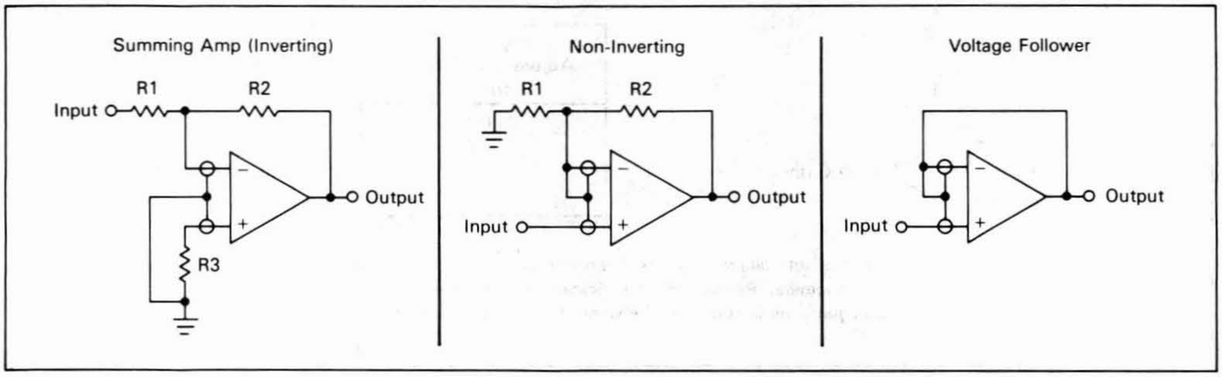
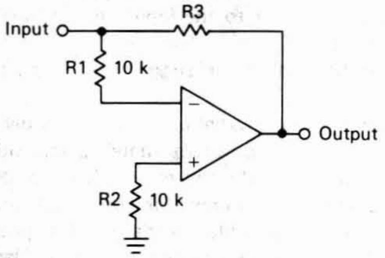
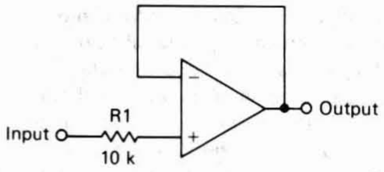


FIGURE 16 — INPUT PROTECTION FOR SUMMING (INVERTING) AMPLIFIER



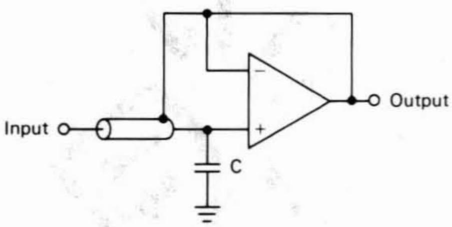
Current is limited by R1 in the event the input is connected to a low impedance source outside the common-mode range of the device. Current is controlled by R2 if one supply reverses. R1 and R2 do not affect normal operation.

FIGURE 17 — INPUT PROTECTION FOR A VOLTAGE FOLLOWER

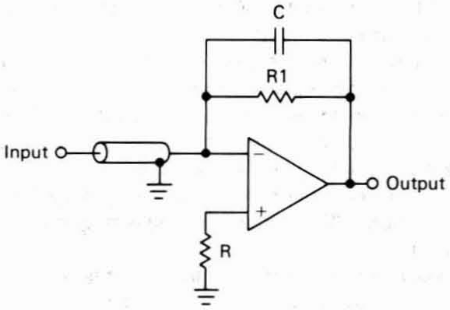


Input current is limited by R1 when the input exceeds supply voltage, power supply is turned off, or output is shorted.

FIGURE 18 — CABLE BOOT STRAPPING AND INPUT SHIELDS

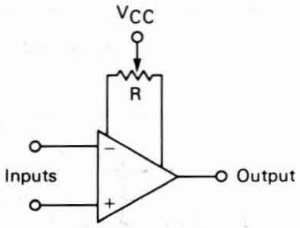


An input shield boot strapped in a voltage follower reduces input capacitance, leakage, and spurious voltages from cable flexing. A small capacitor from the input to ground will prevent any instability.



In a summing amplifier the input is at virtual ground. Therefore the shield can be grounded. A small feedback capacitor will insure stability.

FIGURE 19 — ADJUSTING INPUT OFFSET VOLTAGE WITH BALANCE POTENTIOMETER



| Minimum Adjustment Range (mV) | R Ω |
|---|---|
| ±0.4 | 1.0 k |
| ±1.0 | 3.0 k |
| ±2.0 | 10 k |
| ±5.0 | 100 k |

Input offset voltage adjustment range is a function of the Balance Potentiometer Resistance as indicated by the table above. The potentiometer is connected between the two "Balance" pins.

**MOTOROLA**

# LM101A
# LM201A
# LM301A

## OPERATIONAL AMPLIFIER

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to 10 V/μs can be obtained.

- Low Input Offset Current — 20 nA maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short-Circuit Protection
- Guaranteed Drift Characteristics

**FIGURE 1 – STANDARD COMPENSATION AND OFFSET BALANCING CIRCUIT**

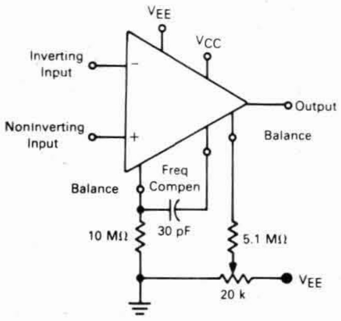
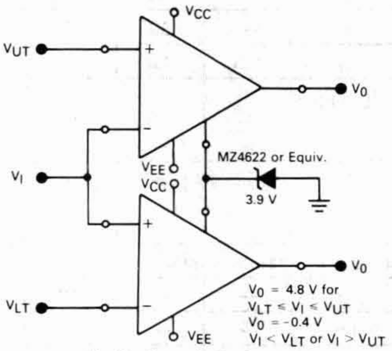
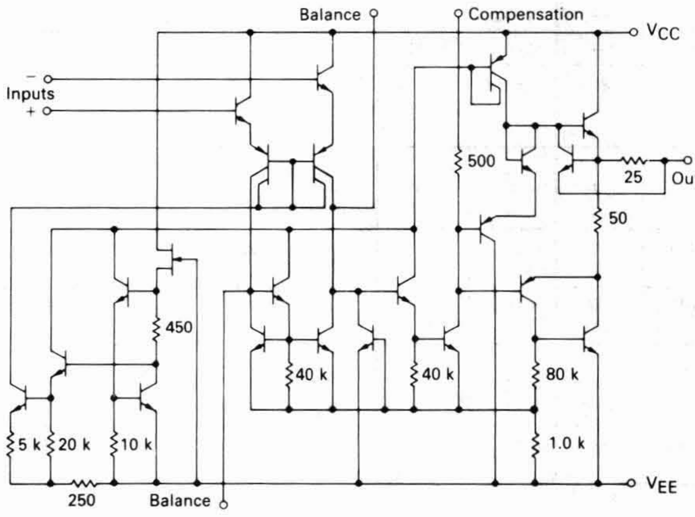

VEE
VCC
Inverting Input
Noninverting Input
Output
Balance
Freq Compen
Balance
30 pF
10 MΩ
5.1 MΩ
20 k
VEE

**FIGURE 2 – DOUBLE-ENDED LIMIT DETECTOR**


VCC
VUT
VO
VEE
VCC
MZ4622 or Equiv.
3.9 V
VI
VO
VLT
VEE
$V_O$ = 4.8 V for
$V_{LT} \le V_I \le V_{UT}$
$V_O$ = −0.4 V
$V_I < V_{LT}$ or $V_I > V_{UT}$

Pins Not Shown Are Not Connected

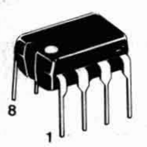
**FIGURE 3 – REPRESENTATIVE CIRCUIT SCHEMATIC**


Balance
Compensation
VCC
− Inputs +
500
25
Output
50
450
40 k
40 k
80 k
5 k
20 k
10 k
1.0 k
250
Balance
VEE

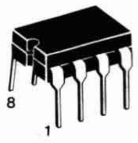
## OPERATIONAL AMPLIFIER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

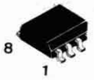
**N SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(LM201A and LM301A)

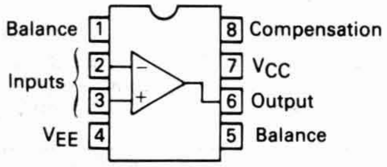


**J SUFFIX**
CERAMIC PACKAGE
CASE 693-02



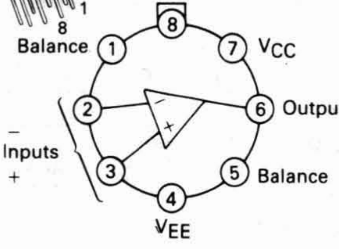
**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8




Balance 1
Inputs 2 −
3 +
VEE 4
8 Compensation
7 VCC
6 Output
5 Balance

(Top View)

**H SUFFIX**
METAL PACKAGE
CASE 601-04


Compensation
8
1
8
Balance 1
7 VCC
2
6 Output
− Inputs +
3
5 Balance
4
VEE

(Top View)

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| LM101AH | −55°C to +125°C | Metal Can |
| LM101AJ | −55°C to +125°C | Ceramic DIP |
| LM201AD | −25°C to +85°C | SO-8 |
| LM201AH | −25°C to +85°C | Metal Can |
| LM201AN | −25°C to +85°C | Plastic DIP |
| LM201AJ | −25°C to +85°C | Ceramic Dip |
| LM301AD | 0°C to +70°C | SO-8 |
| LM301AH | 0°C to +70°C | Metal Can |
| LM301AN | 0°C to +70°C | Plastic DIP |
| LM301AJ | 0°C to +70°C | Ceramic Dip |

## MAXIMUM RATINGS

<table>
<tr><th rowspan="2">Rating</th><th rowspan="2">Symbol</th><th colspan="3">VALUE</th><th rowspan="2">Unit</th></tr>
<tr><th>LM101A</th><th>LM201A</th><th>LM301A</th></tr>
<tr><td>Power Supply Voltage</td><td>$V_{CC}$, $V_{EE}$</td><td>±22</td><td>±22</td><td>±18</td><td>Vdc</td></tr>
<tr><td>Input Differential Voltage</td><td>$V_{ID}$</td><td colspan="3">← ±30 →</td><td>Volts</td></tr>
<tr><td>Input Common-Mode Range (Note 1)</td><td>$V_{ICR}$</td><td colspan="3">← ±15 →</td><td>Volts</td></tr>
<tr><td>Output Short-Circuit Duration</td><td>$t_S$</td><td colspan="3">← Continuous →</td><td></td></tr>
<tr><td>Power Dissipation (Package Limitation)</td><td>$P_D$</td><td></td><td></td><td></td><td></td></tr>
<tr><td>Metal Can</td><td></td><td colspan="3">← 500 →</td><td>mW</td></tr>
<tr><td>Derate above $T_A$ = +75°C</td><td></td><td colspan="3">← 6.8 →</td><td>mW/°C</td></tr>
<tr><td>Plastic Dual In-Line Package (LM201A/301A)</td><td></td><td>—</td><td>625</td><td>625</td><td>mW</td></tr>
<tr><td>Derate above $T_A$ = + 25°C</td><td></td><td>—</td><td>5.0</td><td>5.0</td><td>mW/°C</td></tr>
<tr><td>Ceramic Package</td><td></td><td colspan="3">← 750 →</td><td>mW</td></tr>
<tr><td>Derate above 25°C</td><td></td><td colspan="3">← 6.6 →</td><td>mW/°C</td></tr>
<tr><td>Operating Ambient Temperature Range</td><td>$T_A$</td><td>−55 to +125</td><td>−25 to +85</td><td>0 to +70</td><td>°C</td></tr>
<tr><td>Storage Temperature Range</td><td>$T_{stg}$</td><td colspan="3">← −65 to +150 →</td><td>°C</td></tr>
</table>

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = +25°C unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the LM101A and LM201A, and from ±5.0 V to ±15 V for the LM301A.

| Characteristics | Symbol | LM101A LM201A Min | LM101A LM201A Typ | LM101A LM201A Max | LM301A Min | LM301A Typ | LM301A Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage ($R_S \leq 50$ kΩ) | $V_{IO}$ | — | 0.7 | 2.0 | — | 2.0 | 7.5 | mV |
| Input Offset Current | $I_{IO}$ | — | 1.5 | 10 | — | 3.0 | 50 | nA |
| Input Bias Current | $I_{IB}$ | — | 30 | 75 | — | 70 | 250 | nA |
| Input Resistance | $r_i$ | 1.5 | 4.0 | — | 0.5 | 2.0 | — | Megohms |
| Supply Current | $I_{CC}$, $I_{EE}$ | | | | | | | mA |
| $V_{CC}/V_{EE}$ = ±20 V | | — | 1.8 | 3.0 | — | — | — | |
| $V_{CC}/V_{EE}$ = ±15 V | | — | — | — | — | 1.8 | 3.0 | |
| Large Signal Voltage Gain ($V_{CC}/V_{EE}$ = ± 15 V, $V_O$ = ±10 V, $R_L > 2.0$ kΩ) | $A_V$ | 50 | 160 | — | 25 | 160 | — | V/mV |

The following specifications apply over the operating temperature range.

| Characteristics | Symbol | LM101A LM201A Min | LM101A LM201A Typ | LM101A LM201A Max | LM301A Min | LM301A Typ | LM301A Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage ($R_S \leq 50$ kΩ) | $V_{IO}$ | — | — | 3.0 | — | — | 10 | mV |
| Input Offset Current | $I_{IO}$ | — | — | 20 | — | — | 70 | nA |
| Average Temperature Coefficient of Input Offset Voltage $T_A(min) \leq T_A \leq T_A(max)$ | $\Delta V_{IO}/\Delta T$ | — | 3.0 | 15 | — | 6.0 | 30 | µV/°C |
| Average Temperature Coefficient of Input Offset Current | $\Delta I_{IO}/\Delta T$ | | | | | | | nA/°C |
| +25°C ≤ $T_A$ ≤ $T_A(max)$ | | — | 0.01 | 0.1 | — | 0.01 | 0.3 | |
| $T_{A(min)} \leq T_A \leq 25$°C | | — | 0.02 | 0.2 | — | 0.02 | 0.6 | |
| Input Bias Current | $I_{IB}$ | — | — | 100 | — | — | 300 | nA |
| Large Signal Voltage Gain ($V_{CC}/V_{EE}$ = ±15 V, $V_O$ = ± 10 V, $R_L > 2.0$ kΩ) | $A_V$ | 25 | — | — | 15 | — | — | V/mV |
| Input Voltage Range | $V_I$ | | | | | | | V |
| $V_{CC}/V_{EE}$ = ±20 V | | ±15 | — | — | — | — | — | |
| $V_{CC}/V_{EE}$ = ±15 V | | — | — | — | ±12 | — | — | |
| Common-Mode Rejection Ratio $R_S \leq 50$ kΩ | CMRR | 80 | 96 | — | 70 | 90 | — | dB |
| Supply Voltage Rejection Ratio $R_S \leq 50$ kΩ | PSRR | 80 | 96 | — | 70 | 96 | — | dB |
| Output Voltage Swing | $V_O$ | | | | | | | V |
| $V_{CC}/V_{EE}$ = ±15 V, $R_L$ = 10 kΩ, | | ±12 | ±14 | — | ±12 | ±14 | — | |
| $R_L$ = 2.0 kΩ | | ±10 | ±13 | — | ±10 | ±13 | — | |
| Supply Currents ($T_A$ = $T_A$(max), $V_{CC}/V_{EE}$ = ±20 V) | $I_{CC}$, $I_{EE}$ | — | 1.2 | 2.5 | — | — | — | mA |

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = + 25°C unless otherwise noted.)

**FIGURE 4 — MINIMUM INPUT VOLTAGE RANGE**

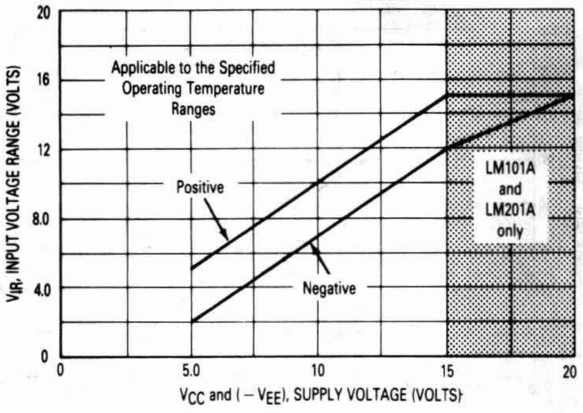


**FIGURE 5 — MINIMUM OUTPUT VOLTAGE SWING**

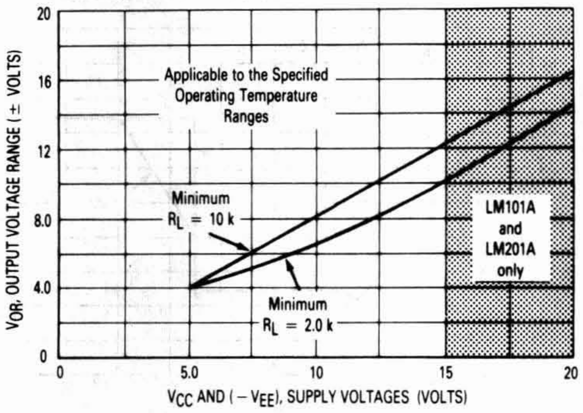


**FIGURE 6 — MINIMUM VOLTAGE GAIN**

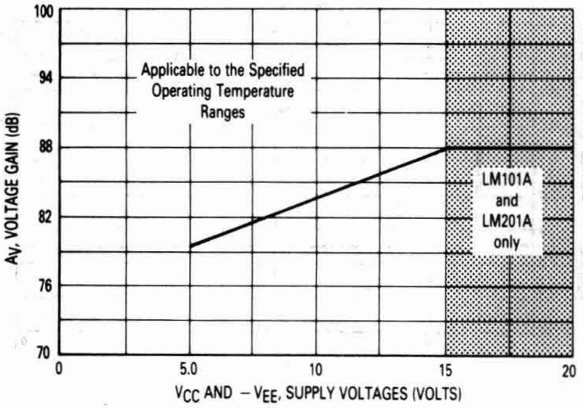


**FIGURE 7 — TYPICAL SUPPLY CURRENTS**

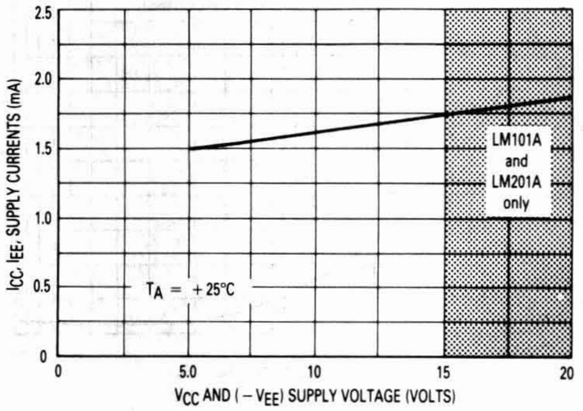


**FIGURE 8 — OPEN-LOOP FREQUENCY RESPONSE**

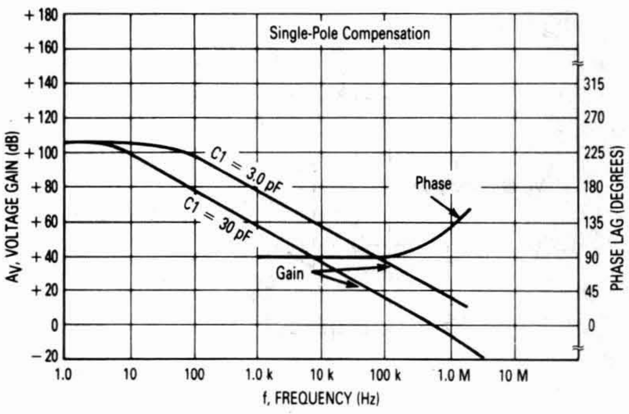
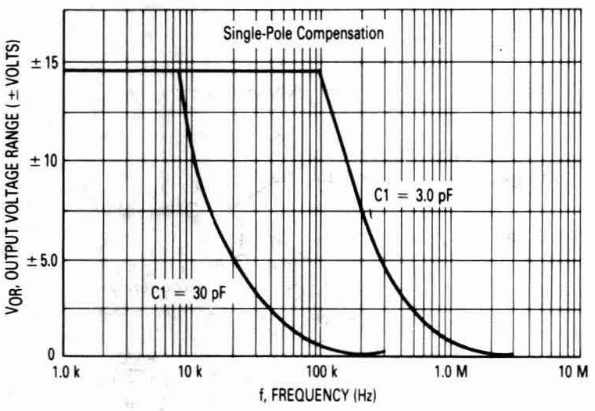


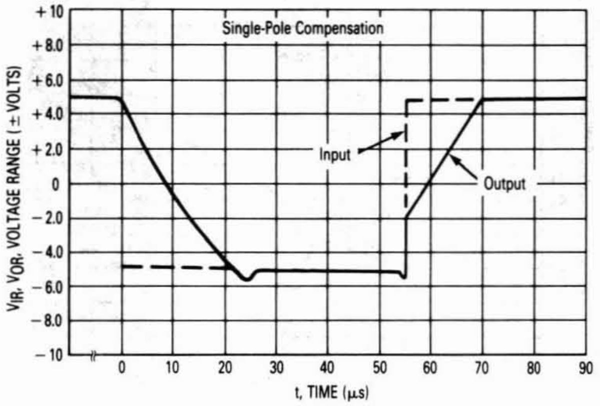
**FIGURE 9 — LARGE-SIGNAL FREQUENCY RESPONSE**



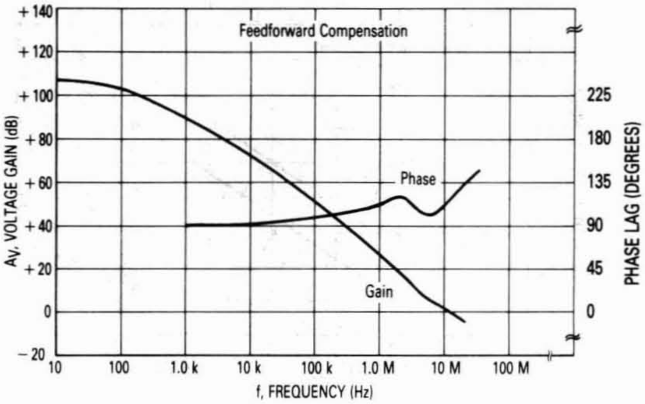
## TYPICAL CHARACTERISTICS (continued)

($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C unless otherwise noted.)

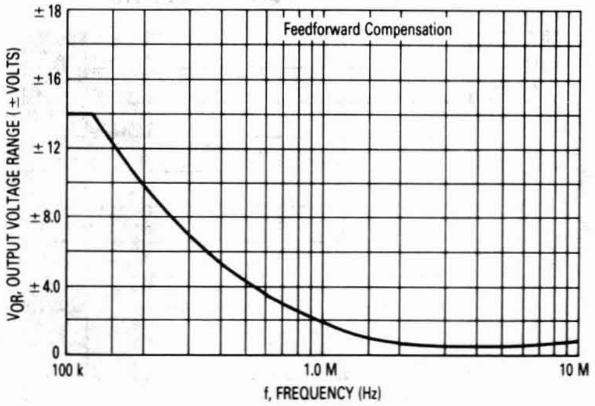
### FIGURE 10 — VOLTAGE FOLLOWER PULSE RESPONSE



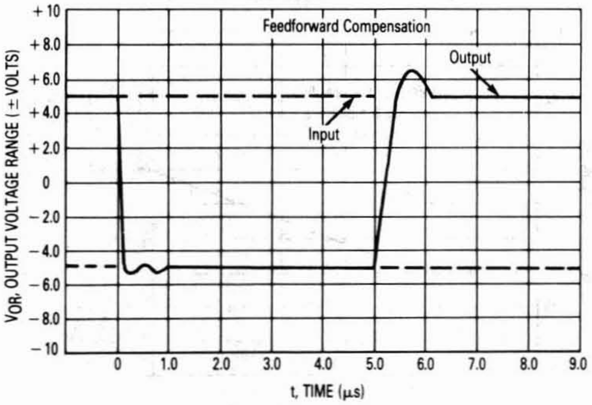
### FIGURE 11 — OPEN-LOOP FREQUENCY RESPONSE



### FIGURE 12 — LARGE-SIGNAL FREQUENCY RESPONSE

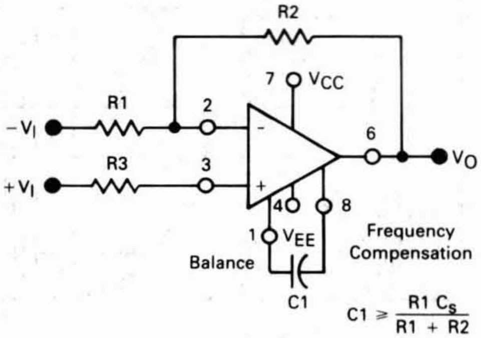


### FIGURE 13 — INVERTER PULSE RESPONSE



## TYPICAL COMPENSATION CIRCUITS

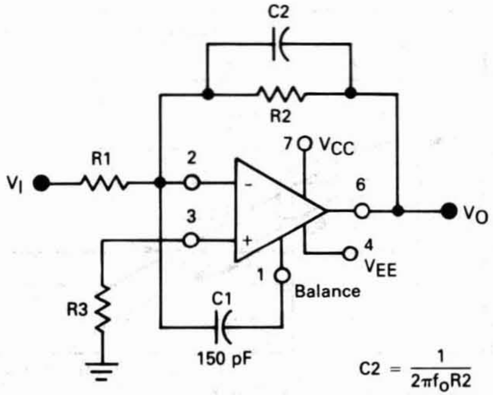
### FIGURE 14 — SINGLE-POLE COMPENSATON


R2
7
VCC
R1
2
−VI
R3
3
+VI
6
VO
4
8
1
VEE
Balance
Frequency Compensation
C1

$C1 \geq \frac{R1\ C_s}{R1 + R2}$

Cs = 30 pF

### FIGURE 15 — FEEDFORWARD COMPENSATION


C2
R2
7
VCC
R1
2
VI
3
6
VO
4
VEE
1
Balance
R3
C1
150 pF

$C2 = \frac{1}{2\pi f_o R2}$

$f_o$ = 3.0 MHz

# LM108, LM108A
# LM208, LM208A
# LM308, LM308A

## SUPER GAIN OPERATIONAL AMPLIFIERS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

## PRECISION OPERATIONAL AMPLIFIERS

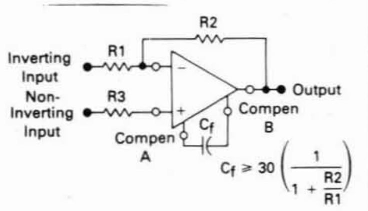
The LM108/LM208/LM308 Series operational amplifiers provide high input impedance, low input offsets and temperature drifts, and low noise. These characteristics are made possible by use of a special Super Beta processing technology. This series of amplifiers is particularly useful for applications where high-accuracy and low-drift performance are essential. In addition high-speed performance may be improved by employing feed-forward compensation techniques to maximize slew rate without compromising other performance criteria.

The LM108A/LM208A/LM308A Series offers extremely low input offset voltage and drift specifications allowing usage in even the most critical applications without external offset nulling.

- Operation From a Wide Range of Power Supply Voltages
- Low Input Bias and Offset Currents
- Low Input Offset Voltage and Guaranteed Offset Voltage Drift Performance
- High Input Impedance

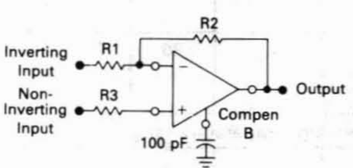
## FREQUENCY COMPENSATION

**Standard Compensation**

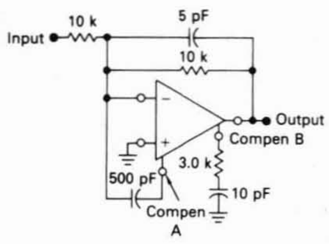

R2
R1
Inverting Input
Non-Inverting Input
R3
Output
Compen B
Cf
Compen A

$C_f \geq 30 \left( \frac{1}{1 + \frac{R2}{R1}} \right)$

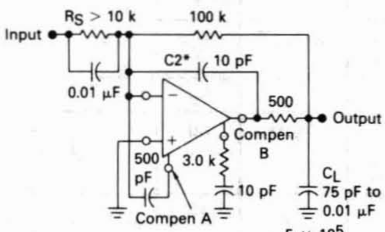
**Modified Compensation**


R2
R1
Inverting Input
Non-Inverting Input
R3
Output
Compen B
100 pF

**Standard Feedforward Compensation**


10 k
Input
5 pF
10 k
Output
Compen B
3.0 k
500 pF
10 pF
Compen A

**Feedforward Compensations for Decoupling Load Capacitance**

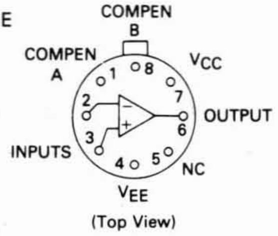

RS > 10 k
100 k
Input
C2*
10 pF
0.01 µF
500
Output
Compen B
500 pF
3.0 k
10 pF
CL
75 pF to 0.01 µF
Compen A

$*C2 > \frac{5 \times 10^5}{R2}$ pF

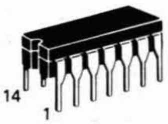
**ORDERING INFORMATION**

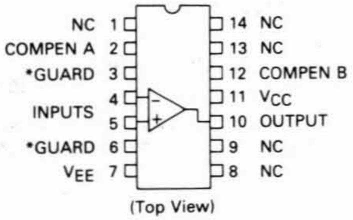
| Device | Temperature Range | Package |
|---|---|---|
| LM108AH, H | −55 to +125°C | Metal Can |
| LM108AJ, J, AJ-8, J-8 | −55 to +125°C | Ceramic DIP |
| LM208AH, H | −25 to + 85°C | Metal Can |
| LM208AJ, J, AJ-8, J-8 | −25 to +85°C | Ceramic DIP |
| LM208AN, N | −25 to +85°C | Plastic DIP |
| LM208AD, D | −25 to +85°C | SO-8 |
| LM308AH, H | 0 to +70°C | Metal Can |
| LM308AJ, J, AJ-8, J-8 | 0 to +70°C | Ceramic DIP |
| LM308AN, N | 0 to +70°C | Plastic DIP |
| LM308AD, D | 0 to +70°C | SO-8 |

**H SUFFIX**
METAL PACKAGE
CASE 601-04

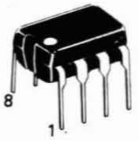

COMPEN B
COMPEN A
VCC
OUTPUT
INPUTS
NC
VEE
1
2
3
4
5
6
7
8
(Top View)

**J SUFFIX**
CERAMIC PACKAGE
CASE 632-02

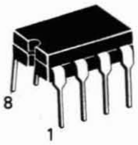



NC 1
COMPEN A 2
*GUARD 3
INPUTS 4
5
*GUARD 6
VEE 7
14 NC
13 NC
12 COMPEN B
11 VCC
10 OUTPUT
9 NC
8 NC
(Top View)

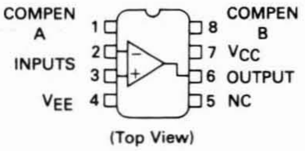
**N SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(LM208, LM208A)
(LM308, LM308A Only)



**J-8 SUFFIX**
CERAMIC PACKAGE
CASE 693-02



**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8


COMPEN A 1
INPUTS 2
3
VEE 4
8 COMPEN B
7 VCC
6 OUTPUT
5 NC
(Top View)

*Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | LM108, LM108A | LM208, LM208A | LM308, LM308A | |
| Power Supply Voltage | $V_{CC}, V_{EE}$ | ±20 | ±20 | ±18 | Vdc |
| Input Voltage (See Note 1) | $V_I$ | ±15 | | | Volts |
| Input Differential Current (See Note 2) | $I_{ID}$ | ±10 | | | mA |
| Output Short-Circuit Duration | $t_S$ | Indefinite | | | |
| Operating Ambient Temperature Range | $T_A$ | −55 to +125 | −25 to +85 | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | | | °C |
| Junction Temperature | $T_J$ | | | | °C |
| Metal, Ceramic Package | | +175 | | | |
| Plastic Package | | +150 | | | |

Note 1. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
Note 2. The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs unless some limiting resistance is used.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted these specifications apply for supply voltages of +5.0 V ≤ $V_{CC}$ ≤ +20 V and −5.0 V ≥ $V_{EE}$ ≥ −20 V, $T_A$ = +25°C.)

| Characteristic | Symbol | LM108A<br>LM208A | | | LM108<br>LM208 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{IO}$ | — | 0.3 | 0.5 | — | 0.7 | 2.0 | mV |
| Input Offset Current | $I_{IO}$ | — | 0.05 | 0.2 | — | 0.005 | 0.2 | nA |
| Input Bias Current | $I_{IB}$ | — | 0.8 | 2.0 | — | 0.8 | 2.0 | nA |
| Input Resistance | $r_i$ | 30 | 70 | — | 30 | 70 | — | Megohms |
| Power Supply Currents<br>$V_{CC}$ = +20 V, $V_{EE}$ = −20 V | $I_{CC}, I_{EE}$ | — | ±0.3 | ±0.6 | — | ±0.3 | ±0.6 | mA |
| Large Signal Voltage Gain<br>$V_{CC} = \|V_{EE}\|$ = +15 V, $V_O$ = ±10 V,<br>$R_L$ ≥ 10 kΩ | $A_{VOL}$ | 80 | 300 | — | 50 | 300 | — | V/mV |
| The following specifications apply over the operating temperature range. | | | | | | | | |
| Input Offset Voltage | $V_{IO}$ | — | — | 1.0 | — | — | 3.0 | mV |
| Input Offset Current | $I_{IO}$ | — | — | 0.4 | — | — | 0.4 | nA |
| Average Temperature Coefficient of<br>Input Offset Voltage<br>$T_A(min) \leq T_A \leq T_A(max)$ | $\Delta V_{IO}/\Delta T$ | — | 1.0 | 5.0 | — | 3.0 | 15 | µV/°C |
| Average Temperature Coefficient of<br>Input Offset Current | $\Delta I_{IO}/\Delta T$ | — | 0.5 | 2.5 | — | 0.5 | 2.5 | pA/°C |
| Input Bias Current | $I_{IB}$ | — | — | 3.0 | — | — | 3.0 | nA |
| Large Signal Voltage Gain<br>$V_{CC} = \|V_{EE}\|$ = +15 V, $V_O$ = ±10 V,<br>$R_L$ = 10 kΩ | $A_{VOL}$ | 40 | — | — | 25 | — | — | V/mV |
| Input Voltage Range<br>$V_{CC} = \|V_{EE}\|$ = +15 V | $V_{IR}$ | ±13.5 | — | — | ±13.5 | — | — | V |
| Common-Mode Rejection Ratio | CMRR | 96 | 110 | — | 85 | 100 | — | dB |
| Power Supply Voltage Rejection Ratio | PSRR | 96 | 100 | — | 80 | 96 | — | dB |
| Output Voltage Range<br>$V_{CC} = \|V_{EE}\|$ = +15 V, $R_L$ = 10 kΩ | $V_{OR}$ | ±13 | ±14 | — | ±13 | ±14 | — | V |
| Supply Current ($T_A = T_A$[max]) | $I_{CC}, I_{EE}$ | — | ±0.15 | ±0.4 | — | ±0.15 | ±0.4 | mA |

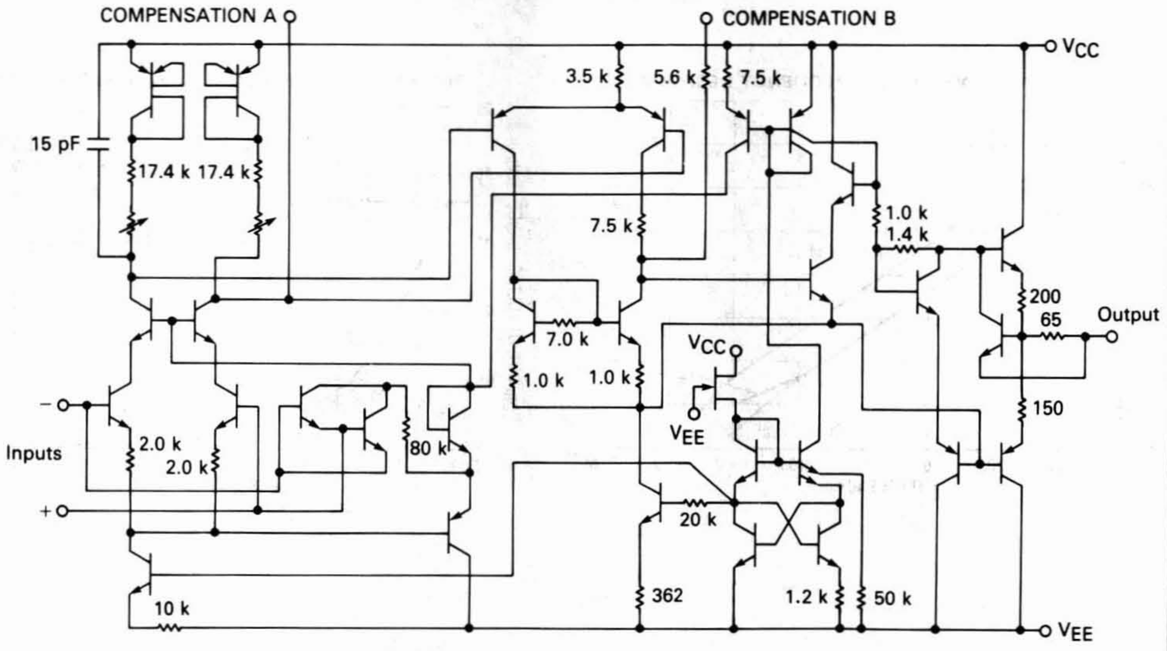
**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted these specifications apply for supply voltages of +5.0 V ≤ $V_{CC}$ ≤ +15 V and −5.0V ≥ $V_{EE}$ ≥ −15 V, $T_A$ = +25°C.)

| Characteristic | Symbol | LM308A Min | LM308A Typ | LM308A Max | LM308 Min | LM308 Typ | LM308 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{IO}$ | — | 0.3 | 0.5 | — | 2.0 | 7.5 | mV |
| Input Offset Current | $I_{IO}$ | — | 0.2 | 1.0 | — | 0.2 | 1.0 | nA |
| Input Bias Current | $I_{IB}$ | — | 1.5 | 7.0 | — | 1.5 | 7.0 | nA |
| Input Resistance | $r_i$ | 10 | 40 | — | 10 | 40 | — | Megohms |
| Power Supply Currents<br>$V_{CC}$ = +15 V, $V_{EE}$ = −15 V | $I_{CC}$,$I_{EE}$ | — | ±0.3 | ±0.8 | — | ±0.3 | ±0.8 | mA |
| Large Signal Voltage Gain<br>$V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $V_O$ = ±10 V,<br>$R_L$ ≥ 10 kΩ | $A_{VOL}$ | 80 | 300 | — | 25 | 300 | — | V/mV |

The following specifications apply over the operating temperature range.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{IO}$ | — | — | 0.73 | — | — | 10 | mV |
| Input Offset Current | $I_{IO}$ | — | — | 1.5 | — | — | 1.5 | nA |
| Average Temperature Coefficient of<br>Input Offset Voltage<br>$T_A$(min) ≤ $T_A$ ≤ $T_A$(max) | $\Delta V_{IO}/\Delta T$ | — | 1.0 | 5.0 | — | 6.0 | 30 | µV/°C |
| Average Temperature Coefficient of<br>Input Offset Current | $\Delta I_{IO}/\Delta T$ | — | 2.0 | 10 | — | 2.0 | 10 | pA/°C |
| Input Bias Current | $I_{IB}$ | — | — | 10 | — | — | 10 | nA |
| Large Signal Voltage Gain<br>$V_{CC}$+15 V, $V_{EE}$ = −15 V, $V_O$ = ±10 V,<br>$R_L$ ≥ 10 kΩ | $A_{VOL}$ | 60 | — | — | 15 | — | — | V/mV |
| Input Voltage Range<br>$V_{CC}$ = +15 V, $V_{EE}$ = −15 V | $V_{IR}$ | ±14 | — | — | ±14 | — | — | V |
| Common-Mode Rejection Ratio<br>$R_S$ ≤ 50 kΩ | CMRR | 96 | 110 | — | 80 | 100 | — | dB |
| Supply Voltage Rejection Ratio<br>$R_S$ ≤ 50 kΩ | PSRR | 96 | 110 | — | 80 | 96 | — | dB |
| Output Voltage Range<br>$V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ = 10 kΩ | $V_{OR}$ | ±13 | ±14 | — | ±13 | ±14 | — | V |

**REPRESENTATIVE CIRCUIT SCHEMATIC**


COMPENSATION A
COMPENSATION B
VCC
3.5 k
5.6 k
7.5 k
15 pF
17.4 k
17.4 k
7.5 k
1.0 k
1.4 k
200
65
Output
7.0 k
1.0 k
1.0 k
VCC
VEE
150
−
Inputs
2.0 k
2.0 k
80 k
+
20 k
362
1.2 k
50 k
10 k
VEE

## TYPICAL CHARACTERISTICS

FIGURE 1 — INPUT BIAS AND INPUT OFFSET CURRENTS

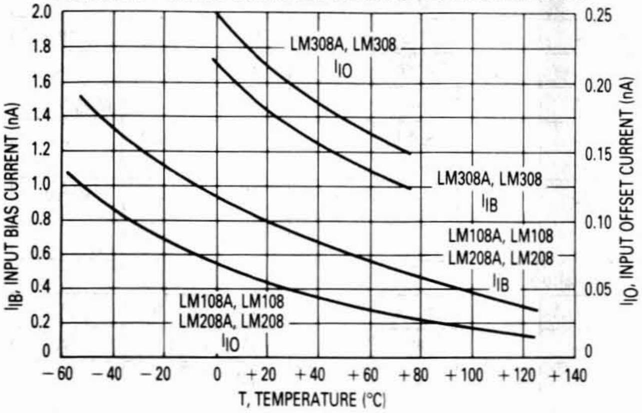


FIGURE 2 — MAXIMUM EQUIVALENT INPUT OFFSET VOLTAGE ERROR versus INPUT RESISTANCE

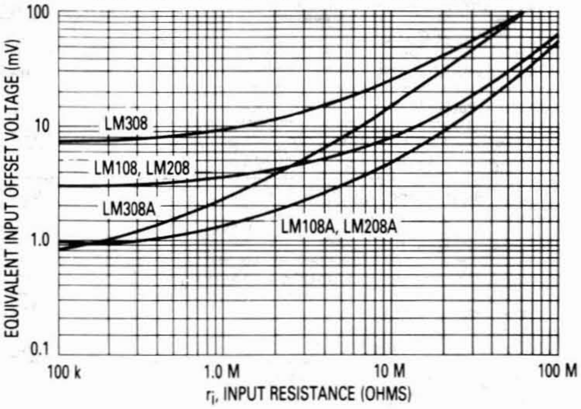


FIGURE 3 — VOLTAGE GAIN versus SUPPLY VOLTAGES

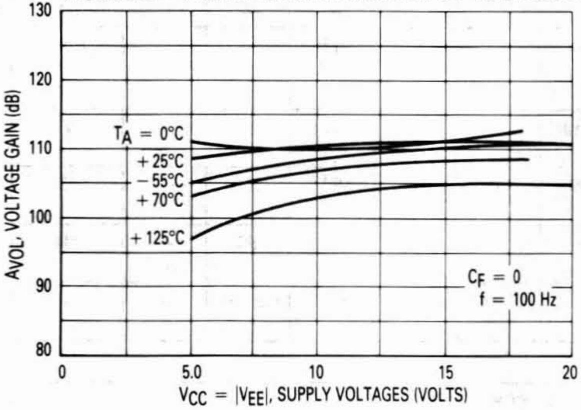


FIGURE 4 — POWER SUPPLY CURRENTS versus POWER SUPPLY VOLTAGE

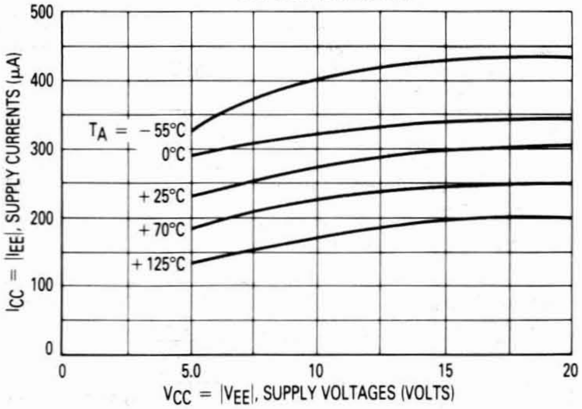


FIGURE 5 — OPEN-LOOP FREQUENCY RESPONSE

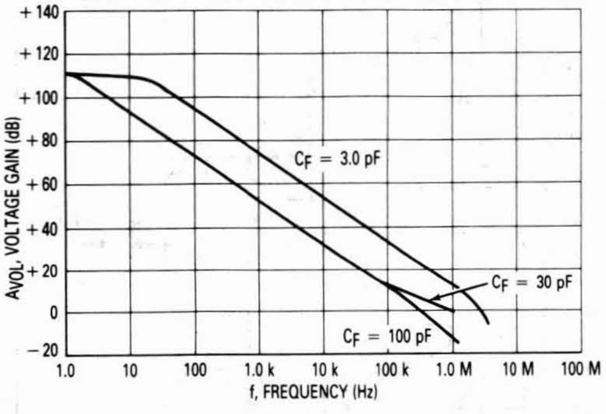
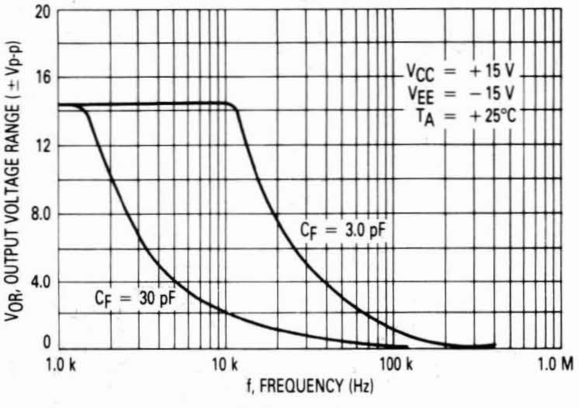
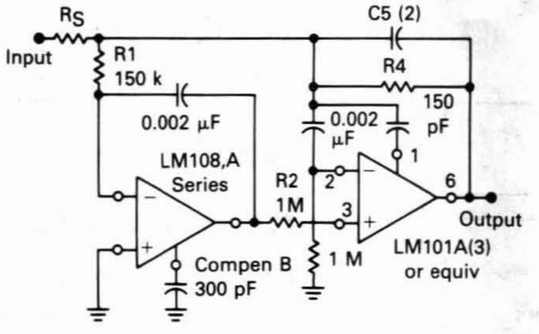


FIGURE 6 — LARGE-SIGNAL FREQUENCY RESPONSE



## SUGGESTED DESIGN APPLICATIONS

FIGURE 7 — FAST (1) SUMMING AMPLIFIER WITH LOW INPUT CURRENT

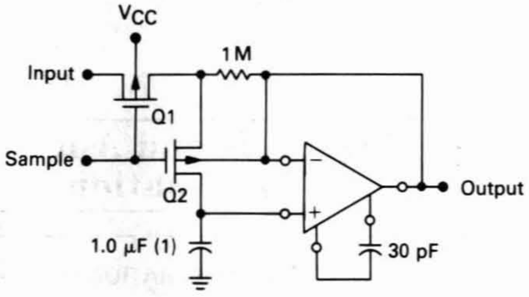

RS
Input
R1
150 k
0.002 µF
LM108,A
Series
Compen B
300 pF
C5 (2)
R4
0.002
µF
150
pF
1
R2
1M
2
3
6
Output
1 M
LM101A(3)
or equiv

(1) Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/µs

(2) $C5 = \frac{6 \times 10^{-8}}{R1}$

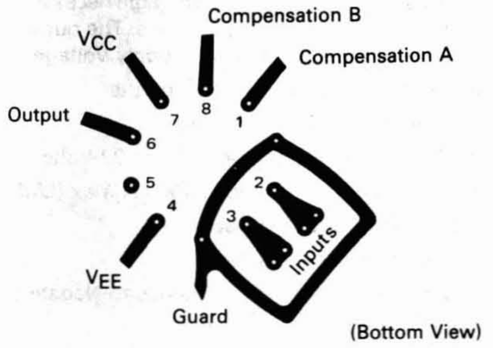
(3) In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

FIGURE 8 — SAMPLE AND HOLD


VCC
Input
1 M
Q1
Sample
Q2
Output
1.0 µF (1)
30 pF

(1) Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

FIGURE 9 — SUGGESTED PRINTED CIRCUIT BOARD LAYOUT for INPUT GUARDING USING METAL PACKAGED DEVICE


Compensation B
VCC
Compensation A
Output
7
8
1
6
5
2
4
3
Inputs
VEE
Guard
(Bottom View)

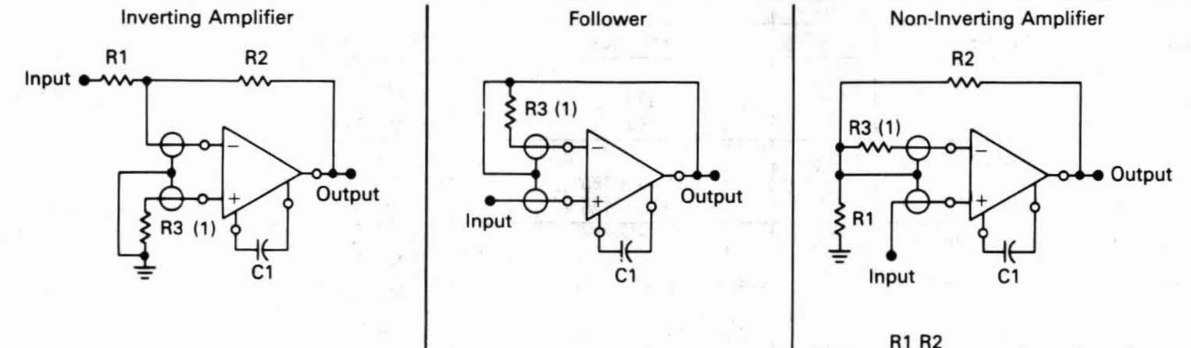
### INPUT GUARDING

Special care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the LM108,A amplifier series. Boards must be thoroughly cleaned with alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at +125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 type package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the boards. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard MC1741 and LM101A pin configuration).

FIGURE 10 — CONNECTION OF INPUT GUARDS


Inverting Amplifier
R1
R2
Input
Output
R3 (1)
C1
Follower
R3 (1)
Output
Input
C1
Non-Inverting Amplifier
R2
R3 (1)
Output
R1
Input
C1

(1) Used to compensate for large source resistances.

Note: $\frac{R1\,R2}{R1 + R2}$ must be an impedance.

**MOTOROLA**

# LM124, LM224,
# LM324, LM324A
# LM2902

## Specifications and Applications Information

### QUAD LOW POWER OPERATIONAL AMPLIFIERS

The LM124 Series are low-cost, quad operational amplifiers with true differential inputs. These have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 32 Volts with quiescent currents about one fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 32 Volts
- Low Input Bias Currents: 100 nA Max (LM324A)
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

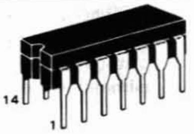
| Rating | Symbol | LM124<br>LM224<br>LM324,A | LM2902 | Unit |
|---|---|---|---|---|
| Power Supply Voltages | | | | Vdc |
| Single Supply | $V_{CC}$ | 32 | 26 | |
| Split Supplies | $V_{CC}$, $V_{EE}$ | ±16 | ±13 | |
| Input Differential Voltage Range (1) | $V_{IDR}$ | ±32 | ±26 | Vdc |
| Input Common Mode Voltage Range | $V_{ICR}$ | −0.3 to 32 | −0.3 to 26 | Vdc |
| Input Forward Current (2) ($V_I < -0.3$ V) | $I_{IF}$ | 50 | — | mA |
| Output Short Circuit Duration | $t_S$ | Continuous | | |
| Junction Temperature | $T_J$ | | | °C |
| Ceramic Package | | 175 | | |
| Plastic Packages | | 150 | | |
| Storage Temperature Range | $T_{stg}$ | | | °C |
| Ceramic Package | | −65 to +150 | | |
| Plastic Packages | | −55 to +125 | | |
| Operating Ambient Temperature Range | $T_A$ | | | °C |
| LM124 | | −55 to +125 | — | |
| LM224 | | −25 to +85 | — | |
| LM324 | | 0 to +70 | — | |
| LM324A | | 0 to +70 | — | |
| LM2902 | | — | −40 to +85 | |

(1) Split Power Supplies.

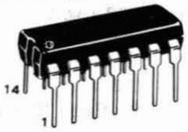
(2) This input current will only exist when the voltage is negative at any of the input leads. Normal output states will reestablish when the input voltage returns to a voltage greater than −0.3 V.

### QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



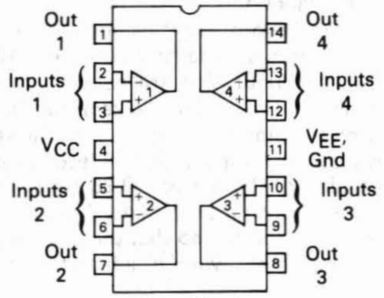
**J SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA
(TO-116)



**N SUFFIX**
PLASTIC PACKAGE
CASE 646-05
(LM224, LM324, LM2902 only)

**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
(SO-14)

**PIN CONNECTIONS**



(Top View)

| ORDERING INFORMATION | | |
|---|---|---|
| **Device** | **Temperature Range** | **Package** |
| LM124J | −55 to +125°C | Ceramic DIP |
| LM2902D | −40 to +85°C | SO-14 |
| LM2902J | | Ceramic DIP |
| LM2902N | | Plastic DIP |
| LM224D | −25 to +85°C | SO-14 |
| LM224J | | Ceramic DIP |
| LM224N | | Plastic DIP |
| LM324AD | 0 to +70°C | SO-14 |
| LM324AN | | Plastic DIP |
| LM324D | | SO-14 |
| LM324J | | Ceramic DIP |
| LM324N | | Plastic DIP |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = Gnd, $T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | LM124/LM224 Min | LM124/LM224 Typ | LM124/LM224 Max | LM324A Min | LM324A Typ | LM324A Max | LM324 Min | LM324 Typ | LM324 Max | LM2902 Min | LM2902 Typ | LM2902 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage<br>$V_{CC}$ = 5.0 V to 30 V (26 V for LM2902),<br>$V_{ICR}$ = 0 V to $V_{CC}$ −1.7 V, $V_O$ ≃ 1.4 V, $R_S$ = 0 Ω | $V_{IO}$ | | | | | | | | | | | | | mV |
| $T_A$ = 25°C | | — | 2.0 | 5.0 | — | 2.0 | 3.0 | — | 2.0 | 7.0 | — | 2.0 | 7.0 | |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | | — | — | 7.0 | — | — | 5.0 | — | — | 9.0 | — | — | 10 | |
| Average Temperature Coefficient of Input Offset Voltage<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | $\Delta V_{IO}/\Delta T$ | — | 7.0 | — | — | 7.0 | 30 | — | 7.0 | — | — | 7.0 | — | µV/°C |
| Input Offset Current | $I_{IO}$ | — | 3.0 | 30 | — | 5.0 | 30 | — | 5.0 | 50 | — | 5.0 | 50 | nA |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | | — | — | 100 | — | — | 75 | — | — | 150 | — | — | 200 | |
| Average Temperature Coefficient of Input Offset Current<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | $\Delta I_{IO}/\Delta T$ | — | 10 | — | — | 10 | 300 | — | 10 | — | — | 10 | — | pA/°C |
| Input Bias Current | $I_{IB}$ | — | −90 | −150 | — | −45 | −100 | — | −90 | −250 | — | −90 | −250 | nA |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | | — | — | −300 | — | — | −200 | — | — | −500 | — | — | −500 | |
| Input Common-Mode Voltage Range (Note 2) | $V_{ICR}$ | | | | | | | | | | | | | V |
| $V_{CC}$ = 30 V (26 V for LM2902) | | 0 | — | 28.3 | 0 | — | 28.3 | 0 | — | 28.3 | 0 | — | 24.3 | |
| $V_{CC}$ = 30 V (26 V for LM2902), $T_A$ = $T_{high}$ to $T_{low}$ | | 0 | — | 28 | 0 | — | 28 | 0 | — | 28 | 0 | — | 24 | |
| Differential Input Voltage Range | $V_{IDR}$ | — | — | $V_{CC}$ | — | — | $V_{CC}$ | — | — | $V_{CC}$ | — | — | $V_{CC}$ | V |
| Large Signal Open-Loop Voltage Gain | $A_{VOL}$ | | | | | | | | | | | | | V/mV |
| $R_L$ = 2.0 kΩ, $V_{CC}$ = 15 V, For Large $V_O$ Swing, | | 50 | 100 | — | 25 | 100 | — | 25 | 100 | — | — | 100 | — | |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | | 25 | — | — | 15 | — | — | 15 | — | — | — | — | — | |
| Channel Separation<br>1.0 kHz ≤ f ≤ 20 kHz, Input Referenced | — | — | −120 | — | — | −120 | — | — | −120 | — | — | −120 | — | dB |
| Common-Mode Rejection Ratio<br>$R_S$ ≤ 10 kΩ | CMRR | 70 | 85 | — | 65 | 70 | — | 65 | 70 | — | 50 | 70 | — | dB |
| Power Supply Rejection Ratio | PSRR | 65 | 100 | — | 65 | 100 | — | 65 | 100 | — | 50 | 100 | — | dB |
| Output Voltage Range<br>$R_L$ = 2.0 kΩ ($R_L$ ≥ 10 kΩ for LM2902) | $V_{OR}$ | 0 | — | 3.3 | 0 | — | 3.3 | 0 | — | 3.3 | 0 | — | 3.3 | V |
| Output Voltage — High Limit ($T_A$ = $T_{high}$ to $T_{low}$) (Note 1) | $V_{OH}$ | | | | | | | | | | | | | V |
| $V_{CC}$ = 30 V (26 V for LM2902), $R_L$ = 2.0 kΩ | | 26 | — | — | 26 | — | — | 26 | — | — | 22 | — | — | |
| $V_{CC}$ = 30 V (26 V for LM2902), $R_L$ = 10 kΩ | | 27 | 28 | — | 27 | 28 | — | 27 | 28 | — | 23 | 24 | — | |
| Output Voltage — Low Limit<br>$V_{CC}$ = 5.0 V, $R_L$ = 10 kΩ, $T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | $V_{OL}$ | — | 5.0 | 20 | — | 5.0 | 20 | — | 5.0 | 20 | — | 5.0 | 100 | mV |
| Output Source Current ($V_{ID}$ = +1.0 V, $V_{CC}$ = 15 V) | $I_{O+}$ | | | | | | | | | | | | | mA |
| $T_A$ = 25°C | | 20 | 40 | — | 20 | 40 | — | 20 | 40 | — | 20 | 40 | — | |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | | 10 | 20 | — | 10 | 20 | — | 10 | 20 | — | 10 | 20 | — | |
| Output Sink Current<br>($V_{ID}$ = −1.0 V, $V_{CC}$ = 15 V | $I_{O-}$ | | | | | | | | | | | | | mA |
| $T_A$ = 25°C | | 10 | 20 | — | 10 | 20 | — | 10 | 20 | — | 10 | 20 | — | |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | | 5.0 | 8.0 | — | 5.0 | 8.0 | — | 5.0 | 8.0 | — | 5.0 | 8.0 | — | |
| $V_{ID}$ = −1.0 V, $V_O$ = 200 mV, $T_A$ = 25°C | | 12 | 50 | — | 12 | 50 | — | 12 | 50 | — | — | — | — | µA |
| Output Short Circuit to Ground (Note 3) | $I_{os}$ | — | 40 | 60 | — | 40 | 60 | — | 40 | 60 | — | 40 | 60 | mA |
| Power Supply Current ($T_A$ = $T_{high}$ to $T_{low}$) (Note 1) | $I_{CC}$ | | | | | | | | | | | | | mA |
| $V_{CC}$ = 30 V (26 V for LM2902), $V_O$ = 0 V, $R_L$ = ∞ | | — | — | 3.0 | — | 1.4 | 3.0 | — | — | 3.0 | — | — | 3.0 | |
| $V_{CC}$ = 5.0 V, $V_O$ = 0 V, $R_L$ = ∞ | | — | — | 1.2 | — | 0.7 | 1.2 | — | — | 1.2 | — | — | 1.2 | |

NOTES:

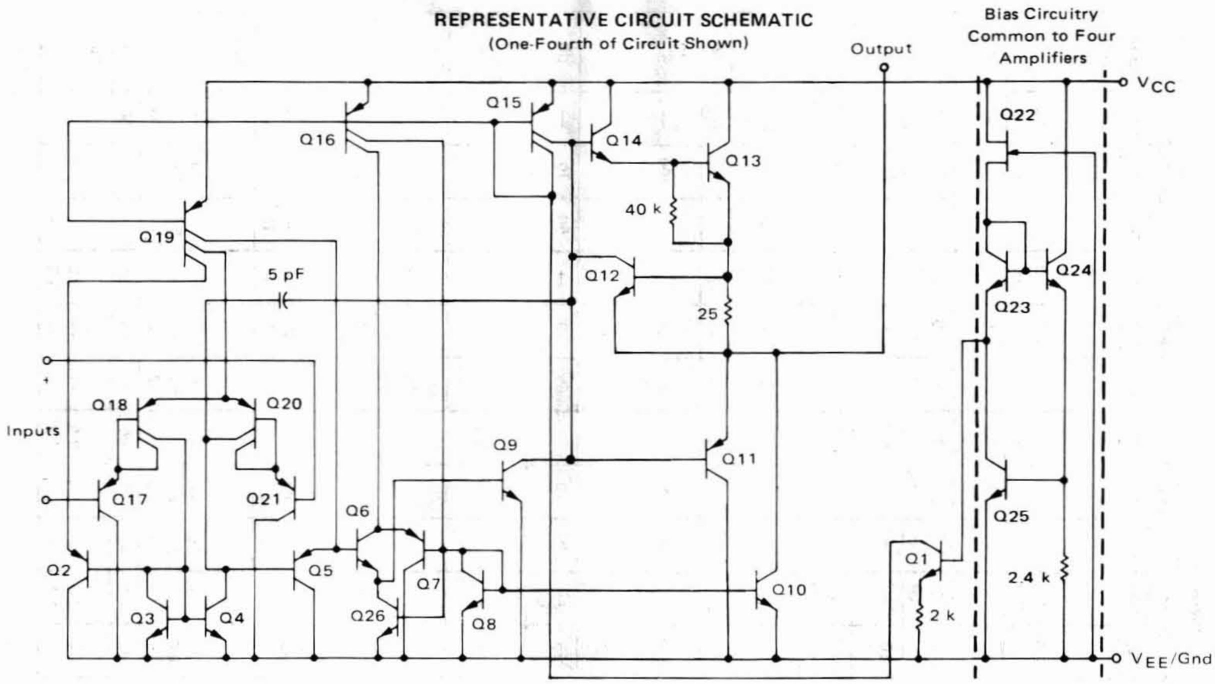
(1) $T_{low}$ = −55°C for LM124
= −40°C for LM2902
= −25°C for LM224
= 0 °C for LM324,A

$T_{high}$ = +125°C for LM124
= +85°C for LM2902 and LM224
= +70°C for LM324,A

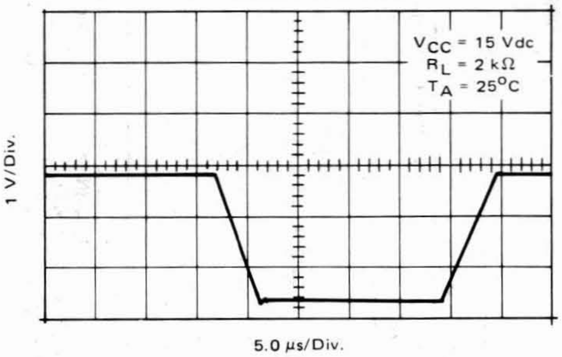
(2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC}$ −1.7 V, but either or both inputs can go to +32 V without damage (+26 V for LM2902).

(3) Short circuits from the output to $V_{CC}$ can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

REPRESENTATIVE CIRCUIT SCHEMATIC
(One-Fourth of Circuit Shown)


Output
Bias Circuitry
Common to Four
Amplifiers
$V_{CC}$
Q15
Q16
Q14
Q13
Q22
40 k
Q19
5 pF
Q12
25
Q24
Q23
+
Inputs
−
Q18
Q20
Q17
Q21
Q9
Q11
Q6
Q25
Q2
Q5
Q7
Q1
2.4 k
Q3
Q4
Q26
Q8
Q10
2 k
$V_{EE}$/Gnd

LARGE SIGNAL VOLTAGE
FOLLOWER RESPONSE

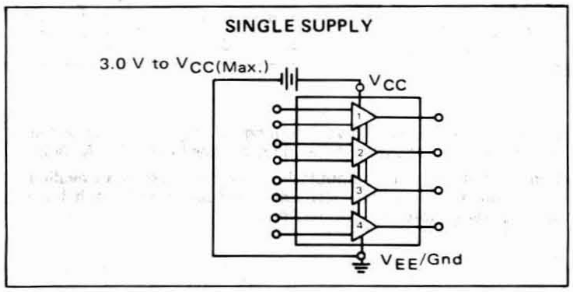


## CIRCUIT DESCRIPTION

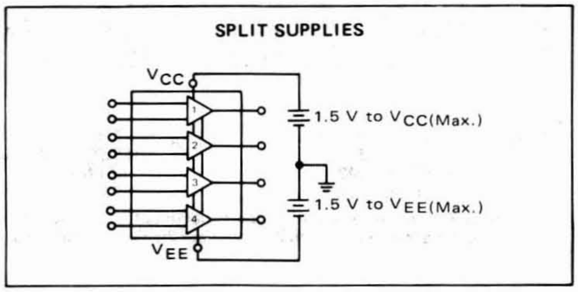
The LM124 Series is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

SINGLE SUPPLY


3.0 V to $V_{CC(Max.)}$
$V_{CC}$
1
2
3
4
$V_{EE}$/Gnd

SPLIT SUPPLIES


$V_{CC}$
1
2
3
4
1.5 V to $V_{CC(Max.)}$
1.5 V to $V_{EE(Max.)}$
$V_{EE}$

## TYPICAL PERFORMANCE CURVES

**FIGURE 1 – INPUT VOLTAGE RANGE**

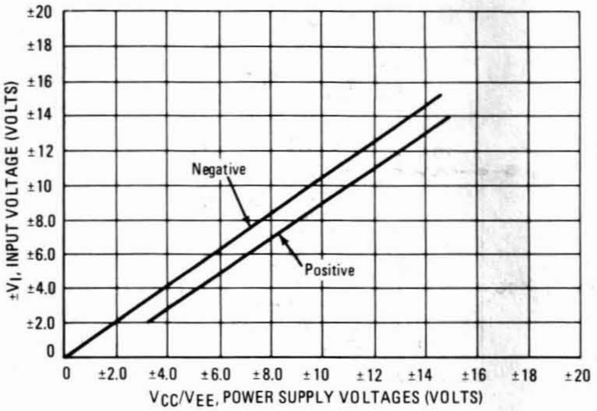


**FIGURE 2 – OPEN LOOP FREQUENCY**

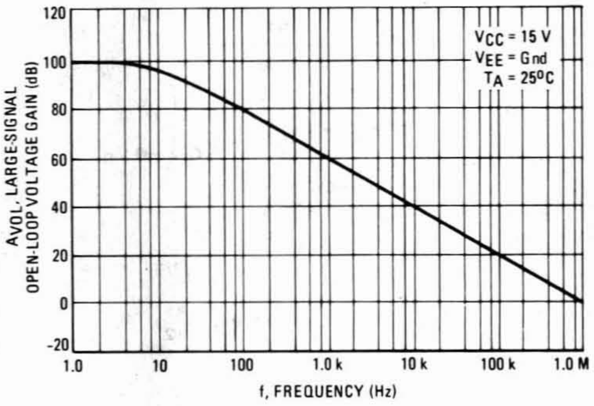


**FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE**

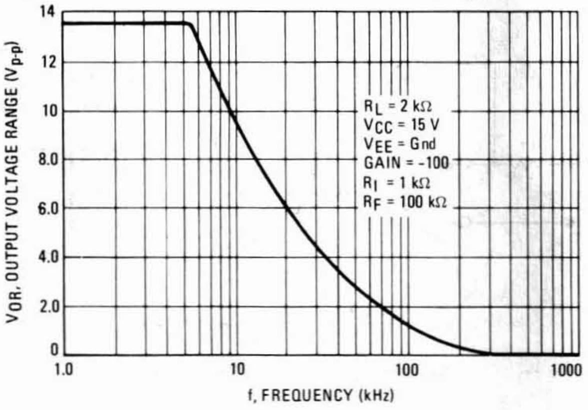


**FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE (Non-Inverting)**

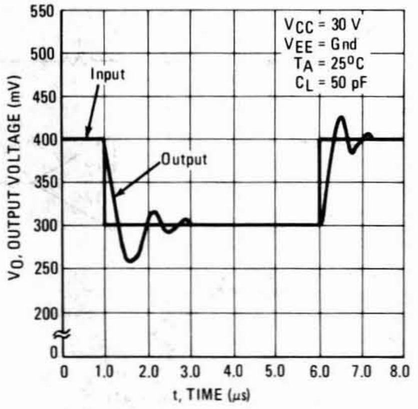


**FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE**

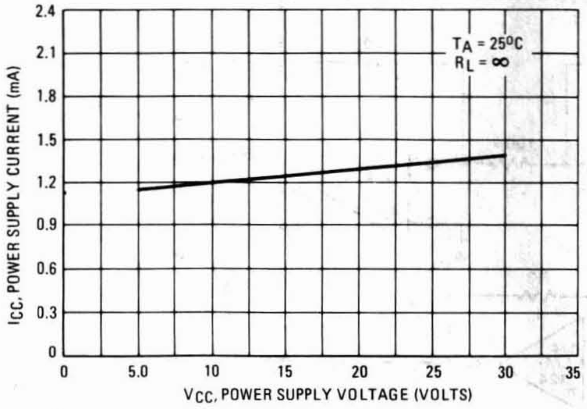
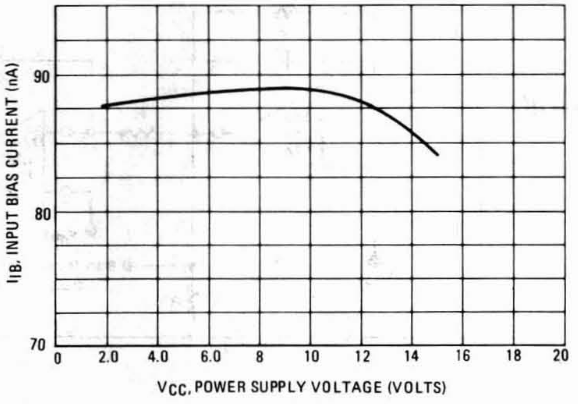
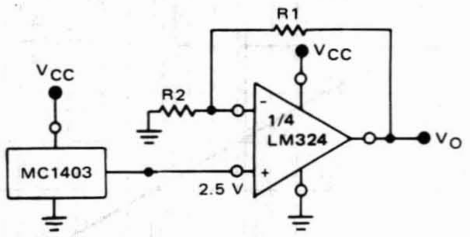


**FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE**



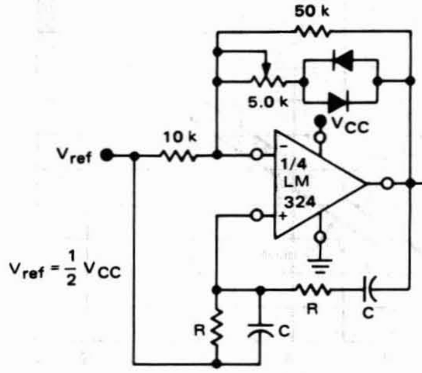
## APPLICATIONS INFORMATION

FIGURE 7 – VOLTAGE REFERENCE


R1
VCC
VCC
R2
1/4
LM324
VO
MC1403
2.5 V

$V_O = 2.5\ V(1 + \frac{R1}{R2})$

FIGURE 8 – WIEN BRIDGE OSCILLATOR

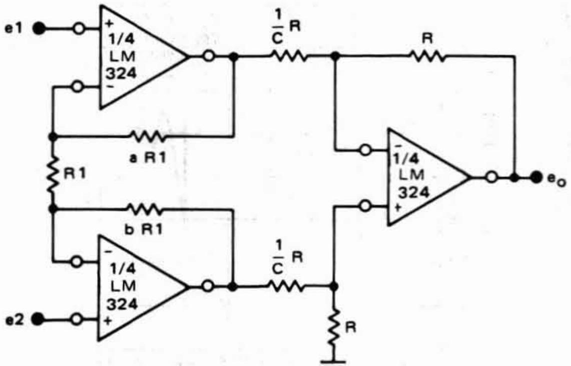

50 k
5.0 k
VCC
10 k
Vref
1/4
LM
324
VO
R
C
R
C

$V_{ref} = \frac{1}{2} V_{CC}$

$f_o = \frac{1}{2\pi RC}$

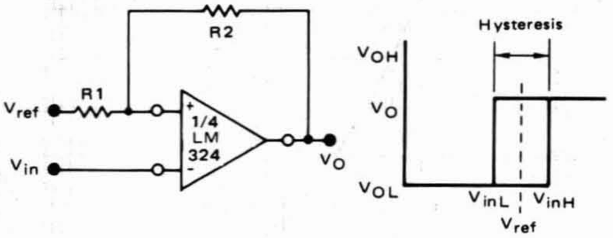
For $f_o = 1\ kHz$
$R = 16\ k\Omega$
$C = 0.01\ \mu F$

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


e1
1/4
LM
324
$\frac{1}{C}$ R
R
a R1
R1
b R1
1/4
LM
324
eo
1/4
LM
324
e2
$\frac{1}{C}$ R
R

$e_o = C\ (1 + a + b)\ (e2 - e1)$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

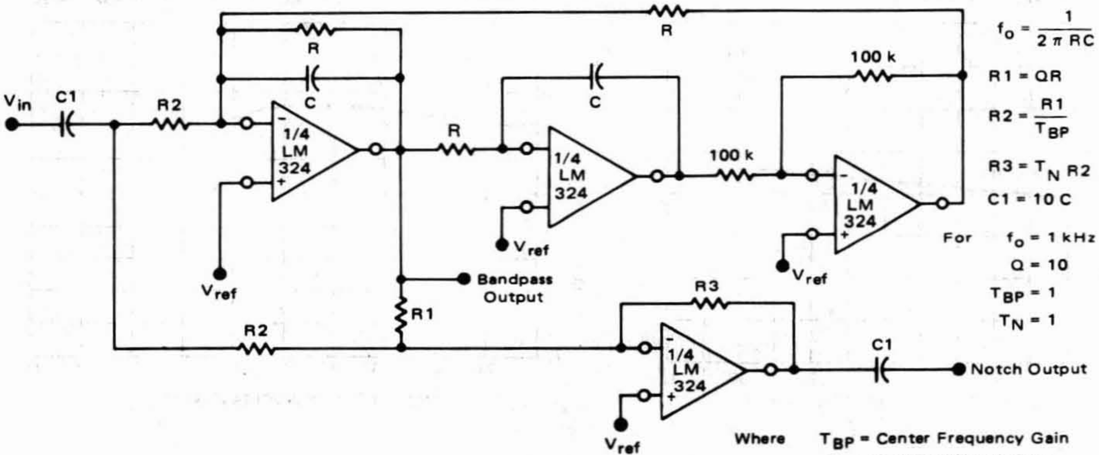

R2
R1
Vref
Vin
1/4
LM
324
VO
Hysteresis
VOH
VO
VOL
VinL
VinH
Vref

$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$

$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$

$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$

FIGURE 11 – BI-QUAD FILTER


R
R
C
Vin
C1
R2
1/4
LM
324
Vref
R
C
1/4
LM
324
Vref
100 k
100 k
1/4
LM
324
Vref
Bandpass Output
R1
R2
R3
1/4
LM
324
Vref
C1
Notch Output

$f_o = \frac{1}{2\pi RC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N\ R2$

$C1 = 10\ C$

$V_{ref} = \frac{1}{2} V_{CC}$

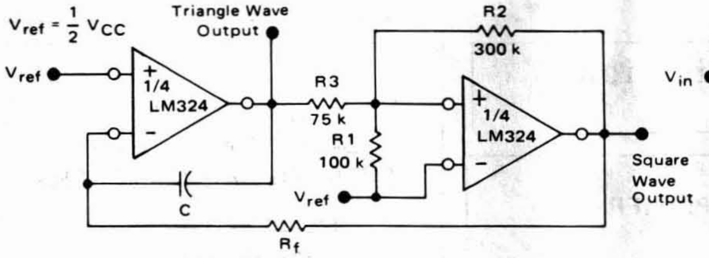
For $f_o = 1\ kHz$
$Q = 10$
$T_{BP} = 1$
$T_N = 1$

$R = 160\ k\Omega$
$C = 0.001\ \mu F$
$R1 = 1.6\ M\Omega$
$R2 = 1.6\ M\Omega$
$R3 = 1.6\ M\Omega$

Where $T_{BP}$ = Center Frequency Gain
$T_N$ = Passband Notch Gain

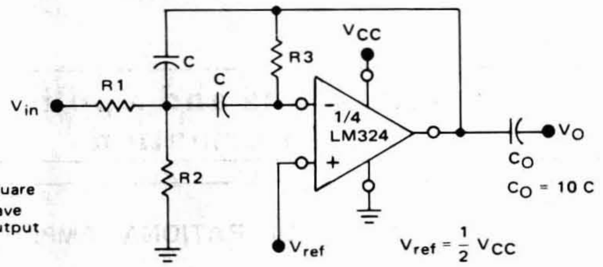
## APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR


$V_{ref} = \frac{1}{2} V_{CC}$
Triangle Wave Output
$V_{ref}$
+
–
1/4 LM324
R3
75 k
R1
100 k
R2
300 k
+
–
1/4 LM324
$V_{ref}$
C
$R_f$
Square Wave Output

$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER


$V_{CC}$
C
R3
R1
C
$V_{in}$
–
+
1/4 LM324
R2
$V_{ref}$
$V_O$
$C_O$
$C_O = 10\,C$
$V_{ref} = \frac{1}{2} V_{CC}$

Given $f_o$ = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value $f_o$, C
Then:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1 \qquad \text{Where } f_o \text{ and BW are expressed in Hz.}$$

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

**MOTOROLA**

# LM148
# LM248
# LM348

## Specifications and Applications Information

**QUAD MC1741 DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS**

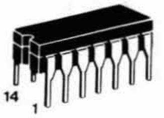
**SILICON MONOLITHIC INTEGRATED CIRCUIT**

### QUAD MC1741 OPERATIONAL AMPLIFIERS

The LM148 series is a true quad MC1741. Integrated on a single monolithic chip are four independent, low power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single MC1741. Other features include input offset currents and input bias currents which are much less than the MC1741 industry standard.

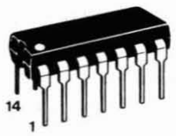
The LM148 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Low Input Offset and Input Bias Currents
- Class AB Output Stage Eliminates Crossover Distortion
- Pin Compatible with MC3503 and LM124
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)



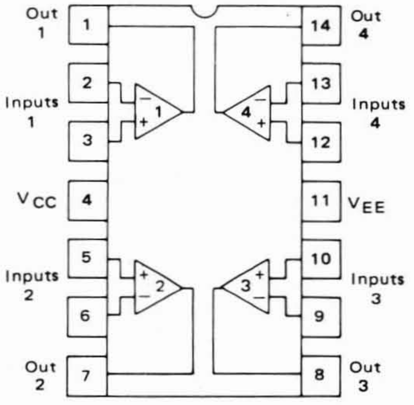
**J SUFFIX**
CERAMIC PACKAGE
CASE 632-02

**N SUFFIX**
PLASTIC PACKAGE
CASE 646-05
(LM248 and
LM348 only)



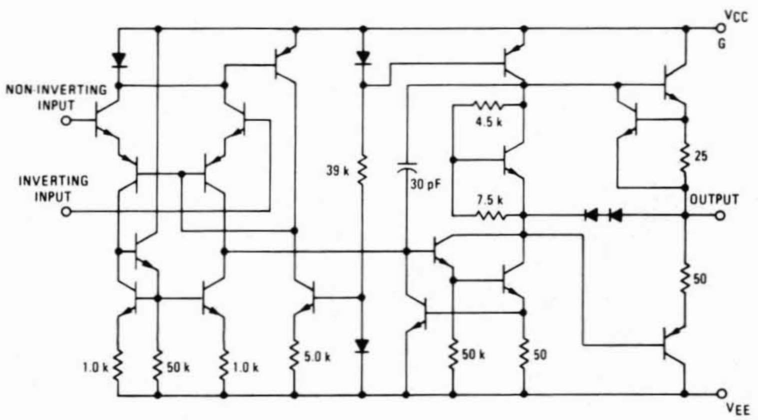
**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14
(LM348 Only)

**PIN CONNECTIONS**



(Top View)

**EQUIVALENT CIRCUIT SCHEMATIC**
**(1/4 of Circuit Shown)**



**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| LM148J | −55 to +125°C | Ceramic DIP |
| LM248J | −25 to +85°C | Ceramic DIP |
| LM248N | −25 to +85°C | Plastic DIP |
| LM348D | 0 to +70°C | SO-14 |
| LM348J | 0 to +70°C | Ceramic DIP |
| LM348N | 0 to +70°C | Plastic DIP |

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | LM148 | LM248/LM348 | | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +22<br>−22 | +18<br>−18 | | Vdc<br>Vdc |
| Input Differential Voltage | $V_{ID}$ | ±44 | ±36 | | Volts |
| Input Common Mode Voltage | $V_{ICM}$ | ±22 | ±18 | | Volts |
| Output Short Circuit Duration | $t_S$ | Continuous | | | |
| Operating Ambient Temperature Range | $T_A$ | −55 to +125 | −25 to +85 | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | | | | °C |
| Ceramic Package | | −65 to +150 | | | |
| Plastic Package | | −55 to +125 | | | |
| Junction Temperature | $T_J$ | | | | °C |
| Ceramic Package | | 175 | | | |
| Plastic Package | | 150 | | | |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | LM148 | | | LM248/348 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage<br>($R_S$ ≤ 10 k) | $V_{IO}$ | – | 1.0 | 5.0 | – | 1.0 | 6.0 | mV |
| Input Offset Current | $I_{IO}$ | – | 4.0 | 25 | – | 4.0 | 50 | nA |
| Input Bias Current | $I_{IB}$ | – | 30 | 100 | – | 30 | 200 | nA |
| Input Resistance | $r_i$ | 0.8 | 2.5 | – | 0.8 | 2.5 | – | MΩ |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±12 | – | – | ±12 | – | – | V |
| Large Signal Voltage Gain<br>($R_L$ ≥ 2.0 k, $V_O$ = ±10 V) | $A_v$ | 50 | 160 | – | 25 | 160 | – | V/mV |
| Channel Separation<br>(f = 1.0 Hz to 20 kHz) | – | – | -120 | – | – | -120 | – | dB |
| Common Mode Rejection Ratio<br>($R_S$ ≤ 10 k) | CMRR | 70 | 90 | – | 70 | 90 | – | dB |
| Supply Voltage Rejection Ratio<br>($R_S$ ≤ 10 k) | PSRR | 77 | 96 | – | 77 | 96 | – | dB |
| Output Voltage Swing | $V_O$ | | | | | | | V |
| ($R_L$ ≥ 10 k) | | ±12 | ±13 | – | ±12 | ±13 | – | |
| ($R_L$ ≥ 2 k) | | ±10 | ±12 | – | ±10 | ±12 | – | |
| Output Short-Circuit Current | $I_{os}$ | – | 25 | – | – | 25 | – | mA |
| Supply Current – (All Amplifiers) | $I_D$ | – | 2.4 | 3.6 | – | 2.4 | 4.5 | mA |
| Small Signal Bandwidth ($A_V$ = 1) | BW | – | 1.0 | – | – | 1.0 | – | MHz |
| Phase Margin ($A_V$ = 1) | $\phi m$ | – | 60 | – | – | 60 | – | degrees |
| Slew Rate ($A_V$ = 1) | SR | – | 0.5 | – | – | 0.5 | – | V/μs |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = *$T_{high}$ to $T_{low}$ unless otherwise noted)

| Characteristic | Symbol | LM148 Min | LM148 Typ | LM148 Max | LM248/348 Min | LM248/348 Typ | LM248/348 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage<br>($R_S$ ≤ 10 kΩ) | $V_{IO}$ | – | – | 6.0 | – | – | 7.5 | mV |
| Input Offset Current | $I_{IO}$ | | | | | | | nA |
| LM148 | | – | – | 75 | – | – | – | |
| LM248 | | – | – | – | – | – | 125 | |
| LM348 | | – | – | – | – | – | 100 | |
| Input Bias Current | $I_{IB}$ | | | | | | | nA |
| LM148 | | – | – | 325 | – | – | – | |
| LM248 | | – | – | – | – | – | 500 | |
| LM348 | | – | – | – | – | – | 400 | |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±12 | – | – | ±12 | – | – | V |
| Large Signal Voltage Gain<br>($R_L$ ≥ 2 k, $V_O$ = ±10 V) | $A_v$ | 25 | – | – | 15 | – | – | V/mV |
| Common Mode Rejection Ratio<br>($R_S$ ≤ 10 k) | CMRR | 70 | 90 | – | 70 | 90 | – | dB |
| Supply Voltage Rejection Ratio<br>($R_S$ ≤ 10 k) | PSRR | 77 | 96 | – | 77 | 96 | – | dB |
| Output Voltage Swing | $V_O$ | | | | | | | V |
| ($R_L$ ≥ 10 k) | | ±12 | ±13 | – | ±12 | ±13 | – | |
| ($R_L$ ≥ 2 k) | | ±10 | ±12 | – | ±10 | ±12 | – | |

*$T_{high}$ = 125°C for LM148, 85°C for LM248, and 70°C for LM348. $T_{low}$ = −55°C for LM148, −25°C for LM248, and 0°C for LM348.

NOTE: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted or the maximum junction temperature will be exceeded.

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C unless otherwise noted).

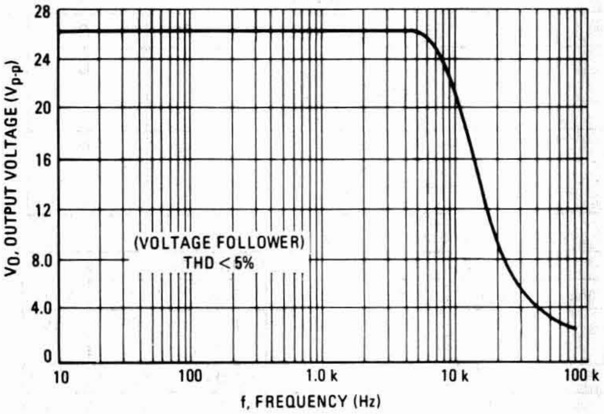


FIGURE 1 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

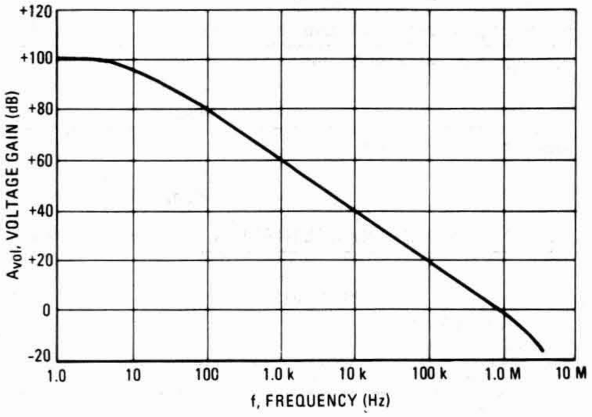


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

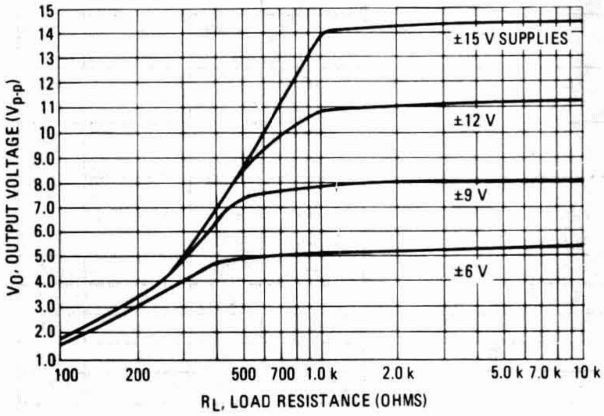


FIGURE 3 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

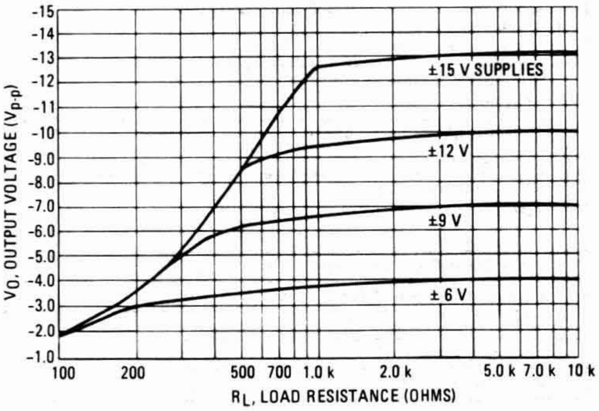


FIGURE 4 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

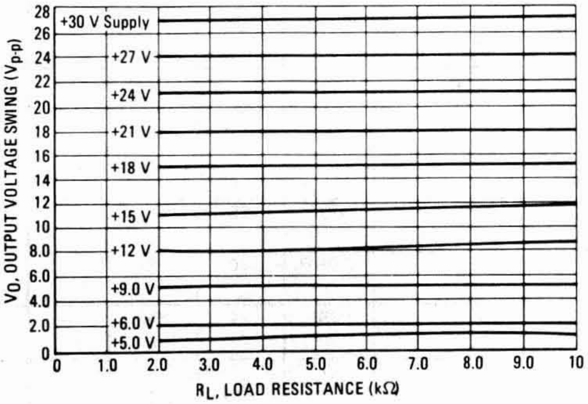


FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

FIGURE 6 — NONINVERTING PULSE RESPONSE

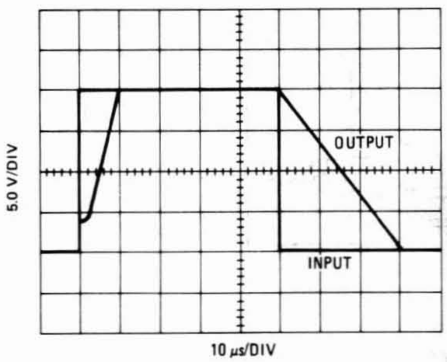
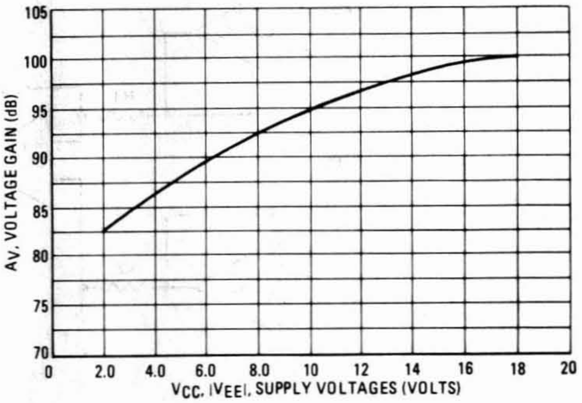
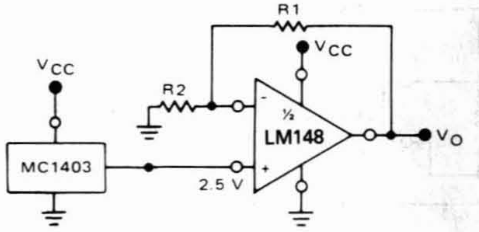


FIGURE 7 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



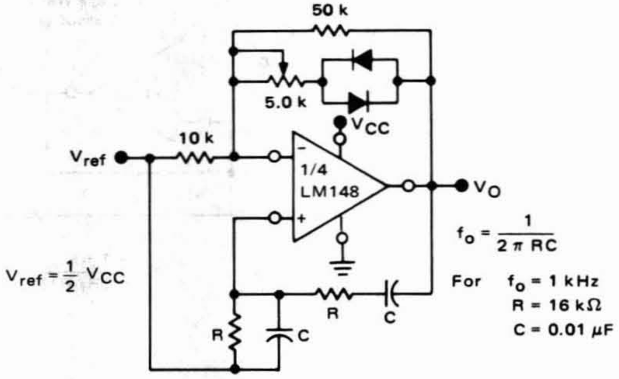
## APPLICATIONS INFORMATION

FIGURE 8 — VOLTAGE REFERENCE


VCC
MC1403
R1
R2
VCC
½
LM148
2.5 V
VO

$V_O = 2.5\ V(1 + \frac{R1}{R2})$

FIGURE 9 — WIEN BRIDGE OSCILLATOR

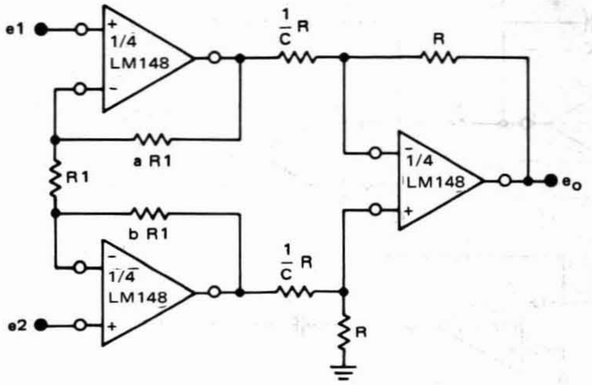

50 k
5.0 k
VCC
10 k
Vref
1/4
LM148
VO
R
C
R
C

$V_{ref} = \frac{1}{2} V_{CC}$

$f_o = \frac{1}{2 \pi RC}$

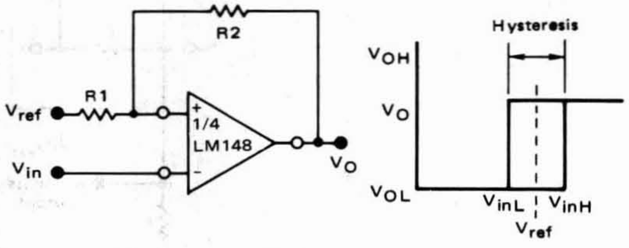
For $f_o = 1\ kHz$
$R = 16\ k\Omega$
$C = 0.01\ \mu F$

FIGURE 10 — HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


e1
1/4
LM148
$\frac{1}{C}R$
R
a R1
R1
b R1
1/4
LM148
e2
1/4
LM148
eo
$\frac{1}{C}R$
R

$e_o = C\ (1 + a + b)\ (e2 - e1)$

FIGURE 11 — COMPARATOR WITH HYSTERESIS


R2
R1
Vref
Vin
1/4
LM148
VO
Hysteresis
VOH
VO
VOL
VinL
VinH
Vref

$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$

$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$

$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$

FIGURE 12 – HIGH IMPEDANCE INSTRUMENTATION BUFFER/FILTER

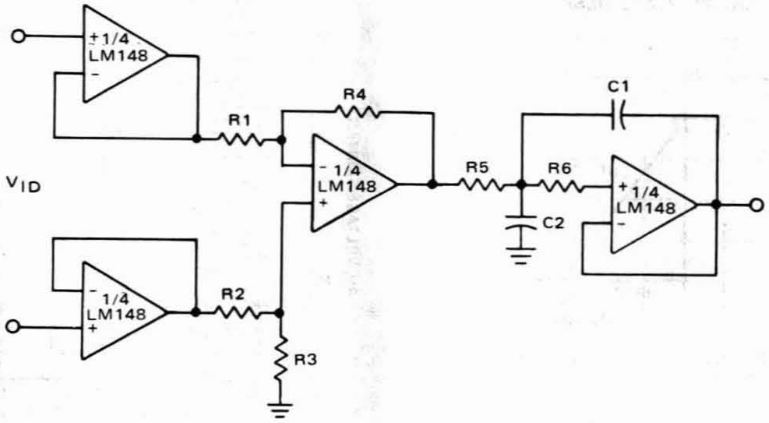
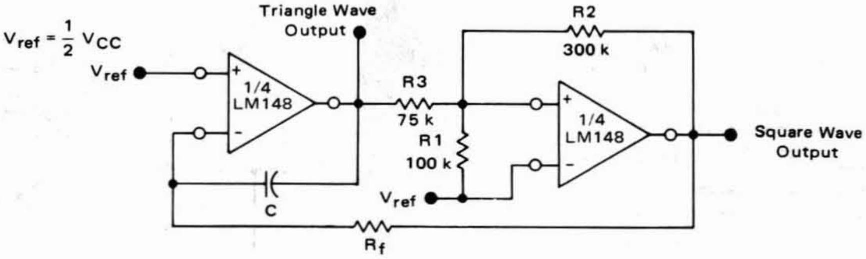

1/4 LM148
1/4 LM148
1/4 LM148
1/4 LM148
V_ID
R1
R2
R3
R4
R5
R6
C1
C2

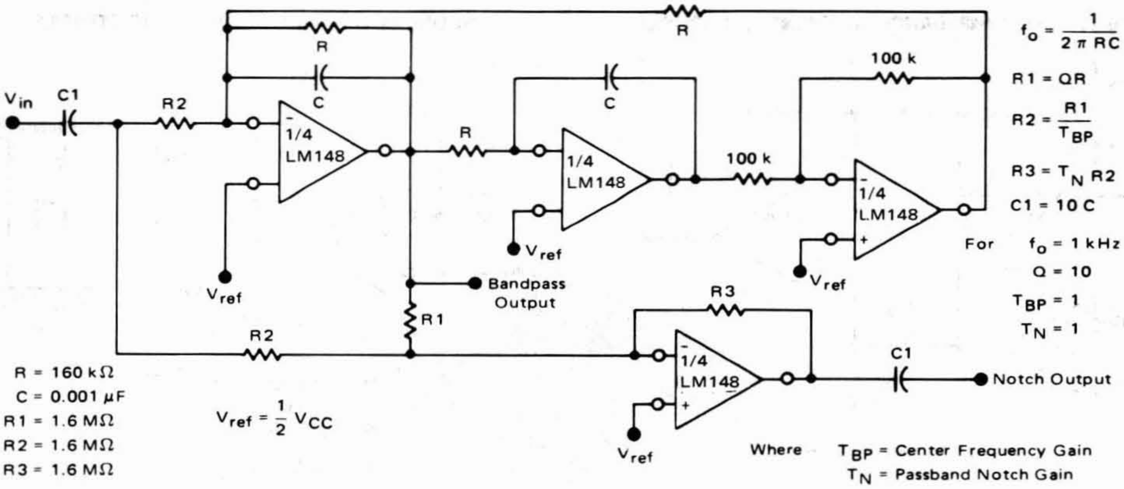
FIGURE 13 – FUNCTION GENERATOR


Triangle Wave Output
Square Wave Output
V_ref
V_ref
1/4 LM148
1/4 LM148
R2 300 k
R3 75 k
R1 100 k
C
R_f

$V_{ref} = \frac{1}{2} V_{CC}$

$f = \frac{R1 + R_C}{4\,CR_f\,R1}$ if $R3 = \frac{R2\,R1}{R2 + R1}$

FIGURE 14 – BI-QUAD FILTER


V_in
C1
R2
R
C
R
C
R
100 k
100 k
1/4 LM148
1/4 LM148
1/4 LM148
1/4 LM148
V_ref
V_ref
V_ref
V_ref
Bandpass Output
R1
R2
R3
C1
Notch Output

$f_o = \frac{1}{2\pi RC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N R2$

$C1 = 10\,C$

For $f_o = 1$ kHz

$Q = 10$

$T_{BP} = 1$

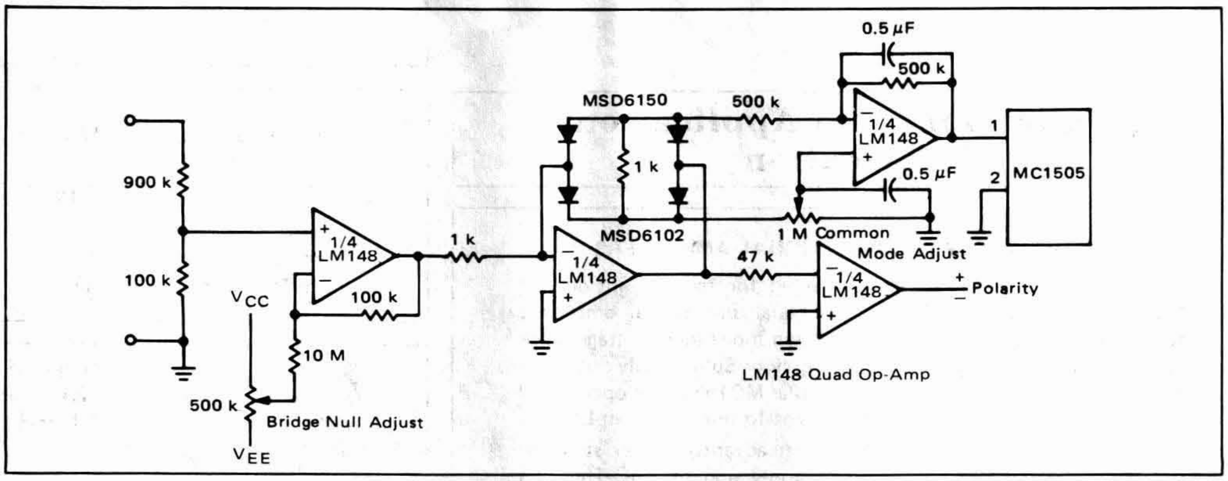
$T_N = 1$

R = 160 kΩ
C = 0.001 μF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

$V_{ref} = \frac{1}{2} V_{CC}$

Where $T_{BP}$ = Center Frequency Gain
$T_N$ = Passband Notch Gain

FIGURE 15 – ABSOLUTE VALUE DVM FRONT END


0.5 μF
500 k
MSD6150
500 k
1/4 LM148
1
MC1505
2
0.5 μF
1 k
900 k
1/4 LM148
1 k
MSD6102
1 M Common Mode Adjust
47 k
100 k
1/4 LM148
1/4 LM148
Polarity
VCC
100 k
10 M
LM148 Quad Op-Amp
500 k
Bridge Null Adjust
VEE

**MOTOROLA**

# LM158, LM258, LM358, LM2904

## Specifications and Applications Information

### DUAL LOW POWER OPERATIONAL AMPLIFIERS

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/$V_{EE}$, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The LM158 Series is equivalent to one-half of an LM124.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 32 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 32 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- Similar Performance to the Popular MC1558

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | LM158<br>LM258<br>LM358 | LM2904 | Unit |
|---|---|---|---|---|
| Power Supply Voltages<br>Single Supply<br>Split Supplies | <br>$V_{CC}$<br>$V_{CC}, V_{EE}$ | <br>32<br>±16 | <br>26<br>±13 | Vdc |
| Input Differential Voltage Range (1) | $V_{IDR}$ | ±32 | ±26 | Vdc |
| Input Common Mode Voltage Range (2) | $V_{ICR}$ | -0.3 to 32 | -0.3 to 26 | Vdc |
| Input Forward Current (3)<br>($V_I < -0.3$ V) | $I_{IF}$ | 50 | – | mA |
| Output Short Circuit Duration | $t_S$ | Continuous | | |
| Junction Temperature<br>Ceramic and Metal Packages<br>Plastic Package | $T_J$ | <br>175<br>150 | | °C |
| Storage Temperature Range<br>Ceramic and Metal Packages<br>Plastic Package | $T_{stg}$ | <br>−65 to +150<br>−55 to +125 | | °C |
| Operating Ambient Temperature Range<br>LM158<br>LM258<br>LM358<br>LM2904 | $T_A$ | <br>-55 to +125<br>-25 to +85<br>0 to +70<br>– | <br>–<br>–<br>–<br>-40 to +85 | °C |

(1) Split Power Supplies.

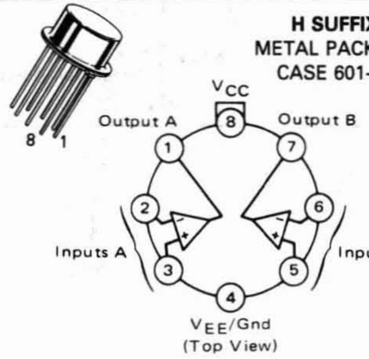
(2) For Supply Voltages less than 32 V for the LM158/258/358 and 26 V for the LM2904, the absolute maximum input voltage is equal to the supply voltage.

(3) This input current will only exist when the voltage is negative at any of the input leads. Normal output states will reestablish when the input voltage returns to a voltage greater than −0.3 V.

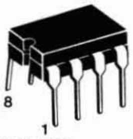
DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

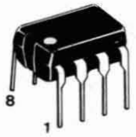
SILICON MONOLITHIC INTEGRATED CIRCUIT

**H SUFFIX**
METAL PACKAGE
CASE 601-04



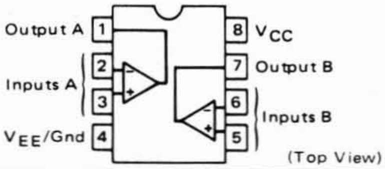
**J SUFFIX**
CERAMIC PACKAGE
CASE 693-02





**N SUFFIX**
PLASTIC PACKAGE
CASE 626-04

**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8



| ORDERING INFORMATION | | |
|---|---|---|
| **Device** | **Temperature Range** | **Package** |
| LM158H | −55 to +125°C | Metal Can |
| LM158J | | Ceramic DIP |
| LM2904D | −40 to +85°C | SO-8 |
| LM2904H | | Metal Can |
| LM2904J | | Ceramic DIP |
| LM2904N | | Plastic DIP |
| LM258D | −25 to +85°C | SO-8 |
| LM258H | | Metal Can |
| LM258J | | Ceramic DIP |
| LM258N | | Plastic DIP |
| LM358D<br>LM358H | 0 to +70°C | SO-8<br>Metal Can |
| LM358J | | Ceramic DIP |
| LM358N | | Plastic DIP |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = Gnd, $T_A$ = 25°C unless otherwise noted)

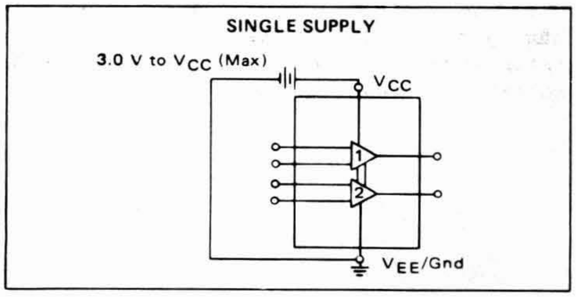
| Characteristic | Symbol | LM158/LM258 | | | LM358 | | | LM2904 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage<br>$V_{CC}$ = 5.0 V to 30 V (26 V for LM2904),<br>$V_{IC}$ = 0 V to $V_{CC}$ − 1.7 V, $V_O \simeq$ 1.4 V, $R_S$ = 0 Ω<br>$T_A$ = 25°C<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | $V_{IO}$ | –<br>– | 2.0<br>– | 5.0<br>7.0 | –<br>– | 2.0<br>– | 7.0<br>9.0 | –<br>– | 2.0<br>– | 7.0<br>10 | mV |
| Average Temperature Coefficient of Input Offset Voltage<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | $\Delta V_{IO}/\Delta T$ | – | 7.0 | – | – | 7.0 | – | – | 7.0 | – | µV/°C |
| Input Offset Current<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | $I_{IO}$ | –<br>– | 3.0<br>– | 30<br>100 | –<br>– | 5.0<br>– | 50<br>150 | –<br>– | 5.0<br>45 | 50<br>200 | nA |
| Average Temperature Coefficient of Input Offset Current<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | $\Delta I_{IO}/\Delta T$ | – | 10 | – | – | 10 | – | – | 10 | – | pA/°C |
| Input Bias Current<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | $I_{IB}$ | –<br>– | -45<br>-50 | -150<br>-300 | –<br>– | -45<br>-50 | -250<br>-500 | –<br>– | -45<br>-50 | -250<br>-500 | nA |
| Input Common-Mode Voltage Range (Note 2)<br>$V_{CC}$ = 30 V (26 V for LM2904)<br>$V_{CC}$ = 30 V (26 V for LM2904), $T_A$ = $T_{high}$ to $T_{low}$ | $V_{ICR}$ | 0<br>0 | –<br>– | 28.3<br>28 | 0<br>0 | –<br>– | 28.3<br>28 | 0<br>0 | –<br>– | 24.3<br>24 | V |
| Differential Input Voltage Range | $V_{IDR}$ | – | – | $V_{CC}$ | – | – | $V_{CC}$ | – | – | $V_{CC}$ | V |
| Large Signal Open-Loop Voltage Gain<br>$R_L$ = 2.0 kΩ, $V_{CC}$ = 15 V, For Large $V_O$ Swing,<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | $A_{VOL}$ | 50<br>25 | 100<br>– | –<br>– | 25<br>15 | 100<br>– | –<br>– | –<br>– | 100<br>– | –<br>– | V/mV |
| Channel Separation<br>1.0 kHz ⩽ f ⩽ 20 kHz, Input Referenced | – | – | -120 | – | – | -120 | – | – | -120 | – | dB |
| Common-Mode Rejection Ratio<br>$R_S$ ⩽ 10 kΩ | CMRR | 70 | 85 | – | 65 | 70 | – | 50 | 70 | – | dB |
| Power Supply Rejection Ratio | PSRR | 65 | 100 | – | 65 | 100 | – | 50 | 100 | – | dB |
| Output Voltage Range<br>$R_L$ = 2 kΩ ($R_L$ ⩾ 10 kΩ for LM2904) | $V_{OR}$ | 0 | – | 3.3 | 0 | – | 3.3 | 0 | – | 3.3 | V |
| Output Voltage–High Limit ($T_A$ = $T_{high}$ to $T_{low}$)(Note 1)<br>$V_{CC}$ = 30 V (26 V for LM2904), $R_L$ = 2 kΩ<br>$V_{CC}$ = 30 V (26 V for LM2904), $R_L$ = 10 kΩ | $V_{OH}$ | 26<br>27 | –<br>28 | –<br>– | 26<br>27 | –<br>28 | –<br>– | 22<br>23 | –<br>24 | –<br>– | V |
| Output Voltage–Low Limit<br>$V_{CC}$ = 5.0 V, $R_L$ = 10 kΩ, $T_A$ = $T_{high}$ to $T_{low}$ (Note 1) | $V_{OL}$ | – | 5.0 | 20 | – | 5.0 | 20 | – | 5.0 | 20 | mV |
| Output Source Current<br>$V_{ID}$ = +1.0 V, $V_{CC}$ = 15 V | $I_{O+}$ | 20 | 40 | – | 20 | 40 | – | 20 | 40 | – | mA |
| Output Sink Current<br>$V_{ID}$ = -1.0 V, $V_{CC}$ = 15 V<br>$V_{ID}$ = -1.0 V, $V_O$ = 200 mV | $I_{O-}$ | 10<br>12 | 20<br>50 | –<br>– | 10<br>12 | 20<br>50 | –<br>– | 10<br>– | 20<br>– | –<br>– | mA<br>µA |
| Output Short Circuit to Ground (Note 3) | $I_{os}$ | – | 40 | 60 | – | 40 | 60 | – | 40 | 60 | mA |
| Power Supply Current ($T_A$ = $T_{high}$ to $T_{low}$)(Note 1)<br>$V_{CC}$ = 30 V (26 V for LM2904), $V_O$ = 0 V, $R_L$ = ∞<br>$V_{CC}$ = 5 V, $V_O$ = 0 V, $R_L$ = ∞ | $I_{CC}$ | –<br>– | 1.5<br>0.7 | 3.0<br>1.2 | –<br>– | 1.5<br>0.7 | 3.0<br>1.2 | –<br>– | 1.5<br>0.7 | 3.0<br>1.2 | mA |

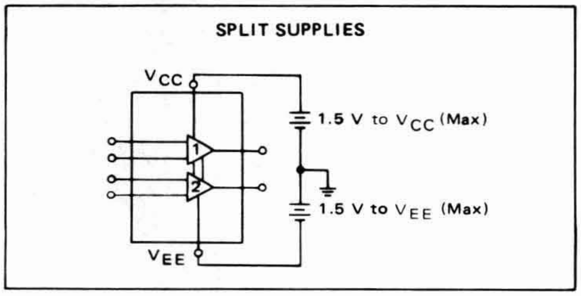
**NOTES:**

(1) $T_{low}$ = -55°C for LM158 $T_{high}$ = +125°C for LM158
= -40°C for LM2904 = +85°C for LM2904
= -25°C for LM258 and LM258
= 0°C for LM358 = +70°C for LM358

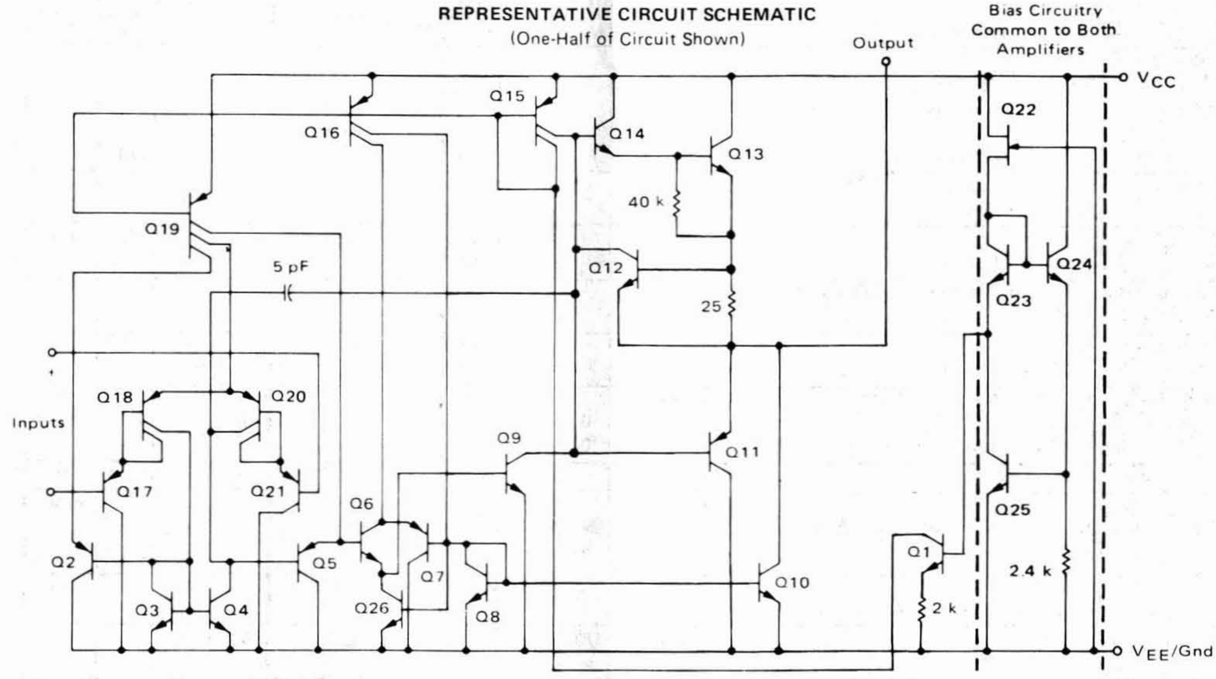
(2) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC}$ -1.7 V, but either or both inputs can go to +32 V without damage (+26 V for LM2904).

(3) Short circuits from the output to $V_{CC}$ can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

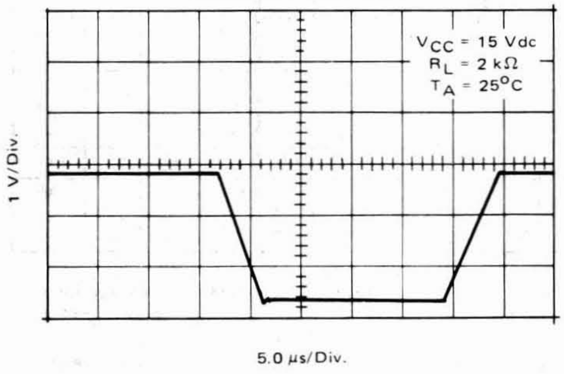




**REPRESENTATIVE CIRCUIT SCHEMATIC**
(One-Half of Circuit Shown)


Bias Circuitry Common to Both Amplifiers
Output
VCC
Q15
Q16
Q14
Q13
Q22
40 k
Q19
5 pF
Q12
Q24
25
Q23
+
Inputs
Q18
Q20
Q9
Q11
Q17
Q21
Q6
Q25
Q1
Q2
Q5
Q7
Q10
2.4 k
Q3
Q4
Q26
Q8
2 k
VEE/Gnd

**LARGE SIGNAL VOLTAGE FOLLOWER RESPONSE**



### CIRCUIT DESCRIPTION

The LM158 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

## TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

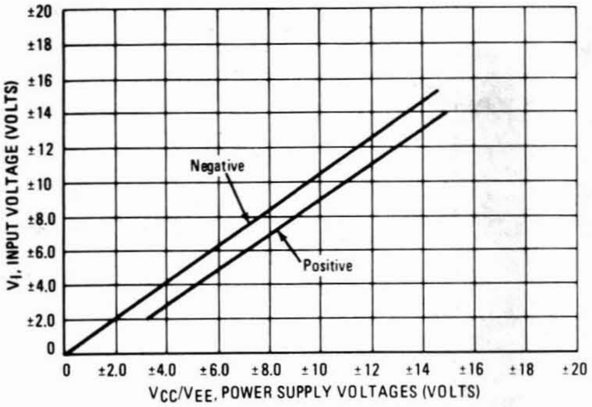


FIGURE 2 – OPEN LOOP FREQUENCY

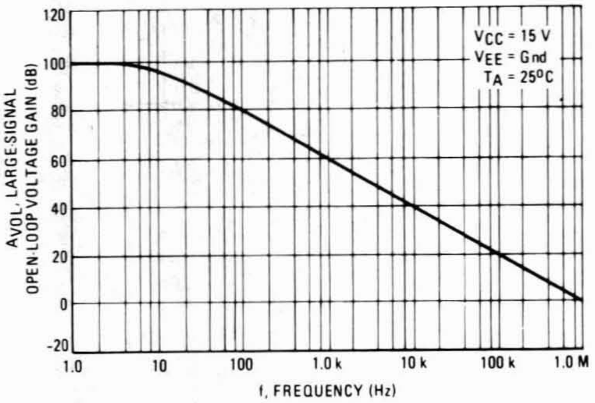


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

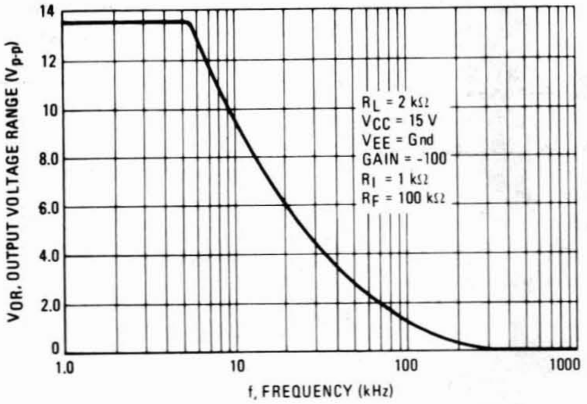


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE (Non-Inverting)

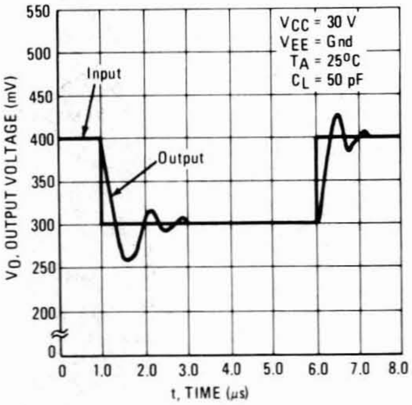


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

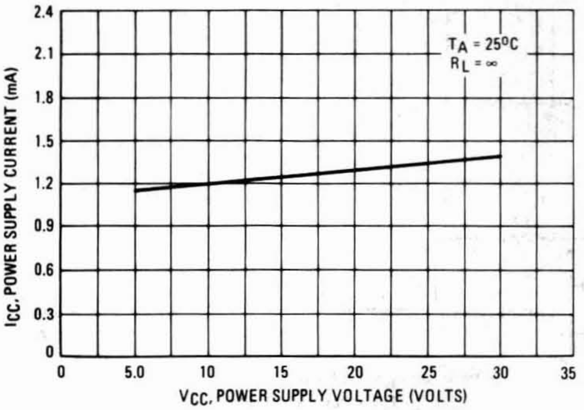
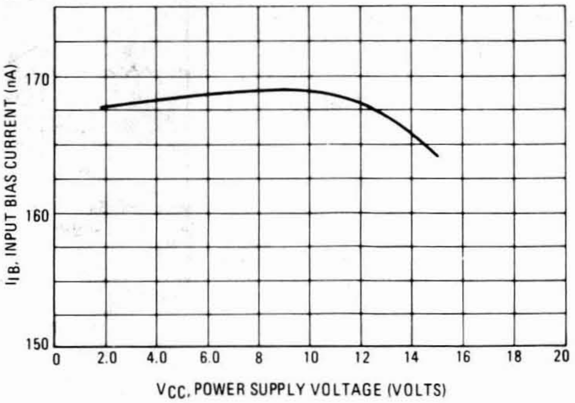
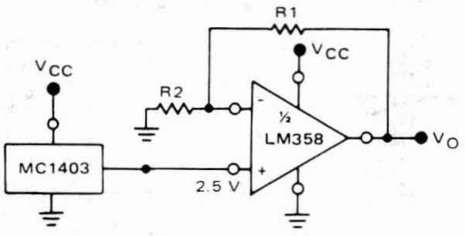


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



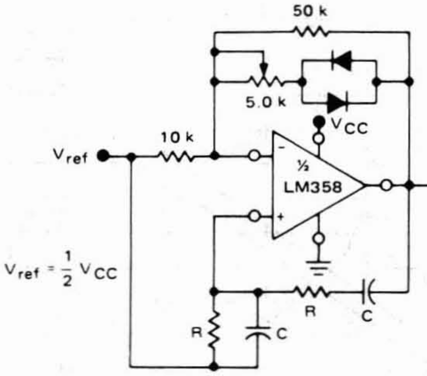
## APPLICATIONS INFORMATION

### FIGURE 7 – VOLTAGE REFERENCE


R1
VCC
VCC
R2
½
LM358
MC1403
2.5 V
VO

$V_O = 2.5\ V(1 + \frac{R1}{R2})$

### FIGURE 8 – WIEN BRIDGE OSCILLATOR

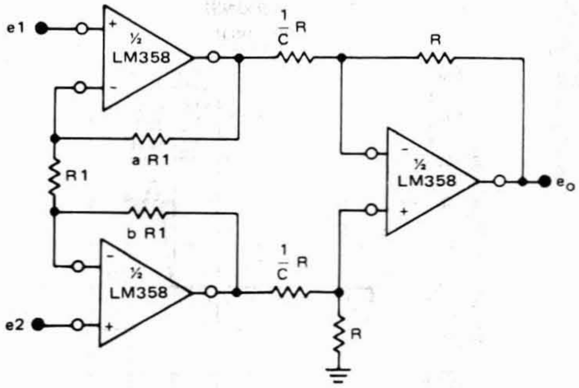

50 k
5.0 k
VCC
10 k
Vref
½
LM358
VO
R
C
R
C

$V_{ref} = \frac{1}{2} V_{CC}$

$f_o = \frac{1}{2 \pi RC}$

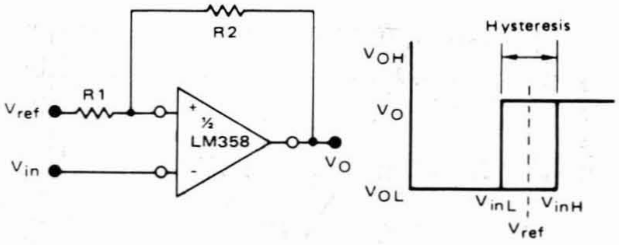
For $f_o = 1\ kHz$
$R = 16\ k\Omega$
$C = 0.01\ \mu F$

### FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


e1
½
LM358
1/C R
R
a R1
R1
b R1
½
LM358
eo
½
LM358
1/C R
e2
R

$e_o = C\ (1 + a + b)\ (e2 - e1)$

### FIGURE 10 – COMPARATOR WITH HYSTERESIS

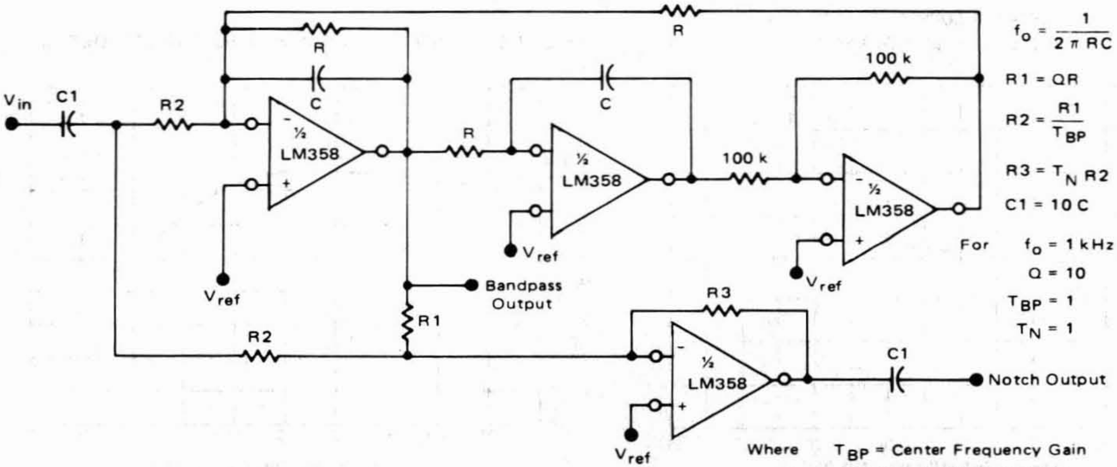

R2
R1
Vref
Vin
½
LM358
VO
Hysteresis
VOH
VO
VOL
VinL
VinH
Vref

$V_{inL} = \frac{R1}{R1 + R2}(V_{OL} - V_{ref}) + V_{ref}$

$V_{inH} = \frac{R1}{R1 + R2}(V_{OH} - V_{ref}) + V_{ref}$

$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$

### FIGURE 11 – BI-QUAD FILTER


R
R
C
Vin
C1
R2
½
LM358
Vref
R
C
½
LM358
Vref
100 k
100 k
½
LM358
Vref
Bandpass Output
R1
R2
R3
½
LM358
C1
Notch Output
Vref

$f_o = \frac{1}{2 \pi RC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N\ R2$

$C1 = 10\ C$

$V_{ref} = \frac{1}{2} V_{CC}$

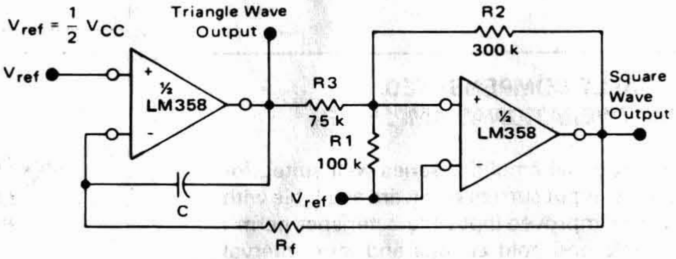
For $f_o = 1\ kHz$
$Q = 10$
$T_{BP} = 1$
$T_N = 1$

$R = 160\ k\Omega$
$C = 0.001\ \mu F$
$R1 = 1.6\ M\Omega$
$R2 = 1.6\ M\Omega$
$R3 = 1.6\ M\Omega$

Where $T_{BP}$ = Center Frequency Gain
$T_N$ = Passband Notch Gain

## APPLICATIONS INFORMATION (continued)

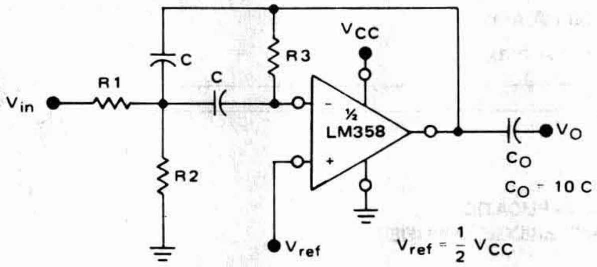
### FIGURE 12 – FUNCTION GENERATOR



Vref = 1/2 VCC
Triangle Wave Output
R2
300 k
Vref
½ LM358
R3
75 k
R1
100 k
½ LM358
Square Wave Output
C
Vref
Rf

$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\,R1}{R2 + R1}.$$

### FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



VCC
C
R3
R1
C
Vin
½ LM358
Vo
R2
Co
Co = 10 C
Vref
Vref = 1/2 VCC

Given $f_o$ = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value $f_o$, C
Then:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier

$\frac{Q_o f_o}{BW} < 0.1$ Where $f_o$ and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

**MOTOROLA**

# LM307

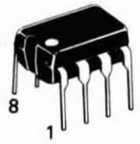
## INTERNALLY COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER

A general purpose operational amplifier series well suited for applications requiring lower input currents than are available with the popular MC1741. These improved input characteristics permit greater accuracy in sample and hold circuits and long interval integrators.

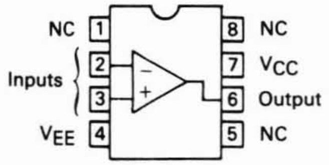
- Internally Compensated
- Low Offset Voltage: 7.5 mV max
- Low Input Offset Current: 50 nA max
- Low Input Bias Current: 250 nA max

## OPERATIONAL AMPLIFIER

### SILICON MONOLITHIC INTEGRATED CIRCUIT



**N SUFFIX**
PLASTIC PACKAGE
CASE 626-04

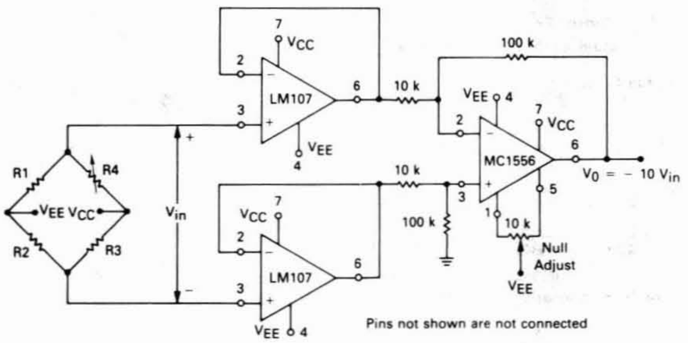

NC 1
Inputs 2
3
VEE 4
8 NC
7 VCC
6 Output
5 NC
−
+

(Top View)

### ORDERING INFORMATION

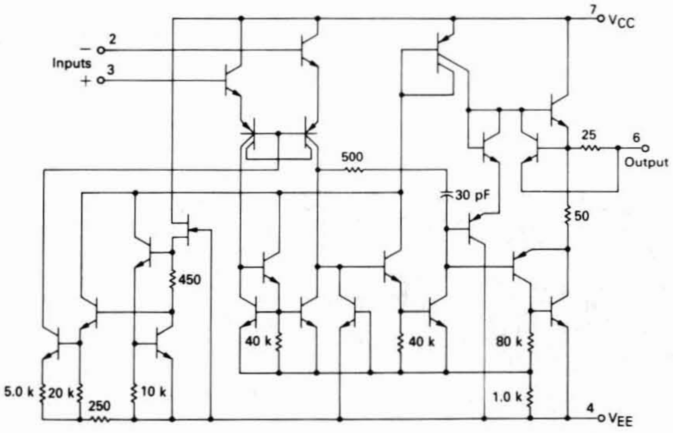
| Device | Temperature Range | Package |
|---|---|---|
| LM307N | 0°C to +70°C | Plastic DIP |

### TYPICAL APPLICATION HIGH IMPEDANCE BRIDGE AMPLIFIER

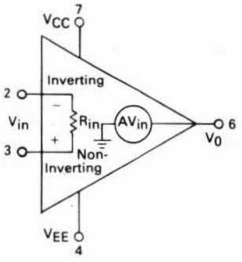

7
VCC
2
LM107
6
3
VEE
4
10 k
100 k
VEE 4
7
VCC
2
MC1556
6
3
5
1
10 k
Null Adjust
VEE
Vo = − 10 Vin
10 k
100 k
VCC
7
2
LM107
6
3
VEE 4
R1
R4
R2
R3
VEE VCC
Vin
+
−

Pins not shown are not connected

### CIRCUIT SCHEMATIC


− 2
Inputs
+ 3
7 VCC
500
25
6 Output
30 pF
50
450
40 k
40 k
80 k
5.0 k
20 k
250
10 k
1.0 k
4 VEE

### EQUIVALENT CIRCUIT


VCC 7
Inverting
2
Vin
3
−
+
Rin
AVin
Non-Inverting
6
Vo
VEE 4

Pins 1, 5, and 8 no connection.

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | LM307 | Unit |
|---|---|---|---|
| Power Supply Voltages | $V_{CC}$<br>$V_{EE}$ | +18<br>−18 | Vdc |
| Differential Input Signal Voltage | $V_{ID}$ | ±30 | Volts |
| Common-Mode Input Swing (Note 1) | $V_{ICR}$ | ±15 | Volts |
| Output Short-Circuit Duration | $t_s$ | Indefinite | |
| Power Dissipation (Package Limitation) (Note 2) | $P_D$ | 500 | mW |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = +25°C unless otherwise noted, see Note 3.)

| Characteristics | Symbol | LM307 Min | LM307 Typ | LM307 Max | Unit |
|---|---|---|---|---|---|
| Input Offset Voltage<br>$R_S \leq 50$ kΩ, $T_A$ = +25°C<br>$R_S \leq 50$ kΩ, $T_A = T_{low}$ to $T_{high}$ | $V_{IO}$ | —<br>— | 2.0<br>— | 7.5<br>10 | mV |
| Input Offset Current<br>$T_A$ = +25°C<br>$T_A = T_{low}$ to $T_{high}$ | $I_{IO}$ | —<br>— | 3.0<br>— | 50<br>70 | nA |
| Input Bias Current<br>$T_A$ = +25°C<br>$T_A = T_{low}$ to $T_{high}$ | $I_{IB}$ | —<br>— | 70<br>— | 250<br>300 | nA |
| Input Resistance | $r_i$ | 0.5 | 2.0 | — | MΩ |
| Supply Current<br>$V_S = \pm 15$ V, $T_A$ = +25°C | $I_D$ | — | 1.8 | 3.0 | mA |
| Large-Signal Voltage Gain<br>$V_S = \pm 15$ V, $V_O = \pm 10$ V, $R_L > 2.0$ kΩ, $T_A$ = +25°C<br>$V_S = \pm 15$ V, $V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ, $T_A = T_{low}$ | $A_v$ | 25<br>15 | 160<br>— | —<br>— | V/mV |
| Average Temperature Coefficient of Input Offset Voltage<br>$T_{low} \leq T_A \leq T_{high}$ | $TCV_{IO}$ | — | 6.0 | 30 | µV/°C |
| Average Temperature Coefficient of Input Offset Current<br>$+25°C \leq T_A \leq T_{high}$<br>$T_{low} \leq T_A \leq +25°C$ | $TCI_{IO}$ | —<br>— | 0.01<br>0.02 | 0.3<br>0.6 | nA/°C |
| Output Voltage Swing ($T_A = T_{low}$ to $T_{high}$)<br>$V_S = \pm 15$ V, $R_L$ = 10 kΩ<br>$R_L$ = 2.0 kΩ | $V_O$ | ±12<br>±10 | +14<br>±13 | —<br>— | V |
| Input Voltage Range ($T_A = T_{low}$ to $T_{high}$)<br>$V_S = \pm 15$ V | $V_{ICR}$ | ±12 | — | — | V |
| Common-Mode Rejection Ratio ($T_A = T_{low}$ to $T_{high}$)<br>$R_S \leq 50$ kΩ | CMRR | 70 | 90 | — | dB |
| Supply-Voltage Rejection Ratio ($T_A = T_{low}$ to $T_{high}$)<br>$R_S \leq 50$ kΩ | PSRR | 70 | 96 | — | dB |

Symbols conform to JEDEC Engineering Bulletin No. 1 when applicable.

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. For operating at elevated temperatures, the device must be derated based on a maximum junction temperature of 100°C for the LM307. The H package is derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

Note 3. Unless otherwise noted, these specifications apply for: $\pm 5.0\text{ V} \leq V_{CC}/V_{EE} \leq \pm 15$ V, $T_{low}$ = 0°C, $T_{high}$ = +70°C

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C unless otherwise noted.)

**FIGURE 1 — MINIMUM INPUT VOLTAGE RANGE**

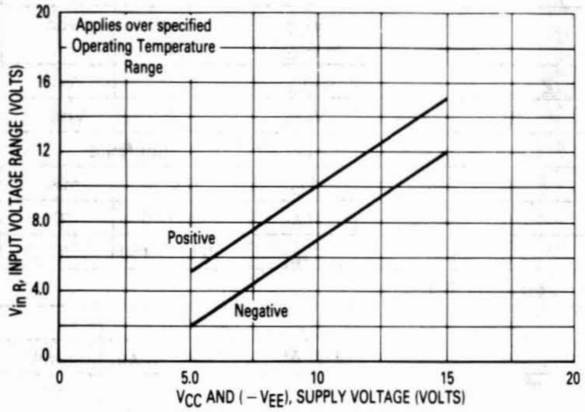


**FIGURE 2 — MINIMUM OUTPUT VOLTAGE SWING**

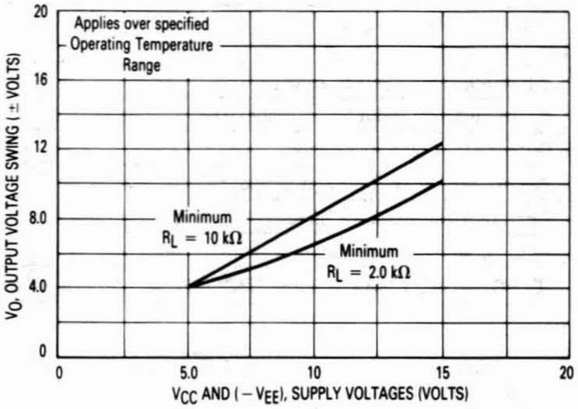


**FIGURE 3 — MINIMUM VOLTAGE GAIN**

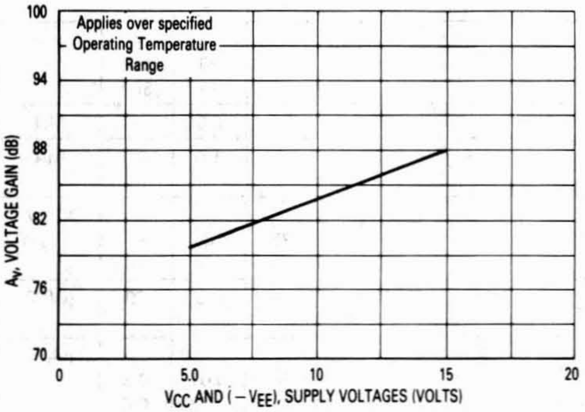


**FIGURE 4 — TYPICAL SUPPLY CURRENTS**

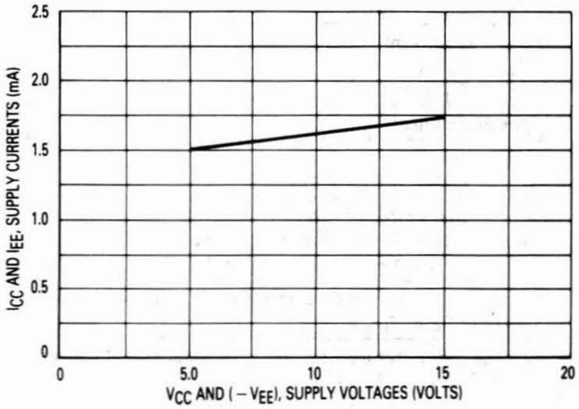


**FIGURE 5 — OPEN-LOOP FREQUENCY RESPONSE**

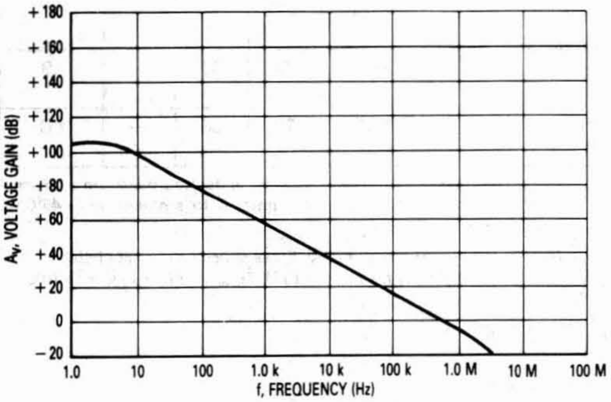
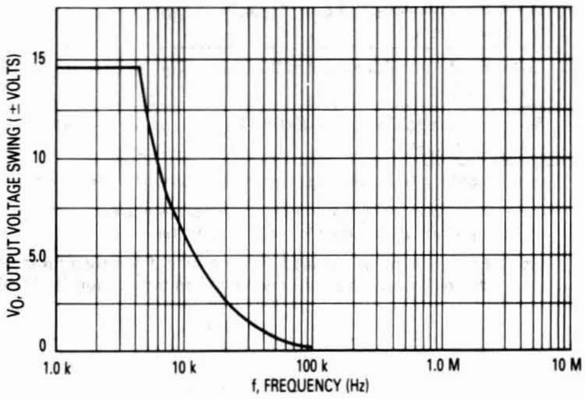
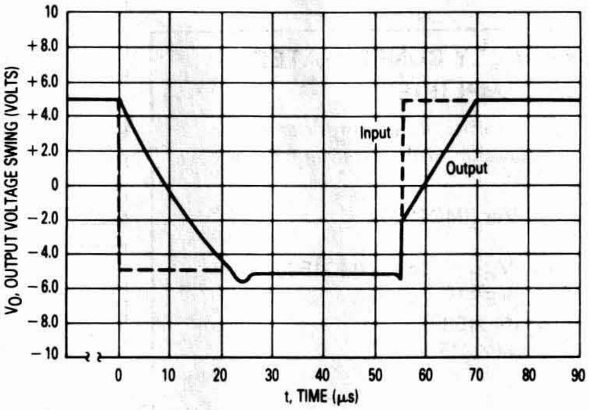


**FIGURE 6 — LARGE-SIGNAL FREQUENCY RESPONSE**



## TYPICAL CHARACTERISTICS (continued)

### FIGURE 7 — VOLTAGE FOLLOWER PULSE RESPONSE



**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1436CD | 0°C to +70°C | SO-8 |
| MC1436D | 0°C to +70°C | SO-8 |
| MC1436P1 | 0°C to +70°C | Plastic DIP |
| MC1436CP1 | 0°C to +70°C | Plastic DIP |
| MC1436G | 0°C to +70°C | Metal Can |
| MC1436U | 0°C to +70°C | Ceramic DIP |
| MC1436CG | 0°C to +70°C | Metal Can |
| MC1436CU | 0°C to +70°C | Ceramic DIP |
| MC1536G | −55°C to +125°C | Metal Can |
| MC1536U | −55°C to +125°C | Ceramic DIP |

# MC1436
# MC1436C
# MC1536

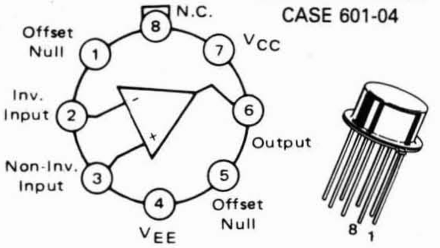
## HIGH VOLTAGE, INTERNALLY COMPENSATED OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Maximum Supply Voltage – ± 40 Vdc (MC1536)
- Output Voltage Swing –
  $\pm 30\ V_{pk(min)}$ ($V_{CC}$ = +36 V, $V_{EE}$ = -36 V) (MC1536)
  $\pm 22\ V_{pk(min)}$ ($V_{CC}$ = +28 V, $V_{EE}$ = -28 V)
- Input Bias Current – 20 nA max (MC1536)
- Input Offset Current – 3.0 nA max (MC1536)
- Fast Slew Rate – 2.0 V/μs typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Over-Voltage Protection
- $A_{VOL}$ – 500,000 typ
- Characteristics Independent of Power Supply Voltages – (± 5.0 Vdc to ± 36 Vdc)

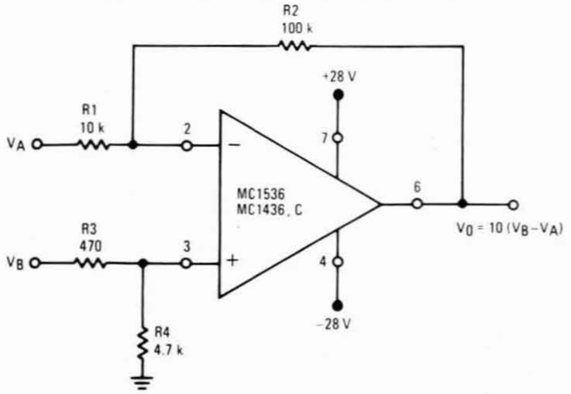
## OPERATIONAL AMPLIFIER

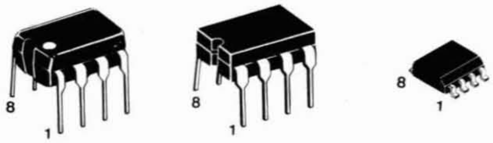
**SILICON MONOLITHIC INTEGRATED CIRCUIT**


N.C.
Offset Null
Vcc
Inv. Input
Output
Non-Inv. Input
Offset Null
VEE
8
1

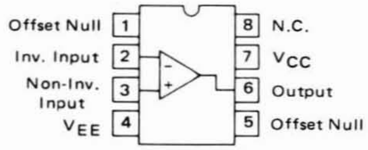
**G SUFFIX**
METAL PACKAGE
CASE 601-04

### FIGURE 1 — DIFFERENTIAL AMPLIFIER WITH ± 20 V COMMON-MODE INPUT VOLTAGE RANGE

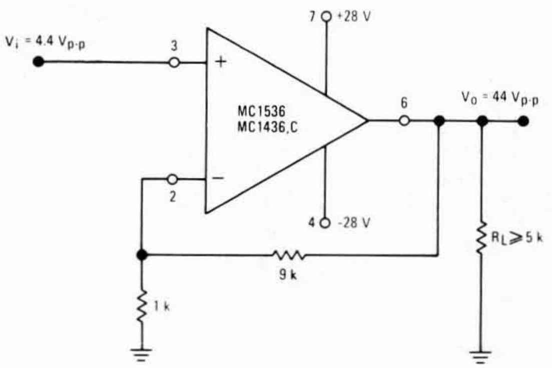

R2
100 k
+28 V
R1
10 k
VA
2
7
MC1536
MC1436, C
6
R3
470
VB
3
4
V0 = 10 (VB−VA)
R4
4.7 k
−28 V



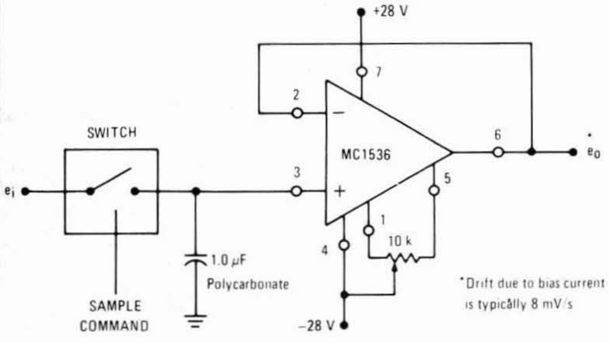
| P1 SUFFIX | U SUFFIX | D SUFFIX |
|---|---|---|
| PLASTIC PACKAGE | CERAMIC PACKAGE | PLASTIC PACKAGE |
| CASE 626-04 | CASE 693-02 | CASE 751-01 |
|  |  | SO-8 |


Offset Null 1
Inv. Input 2
Non-Inv. Input 3
VEE 4
8 N.C.
7 VCC
6 Output
5 Offset Null

### FIGURE 2 — TYPICAL NONINVERTING X10 VOLTAGE AMPLIFIER


Vi = 4.4 Vp-p
3
7
+28 V
MC1536
MC1436,C
6
V0 = 44 Vp-p
2
4
-28 V
RL≥5 k
9 k
1 k

### FIGURE 3 — LOW-DRIFT SAMPLE AND HOLD


+28 V
7
2
SWITCH
6
ei
MC1536
e0
3
5
1
10 k
4
1.0 μF
Polycarbonate
SAMPLE COMMAND
-28 V

*Drift due to bias current is typically 8 mV/s

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | MC1536 | MC1436 | MC1436C | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +40<br>-40 | +34<br>-34 | +30<br>-30 | Vdc |
| Input Differential Voltage Range | $V_{IDR}$ | Note 3 | | | Volts |
| Input Common-Mode Voltage Range | $V_{ICR}$ | Note 3 | | | Volts |
| Output Short Circuit Duration ($V_{CC} = V_{EE} = 28$ Vdc, $V_o = 0$) | $t_S$ | 5.0 | | | s |
| Power Dissipation (Package Limitation)<br>Derate above $T_A$ = +25°C | $P_D$ | 680<br>4.6 | | | mW<br>mW/°C |
| Operating Ambient Temperature Range | $T_A$ | -55 to +125 | 0 to +70 | | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | | | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +28 Vdc, $V_{EE}$ = -28 Vdc, $T_A$ = +25°C unless otherwise noted)

| Characteristics | Symbol | MC1536 | | | MC1436 | | | MC1436C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | $I_{IB}$ | | | | | | | | | | nAdc |
| $T_A$ = +25°C | | – | 8.0 | 20 | – | 15 | 40 | – | 25 | 90 | |
| $T_A = T_{low}$ to $T_{high}$ (See Note 1) | | – | – | 35 | – | – | 55 | – | – | – | |
| Input Offset Current | $I_{IO}$ | | | | | | | | | | nAdc |
| $T_A$ = +25°C | | – | 1.0 | 3.0 | – | 5.0 | 10 | – | 10 | 25 | |
| $T_A$ = +25°C to $T_{high}$ | | – | – | 4.5 | – | – | 14 | – | – | – | |
| $T_A = T_{low}$ to +25°C | | – | – | 7.0 | – | – | 14 | – | – | – | |
| Input Offset Voltage | $V_{IO}$ | | | | | | | | | | mVdc |
| $T_A$ = +25°C | | – | 2.0 | 5.0 | – | 5.0 | 10 | – | 5.0 | 12 | |
| $T_A = T_{low}$ to $T_{high}$ | | – | – | 7.0 | – | – | 14 | – | – | – | |
| Differential Input Impedance (Open-Loop, f ≤ 5.0 Hz) | | | | | | | | | | | |
| Parallel Input Resistance | $r_P$ | – | 10 | – | – | 10 | – | – | 10 | – | Meg ohms |
| Parallel Input Capacitance | $C_P$ | – | 2.0 | – | – | 2.0 | – | – | 2.0 | – | pF |
| Common-Mode Input Impedance (f ≤ 5.0 Hz) | $z_{ic}$ | – | 250 | – | – | 250 | | – | 250 | – | Meg ohms |
| Input Common-Mode Voltage Range | $V_{ICR}$ | ±24 | ±25 | – | ±22 | ±25 | – | ±18 | ±20 | – | $V_{pk}$ |
| **Equivalent Input Noise Voltage** | $e_n$ | | | | | | | | | | nV/(Hz)½ |
| ($A_V$ = 100, $R_s$ = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz) | | – | 50 | – | – | 50 | – | – | 50 | – | |
| Common-Mode Rejection Ratio (dc) | CMRR | 80 | 110 | – | 70 | 110 | – | 50 | 90 | – | dB |
| **Large Signal dc Open Loop Voltage Gain** | $A_{VOL}$ | | | | | | | | | | V/V |
| ($V_o$ = ± 10 V, $R_L$ = 100 k ohms) $T_A$ = +25°C | | 100,000 | 500,000 | – | 70,000 | 500,000 | – | 50,000 | 500,000 | – | |
| ($V_o$ = ± 10 V, $R_L$ = 100 k ohms) $T_A = T_{low}$ to $T_{high}$ | | 50,000 | – | – | 50,000 | – | – | – | – | – | |
| ($V_o$ = ±10 V, $R_L$ = 10 k ohms, $T_A$ = +25°C) | | – | 200,000 | – | – | 200,000 | – | – | 200,000 | – | |
| Power Bandwidth (Voltage Follower) | $BW_P$ | | | | | | | | | | kHz |
| ($A_V$ = 1, $R_L$ = 5.0 k ohms, THD ≤ 5%, $V_o$ = 40 Vp-p) | | – | 23 | – | – | 23 | – | – | 23 | – | |
| Unity Gain Crossover Frequency (open-loop) | $f_c$ | – | 1.0 | – | – | 1.0 | – | – | 1.0 | – | MHz |
| Phase Margin (open-loop, unity gain) | $\phi m$ | – | 50 | | – | 50 | – | – | 50 | – | degrees |
| Gain Margin | $A_M$ | – | 18 | – | – | 18 | – | – | 18 | – | dB |
| Slew Rate (Unity Gain) | SR | – | 2.0 | – | – | 2.0 | – | – | 2.0 | – | V/µs |
| Output Impedance (f ≤ 5.0 Hz) | $z_o$ | – | 1.0 | – | – | 1.0 | – | – | 1.0 | – | k ohms |
| Short-Circuit Output Current | $I_{OS}$ | – | ±17 | – | – | ±17 | – | – | ±19 | – | mAdc |
| Output Voltage Range ($R_L$ = 5.0 k ohms) | $V_{OR}$ | | | | | | | | | | $V_{pk}$ |
| $V_{CC}$ = +28 Vdc, $V_{EE}$ = -28 Vdc | | ±22 | ±23 | – | ±20 | ±22 | – | ±20 | ±22 | – | |
| $V_{CC}$ = +36 Vdc, $V_{EE}$ = -36 Vdc | | ±30 | ±32 | – | – | – | – | – | – | – | |
| **Power Supply Sensitivity (dc)** | | | | | | | | | | | µV/V |
| $V_{EE}$ = constant, $R_s$ ≤ 10 k ohms | PSS+ | – | 15 | 100 | – | 35 | 200 | – | 50 | – | |
| $V_{CC}$ = constant, $R_s$ ≤ 10 k ohms | PSS- | – | 15 | 100 | – | 35 | 200 | – | 50 | | |
| Power Supply Current (See Note 2) | $I_{CC}$ | – | 2.2 | 4.0 | – | 2.6 | 5.0 | – | 2.6 | 5.0 | mAdc |
| | $I_{EE}$ | – | 2.2 | 4.0 | – | 2.6 | 5.0 | – | 2.6 | 5.0 | |
| DC Quiescent Power Consumption | $P_C$ | | | | | | | | | | mW |
| ($V_o$ = 0) | | – | 124 | 224 | – | 146 | 280 | – | 146 | 280 | |

Note 1: $T_{low}$: 0°C for MC1436,C
-55°C for MC1536
$T_{high}$: +70°C for MC1436,C
+125°C for MC1536

Note 2: $V_{CC} = V_{EE}$ = 5.0 Vdc to 36 Vdc for MC1536
$V_{CC} = V_{EE}$ = 5.0 Vdc to 30 Vdc for MC1436
$V_{CC} = V_{EE}$ = 5.0 Vdc to 28 Vdc for MC1436C

Note 3: Either or both input voltages must not exceed the magnitude of $V_{CC}$ or $V_{EE}$ +3.0 volts.

FIGURE 4 – POWER BANDWIDTH

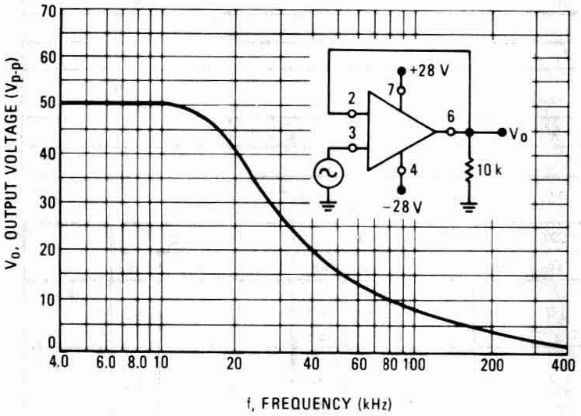


FIGURE 5 – PEAK OUTPUT VOLTAGE SWING versus POWER SUPPLY VOLTAGE

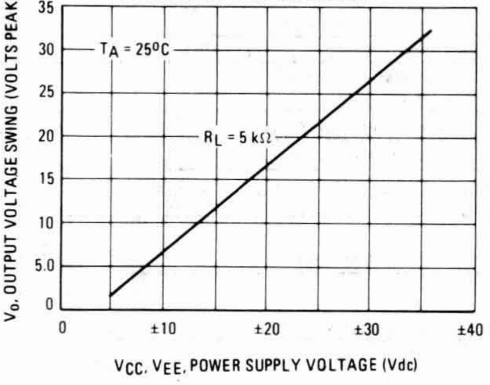


FIGURE 6 – OPEN-LOOP FREQUENCY RESPONSE

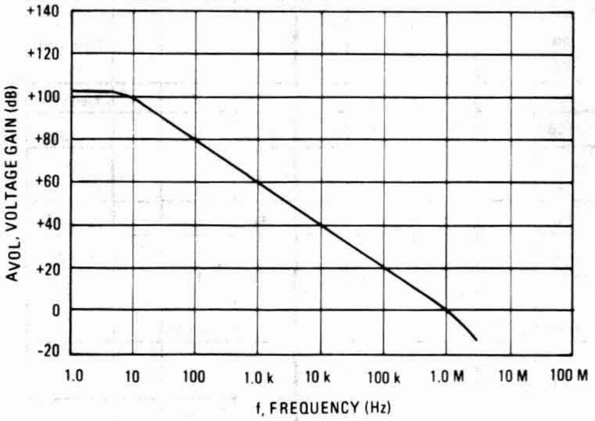


FIGURE 7 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

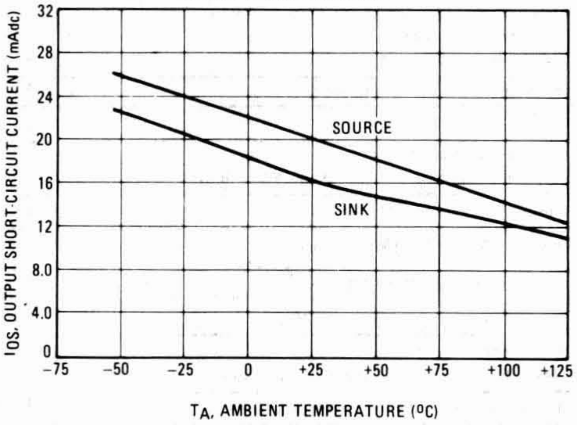


FIGURE 8 – INPUT BIAS CURRENT versus TEMPERATURE

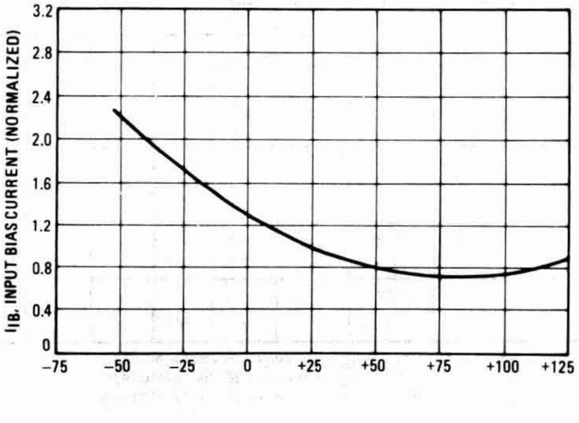


FIGURE 9 – INVERTING FEEDBACK MODEL

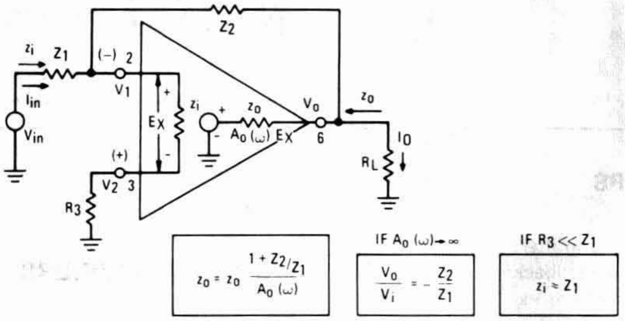

Z2
zi
Z1
(−) 2
Iin
V1
Vin
EX
zi
zo
Ao (ω) EX
Vo
6
zo
Io
RL
(+)
V2 3
R3
$z_o = z_o \frac{1 + Z_2/Z_1}{A_o(\omega)}$
IF Ao (ω)→∞
$\frac{V_o}{V_i} = -\frac{Z_2}{Z_1}$
IF R3 << Z1
$z_i \approx Z_1$

FIGURE 10 – NON-INVERTING FEEDBACK MODEL

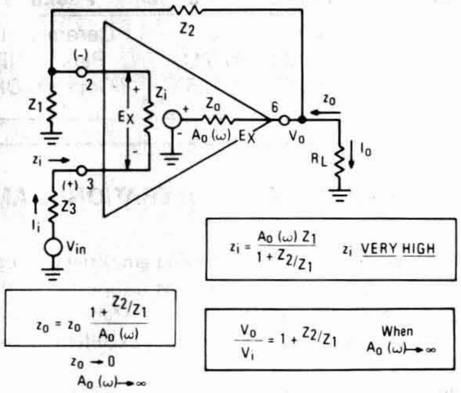

Z2
(−)
2
Z1
EX
Zi
Zo
Ao (ω) EX
6
zo
Vo
RL
Io
zi
(+) 3
Z3
Ii
Vin
$z_i = \frac{A_o(\omega) Z_1}{1 + Z_2/Z_1}$
zi VERY HIGH
$z_o = z_o \frac{1 + Z_2/Z_1}{A_o(\omega)}$
zo → 0
Ao (ω)→∞
$\frac{V_o}{V_i} = 1 + Z_2/Z_1$
When Ao (ω)→∞

FIGURE 11 – AUDIO AMPLIFIER

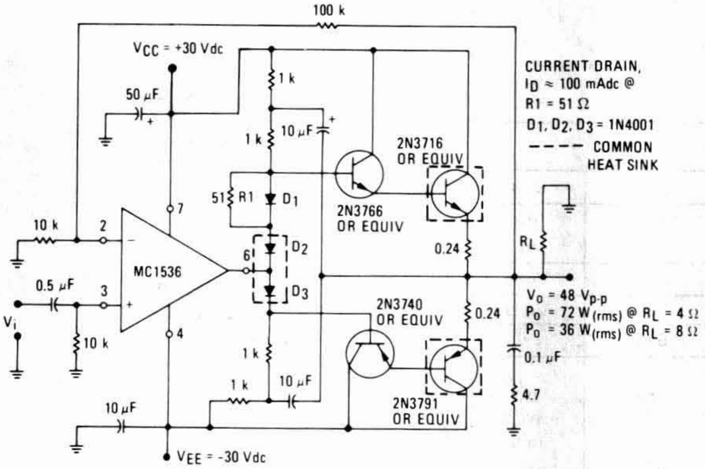

100 k
VCC = +30 Vdc
50 µF
1 k
1 k
10 µF
2N3716 OR EQUIV
51 R1
D1
2N3766 OR EQUIV
7
10 k
2
MC1536
6
D2
D3
0.24
RL
0.5 µF
3
Vi
10 k
4
2N3740 OR EQUIV
0.24
1 k
1 k
10 µF
2N3791 OR EQUIV
0.1 µF
4.7
10 µF
VEE = -30 Vdc
CURRENT DRAIN, ID ≈ 100 mAdc @ R1 = 51 Ω
D1, D2, D3 = 1N4001
- - - - COMMON HEAT SINK
Vo = 48 Vp-p
Po = 72 W(rms) @ RL = 4 Ω
Po = 36 W(rms) @ RL = 8 Ω

FIGURE 12 – VOLTAGE CONTROLLED CURRENT SOURCE or TRANSCONDUCTANCE AMPLIFIER WITH 0 TO 40 V COMPLIANCE

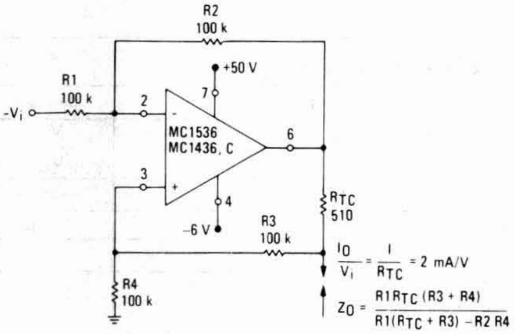

R2
100 k
+50 V
R1
100 k
-Vi
2
7
MC1536
MC1436, C
6
3
4
-6 V
R3
100 k
RTC
510
R4
100 k
$\frac{I_O}{V_i} = \frac{1}{R_{TC}} = 2$ mA/V
$Z_O = \frac{R1 R_{TC} (R3 + R4)}{R1(R_{TC} + R3) - R2\,R4}$

FIGURE 13 – REPRESENTATIVE CIRCUIT SCHEMATIC

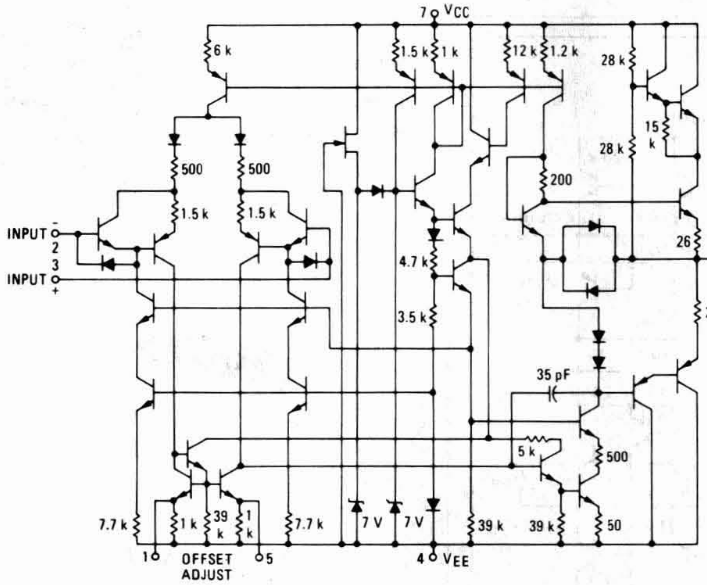
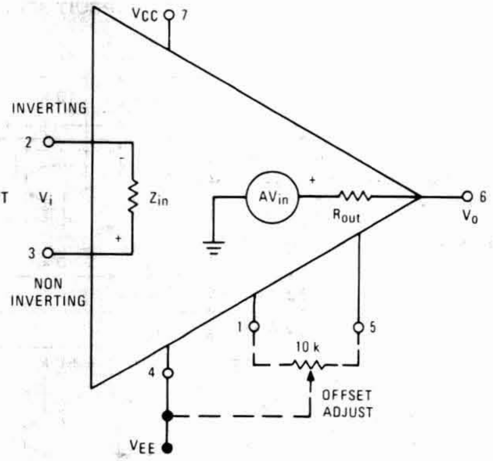

7 VCC
6 k
1.5 k
1 k
12 k
1.2 k
28 k
15 k
28 k
500
500
200
1.5 k
1.5 k
INPUT − 2
INPUT + 3
4.7 k
26
OUTPUT 6
3.5 k
22
35 pF
5 k
500
7.7 k
1 k
39 k
1 k
7.7 k
7 V
7 V
39 k
39 k
50
1
OFFSET ADJUST
5
4 VEE

FIGURE 14 – EQUIVALENT CIRCUIT


VCC 7
INVERTING
2
Vi
Zin
AVin
Rout
6
Vo
3
NON INVERTING
1
5
10 k
OFFSET ADJUST
4
VEE

# MC1437
# MC1537

DUAL MC1709

## OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC1437L | 0°C to +70°C | Ceramic DIP |
| MC1437P | 0°C to +70°C | Plastic DIP |
| MC1537L | −55°C to +125°C | Ceramic DIP |

## MATCHED DUAL OPERATIONAL AMPLIFIERS

. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

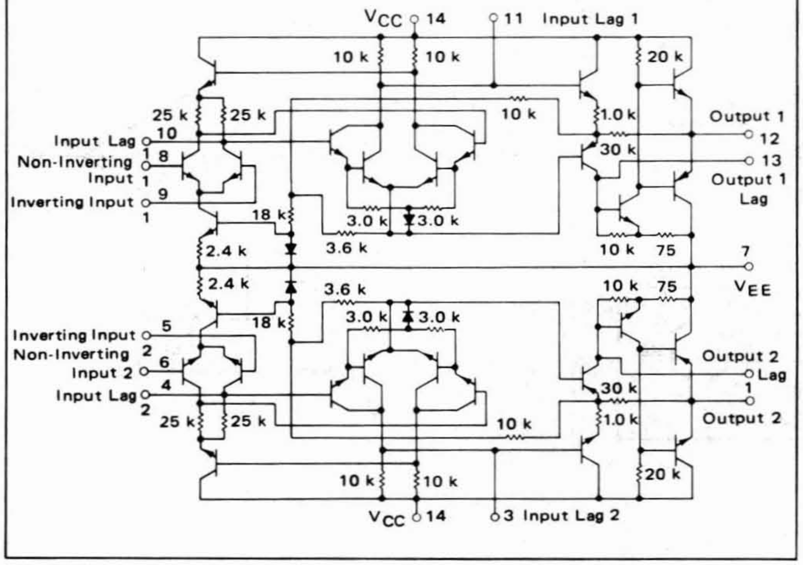
Typical Amplifier Features:

- High-Performance Open Loop Gain Characteristics – $A_{VOL}$ = 45,000 typical
- Low Temperature Drift – ± 3 μV/°C
- Large Output Voltage Swing – ± 14 V typical @ ± 15 V Supply

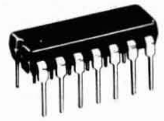
**MAXIMUM RATINGS** ($T_A$ = +25°C)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>-18 | Vdc<br>Vdc |
| Differential Input Voltage Range | $V_{IDR}$ | ±5.0 | Volts |
| Common-Mode Input Voltage Range | $V_{ICR}$ | $\pm V_{CC}$ | Volts |
| Output Short Circuit Duration | $t_S$ | 5.0 | s |
| Power Dissipation (Package Limitation) | $P_D$ | | |
| Ceramic Package | | 750 | mW |
| Derate above $T_A$ = +25°C | | 6.0 | mW/°C |
| Plastic Package MC1437P | | 625 | mW |
| Derate above $T_A$ = +25°C | | 5.0 | mW/°C |
| Operating Ambient Temperature Range | $T_A$ | | °C |
| MC1537 | | -55 to +125 | |
| MC1437 | | 0 to +70 | |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

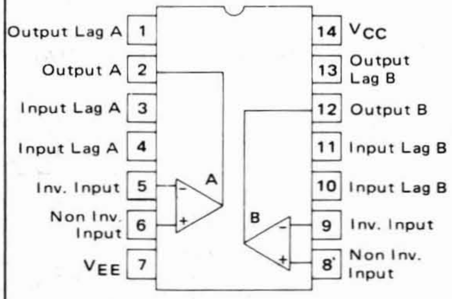
FIGURE 1 – CIRCUIT SCHEMATIC



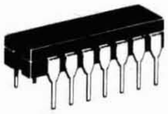
VCC 14
11 Input Lag 1
10 k
10 k
20 k
25 k
25 k
10 k
1.0 k
Output 1
12
13
Input Lag 10
Non-Inverting 8
Input 1
Inverting Input 9
1
30 k
Output 1
Lag
18 k
3.0 k
3.0 k
2.4 k
3.6 k
10 k
75
7
2.4 k
3.6 k
10 k
75
VEE
3.0 k
3.0 k
18 k
Inverting Input 5
Non-Inverting 2
6
Input 2
4
Input Lag 2
30 k
Output 2
Lag
1
25 k
25 k
10 k
1.0 k
Output 2
10 k
10 k
20 k
VCC 14
3 Input Lag 2



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05
(MC1437P only)



Output Lag A 1
Output A 2
Input Lag A 3
Input Lag A 4
Inv. Input 5
Non Inv. Input 6
VEE 7
A
B
14 VCC
13 Output Lag B
12 Output B
11 Input Lag B
10 Input Lag B
9 Inv. Input
8 Non Inv. Input



**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA

**ELECTRICAL CHARACTERISTICS** – Each Amplifier ($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C unless otherwise noted.)

| | | MC1537 | | | MC1437 | | | |
|---|---|---|---|---|---|---|---|---|
| **Characteristic** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Open Loop Voltage Gain ($R_L$ = 5.0 kΩ, $V_o$ = ± 10 V, $T_A$ = $T_{low}$ ① to $T_{high}$ ②) | $A_{VOL}$ | 25,000 | 45,000 | 70,000 | 15,000 | 45,000 | – | – |
| Output Impedance (f = 20 Hz) | $z_o$ | – | 30 | – | – | 30 | – | Ω |
| Input Impedance (f = 20 Hz) | $z_i$ | 150 | 400 | – | 50 | 150 | – | kΩ |
| Output Voltage Range | $V_{OR}$ | | | | | | | $V_{peak}$ |
| ($R_L$ = 10 kΩ) | | ±12 | ±14 | – | ±12 | ±14 | – | |
| ($R_L$ = 2.0 kΩ) | | ±10 | ±13 | – | – | – | – | |
| Input Common-Mode Voltage Range | $V_{ICR}$ | ±8.0 | ±10 | – | ±8.0 | ±10 | – | $V_{peak}$ |
| Common-Mode Rejection Ratio | CMRR | 70 | 100 | – | 65 | 100 | – | dB |
| Input Bias Current $\left(I_{IB} = \frac{I_1 + I_2}{2}\right)$ | $I_{IB}$ | | | | | | | µA |
| ($T_A$ = +25°C) | | – | 0.2 | 0.5 | – | 0.4 | 1.5 | |
| ($T_A$ = $T_{low}$ ①) | | – | 0.5 | 1.5 | – | – | 2.0 | |
| Input Offset Current | $I_{IO}$ | | | | | | | µA |
| ($I_{IO} = I_1 - I_2$) | | – | 0.05 | 0.2 | – | 0.05 | 0.5 | |
| ($I_{IO} = I_1 - I_2$, $T_A$ = $T_{low}$ ①) | | – | – | 0.5 | – | – | 0.75 | |
| ($I_{IO} = I_1 - I_2$, $T_A$ = $T_{high}$ ②) | | – | – | 0.2 | – | – | 0.75 | |
| Input Offset Voltage | $V_{IO}$ | | | | | | | mV |
| ($T_A$ = +25°C) | | – | 1.0 | 5.0 | – | 1.0 | 7.5 | |
| ($T_A$ = $T_{low}$ ① to $T_{high}$ ②) | | – | – | 6.0 | – | – | 10 | |
| Step Response | | | | | | | | |
| (Gain = 100, 5% overshoot, $R_1$ = 1 kΩ, $R_2$ = 100 kΩ, $R_3$ = 1.5 kΩ, $C_1$ = 100 pF, $C_2$ = 3.0 pF) | $t_{TLH}$<br>$t_{PLH}$-$t_{PHL}$<br>SR | –<br>–<br>– | 0.8<br>0.38<br>12 | –<br>–<br>– | –<br>–<br>– | 0.8<br>0.38<br>12 | –<br>–<br>– | µs<br>µs<br>V/µs |
| (Gain = 10, 10% overshoot, $R_1$ = 1 kΩ, $R_2$ = 10 kΩ, $R_3$ = 1.5 kΩ, $C_1$ = 500 pF, $C_2$ = 20 pF) | $t_{TLH}$<br>$t_{PLH}$-$t_{PHL}$<br>SR | –<br>–<br>– | 0.6<br>0.34<br>1.7 | –<br>–<br>– | –<br>–<br>– | 0.6<br>0.34<br>1.7 | –<br>–<br>– | µs<br>µs<br>V/µs |
| (Gain = 1, 5% overshoot, $R_1$ = 10 kΩ, $R_2$ = 10 kΩ, $R_3$ = 1.5 kΩ, $C_1$ = 5000 pF, $C_2$ = 200 pF) | $t_{TLH}$<br>$t_{PLH}$-$t_{PHL}$<br>SR | –<br>–<br>– | 2.2<br>1.3<br>0.25 | –<br>–<br>– | –<br>–<br>– | 2.2<br>1.3<br>0.25 | –<br>–<br>– | µs<br>µs<br>V/µs |
| Average Temperature Coefficient of Input Offset Voltage | $\Delta V_{IO}/\Delta T$ | | | | | | | µV/°C |
| ($R_S$ = 50 Ω, $T_A$ = $T_{low}$ ① to $T_{high}$ ②) | | – | 1.5 | – | – | 1.5 | – | |
| ($R_S$ ≦ 10 kΩ, $T_A$ = $T_{low}$ ① to $T_{high}$ ②) | | – | 3.0 | – | – | 3.0 | – | |
| Average Temperature Coefficient of Input Offset Voltage | $\Delta I_{IO}/\Delta T$ | | | | | | | nA/°C |
| ($T_A$ = $T_{low}$ ① to +25°C) | | – | 0.7 | – | – | 0.7 | – | |
| ($T_A$ = +25°C to $T_{high}$ ②) | | – | 0.7 | – | – | 0.7 | – | |
| DC Power Consumption (Total) (Power Supply = ± 15 V, $V_o$ = 0) | $P_C$ | – | 160 | 225 | – | 160 | 225 | mW |
| Positive Supply Sensitivity ($V_{EE}$ constant) | PSS+ | – | 10 | 150 | – | 10 | 200 | µV/V |
| Negative Supply Sensitivity ($V_{CC}$ constant) | PSS− | – | 10 | 150 | – | 10 | 200 | µV/V |

① $T_{low}$ = 0°C for MC1437
= −55°C for MC1537

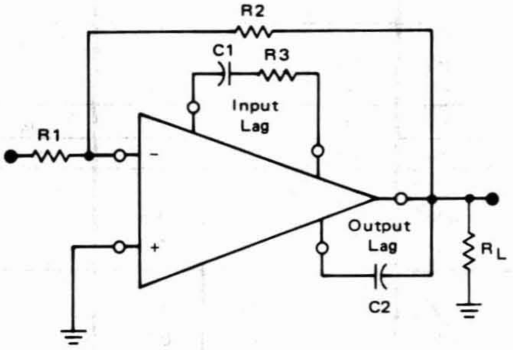
② $T_{high}$ = +70°C for MC1437
= +125°C for MC1537

**MATCHING CHARACTERISTICS**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Open Loop Voltage Gain | $A_{VOL1}$-$A_{VOL2}$ | – | ±1.0 | – | – | ±1.0 | – | dB |
| Input Bias Current | $I_{IB1}$-$I_{IB2}$ | – | ±0.15 | – | – | ±0.15 | – | µA |
| Input Offset Current | $I_{IO1}$-$I_{IO2}$ | – | ±0.02 | – | – | ±0.02 | – | µA |
| Average Temperature Coefficient | $\left\lvert\frac{\Delta I_{IO1}}{\Delta T}\right\rvert - \left\lvert\frac{\Delta I_{IO2}}{\Delta T}\right\rvert$ | – | ±0.2 | – | – | ±0.2 | – | nA/°C |
| Input Offset Voltage | $V_{IO1}$-$V_{IO2}$ | – | ±0.2 | – | – | ±0.2 | – | mV |
| Average Temperature Coefficient | $\left\lvert\frac{\Delta V_{IO1}}{\Delta T}\right\rvert - \left\lvert\frac{\Delta V_{IO2}}{\Delta T}\right\rvert$ | – | ±0.5 | – | – | ±0.5 | – | µV/°C |
| Channel Separation (f = 10 kHz) | $\frac{e_{o1}}{e_{o2}}$ | – | 90 | – | – | 90 | – | dB |

## TYPICAL OUTPUT CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT
$V_{CC} = +15$ Vdc, $V_{EE} = 15$ Vdc, $T_A = 25^\circ C$



| FIGURE NO. | CURVE NO. | VOLTAGE GAIN | TEST CONDITIONS $R_1(\Omega)$ | $R_2(\Omega)$ | $R_3(\Omega)$ | $C_1$(pF) | $C_2$(pF) | OUTPUT NOISE (mV[rms]) |
|---|---|---|---|---|---|---|---|---|
| 4 | 1 | 1 | 10 k | 10 k | 1.5 k | 5.0 k | 200 | 0.10 |
|  | 2 | 10 | 10 k | 100 k | 1.5 k | 500 | 20 | 0.14 |
|  | 3 | 100 | 10 k | 1.0 M | 1.5 k | 100 | 3.0 | 0.7 |
|  | 4 | 1000 | 1.0 k | 1.0 M | 0 | 10 | 3.0 | 5.2 |
| 5 | 1 | 1 | 10 k | 10 k | 1.5 k | 5.0 k | 200 | 0.10 |
|  | 2 | 10 | 10 k | 100 k | 1.5 k | 500 | 20 | 0.14 |
|  | 3 | 100 | 10 k | 1.0 M | 1.5 k | 100 | 3.0 | 0.7 |
|  | 4 | 1000 | 1.0 k | 1.0 M | 0 | 10 | 3.0 | 5.2 |
| 6 | 1 | $A_{VOL}$ | 0 | ∞ | 1.5 k | 5.0 k | 200 | 5.5 |
|  | 2 | $A_{VOL}$ | 0 | ∞ | 1.5 k | 500 | 20 | 10.5 |
|  | 3 | $A_{VOL}$ | 0 | ∞ | 1.5 k | 100 | 3.0 | 21.0 |
|  | 4 | $A_{VOL}$ | 0 | ∞ | 0 | 10 | 3.0 | 39.0 |
|  | 5 | $A_{VOL}$ | 0 | ∞ | ∞ | 0 | 3.0 | — |

FIGURE 4 – LARGE SIGNAL SWING versus FREQUENCY

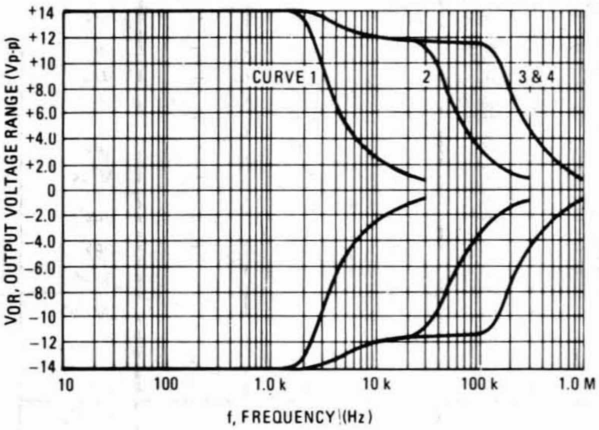


FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

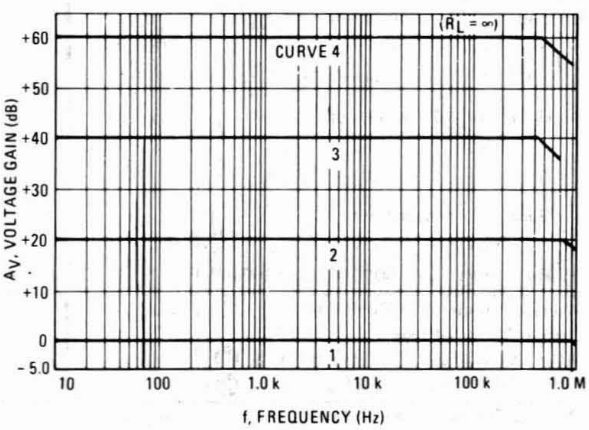


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

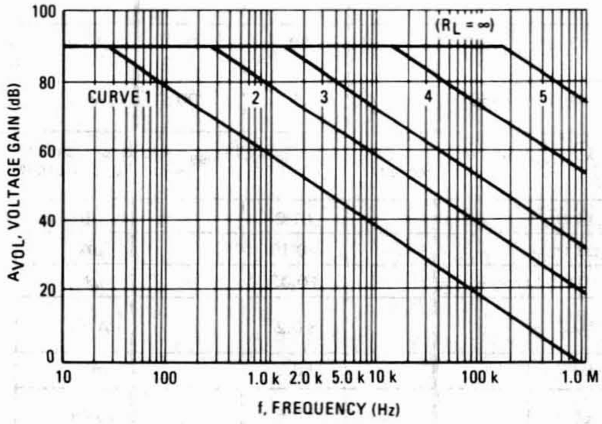
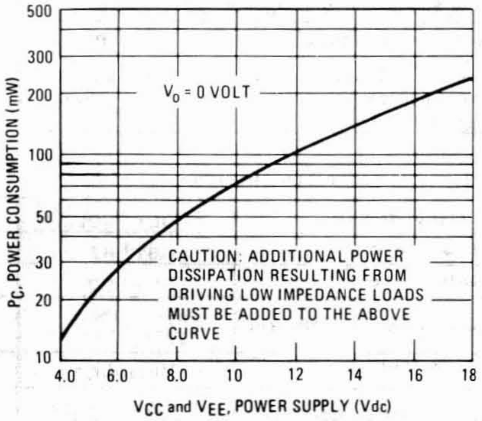


FIGURE 7 – TOTAL POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



## TYPICAL CHARACTERISTICS (continued)

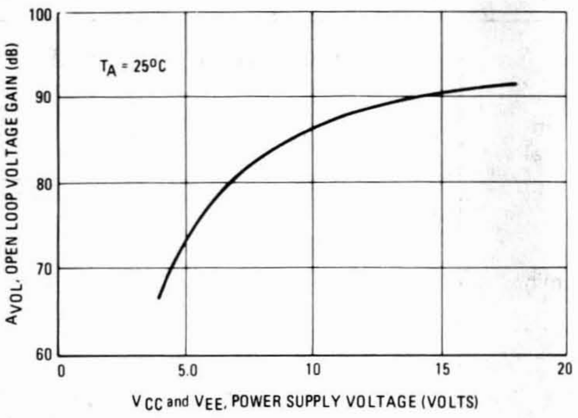


FIGURE 8 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

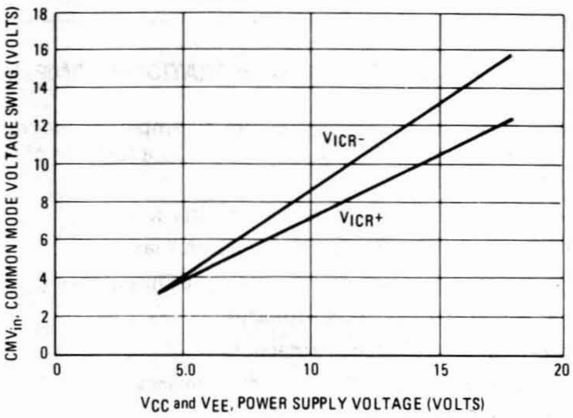


FIGURE 9 – COMMON INPUT SWING versus POWER SUPPLY VOLTAGE

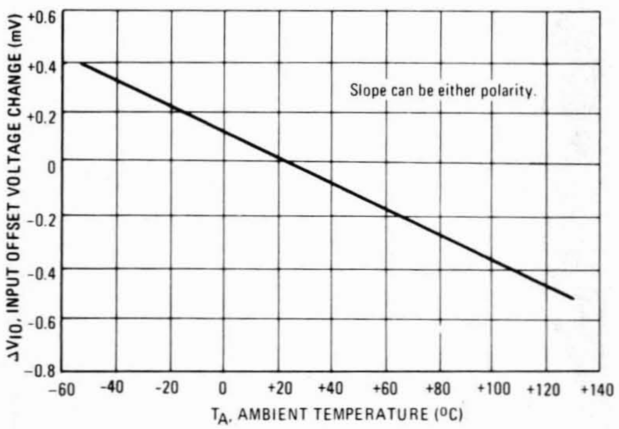


FIGURE 10 – INPUT OFFSET VOLTAGE versus TEMPERATURE

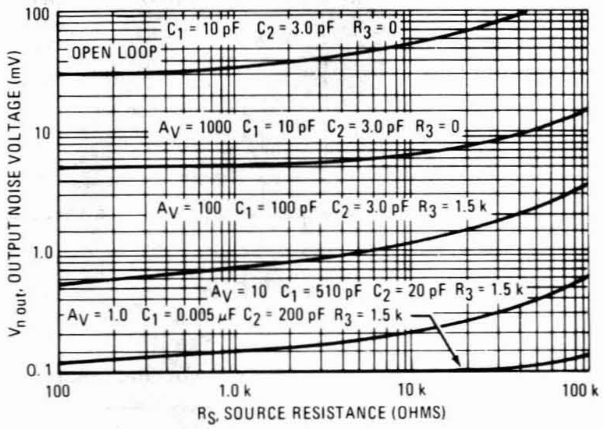
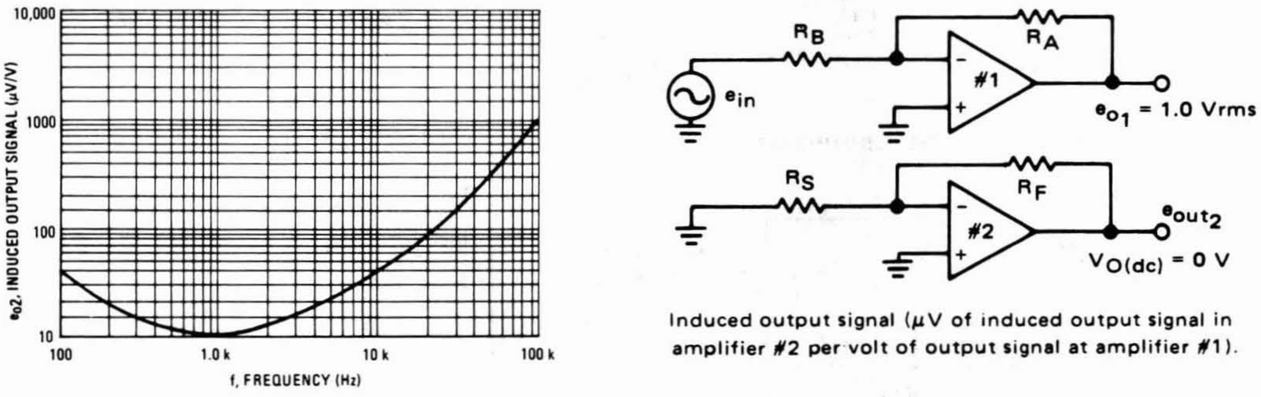


FIGURE 11 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE

FIGURE 12 – INDUCED OUTPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY



Induced output signal (μV of induced output signal in amplifier #2 per volt of output signal at amplifier #1).

## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC1439G | 0°C to +70°C | Metal Can |
| MC1439P1 | 0°C to +70°C | Plastic DIP |
| MC1539G | −55°C to +125°C | Metal Can |

# MC1439
# MC1539

## UNCOMPENSATED OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Low Input Offset Voltage — 3.0 mV max
- Low Input Offset Current — 60 nA max
- Large Power-Bandwidth — 20 Vp-p Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- High Slew Rate — 34 V/μs typ

## OPERATIONAL AMPLIFIER

### SILICON MONOLITHIC
### INTEGRATED CIRCUIT

FIGURE 1 – HIGH SLEW-RATE INVERTER

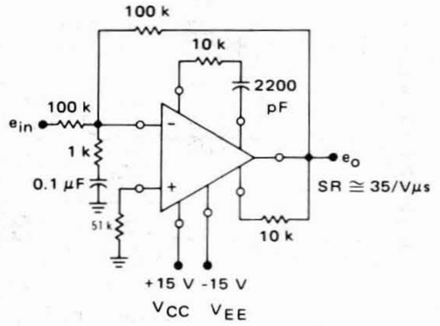
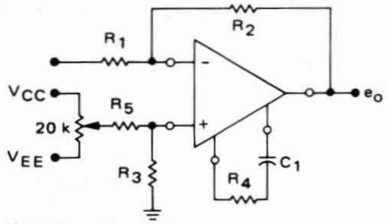
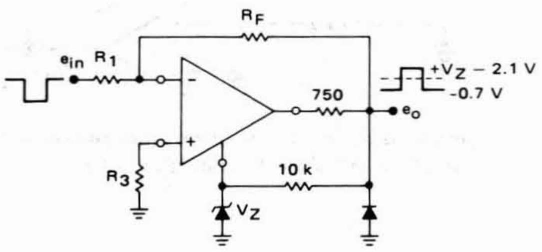

100 k
10 k
2200 pF
100 k
$e_{in}$
1 k
0.1 μF
51 k
$e_o$
SR ≅ 35/Vμs
10 k
+15 V
-15 V
$V_{CC}$
$V_{EE}$

FIGURE 2 – OUTPUT NULLING CIRCUIT

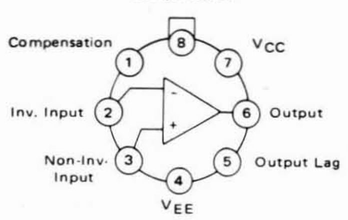

$R_1$
$R_2$
$V_{CC}$
$R_5$
20 k
$V_{EE}$
$R_3$
$R_4$
$C_1$
$e_o$

$10\ k \leqslant R_S \leqslant 100(R_3)\ (V_{CC})$

FIGURE 3 – OUTPUT LIMITING CIRCUIT

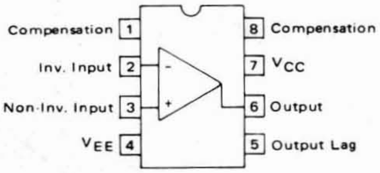

$R_F$
$e_{in}$
$R_1$
750
$+V_Z - 2.1$ V
-0.7 V
$e_o$
$R_3$
10 k
$V_Z$

**G SUFFIX**
METAL PACKAGE
CASE 601-04


Compensation
Compensation
$V_{CC}$
Inv. Input
Output
Non-Inv. Input
Output Lag
$V_{EE}$
1
2
3
4
5
6
7
8

(Top View)

**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(MC1439 only)


Compensation 1
Inv. Input 2
Non-Inv. Input 3
$V_{EE}$ 4
8 Compensation
7 $V_{CC}$
6 Output
5 Output Lag

(Top View)

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C unless otherwise noted.)

| | | MC1539 | | | MC1439 | | | |
|---|---|---|---|---|---|---|---|---|
| **Characteristic** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Input Bias Current | $I_{IB}$ | | | | | | | μA |
| ($T_A$ = +25°C) | | – | 0.20 | 0.50 | – | 0.20 | 1.0 | |
| ($T_A$ = $T_{low}$ ①) | | – | 0.23 | 0.70 | – | 0.23 | 1.5 | |
| Input Offset Current | $\|I_{IO}\|$ | | | | | | | nA |
| ($T_A$ = $T_{low}$) | | – | – | 75 | – | – | 150 | |
| ($T_A$ = +25°C) | | – | 20 | 60 | – | 20 | 100 | |
| ($T_A$ = $T_{high}$ ①) | | – | – | 75 | – | – | 150 | |
| Input Offset Voltage | $\|V_{IO}\|$ | | | | | | | mV |
| ($T_A$ = +25°C) | | – | 1.0 | 3.0 | – | 2.0 | 7.5 | |
| ($T_A$ = $T_{low}$, $T_{high}$) | | – | – | 4.0 | – | – | – | |
| Average Temperature Coefficient of Input Offset Voltage ($T_A$ = $T_{low}$ to $T_{high}$) | $\|TCV_{IO}\|$ | | | | | | | μV/°C |
| ($R_S$ = 50 Ω) | | – | 3.0 | – | – | 3.0 | – | |
| ($R_S$ ≤ 10 kΩ) | | – | 5.0 | – | – | 5.0 | – | |
| Input Impedance (f = 20 Hz) | $z_{in}$ | 150 | 300 | – | 100 | 300 | – | kΩ |
| Input Common-Mode Voltage Range | $V_{ICR}$ | ±11 | ±12 | – | ±11 | ±12 | – | $V_{pk}$ |
| Equivalent Input Noise Voltage ($R_S$ = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz) | $e_n$ | – | 30 | – | – | 30 | – | nV/(Hz)½ |
| Common-Mode Rejection Ratio (f = 1.0 kHz) | CMRR | 80 | 110 | – | 80 | 110 | – | dB |
| Open-Loop Voltage Gain ($V_O$ = ±10 V, $R_L$ = 10 kΩ, $R_5$ = ∞) ($T_A$ = +25°C to $T_{high}$) | $A_{VOL}$ | 50,000 | 120,000 | – | 15,000 | 100,000 | – | – |
| ($T_A$ = $T_{low}$) | | 25,000 | 100,000 | – | 15,000 | 100,000 | – | |
| Power Bandwidth ($A_v$ = 1, THD ≤ 5%, $V_O$ = 20 Vp-p) | PBW | | | | | | | kHz |
| ($R_L$ = 2.0 kΩ) | | – | – | – | 10 | 50 | – | |
| ($R_L$ = 1.0 kΩ, $R_5$ = 10 k) | | 20 | 50 | – | – | – | – | |
| Step Response | | | | | | | | |
| Gain = 1000, no overshoot, | $t_{THL}$ | – | 130 | – | – | 130 | – | ns |
| R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ, | $t_{pd}$ | – | 190 | – | – | 190 | – | ns |
| R4 = 30 kΩ, R5 = 10 kΩ, C1 = 1000 pF | SR | – | 6.0 | – | – | 6.0 | – | V/μs |
| Gain = 1000, 15% overshoot, | $t_{THL}$ | – | 80 | – | – | 80 | – | ns |
| R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ, | $t_{pd}$ | – | 100 | – | – | 100 | – | ns |
| R4 = 0, R5 = 10 kΩ, C1 = 10 pF | SR | – | 14 | – | – | 14 | – | V/μs |
| Gain = 100, no overshoot, | $t_{THL}$ | – | 60 | – | – | 60 | – | ns |
| R1 = 1.0 kΩ, R2 = 100 kΩ, R3 = 1.0 kΩ, | $t_{pd}$ | – | 100 | – | – | 100 | – | ns |
| R4 = 10 kΩ, R5 = 10 kΩ, C1 = 2200 pF | SR | – | 34 | – | – | 34 | – | V/μs |
| Gain = 10, 15% overshoot, | $t_{THL}$ | – | 120 | – | – | 120 | – | ns |
| R1 = 1.0 kΩ, R2 = 10 kΩ, R3 = 1.0 kΩ, | $t_{pd}$ | – | 80 | – | – | 80 | – | ns |
| R4 = 1.0 kΩ, R5 = 10 kΩ, C1 = 2200 pF | SR | – | 6.25 | – | – | 6.25 | – | V/μs |
| Gain = 1, 15% overshoot, | $t_{THL}$ | – | 160 | – | – | 160 | – | ns |
| R1 = 10 kΩ, R2 = 10 kΩ, R3 = 5.0 kΩ, | $t_{pd}$ | – | 80 | – | – | 80 | – | ns |
| R4 = 390 Ω, R5 = 10 kΩ, C1 = 2200 pF | SR | – | 4.2 | – | – | 4.2 | – | V/μs |
| Output Impedance (f = 20 Hz) | $z_o$ | – | 4.0 | – | – | 4.0 | – | kΩ |
| Output Voltage Swing | $V_O$ | | | | | | | $V_{pk}$ |
| ($R_L$ = 2.0 kΩ, f = 1.0 kHz) | | – | – | – | ±10 | ±13 | – | |
| ($R_L$ = 1.0 kΩ, f = 1.0 kHz) | | ±10 | ±13 | – | – | – | – | |
| Positive Supply Rejection Ratio ($V_{EE}$ constant, $R_5$ = ∞) | PSRR+ | – | 50 | 150 | – | 50 | 200 | μV/V |
| Negative Supply Rejection Ratio ($V_{CC}$ constant, $R_5$ = ∞) | PSRR− | – | 50 | 150 | – | 50 | 200 | μV/V |
| Power Supply Current ($V_O$ = 0) | $I_{CC}$ | – | 3.0 | 5.0 | – | 3.0 | 6.7 | mAdc |
| | $I_{EE}$ | – | 3.0 | 5.0 | – | 3.0 | 6.7 | |

① $T_{low}$ = 0°C for MC1439 $T_{high}$ = +70°C for MC1439
−55°C for MC1539 +125°C for MC1539

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>+18 | Vdc |
| Differential Input Voltage Range | $V_{IDR}$ | $\pm(V_{CC} + \lvert V_{EE}\rvert)$ | Vdc |
| Common-Mode Input Voltage Range | $V_{ICR}$ | $+V_{CC}, -\lvert V_{EE}\rvert$ | Vdc |
| Load Current | $I_L$ | 15 | mA |
| Output Short-Circuit Duration | $t_S$ | Continuous | |
| Power Dissipation (Package Limitation) | $P_D$ | | |
| Metal Package | | 680 | mW |
| Derate above $T_A$ = +25°C | | 4.6 | mW/°C |
| Plastic Dual In-Line Packages MC1439 | | 625 | mW |
| Derate above $T_A$ = +25°C | | 5.0 | mW/°C |
| Operating Temperature Range MC1539<br>MC1439 | $T_A$ | -55 to +125<br>0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | | °C |
| Metal Packages | | -65 to +150 | |
| Plastic Packages | | -55 to +125 | |

FIGURE 4 – EQUIVALENT CIRCUIT SCHEMATIC

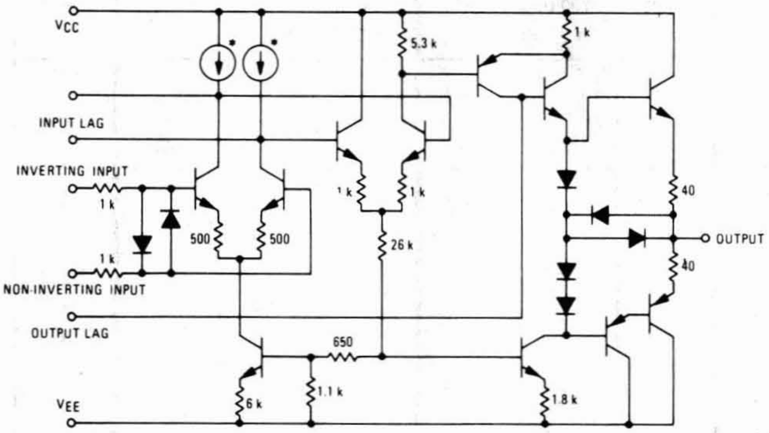

VCC
INPUT LAG
INVERTING INPUT
1 k
1 k
NON-INVERTING INPUT
OUTPUT LAG
VEE
500
500
5.3 k
1 k
1 k
26 k
650
6 k
1.1 k
1.8 k
1 k
40
40
OUTPUT

FIGURE 5 – EQUIVALENT CIRCUIT

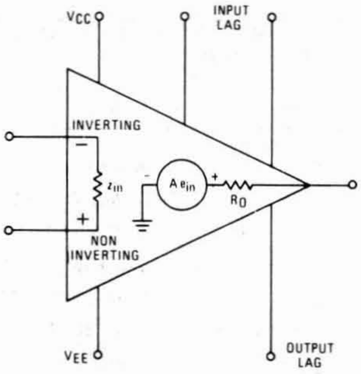
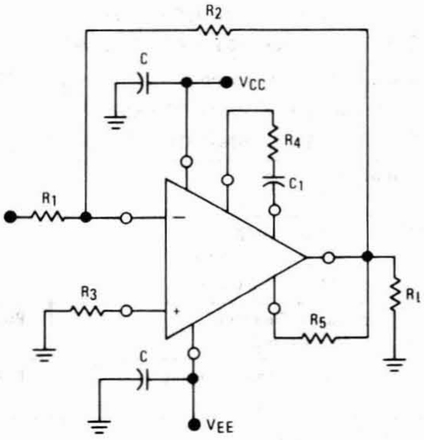

VCC
INPUT LAG
INVERTING
−
zin
+
NON INVERTING
A ein
R0
VEE
OUTPUT LAG

FIGURE 6 – TEST CIRCUIT


R2
C
VCC
R4
C1
R1
−
+
R3
R5
RL
C
VEE

TYPICAL OUTPUT CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $V_{EE}$ = -15 Vdc, $T_A$ = +25°C

| FIGURE NO. | CURVE NO. | VOLTAGE GAIN | TEST CONDITIONS (FIGURE 6) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | $R_1$ (Ω) | $R_2$ (Ω) | $R_3$ (Ω) | $R_4$ (Ω) | $R_5$ (Ω) | $C_1$ (pF) |
| 7,10,12 | 1 | $A_{vol}$ | 0 | ∞ | 0 | ∞ | ∞ | 0 |
| | 2 | 1 | 10 k | 10 k | 5.0 k | 390 | 10 k | 2200 |
| | 3 | 10 | 1.0 k | 10 k | 1.0 k | 1.0 k | 10 k | 2200 |
| | 4 | 100 | 1.0 k | 100 k | 1.0 k | 10 k | 10 k | 2200 |
| | 5 | 1000 | 1.0 k | 1.0 M | 1.0 k | 30 k | 10 k | 1000 |
| | 6 | 1000 | 1.0 k | 1.0 M | 1.0 k | 0 | 10 k | 10 |
| 8 | 1 | $A_{vol}$ | 0 | ∞ | 0 | ∞ | ∞ | 0 |
| | 2 | ↓ | ↓ | ↓ | ↓ | 390 | ↓ | 2200 |
| | 3 | ↓ | ↓ | ↓ | ↓ | 1.0 k | ↓ | 2200 |
| | 4 | ↓ | ↓ | ↓ | ↓ | 10 k | ↓ | 2200 |
| | 5 | ↓ | ↓ | ↓ | ↓ | 30 k | ↓ | 1000 |
| | 6 | ↓ | ↓ | ↓ | ↓ | 0 | ↓ | 10 |
| 13 | ALL | 1 | 10 k | 10 k | 5.0 k | 390 | 10 k | 2200 |
| 14 | ALL | 10 | 1.0 k | 10 k | 1.0 k | 1.0 k | 10 k | 2200 |
| 15 | ALL | 100 | 1.0 k | 100 k | 1.0 k | 10 k | 10 k | 2200 |
| 16 | ALL | 1000 | 1.0 k | 1.0 M | 1.0 k | 30 k | 10 k | 2200 |

## TYPICAL CHARACTERISTICS (continued)

($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C, unless otherwise noted.)

FIGURE 7 – LARGE-SIGNAL SWING versus FREQUENCY

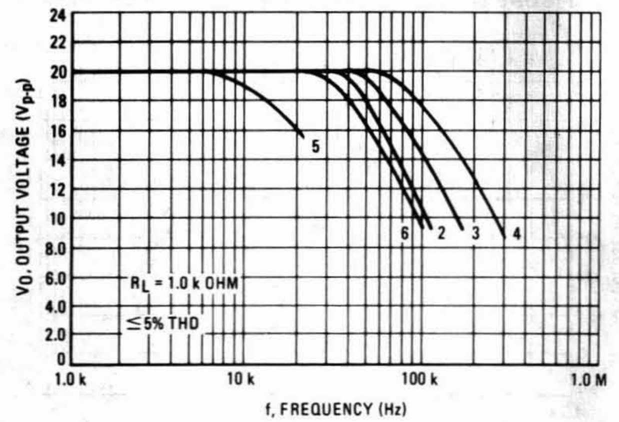


FIGURE 8 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

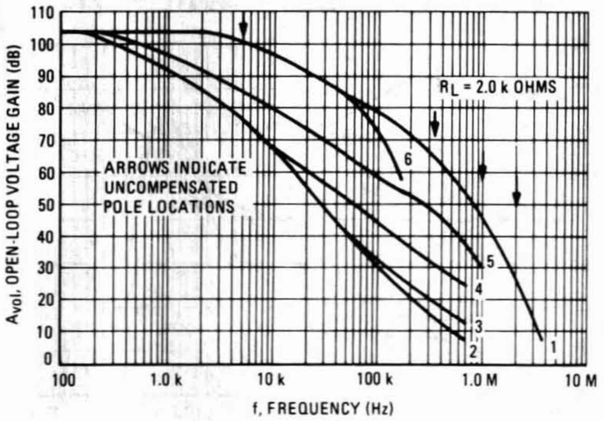


FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

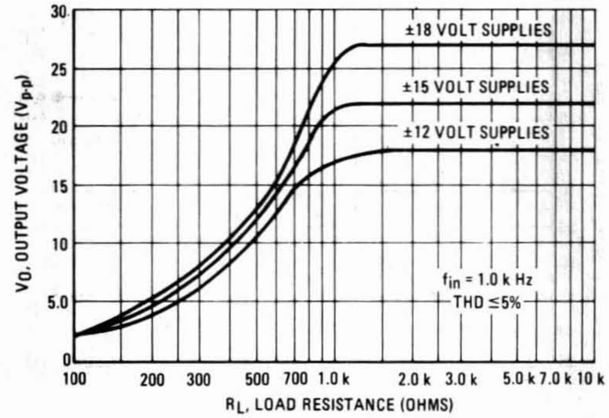


FIGURE 10 – OPEN-LOOP PHASE-SHIFT versus FREQUENCY

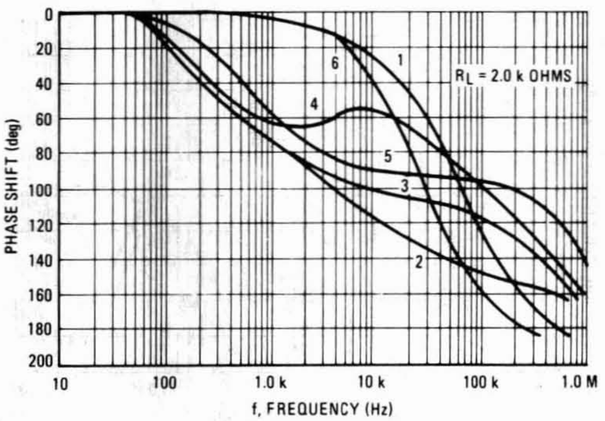


FIGURE 11 – OUTPUT VOLTAGE SWING (to clipping) versus SUPPLY

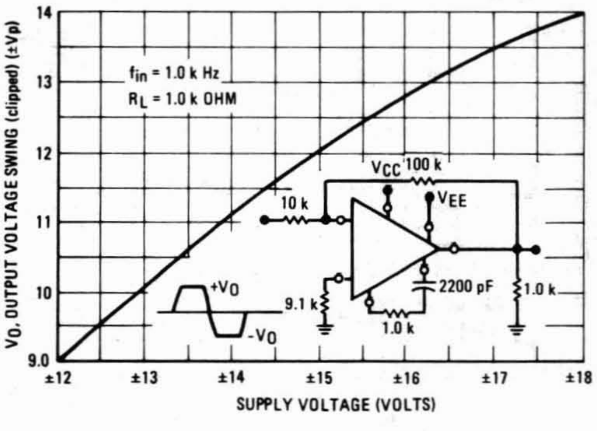
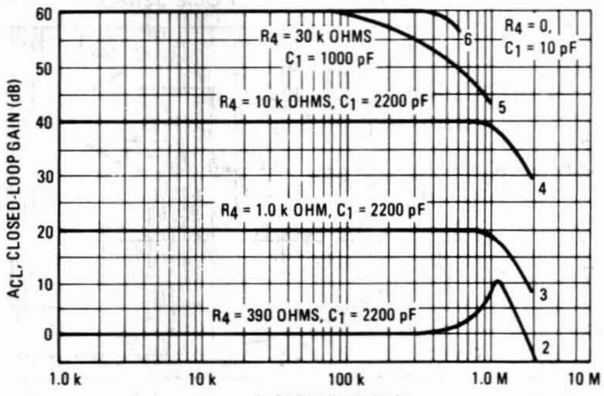


FIGURE 12 – CLOSED-LOOP GAIN versus FREQUENCY



*$A_{CL}$ = Closed-Loop Gain

## TYPICAL CHARACTERISTICS (continued)

($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C, unless otherwise noted.)

FIGURE 13 – $A_{CL}$* = 1 RESPONSE versus TEMPERATURE

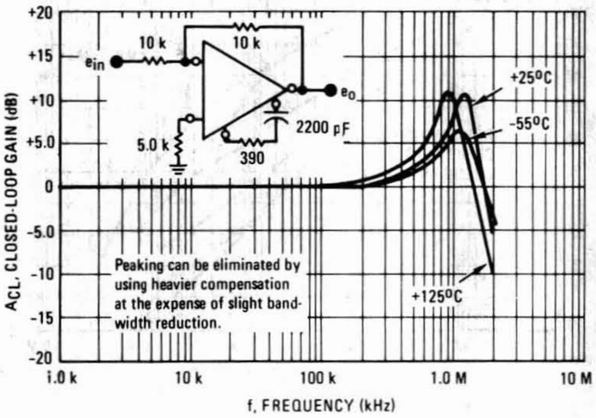


FIGURE 14 – $A_{CL}$ = 10 RESPONSE versus TEMPERATURE

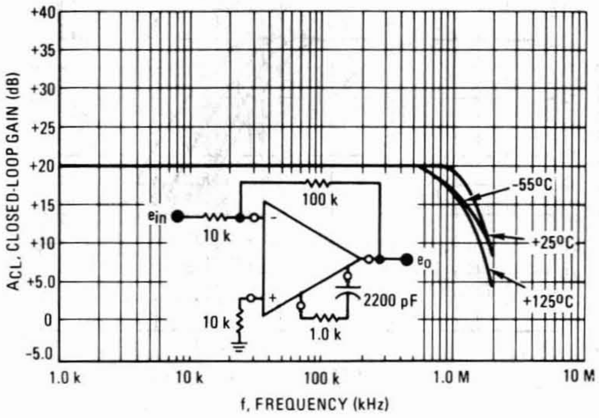


FIGURE 15 – $A_{CL}$ = 100 RESPONSE versus TEMPERATURE

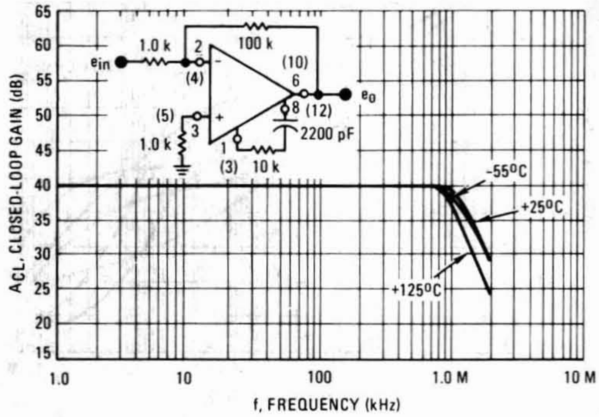


FIGURE 16 – $A_{CL}$ = 1000 RESPONSE versus TEMPERATURE

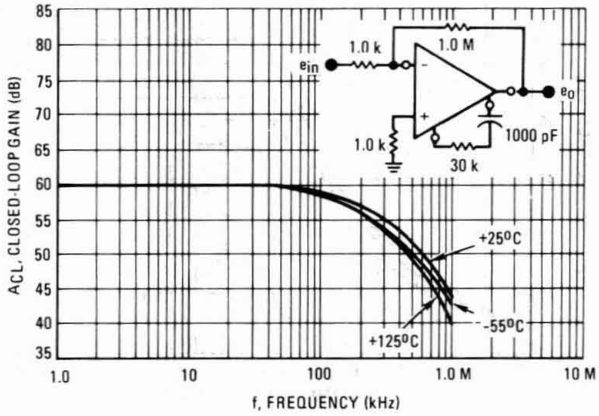


FIGURE 17 – SPECTRAL NOISE DENSITY

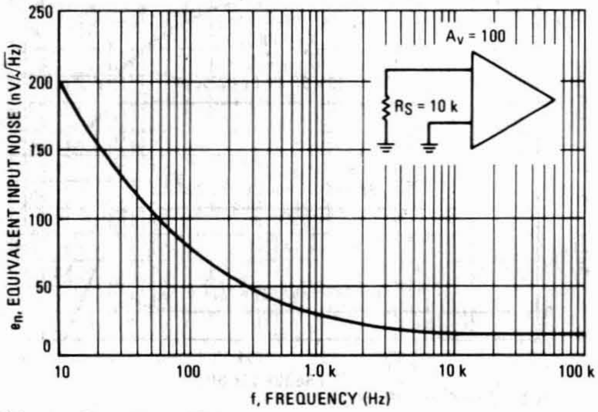
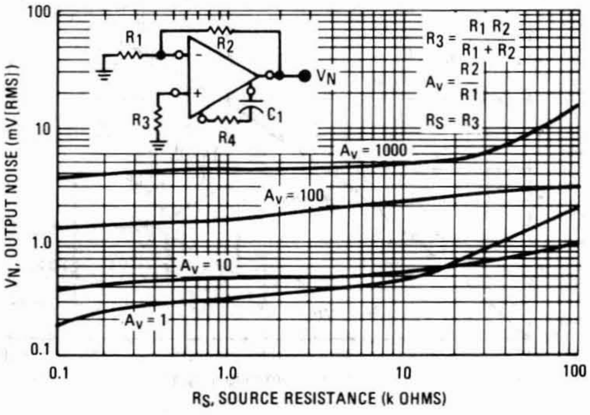


FIGURE 18 – OUTPUT NOISE versus SOURCE RESISTANCE



*$A_{CL}$ = Closed-Loop Gain

## TYPICAL CHARACTERISTICS (continued)

($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C, unless otherwise noted.)

FIGURE 19 – POWER DISSIPATION versus TEMPERATURE

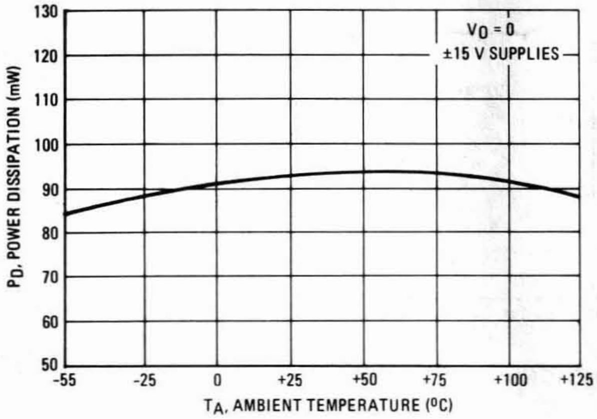


FIGURE 20 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

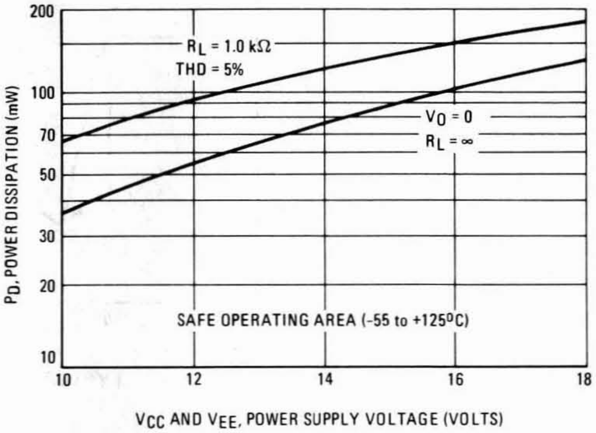


FIGURE 21 – POWER BANDWIDTH (LARGE-SIGNAL SWING versus FREQUENCY)

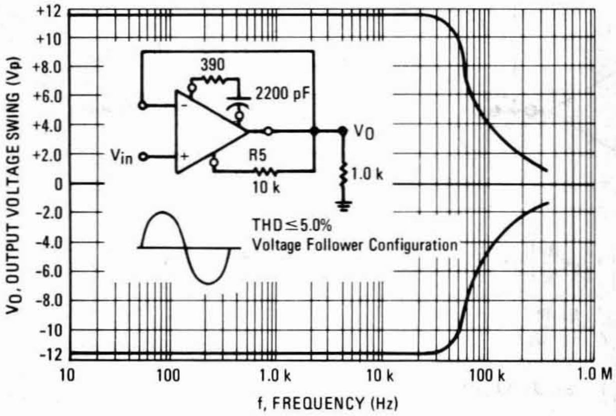


FIGURE 22 – COMMON-MODE INPUT VOLTAGE versus SUPPLY VOLTAGE

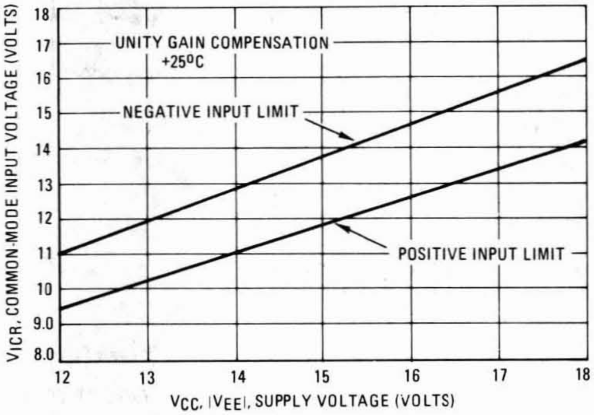


FIGURE 23 – COMMON-MODE REJECTION RATIO versus FREQUENCY

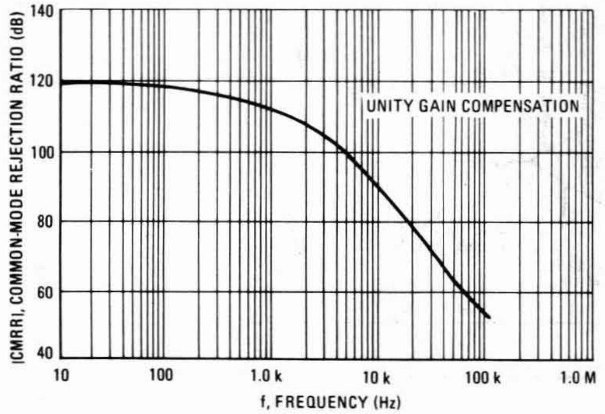


FIGURE 24 – COMMON-MODE REJECTION RATIO versus TEMPERATURE

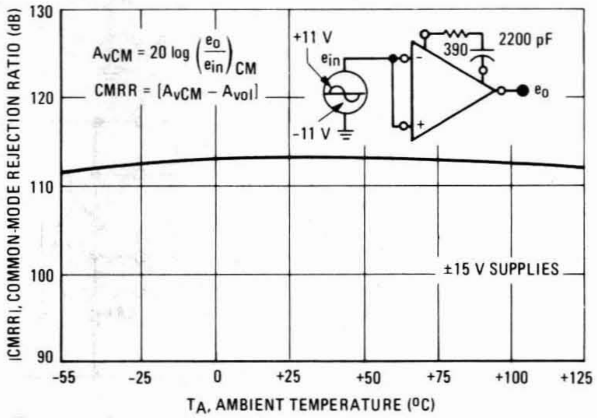
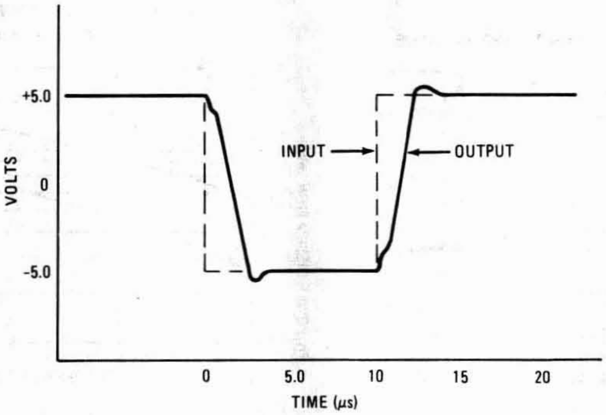
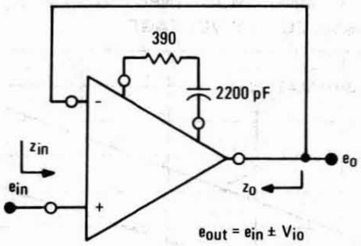


**FIGURE 25 – VOLTAGE-FOLLOWER PULSE RESPONSE**



## TYPICAL APPLICATIONS

**FIGURE 26 – VOLTAGE FOLLOWER**

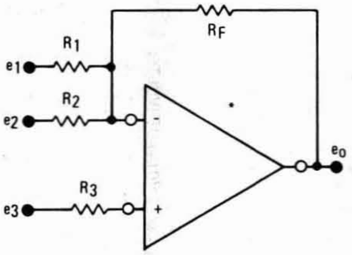

390
2200 pF
-
+
$z_{in}$
$e_{in}$
$z_o$
$e_o$

$e_{out} = e_{in} \pm V_{io}$

$z_{in} > 40$ M OHMS

$$z_{oCL} = z_{oOL}\left[\frac{1+\frac{R_F}{R_i}}{A_{ol}}\right] = 4\text{ k}\left[\frac{1+0}{10^5}\right] \approx 0.04\text{ OHM}$$

**FIGURE 27 – DIFFERENTIAL AMPLIFIER**

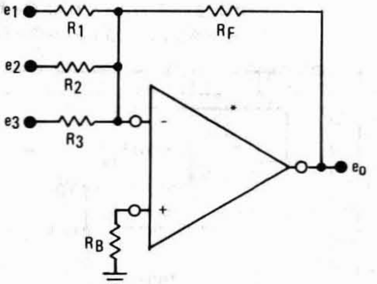

$R_F$
$R_1$
$R_2$
$R_3$
e1
e2
e3
-
+
*
$e_o$

$$e_o = -\left[\frac{R_F}{R_1}e1 + \frac{R_F}{R_2}e2\right] + \left[1 + \frac{R_F}{R_3}\right] e3$$

$$\text{For } R_3 = \frac{R_1, R_2}{R_1 + R_2}$$

*Properly Compensated

**FIGURE 28 – SUMMING AMPLIFIER**

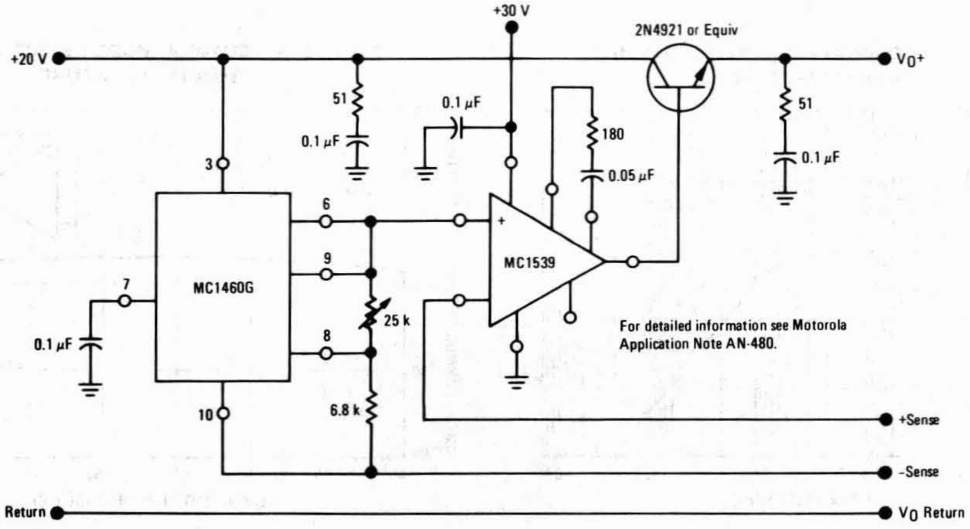

e1
e2
e3
$R_1$
$R_2$
$R_3$
$R_F$
$R_B$
-
+
*
$e_o$

$R_B$ = Parallel Combination of $R_1$, $R_2$, $R_3$, $R_F$.

$$e_o = -\left[\frac{R_F}{R_1}e1 + \frac{R_F}{R_2}e2 + \frac{R_F}{R_3}e3\right]$$

*Properly Compensated

**FIGURE 29 – +15 VOLT REGULATOR**


+30 V
2N4921 or Equiv
+20 V
$V_O$+
51
0.1 μF
0.1 μF
180
0.05 μF
51
0.1 μF
3
6
9
7
8
10
MC1460G
0.1 μF
25 k
6.8 k
MC1539
+
+Sense
-Sense
Return
$V_O$ Return

For detailed information see Motorola Application Note AN-480.

## TYPICAL APPLICATIONS (continued)

**FIGURE 30 – LOAD REGULATION FOR CIRCUIT OF FIGURE 29**

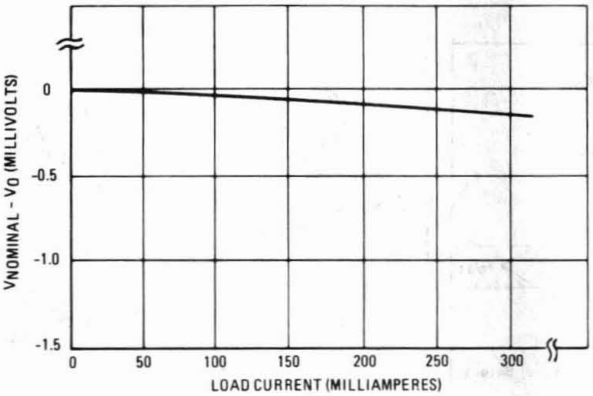
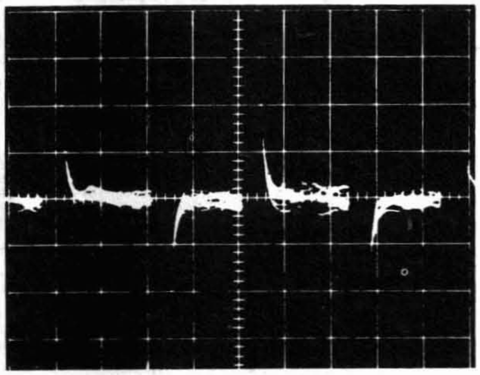


**FIGURE 31 – REGULATOR OUTPUT VOLTAGE (under pulsed load condition)**



Horizontal Scale: 200 µs/Div
Vertical Scale: 1 mV/Div

# MC1445
# MC1545

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1445G | 0°C to +75°C | Metal Can |
| MC1445L | 0°C to +75°C | Ceramic DIP |
| MC1545G | −55°C to +125°C | Metal Can |
| MC1545L | −55°C to +125°C | Ceramic DIP |

## GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

. . . designed for use as a general-purpose gated wideband-amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN491 for design details.

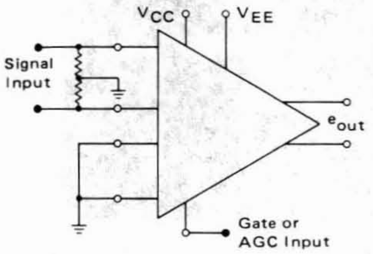
- Large Bandwidth; 50 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

## GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

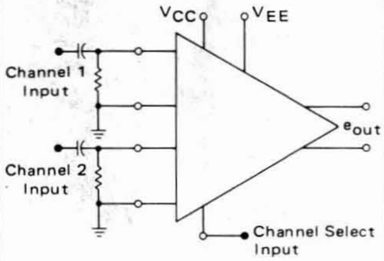
**SILICON MONOLITHIC INTEGRATED CIRCUIT**

### TYPICAL APPLICATIONS

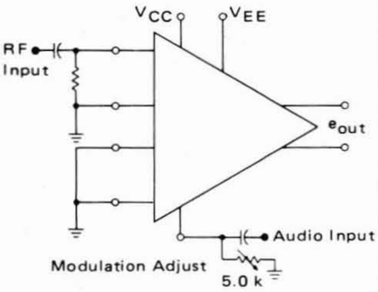
**VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC**


VCC
VEE
Signal Input
eout
Gate or AGC Input

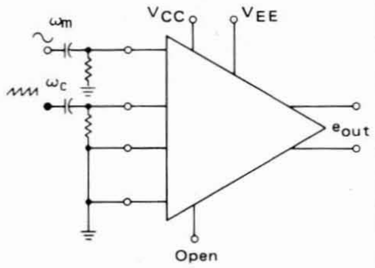
**MULTIPLEX OR FSK**


VCC
VEE
Channel 1 Input
Channel 2 Input
eout
Channel Select Input

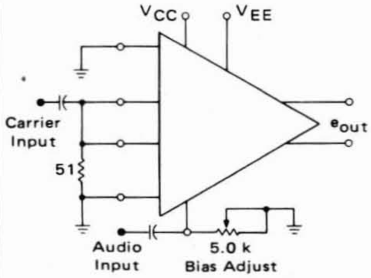
**AMPLITUDE MODULATOR**


VCC
VEE
RF Input
eout
Audio Input
Modulation Adjust
5.0 k

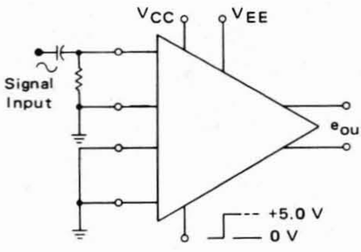
**PULSE-WIDTH MODULATOR**

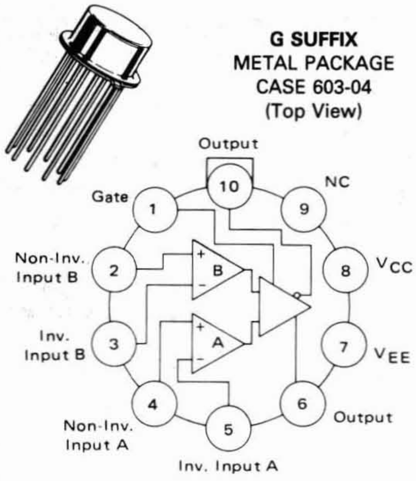

VCC
VEE
ωm
ωc
eout
Open

**BALANCED MODULATOR**

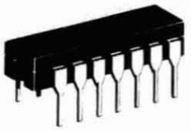

VCC
VEE
Carrier Input
51
eout
Audio Input
5.0 k
Bias Adjust

**ANALOG SWITCH**

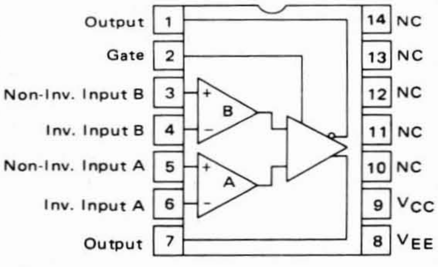

VCC
VEE
Signal Input
eout
+5.0 V
0 V


Output
10
NC
9
Gate
1
Non-Inv. Input B
2
8
VCC
Inv. Input B
3
7
VEE
B
A
4
Non-Inv. Input A
5
Inv. Input A
6
Output

**G SUFFIX**
METAL PACKAGE
CASE 603-04
(Top View)



**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02


Output 1
Gate 2
Non-Inv. Input B 3
Inv. Input B 4
Non-Inv. Input A 5
Inv. Input A 6
Output 7
14 NC
13 NC
12 NC
11 NC
10 NC
9 VCC
8 VEE
B
A

(Top View)

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +12<br>-12 | Vdc<br>Vdc |
| Input Differential Voltage Range | $V_{IDR}$ | ±5.0 | Volts |
| Load Current | $I_L$ | 25 | mA |
| Power Dissipation (Package Limitation)<br>Flat Package<br>Derate above $T_A$ = +25°C<br>Ceramic Dual In-Line Package<br>Derate above $T_A$ = +25°C<br>Metal Can<br>Derate above $T_A$ = +25°C | $P_D$ | <br>500<br>3.3<br>625<br>5.0<br>680<br>4.6 | <br>mW<br>mW/°C<br>mW<br>mW/°C<br>mW<br>mW/°C |
| Operating Ambient Temperature Range MC1445<br>MC1545 | $T_A$ | 0 to +75<br>-55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $V_{EE}$ = 5.0 Vdc, at $T_A$ = +25°C, specifications apply to both input channels unless otherwise noted.)

| Characteristic | Fig. No. | Symbol | MC1545 | | | MC1445 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Single-Ended Voltage Gain | 1,12 | $A_{vs}$ | 16 | 19 | 21 | 16 | 19.5 | 23 | dB |
| Bandwidth | 1,12 | BW | 40 | 50 | – | – | 50 | – | MHz |
| Input Impedance (f = 50 kHz) | 5,14 | $z_i$ | 4.0 | 10 | – | 3.0 | 10 | – | k ohms |
| Output Impedance (f = 50 kHz) | 6,15 | $z_o$ | – | 25 | – | – | 25 | – | Ohms |
| Output Differential Voltage Range ($R_L$ = 1.0 k ohm, f = 50 kHz) | 4,13 | $V_{ODR}$ | 1.5 | 2.5 | – | 1.5 | 2.5 | – | Vp-p |
| Input Bias Current | 16 | $I_{IB}$ | – | 15 | 25 | – | 15 | 30 | μAdc |
| Input Offset Current | 16 | $I_{IO}$ | – | 2.0 | – | – | 2.0 | – | μAdc |
| Input Offset Voltage | 17 | $V_{IO}$ | – | 1.0 | 5.0 | – | – | 7.5 | mVdc |
| Quiescent Output dc Level | 17 | $V_O$ | – | 0.1 | – | – | 0.1 | – | Vdc |
| Output dc Level Change (Gate Input Voltage Change: +5.0 V to 0 V) | 17 | $\Delta V_O$ | – | ±15 | – | – | ±15 | – | mV |
| Common-Mode Rejection Ratio (f = 50 kHz) | 9,18 | CMRR | – | 85 | – | – | 85 | – | dB |
| Input Common-Mode Voltage Range | 18 | $V_{ICR}$ | – | ±2.5 | – | – | ±2.5 | – | Vp |
| Gate Characteristics<br>Gate Input Voltage – Low Logic State (Note 1) | 8 | $V_{IL(G)}$ | 0.40 | 0.70 | – | 0.2 | 0.4 | – | Vdc |
| Gate Input Voltage – High Logic State (Note 2) | | $V_{IH(G)}$ | – | 1.5 | 2.2 | – | 1.3 | 3.0 | |
| Gate Input Current – Low Logic State ($V_{IL(G)}$ = 0 V) | 18 | $I_{IL(G)}$ | – | – | 2.5 | – | – | 4.0 | mA |
| Gate Input Current – High Logic State ($V_{IH(G)}$ = +5.0 V) | 18 | $I_{IH(G)}$ | – | – | 2.0 | – | – | 4.0 | μA |
| Step Response ($e_{in}$ = 20 mV) | 19 | $t_{PLH}$ | – | 6.5 | 10 | – | 6.5 | – | ns |
| | | $t_{PHL}$ | – | 6.3 | 10 | – | 6.3 | – | |
| | | $t_{TLH}$ | – | 6.5 | 15 | – | 6.5 | – | |
| | | $t_{THL}$ | – | 7.0 | 15 | – | 7.0 | – | |
| Wideband Input Noise (5.0 Hz – 10 MHz, $R_S$ = 50 ohms) | 10,20 | $e_n$ | – | 25 | – | – | 25 | – | μV(rms) |
| DC Power Consumption | 11,20 | $P_C$ | – | 70 | 110 | – | 70 | 150 | mW |

Note 1. $V_{IL(G)}$ is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
Note 2. $V_{IH(G)}$ is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

FIGURE 1 – SINGLE-ENDED VOLTAGE GAIN versus FREQUENCY

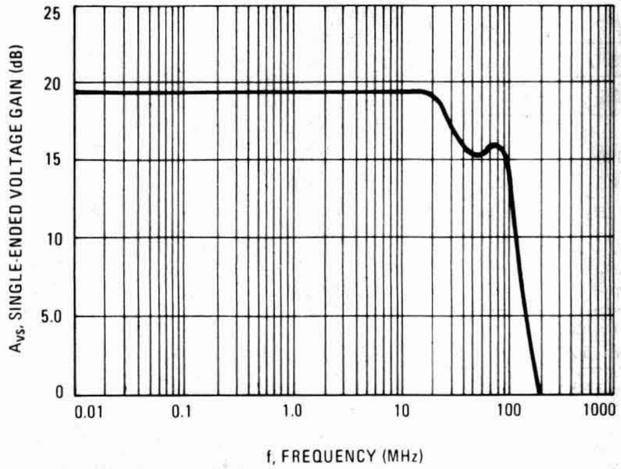


FIGURE 2 – SINGLE-ENDED VOLTAGE GAIN versus TEMPERATURE

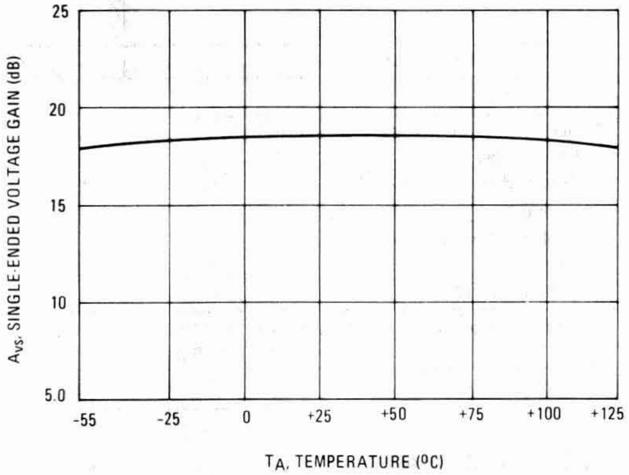


FIGURE 3 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGES

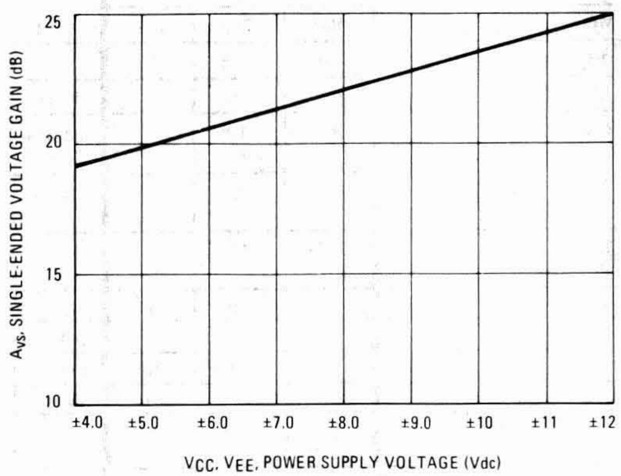


FIGURE 4 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

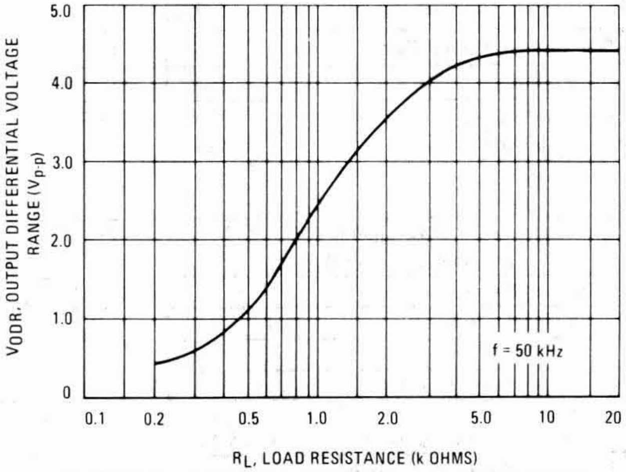


FIGURE 5 – INPUT Cp AND Rp versus FREQUENCY (BOTH CHANNELS)

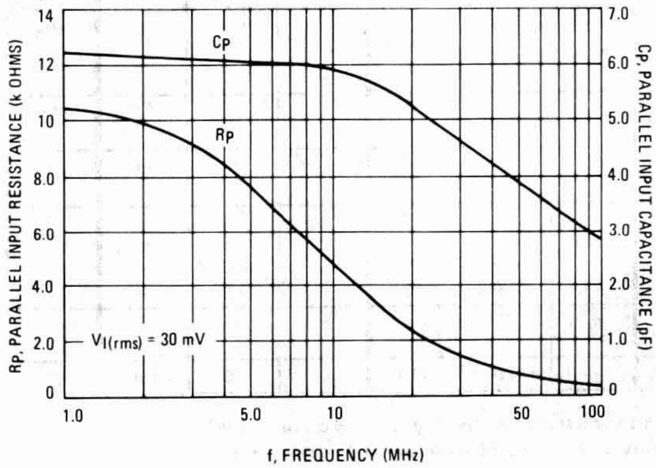


FIGURE 6 – OUTPUT IMPEDANCE versus FREQUENCY

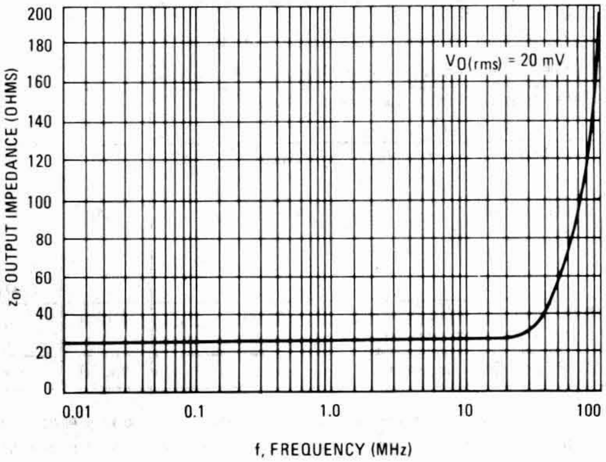


FIGURE 7 – CHANNEL SEPARATION versus FREQUENCY

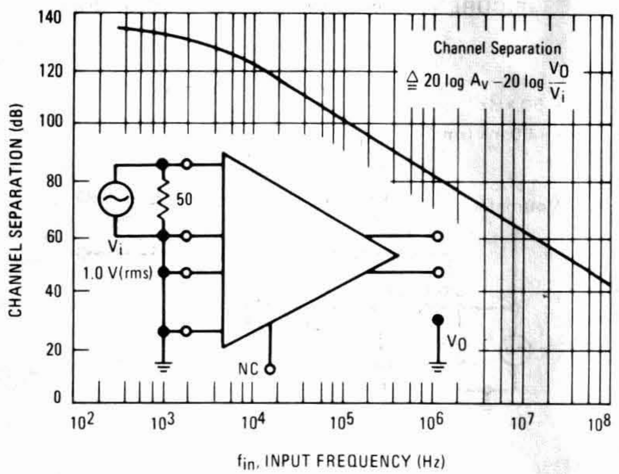


FIGURE 8 – GATE CHARACTERISTICS

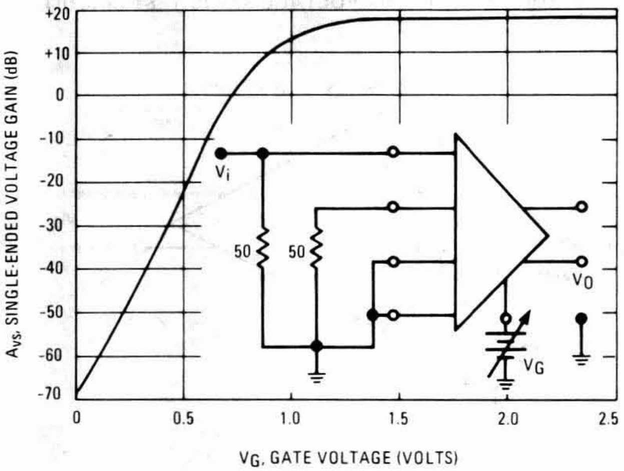


FIGURE 9 – COMMON MODE REJECTION RATIO versus FREQUENCY

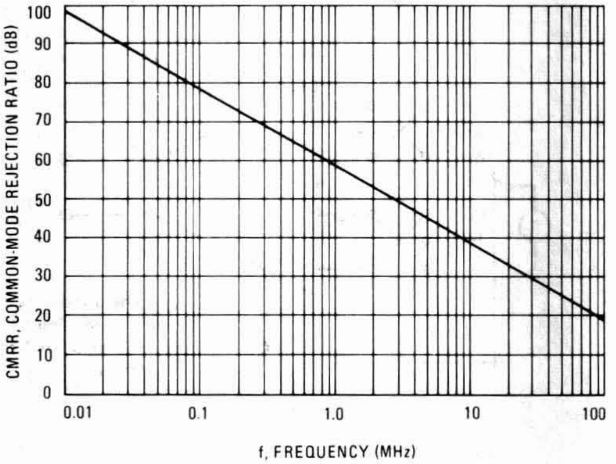


FIGURE 10 – INPUT WIDEBAND NOISE versus SOURCE RESISTANCE

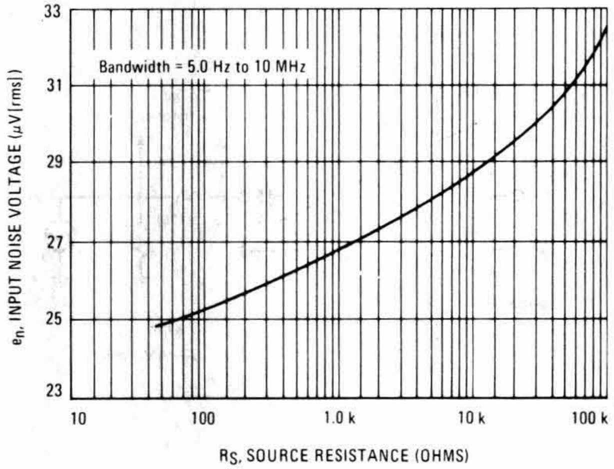


FIGURE 11 – CIRCUIT SCHEMATIC

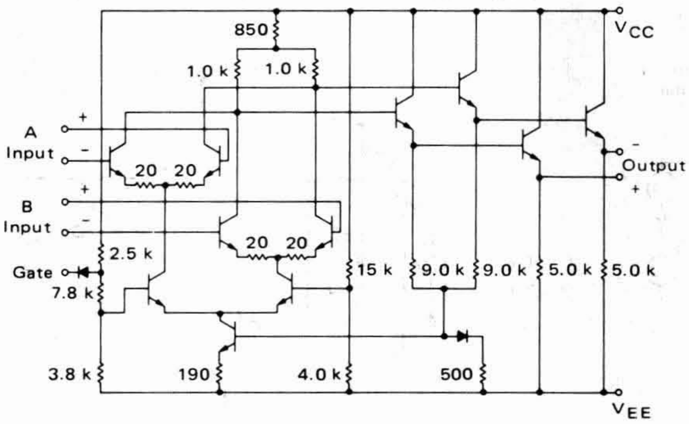
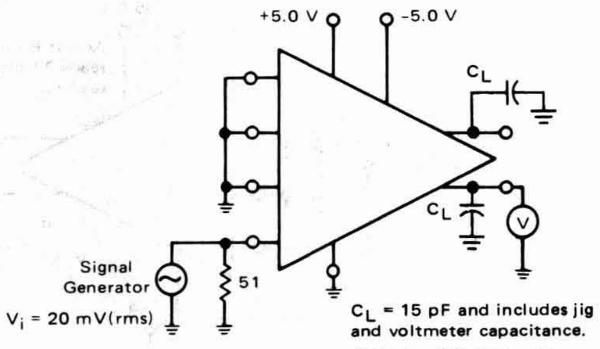

850
1.0 k
1.0 k
$V_{CC}$
A
Input
+
−
20
20
B
Input
+
−
20
20
Gate
2.5 k
7.8 k
15 k
9.0 k
9.0 k
5.0 k
5.0 k
Output
−
+
3.8 k
190
4.0 k
500
$V_{EE}$

FIGURE 12 – SINGLE-ENDED VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT


+5.0 V
-5.0 V
$C_L$
$C_L$
V
Signal Generator
$V_i$ = 20 mV(rms)
51

$C_L$ = 15 pF and includes jig and voltmeter capacitance.

Boonton RF Voltmeter or Equivalent

FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

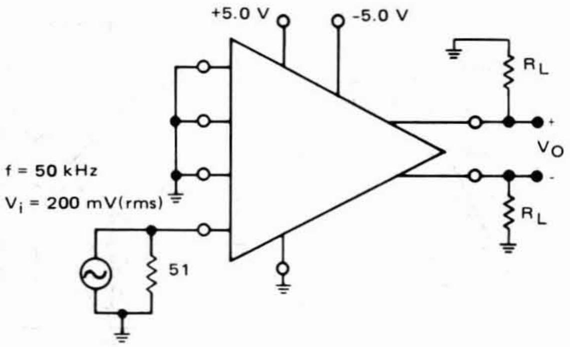

+5.0 V
-5.0 V
$R_L$
+
$V_O$
-
$R_L$
f = 50 kHz
$V_i$ = 200 mV(rms)
51

FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

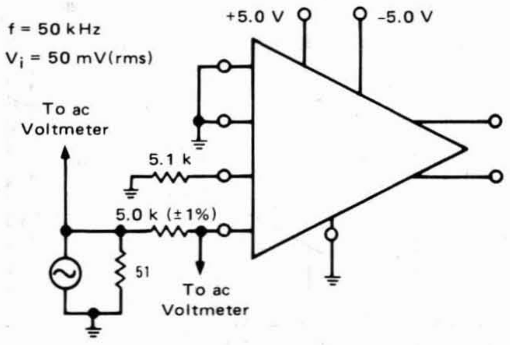

f = 50 kHz
$V_i$ = 50 mV(rms)
+5.0 V
-5.0 V
To ac Voltmeter
5.1 k
5.0 k (±1%)
51
To ac Voltmeter

FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

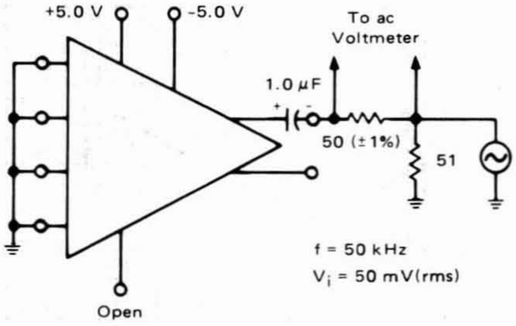
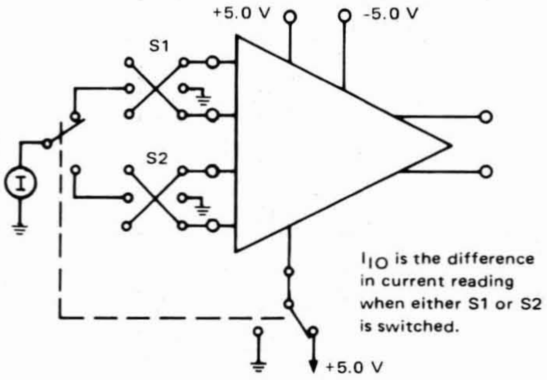
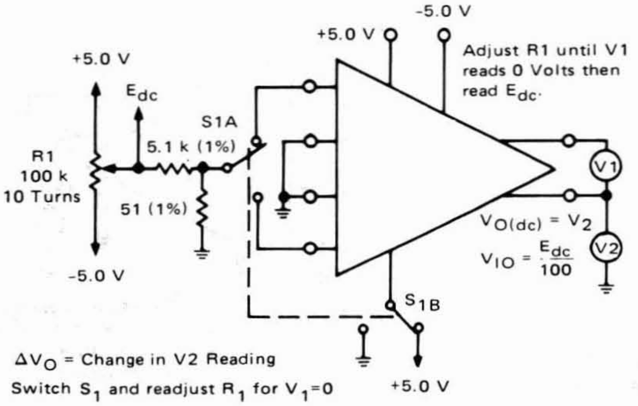

+5.0 V
-5.0 V
To ac Voltmeter
1.0 μF
+
-
50 (±1%)
51
f = 50 kHz
$V_i$ = 50 mV(rms)
Open

FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT


+5.0 V
-5.0 V
S1
S2
I
+5.0 V

$I_{IO}$ is the difference in current reading when either S1 or S2 is switched.

FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT


-5.0 V
+5.0 V
+5.0 V
$E_{dc}$
S1A
R1
100 k
10 Turns
5.1 k (1%)
51 (1%)
-5.0 V
V1
V2
$S_{1B}$
+5.0 V

Adjust R1 until V1 reads 0 Volts then read $E_{dc}$.

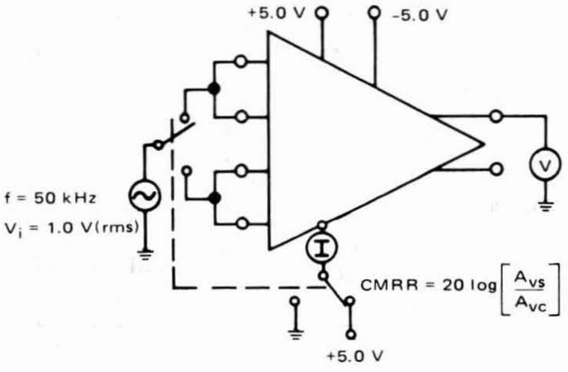
$V_{O(dc)} = V_2$

$V_{IO} = \frac{E_{dc}}{100}$

$\Delta V_O$ = Change in V2 Reading

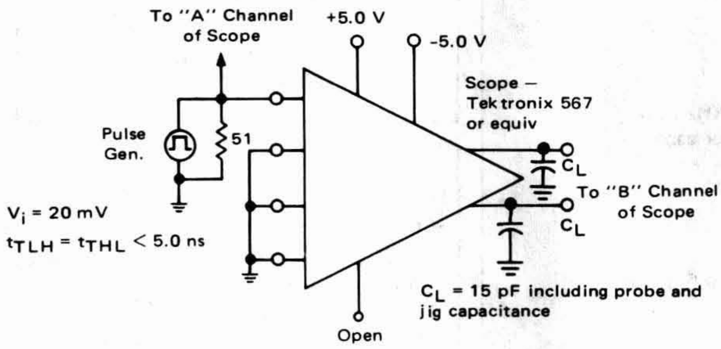
Switch $S_1$ and readjust $R_1$ for $V_1 = 0$

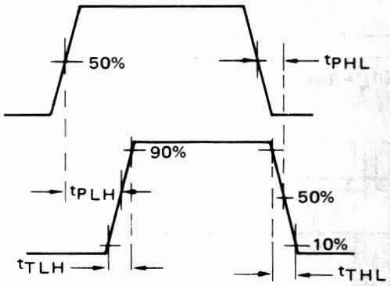
FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT


+5.0 V
-5.0 V
V
f = 50 kHz
$V_i$ = 1.0 V(rms)
I
+5.0 V

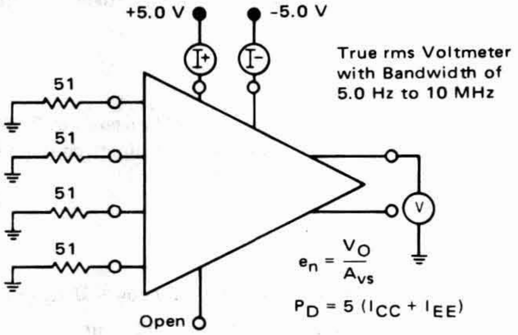
$\mathrm{CMRR} = 20 \log \left[\frac{A_{vs}}{A_{vc}}\right]$

### FIGURE 19 – PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT

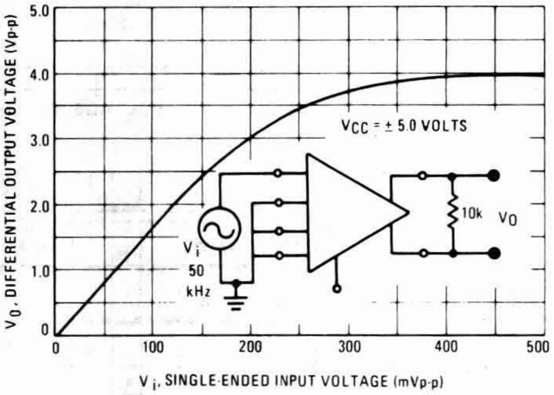

To "A" Channel of Scope
+5.0 V
-5.0 V
Scope – Tektronix 567 or equiv
Pulse Gen.
51
$C_L$
To "B" Channel of Scope
$C_L$
$V_i$ = 20 mV
$t_{TLH} = t_{THL} < 5.0$ ns
$C_L$ = 15 pF including probe and jig capacitance
Open


50%
$t_{PHL}$
90%
$t_{PLH}$
50%
10%
$t_{TLH}$
$t_{THL}$

### FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT


+5.0 V
-5.0 V
I+
I-
True rms Voltmeter with Bandwidth of 5.0 Hz to 10 MHz
51
51
51
51
V
$e_n = \frac{V_O}{A_{vs}}$
$P_D = 5\,(I_{CC} + I_{EE})$
Open

### FIGURE 21 – LIMITING CHARACTERISTIC



**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1454G | 0°C to +70°C | Metal Can |
| MC1554G | −55°C to +125°C | Metal Can |

# MC1454G
# MC1554G

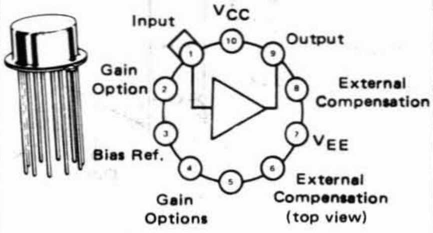
## 1-WATT POWER AMPLIFIERS

. . . designed to amplify signals to 300-kHz with 1-Watt delivered to a direct coupled or capacitively coupled load.

- Low Total Harmonic Distortion – 0.4% (Typ) @ 1 Watt
- Low Output Impedance – 0.2 Ohm
- Excellent Gain – Temperature Stability

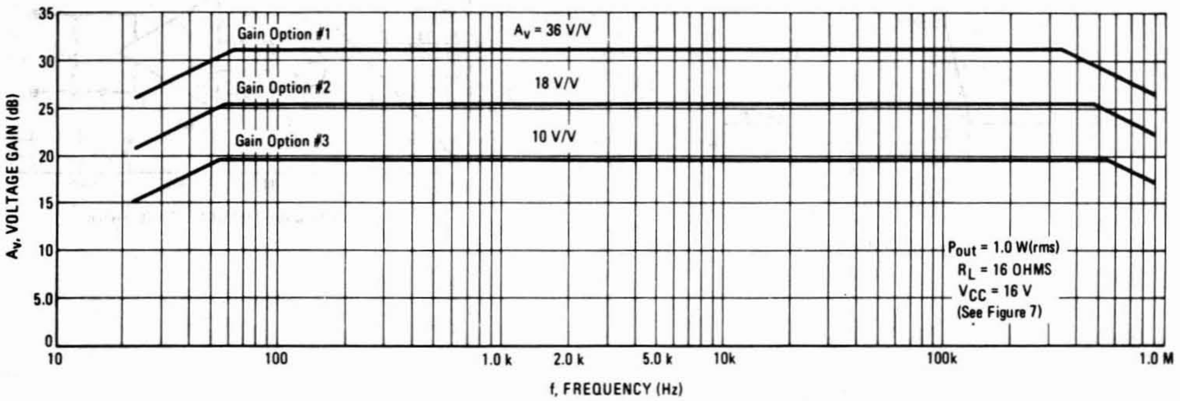
**1-WATT**
**POWER AMPLIFIER**
**INTEGRATED CIRCUIT**

**SILICON MONOLITHIC**
**EPITAXIAL PASSIVATED**

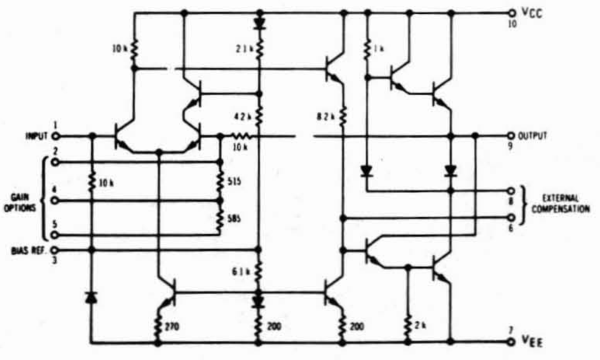

Input
$V_{CC}$
Output
Gain Option
External Compensation
$V_{EE}$
Bias Ref.
External Compensation
Gain Options
(top view)
1
10
9
2
8
3
7
4
5
6

**G SUFFIX**
CASE 603C-01

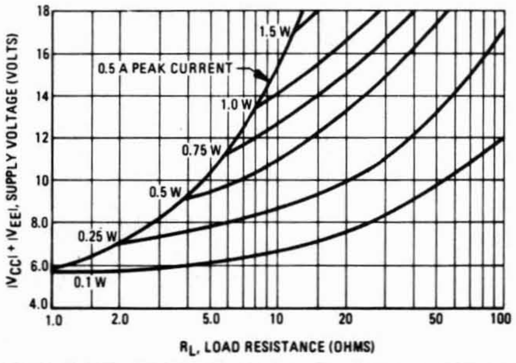
**VOLTAGE GAIN versus FREQUENCY ($R_L$ = 16 OHMS)**



**CIRCUIT SCHEMATIC**


$V_{CC}$
10
10 k
2.1 k
1 k
42 k
82 k
INPUT
1
2
10 k
OUTPUT
9
GAIN OPTIONS
4
5
10 k
515
585
EXTERNAL COMPENSATION
8
6
BIAS REF.
3
61 k
270
200
200
2 k
7
$V_{EE}$

**MAXIMUM AVAILABLE OUTPUT POWER (SINE WAVE)**



**ELECTRICAL CHARACTERISTICS** ($T_C$ = +25°C unless otherwise noted)
Frequency compensation shown in Figures 6 and 7.

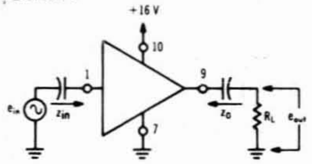
| Characteristic | Figure | $R_L$ (Ohms) | Gain Option* | Symbol | MC1554 (-55 to +125°C) Min | MC1554 Typ | MC1554 Max | MC1454 (0 to +70°C) Min | MC1454 Typ | MC1454 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Output Power (for $e_{out}$<5.0% THD) | 1 | 16 | – | $P_{out}$ | 1.0 | 1.1 | – | – | 1.0 | – | Watt |
| Power Dissipation (@ $P_{out}$ = 1.0 W) | 1 | 16 | – | $P_D$ | – | 0.9 | 1.2 | – | 0.9 | – | Watt |
| Voltage Gain | 1 | 16<br>16<br>16 | 10<br>18<br>36 | $A_v$ | 8.0<br>–<br>– | 10<br>18<br>36 | 12<br>–<br>– | –<br>–<br>– | 10<br>18<br>36 | –<br>–<br>– | V/V |
| Input Impedance | 1 | – | 10 | $z_{in}$ | 7.0 | 10 | – | 3.0 | 10 | – | kΩ |
| Output Impedance | 1 | – | 10 | $z_o$ | – | 0.2 | – | – | 0.4 | – | Ω |
| Power Bandwidth (for $e_{out}$<5.0% THD) | 2 | 16<br>16<br>16 | 10<br>18<br>36 | BW | –<br>–<br>– | 270<br>250<br>210 | –<br>–<br>– | –<br>–<br>– | 270<br>250<br>210 | –<br>–<br>– | kHz |
| Total Harmonic Distortion (for $e_{in}$<0.05% THD, f = 20 Hz to 20 kHz) | 2 | | | THD | | | | | | | % |
| $P_{out}$ = 1.0 Watt (sinewave) | | 16 | 10 | | – | 0.4 | – | – | 0.4 | – | |
| $P_{out}$ = 0.1 Watt (sinewave) | | 16 | 10 | | – | 0.5 | – | – | 0.5 | – | |
| Zero Signal Current Drain | 3 | ∞ | – | $I_D$ | – | 11 | 15 | – | 11 | 20 | mAdc |
| Output Noise Voltage | 3 | 16 | 10 | $V_n$ | – | 0.3 | – | – | 0.3 | – | mV(rms) |
| Output Quiescent Voltage (Split Supply Operation) | 4 | 16 | – | $V_o$ (dc) | – | ±10 | ±30 | – | ±10 | – | mVdc |
| Positive Supply Sensitivity ($V_{EE}$ constant) | 5 | ∞ | – | $S^+$ | – | -40 | – | – | -40 | – | mV/V |
| Negative Supply Sensitivity ($V_{CC}$ constant) | 5 | ∞ | – | $S^-$ | – | -40 | – | – | -40 | – | mV/V |

*To obtain the voltage gain characteristic desired, use the following pin connections:

| Voltage Gain | Pin Connection |
|---|---|
| 10 | Pins 2 and 4 open, Pin 5 to ac ground |
| 18 | Pins 2 and 5 open, Pin 4 to ac ground |
| 36 | Pin 2 connected to Pin 5, Pin 4 to ac ground |

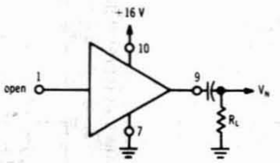
## Characteristic Definitions
(Linear Operation)

**FIGURE 1**



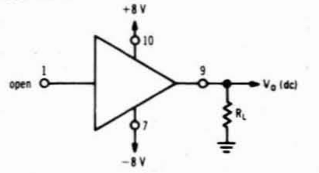
+16 V
10
1
9
$e_{in}$
$z_{in}$
$z_o$
7
$R_L$
$e_{out}$

**FIGURE 3**



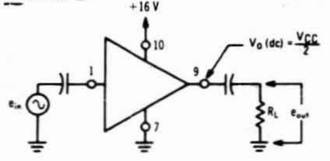
+16 V
10
open
1
9
$V_n$
$R_L$
7

**FIGURE 4**

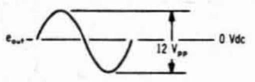


+8 V
10
open
1
9
$V_o$ (dc)
$R_L$
7
-8 V

**FIGURE 2**

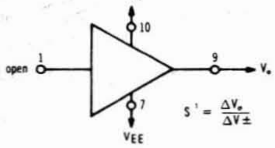


+16 V
10
1
9
$V_o$ (dc) = $\frac{V_{CC}}{2}$
$e_{in}$
$R_L$
$e_{out}$
7



$e_{out}$
12 $V_{pp}$
0 Vdc

**FIGURE 5**



$V_{CC}$
10
open
1
9
$V_o$
7
$V_{EE}$
$S^{\pm} = \frac{\Delta V_o}{\Delta V \pm}$

**MAXIMUM RATINGS** ($T_C$ = +25°C unless otherwise noted)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Total Power Supply Voltage | | $\lvert V_{CC}\rvert + \lvert V_{EE}\rvert$ | 18 | Vdc |
| Peak Load Current | | $I_{out}$ | 0.5 | Ampere |
| Audio Output Power | | $P_{out}$ | 1.8 | Watts |
| Power Dissipation (package limitation) | | | | |
| $T_A$ = +25°C | | $P_D$ | 600 | mW |
| Derate above 25°C | | $1/\theta_{JA}$ | 4.8 | mW/°C |
| $T_C$ = +25°C | | $P_D$ | 1.8 | Watts |
| Derate above 25°C | | $1/\theta_{JC}$ | 14.4 | mW/°C |
| Operating Temperature Range | MC1454<br>MC1554 | $T_A$ | 0 to +70<br>-55 to +125 | °C |
| Storage Temperature Range | | $T_{stg}$ | -55 to +150 | °C |

## TYPICAL CONNECTIONS

**FIGURE 6 – SPLIT SUPPLY OPERATION VOLTAGE GAIN ($A_V$) = 10, $f_{LOW} \approx 25$ Hz**

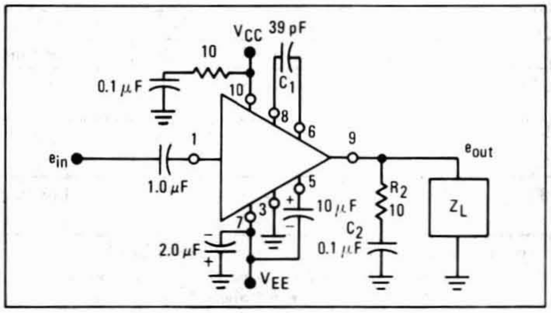
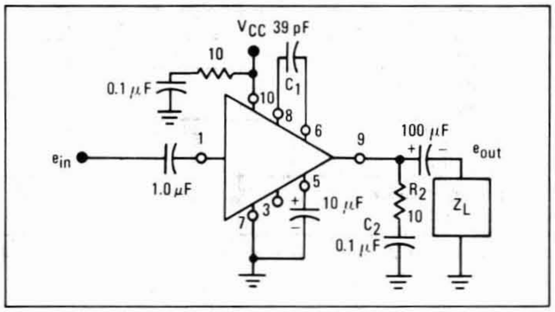


**FIGURE 7 – SINGLE SUPPLY OPERATION VOLTAGE GAIN ($A_V$) = 10, $f_{LOW} \approx 100$ Hz**



## RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to:

1. An R-C stabilizing network (0.1 μF in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 6 and 7, using short leads, to eliminate local VHF instability caused by lead inductance to the load.
2. Excessive lead inductance from the $V_{CC}$ supply to pin 10 can cause high frequency instability. To prevent this, the $V_{CC}$ by-pass capacitor should be connected with short leads from the $V_{CC}$ pin to ground. If this capacitor is remotely located a series R-C network (0.1 μF and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 6 and 7.
3. Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points.

Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads. This can be assured by either (a) use of short leads which are well isolated, (b) narrow-banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low-pass filter in combination with the source impedance, or (c) use of a shielded input cable. In applications which require upper band-edge control the input low-pass filter is recommended.

## TYPICAL CHARACTERISTICS

**FIGURE 8 – TOTAL HARMONIC DISTORTION versus LOAD RESISTANCE**

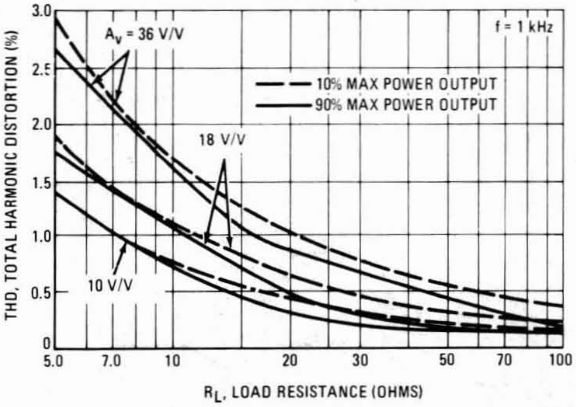
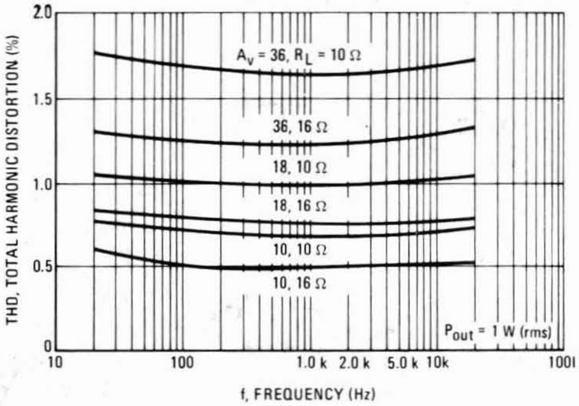


**FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY**



## TYPICAL CHARACTERISTICS (continued)

**FIGURE 10 – VOLTAGE GAIN versus TEMPERATURE**

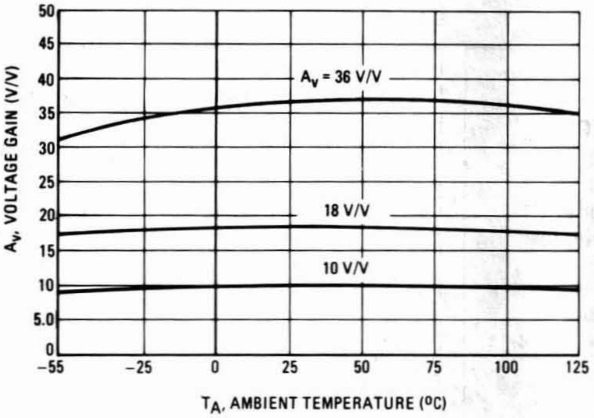


**FIGURE 11 – OUTPUT VOLTAGE CHANGE**

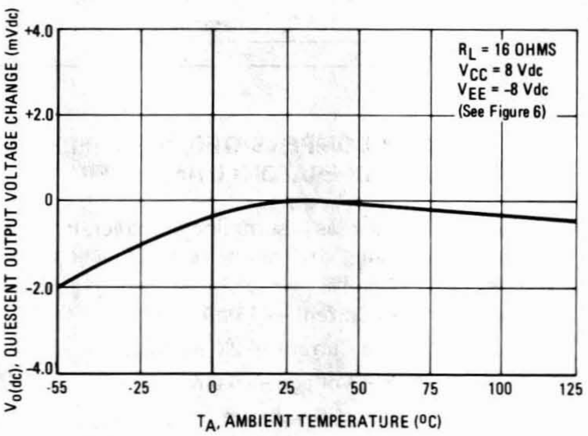


**FIGURE 12 – VOLTAGE GAIN versus FREQUENCY ($R_L = \infty$)**

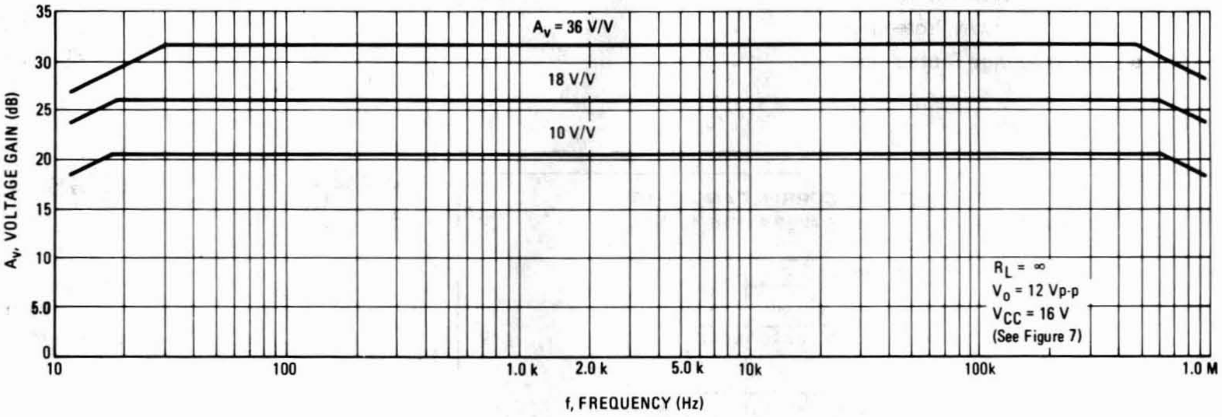
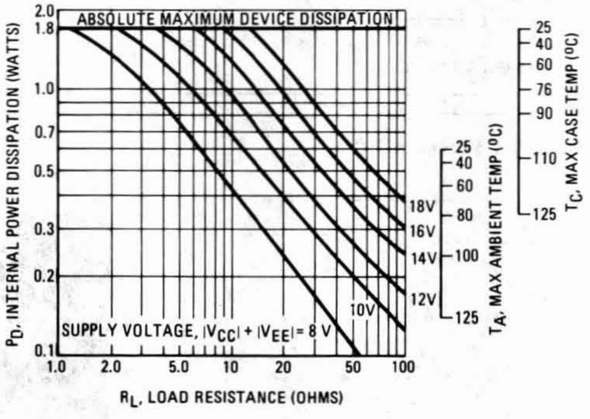


**FIGURE 13 – MAXIMUM DEVICE DISSIPATION (SINE WAVE)**



# MC1456
# MC1456C
# MC1556

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1456G,CG | 0°C to +70°C | Metal Can |
| MC1456CP1,P1 | 0°C to +70°C | Plastic DIP |
| MC1556G | −55°C to +125°C | Metal Can |
| MC1556U | −55°C to +125°C | Ceramic DIP |

## OPERATIONAL AMPLIFIER

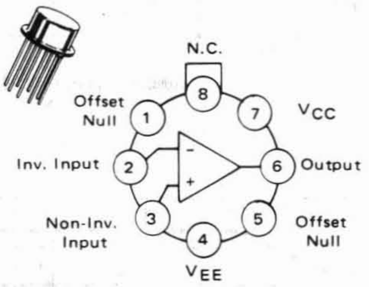
SILICON MONOLITHIC
INTEGRATED CIRCUIT

## INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Low Input Bias Current — 15 nA max
- Low Input Offset Current — 2.0 nA max
- Low Input Offset Voltage — 4.0 mV max
- Fast Slew Rate — 2.5 V/µs typ
- Large Power Bandwidth — 40 kHz typ
- Low Power Consumption — 45 mW max
- Offset Voltage Null Capability
- Output Short-Circuit Protection
- Input Over-Voltage Protection

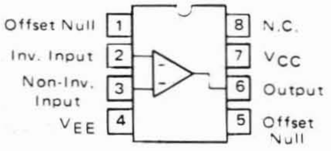
**G PACKAGE**
CASE 601-04


N.C.
8
Offset Null
1
7
VCC
Inv. Input
2
−
+
6
Output
Non-Inv. Input
3
4
5
Offset Null
VEE

(Top View)

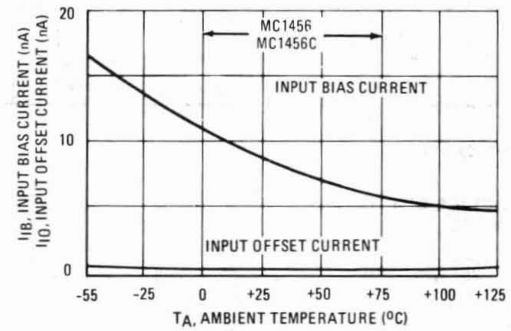
**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04

**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02

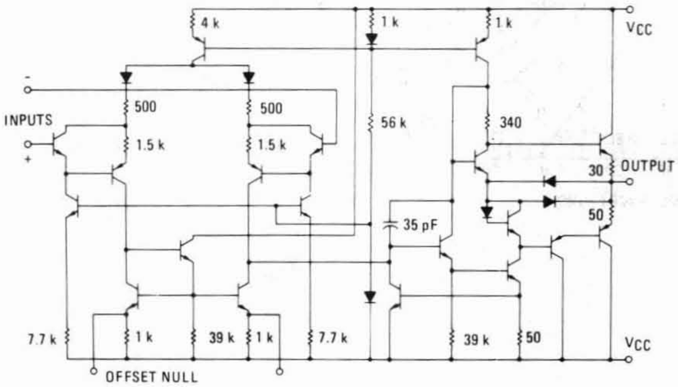

Offset Null
1
Inv. Input
2
Non-Inv. Input
3
VEE
4
8
N.C.
7
VCC
6
Output
5
Offset Null
+
−

(Top View)

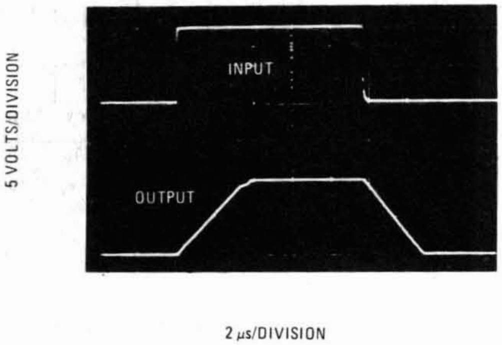
**TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT versus TEMPERATURE for MC1556**



**REPRESENTATIVE CIRCUIT SCHEMATIC**


4 k
1 k
1 k
VCC
500
500
INPUTS
−
+
1.5 k
1.5 k
56 k
340
30
OUTPUT
35 pF
50
7.7 k
1 k
39 k
1 k
7.7 k
39 k
50
VCC
OFFSET NULL

**VOLTAGE-FOLLOWER PULSE RESPONSE**



**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | MC1556 | MC1456<br>MC1456C | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +22<br>-22 | +18<br>-18 | Vdc |
| Differential Input Voltage Range | $V_{IDR}$ | $\pm V_{CC}$ | | Volts |
| Common-Mode Voltage Range | $V_{ICR}$ | $\pm V_{CC}$ | | Volts |
| Load Current | $I_L$ | 20 | | mA |
| Output Short Circuit Duration | $t_S$ | Continuous | | |
| Power Dissipation (Package Limitation)<br>Derate above $T_A$ = +25°C | $P_D$ | 680<br>4.6 | | mW<br>mW/°C |
| Operating Temperature Range | $T_A$ | -55 to +125 | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 Vdc, $V_{EE}$ = - 15 Vdc, $T_A$ = +25°C unless otherwise noted).

| | | | MC1556 | | | MC1456 | | | MC1456C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Characteristic | Fig. | Symbol | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| Input Bias Current | | $I_{IB}$ | | | | | | | | | | nAdc |
| $T_A$ = +25°C | | | – | 8.0 | 15 | – | 15 | 30 | – | 15 | 90 | |
| $T_A$ = $T_{low}$ to $T_{high}$ (See Note 1) | | | – | – | 30 | – | – | 40 | – | – | – | |
| Input Offset Current | | $I_{IO}$ | | | | | | | | | | nAdc |
| $T_A$ = +25°C | | | – | 1.0 | 2.0 | – | 5.0 | 10 | – | 5.0 | 30 | |
| $T_A$ = +25°C to $T_{high}$ | | | – | – | 3.0 | – | – | 14 | – | – | – | |
| $T_A$ = $T_{low}$ to +25°C | | | – | – | 5.0 | – | – | 14 | – | – | – | |
| Input Offset Voltage | | $V_{IO}$ | | | | | | | | | | mVdc |
| $T_A$ = +25°C | | | – | 2.0 | 4.0 | – | 5.0 | 10 | – | 5.0 | 12 | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | | – | – | 6.0 | – | – | 14 | – | – | – | |
| Differential Input Impedance (Open-Loop, f = 20 Hz) | | | | | | | | | | | | |
| Parallel Input Resistance | | $r_p$ | – | 5.0 | – | – | 3.0 | – | – | 3.0 | – | Megohms |
| Parallel Input Capacitance | | $c_p$ | – | 6.0 | – | – | 6.0 | – | – | 6.0 | – | pF |
| Common-Mode Input Impedance (f = 20 Hz) | | $z_i$ | – | 250 | – | – | 250 | | – | 250 | – | Megohms |
| Common-Mode Input Voltage Range | 1 | $V_{ICR}$ | ±12 | ±13 | – | +11 | ±12 | – | ±10.5 | ±12 | – | $V_{pk}$ |
| Equivalent Input Noise Voltage ($A_V$ = 100, $R_s$ = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz) | 2 | $e_n$ | – | 45 | | | 45 | – | – | 45 | – | nV/(Hz)½ |
| Common-Mode Rejection Ratio (f = 100 Hz) | 3 | CMRR | 80 | 110 | – | 70 | 110 | – | – | 110 | – | dB |
| Open-Loop Voltage Gain, ($V_O$ = ± 10 V, $R_L$ = 2.0 k ohms) | 4,5,6 | $A_{VOL}$ | | | | | | | | | | V/V |
| $T_A$ = +25°C | | | 100,000 | 200,000 | – | 70,000 | 100,000 | – | 25,000 | 100,000 | – | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | | 40,000 | – | – | 40,000 | – | – | – | – | – | |
| Power Bandwidth ($A_V$ = 1, $R_L$ = 2.0 k ohms, THD≤5%, $V_O$ = 20 Vp-p) | 9 | $BW_p$ | – | 40 | – | – | 40 | – | | 40 | – | kHz |
| Unity Gain Crossover Frequency (open-loop) | 5 | BW | – | 1.0 | – | – | 1.0 | – | – | 1.0 | – | MHz |
| Phase Margin (open-loop, unity gain) | 5,7 | | – | 70 | – | – | 70 | – | – | 70 | – | degrees |
| Gain Margin | 5,7 | | – | 18 | – | – | 18 | – | – | 18 | – | dB |
| Slew Rate (Unity Gain) | | SR | – | 2.5 | – | – | 2.5 | – | – | 2.5 | – | V/µs |
| Output Impedance (f = 20 Hz) | | $z_o$ | – | 1.0 | 2.0 | – | 1.0 | 2.5 | – | 1.0 | – | kohms |
| Short-Circuit Output Current | 8 | $I_{OS}$ | – | -17, +9.0 | – | – | -17, +9.0 | – | – | -17, +9.0 | – | mAdc |
| Output Voltage Swing ($R_L$ = 2.0 k ohms) | 10 | $V_{OR}$ | ±12 | ±13 | – | +11 | ±12 | – | ±10 | ±12 | – | $V_{pk}$ |
| Power Supply Rejection Ratio | | | | | | | | | | | | µV/V |
| $V_{CC}$ = constant, $R_S \leqslant$ 10 k ohms | | PSRR+ | | 50 | 100 | – | 75 | 200 | – | 75 | – | |
| $V_{EE}$ = constant, $R_S \leqslant$ 10 k ohms | | PSRR- | | 50 | 100 | – | 75 | 200 | – | 75 | – | |
| Power Supply Current | | $I_{CC}$ | – | 1.0 | 1.5 | – | 1.3 | 3.0 | – | 1.3 | 4.0 | mAdc |
| | | $I_{EE}$ | – | 1.0 | 1.5 | – | 1.3 | 3.0 | – | 1.3 | 4.0 | |
| DC Quiescent Power Dissipation ($V_O$ = 0) | 11 | $P_D$ | – | 30 | 45 | – | 40 | 90 | – | 40 | 120 | mW |

Note 1: $T_{low}$: 0° for MC1456 and MC1456C
-55°C for MC1556
$T_{high}$: +70°C for MC1456 and MC1456C
+125°C for MC1556

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C unless otherwise noted).

FIGURE 1 – INPUT COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

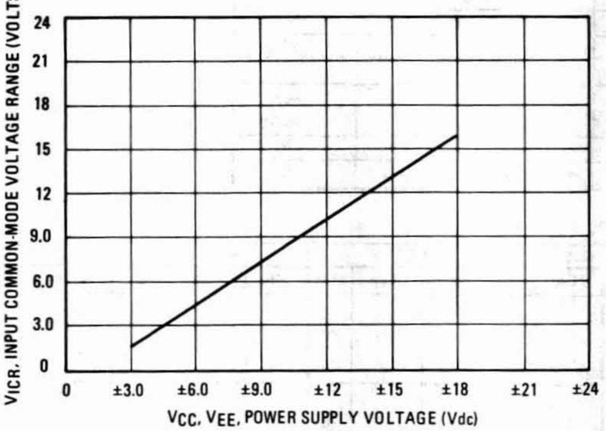


FIGURE 2 – SPECTRAL NOISE DENSITY

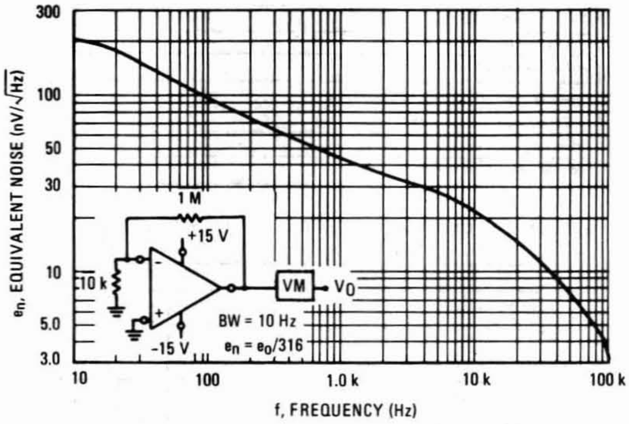


FIGURE 3 – COMMON-MODE REJECTION RATIO versus FREQUENCY

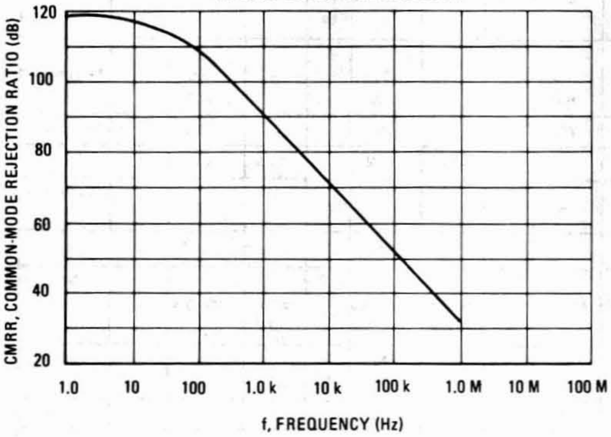


FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

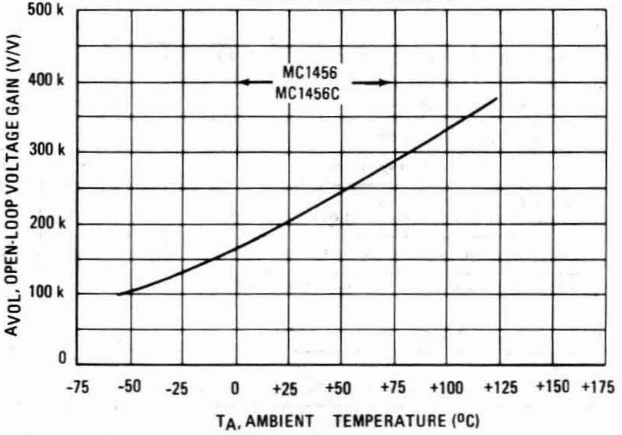


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

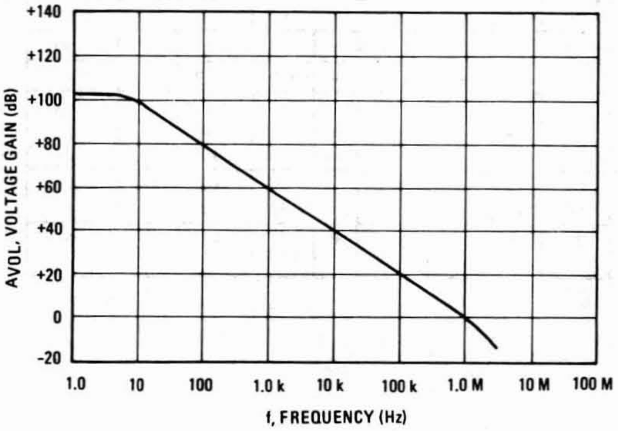
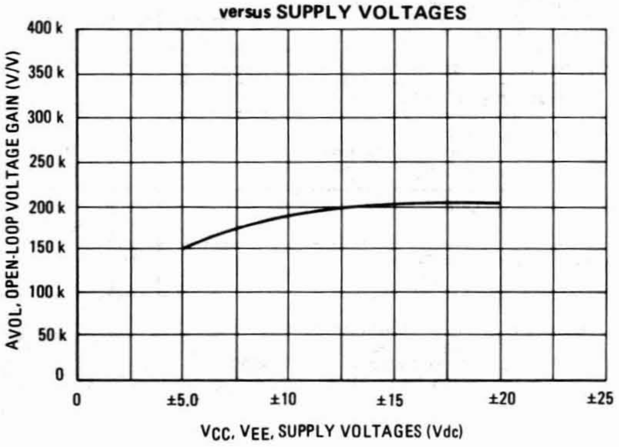


FIGURE 6 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGES



## TYPICAL CHARACTERISTICS (continued)

**FIGURE 7 – OPEN-LOOP PHASE SHIFT**

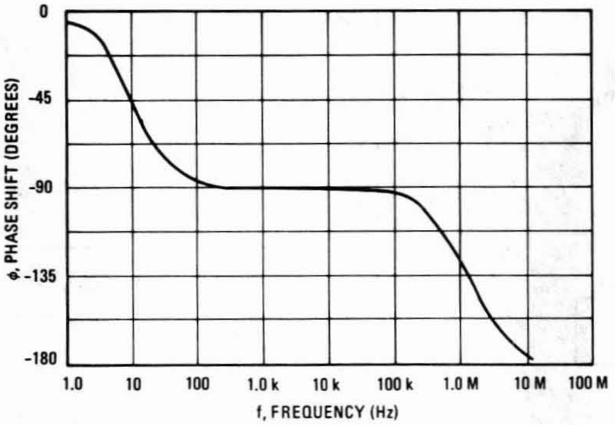


**FIGURE 8 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE**

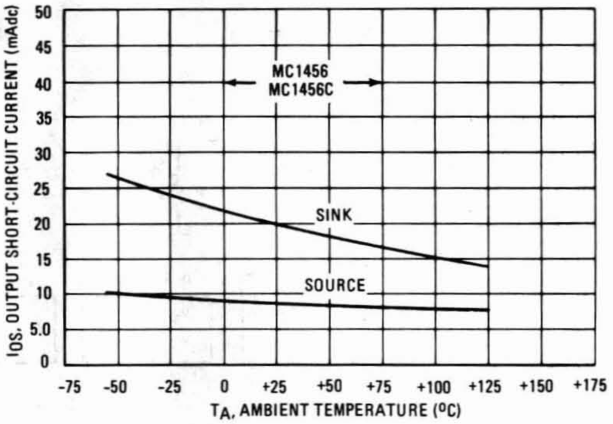


**FIGURE 9 – POWER BANDWIDTH**

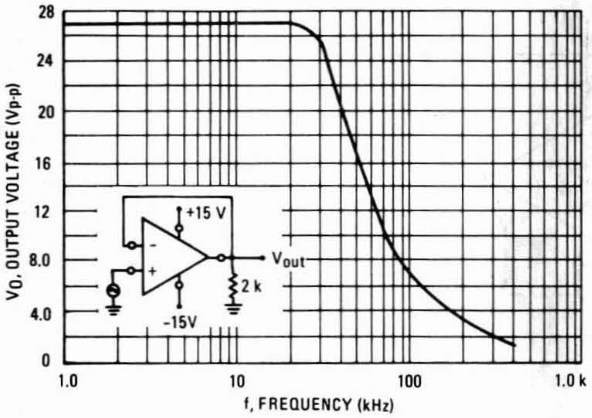


**FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE**

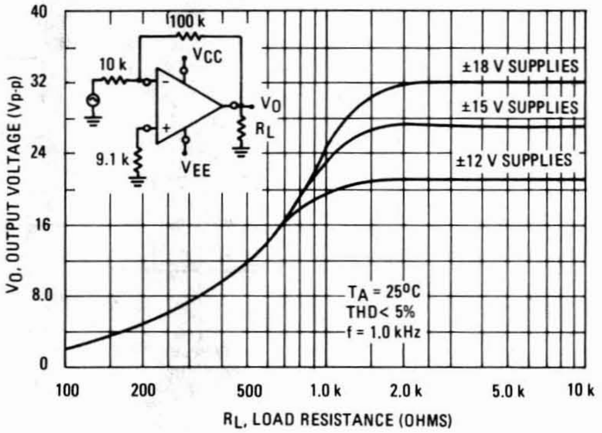
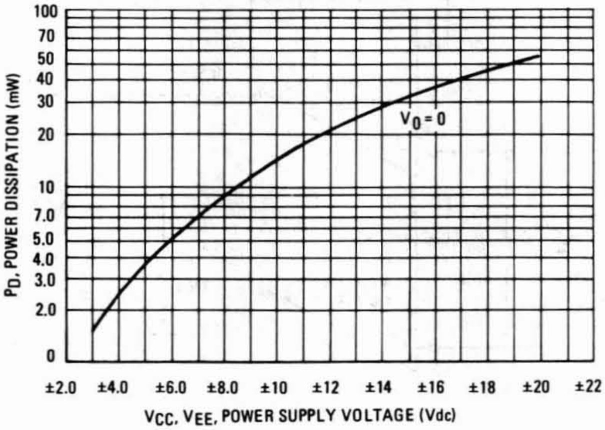


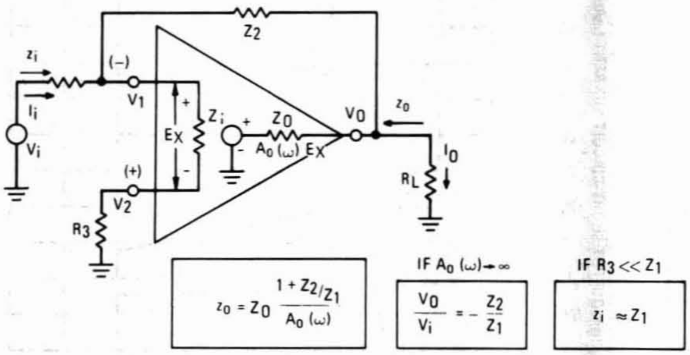
**FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE**



## TYPICAL APPLICATIONS

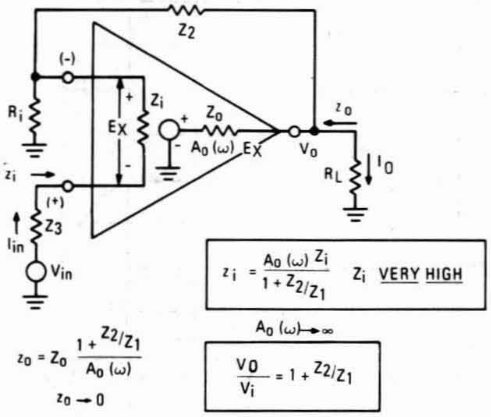
Where values are not given for external components they must be selected by the designer to fit the requirements of the system.

FIGURE 12 — INVERTING FEEDBACK MODEL



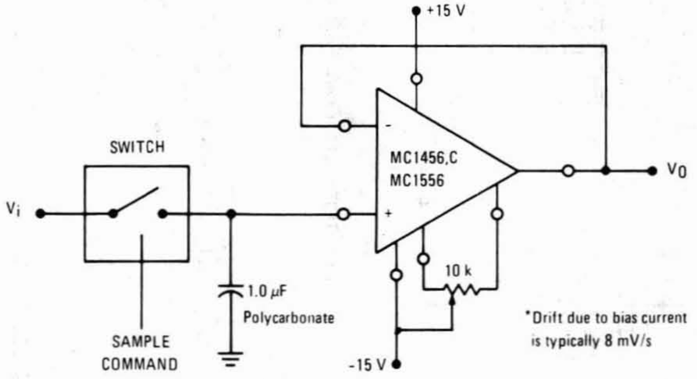
Z2
zi
Ii
Vi
(−)
V1
(+)
V2
R3
Ex
Zi
Z0
A0 (ω) EX
V0
z0
I0
RL
$z_0 = Z_0 \frac{1 + Z_2/Z_1}{A_0(\omega)}$
IF $A_0(\omega) \to \infty$
$\frac{V_0}{V_i} = -\frac{Z_2}{Z_1}$
IF $R_3 << Z_1$
$z_i \approx Z_1$

FIGURE 13 — NONINVERTING FEEDBACK MODEL



Z2
(−)
Ri
Zi
Ex
Zo
Ao (ω) Ex
Vo
zo
Io
RL
zi
(+)
Z3
Iin
Vin
$z_i = \frac{A_0(\omega) Z_i}{1 + Z_2/Z_1}$ Zi VERY HIGH
$A_0(\omega) \to \infty$
$\frac{V_0}{V_i} = 1 + Z_2/Z_1$
$z_0 = Z_0 \frac{1 + Z_2/Z_1}{A_0(\omega)}$
$z_0 \to 0$

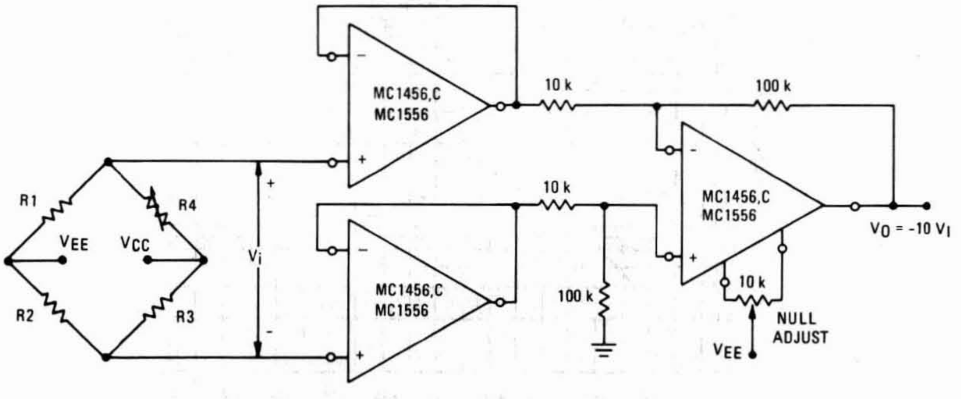
FIGURE 14 — LOW-DRIFT SAMPLE AND HOLD



+15 V
SWITCH
Vi
MC1456,C
MC1556
Vo
1.0 μF
Polycarbonate
SAMPLE
COMMAND
10 k
-15 V

*Drift due to bias current is typically 8 mV/s

FIGURE 15 — HIGH IMPEDANCE BRIDGE AMPLIFIER



MC1456,C
MC1556
10 k
100 k
R1
R4
VEE
VCC
R2
R3
Vi
+
−
100 k
10 k
NULL
ADJUST
VEE
Vo = -10 Vi

## TYPICAL APPLICATIONS (continued)

**FIGURE 16 – LOGARITHMIC AMPLIFIER**

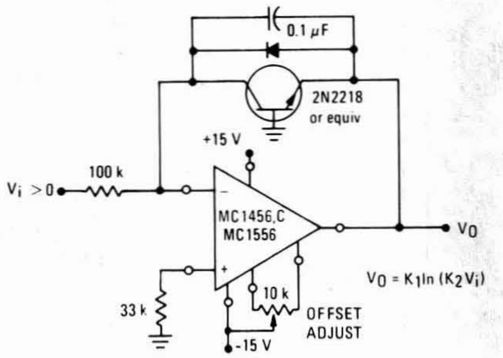

0.1 μF
2N2218
or equiv
+15 V
100 k
$V_i > 0$
MC1456,C
MC1556
$V_O$
$V_O = K_1 \ln (K_2 V_i)$
33 k
10 k
OFFSET
ADJUST
-15 V

**FIGURE 17 – VOLTAGE OFFSET NULL CIRCUIT**

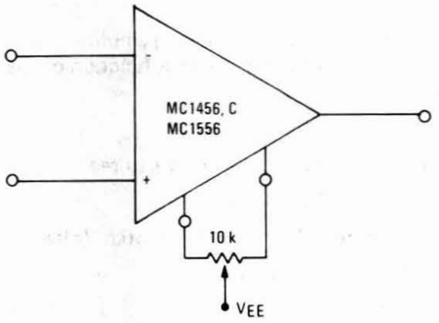
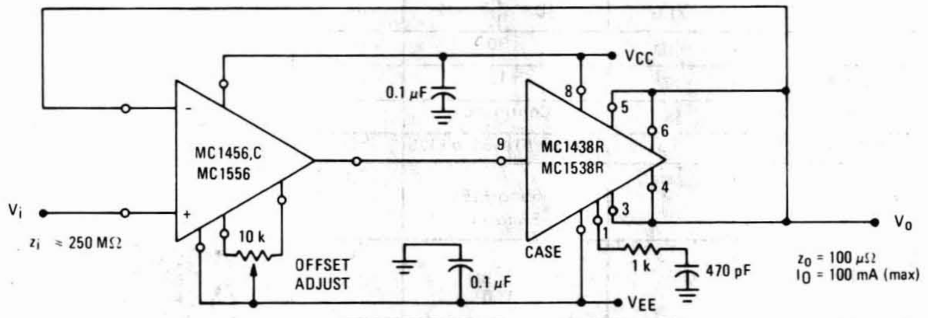

-
+
MC1456, C
MC1556
10 k
$V_{EE}$

**FIGURE 18 – HIGH INPUT IMPEDANCE, HIGH OUTPUT CURRENT VOLTAGE FOLLOWER**


$V_{CC}$
0.1 μF
8
5
6
-
MC1456,C
MC1556
9
MC1438R
MC1538R
4
3
1
$V_i$
+
$z_i \approx 250\ M\Omega$
10 k
OFFSET
ADJUST
0.1 μF
CASE
1 k
470 pF
$V_{EE}$
$V_o$
$z_o = 100\ \mu\Omega$
$I_O = 100$ mA (max)

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1458CD,D | 0°C to +70°C | SO-8 |
| MC1458G,CG | 0°C to +70°C | Metal Can |
| MC1558G | −55°C to +125°C | Metal Can |
| MC1458CU | 0°C to +70°C | Ceramic DIP |
| MC1558U | −55°C to +125°C | Ceramic DIP |
| MC1458CP | 0°C to +70°C | Plastic DIP |

# MC1458
# MC1458C
# MC1558

## DUAL MC1741
## INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIERS

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

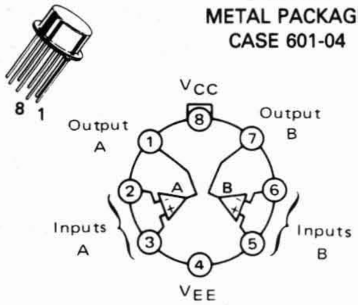
- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

(DUAL MC1741)

## DUAL
## OPERATIONAL AMPLIFIER

**SILICON MONOLITHIC**
**INTEGRATED CIRCUIT**

**G SUFFIX**
METAL PACKAGE
CASE 601-04


8
1
VCC
Output A
Output B
Inputs A
Inputs B
VEE
A
B
1
2
3
4
5
6
7
8

(Top View)

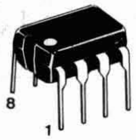
**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | MC1458 | MC1558 | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>-18 | +22<br>-22 | Vdc<br>Vdc |
| Input Differential Voltage | $V_{ID}$ | ±30 | | Volts |
| Input Common Mode Voltage (Note 1) | $V_{ICM}$ | ±15 | | Volts |
| Output Short Circuit Duration (Note 2) | $t_S$ | Continuous | | |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | -55 to +125 | °C |
| Storage Temperature Range<br>Metal and Ceramic Packages<br>Plastic Package | $T_{stg}$ | <br>-65 to +150<br>-55 to +125 | | °C |
| Junction Temperature<br>Metal and Ceramic Packages<br>Plastic Package | $T_J$ | <br>175<br>150 | | °C |

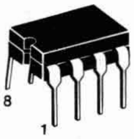
Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

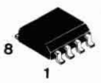
**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(MC1458, MC1458C)

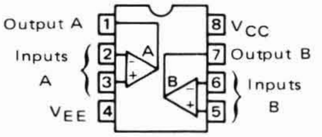


**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02



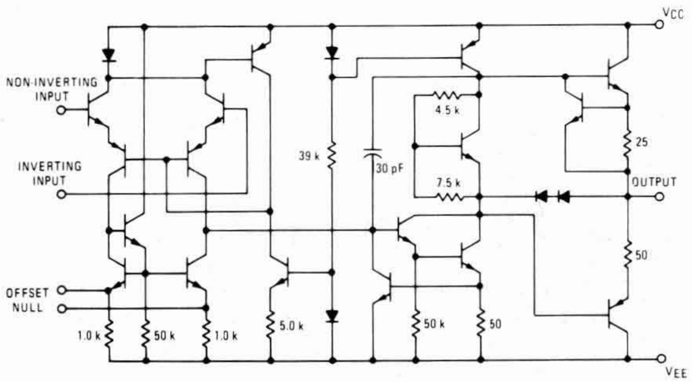
**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8




Output A
Inputs A
VEE
VCC
Output B
Inputs B
A
B
1
2
3
4
5
6
7
8

(Top View)

## EQUIVALENT CIRCUIT SCHEMATIC


VCC
NON-INVERTING INPUT
INVERTING INPUT
OFFSET NULL
4.5 k
39 k
30 pF
7.5 k
25
OUTPUT
50
1.0 k
50 k
1.0 k
5.0 k
50 k
50
VEE

**ELECTRICAL CHARACTERISTICS** – Note 1. ($V_{CC}$ = 15 V, $V_{EE}$ = 15 V, $T_A$ = 25°C unless otherwise noted).

| Characteristic | Symbol | MC1558 | | | MC1458 | | | MC1458C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage<br>($R_S \leqslant 10$ k) | $V_{IO}$ | – | 1.0 | 5.0 | – | 2.0 | 6.0 | – | 2.0 | 10 | mV |
| Input Offset Current | $I_{IO}$ | – | 20 | 200 | – | 20 | 200 | – | 20 | 300 | nA |
| Input Bias Current | $I_{IB}$ | – | 80 | 500 | – | 80 | 500 | – | 80 | 700 | nA |
| Input Resistance | $r_i$ | 0.3 | 2.0 | – | 0.3 | 2.0 | – | – | 2.0 | – | MΩ |
| Input Capacitance | $C_i$ | – | 1.4 | – | – | 1.4 | – | – | 1.4 | – | pF |
| Offset Voltage Adjustment Range | $V_{IOR}$ | – | ±15 | – | – | ±15 | – | – | ±15 | – | mV |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±12 | ±13 | – | ±12 | ±13 | – | ±11 | ±13 | – | V |
| Large Signal Voltage Gain<br>($V_O = \pm 10$ V, $R_L$ = 2.0 k)<br>($V_O = \pm 10$ V, $R_L$ = 10 k) | $A_v$ | <br>50<br>– | <br>200<br>– | <br>–<br>– | <br>20<br>– | <br>200<br>– | <br>–<br>– | <br>–<br>20 | <br>–<br>200 | <br>–<br>– | V/mV |
| Output Resistance | $r_o$ | – | 75 | – | – | 75 | – | – | 75 | – | Ω |
| Common Mode Rejection Ratio<br>($R_S \leqslant 10$ k) | CMRR | 70 | 90 | – | 70 | 90 | – | 60 | 90 | – | dB |
| Supply Voltage Rejection Ratio<br>($R_S \leqslant 10$ k) | PSRR | – | 30 | 150 | – | 30 | 150 | – | 30 | – | µV/V |
| Output Voltage Swing<br>($R_L \geqslant 10$ k)<br>($R_L \geqslant 2$ k) | $V_O$ | <br>±12<br>±10 | <br>±14<br>±13 | <br>–<br>– | <br>±12<br>±10 | <br>±14<br>±13 | <br>–<br>– | <br>±11<br>±9.0 | <br>±14<br>±13 | <br>–<br>– | V |
| Output Short-Circuit Current | $I_{os}$ | – | 20 | – | – | 20 | – | – | 20 | – | mA |
| Supply Currents (Both Amplifiers) | $I_D$ | – | 2.3 | 5.0 | – | 2.3 | 5.6 | – | 2.3 | 8.0 | mA |
| Power Consumption | $P_C$ | – | 70 | 150 | – | 70 | 170 | – | 70 | 240 | mW |
| Transient Response (Unity Gain)<br>($V_I$ = 20 mV, $R_L \geqslant 2$ kΩ, $C_L \leqslant 100$ pF) Rise Time<br>($V_I$ = 20 mV, $R_L \geqslant 2$ kΩ, $C_L \leqslant 100$ pF) Overshoot<br>($V_I$ = 10 V, $R_L \geqslant 2$ kΩ, $C_L \leqslant 100$ pF) Slew Rate | <br>$t_{TLH}$<br>os<br>SR | <br>–<br>–<br>– | <br>0.3<br>15<br>0.5 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>0.3<br>15<br>0.5 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>0.3<br>15<br>0.5 | <br>–<br>–<br>– | <br>µs<br>%<br>V/µs |

**ELECTRICAL CHARACTERISTICS** Note 1 ($V_{CC}$ = 15 V, $V_{EE}$ = 15 V, $T_A$ = *$T_{high}$ to $T_{low}$ unless otherwise noted).

| Characteristic | Symbol | MC1558 | | | MC1458 | | | MC1458C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage<br>($R_S \leqslant 10$ kΩ) | $V_{IO}$ | – | 1.0 | 6.0 | – | – | 7.5 | – | – | 12 | mV |
| Input Offset Current<br>($T_A$ = 125°C)<br>($T_A$ = -55°C)<br>($T_A$ = 0°C to +70°C) | $I_{IO}$ | <br>–<br>–<br>– | <br>7.0<br>85<br>– | <br>200<br>500<br>– | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>–<br>–<br>300 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>–<br>–<br>400 | nA |
| Input Bias Current<br>($T_A$ = 125°C)<br>($T_A$ = -55°C)<br>($T_A$ = 0°C to +70°C) | $I_{IB}$ | <br>–<br>–<br>– | <br>30<br>300<br>– | <br>500<br>1500<br>– | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>–<br>–<br>800 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>–<br>–<br>1000 | nA |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±12 | ±13 | – | – | – | – | – | – | – | V |
| Common Mode Rejection Ratio<br>($R_S \leqslant 10$ k) | CMRR | 70 | 90 | – | – | – | – | – | – | – | dB |
| Supply Voltage Rejection Ratio<br>($R_S \leqslant 10$ k) | PSRR | – | 30 | 150 | – | – | – | – | – | – | µV/V |
| Output Voltage Swing<br>($R_L \geqslant 10$ k)<br>($R_L \geqslant 2$ k) | $V_O$ | <br>±12<br>±10 | <br>±14<br>±13 | <br>–<br>– | <br>±12<br>±10 | <br>±14<br>±13 | <br>–<br>– | <br>–<br>±9.0 | <br>–<br>±13 | <br>–<br>– | V |
| Large Signal Voltage Gain<br>($V_O = \pm 10$ V, $R_L$ = 2 k)<br>($V_O = \pm 10$ V, $R_L$ = 10 k) | $A_v$ | <br>25<br>– | <br>–<br>– | <br>–<br>– | <br>15<br>– | <br>–<br>– | <br>–<br>– | <br>–<br>15 | <br>–<br>– | <br>–<br>– | V/mV |
| Supply Currents (Both Amplifiers)<br>($T_A$ = 125°C)<br>($T_A$ = -55°C) | $I_D$ | <br>–<br>– | <br>–<br>– | <br>4.5<br>6.0 | <br>–<br>– | <br>–<br>– | <br>–<br>– | <br>–<br>– | <br>–<br>– | <br>–<br>– | mA |
| Power Consumption ($T_A$ = 125°C)<br>($T_A$ = -55°C) | $P_C$ | –<br>– | –<br>– | 135<br>180 | –<br>– | –<br>– | –<br>– | –<br>– | –<br>– | –<br>– | mW |

*$T_{high}$ = 125°C for MC1558 and 70°C for MC1458, MC1458C
$T_{low}$ = −55°C for MC1558 and 0°C for MC1458, MC1458C

Note 1. Input pins of an unused amplifier must be grounded for split supply operation or biased at least 3.0 V above $V_{EE}$ for single supply operation.

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

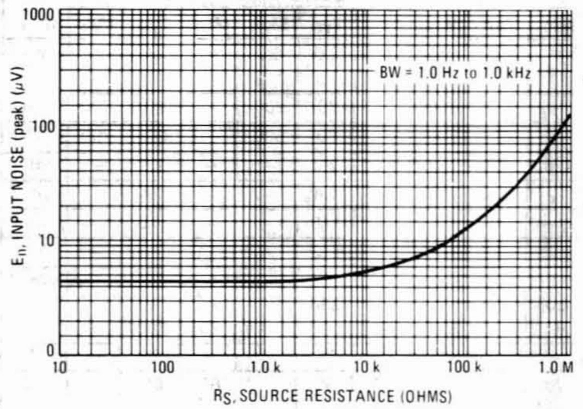


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

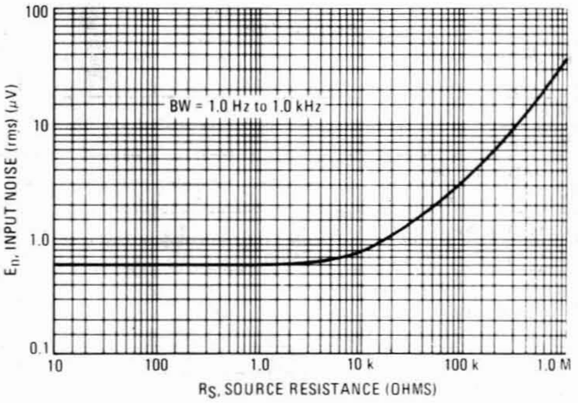


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

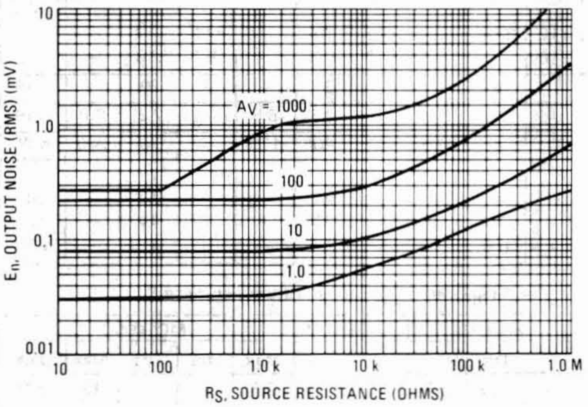


FIGURE 4 – SPECTRAL NOISE DENSITY

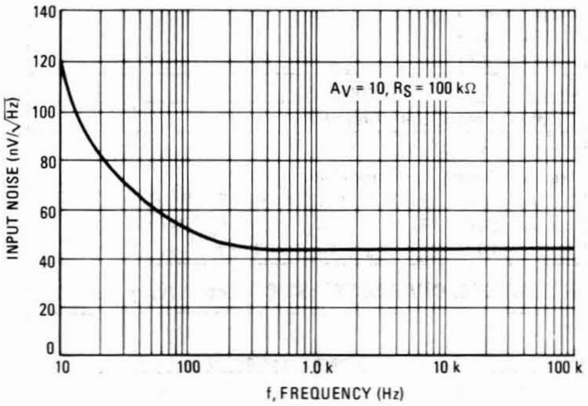
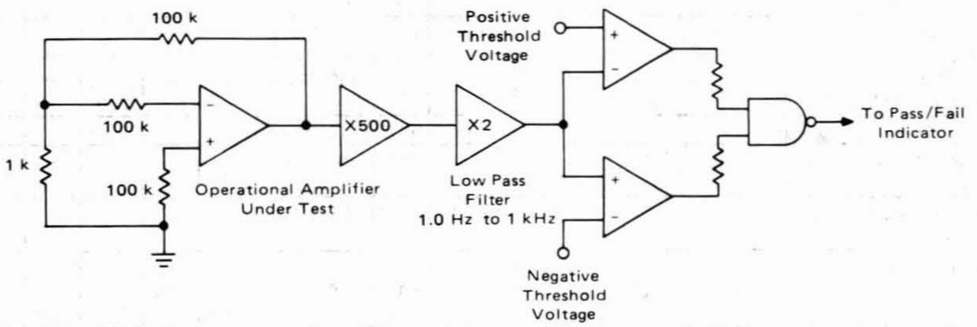


FIGURE 5 – BURST NOISE TEST CIRCUIT


100 k
100 k
1 k
100 k
Operational Amplifier Under Test
X500
X2
Low Pass Filter 1.0 Hz to 1 kHz
Positive Threshold Voltage
Negative Threshold Voltage
To Pass/Fail Indicator

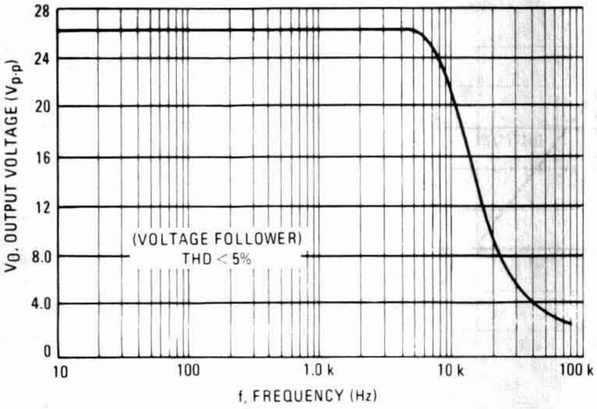
Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

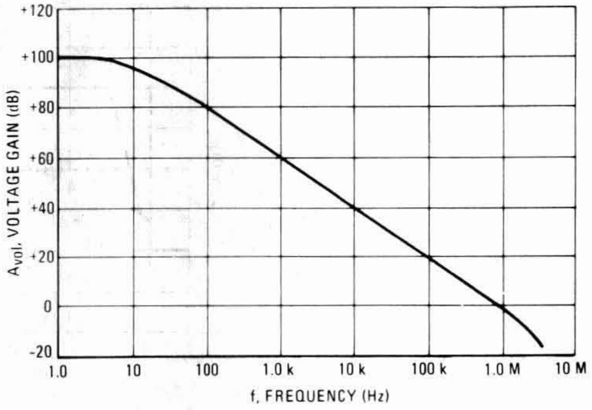
## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $V_{EE}$ = -15 Vdc, $T_A$ = +25°C unless otherwise noted).

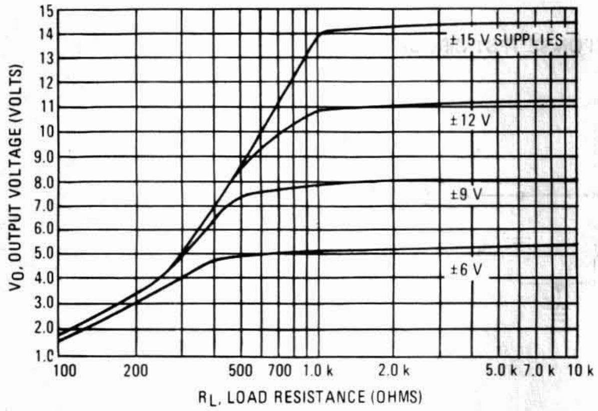
### FIGURE 6 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)



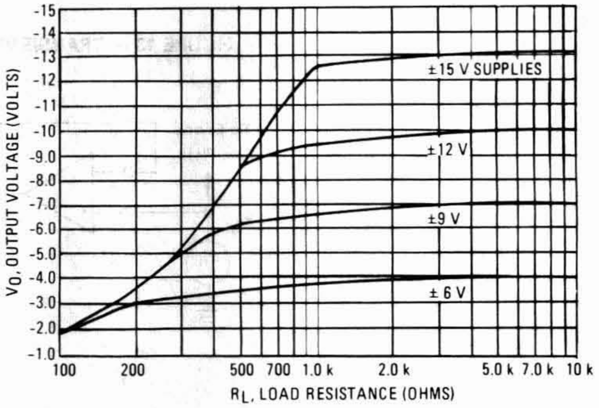
### FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE



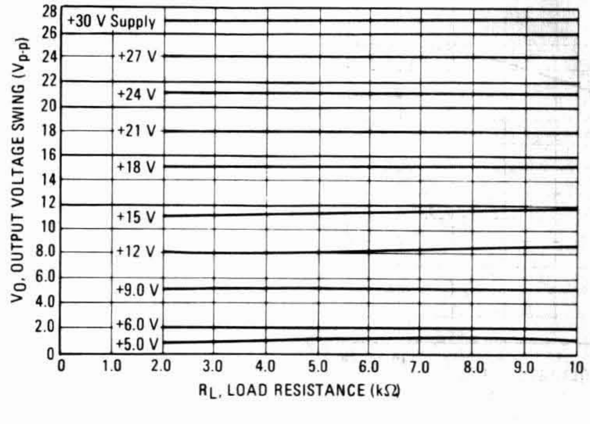
### FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



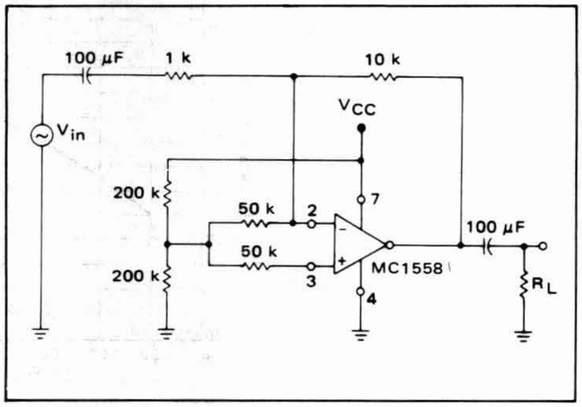
### FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



### FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)



### FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER



100 μF
1 k
10 k
VCC
Vin
200 k
50 k
2
7
50 k
200 k
3
MC1558
4
100 μF
RL

FIGURE 12 — NONINVERTING PULSE RESPONSE

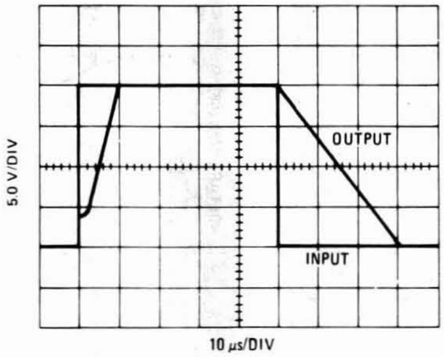


FIGURE 13 — TRANSIENT RESPONSE TEST CIRCUIT

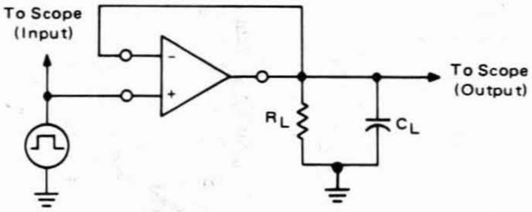
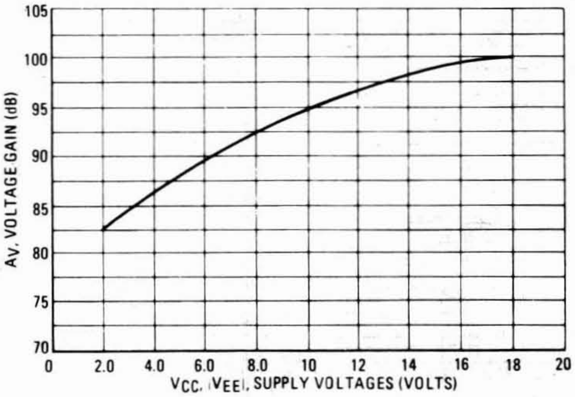

To Scope
(Input)
-
+
$R_L$
$C_L$
To Scope
(Output)

FIGURE 14 — OPEN LOOP VOLTAGE GAIN
versus SUPPLY VOLTAGE



# MC1458S
# MC1558S

**ORDERING INFORMATION**

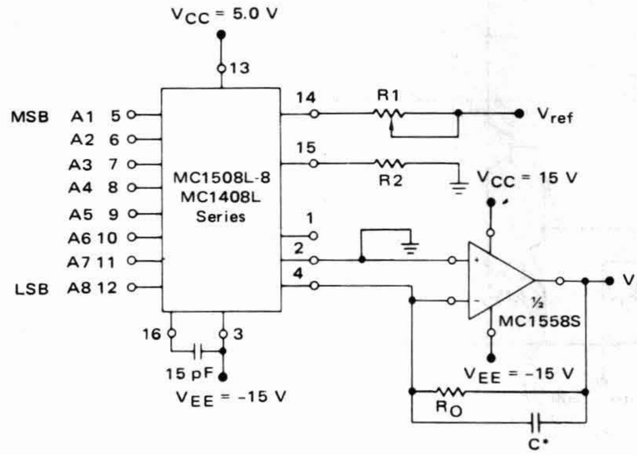
| Device | Temperature Range | Package |
|---|---|---|
| MC1458SD | 0°C to +70°C | SO-8 |
| MC1458SG | 0°C to +70°C | Metal Can |
| MC1458SP1 | 0°C to +70°C | Plastic DIP |
| MC1458SU | 0°C to +70°C | Ceramic DIP |
| MC1558SG | −55°C to +125°C | Metal Can |
| MC1558SU | −55°C to +125°C | Ceramic DIP |

## DUAL HIGH SLEW-RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIERS

The MC1558S is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1558 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D/A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/μs Guaranteed Minimum (for inverting unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

### TYPICAL APPLICATION OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



$V_{CC}$ = 5.0 V
13
14
R1
$V_{ref}$
MSB
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
LSB
A8 12
MC1508L-8
MC1408L
Series
15
R2
$V_{CC}$ = 15 V
1
2
4
$V_O$
½
MC1558S
16
3
15 pF
$V_{EE}$ = −15 V
$V_{EE}$ = −15 V
$R_O$
C*

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical $V_O$

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

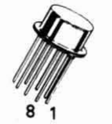
Adjust $V_{ref}$, R1 or $R_O$ so that $V_O$ with all digital inputs at high level is equal to 9.961 volts.

$$V_{ref} = 2.0\ \text{Vdc}$$
$$R1 = R2 \cong 1.0\ \text{k}\Omega$$
$$R_O = 5.0\ \text{k}\Omega$$

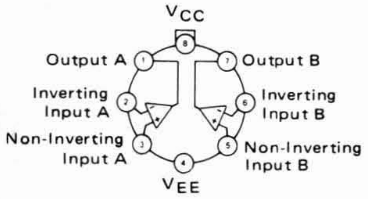
$$V_O = \frac{2\ \text{V}}{1\ \text{k}}(5\ \text{k})\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\ \text{V}\left[\frac{255}{256}\right] = 9.961\ \text{V}$$

## DUAL
## OPERATIONAL AMPLIFIERS

**SILICON MONOLITHIC**
**INTEGRATED CIRCUIT**

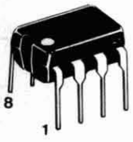


**G SUFFIX**
METAL PACKAGE
CASE 601-04

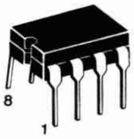


$V_{CC}$
Output A
Output B
Inverting Input A
Inverting Input B
Non-Inverting Input A
Non-Inverting Input B
$V_{EE}$

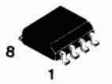
(Top View)



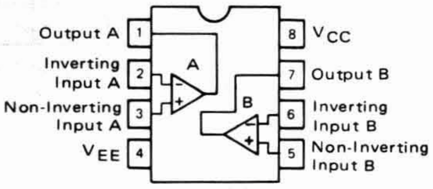
**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(MC1458S Only)



**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02



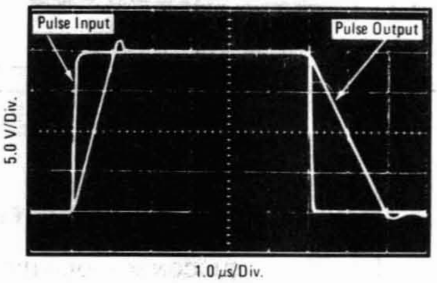
**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8
(MC1458S Only)



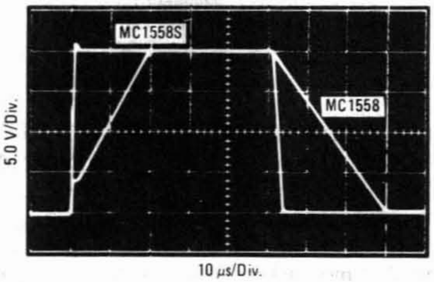
Output A 1
Inverting Input A 2
Non-Inverting Input A 3
$V_{EE}$ 4
8 $V_{CC}$
7 Output B
6 Inverting Input B
5 Non-Inverting Input B
A
B

(Top View)

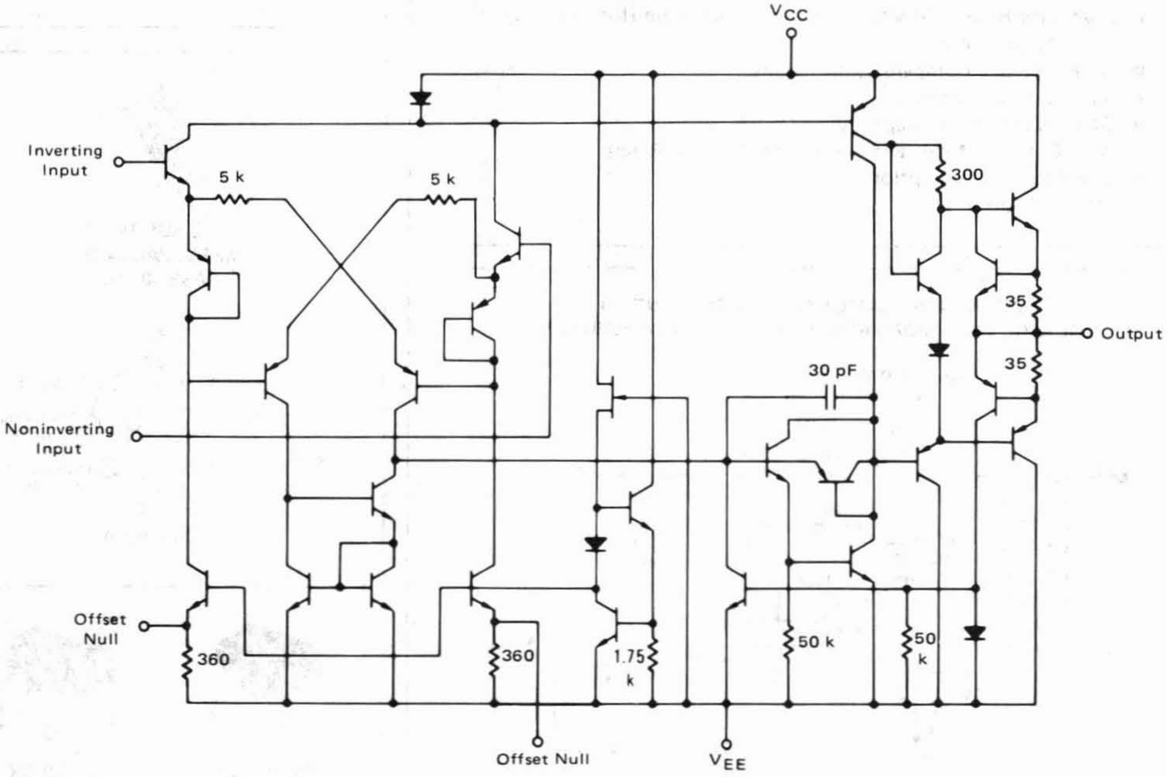
**MC1558S LARGE-SIGNAL TRANSIENT RESPONSE**
**(Inverting Mode)**



**STANDARD MC1558 versus MC1558S RESPONSE COMPARISON**
**(Inverting Mode)**



**½ REPRESENTATIVE CIRCUIT SCHEMATIC**


$V_{CC}$
Inverting Input
5 k
5 k
300
35
Output
35
30 pF
Noninverting Input
Offset Null
360
360
1.75 k
50 k
50 k
Offset Null
$V_{EE}$

## MAXIMUM RATINGS ($T_A$ = +25°C unless otherwise noted.)

| Rating | | Symbol | MC1558S | MC1458S | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | | $V_{CC}$<br>$V_{EE}$ | +22<br>-22 | +18<br>-18 | Vdc |
| Input Differential Voltage Range ① | | $V_{IDR}$ | ±30 | | Volts |
| Input Common-Mode Voltage Range ② | | $V_{ICR}$ | ±15 | | Volts |
| Output Short Circuit Duration | | $t_S$ | Continuous | | |
| Operating Ambient Temperature Range | | $T_A$ | -55 to +125 | 0 to +70 | °C |
| Storage Temperature Range | | $T_{stg}$ | -65 to +150 | -65 to +150 | °C |
| Junction Temperature | Ceramic and Metal Package<br>Plastic Package | $T_J$ | 175<br>150 | 175<br>150 | °C<br>°C |

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C unless otherwise noted.)

| Characteristic | Symbol | MC1558S Min | MC1558S Typ | MC1558S Max | MC1458S Min | MC1458S Typ | MC1458S Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Power Bandwidth (See Figure 3) | $BW_P$ | | | | | | | kHz |
| $A_v$ = 1, $R_L$ = 2.0 kΩ, THD = 5%, $V_O$ = 20 V(p-p) | | 150 | 200 | – | 150 | 200 | – | |
| Large-Signal Transient Response | | | | | | | | |
| Slew Rate (Figures 10 and 11) | SR | | | | | | | |
| V(−) to V(+) | | 10 | 20 | – | 10 | 20 | – | V/µs |
| V(+) to V(−) | | 10 | 12 | – | 10 | 12 | – | |
| Settling Time (Figures 10 and 11) (to within 0.1%) | $t_{setlg}$ | – | 3.0 | – | – | 3.0 | – | µs |
| Small-Signal Transient Response (Gain = 1, $E_{in}$ = 20 mV, see Figures 7 and 8) | | | | | | | | |
| Rise Time | $t_{TLH}$ | – | 0.25 | – | – | 0.25 | – | µs |
| Fall Time | $t_{THL}$ | – | 0.25 | – | – | 0.25 | – | µs |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | – | 0.25 | – | – | 0.25 | – | µs |
| Overshoot | OS | – | 20 | – | – | 20 | – | % |
| Short-Circuit Output Currents | $I_{OS}$ | ±10 | – | ±45 | ±10 | – | ±45 | mA |
| Open-Loop Voltage Gain ($R_L$ = 2.0 kΩ) (See Figure 4) | $A_{VOL}$ | | | | | | | – |
| $V_O$ = ±10 V | | 50,000 | 200,000 | – | 20,000 | 100,000 | – | |
| Output Impedance (f = 20 Hz) | $z_o$ | – | 75 | – | – | 75 | – | Ω |
| Input Impedance (f = 20 Hz) | $z_i$ | 0.3 | 1.0 | – | 0.3 | 1.0 | – | MΩ |
| Output Voltage Swing | $V_O$ | | | | | | | $V_{pk}$ |
| $R_L$ = 10 kΩ | | ±12 | ±14 | – | ±12 | ±14 | – | |
| $R_L$ = 2.0 kΩ | | ±10 | ±13 | – | ±10 | ±13 | – | |
| Input Common-Mode Voltage Swing | $V_{ICR}$ | ±12 | ±13 | – | ±12 | ±13 | – | $V_{pk}$ |
| Common-Mode Rejection Ratio (f = 20 Hz) | CMRR | 70 | 90 | – | 70 | 90 | – | dB |
| Input Bias Current (See Figure 2) | $I_{IB}$ | – | 200 | 500 | – | 200 | 500 | nA |
| Input Offset Current | $\|I_{IO}\|$ | – | 30 | 200 | – | 30 | 200 | nA |
| Input Offset Voltage ($R_S$ = ⩽10 kΩ) | $\|V_{IO}\|$ | – | 1.0 | 5.0 | – | 2.0 | 6.0 | mV |
| DC Power Consumption (See Figure 9) (Power Supply = ±15 V, $V_O$ = 0) | $P_C$ | – | 70 | 150 | – | 70 | 170 | mW |
| Positive Voltage Supply Sensitivity ($V_{EE}$ constant) | PSS+ | – | 2.0 | 150 | – | 2.0 | 150 | µV/V |
| Negative Voltage Supply Sensitivity ($V_{CC}$ constant) | PSS− | – | 10 | 150 | – | 10 | 150 | µV/V |

**Plastic package offered in limited temperature range device only.

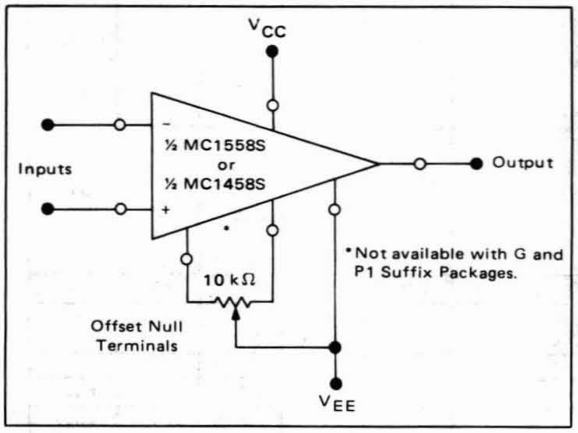
**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = −55 to +125°C for MC1558S and $T_A$ = 0 to 70°C for MC1458S, unless otherwise noted.)

| Characteristic | Symbol | MC1558S Min | MC1558S Typ | MC1558S Max | MC1458S Min | MC1458S Typ | MC1458S Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Open Loop Voltage Gain<br>$V_O$ = ±10 V | $A_{VOL}$ | 25,000 | – | – | 15,000 | – | – | V/V |
| Output Voltage Swing | $V_O$ | | | | | | | $V_{pk}$ |
| $R_L$ = 10 kΩ | | ±12 | – | – | ±12 | – | – | |
| $R_L$ = 2 kΩ | | ±10 | – | – | ±10 | – | – | |
| Input Common-Mode Voltage Range | $V_{ICR}$ | ±12 | – | – | – | – | – | $V_{pk}$ |
| Common-Mode Rejection Ratio (f = 20 Hz) | CMRR | 70 | – | – | – | – | – | dB |
| Input Bias Current | $I_{IB}$ | | | | | | | nA |
| $T_A$ = 125°C | | – | 200 | 500 | – | – | – | |
| $T_A$ = −55°C | | – | 500 | 1500 | – | – | – | |
| $T_A$ = 0 to 70°C | | – | – | – | – | – | 800 | |
| Input Offset Current | $I_{IO}$ | | | | | | | nA |
| $T_A$ = 125°C | | – | 30 | 200 | – | – | – | |
| $T_A$ = −55°C | | – | – | 500 | – | – | – | |
| $T_A$ = 0 to 70°C | | – | – | – | – | – | 300 | |
| Input Offset Voltage<br>$R_S$ ⩽ 10 kΩ | $V_{IO}$ | – | – | 6.0 | – | – | 7.5 | mV |
| DC Power Consumption<br>$V_O$ = 0 V | $P_C$ | – | – | 200 | – | – | – | mW |
| Positive Power Supply Sensitivity<br>$V_{EE}$ = −15 V | $P_{SS+}$ | – | – | 150 | – | – | – | µV/V |
| Negative Power Supply Sensitivity<br>$V_{CC}$ = 15 V | $P_{SS-}$ | – | – | 150 | – | – | – | µV/V |

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C unless otherwise noted.)

FIGURE 1 – OFFSET ADJUST CIRCUIT



V<sub>CC</sub>
Inputs
–
+
½ MC1558S
or
½ MC1458S
Output
10 kΩ
Offset Null
Terminals
V<sub>EE</sub>

*Not available with G and P1 Suffix Packages.

FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

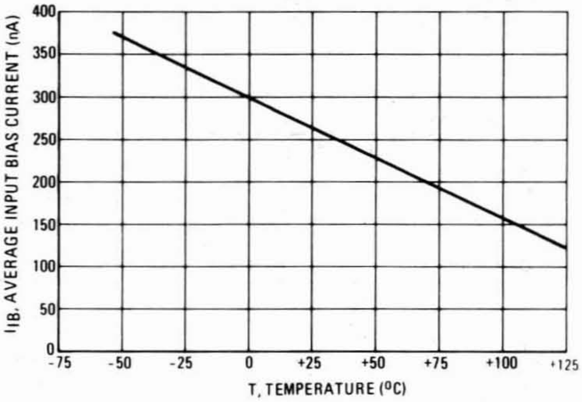


FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

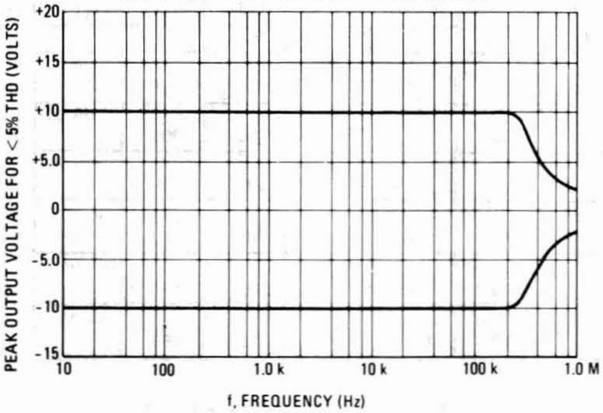


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

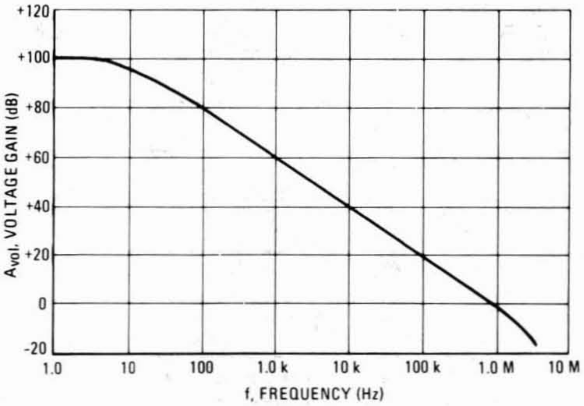
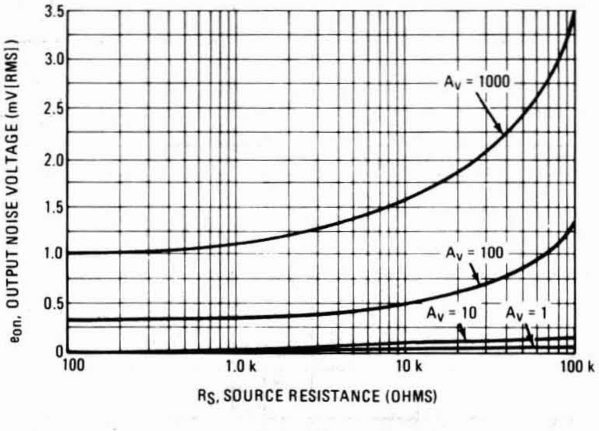


FIGURE 5 – OUTPUT NOISE versus SOURCE RESISTANCE



## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C unless otherwise noted.)

**FIGURE 6 – SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS**

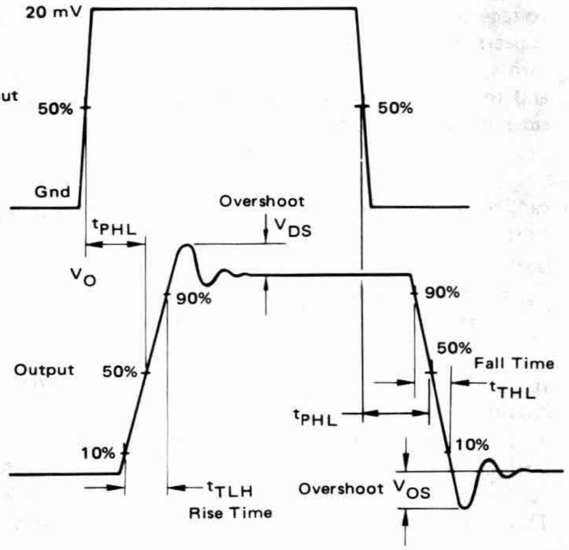

20 mV
Input
50%
50%
Gnd
Overshoot
$V_{DS}$
$t_{PHL}$
$V_O$
90%
90%
50%
Fall Time
Output
50%
$t_{THL}$
$t_{PHL}$
10%
10%
$t_{TLH}$
Rise Time
Overshoot $V_{OS}$

**FIGURE 7 – SMALL-SIGNAL TRANSIENT RESPONSE**

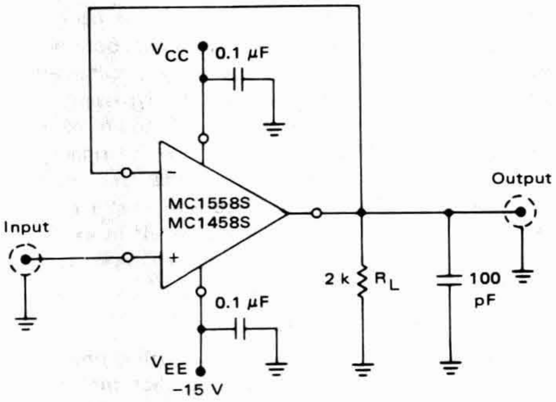

$V_{CC}$
0.1 µF
MC1558S
MC1458S
Input
Output
2 k
$R_L$
100 pF
0.1 µF
$V_{EE}$
−15 V

**FIGURE 8 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGES**

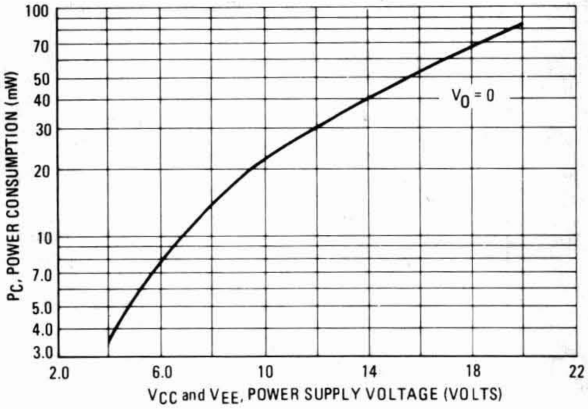


**FIGURE 9 – LARGE-SIGNAL TRANSIENT WAVEFORMS**

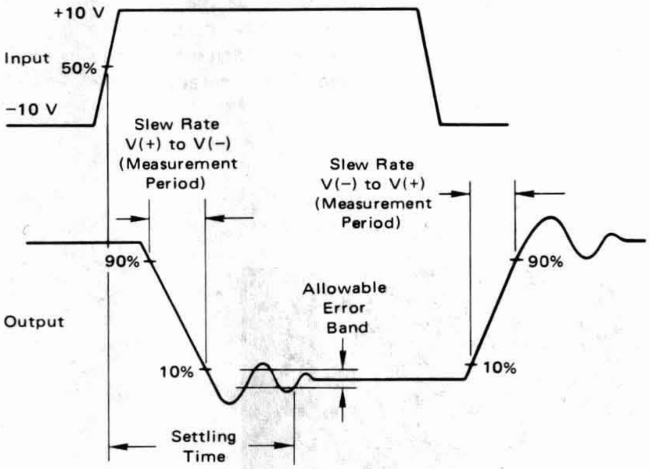
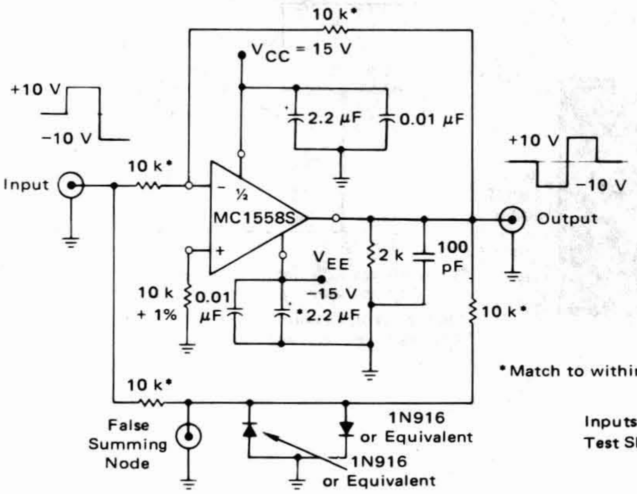

+10 V
Input
50%
−10 V
Slew Rate
V(+) to V(−)
(Measurement Period)
Slew Rate
V(−) to V(+)
(Measurement Period)
90%
90%
Output
Allowable Error Band
10%
10%
Settling Time

**FIGURE 10 – SLEW RATE AND SETTLING TIME TEST CIRCUIT***


10 k*
$V_{CC}$ = 15 V
+10 V
−10 V
2.2 µF
0.01 µF
10 k*
Input
½
MC1558S
+10 V
−10 V
Output
$V_{EE}$
2 k
100 pF
10 k
+ 1%
0.01 µF
−15 V
2.2 µF
10 k*
10 k*
False Summing Node
1N916 or Equivalent
1N916 or Equivalent

*Match to within 0.01%.

Inputs of Amplifier Not Under Test Should Be Grounded.

## SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

## SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

$t_{setlg}$ = observed settling time

x = amplifier settling time (to be determined)

y = false summing junction settling time

z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1558S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L-8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

**FIGURE 11 – WAVEFORM AT FALSE SUMMING NODE**
**(Inverting Mode)**

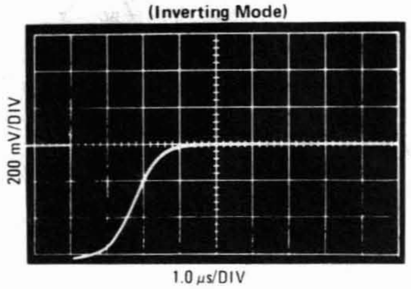
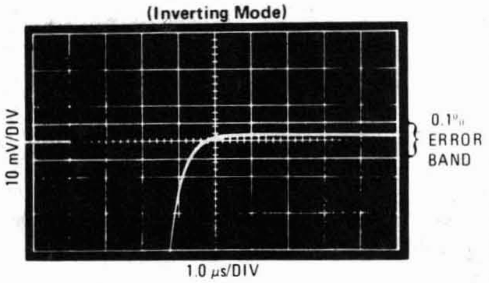
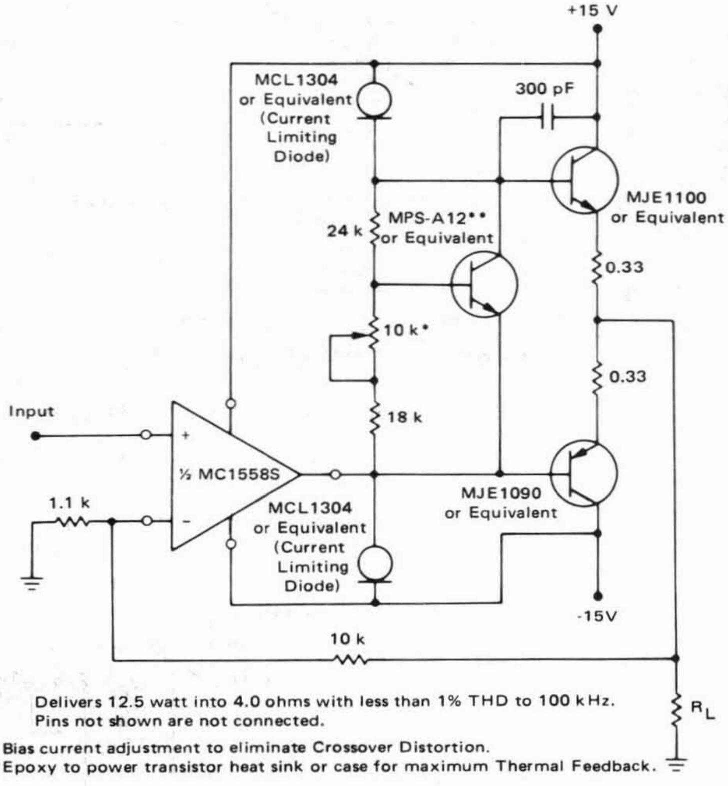


**FIGURE 12 – EXPANDED WAVEFORM AT FALSE SUMMING NODE**
**(Inverting Mode)**



### TYPICAL APPLICATION

**FIGURE 13 – 12.5-WATT WIDEBAND POWER AMPLIFIER**



Delivers 12.5 watt into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.

*Bias current adjustment to eliminate Crossover Distortion.

**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.

**MOTOROLA**

# MC1590G

## WIDEBAND AMPLIFIER WITH AGC

SILICON MONOLITHIC INTEGRATED CIRCUIT

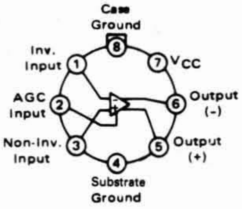
## RF/IF/AUDIO AMPLIFIER

. . . an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, −55 to +125°C. See Motorola Application Note AN513 for design details.

- High Power Gain — 50 dB Typ at 10 MHz
  45 dB Typ at 60 MHz
  35 dB Typ at 100 MHz
- Wide-Range AGC — 60 dB min, dc to 60 MHz
- Low Reverse Transfer Admittance — <10 μmhos Typ at 60 MHz
- 6.0 to 15-Volt Operation, Single-Polarity Power Supply

### PIN CONNECTIONS

G SUFFIX
METAL PACKAGE
CASE 601
TO-99



### MAXIMUM RATINGS ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol* | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +18 | Vdc |
| Output Supply | $V_O$ | +18 | Vdc |
| AGC Supply | $V_{2(AGC)}$ | $V_{CC}$ | Vdc |
| Differential Input Voltage | $V_I$ | 5.0 | Vdc |
| Operating Temperature Range | $T_A$ | −55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature | $T_J$ | +175 | °C |

### ADMITTANCE PARAMETERS ($V_{CC}$ = +12 Vdc, $T_A$ = +25°C)

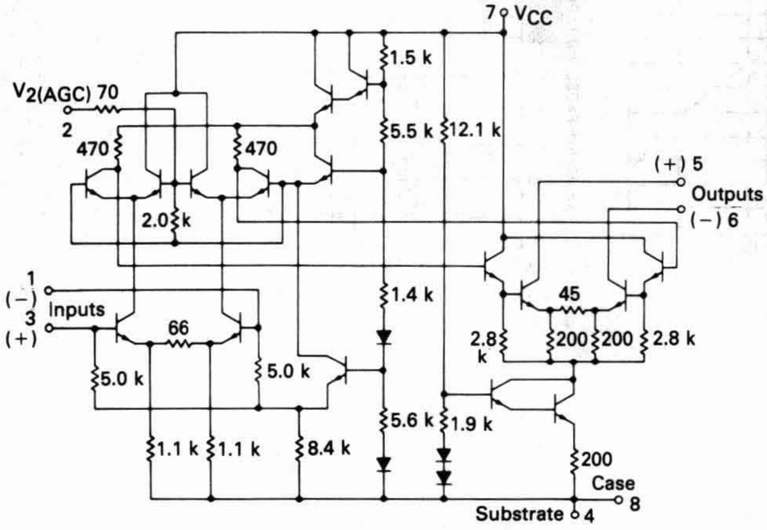
| Parameter | Symbol | f = MHz Typ | | Unit |
|---|---|---|---|---|
| | | 30 | 60 | |
| Single-Ended Input Admittance | $g_{11}$<br>$b_{11}$ | 0.4<br>1.2 | 0.6<br>−3.0 | mmhos |
| Single-Ended Output Admittance | $g_{22}$<br>$b_{22}$ | 0.05<br>0.50 | 0.1<br>1.0 | mmho |
| Forward Transfer Admittance (Pin 1 to Pin 5) | $Y_{21}$<br>$\theta_{21}$<br>(Polar) | 175<br>−30 | 150<br>−105 | mmhos<br>degrees |
| Reverse Transfer Admittance* | $g_{12}$<br>$b_{12}$ | −0<br>-5.0 | −0<br>−10 | μmhos |

*The value of Reverse Transfer Admittance includes the feedback admittance of the test circuit used in the measurement. The total feedback capacitance (including test circuit) is 0.025 pF and is a more practical value for design calculations than the internal feedback of the device alone. (See Figure 10.)

### SCATTERING PARAMETERS ($V_{CC}$ = +12 Vdc, $T_A$ = +25°C, $Z_o$ = 50 Ω)

| Parameter | Symbol | f = MHz Typ | | Unit |
|---|---|---|---|---|
| | | 30 | 60 | |
| Input Reflection Coefficient | $S_{11}$<br>$\theta_{11}$ | 0.95<br>-7.3 | 0.93<br>−16 | –<br>degrees |
| Output Reflection Coefficient | $S_{22}$<br>$\theta_{22}$ | 0.99<br>−3.0 | 0.98<br>−5.5 | –<br>degrees |
| Forward Transmission Coefficient | $S_{21}$<br>$\theta_{21}$ | 16.8<br>128 | 14.7<br>64.3 | –<br>degrees |
| Reverse Transmission Coefficient | $S_{12}$<br>$\theta_{12}$ | 0.00048<br>84.9 | 0.00092<br>79.2 | –<br>degrees |

### REPRESENTATIVE CIRCUIT SCHEMATIC



Pins 4 and 8 should both be connected to circuit ground.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 12 Vdc, f = 60 MHz, BW = 1.0 MHz, $T_A$ = −55°C to +125°C unless otherwise noted)

| Characteristic | Fig. | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| AGC Range | 24 | $M_{AGC}$ | | | | dB |
| ($V_{2(AGC)}$ = 5.0 V to 7.0 V) | | | 58 | — | — | |
| ($V_{2(AGC)}$ = 5.0 V to 7.0 V, $T_A$ = 25°C) | | | 60 | 68 | — | |
| Single-Ended Power Gain | 24 | $G_p$ | 37 | — | — | dB |
| ($T_A$ = 25°C) | | | 40 | 45 | — | |
| Noise Figure ($R_s$ optimized for best NF) ($T_A$ = 25°C) | 24 | NF | — | 6.0 | 7.0 | dB |
| Output Stage Current (Sum of Pins 5 and 6) | 32 | $I_O$ | 3.5 | — | 8.0 | mA |
| ($T_A$ = 25°C) | | | 4.0 | 5.6 | 7.5 | |
| Output Current Matching (Magnitude of Difference of Output Currents) ($I_5 - I_6$) ($T_A$ = 25°C) | 32 | $\Delta I_O$ | — | 0.7 | — | mA |
| Power Supply Current | 32 | $I_{CC}$ | | | | mA |
| ($V_O$ = 0 V) | | | — | — | 20 | |
| ($V_O$ = 0 V, $T_A$ = 25°C) | | | — | 14 | 17 | |
| Power Consumption (12 × $I_{CC}$) | — | $P_C$ | | | | mW |
| ($V_I$ = 0 V) | | | — | — | 240 | |
| ($V_I$ = 0 V, $T_A$ = 25°C) | | | — | 168 | 204 | |

FIGURE 1 – UNNEUTRALIZED POWER GAIN versus FREQUENCY
(Tuned Amplifier, See Figure 24)

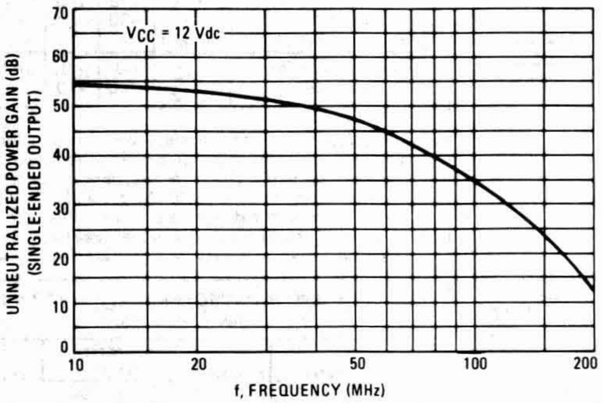
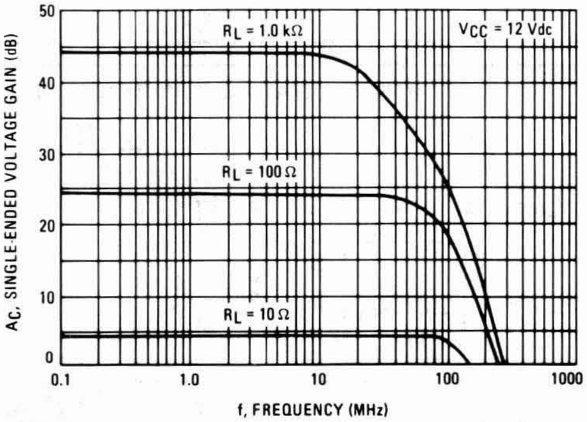


FIGURE 2 – VOLTAGE GAIN versus FREQUENCY
(Video Amplifier, See Figure 26)



## TYPICAL CHARACTERISTICS

($V_{2\,(AGC)} = 0$, $V_{CC} = 12$ Vdc, $T_A = +25^{\circ}C$ unless otherwise noted)

**FIGURE 3 – DYNAMIC RANGE: OUTPUT VOLTAGE versus INPUT VOLTAGE (Video Amplifier, See Figure 26)**

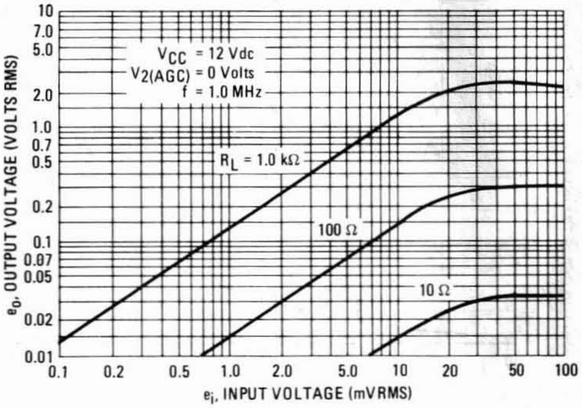


**FIGURE 4 – VOLTAGE GAIN versus FREQUENCY (Video Amplifier, See Figure 26)**

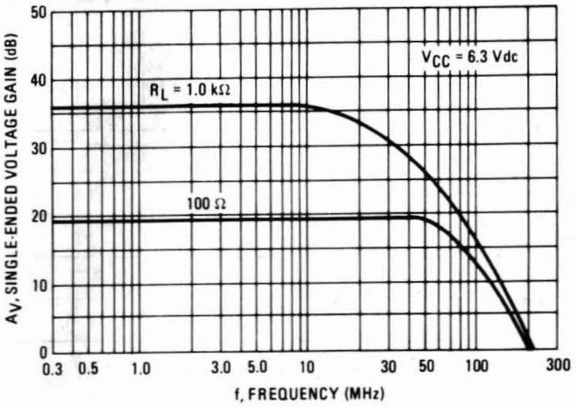


**FIGURE 5 – VOLTAGE GAIN AND SUPPLY CURRENT versus SUPPLY VOLTAGE (Video Amplifier, See Figure 26)**

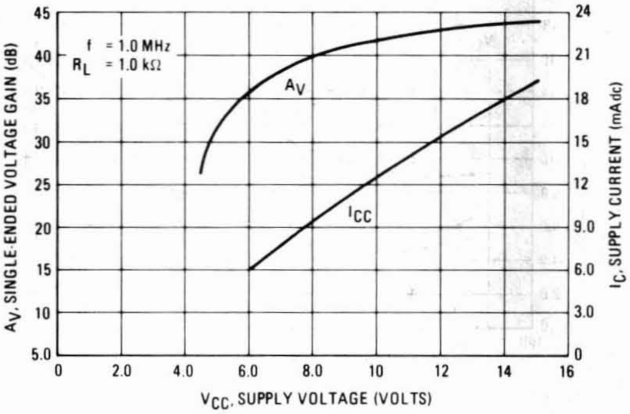


**FIGURE 6 – TYPICAL GAIN REDUCTION versus AGC VOLTAGE**

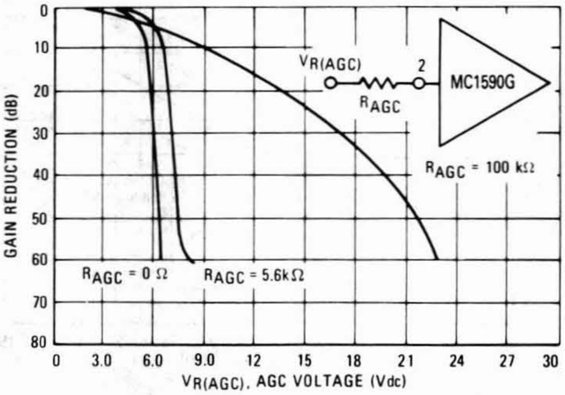


**FIGURE 7 – TYPICAL GAIN REDUCTION versus AGC CURRENT**

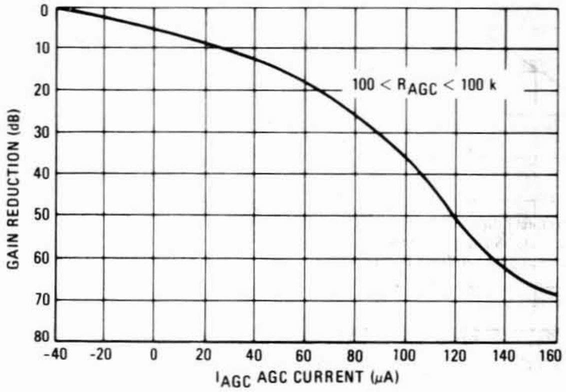
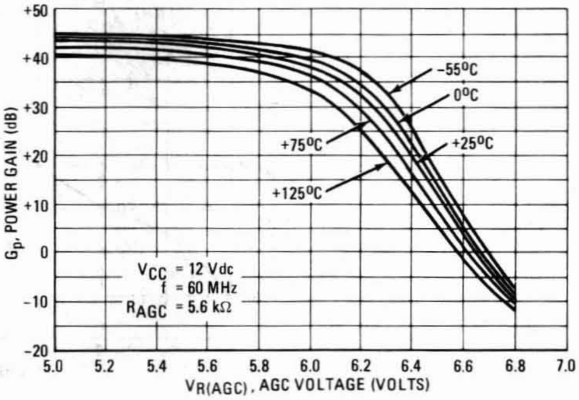


**FIGURE 8 – FIXED TUNED POWER GAIN REDUCTION versus TEMPERATURE (See Test Circuit, Figure 24)**



## TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – POWER GAIN versus SUPPLY VOLTAGE (See Test Circuit, Figure 24)

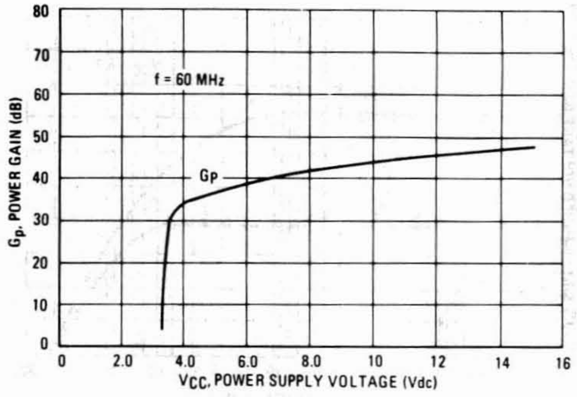


FIGURE 10 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY (See Parameter Table, Page 1)

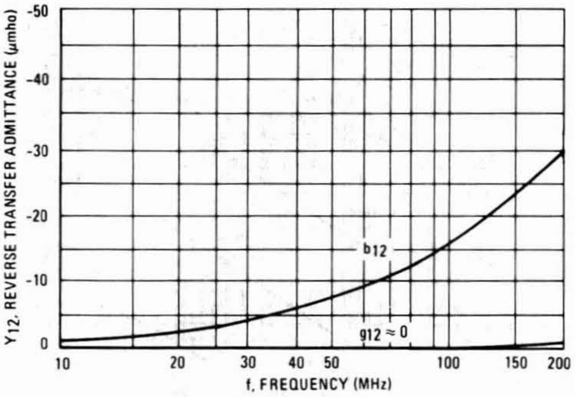


FIGURE 11 – NOISE FIGURE versus FREQUENCY

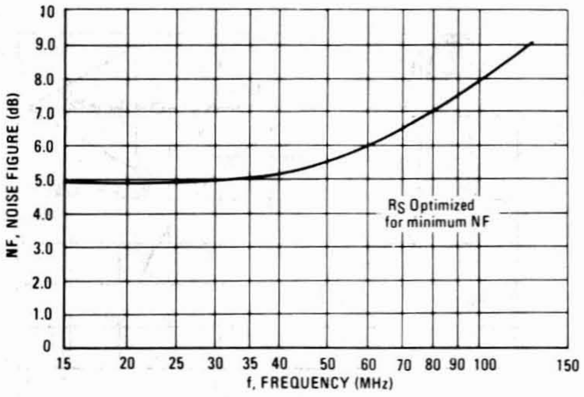


FIGURE 12 – NOISE FIGURE versus SOURCE RESISTANCE

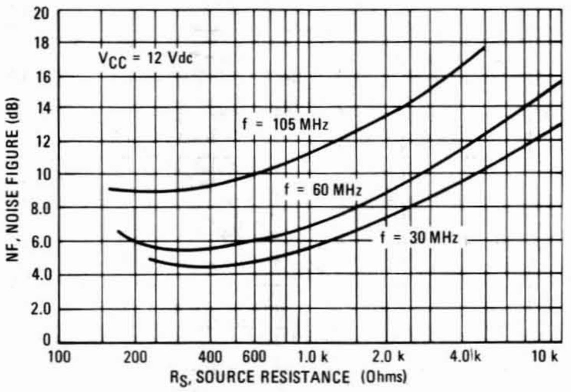
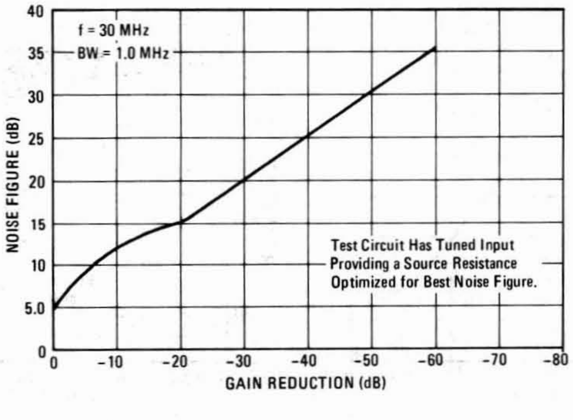


FIGURE 13 – NOISE FIGURE versus AGC GAIN REDUCTION



## TYPICAL CHARACTERISTICS (continued)

FIGURE 14 – SINGLE-ENDED OUTPUT ADMITTANCE

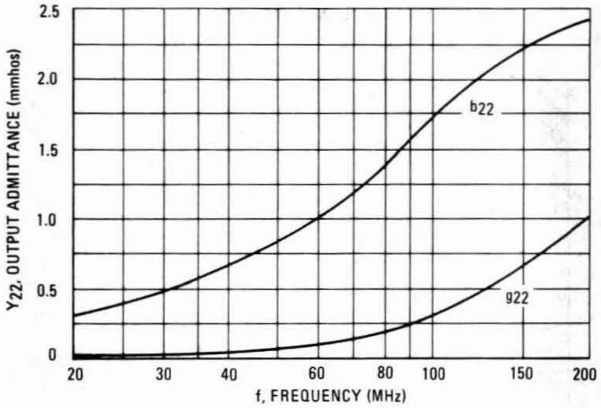


FIGURE 15 – SINGLE-ENDED INPUT ADMITTANCE

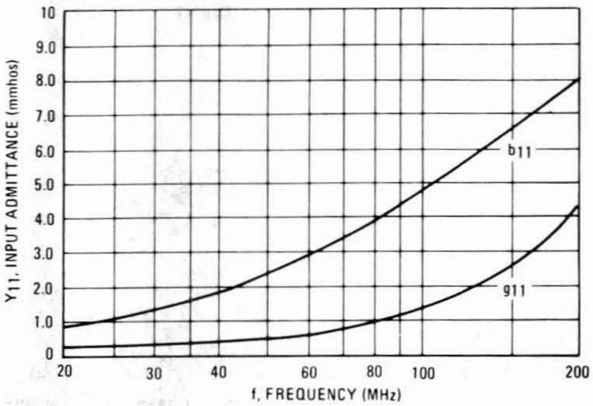


FIGURE 16 – HARMONIC DISTORTION versus AGC GAIN REDUCTION FOR AM CARRIER (For Test Circuit, See Figure 17)

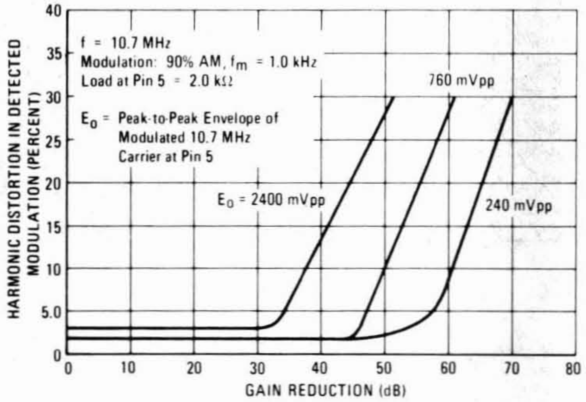
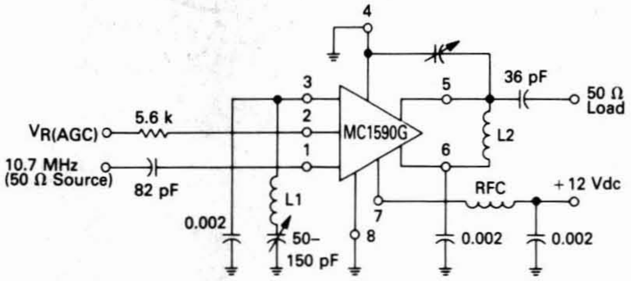


FIGURE 17 — 10.7 MHz AMPLIFIER
Gain ≈ 55 dB, BW ≈ 100 kHz


4
3
5
36 pF
50 Ω Load
2
VR(AGC)
5.6 k
MC1590G
L2
1
6
10.7 MHz (50 Ω Source)
82 pF
RFC
+12 Vdc
7
L1
0.002
50–150 pF
8
0.002
0.002

L1 = 24 Turns, No. 22 AWG Wire on a T12-44 Micro Metal Toroid Core (– 124 pF)

L2 = 20 Turns, No. 22 AWG Wire on a T12-44 Micro Metal Toroid Core (– 100 pF)

FIGURE 18 – $Y_{21}$, FORWARD TRANSFER ADMITTANCE RECTANGULAR FORM

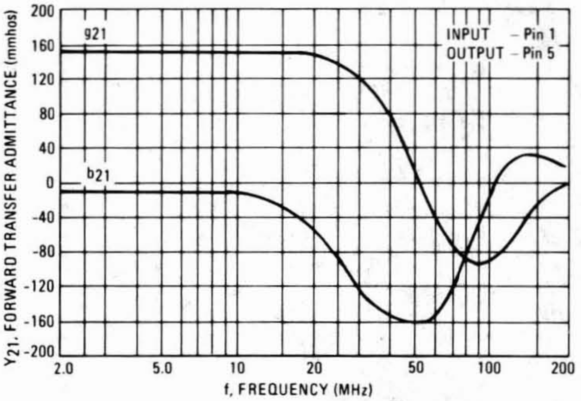
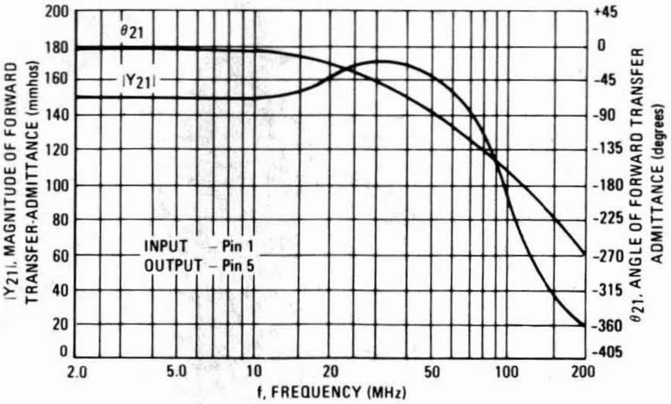


FIGURE 19 — $Y_{21}$, FORWARD TRANSFER ADMITTANCE POLAR FORM



## TYPICAL CHARACTERISTICS (continued)

**FIGURE 20 – $S_{11}$ AND $S_{22}$, INPUT AND OUTPUT REFLECTION COEFFICIENT**

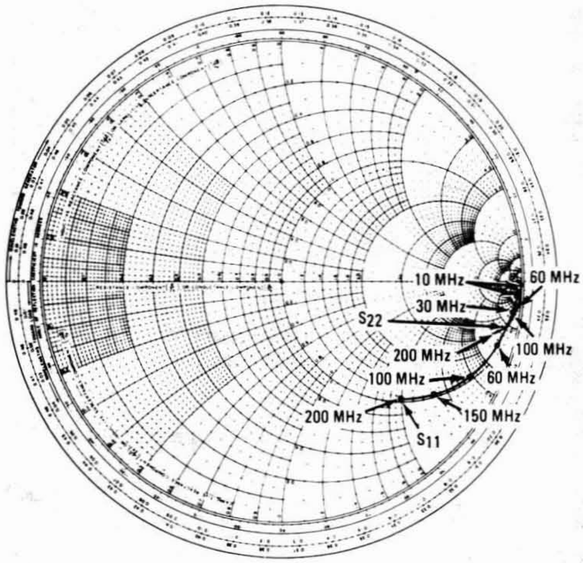


**FIGURE 21 – $S_{11}$ AND $S_{22}$, INPUT AND OUTPUT REFLECTION COEFFICIENT**

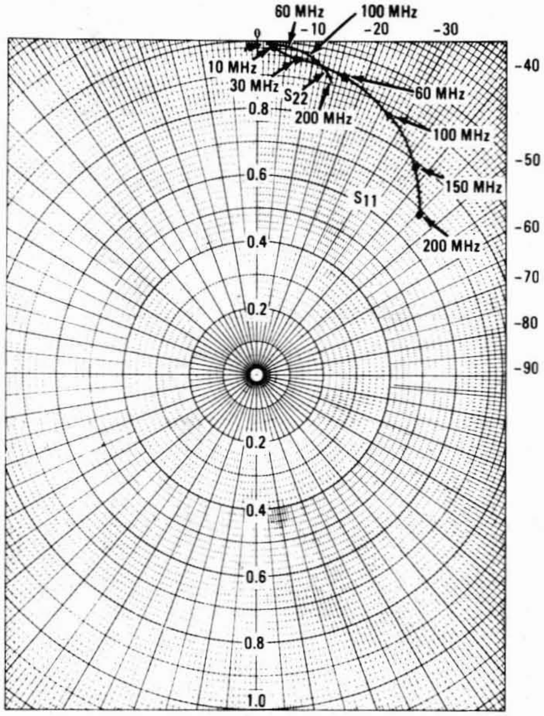


**FIGURE 22 – $S_{21}$, FORWARD TRANSMISSION COEFFICIENT (GAIN)**

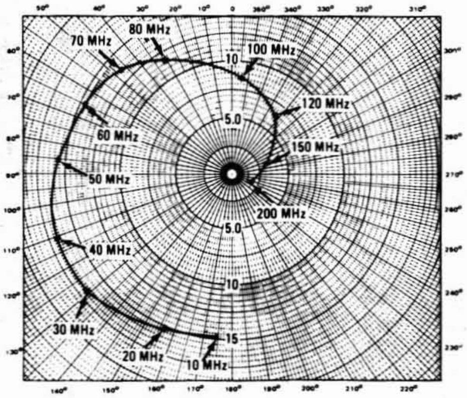
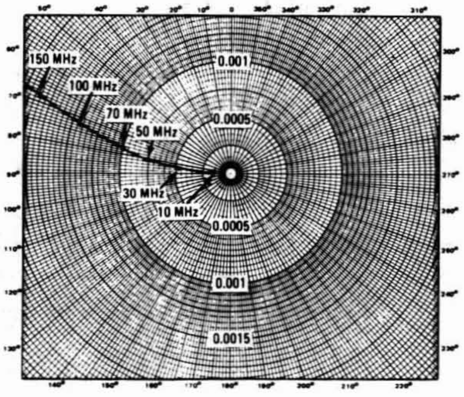
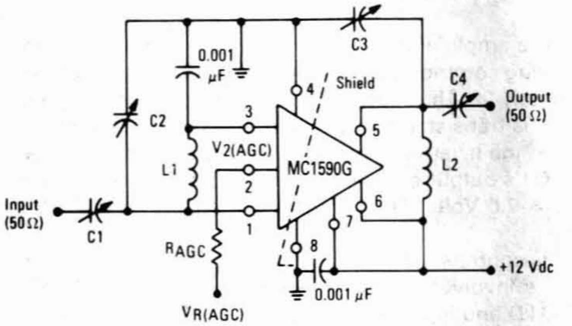


**FIGURE 23 – $S_{12}$, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)**



## TYPICAL APPLICATIONS

### FIGURE 24 — 60 MHz POWER GAIN TEST CIRCUIT


0.001 μF
C3
C4
4
Shield
Output (50 Ω)
C2
3
5
V2(AGC)
L1
MC1590G
L2
2
6
Input (50Ω)
C1
1
7
RAGC
8
+12 Vdc
0.001 μF
VR(AGC)

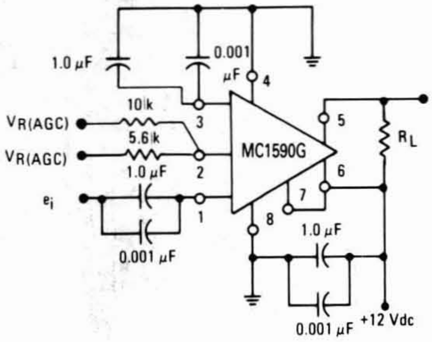
L1 = 7 Turns, #20 AWG Wire, 5/16" Dia., 5/8" Long
L2 = 6 Turns, #14 AWG Wire, 9/16" Dia., 3/4" Long

C1,C2,C3 = (1-30) pF
C4 = (1-10) pF

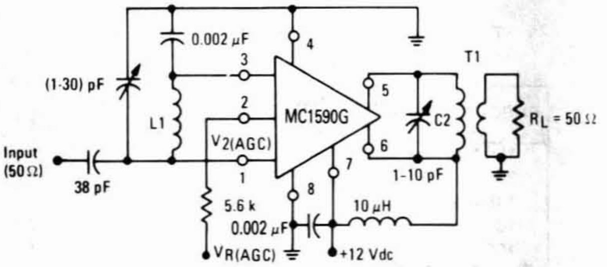
### FIGURE 25 — PROCEDURE FOR SETUP USING FIGURE 24

| Test | $e_{in}$ | $V_{2(AGC)}$ | $R_{AGC}$(kΩ) |
|---|---|---|---|
| $M_{AGC}$ | 2.23 mV (−40dBm) | 5-7 V | 0 |
| Gp | 1.0 mV (−47dBm) | ⩽5.0 V | 5.6 |
| NF | 1.0 mV (−47dBm) | ⩽5.0 V | 5.6 |

### FIGURE 26 – VIDEO AMPLIFIER

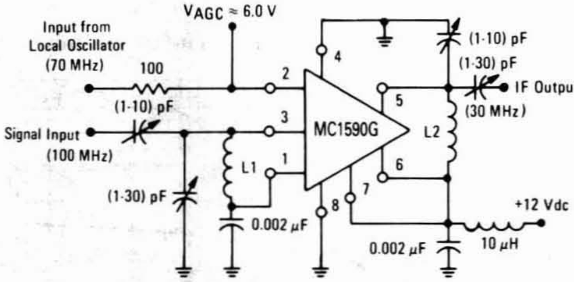

1.0 μF
0.001 μF
4
10 k
VR(AGC)
3
e0
5.6 k
5
RL
VR(AGC)
MC1590G
1.0 μF
2
6
ei
7
1
8
1.0 μF
0.001 μF
0.001 μF
+12 Vdc

### FIGURE 27 — 30 MHz AMPLIFIER (Power Gain = 50 dB, BW ≈ 1.0 MHz)


0.002 μF
4
3
T1
(1-30) pF
5
2
MC1590G
C2
RL = 50 Ω
L1
V2(AGC)
6
Input (50Ω)
7
38 pF
1
1-10 pF
8
5.6 k
10 μH
0.002 μF
VR(AGC)
+12 Vdc

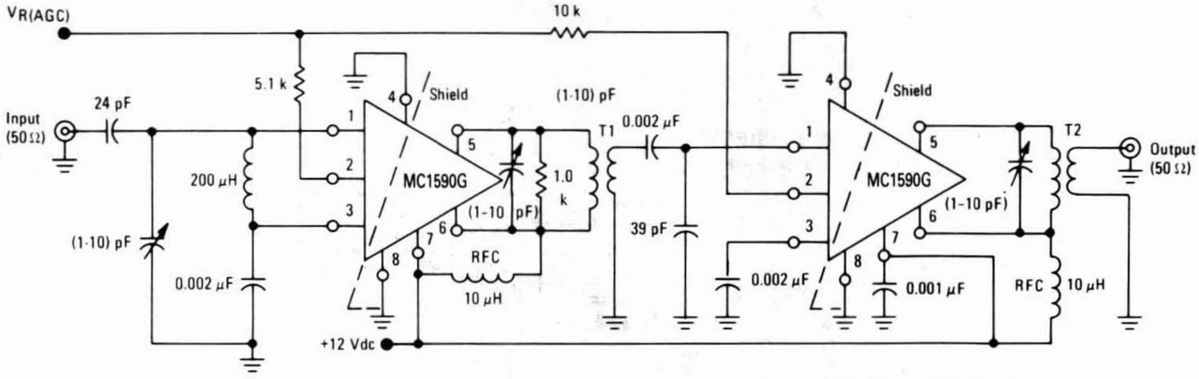
L1 = 12 Turns #22 AWG Wire on a Toroid Core, (T37-6 Micro Metal or Equiv)
T1: Primary = 17 Turns #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)
Secondary = 2 Turns #20 AWG Wire

### FIGURE 28 – 100 MHz MIXER


VAGC ≈ 6.0 V
Input from Local Oscillator (70 MHz)
100
4
(1-10) pF
(1-30) pF
2
IF Output (30 MHz)
(1-10) pF
5
3
Signal Input (100 MHz)
MC1590G
L2
L1
1
6
(1-30) pF
7
8
+12 Vdc
0.002 μF
0.002 μF
10 μH

L1 = 5 Turns, #16 AWG Wire, 1/4" ID, 5/8" Long
L2 = 16 Turns, #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)

### FIGURE 29 – TWO-STAGE 60 MHz IF AMPLIFIER (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)

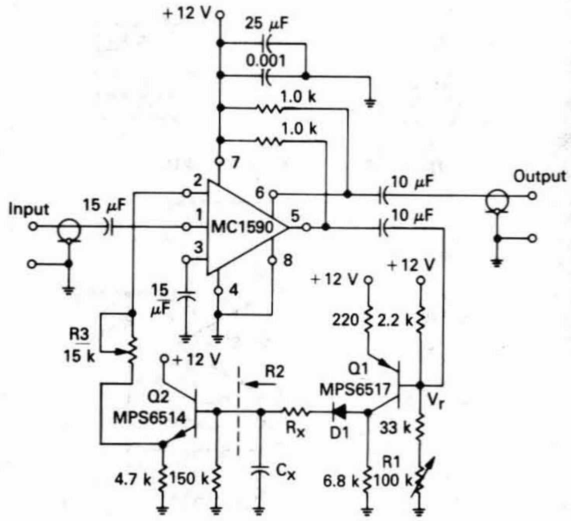

VR(AGC)
10 k
5.1 k
4
Shield
(1-10) pF
4
Shield
24 pF
0.002 μF
Input (50Ω)
1
T1
1
T2
5
5
Output (50 Ω)
2
MC1590G
1.0 k
2
MC1590G
200 μH
3
(1-10 pF)
39 pF
3
(1-10 pF)
6
6
(1-10) pF
7
7
RFC
8
8
0.002 μF
10 μH
0.002 μF
0.001 μF
RFC
10 μH
+12 Vdc

T1: Primary Winding = 15 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 4 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

T2: Primary Winding = 10 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 2 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

## TYPICAL APPLICATIONS (continued)

FIGURE 30 – SPEECH COMPRESSOR


+12 V
25 µF
0.001
1.0 k
1.0 k
7
2
6
Output
10 µF
Input
15 µF
1
MC1590
5
10 µF
3
8
+12 V
+12 V
15 µF
4
220
2.2 k
R3
15 k
+12 V
R2
Q1
MPS6517
Q2
MPS6514
$V_r$
$R_X$
D1
33 k
R1
$C_X$
4.7 k
150 k
6.8 k
100 k

## DESCRIPTION OF SPEECH COMPRESSOR

The amplifier drives the base of a PNP MPS6517 operating common-emitter with a voltage gain of approximately 20. The control R1 varies the quiescent Q point of this transistor so that varying amounts of signal exceed the level $V_r$. Diode D1 rectifies the positive peaks of Q1's output only when these peaks are greater than $V_r \approx 7.0$ Volts. The resulting output is filtered by $C_X$, $R_X$.

$R_X$ controls the charging time constant or attack time. $C_X$ is involved in both charge and discharge. R2 (the 150 kΩ and input resistance of the emitter-follower Q2) controls the decay time. Making the decay long and attack short is accomplished by making $R_X$ small and R2 large. (A Darlington emitter-follower may be needed if extremely slow decay times are required.)

The emitter-follower Q2 drives the AGC Pin 2 of the MC1590G and reduces the gain. R3 controls the slope of signal compression. The following graph (Figure 31) details performance with R3 set to 15 kΩ.

FIGURE 31 – OUTPUT VOLTAGE versus INPUT VOLTAGE

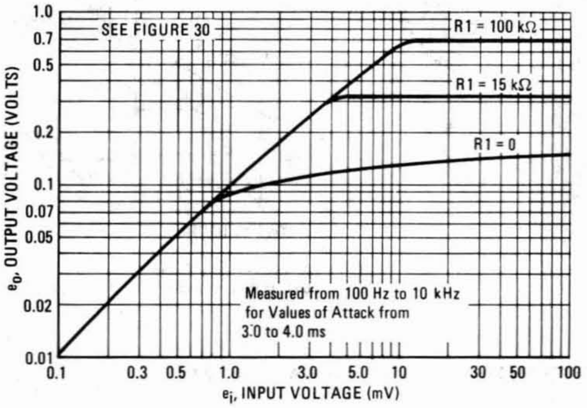
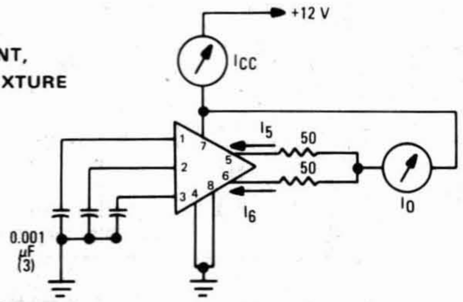


TABLE 1 — DISTORTION versus FREQUENCY

| FREQUENCY | DISTORTION | | DISTORTION | |
|---|---|---|---|---|
| | 10 mV $e_i$ | 100 mV $e_i$ | 10 mV $e_i$ | 100 mV $e_i$ |
| 100 Hz | 3.5% | 12% | 15% | 27% |
| 300 Hz | 2% | 10% | 6% | 20% |
| 1.0 kHz | 1.5% | 8% | 3% | 9% |
| 10 kHz | 1.5% | 8% | 1% | 3% |
| 100 kHz | 1.5% | 8% | 1% | 3% |
| | Notes 1 and 2 | | Notes 3 and 4 | |

Note:
(1) Decay = 300 ms
Attack = 20 ms
(2) $C_X$ = 7.5 µF
$R_X$ = 0 (Short)
(3) Decay = 20 ms
Attack = 3 ms
(4) $C_X$ = 0.68 µF
$R_X$ = 1.5 kΩ

FIGURE 32 – OUTPUT CURRENT, CURRENT MATCH AND $I_{CC}$ FIXTURE


+12 V
$I_{CC}$
$I_5$
50
50
$I_6$
$I_0$
1
7
2
5
6
3
4
8
0.001 µF (3)

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1709CG | 0°C to +70°C | Metal Can |
| MC1709CU | 0°C to +70°C | Ceramic DIP |
| MC1709CP1 | 0°C to +70°C | Plastic DIP |
| MC1709G,AG | −55°C to +125°C | Metal Can |
| MC1709AU | −55°C to +125°C | Ceramic DIP |

# MC1709
# MC1709A
# MC1709C

## MONOLITHIC OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics
  $A_{vol}$ = 45,000 typical
- Low Temperature Drift – ±3.0 $\mu$V/°C typical (MC1709)
- Large Output Voltage Swing – ±14 V typical @ ±15 V Supply
- Low Output Impedance – $z_o$ = 150 ohms typical

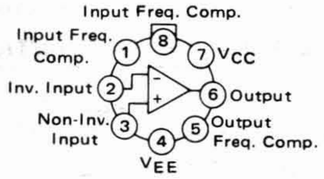
## OPERATIONAL AMPLIFIER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>−18 | Vdc |
| Input Differential Voltage Range | $V_{IDR}$ | ±5.0 | Volts |
| Input Common-Mode Range | $V_{ICR}$ | ±10 | Volts |
| Output Load Current | $I_L$ | 10 | mA |
| Output Short-Circuit Duration | $t_S$ | 5.0 | s |
| Power Dissipation (Package Limitation) | $P_D$ | | |
| Metal Can | | 680 | mW |
| Derate above $T_A$ = +25°C | | 4.6 | mW/°C |
| Plastic Dual In-Line Packages (MC1709C only) | | 625 | mW |
| Derate above $T_A$ = +25°C | | 5.0 | mW/°C |
| Ceramic Dual In-Line Package | | 750 | mW/°C |
| Derate above $T_A$ = +25°C | | 6.0 | mW/°C |
| Operating Ambient Temperature Range MC1709A, MC1709 | $T_A$ | −55 to +125 | °C |
| MC1709C | | 0 to +70 | |
| Storage Temperature Range | $T_{stg}$ | | °C |
| Metal and Ceramic Packages | | −65 to +150 | |
| Plastic Packages | | −55 to +125 | |

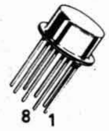
**PIN CONNECTIONS**



Input Freq. Comp.
Input Freq. Comp.
1
8
7
$V_{CC}$
Inv. Input
2
6
Output
Non-Inv. Input
3
4
5
Output Freq. Comp.
$V_{EE}$

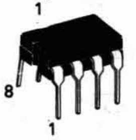
(Top View)

**G SUFFIX**
METAL PACKAGE
CASE 601-04

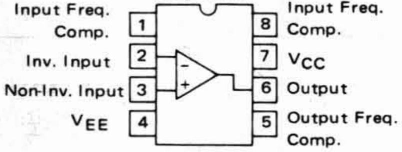


**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(MC1709C only)

**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02

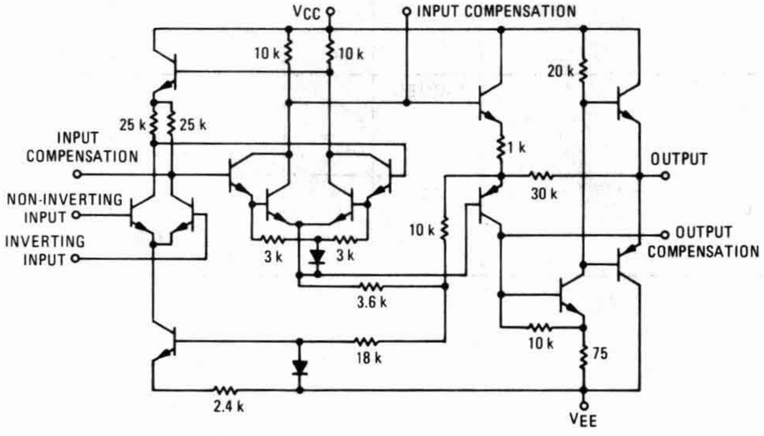


(Top View)



Input Freq. Comp.
1
Inv. Input
2
Non-Inv. Input
3
$V_{EE}$
4
8
Input Freq. Comp.
7
$V_{CC}$
6
Output
5
Output Freq. Comp.

**FIGURE 1 – EQUIVALENT CIRCUIT SCHEMATIC**



$V_{CC}$
INPUT COMPENSATION
10 k
10 k
20 k
25 k
25 k
INPUT COMPENSATION
1 k
OUTPUT
NON-INVERTING INPUT
30 k
INVERTING INPUT
10 k
OUTPUT COMPENSATION
3 k
3 k
3.6 k
10 k
75
18 k
2.4 k
$V_{EE}$

**ELECTRICAL CHARACTERISTICS** (unless otherwise noted, 9.0 V $\leqslant V_{CC} \leqslant$ 15 V, -9.0 V $\geqslant V_{EE} \geqslant$ -15 V, $T_A$ = 25°C)

| Characteristic | Symbol | MC1709A Min | MC1709A Typ | MC1709A Max | MC1709 Min | MC1709 Typ | MC1709 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage ($R_S \leqslant$ 10 kΩ) | $V_{IO}$ | – | 0.6 | 2.0 | – | 1.0 | 5.0 | mV |
| Input Offset Current | $I_{IO}$ | – | 10 | 50 | – | 50 | 200 | nA |
| Input Bias Current | $I_{IB}$ | – | 100 | 200 | – | 200 | 500 | nA |
| Input Resistance | $r_i$ | 350 | 700 | – | 150 | 400 | – | kΩ |
| Output Resistance | $r_o$ | – | 150 | – | – | 150 | – | Ω |
| Power Supply Currents ($V_{CC}$ = 15 V, $V_{EE}$ = -15 V) | $I_{CC}, I_{EE}$ | – | 2.5 | 3.6 | – | – | – | mA |
| Power Consumption ($V_{CC}$ = 15 V, $V_{EE}$ = -15 V) | $P_C$ | – | 75 | 108 | – | 80 | 165 | mW |
| Transient Response ($V_{CC}$ = 15 V, $V_{EE}$ = -15 V) See Figure 8 | | | | | | | | |
| Risetime | $t_{TLH}$ | – | – | 1.5 | – | 0.3 | 1.0 | µs |
| Overshoot | OS | – | – | 30 | – | 10 | 30 | % |

**ELECTRICAL CHARACTERISTICS** (unless otherwise noted, 9.0 V $\leqslant V_{CC} \leqslant$ 15 V, -9.0 V $\geqslant V_{EE} \geqslant$ -15 V, $T_A$ = -55°C to +125°C)

| Characteristic | Symbol | MC1709A Min | MC1709A Typ | MC1709A Max | MC1709 Min | MC1709 Typ | MC1709 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage ($R_S \leqslant$ 10 kΩ) | $V_{IO}$ | – | – | 3.0 | – | – | 6.0 | mV |
| Average Temperature Coefficient of Input Offset Voltage | $\Delta V_{IO}/\Delta T$ | | | | | | | µV/°C |
| ($R_S$ = 50 Ω, $T_A$ = 25°C to 125°C) | | – | 1.8 | 10 | – | – | – | |
| ($R_S$ = 50 Ω, $T_A$ = -55°C to 25°C) | | – | 1.8 | 10 | – | – | – | |
| ($R_S$ = 50 Ω, $T_A$ = -55°C to 125°C) | | – | – | – | – | 3.0 | – | |
| ($R_S$ = 10 kΩ, $T_A$ = 25°C to 125°C) | | – | 2.0 | 15 | – | – | – | |
| ($R_S$ = 10 kΩ, $T_A$ = -55°C to 25°C) | | – | 4.8 | 25 | – | – | – | |
| ($R_S$ = 10 kΩ, $T_A$ = -55°C to 125°C) | | – | – | – | – | 6.0 | – | |
| Input Offset Current | $I_{IO}$ | | | | | | | nA |
| ($T_A$ = -55°C) | | – | 40 | 250 | – | 100 | 500 | |
| ($T_A$ = 125°C) | | – | 3.5 | 50 | – | 20 | 200 | |
| Average Temperature Coefficient of Input Offset Current | $\Delta I_{IO}/\Delta T$ | | | | | | | nA/°C |
| ($T_A$ = -55°C to 25°C) | | – | 0.45 | 2.8 | – | – | – | |
| ($T_A$ = 25°C to 125°C) | | – | 0.08 | 0.5 | – | – | – | |
| Input Bias Current ($T_A$ = -55°C) | $I_{IB}$ | – | 300 | 600 | – | 500 | 1500 | nA |
| Input Resistance ($T_A$ = -55°C) | $r_i$ | 85 | 170 | – | 40 | 100 | – | kΩ |
| Input Common-Mode Voltage Range ($V_{CC}$ = 15 V, $V_{EE}$ = -15 V) | $V_{ICR}$ | ±8.0 | ±10 | – | ±8.0 | ±10 | – | V |
| Common Mode Rejection Ratio ($R_S \leqslant$ 10 kΩ) | CMRR | 80 | 110 | – | 70 | 90 | – | dB |
| Supply Voltage Rejection Ratio ($V_{CC}$ = 15 V, $V_{EE}$ = -15 V, $R_S \leqslant$ 10 kΩ) | PSRR | – | 40 | 100 | – | 25 | 150 | µV/V |
| Large Signal Voltage Gain ($V_{CC}$ = 15 V, $V_{EE}$ = -15 V, $R_L \geqslant$ 2.0 kΩ, $V_O$ = ±15 V) | $A_V$ | 25 | 45 | 70 | 25 | 45 | 70 | V/mV |
| Output Voltage Range ($V_{CC}$ = 15 V, $V_{EE}$ = -15 V) | $V_{OR}$ | | | | | | | V |
| ($R_L \geqslant$ 10 kΩ) | | ±12 | ±14 | – | ±12 | ±14 | – | |
| ($R_L \geqslant$ 2.0 kΩ) | | ±10 | ±13 | – | ±10 | ±13 | – | |
| Power Supply Currents ($V_{CC}$ = 15 V, $V_{EE}$ = -15 V) | $I_{CC}/I_{EE}$ | | | | | | | mA |
| ($T_A$ = -55°C) | | – | 2.7 | 4.5 | – | – | – | |
| ($T_A$ = 125°C) | | – | 2.1 | 3.0 | – | – | – | |
| Power Consumption ($V_{CC}$ = 15, $V_{EE}$ = -15 V) | $P_C$ | | | | | | | mW |
| ($T_A$ = -55°C) | | – | 81 | 135 | – | – | – | |
| ($T_A$ = 125°C) | | – | 63 | 90 | – | – | – | |

**ELECTRICAL CHARACTERISTICS** (unless otherwise ntoed, $V_{CC}$ = 15 V, $V_{EE}$ = -15 V, $T_A$ = 25°C)

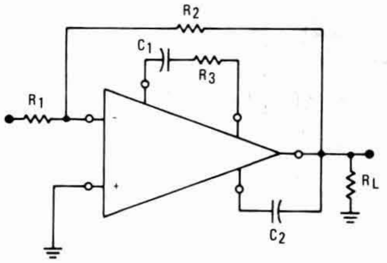
| Characteristic | Symbol | MC1709C Min | MC1709C Typ | MC1709C Max | Unit |
|---|---|---|---|---|---|
| Input Offset Voltage<br>($R_S \leqslant$ 10 kΩ, 9.0 V $\leqslant$ 15 V, -9.0 V $\geqslant V_{EE} \geqslant$ -15 V) | $V_{IO}$ | – | 2.0 | 7.5 | mV |
| Input Offset Current | $I_{IO}$ | – | 100 | 500 | nA |
| Input Bias Current | $I_{IB}$ | – | 300 | 1500 | nA |
| Input Resistance | $r_i$ | 50 | 250 | – | kΩ |
| Output Resistance | $r_o$ | – | 150 | – | Ω |
| Power Consumption | $P_C$ | – | 80 | 200 | mW |
| Large Signal Voltage Gain<br>($R_L \geqslant$ 2.0 kΩ, $V_O$ = ±10 V) | $A_V$ | 15 | 45 | – | V/mV |
| Output Voltage Range | $V_{OR}$ | | | | V |
| ($R_L \geqslant$10 kΩ) | | ±12 | ±14 | – | |
| ($R_L \geqslant$2.0 kΩ) | | ±10 | ±13 | – | |
| Input Common-Mode Voltage Range | $V_{ICR}$ | ±8.0 | ±10 | – | V |
| Common Mode Rejection Ratio<br>($R_S \leqslant$10 kΩ) | CMRR | 65 | 90 | – | dB |
| Supply Voltage Rejection Ratio<br>($R_S \leqslant$10 kΩ) | PSRR | – | 25 | 200 | μV/V |
| Transient Response<br>See Figure 8 | | | | | |
| Rise Time | $t_{TLH}$ | – | 0.3 | – | μs |
| Overshoot | OS | – | 10 | – | % |

**ELECTRICAL CHARACTERISTICS** (unless otherwise specified, $V_{CC}$ = 15 V, $V_{EE}$ = -15 V, $T_A$ = 0°C to 70°C)

| Parameter | Symbol | MC1709C Min | MC1709C Typ | MC1709C Max | Unit |
|---|---|---|---|---|---|
| Input Offset Voltage<br>($R_S \leqslant$ 10 kΩ, 9.0 V $\leqslant V_{CC} \leqslant$ 15 V, -9.0 V $\geqslant V_{EE} \geqslant$ 15 V) | $V_{IO}$ | – | – | 10 | mV |
| Input Offset Current | $I_{IO}$ | – | – | 750 | nA |
| Input Bias Current | $I_{IB}$ | – | – | 2.0 | μA |
| Large Signal Voltage Gain<br>($R_L \geqslant$ 2.0 kΩ, $V_O$ = ±10 V) | $A_V$ | 12 | – | – | V/mV |
| Input Resistance | ri | 35 | – | – | kΩ |

## TYPICAL CHARACTERISTICS

**FIGURE 2 – TEST CIRCUIT**
($V_{CC}$ = +15 Vdc, $V_{EE}$ = -15 Vdc, $T_A$ = +25°C)



| Fig. No. | Curve No. | Test Conditions $R_1$ (Ω) | $R_2$ (Ω) | $R_3$ (Ω) | $C_1$ (pF) | $C_2$ (pF) |
|---|---|---|---|---|---|---|
| 3 | 1 | 10 k | 10 k | 1.5 k | 5.0 k | 200 |
| | 2 | 10 k | 100 k | 1.5 k | 500 | 20 |
| | 3 | 10 k | 1.0 M | 1.5 k | 100 | 3.0 |
| | 4 | 1.0 k | 1.0 M | 0 | 10 | 3.0 |
| 4 | 1 | 1.0 k | 1.0 M | 0 | 10 | 3.0 |
| | 2 | 10 k | 1.0 M | 1.5 k | 100 | 3.0 |
| | 3 | 10 k | 100 k | 1.5 k | 500 | 20 |
| | 4 | 10 k | 10 k | 1.5 k | 5.0 k | 200 |
| 5 | 1 | 0 | ∞ | 1.5 k | 5.0 k | 200 |
| | 2 | 0 | ∞ | 1.5 k | 500 | 20 |
| | 3 | 0 | ∞ | 1.5 k | 100 | 3.0 |
| | 4 | 0 | ∞ | 0 | 10 | 3.0 |

FIGURE 3 – LARGE SIGNAL SWING versus FREQUENCY

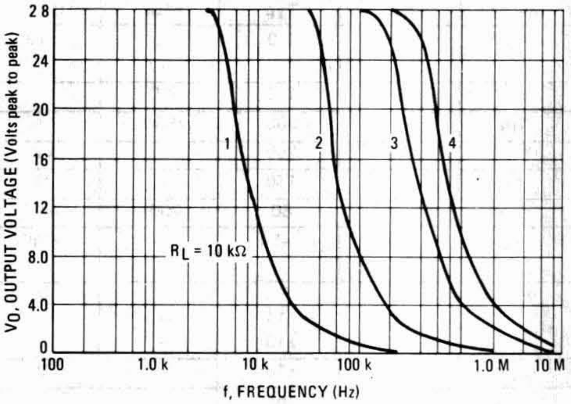


FIGURE 4 – CLOSED LOOP VOLTAGE GAIN versus FREQUENCY

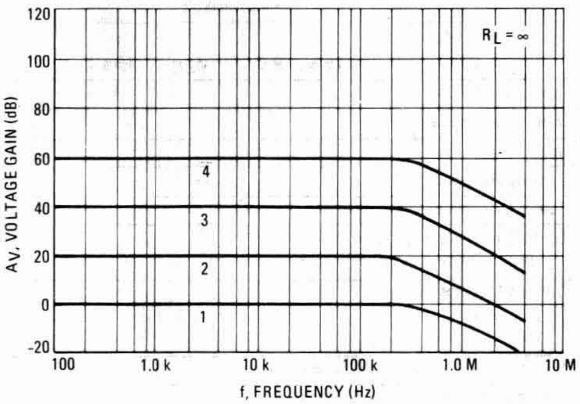


FIGURE 5 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

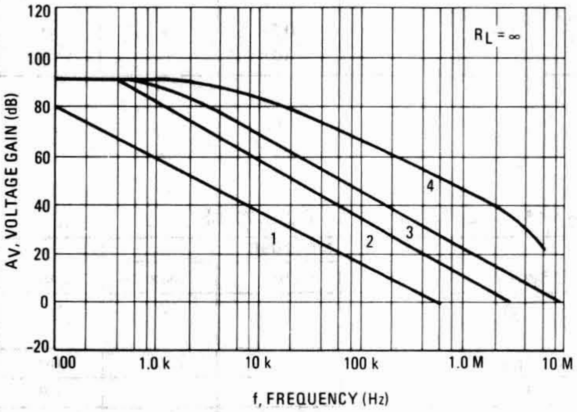


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

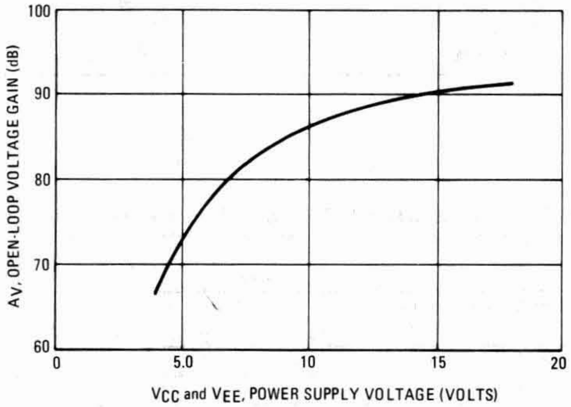


FIGURE 7 – SLEW RATE versus CLOSED LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

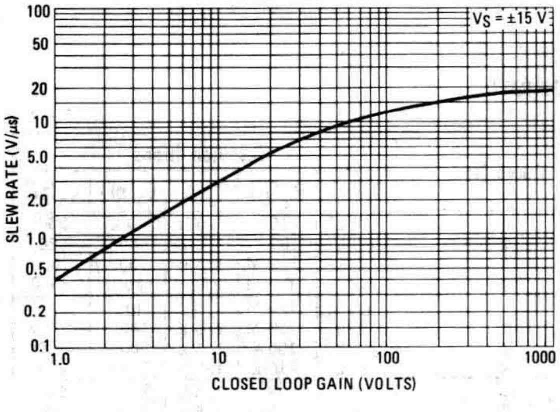
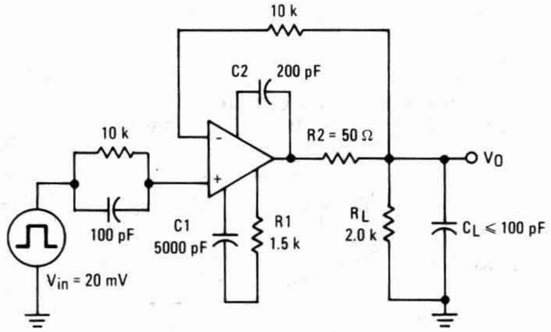


FIGURE 8 – TRANSIENT RESPONSE TEST CIRCUIT


10 k
C2
200 pF
10 k
R2 = 50 Ω
-
+
VO
100 pF
C1
5000 pF
R1
1.5 k
RL
2.0 k
CL ≤ 100 pF
Vin = 20 mV

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1733G | −55°C to +125°C | Metal Can |
| MC1733L | −55°C to +125°C | Ceramic DIP |
| MC1733CD | 0°C to +70°C | SO-14 |
| MC1733CG | 0°C to +70°C | Metal Can |
| MC1733CL | 0°C to +70°C | Ceramic DIP |
| MC1733CP | 0°C to +70°C | Plastic DIP |

# MC1733
# MC1733C

## DIFFERENTIAL VIDEO AMPLIFIER

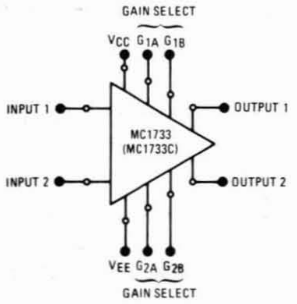
. . . a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

- Bandwidth — 120 MHz typical @ $A_{vd}$ = 10
- Rise Time — 2.5 ns typical @ $A_{vd}$ = 10
- Propagation Delay Time — 3.6 ns typical @ $A_{vd}$ = 10

## DIFFERENTIAL VIDEO WIDEBAND AMPLIFIER

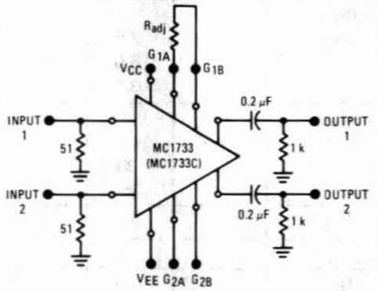
### SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 — BASIC CIRCUIT



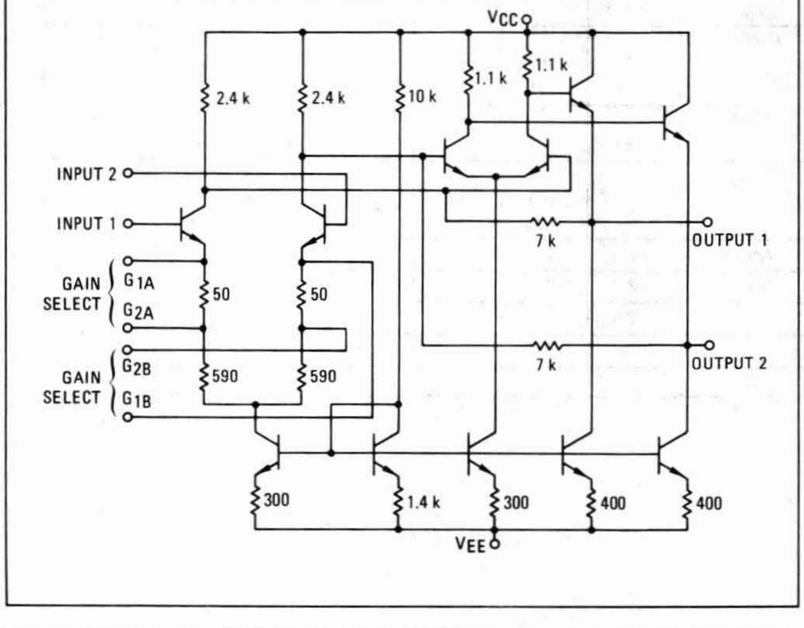
GAIN SELECT
VCC G1A G1B
INPUT 1
OUTPUT 1
MC1733 (MC1733C)
INPUT 2
OUTPUT 2
VEE G2A G2B
GAIN SELECT

FIGURE 2 — VOLTAGE GAIN ADJUST CIRCUIT



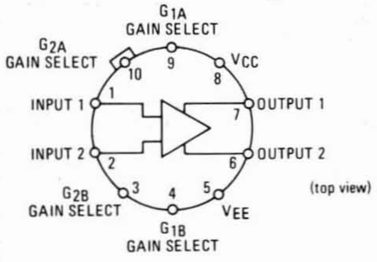
Radj
G1A
VCC
G1B
0.2 µF
INPUT 1
OUTPUT 1
51
MC1733 (MC1733C)
1 k
INPUT 2
OUTPUT 2
0.2 µF
51
1 k
VEE G2A G2B

FIGURE 3 — EQUIVALENT CIRCUIT SCHEMATIC



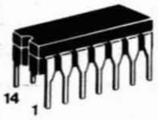
VCC
2.4 k
2.4 k
10 k
1.1 k
1.1 k
INPUT 2
INPUT 1
7 k
OUTPUT 1
GAIN SELECT G1A G2A
50
50
GAIN SELECT G2B G1B
590
590
7 k
OUTPUT 2
300
1.4 k
300
400
400
VEE

**G SUFFIX**
METAL PACKAGE
CASE 603-04
TO-100



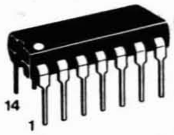
G1A GAIN SELECT
G2A GAIN SELECT
10
9
VCC
8
INPUT 1
1
OUTPUT 1
7
INPUT 2
2
OUTPUT 2
6
G2B GAIN SELECT
3
4
5
VEE
(top view)
G1B GAIN SELECT

(Top View)

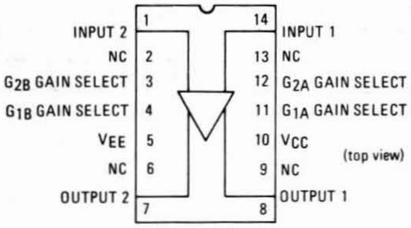


**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA

**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05



**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14



INPUT 2 1
NC 2
G2B GAIN SELECT 3
G1B GAIN SELECT 4
VEE 5
NC 6
OUTPUT 2 7
14 INPUT 1
13 NC
12 G2A GAIN SELECT
11 G1A GAIN SELECT
10 VCC
9 NC
8 OUTPUT 1
(top view)

(Top View)

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +8.0<br>-8.0 | Volts |
| Differential Input Voltage | $V_{in}$ | ±5.0 | Volts |
| Common-Mode Input Voltage | $V_{ICM}$ | ±6.0 | Volts |
| Output Current | $I_O$ | 10 | mA |
| Internal Power Dissipation (Note 1) | $P_D$ | | |
| Metal Can Package | | 500 | mW |
| Ceramic Dual In-Line Package | | 500 | |
| Operating Temperature Range MC1733C | $T_A$ | 0 to +70 | °C |
| MC1733 | | -55 to +125 | |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +6.0 Vdc, $V_{EE}$ = -6.0 Vdc, at $T_A$ = +25°C unless otherwise noted.)

| | | MC1733 | | | MC1733C | | | |
|---|---|---|---|---|---|---|---|---|
| Characteristic | Symbol | Min | Typ | Max | Min | Typ | Max | Units |
| Differential Voltage Gain | $A_{vd}$ | | | | | | | V/V |
| Gain 1 (Note 2) | | 300 | 400 | 500 | 250 | 400 | 600 | |
| Gain 2 (Note 3) | | 90 | 100 | 110 | 80 | 100 | 120 | |
| Gain 3 (Note 4) | | 9.0 | 10 | 11 | 8.0 | 10 | 12 | |
| Bandwidth ($R_s$ = 50 Ω) | BW | | | | | | | MHz |
| Gain 1 | | – | 40 | – | – | 40 | – | |
| Gain 2 | | – | 90 | – | – | 90 | – | |
| Gain 3 | | – | 120 | – | – | 120 | – | |
| Rise Time ($R_s$ = 50 Ω, $V_O$ = 1 Vp-p) | $t_{TLH}$<br>$t_{THL}$ | | | | | | | ns |
| Gain 1 | | – | 10.5 | – | – | 10.5 | – | |
| Gain 2 | | – | 4.5 | 10 | – | 4.5 | 12 | |
| Gain 3 | | – | 2.5 | – | – | 2.5 | – | |
| Propagation Delay ($R_s$ = 50 Ω, $V_O$ = 1 Vp-p) | $t_{PLH}$<br>$t_{PHL}$ | | | | | | | ns |
| Gain 1 | | – | 7.5 | – | – | 7.5 | – | |
| Gain 2 | | – | 6.0 | 10 | – | 6.0 | 10 | |
| Gain 3 | | – | 3.6 | – | – | 3.6 | – | |
| Input Resistance | $R_{in}$ | | | | | | | kΩ |
| Gain 1 | | – | 4.0 | – | – | 4.0 | – | |
| Gain 2 | | 20 | 30 | – | 10 | 30 | – | |
| Gain 3 | | – | 250 | – | – | 250 | – | |
| Input Capacitance (Gain 2) | $C_{in}$ | – | 2.0 | – | – | 2.0 | – | pF |
| Input Offset Current (Gain 3) | $\|I_{IO}\|$ | – | 0.4 | 3.0 | – | 0.4 | 5.0 | µA |
| Input Bias Current (Gain 3) | $I_{IB}$ | – | 9.0 | 20 | – | 9.0 | 30 | µA |
| Input Noise Voltage ($R_s$ = 50 Ω, BW = 1 kHz to 10 MHz | $V_n$ | – | 12 | – | – | 12 | – | µV(rms) |
| Input Voltage Range (Gain 2) | $V_{in}$ | ±1.0 | – | – | ±1.0 | – | – | V |
| Common-Mode Rejection Ratio | CMRR | | | | | | | dB |
| Gain 2 ($V_{CM}$ = ±1 V, f ≤ 100 kHz) | | 60 | 86 | – | 60 | 86 | – | |
| Gain 2 ($V_{CM}$ = ±1 V, f = 5 MHz) | | – | 60 | – | – | 60 | – | |
| Supply Voltage Rejection Ratio | PSRR | | | | | | | dB |
| Gain 2 ($\Delta V_s$ = ±0.5 V) | | 50 | 70 | – | 50 | 70 | – | |
| Output Offset Voltage | $V_{OO}$ | | | | | | | V |
| Gain 1 | | – | 0.6 | 1.5 | – | 0.6 | 1.5 | |
| Gain 2 and Gain 3 | | – | 0.35 | 1.0 | – | 0.35 | 1.5 | |
| Output Common-Mode Voltage (Gain3) | $V_{CMO}$ | 2.4 | 2.9 | 3.4 | 2.4 | 2.9 | 3.4 | V |
| Output Voltage Swing (Gain 2) | $V_O$ | 3.0 | 4.0 | – | 3.0 | 4.0 | – | Vp-p |
| Output Sink Current (Gain 2) | $I_O$ | 2.5 | 3.6 | – | 2.5 | 3.6 | – | mA |
| Output Resistance | $R_{out}$ | – | 20 | – | – | 20 | – | Ω |
| Power Supply Current (Gain 2) | $I_D$ | – | 18 | 24 | – | 18 | 24 | mA |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +6.0 Vdc, $V_{EE}$ = –6.0 Vdc, at $T_A$ = $T_{high}$ to $T_{low}$ unless otherwise noted.)*

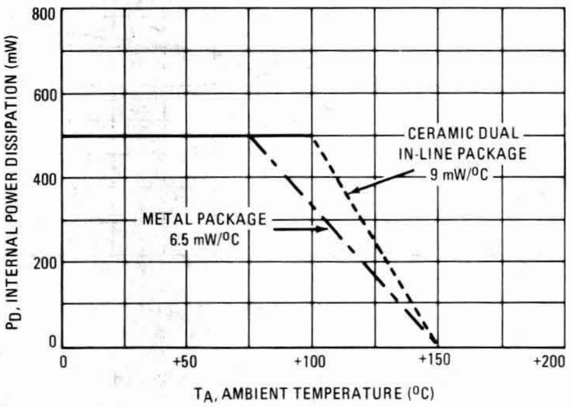
| Characteristic | Symbol | MC1733 Min | MC1733 Typ | MC1733 Max | MC1733C Min | MC1733C Typ | MC1733C Max | Units |
|---|---|---|---|---|---|---|---|---|
| Differential Voltage Gain | $A_{vd}$ | | | | | | | V/V |
| Gain 1 (Note 2) | | 200 | – | 600 | 250 | – | 600 | |
| Gain 2 (Note 3) | | 80 | – | 120 | 80 | – | 120 | |
| Gain 3 (Note 4) | | 8.0 | – | 12 | 8.0 | – | 12 | |
| Input Resistance<br>Gain 2 | $R_{in}$ | 8.0 | – | – | 8.0 | – | – | kΩ |
| Input Offset Current (Gain 3) | $\lvert I_{IO}\rvert$ | – | – | 5.0 | – | – | 6.0 | µA |
| Input Bias Current (Gain 3) | $I_{IB}$ | – | – | 40 | – | – | 40 | µA |
| Input Voltage Range (Gain 2) | $V_{in}$ | ±1.0 | – | – | ±1.0 | – | – | V |
| Common-Mode Rejection Ratio<br>Gain 2 ($V_{CM}$ = ±1 V, f ≤ 100 kHz) | CMRR | 50 | – | – | 50 | – | – | dB |
| Supply Voltage Rejection Ratio<br>Gain 2 ($\Delta V_s$ = ±0.5 V) | PSRR | 50 | – | – | 50 | – | – | dB |
| Output Offset Voltage | $V_{OO}$ | | | | | | | V |
| Gain 1 | | – | – | 1.5 | – | – | 1.5 | |
| Gain 2 and Gain 3 | | – | – | 1.2 | – | – | 1.5 | |
| Output Voltage Swing (Gain 2) | $V_O$ | 2.5 | – | – | 2.5 | – | – | Vp-p |
| Output Sink Current (Gain 2) | $I_O$ | 2.2 | – | – | 2.5 | – | – | mA |
| Power Supply Current (Gain 2) | $I_D$ | – | – | 27 | – | – | 27 | mA |

*$T_{low}$ = 0°C for MC1733C, –55°C for MC1733
$T_{high}$ = +70°C for MC1733C, +125°C for MC1733.

**NOTES**

Note 1: Derate metal package at 6.5 mW/°C for operation at ambient temperatures above 75°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 100°C (see Figure 4). If operation at high ambient temperatures is required (MC1733) a heatsink may be necessary to limit maximum junction temperature to 150°C. Thermal resistance, junction-to-case, for the metal package is 69.4°C per Watt.
Note 2: Gain Select pins $G_{1A}$ and $G_{1B}$ connected together.
Note 3: Gain Select pins $G_{2A}$ and $G_{2B}$ connected together.
Note 4: All Gain Select pins open.

**FIGURE 4 – MAXIMUM ALLOWABLE POWER DISSIPATION**



## TYPICAL CHARACTERISTICS

($V_{CC}$ = +6.0 Vdc, $V_{EE}$ = –6.0 Vdc, $T_A$ = +25°C unless otherwise noted.)

**FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE**

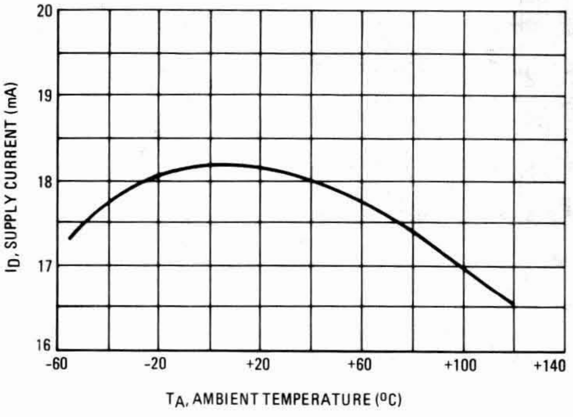
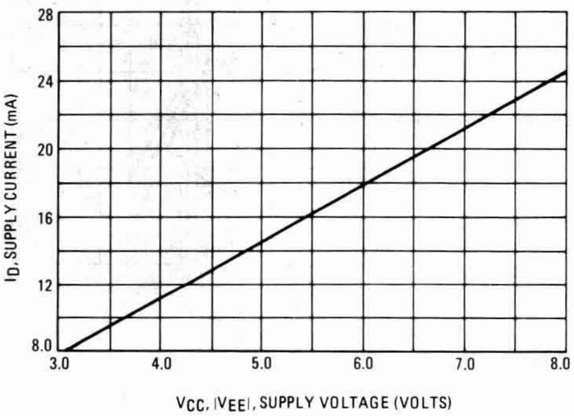


**FIGURE 6 – SUPPLY CURRENT versus SUPPLY VOLTAGE**



## TYPICAL CHARACTERISTICS (continued)

($V_{CC}$ = +6.0 Vdc, $V_{EE}$ = −6.0 Vdc, $T_A$ = +25°C unless otherwise noted.)

FIGURE 7 – GAIN verus TEMPERATURE

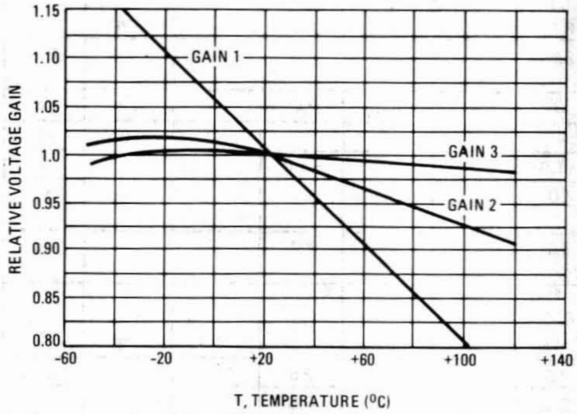


FIGURE 8 – GAIN versus FREQUENCY

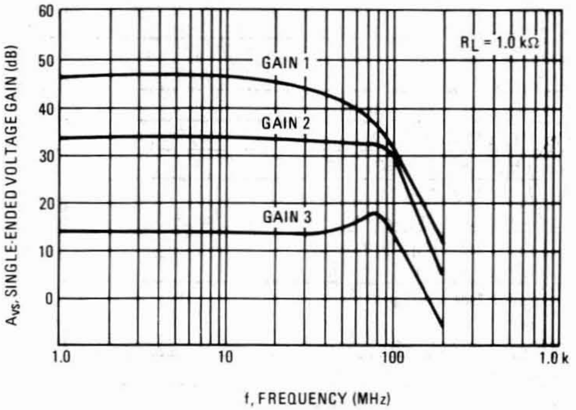


FIGURE 9 – GAIN versus SUPPLY VOLTAGE

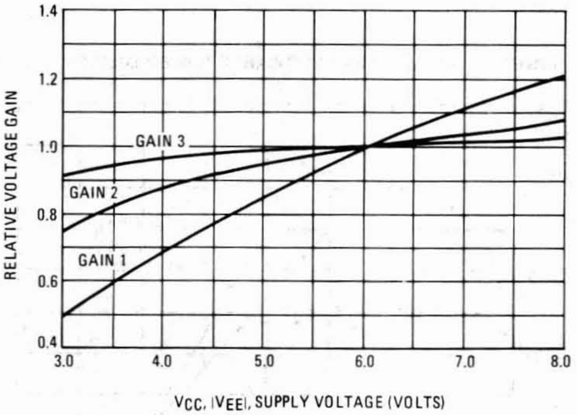


FIGURE 10 – GAIN versus R$_{ADJUST}$

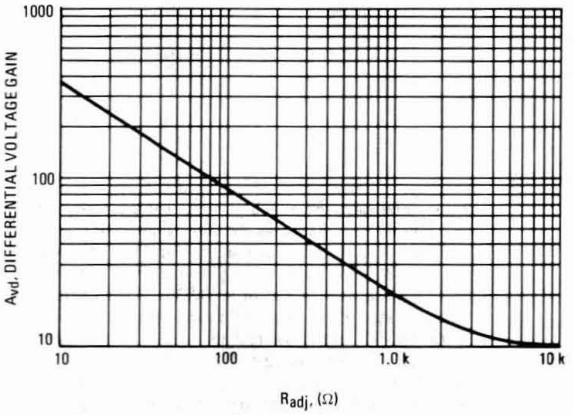


FIGURE 11 – GAIN versus FREQUENCY and SUPPLY VOLTAGE

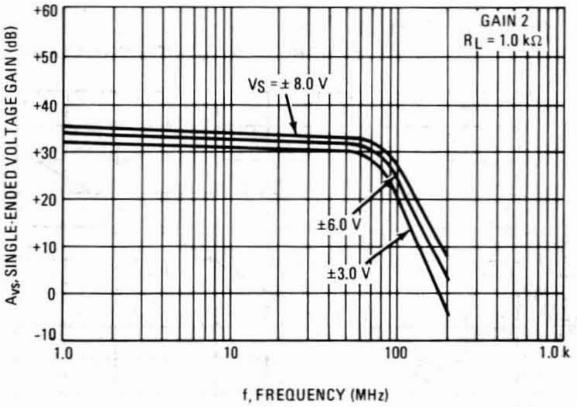
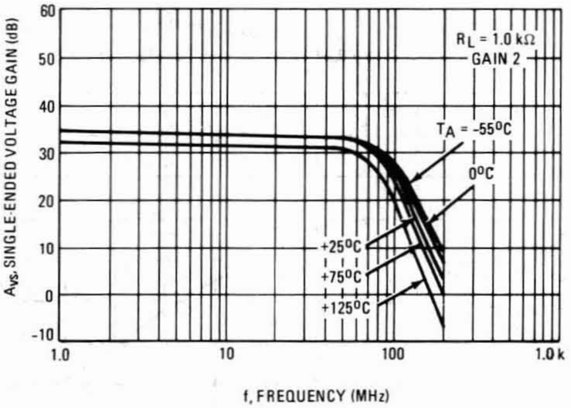


FIGURE 12 – GAIN versus FREQUENCY and TEMPERATURE



## TYPICAL CHARACTERISTICS (continued)

($V_{CC}$ = +6.0 Vdc, $V_{EE}$ = -6.0 Vdc, $T_A$ = +25°C unless otherwise noted.)

**FIGURE 13 – PULSE RESPONSE versus GAIN**

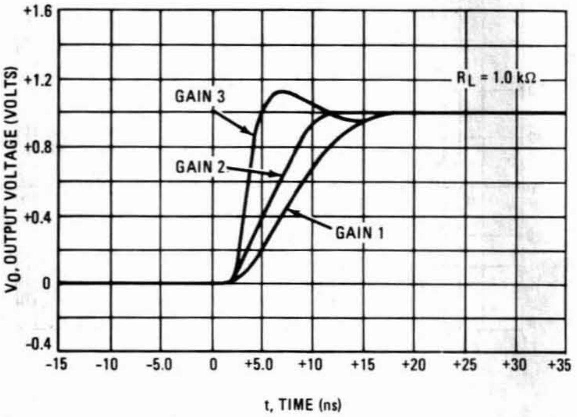


**FIGURE 14 – PULSE RESPONSE versus SUPPLY VOLTAGE**

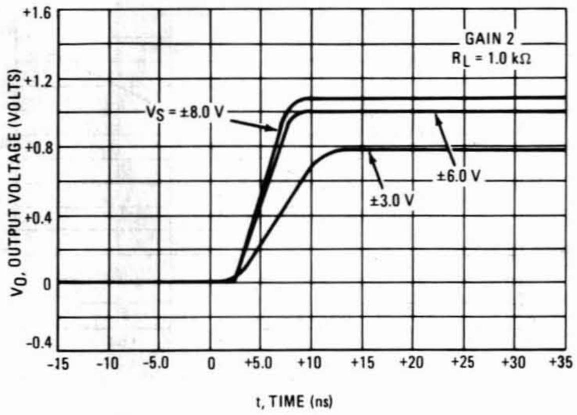


**FIGURE 15 – PULSE RESPONSE versus TEMPERATURE**

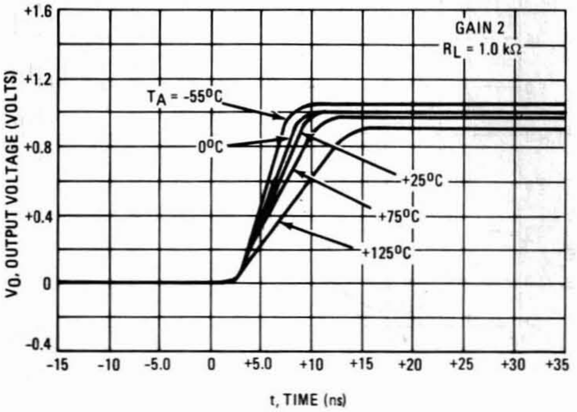


**FIGURE 16 – DIFFERENTIAL OVERDRIVE RECOVERY TIME**

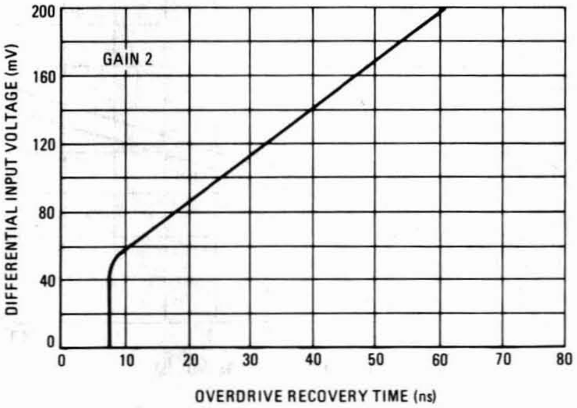


**FIGURE 17 – PHASE SHIFT versus FREQUENCY**

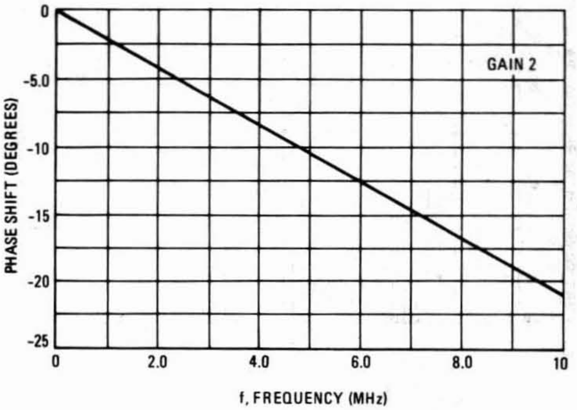
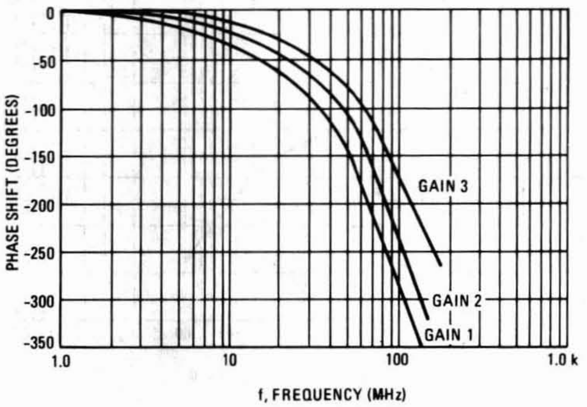


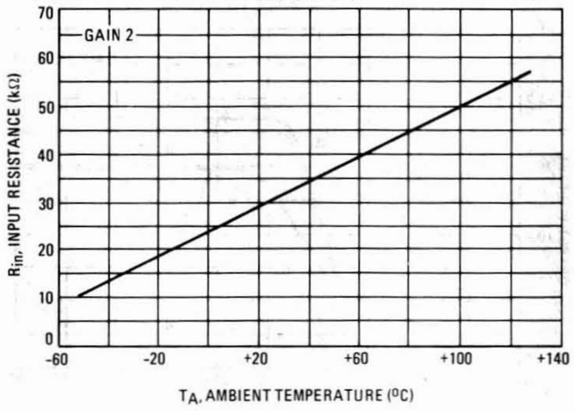
**FIGURE 18 – PHASE SHIFT versus FREQUENCY**



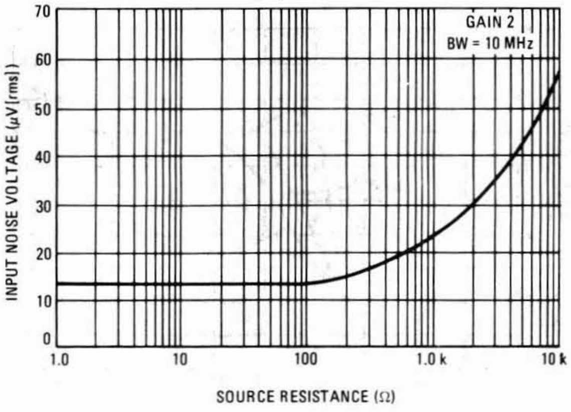
## TYPICAL CHARACTERISTICS (Continued)

($V_{CC}$ = +6.0 Vdc, $V_{EE}$ = -6.0 Vdc, $T_A$ = +25°C unless otherwise noted.)

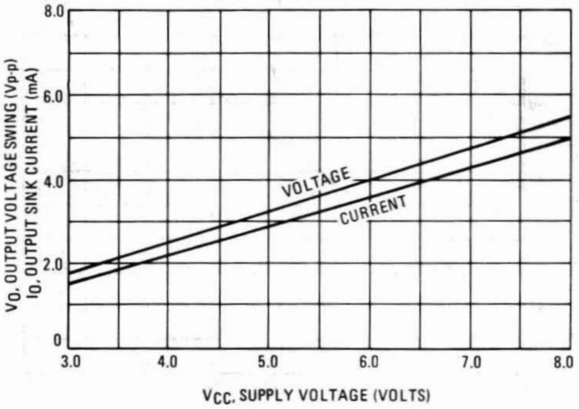
### FIGURE 19 – INPUT RESISTANCE versus TEMPERATURE



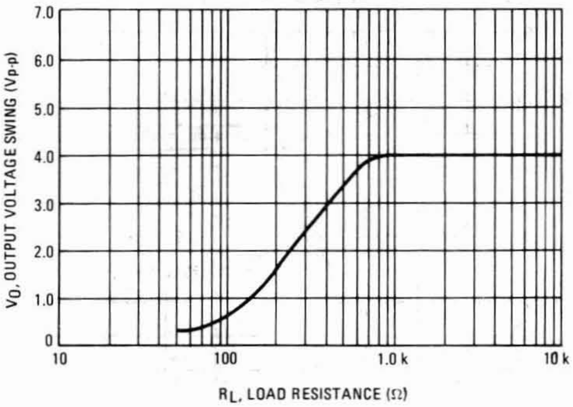
### FIGURE 20 – INPUT NOISE VOLTAGE



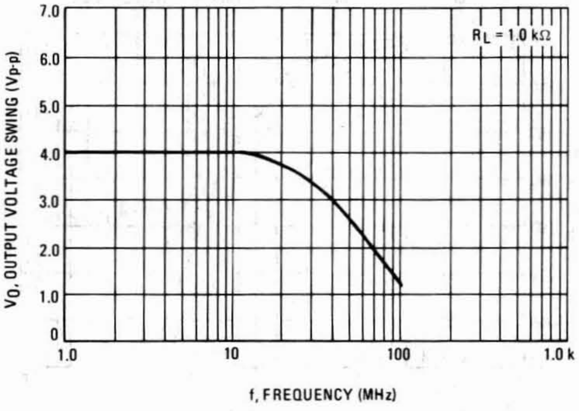
### FIGURE 21 – OUTPUT VOLTAGE SWING and SINK CURRENT versus SUPPLY VOLTAGE



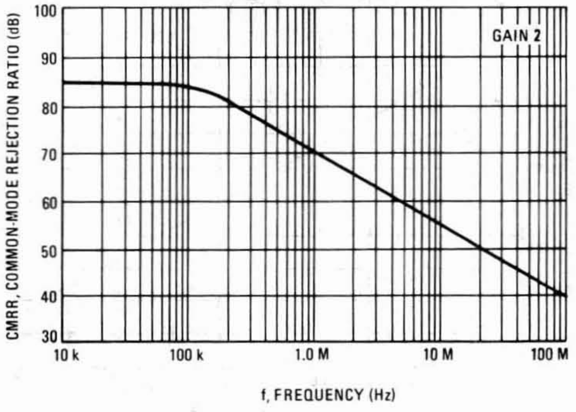
### FIGURE 22 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



### FIGURE 23 – OUTPUT VOLTAGE SWING versus FREQUENCY

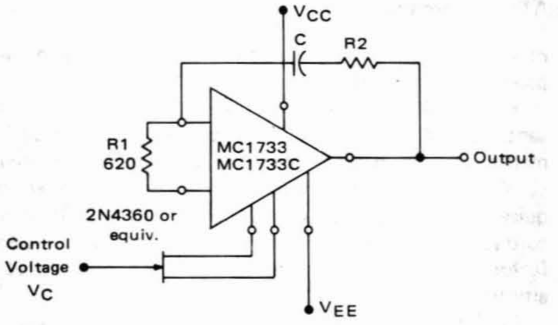


### FIGURE 24 – COMMON-MODE REJECTION RATIO



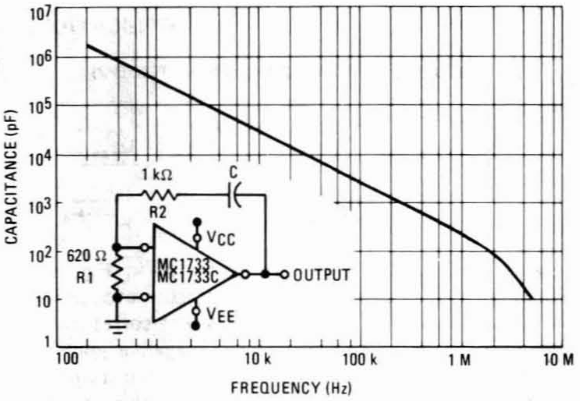
## APPLICATIONS INFORMATION

FIGURE 25 – VOLTAGE CONTROLLED OSCILLATOR



By changing the voltage $V_C$ the gain will vary over a range of 10 to 400. This will give a frequency variation about the value set by the capacitor and shown in Figure 26.

FIGURE 26 – OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES



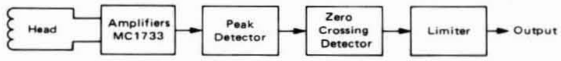
### TAPE, DRUM OR DISC MEMORY READ AMPLIFIERS

The first of several methods to be discussed is shown in Figure 27. This block diagram describes a simple Read circuit with no threshold circuitry. Each block represents a basic function that must be performed by the Read circuit. The first block, referred to as "amplfiication", increases the level of the signal available from the Read head to a level adequate to drive the peak detector. Obviously, these signal levels will vary depending on factors such as tape speed, whether the system used is disc or tape, and the type of head and the circuitry used. For a representative tape system, levels of 7 to 25 mV for the signal from the Read head and 2 V for the signal to the peak detector are typical. These signal levels are "peak-to-peak" unless otherwise specified. On the basis of the signal levels mentioned above, the overall amplification required is 38 to 49 dB.

How the overall gain requirement is implemented will depend somewhat on the system used. For instance, a tape cassette system with variable tape speed may utilize a first stage for gain and a second stage primarily for gain control. Thus, a typical circuit would utilize 35 dB in the first stage and 10 to 15 dB in the second stage.

Devices suitable for use as amplifiers fall into one of two categories, operational amplifiers or wideband video amplifiers. Lower speed equipment with low transfer rates commonly uses low cost operational amplifiers. Examples of these are the MC1741, MC1458, MC1709, and MLM301. Equipment requiring higher transfer rates, such as disc systems normally use wideband amplifiers such as the MC1733. The actual cross-over point where wideband amplifiers are used exclusively varies with equipment design. For purposes of comparison, the MLM301 has slightly less than a 40 dB open-loop gain at 100 kHz; the MC1741, a compensated op-amp, has approximately 20 dB open loop gain at 100 kHz; the MC1733 has approximately 33 dB of gain out to 100 MHz (depending on gain option and loading).

FIGURE 27 – TYPICAL READ CIRCUIT (METHOD 1)



There are a number of ways to implement the peak detector function. However, the simplest and most widely used method is a passive differentiator that generates "zero-crossings" for each of the data peaks in the Read signal.

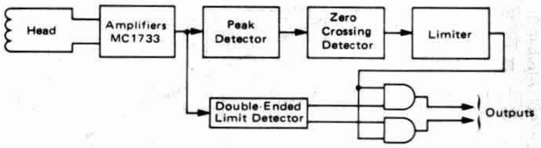
The actual circuitry used to differentiate the Read signal varies from a differential LC type in disc systems to a simple RC type in reel and cassette systems. Either type, of course, attenuates the signal by an amount depending on the circuit used and system specifications. A good approximation of attenuation using the RC type is 20 dB. Thus, the 2 V signal going into the differentiator is reduced to 200 mV.

The next block in Figure 27 to be discussed is the zero-crossing detector. In most cases detection of the zero-crossings is combined with the limiter. These functions serve to generate a TTL compatible pulse waveform with "edges" corresponding to zero-crossings. For low transfer rates, the circuit often used consists of an operational amplifier with series or shunt limiting. For higher transfer rates (greater than 100K B/S) comparators are used.

The method described above is often modified to include threshold sensing. In Figure 28, the function called "double-ended, limit-detector" enables the output NAND gate when either the negative or positive data peaks of the Read signal exceed a predetermined threshold. This function can be implemented in either of two ways. One method first rectifies the signal before it is applied to a comparator with a set threshold. The other method utilizes two comparators, one comparator for positive-going peaks and the other for negative-going peaks. These comparator outputs are then combined in the output logic gates.

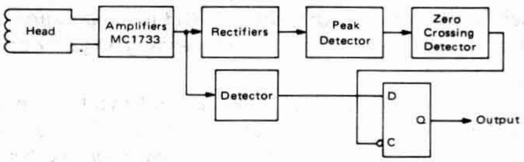
## APPLICATIONS INFORMATION (continued)

FIGURE 28 – READ CIRCUIT (METHOD 2)


Head
Amplifiers MC1733
Peak Detector
Zero Crossing Detector
Limiter
Double-Ended Limit Detector
Outputs

Another common technique is shown in Figure 29. The branch labeled rectifiers, peak detector, etc., provides a clock transition of the D flip-flop that corresponds to the peak of both the positive and negative-going data peaks. This branch may include threshold circuitry prior to the peak detector. The detector in the lower path detects whether the signal peaks are positive or negative and feeds this data to the flip-flop. This detector can be implemented using a comparator with pre-set threshold.

FIGURE 29 – READ CIRCUIT (METHOD 3)

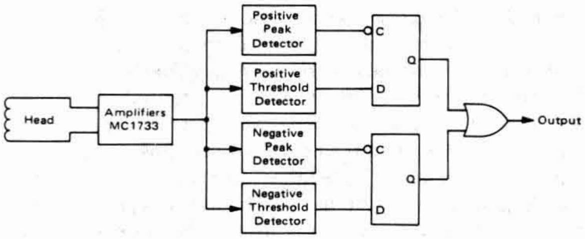

Head
Amplifiers MC1733
Rectifiers
Peak Detector
Zero Crossing Detector
Detector
D
Q
C
Output

The technique shown in Figure 30 uses separate circuits with threshold provisions for both negative and positive peaks. The peak detectors and threshold detectors may be implemented with two comparators and two passive differentiators.

Each of the methods shown offer certain intrinsic advantages or disadvantages. The overall decision as to which method to use however often involves other important considerations. These could include cost and system requirements or circuitry other than simply the Read circuitry. For instance, if cost is the predominate overall factor, then approach one may be the only feasible alternative.

Method four was included as a design example because it illustrates several unique advantages. First, it uses threshold sensing to reduce noise peak errors. Second, it may be implemented using only integrated circuits. Third, it offers separate, direct threshold sensing for both positive and negative peaks.

FIGURE 30 – READ CIRCUIT (Method 4)


Positive Peak Detector
Positive Threshold Detector
Negative Peak Detector
Negative Threshold Detector
Head
Amplifiers MC1733
C
Q
D
C
Q
D
Output

**ORDERING INFORMATION**

| Device | Alternate | Temperature Range | Package |
|---|---|---|---|
| MC1741CD | — | 0°C to +70°C | SO-8 |
| MC1741CG | LM741CD, μA741HC | 0°C to +70°C | Metal Can |
| MC1741CP1 | LM741CN, μA741TC | 0°C to +70°C | Plastic DIP |
| MC1741CU | — | 0°C to +70°C | Ceramic DIP |
| MC1741G | — | −55°C to +125°C | Metal Can |
| MC1741U | — | −55°C to +125°C | Ceramic DIP |

# MC1741
# MC1741C

## INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

## OPERATIONAL AMPLIFIER
### SILICON MONOLITHIC INTEGRATED CIRCUIT

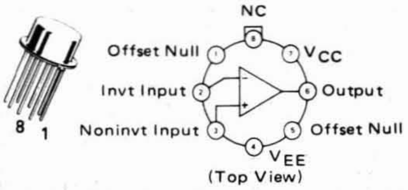
**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

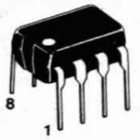
| Rating | Symbol | MC1741C | MC1741 | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>−18 | +22<br>−22 | Vdc<br>Vdc |
| Input Differential Voltage | $V_{ID}$ | ±30 | | Volts |
| Input Common Mode Voltage (Note 1) | $V_{ICM}$ | ±15 | | Volts |
| Output Short Circuit Duration (Note 2) | $t_S$ | Continuous | | |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | −55 to +125 | °C |
| Storage Temperature Range<br>Metal and Ceramic Packages<br>Plastic Packages | $T_{stg}$ | <br>−65 to +150<br>−55 to +125 | | °C |

Note 1. For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

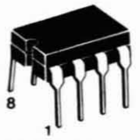
**G SUFFIX**
METAL PACKAGE
CASE 601-04

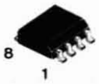

NC
8
Offset Null
VCC
Invt Input
Output
Noninvt Input
Offset Null
8
1
VEE
(Top View)



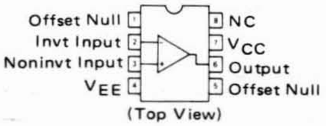
**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04

**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02

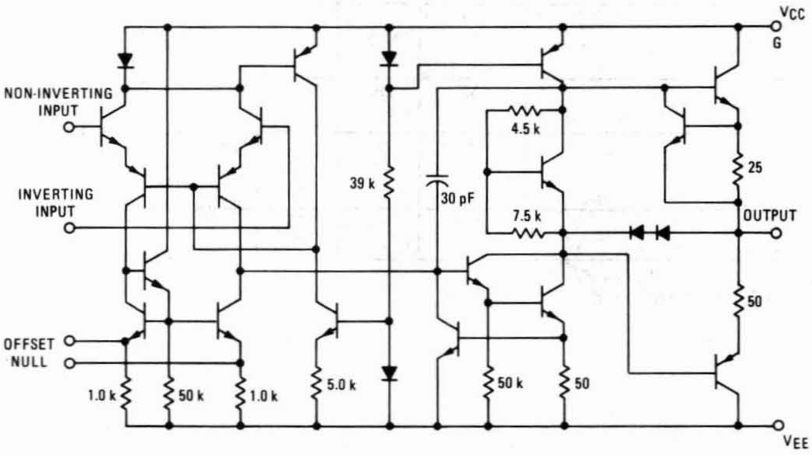




**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8


Offset Null 1
Invt Input 2
Noninvt Input 3
VEE 4
8 NC
7 VCC
6 Output
5 Offset Null
(Top View)

## EQUIVALENT CIRCUIT SCHEMATIC


VCC
G
NON-INVERTING INPUT
INVERTING INPUT
OFFSET NULL
1.0 k
50 k
1.0 k
5.0 k
39 k
30 pF
4.5 k
7.5 k
50 k
50
25
OUTPUT
50
VEE

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $V_{EE}$ = 15 V, $T_A$ = 25°C unless otherwise noted).

| Characteristic | Symbol | MC1741 | | | MC1741C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($R_S \leqslant$ 10 k) | $V_{IO}$ | – | 1.0 | 5.0 | – | 2.0 | 6.0 | mV |
| Input Offset Current | $I_{IO}$ | – | 20 | 200 | – | 20 | 200 | nA |
| Input Bias Current | $I_{IB}$ | – | 80 | 500 | – | 80 | 500 | nA |
| Input Resistance | $r_i$ | 0.3 | 2.0 | – | 0.3 | 2.0 | – | MΩ |
| Input Capacitance | $C_i$ | – | 1.4 | – | – | 1.4 | – | pF |
| Offset Voltage Adjustment Range | $V_{IOR}$ | – | ±15 | – | – | ±15 | – | mV |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±12 | ±13 | – | ±12 | ±13 | – | V |
| Large Signal Voltage Gain ($V_O$ = ±10 V, $R_L \geqslant$ 2.0 k) | $A_v$ | 50 | 200 | – | 20 | 200 | – | V/mV |
| Output Resistance | $r_o$ | – | 75 | – | – | 75 | – | Ω |
| Common Mode Rejection Ratio ($R_S \leqslant$ 10 k) | CMRR | 70 | 90 | – | 70 | 90 | – | dB |
| Supply Voltage Rejection Ratio ($R_S \leqslant$ 10 k) | PSRR | – | 30 | 150 | – | 30 | 150 | μV/V |
| Output Voltage Swing | $V_O$ | | | | | | | V |
| ($R_L \geqslant$ 10 k) | | ±12 | ±14 | – | ±12 | ±14 | – | |
| ($R_L \geqslant$ 2 k) | | ±10 | ±13 | – | ±10 | ±13 | – | |
| Output Short-Circuit Current | $I_{os}$ | – | 20 | – | – | 20 | – | mA |
| Supply Current | $I_D$ | – | 1.7 | 2.8 | – | 1.7 | 2.8 | mA |
| Power Consumption | $P_C$ | – | 50 | 85 | – | 50 | 85 | mW |
| Transient Response (Unity Gain – Non-Inverting) | | | | | | | | |
| ($V_I$ = 20 mV, $R_L \geqslant$ 2 k, $C_L \leqslant$ 100 pF) Rise Time | $t_{TLH}$ | – | 0.3 | – | – | 0.3 | – | μs |
| ($V_I$ = 20 mV, $R_L \geqslant$ 2 k, $C_L \leqslant$ 100 pF) Overshoot | os | – | 15 | – | – | 15 | – | % |
| ($V_I$ = 10 V, $R_L \geqslant$ 2 k, $C_L \leqslant$ 100 pF) Slew Rate | SR | – | 0.5 | – | – | 0.5 | – | V/μs |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = $T_{low}$ to $T_{high}$ unless otherwise noted).

| Characteristic | Symbol | MC1741 | | | MC1741C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($R_S \leqslant$ 10 kΩ) | $V_{IO}$ | – | 1.0 | 6.0 | – | – | 7.5 | mV |
| Input Offset Current | $I_{IO}$ | | | | | | | nA |
| ($T_A$ = 125°C) | | – | 7.0 | 200 | – | – | – | |
| ($T_A$ = -55°C) | | – | 85 | 500 | – | – | – | |
| ($T_A$ = 0°C to +70°C) | | – | – | – | – | – | 300 | |
| Input Bias Current | $I_{IB}$ | | | | | | | nA |
| ($T_A$ = 125°C) | | – | 30 | 500 | – | – | – | |
| ($T_A$ = -55°C) | | – | 300 | 1500 | – | – | – | |
| ($T_A$ = 0°C to +70°C) | | – | – | – | – | – | 800 | |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±12 | ±13 | – | – | – | – | V |
| Common Mode Rejection Ratio ($R_S \leqslant$ 10 k) | CMRR | 70 | 90 | – | – | – | – | dB |
| Supply Voltage Rejection Ratio ($R_S \leqslant$ 10 k) | PSRR | – | 30 | 150 | – | – | – | μV/V |
| Output Voltage Swing | $V_O$ | | | | | | | V |
| ($R_L \geqslant$ 10 k) | | ±12 | ±14 | – | – | – | – | |
| ($R_L \geqslant$ 2 k) | | ±10 | ±13 | – | ±10 | ±13 | – | |
| Large Signal Voltage Gain ($R_L \geqslant$ 2 k, $V_{out}$ = ±10 V) | $A_v$ | 25 | – | – | 15 | – | – | V/mV |
| Supply Currents | $I_D$ | | | | | | | mA |
| ($T_A$ = 125°C) | | – | 1.5 | 2.5 | – | – | – | |
| ($T_A$ = -55°C) | | – | 2.0 | 3.3 | – | – | – | |
| Power Consumption ($T_A$ = +125°C) | $P_C$ | – | 45 | 75 | – | – | – | mW |
| ($T_A$ = -55°C) | | – | 60 | 100 | – | – | – | |

*$T_{high}$ = 125°C for MC1741 and 70°C for MC1741C
$T_{low}$ = -55°C for MC1741 and 0°C for MC1741C

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

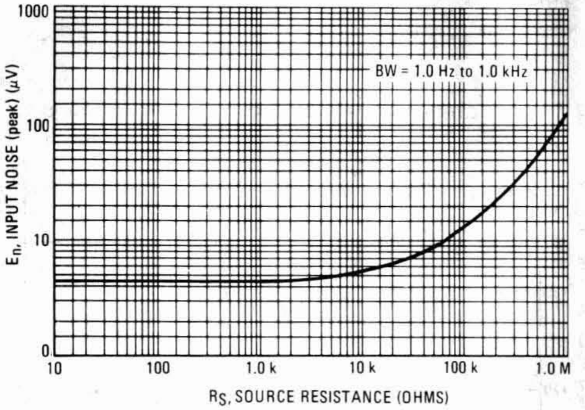


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

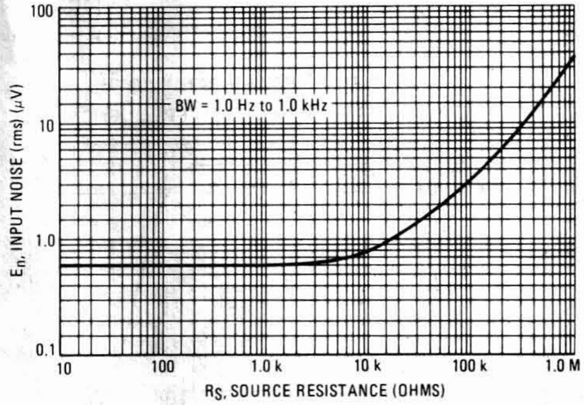


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

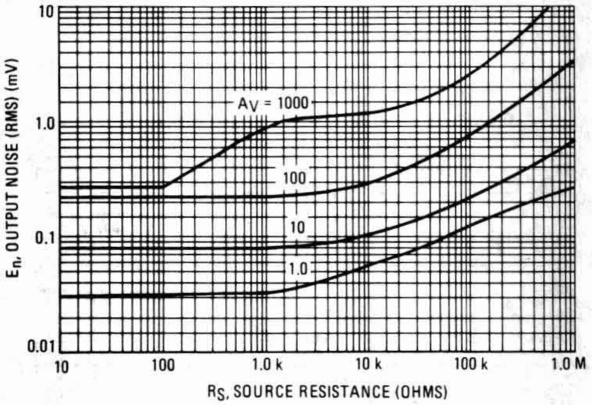


FIGURE 4 – SPECTRAL NOISE DENSITY

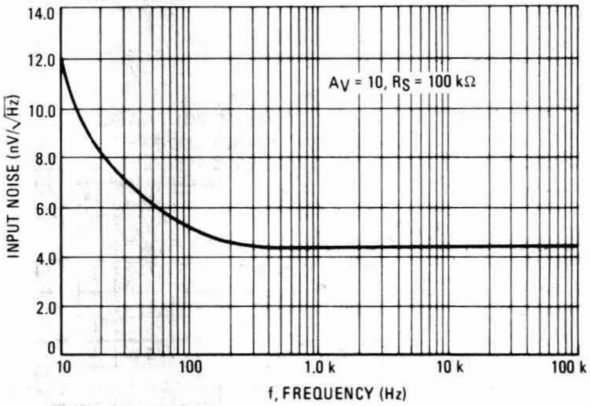
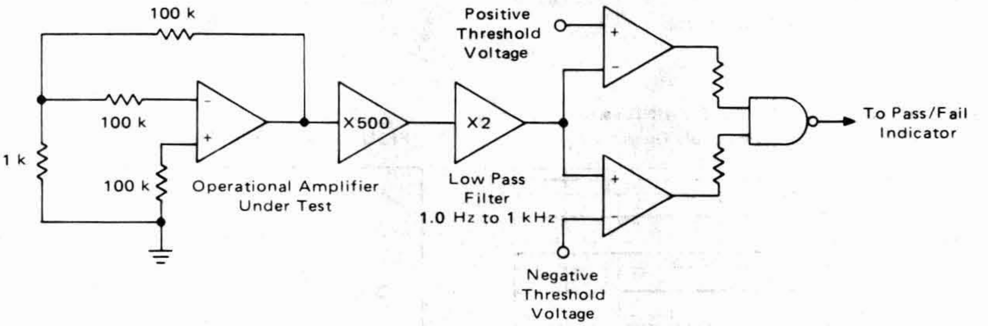


FIGURE 5 – BURST NOISE TEST CIRCUIT


100 k
100 k
1 k
100 k
Operational Amplifier
Under Test
X500
X2
Low Pass
Filter
1.0 Hz to 1 kHz
Positive
Threshold
Voltage
Negative
Threshold
Voltage
To Pass/Fail
Indicator

Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $V_{EE}$ = -15 Vdc, $T_A$ = +25°C unless otherwise noted)

FIGURE 6 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

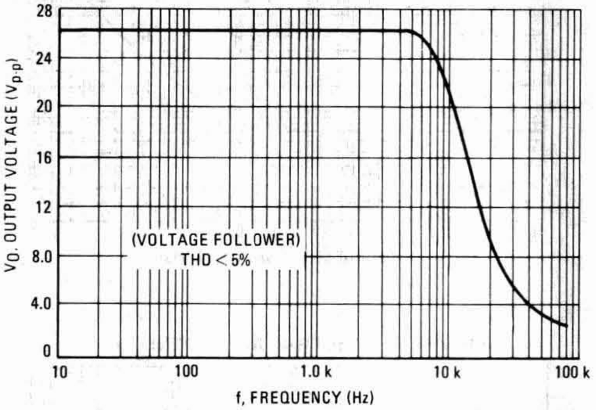


FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE

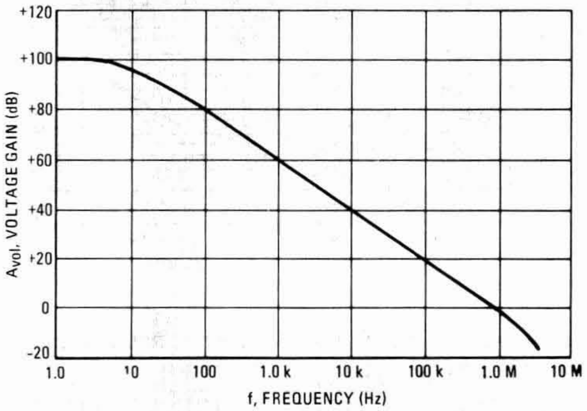


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

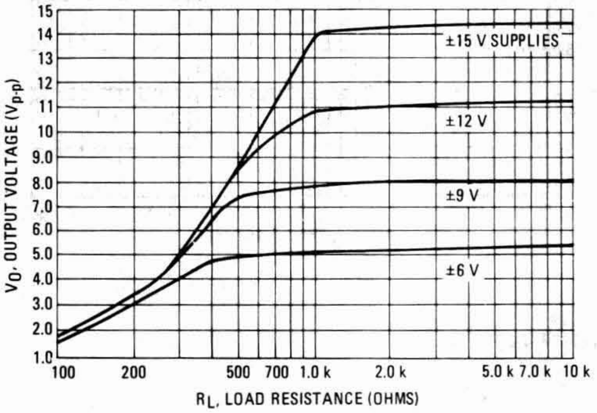


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

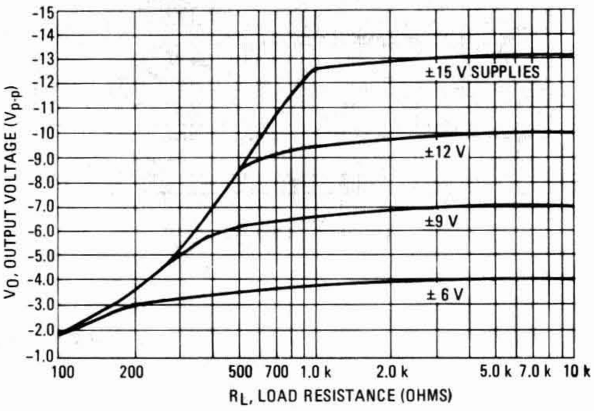


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

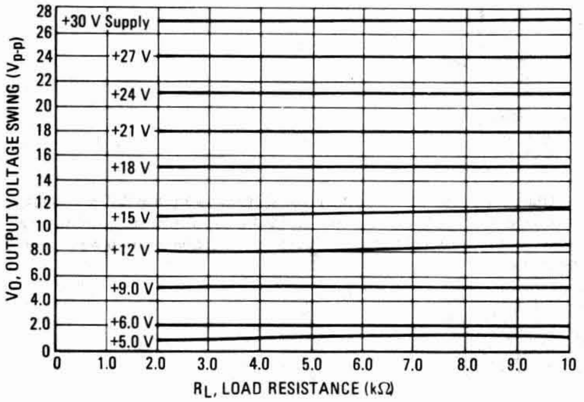


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER

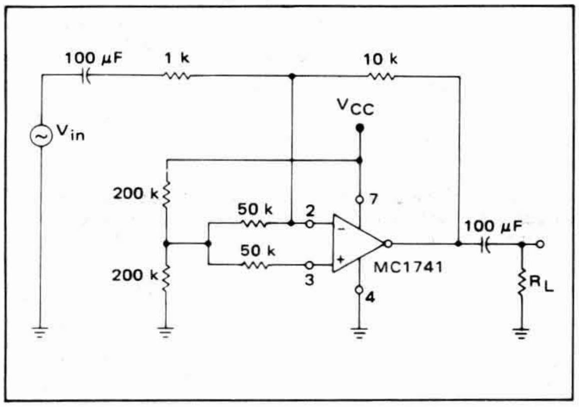

100 μF
1 k
10 k
$V_{in}$
$V_{CC}$
200 k
200 k
50 k
50 k
2
3
7
4
MC1741
100 μF
$R_L$

FIGURE 12 — NONINVERTING PULSE RESPONSE

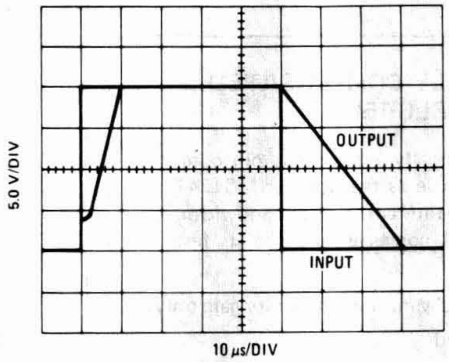


FIGURE 13 — TRANSIENT REPONSE TEST CIRCUIT

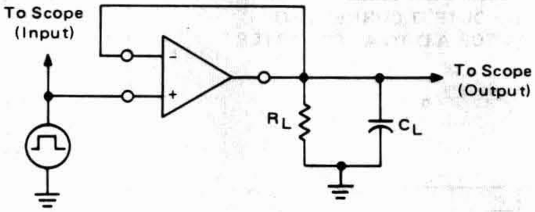
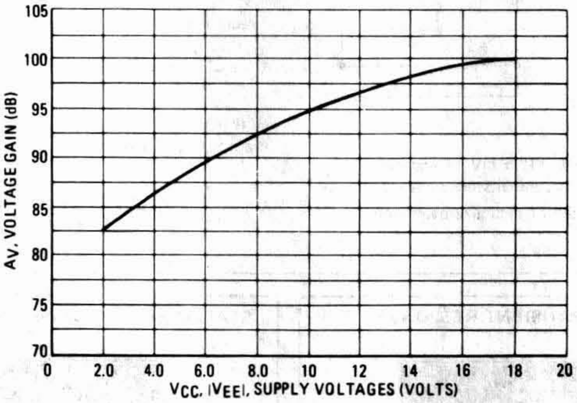

To Scope
(Input)
-
+
To Scope
(Output)
$R_L$
$C_L$

FIGURE 14 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1741SG | −55°C to +125°C | Metal Can |
| MC1741SCD | 0°C to +70°C | SO-8 |
| MC1741SCG | 0°C to +70°C | Metal Can |
| MC1741SCP1 | 0°C to +70°C | Plastic DIP |

# MC1741S
# MC1741SC

## HIGH SLEW-RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIER

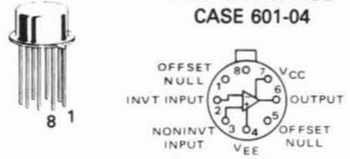
The MC1741S/MC1741SC is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1741 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D-to-A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/µs Guaranteed Minimum (for unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

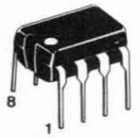
## OPERATIONAL AMPLIFIER

### SILICON MONOLITHIC INTEGRATED CIRCUIT

**G SUFFIX**
METAL PACKAGE
CASE 601-04

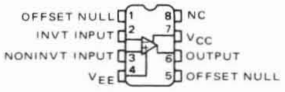

8
1
OFFSET NULL
INVT INPUT
NONINVT INPUT
$V_{EE}$
$V_{CC}$
OUTPUT
OFFSET NULL
1
2
3
4
5
6
7
8

(Top View)



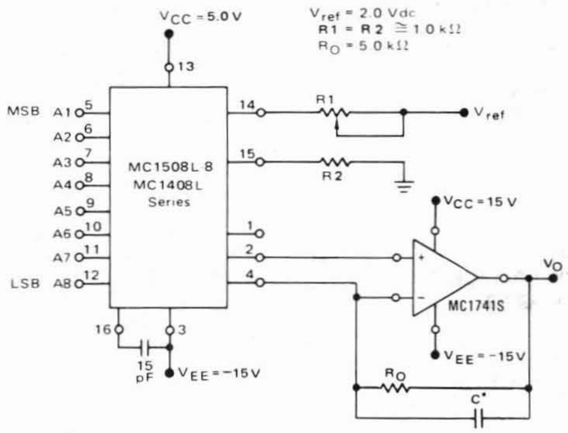
**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04

**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8


OFFSET NULL
INVT INPUT
NONINVT INPUT
$V_{EE}$
NC
$V_{CC}$
OUTPUT
OFFSET NULL
1
2
3
4
5
6
7
8

(Top View)

### TYPICAL APPLICATION OF OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER


$V_{CC}$ = 5.0 V
$V_{ref}$ = 2.0 Vdc
R1 = R2 ≅ 1.0 kΩ
$R_O$ = 5.0 kΩ
13
MSB
A1
A2
A3
A4
A5
A6
A7
LSB
A8
5
6
7
8
9
10
11
12
MC1508L-8
MC1408L
Series
14
15
1
2
4
R1
R2
$V_{ref}$
$V_{CC}$ = 15 V
MC1741S
$V_{EE}$ = −15 V
$V_O$
16
3
15 pF
$V_{EE}$ = −15 V
$R_O$
C*

Pins not shown are not connected.

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 µs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 150 pF).

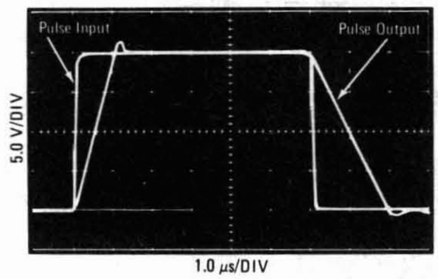
Theoretical $V_O$

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

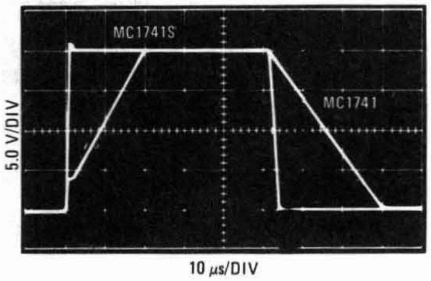
Adjust $V_{ref}$, R1 or $R_O$ so that $V_O$ with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

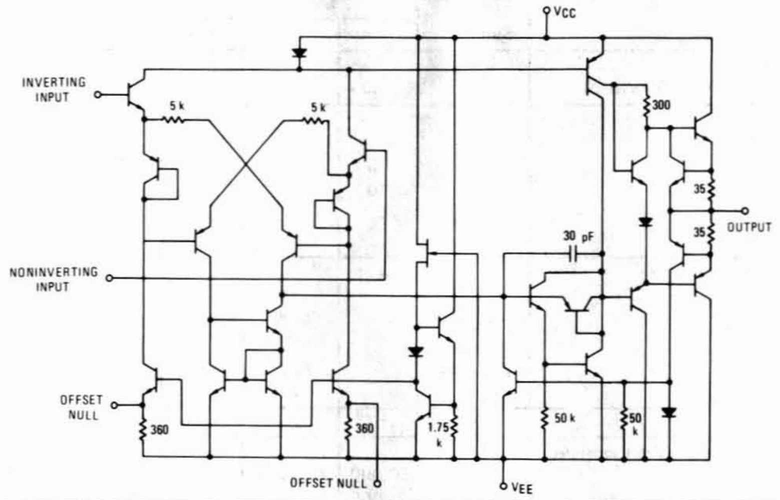
### MC1741S LARGE-SIGNAL TRANSIENT RESPONSE



### STANDARD MC1741 versus MC1741S RESPONSE COMPARISON



## CIRCUIT SCHEMATIC


VCC
INVERTING INPUT
5 k
5 k
300
35
OUTPUT
35
30 pF
NONINVERTING INPUT
OFFSET NULL
360
360
1.75 k
50 k
50 k
OFFSET NULL
VEE

## MAXIMUM RATINGS ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | MC1741SC | MC1741S | |
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>-18 | +22<br>-22 | Vdc |
| Differential Input Signal Voltage | $V_{ID}$ | ±30 | | Volts |
| Common-Mode Input Voltage Swing (See Note 1) | $V_{ICR}$ | ±15 | | Volts |
| Output Short-Circuit Duration (See Note 2) | $t_s$ | Continuous | | |
| Power Dissipation (Package Limitation)<br>Metal Package<br>Derate above $T_A$ = +25°C<br>Plastic Dual In-Line Package<br>Derate above $T_A$ = +25°C | $P_D$ | <br>680<br>4.6<br>625<br>5.0 | | <br>mW<br>mW/°C<br>mW<br>mW/°C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +75 | -55 to +125 | °C |
| Storage Temperature Range<br>Metal Package<br>Plastic Package | $T_{stg}$ | <br>-65 to +150<br>-55 to +125 | | °C |

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 Vdc.

FIGURE 1 – OFFSET ADJUST CIRCUIT

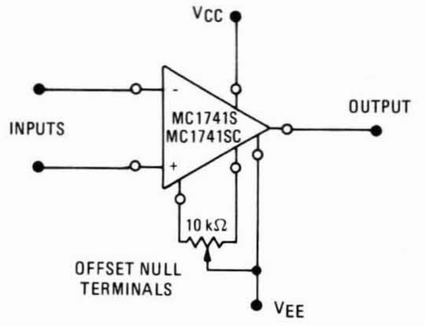
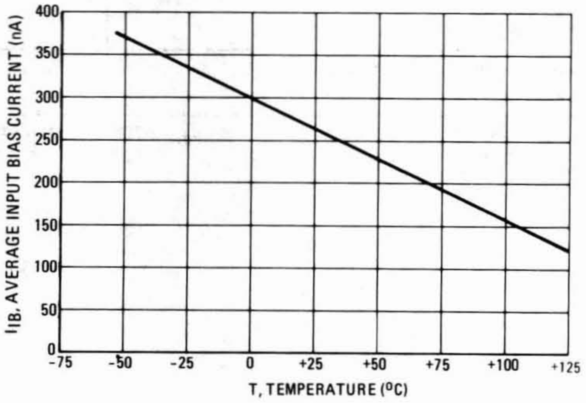

VCC
INPUTS
-
+
MC1741S
MC1741SC
OUTPUT
10 kΩ
OFFSET NULL TERMINALS
VEE

FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE



**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 Vdc, $V_{EE}$ = –15 Vdc, $T_A$ = +25°C unless otherwise noted.)

| Characteristic | Symbol | MC1741S | | | MC1741SC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Power Bandwidth (See Figure 3) | $BW_P$ | | | | | | | kHz |
| $A_v$ = 1, $R_L$ = 2.0 kΩ, THD = 5%, $V_O$ = 20 V(p-p) | | 150 | 200 | – | 150 | 200 | – | |
| Large-Signal Transient Response | | | | | | | | |
| Slew Rate (Figures 10 and 11) | SR | | | | | | | |
| V(–) to V(+) | | 10 | 20 | – | 10 | 20 | – | V/µs |
| V(+) to V(–) | | 10 | 12 | – | 10 | 12 | – | |
| Settling Time (Figures 10 and 11) (to within 0.1%) | $t_{setlg}$ | – | 3.0 | – | – | 3.0 | – | µs |
| Small-Signal Transient Response | | | | | | | | |
| (Gain = 1, $E_{in}$ = 20 mV, see Figures 7 and 8) | | | | | | | | |
| Rise Time | $t_{TLH}$ | – | 0.25 | – | – | 0.25 | – | µs |
| Fall Time | $t_{THL}$ | – | 0.25 | – | – | 0.25 | – | µs |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | – | 0.25 | – | – | 0.25 | – | µs |
| Overshoot | OS | – | 20 | – | – | 20 | – | % |
| Short-Circuit Output Currents | $I_{OS}$ | ±10 | – | ±35 | ±10 | – | ±35 | mA |
| Open-Loop Voltage Gain ($R_L$ = 2.0 kΩ) (See Figure 4) | $A_{vol}$ | | | | | | | – |
| $V_O$ = ±10 V, $T_A$ = +25°C | | 50,000 | 200,000 | – | 20,000 | 100,000 | – | |
| $V_O$ = ±10 V, $T_A$ = $T_{low}$* to $T_{high}$* | | 25,000 | – | – | 15,000 | – | – | |
| Output Impedance (f = 20 Hz) | $z_O$ | – | 75 | – | – | 75 | – | Ω |
| Input Impedance (f = 20 Hz) | $z_i$ | 0.3 | 1.0 | – | 0.3 | 1.0 | – | MΩ |
| Output Voltage Swing | $V_O$ | | | | | | | $V_{pk}$ |
| $R_L$ = 10 kΩ, $T_A$ = $T_{low}$ to $T_{high}$ (MC1741S only) | | ±12 | ±14 | – | ±12 | ±14 | – | |
| $R_L$ = 2.0 kΩ, $T_A$ = +25°C | | ±10 | ±13 | – | ±10 | ±13 | – | |
| $R_L$ = 2.0 kΩ, $T_A$ = $T_{low}$ to $T_{high}$ | | ±10 | – | – | ±10 | – | – | |
| Input Common-Mode Voltage Range | $V_{ICR}$ | ±12 | ±13 | – | ±12 | ±13 | – | $V_{pk}$ |
| $T_A$ = $T_{low}$ to $T_{high}$ (MC1741S) | | | | | | | | |
| Common-Mode Rejection Ratio (f = 20 Hz) | CMRR | 70 | 90 | – | 70 | 90 | – | dB |
| $T_A$ = $T_{low}$ to $T_{high}$ (MC1741S) | | | | | | | | |
| Input Bias Current (See Figure 2) | $I_{IB}$ | | | | | | | nA |
| $T_A$ = +25°C and $T_{high}$ | | – | 200 | 500 | – | 200 | 500 | |
| $T_A$ = $T_{low}$ | | – | 500 | 1500 | – | – | 800 | |
| Input Offset Current | $\|I_{IO}\|$ | | | | | | | nA |
| $T_A$ = +25°C and $T_{high}$ | | – | 30 | 200 | – | 30 | 200 | |
| $T_A$ = $T_{low}$ | | – | – | 500 | – | – | 300 | |
| Input Offset Voltage ($R_S$ = ≤ 10 kΩ) | $\|V_{IO}\|$ | | | | | | | mV |
| $T_A$ = +25°C | | – | 1.0 | 5.0 | – | 2.0 | 6.0 | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | – | – | 6.0 | – | – | 7.5 | |
| DC Power Consumption (See Figure 9) | $P_C$ | | | | | | | mW |
| (Power Supply = ±15 V, $V_O$ = 0) | | – | 50 | 85 | – | 50 | 85 | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | | | | | | | |
| Positive Voltage Supply Sensitivity | PSS+ | | | | | | | µV/V |
| ($V_{EE}$ constant) | | – | 2.0 | 100 | – | 2.0 | 150 | |
| $T_A$ = $T_{low}$ to $T_{high}$ on MC1741S | | | | | | | | |
| Negative Voltage Supply Sensitivity | PSS– | | | | | | | µV/V |
| ($V_{CC}$ constant) | | – | 10 | 150 | – | 10 | 150 | |

*$T_{low}$ = 0 for MC1741SC
= –55 °C for MC1741S

$T_{high}$ = +70°C for MC1741SC
= +125 °C for MC1741S

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $V_{EE}$ = -15 Vdc, $T_A$ = +25°C unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

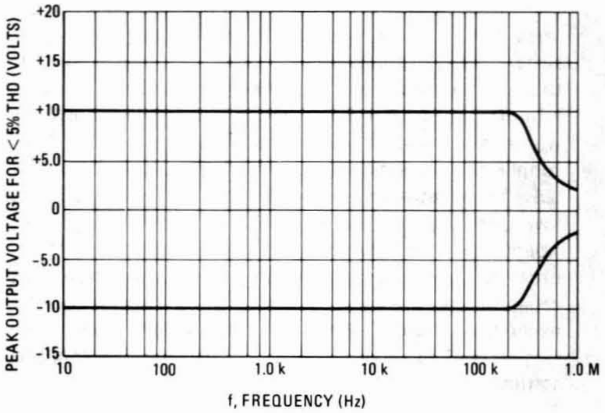


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

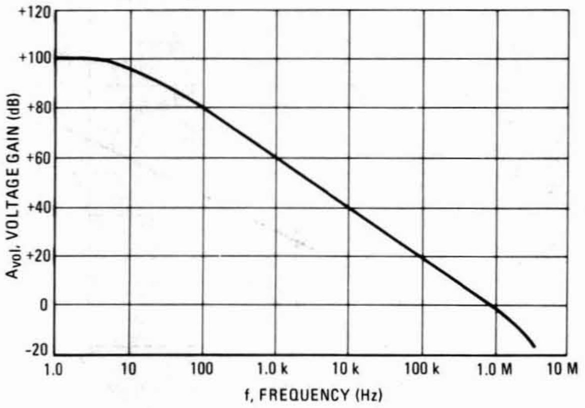


FIGURE 5 – NOISE versus FREQUENCY

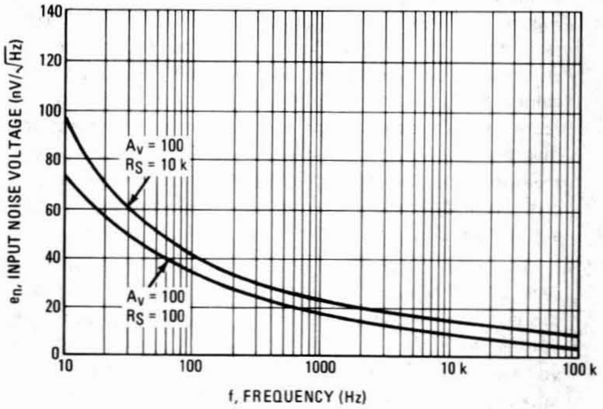


FIGURE 6 – OUTPUT NOISE versus SOURCE RESISTANCE

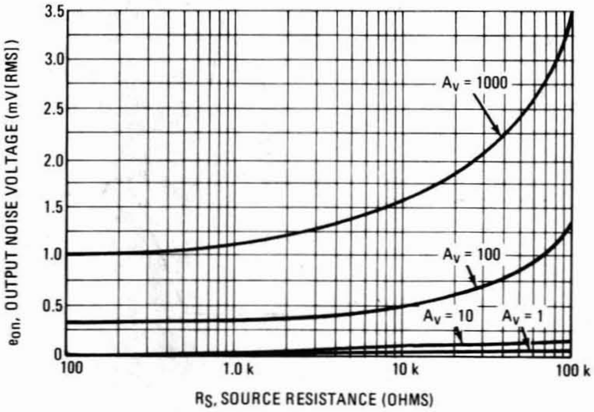


FIGURE 7 – SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

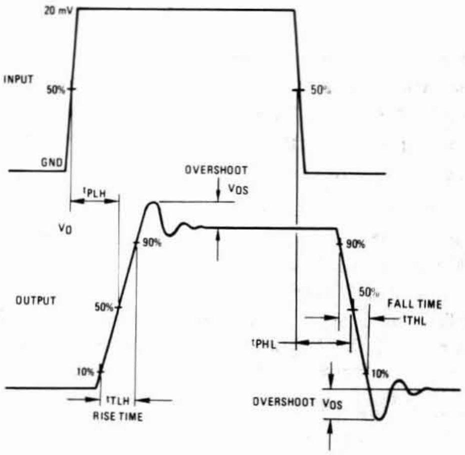
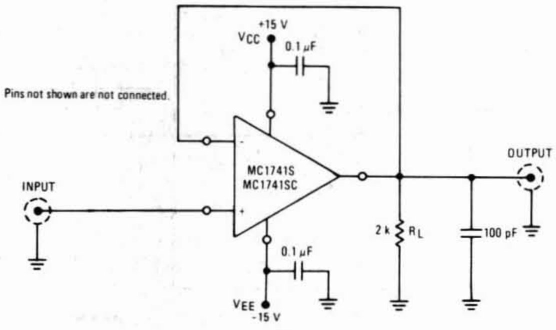

20 mV
INPUT
50%
50%
GND
OVERSHOOT
$V_{OS}$
$t_{PLH}$
$V_O$
90%
90%
OUTPUT
50%
50%
FALL TIME
$t_{THL}$
$t_{PHL}$
10%
10%
$t_{TLH}$
RISE TIME
OVERSHOOT $V_{OS}$

FIGURE 8 – SMALL-SIGNAL TRANSIENT RESPONSE TEST CIRCUIT


Pins not shown are not connected.
+15 V
$V_{CC}$
0.1 µF
-
+
MC1741S
MC1741SC
INPUT
OUTPUT
2 k
$R_L$
100 pF
0.1 µF
$V_{EE}$
-15 V

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C unless otherwise noted.)

**FIGURE 9 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGES**

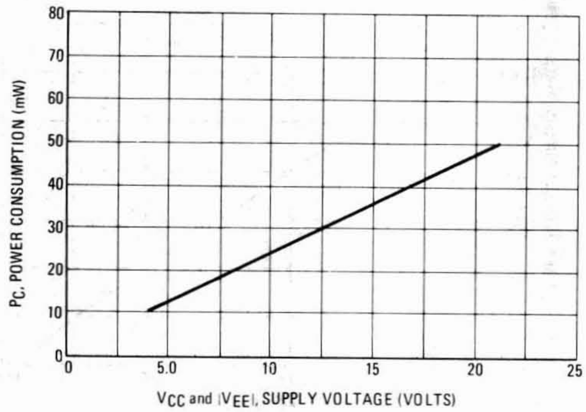


**FIGURE 10 – LARGE-SIGNAL TRANSIENT WAVEFORMS**

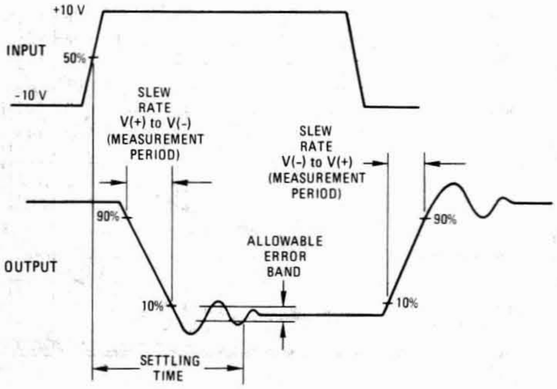
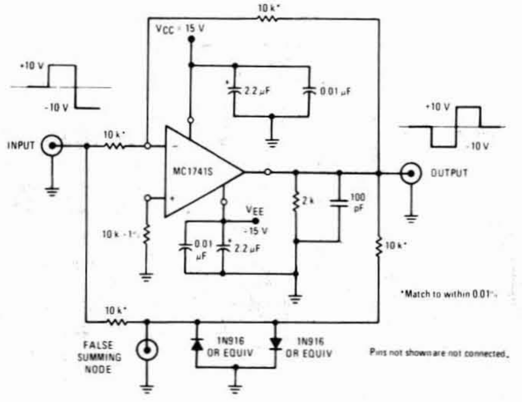

+10 V
INPUT
50%
-10 V
SLEW RATE V(+) to V(-) (MEASUREMENT PERIOD)
SLEW RATE V(-) to V(+) (MEASUREMENT PERIOD)
90%
OUTPUT
ALLOWABLE ERROR BAND
10%
90%
10%
SETTLING TIME

**FIGURE 11 – SETTLING TIME AND SLEW RATE TEST CIRCUIT**


10 k*
VCC = 15 V
+10 V
-10 V
2.2 µF
0.01 µF
+10 V
-10 V
INPUT
10 k*
MC1741S
OUTPUT
2 k
100 pF
VEE
-15 V
10 k - 1%
0.01 µF
2.2 µF
10 k*
*Match to within 0.01%
10 k*
FALSE SUMMING NODE
1N916 OR EQUIV
1N916 OR EQUIV
Pins not shown are not connected.

### SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

### SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

$t_{setlg}$ = observed settling time
x = amplifier settling time (to be determined)
y = false summing junction settling time
z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1741S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

FIGURE 12 – WAVEFORM AT FALSE SUMMING NODE

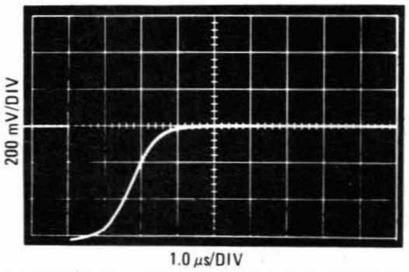
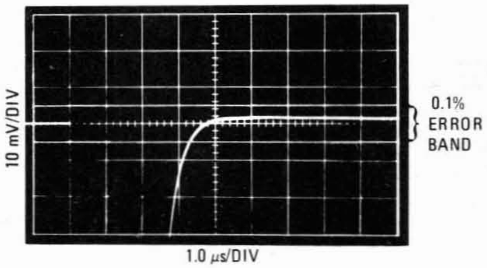
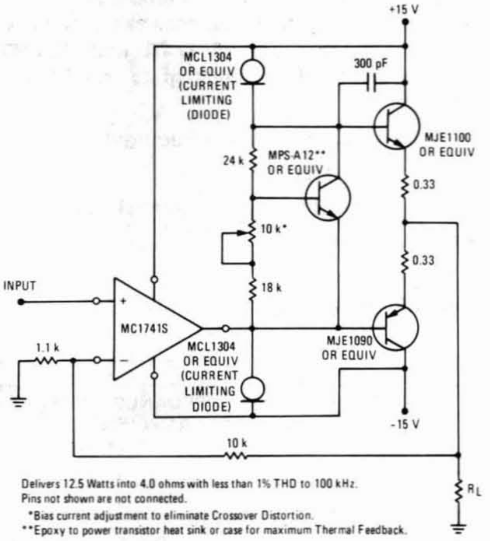


FIGURE 13 – EXPANDED WAVEFORM AT FALSE SUMMING NODE



## TYPICAL APPLICATION

FIGURE 14 – 12.5-WATT WIDEBAND POWER AMPLIFIER


+15 V
MCL1304 OR EQUIV (CURRENT LIMITING DIODE)
300 pF
MJE1100 OR EQUIV
24 k
MPS-A12** OR EQUIV
0.33
10 k*
0.33
18 k
INPUT
+
MC1741S
−
1.1 k
MCL1304 OR EQUIV (CURRENT LIMITING DIODE)
MJE1090 OR EQUIV
-15 V
10 k
R_L

Delivers 12.5 Watts into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.
*Bias current adjustment to eliminate Crossover Distortion.
**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1747G | −55°C to +125°C | Metal Can |
| MC1747L | −55°C to +125°C | Ceramic DIP |
| MC1747CD | 0°C to +70°C | SO-14 |
| MC1747CG | 0°C to +70°C | Metal Can |
| MC1747CL | 0°C to +70°C | Ceramic DIP |
| MC1747CP2 | 0°C to +70°C | Plastic DIP |

# MC1747
# MC1747C

## DUAL MC1741
## INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIER

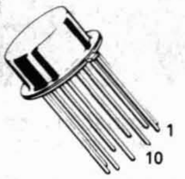
. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. The MC1747L and MC1747CL are functionally and electrically equivalent to the μA747 and μA747C respectively.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Offset Voltage Null Capability

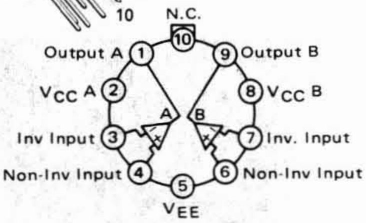
(DUAL MC1741)

DUAL
OPERATIONAL AMPLIFIER

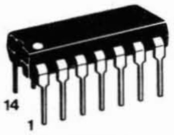
SILICON MONOLITHIC
INTEGRATED CIRCUIT



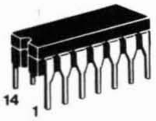
**G SUFFIX**
METAL PACKAGE
CASE 603-04
TO-100


10
N.C.
10
Output A 1
9 Output B
$V_{CC}$ A 2
8 $V_{CC}$ B
A
B
Inv Input 3
7 Inv. Input
Non-Inv Input 4
6 Non-Inv Input
5
$V_{EE}$

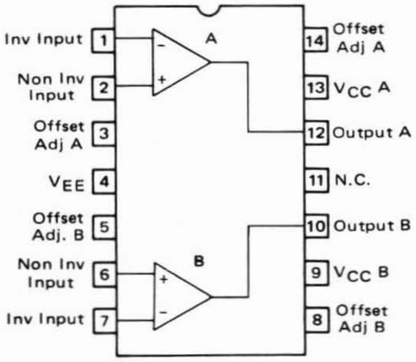
**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14



**P2 SUFFIX**
PLASTIC PACKAGE
CASE 646-05

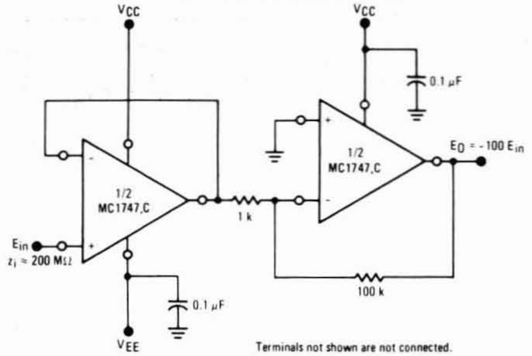


**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA


Inv Input 1
Non Inv Input 2
Offset Adj A 3
$V_{EE}$ 4
Offset Adj. B 5
Non Inv Input 6
Inv Input 7
14 Offset Adj A
13 $V_{CC}$ A
12 Output A
11 N.C.
10 Output B
9 $V_{CC}$ B
8 Offset Adj B
A
B
−
+
+
−

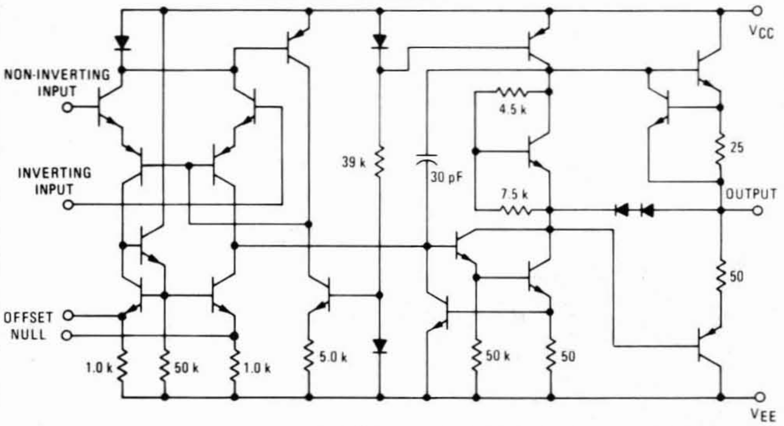
$V_{CC}A$ and $V_{CC}B$ are not connected internally.

FIGURE 1 — HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER


$V_{CC}$
$V_{CC}$
0.1 μF
$E_O = -100\ E_{in}$
1/2 MC1747,C
1/2 MC1747,C
1 k
$E_{in}$
$z_i \approx 200\ M\Omega$
100 k
0.1 μF
$V_{EE}$

Terminals not shown are not connected.

FIGURE 2 — CIRCUIT SCHEMATIC


NON-INVERTING INPUT
INVERTING INPUT
OFFSET NULL
1.0 k
50 k
1.0 k
5.0 k
39 k
30 pF
4.5 k
7.5 k
50 k
50
25
50
$V_{CC}$
OUTPUT
$V_{EE}$

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent right of Motorola Inc. or others.

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | MC1747 | MC1747C | Unit |
|---|---|---|---|---|
| Power Supply Voltages | $V_{CC}$<br>$V_{EE}$ | +22<br>-22 | +18<br>-18 | Vdc |
| Differential Input Signal Voltage ① | $V_{ID}$ | ± 30 | | Volts |
| Common-Mode Input Swing Voltage ② | $V_{ICR}$ | ± 15 | | Volts |
| Output Short-Circuit Duration | $t_{OS}$ | Continuous | | |
| Voltage (Measurement between Offset Null and $V_{EE}$) | | ± 0.5 | | Volts |
| Operating Ambient Temperature Range | $T_A$ | -55 to +125 | 0 to + 70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | -65 to +150 | °C |
| Junction Temperature | $T_J$ | | | °C |
| Ceramic and Metal Package | | 175 | | |
| Plastic Package | | 150 | | |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 Vdc, $V_{EE}$ = -15 Vdc, $T_A$ = +25°C unless otherwise noted.)

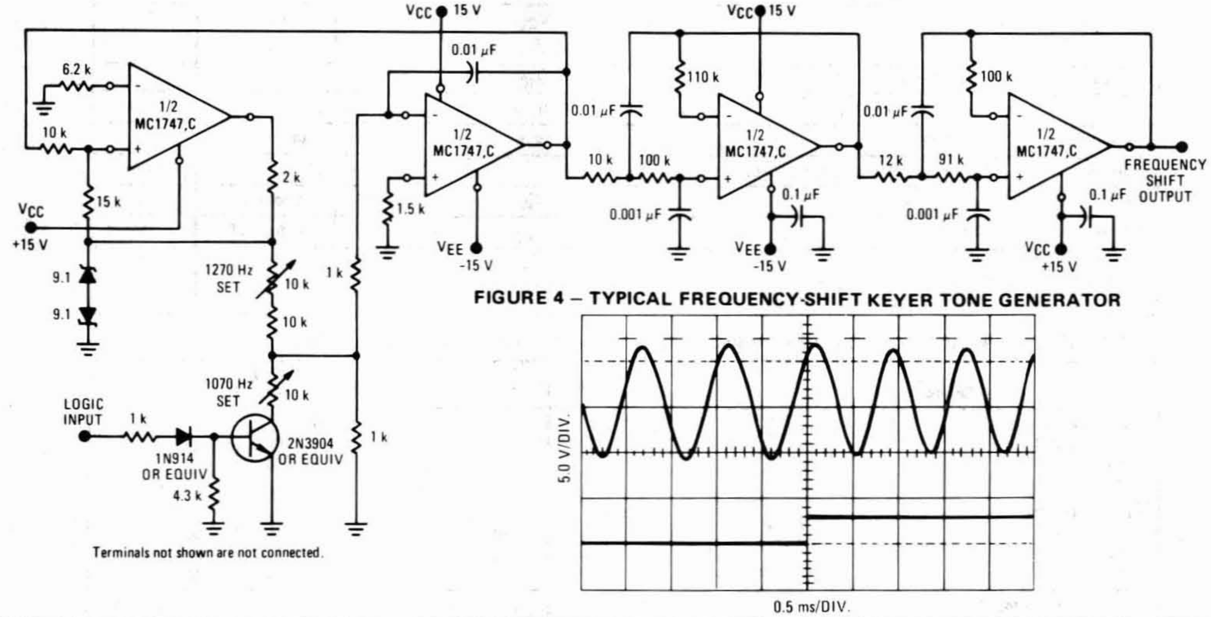
| Characteristics | Symbol | MC1747 | | | MC1747C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | $I_{IB}$ | | | | | | | nAdc |
| $T_A$ = +25°C | | – | 80 | 500 | – | 80 | 500 | |
| $T_A = T_{high}$ ③ | | – | 30 | 500 | – | 30 | 800 | |
| $T_A = T_{low}$ ③ | | – | 300 | 1500 | – | 30 | 800 | |
| Input Offset Current | $I_{IO}$ | | | | | | | nAdc |
| $T_A$ = +25°C | | – | 20 | 200 | – | 20 | 200 | |
| $T_A = T_{high}$ | | – | 7.0 | 200 | – | 7.0 | 300 | |
| $T_A = T_{low}$ | | – | 85 | 500 | – | 7.0 | 300 | |
| Input Offset Voltage ($R_S \leqslant 10$ kΩ) | $V_{IO}$ | | | | | | | mVdc |
| $T_A$ = +25°C | | – | 1.0 | 5.0 | – | 1.0 | 6.0 | |
| $T_A = T_{low}$ to $T_{high}$ | | – | 1.0 | 6.0 | – | 1.0 | 7.5 | |
| Offset Voltage Adjustment Range | | – | ± 15 | – | – | ± 15 | – | mV |
| Differential Input Impedance (Open-loop, f = 20 Hz) | | | | | | | | |
| Parallel Input Resistance | $r_i$ | 0.3 | 2.0 | – | 0.3 | 2.0 | – | MΩ |
| Parallel Input Capacitance | $c_i$ | – | 1.4 | – | – | 1.4 | – | pF |
| Common-Mode Input Voltage Swing | $V_{ICR}$ | | | | | | | Volts |
| $T_{low} \leqslant T_A \leqslant T_{high}$ | | ± 12 | ± 13 | – | ± 12 | ± 13 | – | |
| Common-Mode Rejection Ratio ($R_S$ = 10 kΩ) | CMRR | | | | | | | dB |
| $T_{low} \leqslant T_A \leqslant T_{high}$ | | 70 | 90 | – | 70 | 90 | – | |
| Open-Loop Voltage Gain | $A_{vol}$ | | | | | | | Volts |
| $T_A$ = +25°C ($V_O$ = ±10 V, $R_L$ = 2.0 kΩ) | | 50,000 | 200,000 | – | 25,000 | 200,000 | – | |
| $T_A = T_{low}$ to $T_{high}$ ($V_O$ = ±10 V, $R_L$ = 2.0 kΩ) | | 25,000 | – | – | 15,000 | – | – | |
| Transient Response (Unity Gain) ($V_{in}$ = 20 mV, $R_L$ = 2.0 kΩ, $C_L \leqslant 100$ pF) | | | | | | | | |
| Rise Time | $t_{PLH}$ | – | 0.3 | – | – | 0.3 | – | µs |
| Overshoot Percentage | | – | 5.0 | – | – | 5.0 | – | % |
| Slew Rate (Unity Gain) | SR | – | 0.5 | – | – | 0.5 | – | V/µs |
| Output Impedance | $z_o$ | – | 75 | – | – | 75 | – | ohms |
| Short-Circuit Output Current | $I_{OS}$ | – | 25 | – | – | 25 | – | mAdc |
| Channel Separation | | – | 120 | – | – | 120 | – | dB |
| Output Voltage Swing ($T_{low} \leqslant T_A \leqslant T_{high}$) | $V_{OR}$ | | | | | | | $V_{pk}$ |
| $R_L$ = 10 kΩ | | ± 12 | ± 14 | – | ± 12 | ± 14 | – | |
| $R_L$ = 2.0 kΩ | | ± 10 | ± 13 | – | ± 10 | ± 13 | – | |
| Power Supply Sensitivity ($T_{low}$ to $T_{high}$) | | | | | | | | µV/V |
| $V_{EE}$ = Constant, $R_S \leqslant 10$ kΩ | PSS+ | – | 30 | 150 | – | 30 | 150 | |
| $V_{CC}$ = Constant, $R_S \leqslant 10$ kΩ | PSS- | – | 30 | 150 | – | 30 | 150 | |
| Power Supply Current (each amplifier) | $I_{CC}, I_{EE}$ | | | | | | | mAdc |
| $T_A$ = +25°C | | – | 1.7 | 2.8 | – | 1.7 | 2.8 | |
| $T_A = T_{low}$ | | – | 2.0 | 3.3 | – | 2.0 | 3.3 | |
| $T_A = T_{high}$ | | – | 1.5 | 2.5 | – | 2.0 | 3.3 | |
| DC Power Consumption (each amplifier) | $P_C$ | | | | | | | mW |
| $T_A$ = +25°C | | – | 50 | 85 | – | 50 | 85 | |
| $T_A = T_{low}$ | | – | 60 | 100 | – | 60 | 100 | |
| $T_A = T_{high}$ | | – | 45 | 75 | – | 60 | 100 | |

① For supply voltages of less than ±15 V, the maximum differential input voltage is equal to ± ($V_{CC}$ + $|V_{EE}|$).

② For supply voltages of less than ±15 V, the maximum input voltage is equal to the supply voltage ($+V_{CC}$, $-|V_{EE}|$).

③ $T_{low}$ : 0°C for MC1747CL
−55°C for MC1747L
$T_{high}$: +70°C for MC1747CL
+125°C for MC1747L

### FIGURE 3 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR TEST CIRCUIT


VCC 15 V
0.01 µF
6.2 k
1/2 MC1747,C
10 k
15 k
VCC
+15 V
9.1
9.1
2 k
1270 Hz SET
10 k
10 k
1070 Hz SET
10 k
1 k
1 k
1 k
1.5 k
VEE -15 V
LOGIC INPUT
1 k
1N914 OR EQUIV
4.3 k
2N3904 OR EQUIV
0.01 µF
10 k
100 k
0.001 µF
110 k
VCC 15 V
1/2 MC1747,C
0.1 µF
VEE -15 V
0.01 µF
12 k
91 k
100 k
0.001 µF
1/2 MC1747,C
0.1 µF
VCC +15 V
FREQUENCY SHIFT OUTPUT

Terminals not shown are not connected.

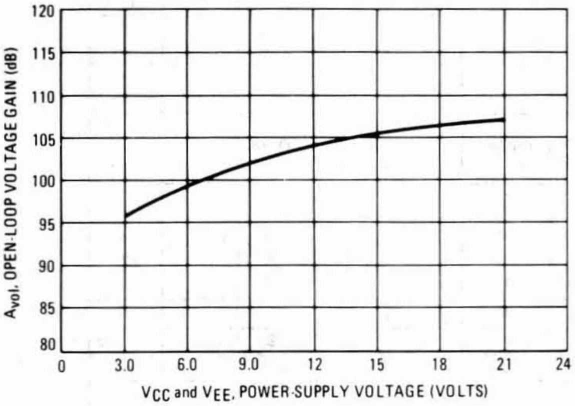
### FIGURE 4 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR

5.0 V/DIV.
0.5 ms/DIV.

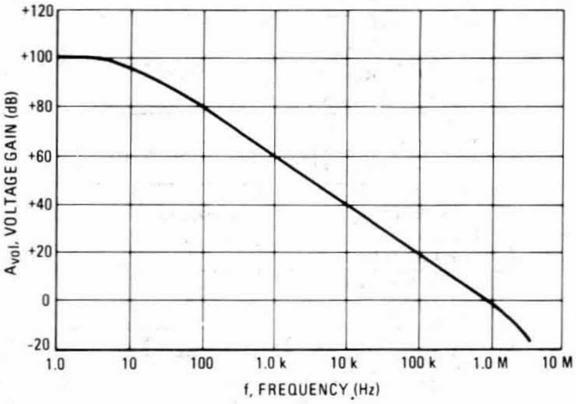
## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C unless otherwise noted.)

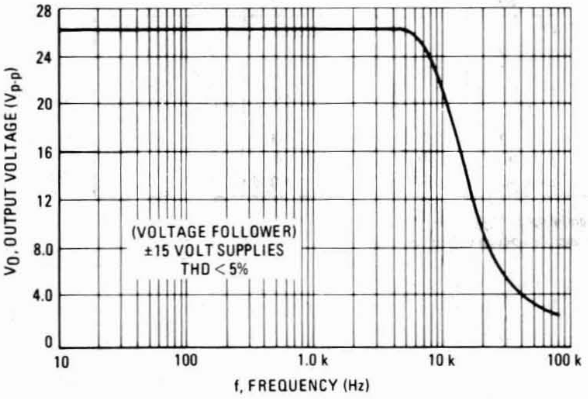
### FIGURE 5 – OPEN-LOOP VOLTAGE GAIN versus POWER-SUPPLY VOLTAGE



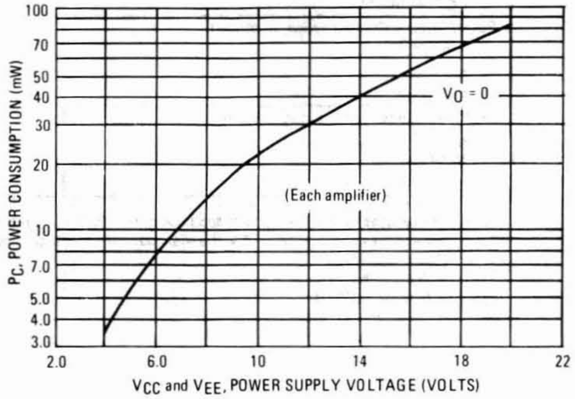
### FIGURE 6 – OPEN-LOOP FREQUENCY RESPONSE



### FIGURE 7 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)



### FIGURE 8 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



## TYPICAL CHARACTERISTICS (continued)

($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C unless otherwise noted.)

FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

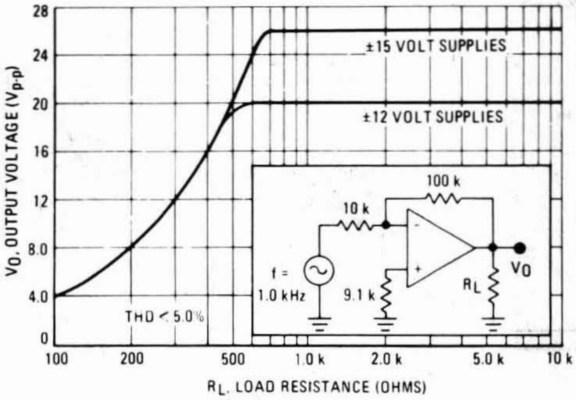
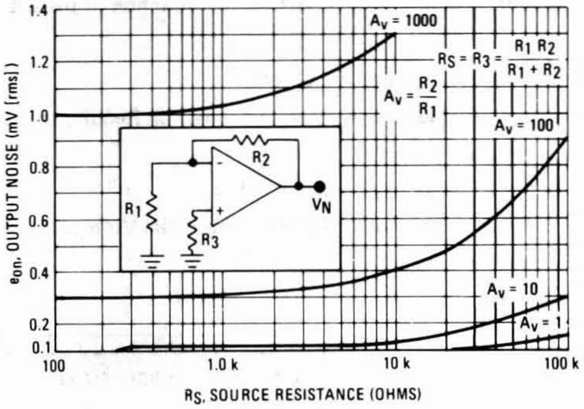


FIGURE 10 – OUTPUT NOISE versus SOURCE RESISTANCE



## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC1748G | −55°C to +125°C | Metal Can |
| MC1748U | −55°C to +125°C | Ceramic DIP |
| MC1748CG | 0°C to +70°C | Metal Can |
| MC1748CP1 | 0°C to +70°C | Plastic DIP |
| MC1748CU | 0°C to +70°C | Ceramic DIP |

# MC1748
# MC1748C

## HIGH PERFORMANCE OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

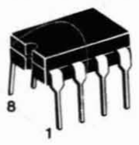
- Noncompensated MC1741
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

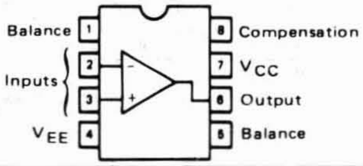
## OPERATIONAL AMPLIFIER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(MC1748C only)

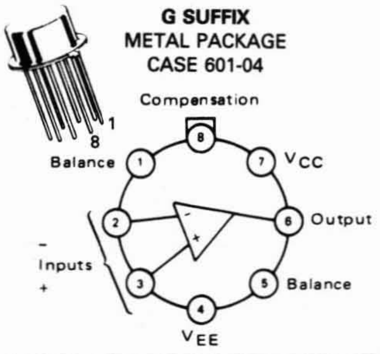
**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02





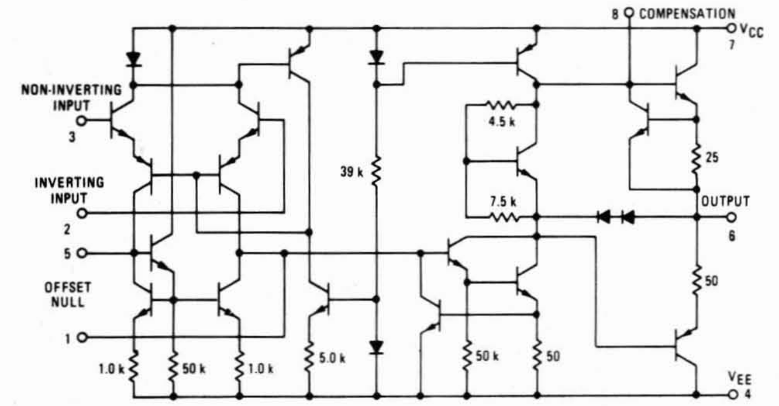
Balance 1
Inputs
2 −
3 +
VEE 4
8 Compensation
7 VCC
6 Output
5 Balance

**G SUFFIX**
METAL PACKAGE
CASE 601-04



1
8
Compensation
8
Balance 1
7 VCC
2
6 Output
−
Inputs
+
3
5 Balance
4
VEE

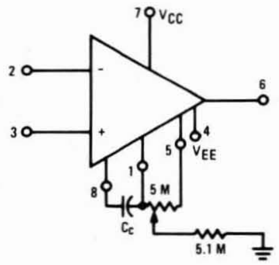
**FIGURE 1 – CIRCUIT SCHEMATIC**



8 COMPENSATION
VCC
7
NON-INVERTING INPUT
3
INVERTING INPUT
2
5
OFFSET NULL
1
4.5 k
39 k
7.5 k
25
OUTPUT
6
50
1.0 k
50 k
1.0 k
5.0 k
50 k
50
VEE
4

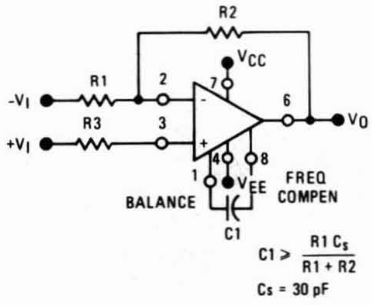
## TYPICAL COMPENSATION CIRCUITS

**FIGURE 2 – OFFSET ADJUST AND FREQUENCY COMPENSATION**



7 VCC
2
3
−
+
6
4
5 VEE
1
8
5 M
Cc
5.1 M

**FIGURE 3 – SINGLE-POLE COMPENSATION**

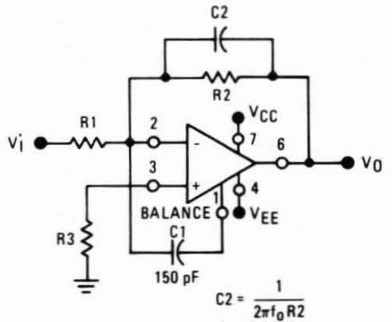


R2
VCC
R1
2
7
6
−VI
R3
3
VO
+VI
−
+
4
8
1
VEE
FREQ COMPEN
BALANCE
C1

$C1 > \frac{R1\,C_s}{R1 + R2}$

$C_s = 30$ pF

**FIGURE 4 – FEEDFORWARD COMPENSATION**



C2
R2
VCC
R1
2
7
6
VI
−
+
3
VO
1
4
BALANCE
VEE
C1
R3
150 pF

$C2 = \frac{1}{2\pi f_0 R2}$

$f_0 = 3.0$ MHz

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | MC1748 | MC1748C | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +22<br>-22 | +18<br>-18 | Vdc |
| Differential Input Signal | $V_{in}$ | ±30 | | Volts |
| Common-Mode Input Swing ① | $V_{ICR}$ | ±15 | | Volts |
| Output Short Circuit Duration | $t_s$ | Continuous | | |
| Power Dissipation (Package Limitation)<br>Derate above $T_A$ = +25°C | $P_D$ | 680<br>4.6 | | mW<br>mW/°C |
| Operating Temperature Range | $T_A$ | -55 to +125 | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 Vdc, $V_{EE}$ = -15 Vdc, $T_A$ = +25°C unless otherwise noted.)

| Characteristics | Symbol | MC1748 | | | MC1748C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | $I_{IB}$ | | | | | | | µAdc |
| $T_A$ = +25°C | | – | 0.08 | 0.5 | – | 0.08 | 0.5 | |
| $T_A$ = $T_{low}$ to $T_{high}$ ② | | – | 0.3 | 1.5 | – | – | 0.8 | |
| Input Offset Current | $\|I_{IO}\|$ | | | | | | | µAdc |
| $T_A$ = +25°C | | – | 0.02 | 0.2 | – | 0.02 | 0.2 | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | – | 0.08 | 0.5 | – | – | 0.3 | |
| Input Offset Voltage ($R_S \le$ 10 k Ω) | $\|V_{IO}\|$ | | | | | | | mVdc |
| $T_A$ = +25°C | | – | 1.0 | 5.0 | – | 1.0 | 6.0 | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | – | – | 6.0 | – | – | 7.5 | |
| Differential Input Impedance (Open-Loop, f = 20 Hz) | | | | | | | | |
| Parallel Input Resistance | $R_p$ | 0.3 | 2.0 | – | 0.3 | 2.0 | – | Megohm |
| Parallel Input Capacitance | $C_p$ | – | 1.4 | – | – | 1.4 | – | pF |
| Common-Mode Input Impedance (f 20 Hz) | $z_{in}$ | – | 200 | – | – | 200 | | Megohms |
| Common-Mode Input Voltage Swing | $V_{ICR}$ | ±12 | ±13 | – | ±12 | ±13 | – | $V_{pk}$ |
| Common-Mode Rejection Ratio (f = 100 Hz) | CMRR | 70 | 90 | – | 70 | 90 | – | dB |
| Open-Loop Voltage Gain, ($V_o$ = ±10 V, $R_L$ = 2.0 k ohms) | $A_{vol}$ | | | | | | | V/V |
| $T_A$ = +25°C | | 50,000 | 200,000 | – | 20,000 | 200,000 | – | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | 25,000 | – | – | 15,000 | – | – | |
| Step Response ($V_{in}$ = 20 mV, $C_c$ = 30 pF, $R_L$ = 2 kΩ, $C_L$ = 100 pF) | | | | | | | | |
| Rise Time | $t_r$ | – | 0.3 | – | – | 0.3 | – | µs |
| Overshoot Percentage | | – | 5.0 | – | – | 5.0 | – | % |
| Slew Rate | $dV_{out}/dt$ | – | 0.8 | – | – | 0.8 | – | V/µs |
| Output Impedance (f = 20 Hz) | $z_o$ | – | 75 | – | – | 75 | – | ohms |
| Short-Circuit Output Current | $I_{sc}$ | – | 25 | – | – | 25 | – | mAdc |
| Output Voltage Swing ($R_L$ = 10 k ohms) | $V_O$ | ±12 | ±14 | – | ±12 | ±14 | – | Vpk |
| $R_L$ = 2 k ohms ($T_A$ = $T_{low}$ to $t_{high}$) | | ±10 | ±13 | – | ±10 | ±13 | – | |
| Power Supply Sensitivity | | | | | | | | µV/V |
| $V_{EE}$ = constant, $R_s \leqslant$ 10 k ohms | S+ | – | 30 | 150 | – | 30 | 150 | |
| $V_{CC}$ = constant, $R_s \leqslant$ 10 k ohms | S- | – | 30 | 150 | – | 30 | 150 | |
| Power Supply Current | $I_D^+$ | – | 1.67 | 2.83 | – | 1.67 | 2.83 | mAdc |
| | $I_D^-$ | – | 1.67 | 2.83 | – | 1.67 | 2.83 | |
| DC Quiescent Power Dissipation ($V_o$ = 0) | $P_D$ | – | 50 | 85 | – | 50 | 85 | mW |

① For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage.

② $T_{low}$: 0°C for MC1748C
-55°C for MC1748
$T_{high}$: +70° for MC1748C
+125°C for MC1748

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C unless otherwise noted.)

FIGURE 5 – MINIMUM INPUT VOLTAGE RANGE

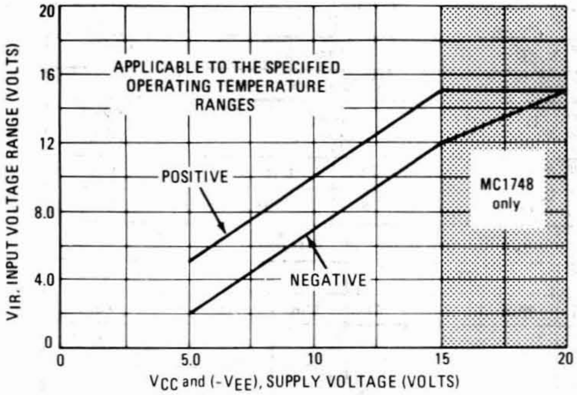


FIGURE 6 – MINIMUM OUTPUT VOLTAGE SWING

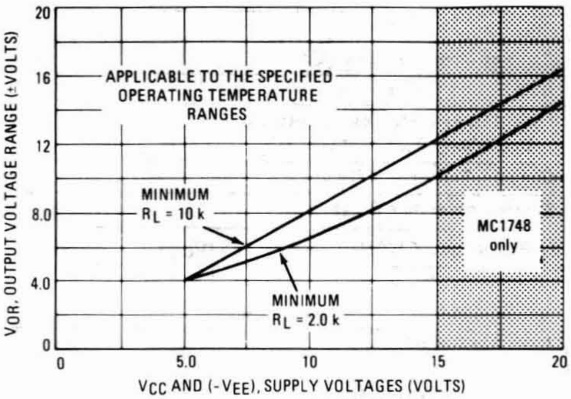


FIGURE 7 – MINIMUM VOLTAGE GAIN

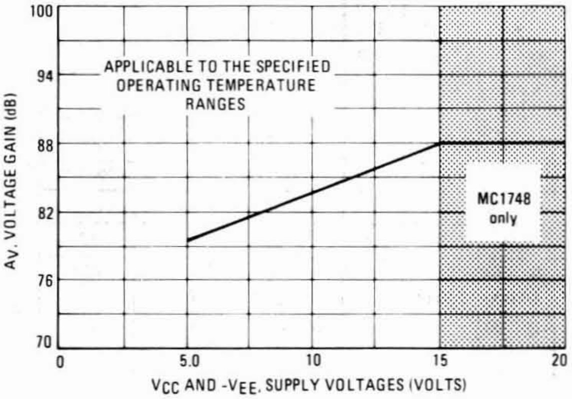


FIGURE 8 – TYPICAL SUPPLY CURRENTS

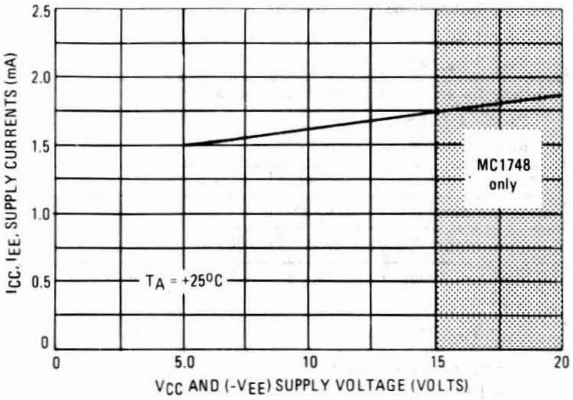


FIGURE 9 – OPEN-LOOP FREQUENCY RESPONSE

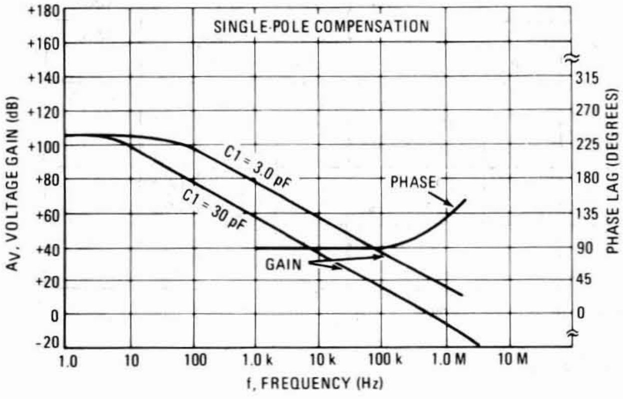
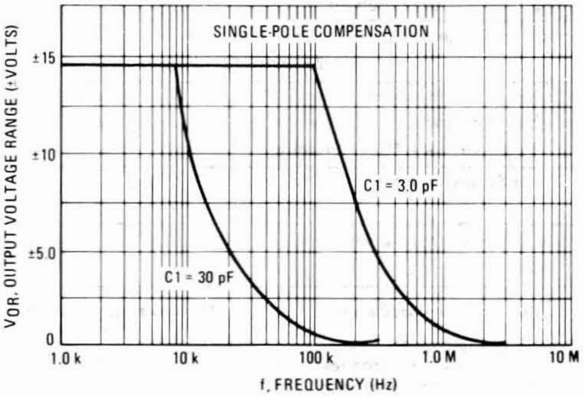


FIGURE 10 – LARGE-SIGNAL FREQUENCY RESPONSE



## TYPICAL CHARACTERISTICS (continued)

($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C unless otherwise noted.)

FIGURE 11 – VOLTAGE FOLLOWER PULSE RESPONSE

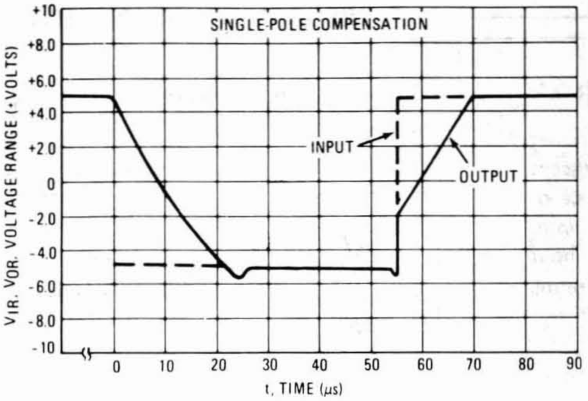


FIGURE 12 – OPEN-LOOP FREQUENCY RESPONSE

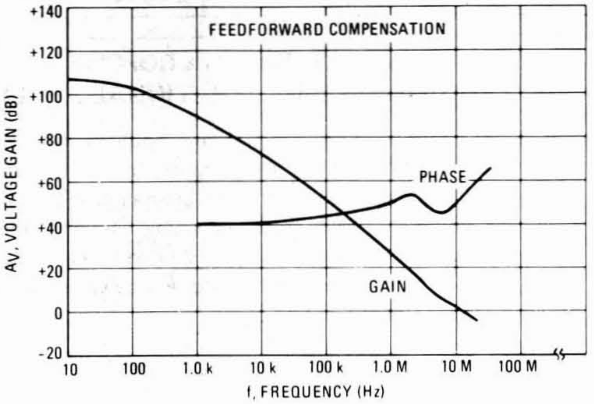


FIGURE 13 – LARGE-SIGNAL FREQUENCY RESPONSE

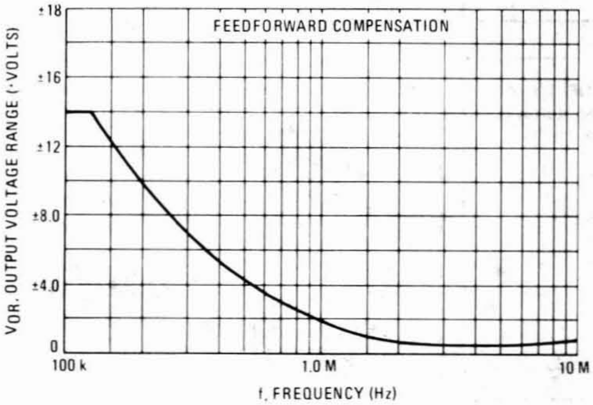
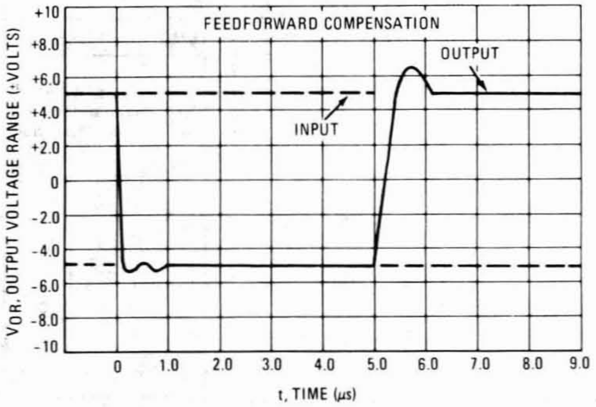


FIGURE 14 – INVERTER PULSE RESPONSE



**MOTOROLA**

# MC1776
# MC1776C

## Specifications and Applications Information

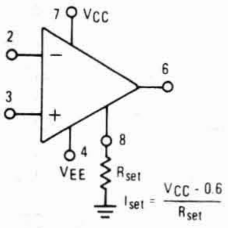
### MONOLITHIC MICROPOWER PROGRAMMABLE OPERATIONAL AMPLIFIER

This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the $I_{set}$ input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ±1.2 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

### RESISTIVE PROGRAMMING (See Figure 1.)

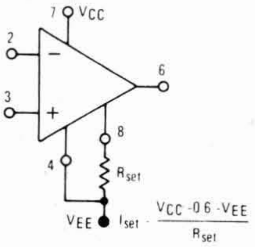
**$R_{set}$ to GROUND**


7
VCC
2
3
6
4
VEE
8
Rset
Iset = (VCC - 0.6)/Rset

| Typical $R_{set}$ Values | | |
|---|---|---|
| $V_{CC}$, $V_{EE}$ | $I_{set}$ = 1.5 μA | $I_{set}$ = 15 μA |
| ±6.0V | 3.6 MΩ | 360 kΩ |
| ±10V | 6.2 MΩ | 620 kΩ |
| ±12V | 7.5 MΩ | 750 kΩ |
| ±15V | 10 MΩ | 1.0 MΩ |

**$R_{set}$ to NEGATIVE SUPPLY**

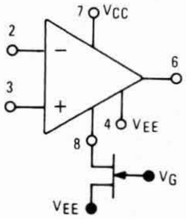
(Recommended for supply voltage less than ±6.0 V)


7
VCC
2
3
6
8
4
Rset
VEE
Iset = (VCC - 0.6 - VEE)/Rset

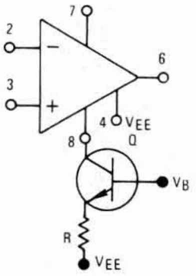
| Typical $R_{set}$ Values | | |
|---|---|---|
| $V_{CC}$, $V_{EE}$ | $I_{set}$ = 1.5 μA | $I_{set}$ = 15 μA |
| ±1.5V | 1.6 MΩ | 160 kΩ |
| ±3.0V | 3.6 MΩ | 360 kΩ |
| ±6.0V | 7.5 MΩ | 750 kΩ |
| ±15 V | 20 MΩ | 2.0 MΩ |

### ACTIVE PROGRAMMING

**FET CURRENT SOURCE**


7
VCC
2
3
6
4
VEE
8
VG
VEE

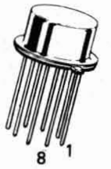
**BIPOLAR CURRENT SOURCE**


7
2
3
6
4
VEE
8
Q
VB
R
VEE

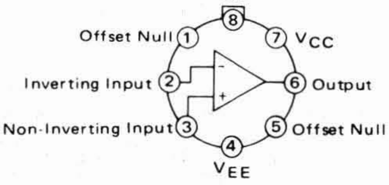
Pins not shown are not connected.

### PROGRAMMABLE OPERATIONAL AMPLIFIER

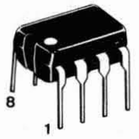
**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**G SUFFIX**
METAL PACKAGE
CASE 601-04

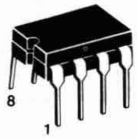

Iset
8
Offset Null 1
7 VCC
Inverting Input 2
6 Output
Non-Inverting Input 3
5 Offset Null
4
VEE

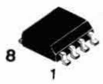
(Top View)



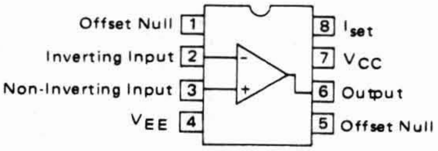
**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(MC1776C only)

**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02





**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8


Offset Null 1
Inverting Input 2
Non-Inverting Input 3
VEE 4
8 Iset
7 VCC
6 Output
5 Offset Null

(Top View)

**ORDERING INFORMATION**

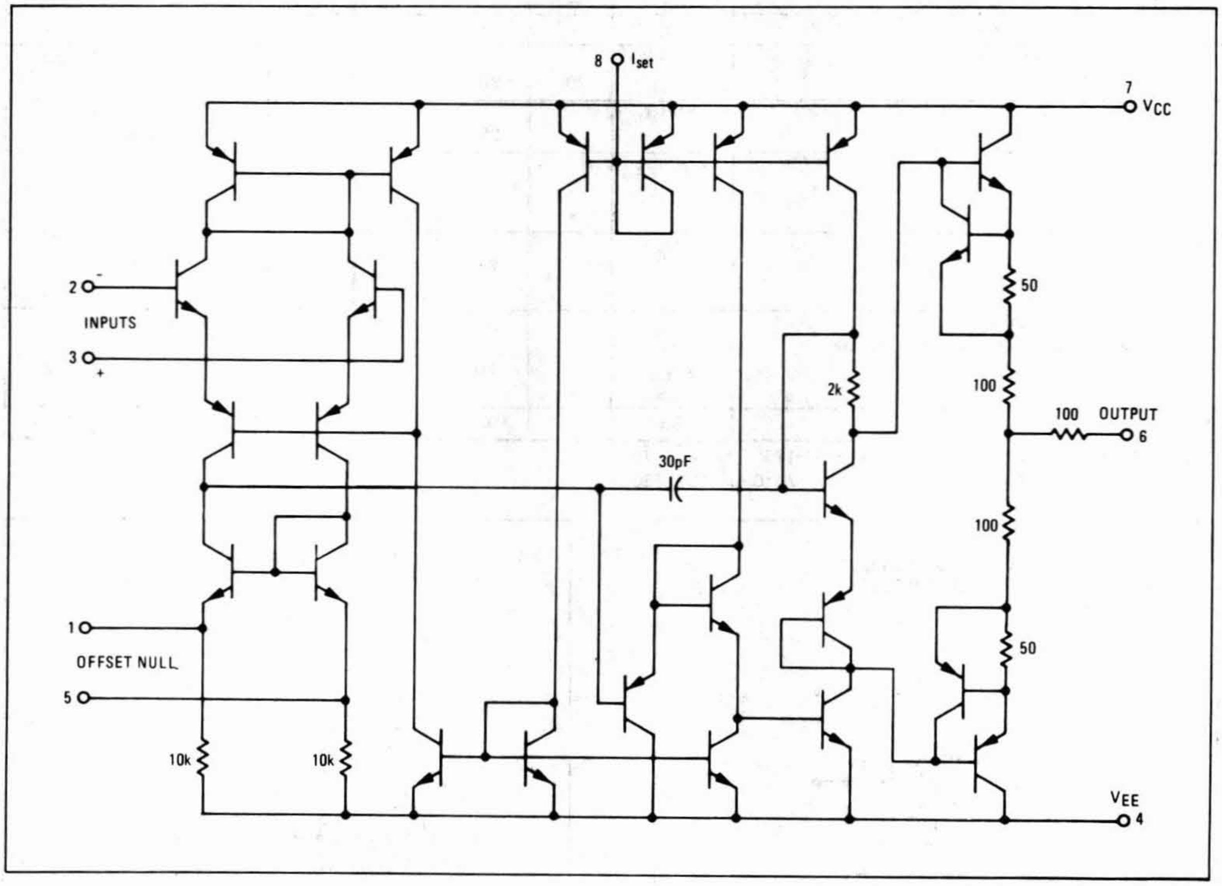
| Device | Temperature Range | Package |
|---|---|---|
| MC1776G | −55 to +125°C | Metal Can |
| MC1776U | | Ceramic DIP |
| MC1776CD | 0 to +70°C | SO-8 |
| MC1776CG | | Metal Can |
| MC1776CP1 | | Plastic DIP |
| MC1776CU | | Ceramic DIP |

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltages | $V_{CC}, V_{EE}$ | ± 18 | Vdc |
| Differential Input Voltage | $V_{ID}$ | ± 30 | Vdc |
| Common-Mode Input Voltage<br>$V_{CC}$ and $\lvert V_{EE} \rvert < 15$ V<br>$V_{CC}$ and $\lvert V_{EE} \rvert \geq 15$ V | $V_{ICM}$ | <br>$V_{CC}, V_{EE}$<br>± 15 | Vdc |
| Offset Null to $V_{EE}$ Voltage | $V_{off}-V_{EE}$ | ± 0.5 | Vdc |
| Programming Current | $I_{set}$ | 500 | μA |
| Programming Voltage<br>(Voltage from $I_{set}$ terminal to ground) | $V_{set}$ | ($V_{CC}$ -2.0 V)<br>to<br>$V_{CC}$ | Vdc |
| Output Short-Circuit Duration* | $t_s$ | Indefinite | s |
| Operating Temperature Range<br>MC1776<br>MC1776C | $T_A$ | <br>-55 to +125<br>0 to +70 | °C |
| Storage Temperature Range<br>Metal and Ceramic Packages<br>Plastic Package | $T_{stg}$ | <br>-65 to +150<br>-55 to +125 | °C |
| Junction Temperature<br>Metal and Ceramic Packages<br>Plastic Package | $T_J$ | <br>175<br>150 | °C |

*May be to ground or either Supply Voltage. Rating applies up to a case temperature of +125°C or ambient temperature of +70°C and $I_{set} \leq 30$ μA.

**SCHEMATIC DIAGRAM**

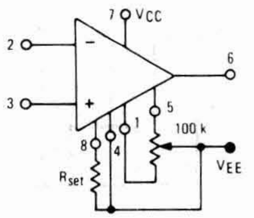


**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +3.0 V, $V_{EE}$ = −3.0 V, $I_{set}$ = 1.5 μA, $T_A$ = +25°C unless otherwise noted.)

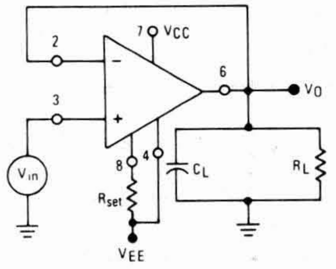
| Characteristic | Symbol | MC1776 Min | MC1776 Typ | MC1776 Max | MC1776C Min | MC1776C Typ | MC1776C Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage ($R_S \leqslant$ 10 kΩ) | $V_{IO}$ | | | | | | | mV |
| $T_A$ = +25°C | | – | 2.0 | 5.0 | – | 2.0 | 6.0 | |
| $T_{low}$* $\leqslant T_A \leqslant T_{high}$* | | – | – | 6.0 | – | – | 7.5 | |
| Offset Voltage Adjustment Range | $V_{IOR}$ | – | 9.0 | – | – | 9.0 | – | mV |
| Input Offset Current | $I_{IO}$ | | | | | | | nA |
| $T_A$ = +25°C | | – | 0.7 | 3.0 | – | 0.7 | 6.0 | |
| $T_A = T_{high}$ | | – | – | 5.0 | – | – | 6.0 | |
| $T_A = T_{low}$ | | – | – | 10 | – | – | 10 | |
| Input Bias Current | $I_{IB}$ | | | | | | | nA |
| $T_A$ = +25°C | | – | 2.0 | 7.5 | – | 2.0 | 10 | |
| $T_A = T_{high}$ | | – | – | 7.5 | – | – | 10 | |
| $T_A = T_{low}$ | | – | – | 20 | – | – | 20 | |
| Input Resistance | $r_i$ | – | 50 | – | – | 50 | – | MΩ |
| Input Capacitance | $c_i$ | – | 2.0 | – | – | 2.0 | – | pF |
| Input Voltage Range | $V_{ID}$ | | | | | | | V |
| $T_{low} \leqslant T_A \leqslant T_{high}$ | | ±1.0 | – | – | ±1.0 | – | – | |
| Large Signal Voltage Gain | $A_{VOL}$ | | | | | | | V/V |
| $R_L \geqslant$ 75 kΩ, $V_O$ = ±1.0 V, $T_A$ = +25°C | | 50 k | 200 k | – | 25 k | 200 k | – | |
| $R_L \geqslant$ 75 kΩ, $V_O$ = ±1.0 V, $T_{low} \leqslant T_A \leqslant T_{high}$ | | 25 k | – | – | 25 k | – | – | |
| Output Voltage Swing | $V_O$ | | | | | | | V |
| $R_L \geqslant$ 75 kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$ | | ±2.0 | ±2.4 | – | ±2.0 | ±2.4 | – | |
| Output Resistance | $r_o$ | – | 5.0 | – | – | 5.0 | – | kΩ |
| Output Short-Circuit Current | $I_{os}$ | – | 3.0 | – | – | 3.0 | – | mA |
| Common-Mode Rejection Ratio | CMRR | | | | | | | dB |
| $R_S \leqslant$ 10 kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$ | | 70 | 86 | – | 70 | 86 | – | |
| Supply Voltage Rejection Ratio | PSRR | | | | | | | μV/V |
| $R_S \leqslant$ 10 kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$ | | – | 25 | 150 | – | 25 | 200 | |
| Supply Current | $I_{CC}$, $I_{EE}$ | | | | | | | μA |
| $T_A$ = +25°C | | – | 13 | 20 | – | 13 | 20 | |
| $T_{low} \leqslant T_A \leqslant T_{high}$ | | – | – | 25 | – | – | 25 | |
| Power Dissipation | $P_D$ | | | | | | | μW |
| $T_A$ = +25°C | | – | 78 | 120 | – | 78 | 120 | |
| $T_{low} \leqslant T_A \leqslant T_{high}$ | | – | – | 150 | – | – | 150 | |
| Transient Response (Unity Gain) | | | | | | | | |
| $V_{in}$ = 20 mV, $R_L \geqslant$ 5.0 kΩ, $C_L$ = 100 pF | | | | | | | | |
| Rise Time | $t_{TLH}$ | – | 3.0 | – | – | 3.0 | – | μs |
| Overshoot | OS | – | 0 | – | – | 0 | – | % |
| Slew Rate ($R_L \geqslant$ 5.0 kΩ) | $S_R$ | – | 0.03 | – | – | 0.03 | – | V/μs |

*$T_{low}$ = −55°C for MC1776 — $T_{high}$ = +125°C for MC1776
0°C for MC1776C — +70°C for MC1776C

**VOLTAGE OFFSET NULL CIRCUIT**



**TRANSIENT-RESPONSE TEST CIRCUIT**



Pins not shown are not connected.

**ELECTRICAL CHARACTERISTICS** ($V_{CC} = +3.0$ V, $V_{EE} = -3.0$ V, $I_{set} = 15$ μA, $T_A = +25^\circ C$ unless otherwise noted.)

| Characteristic | Symbol | MC1776 | | | MC1776C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($R_S \leq 10$ kΩ) | $V_{IO}$ | | | | | | | mV |
| $T_A = +25^\circ C$ | | – | 2.0 | 5.0 | – | 2.0 | 6.0 | |
| $T_{low}^* \leq T_A \leq T_{high}^*$ | | – | – | 6.0 | – | – | 7.5 | |
| Offset Voltage Adjustment Range | $V_{IOR}$ | – | 18 | – | – | 18 | – | mV |
| Input Offset Current | $I_{IO}$ | | | | | | | nA |
| $T_A = +25^\circ C$ | | – | 2.0 | 15 | – | 2.0 | 25 | |
| $T_A = T_{high}$ | | – | – | 15 | – | – | 25 | |
| $T_A = T_{low}$ | | – | – | 40 | – | – | 40 | |
| Input Bias Current | $I_{IB}$ | | | | | | | nA |
| $T_A = +25^\circ C$ | | – | 15 | 50 | – | 15 | 50 | |
| $T_A = T_{high}$ | | – | – | 50 | – | – | 50 | |
| $T_A = T_{low}$ | | – | – | 120 | – | – | 100 | |
| Input Resistance | $r_i$ | – | 5.0 | – | – | 5.0 | – | MΩ |
| Input Capacitance | $c_i$ | – | 2.0 | – | – | 2.0 | – | pF |
| Input Voltage Range | $V_{ID}$ | | | | | | | V |
| $T_{low} \leq T_A \leq T_{high}$ | | ±1.0 | – | – | ±1.0 | – | – | |
| Large Signal Voltage Gain | $A_{VOL}$ | | | | | | | V/V |
| $R_L \geq 5.0$ kΩ, $V_O = \pm 1.0$ V, $T_A = +25^\circ C$ | | 50 k | 200 k | – | 25 k | 200 k | – | |
| $R_L \geq 5.0$ kΩ, $V_O = \pm 1.0$ V, $T_{low} \leq T_A \leq T_{high}$ | | 25 k | – | – | 25k | – | – | |
| Output Voltage Swing | $V_O$ | | | | | | | V |
| $R_L \geq 5.0$ kΩ, $T_{low} \leq T_A \leq T_{high}$ | | ±1.9 | ±2.1 | – | ±2.0 | ±2.1 | – | |
| Output Resistance | $r_o$ | – | 1.0 | – | – | 1.0 | – | kΩ |
| Output Short-Circuit Current | $I_{os}$ | – | 5.0 | – | – | 5.0 | – | mA |
| Common-Mode Rejection Ratio | CMRR | | | | | | | dB |
| $R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$ | | 70 | 86 | – | 70 | 86 | – | |
| Supply Voltage Rejection Ratio | PSRR | | | | | | | μV/V |
| $R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$ | | – | 25 | 150 | – | 25 | 200 | |
| Supply Current | $I_{CC}$, $I_{EE}$ | | | | | | | μA |
| $T_A = +25^\circ C$ | | – | 130 | 160 | – | 130 | 170 | |
| $T_{low} \leq T_A \leq T_{high}$ | | – | – | 180 | – | – | 180 | |
| Power Dissipation | $P_D$ | | | | | | | μW |
| $T_A = +25^\circ C$ | | – | 780 | 960 | – | 780 | 1020 | |
| $T_{low} \leq T_A \leq T_{high}$ | | – | – | 1080 | – | – | 1080 | |
| Transient Response (Unity Gain) | | | | | | | | |
| $V_{in} = 20$ mV, $R_L \geq 5.0$ kΩ, $C_L = 100$ pF | | | | | | | | |
| Rise Time | $t_{TLH}$ | – | 0.6 | – | – | 0.6 | – | μs |
| Overshoot | OS | – | 5.0 | – | – | 5.0 | – | % |
| Slew Rate ($R_L \geq 5.0$ kΩ) | $S_R$ | – | 0.35 | – | – | 0.35 | – | V/μs |

$^*T_{low} = -55^\circ C$ for MC1776 $\quad T_{high} = +125^\circ C$ for MC1776
$0^\circ C$ for MC1776C $\quad +70^\circ C$ for MC1776C

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $I_{set}$ = 1.5 μA, $T_A$ = +25°C unless otherwise noted.)

| Characteristic | Symbol | MC1776 | | | MC1776C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($R_S \leqslant$ 10 kΩ) | $V_{IO}$ | | | | | | | mV |
| $T_A$ = +25°C | | – | 2.0 | 5.0 | – | 2.0 | 6.0 | |
| $T_{low}$* $\leqslant T_A \leqslant T_{high}$* | | – | – | 6.0 | – | – | 7.5 | |
| Offset Voltage Adjustment Range | $V_{IOR}$ | – | 9.0 | – | – | 9.0 | – | mV |
| Input Offset Current | $I_{IO}$ | | | | | | | nA |
| $T_A$ = +25°C | | – | 0.7 | 3.0 | – | 0.7 | 6.0 | |
| $T_A = T_{high}$ | | – | – | 5.0 | – | – | 6.0 | |
| $T_A = T_{low}$ | | – | – | 10 | – | – | 10 | |
| Input Bias Current | $I_{IB}$ | | | | | | | nA |
| $T_A$ = +25°C | | – | 2.0 | 7.5 | – | 2.0 | 10 | |
| $T_A = T_{high}$ | | – | – | 7.5 | – | – | 10 | |
| $T_A = T_{low}$ | | – | – | 20 | – | – | 20 | |
| Input Resistance | $r_i$ | – | 50 | – | – | 50 | – | MΩ |
| Input Capacitance | $c_i$ | – | 2.0 | – | – | 2.0 | – | pF |
| Input Voltage Range | $V_{ID}$ | | | | | | | V |
| $T_{low} \leqslant T_A \leqslant T_{high}$ | | ±10 | – | – | ±10 | – | – | |
| Large Signal Voltage Gain | $A_{VOL}$ | | | | | | | V/V |
| $R_L \geqslant$ 75 kΩ, $V_O$ = ±10 V, $T_A$ = +25°C | | 200 k | 400 k | – | 50 k | 400 k | – | |
| $R_L \geqslant$ 75 kΩ, $V_O$ = ±10 V, $T_{low} \leqslant T_A \leqslant T_{high}$ | | 100 k | – | – | 50 k | – | – | |
| Output Voltage Swing | $V_O$ | | | | | | | V |
| $R_L \geqslant$ 75 kΩ, $T_A$ = +25°C | | ±12 | ±14 | – | ±12 | ±14 | – | |
| $R_L \geqslant$ 75 kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$ | | ±10 | – | – | ±10 | – | – | |
| Output Resistance | $r_o$ | – | 5.0 | – | – | 5.0 | – | kΩ |
| Output Short-Circuit Current | $I_{OS}$ | – | 3.0 | – | – | 3.0 | – | mA |
| Common-Mode Rejection Ratio | CMRR | | | | | | | dB |
| $R_S \leqslant$ 10 kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$ | | 70 | 90 | – | 70 | 90 | – | |
| Supply Voltage Rejection Ratio | PSRR | | | | | | | μV/V |
| $R_S \leqslant$ 10 kΩ, $T_{low} \leqslant T_A \leqslant T_{high}$ | | – | 25 | 150 | – | 25 | 200 | |
| Supply Current | $I_{CC}$, $I_{EE}$ | | | | | | | μA |
| $T_A$ = +25°C | | – | 20 | 25 | – | 20 | 30 | |
| $T_{low} \leqslant T_A \leqslant T_{high}$ | | – | – | 30 | – | – | 35 | |
| Power Dissipation | $P_D$ | | | | | | | mW |
| $T_A$ = +25°C | | – | – | 0.75 | – | – | 0.9 | |
| $T_{low} \leqslant T_A \leqslant T_{high}$ | | – | – | 0.9 | – | – | 1.05 | |
| Transient Response (Unity Gain) | | | | | | | | |
| $V_{in}$ = 20 mV, $R_L \geqslant$ 5.0 kΩ, $C_L$ = 100 pF | | | | | | | | |
| Rise Time | $t_{TLH}$ | – | 1.6 | – | – | 1.6 | – | μs |
| Overshoot | OS | – | 0 | – | – | 0 | – | % |
| Slew Rate ($R_L \geqslant$ 5.0 kΩ) | $S_R$ | – | 0.1 | – | – | 0.1 | – | V/μs |

*$T_{low}$ = −55°C for MC1776 $T_{high}$ = +125°C for MC1776
0°C for MC1776C +70°C for MC1776C

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $I_{set}$ = 15 μA, $T_A$ = +25°C unless otherwise noted.)

| | | MC1776 | | | MC1776C | | | |
|---|---|---|---|---|---|---|---|---|
| **Characteristic** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Input Offset Voltage ($R_S \leq 10$ kΩ) | $V_{IO}$ | | | | | | | mV |
| $T_A$ = +25°C | | – | 2.0 | 5.0 | – | 2.0 | 6.0 | |
| $T_{low}$* ≤ $T_A$ ≤ $T_{high}$* | | – | – | 6.0 | – | – | 7.5 | |
| Offset Voltage Adjustment Range | $V_{IOR}$ | – | 18 | – | – | 18 | – | mV |
| Input Offset Current | $I_{IO}$ | | | | | | | nA |
| $T_A$ = +25°C | | – | 2.0 | 15 | – | 2.0 | 25 | |
| $T_A = T_{high}$ | | – | – | 15 | – | – | 25 | |
| $T_A = T_{low}$ | | – | – | 40 | – | – | 40 | |
| Input Bias Current | $I_{IB}$ | | | | | | | nA |
| $T_A$ = +25°C | | – | 15 | 50 | – | 15 | 50 | |
| $T_A = T_{high}$ | | – | – | 50 | – | – | 50 | |
| $T_A = T_{low}$ | | – | – | 120 | – | – | 100 | |
| Input Resistance | $r_i$ | – | 5.0 | – | – | 5.0 | – | MΩ |
| Input Capacitance | $c_i$ | – | 2.0 | – | – | 2.0 | – | pF |
| Input Voltage Range | $V_{ID}$ | | | | | | | V |
| $T_{low} \leq T_A \leq T_{high}$ | | ±10 | – | – | ±10 | – | – | |
| **Large Signal Voltage Gain** | $A_{VOL}$ | | | | | | | V/V |
| $R_L \geq 5.0$ kΩ, $V_O$ = ±10 V, $T_A$ = +25°C | | 100 k | 400 k | – | 50 k | 400 k | – | |
| $R_L \geq 75$ kΩ, $V_O$ = ±10 V, $T_{low} \leq T_A \leq T_{high}$ | | 75 k | – | – | 50 k | – | – | |
| **Output Voltage Swing** | $V_O$ | | | | | | | V |
| $R_L \geq 5.0$ kΩ, $T_A$ = +25°C | | ±10 | ±13 | – | ±10 | ±13 | – | |
| $R_L \geq 75$ kΩ, $T_{low} \leq T_A \leq T_{high}$ | | ±10 | – | – | ±10 | – | – | |
| Output Resistance | $r_o$ | – | 1.0 | – | – | 1.0 | – | kΩ |
| Output Short-Circuit Current | $I_{os}$ | – | 12 | – | – | 12 | – | mA |
| **Common-Mode Rejection Ratio** | CMRR | | | | | | | dB |
| $R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$ | | 70 | 90 | – | 70 | 90 | – | |
| **Supply Voltage Rejection Ratio** | PSRR | | | | | | | μV/V |
| $R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$ | | – | 25 | 150 | – | 25 | 200 | |
| Supply Current | $I_{CC}, I_{EE}$ | | | | | | | μA |
| $T_A$ = +25°C | | – | 160 | 180 | – | 160 | 190 | |
| $T_{low} \leq T_A \leq T_{high}$ | | – | – | 200 | – | – | 200 | |
| Power Dissipation | $P_D$ | | | | | | | mW |
| $T_A$ = +25°C | | – | – | 5.4 | – | – | 5.7 | |
| $T_{low} \leq T_A \leq T_{high}$ | | – | – | 6.0 | – | – | 6.0 | |
| Transient Response (Unity Gain) | | | | | | | | |
| $V_{in}$ = 20 mV, $R_L \geq 5.0$ kΩ, $C_L$ = 100 pF | | | | | | | | |
| Rise Time | $t_{TLH}$ | – | 0.35 | – | – | 0.35 | – | μs |
| Overshoot | OS | – | 10 | – | – | 10 | – | % |
| Slew Rate ($R_L \geq 5.0$ kΩ) | $S_R$ | – | 0.8 | – | – | 0.8 | – | V/μs |

*$T_{low}$ = −55°C for MC1776
0°C for MC1776C

$T_{high}$ = +125°C for MC1776
+70°C for MC1776C

## TYPICAL CHARACTERISTICS

($T_A$ = +25°C unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

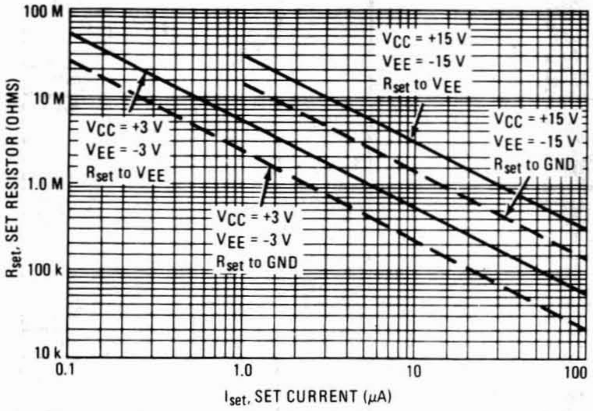


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

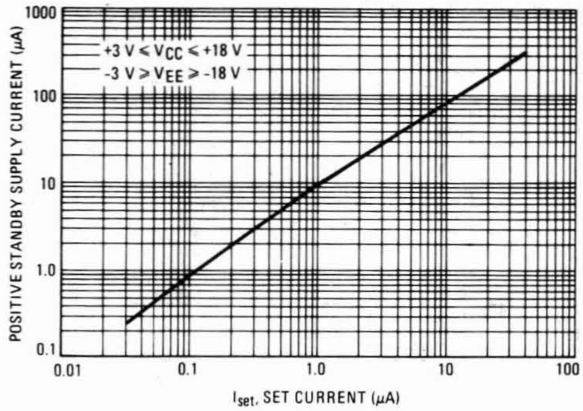


FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

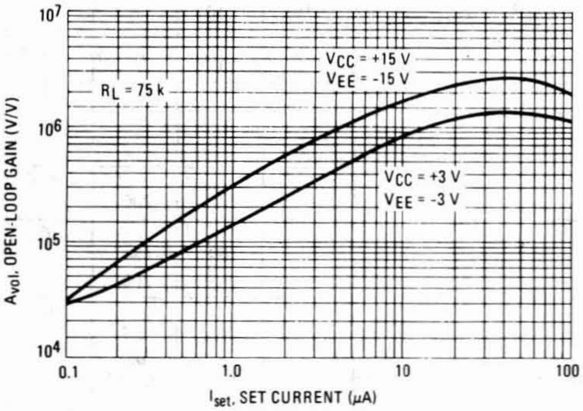


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

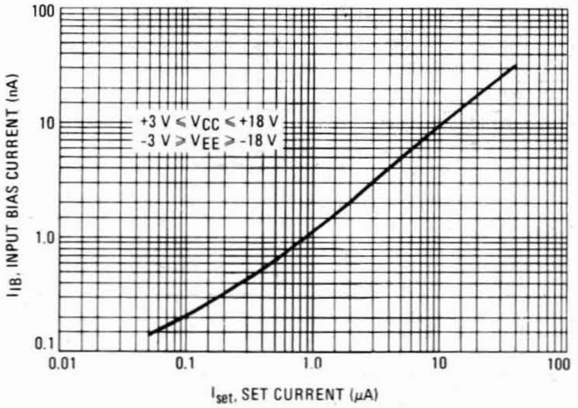


FIGURE 5 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

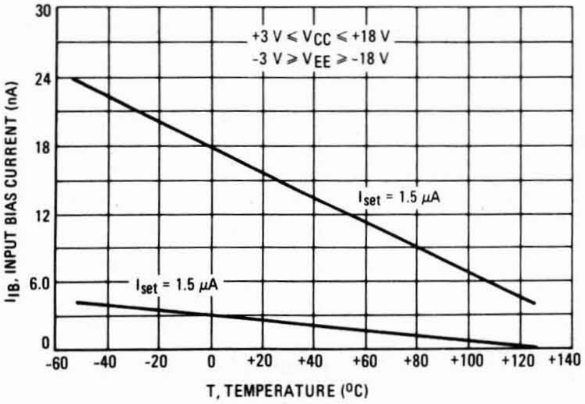
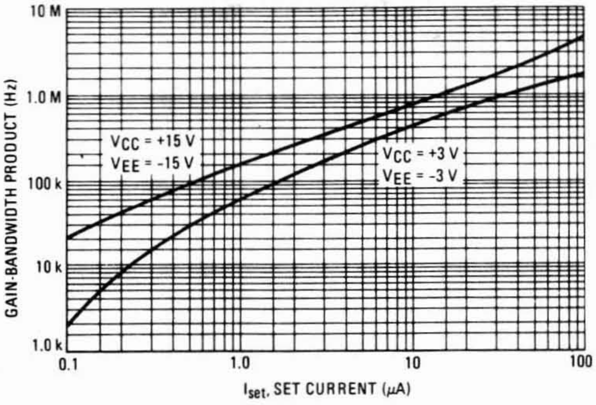


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



## TYPICAL CHARACTERISTICS (continued)

($T_A$ = +25°C unless otherwise noted.)

FIGURE 7 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

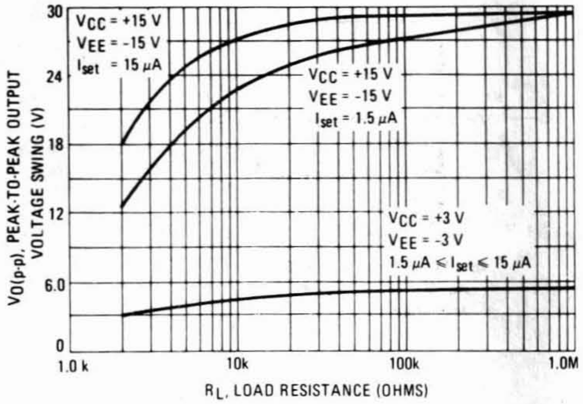


FIGURE 8 – SUPPLY CURRENT versus AMBIENT TEMPERATURE

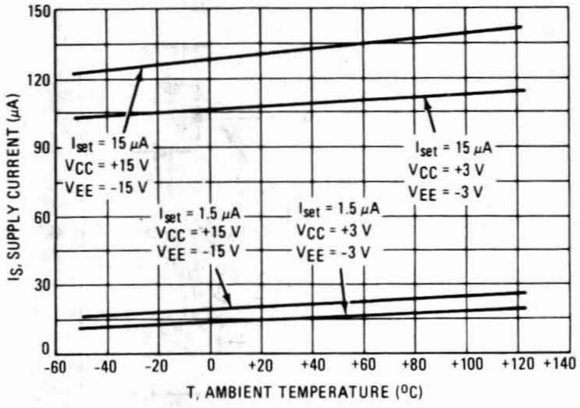


FIGURE 9 – OUTPUT SWING versus SUPPLY VOLTAGE

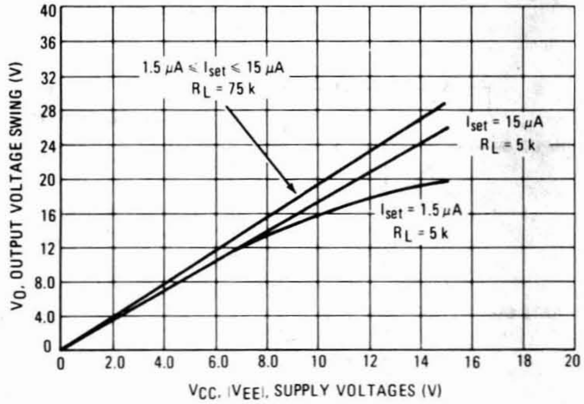


FIGURE 10 – SLEW RATE versus SET CURRENT

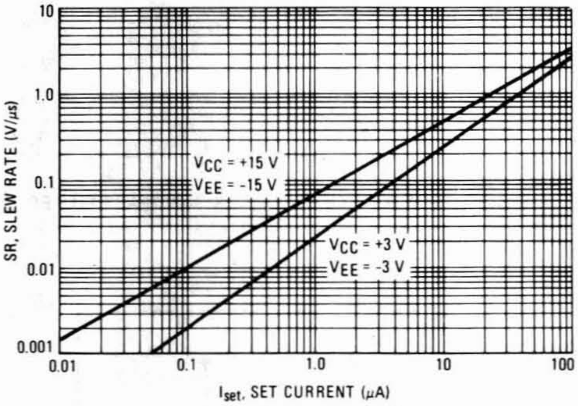


FIGURE 11 – INPUT NOISE VOLTAGE versus SET CURRENT

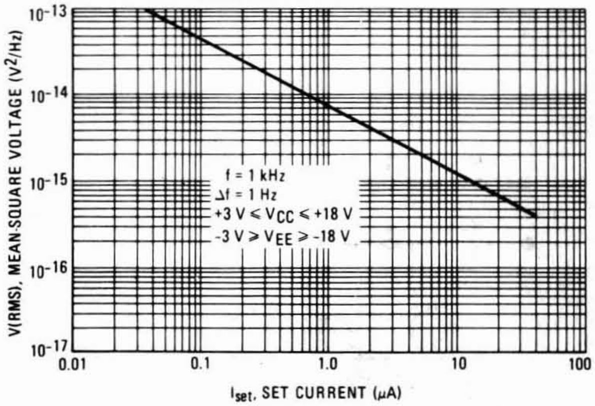
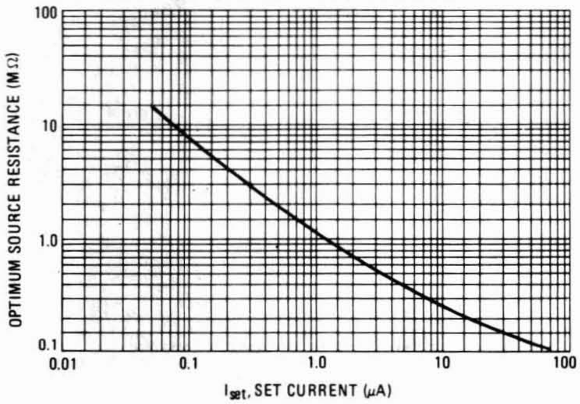
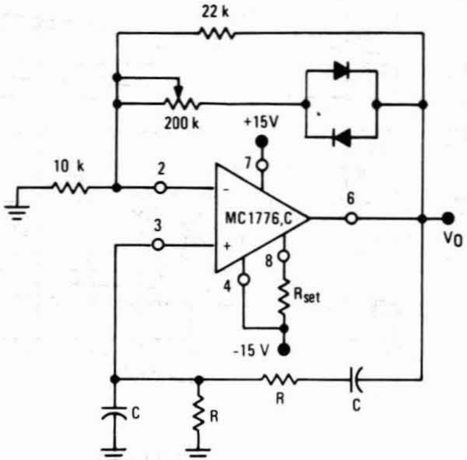


FIGURE 12 – OPTIMUM SOURCE RESISTANCE FOR MINIMUM NOISE versus SET CURRENT



## APPLICATIONS INFORMATION

FIGURE 13 – WIEN BRIDGE OSCILLATOR

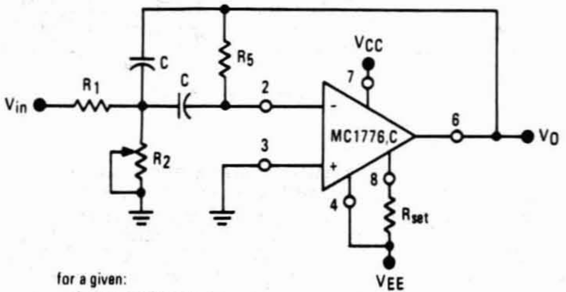

22 k
200 k
+15V
10 k
2
7
3
6
MC1776,C
8
4
Rset
-15 V
Vo
R
C
C
R

$$f_o = \frac{1}{2\pi RC}$$

(for $f_o$ = 1.0 kHz)

R = 16 kΩ
C = 0.01 μF

FIGURE 14 – MULTIPLE FEEDBACK BANDPASS FILTER


VCC
C
R5
R1
C
2
7
Vin
6
MC1776,C
Vo
3
R2
8
4
Rset
VEE

for a given:
$f_o$ = center frequency
A $(f_o)$ = Gain at center frequency
Q = quality factor
Choose a value for C, then

$$R_5 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R5}{2A\,(f_o)}$$

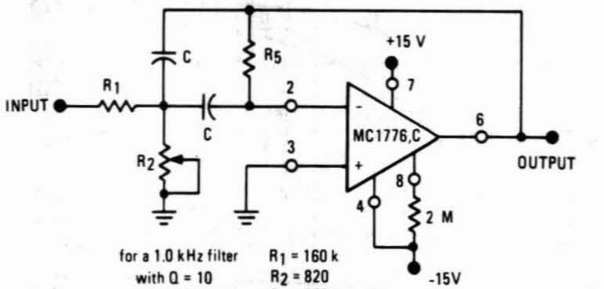
$$R2 = \frac{R1\,R5}{4Q^2\,R1 - R5}$$

To obtain less than 10% error from the operational amplifier:

$$\frac{Q_0\,f_o}{GBW} \leq 0.1$$

where $f_o$ and GBW are expressed in Hz. GBW is available from Figure 6 as a function of Set Current, $I_{set}$.

FIGURE 15 – MULTIPLE FEEDBACK BANDPASS FILTER (1.0 kHz)


C
R5
+15 V
R1
2
7
INPUT
C
6
MC1776,C
3
OUTPUT
R2
8
4
2 M
-15V

for a 1.0 kHz filter
with Q = 10
and A $(f_o)$ = 1

$R_1$ = 160 k
$R_2$ = 820
$R_5$ = 300 k
C = 0.01 μF

FIGURE 16 – GATED AMPLIFIER

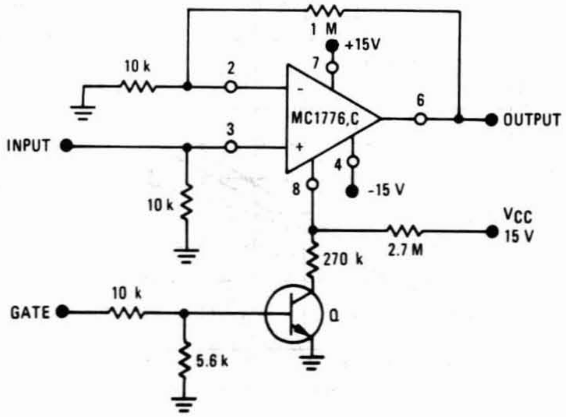
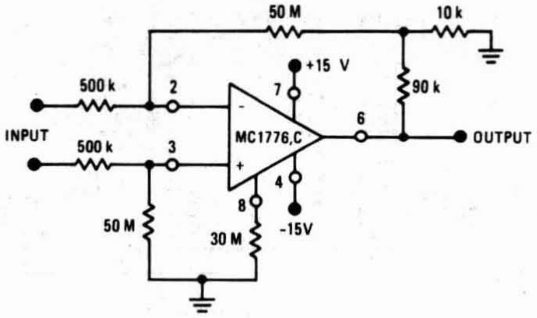

1 M
+15V
10 k
2
7
6
MC1776,C
OUTPUT
INPUT
3
4
8
-15 V
10 k
Vcc
15 V
2.7 M
270 k
10 k
GATE
Q
5.6 k

FIGURE 17 – HIGH INPUT IMPEDANCE AMPLIFIER


50 M
10 k
+15 V
500 k
2
7
90 k
6
INPUT
500 k
3
MC1776,C
OUTPUT
4
8
50 M
30 M
-15V

**MOTOROLA**

# MC3301 LM2900
# MC3401 LM3900

## Specifications and Applications Information

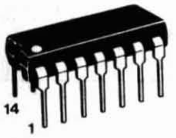
## QUAD OPERATIONAL AMPLIFIER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

### QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER

These internally compensated Norton operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each device contains four independent amplifiers — making it ideal for applications such as active filters, multi-channel amplifiers, tachometers, oscillators and other similar usages.

- Single-Supply Operation
- Internally Compensated
- Wide Unity Gain Bandwidth: 4.0 MHz Typical
- Low Input Bias Current: 50 nA Typical
- High Open-Loop Gain: 1000 V/V Minimum
- Large Output Voltage Swing: $(V_{CC} - 1)\ V_{p\text{-}p}$



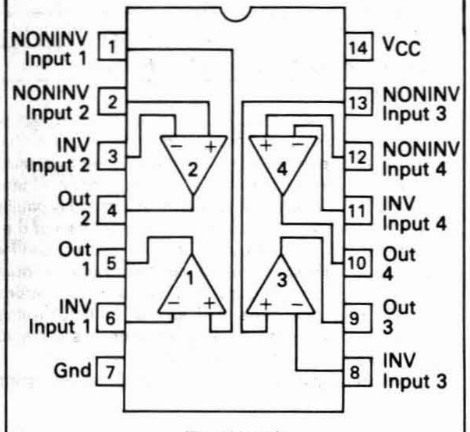
**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14

### MAXIMUM RATINGS

| Rating | Symbol | LM2900/ LM3900 | MC3301 | MC3401 | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | +32 | +28 | +18 | V |
| Input Currents ($I_{in}^+$ or $I_{in}^-$) | $I_{in}$ | 5.0 | 5.0 | 5.0 | mA |
| Output Current | $I_O$ | 50 | 50 | 50 | mA |
| Power Dissipation ($T_A$ = +25°C)<br>Derate above $T_A$ = +25°C | $P_D$<br>$1/R_{\theta JA}$ | 625<br>5.0 | 625<br>5.0 | 625<br>5.0 | mW<br>mW/°C |
| Operating Ambient Temperature Range | $T_A$ | — | −40 to +85 | 0 to +70 | °C |
| LM2900 | | −40 to +85 | — | — | |
| LM3900 | | 0 to +70 | — | — | |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | −65 to +150 | −65 to +150 | °C |

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| LM3900D<br>MC3401D | 0°C to +70°C | SO-14 |
| LM3900N<br>MC3401P | | Plastic DIP |
| LM2900N<br>MC3301P | −40°C to +85°C | |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $T_A$ = +25°C unless otherwise noted)

| Characteristic | Symbol | LM2900 | | | LM3900 | | | MC3301 | | | MC3401 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Open-Loop Voltage Gain | $A_{VOL}$ | | | | | | | | | | | | | V/mV |
| f = 100 Hz, $R_L$ = 5.0 k | | 1.2 | 2.0 | — | 1.2 | 2.0 | — | 1.2 | 2.0 | — | 1.2 | 2.0 | — | |
| $T_A$ = $T_{low}$ to $T_{high}$ (Notes 1, 2) | | — | — | — | — | — | — | — | — | — | 0.8 | — | — | |
| Input Resistance (Inverting Input) | $r_i$ | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | 0.1 | 1.0 | — | MΩ |
| Output Resistance | $r_O$ | — | 8.0 | — | — | 8.0 | — | — | 8.0 | — | — | 8.0 | — | kΩ |
| Input Bias Current (Inverting Input) | $I_{IB}$ | — | 50 | 200 | — | 50 | 200 | — | 50 | 300 | — | 50 | 300 | nA |
| $T_A$ = $T_{low}$ to $T_{high}$ (Note 1) | | — | — | — | — | — | — | — | — | — | — | — | 500 | |
| Slew Rate ($C_L$ = 100 pF, $R_L$ = 2.0 k) | SR | | | | | | | | | | | | | V/μs |
| Positive Output Swing | | — | 0.5 | — | — | 0.5 | — | — | 0.5 | — | — | 0.5 | — | |
| Negative Output Swing | | — | 20 | — | — | 20 | — | — | 20 | — | — | 20 | — | |
| Unity Gain Bandwidth | BW | — | 4.0 | — | — | 4.0 | — | — | 4.0 | — | — | 4.0 | — | MHz |
| Output Voltage Swing (Note 7) | | | | | | | | | | | | | | V |
| $V_{CC}$ = +15 V, $R_L$ = 2.0 k | | | | | | | | | | | | | | |
| $V_{out}$ High ($I_{in}^-$ = 0, $I_{in}^+$ = 0) | $V_{OH}$ | 13.5 | 14.2 | — | 13.5 | 14.2 | — | 13.5 | 14.2 | — | 13.5 | 14.2 | — | |
| $V_{out}$ Low ($I_{in}^-$ = 10 μA, $I_{in}^+$ = 0) | $V_{OL}$ | — | 0.03 | 0.2 | — | 0.03 | 0.2 | — | 0.03 | 0.2 | — | 0.03 | 0.2 | |
| $V_{CC}$ = Maximum Rating, $R_L$ = ∞ | | | | | | | | | | | | | | |
| $V_{out}$ High ($I_{in}^-$ = 0, $I_{in}^+$ = 0) | $V_{OH}$ | — | 29.5 | — | — | 29.5 | — | — | 25.5 | — | — | 15.5 | — | |
| Output Current | | | | | | | | | | | | | | mA |
| Source | $I_{source}$ | 6.0 | 10 | — | 6.0 | 10 | — | 5.0 | 10 | — | 5.0 | 10 | — | |
| Sink (Note 3) | $I_{sink}$ | 0.5 | 0.87 | — | 0.5 | 0.87 | — | 0.5 | 0.87 | — | 0.5 | 0.87 | — | |
| Low Level Output Current | $I_{OL}$ | — | 5.0 | — | — | 5.0 | — | — | 5.0 | — | — | 5.0 | — | |
| $I_{in}^-$ = 5.0 μA, $V_{OL}$ = 1.0 V | | | | | | | | | | | | | | |
| Supply Current (All Four Amplifiers) | | | | | | | | | | | | | | mA |
| Noninverting Inputs Open | $I_{DO}$ | — | 6.9 | 10 | — | 6.9 | 10 | — | 6.9 | 10 | — | 6.9 | 10 | |
| Noninverting Inputs Grounded | $I_{DG}$ | — | 7.8 | 14 | — | 7.8 | 14 | — | 7.8 | 14 | — | 7.8 | 14 | |
| Power Supply Rejection (f = 100 Hz) | PSRR | — | 55 | — | — | 55 | — | — | 55 | — | — | 55 | — | dB |
| Mirror Gain ($T_A$ = $T_{low}$ to $T_{high}$; Notes 1, 4) | $A_i$ | | | | | | | | | | | | | μA |
| $I_{in}^+$ = 20 μA | | 0.90 | 1.0 | 1.1 | 0.90 | 1.0 | 1.1 | 0.90 | 1.0 | 1.1 | 0.90 | 1.0 | 1.1 | |
| $I_{in}^+$ = 200 μA | | 0.90 | 1.0 | 1.1 | 0.90 | 1.0 | 1.1 | 0.90 | 1.0 | 1.1 | 0.90 | 1.0 | 1.0 | |
| Δ Mirror Gain ($T_A$ = $T_{low}$ to $T_{high}$; Notes 1, 4) 20 μA ≤ $I_{in}^+$ ≤ 200 μA | $\Delta A_i$ | — | 2.0 | 5.0 | — | 2.0 | 5.0 | — | 2.0 | 5.0 | — | 2.0 | 5.0 | % |
| Mirror Current ($T_A$ = $T_{low}$ to $T_{high}$; Note 1) | | — | 10 | 500 | — | 10 | 500 | — | 10 | 500 | — | 10 | 500 | μA |
| Negative Input Current (Note 6) | | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | mA |

NOTES:

1. $T_{low}$ = −40°C for LM2900, MC3301 $T_{high}$ = +85°C for LM2900, MC3301
   = 0°C for LM3900, MC3401 = +70°C ffor LM3900, MC3401
2. Open-loop voltage gain is defined as voltage gain from the inverting input to the output.
3. Sink current is specified for linear operation. When the device is used as a comparator (non-linear operation) where the inverting input is overdriven, the sink current (low level output current) capability is typically 5.0 mA.
4. This specification indicates the current gain of the current mirror which is used as the noninverting input.
5. Input $V_{BE}$ match between the noninverting and inverting inputs occurs for a mirror current (noninverting input current) of approximately 10 μA.
6. Clamp transistors are included to prevent the input voltages from swinging below ground more than approximately −0.3 volts. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately 1.0 mA. Negative input currents in excess of 4.0 mA will cause the output to drop to a low voltage. These values apply for any one of the input terminals. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common-mode biasing can be used to prevent negative input voltages.
7. When used as a noninverting amplifier, the minimum output voltage is the $V_{BE}$ of the inverting input transistor.

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $R_L$ = 5.0 kΩ, $T_A$ = +25°C
[each amplifier] unless otherwise noted.)

**FIGURE 1 — OPEN-LOOP VOLTAGE GAIN versus FREQUENCY**

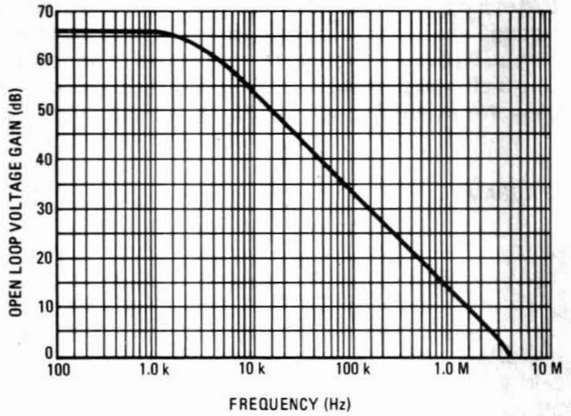


**FIGURE 2 — OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE**

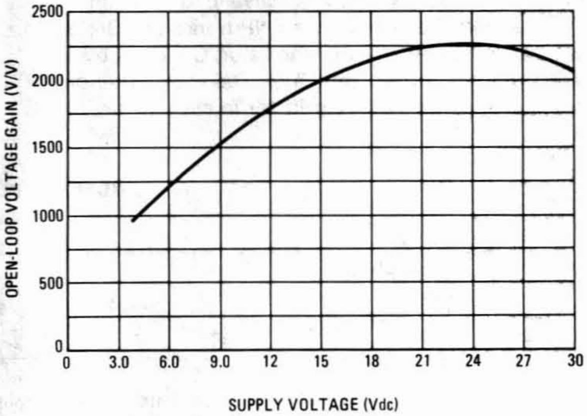


**FIGURE 3 — OUTPUT RESISTANCE versus FREQUENCY**

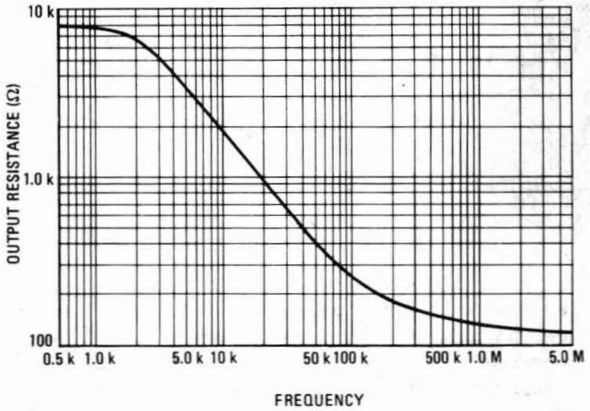


**FIGURE 4 — SUPPLY CURRENT versus SUPPLY VOLTAGE**

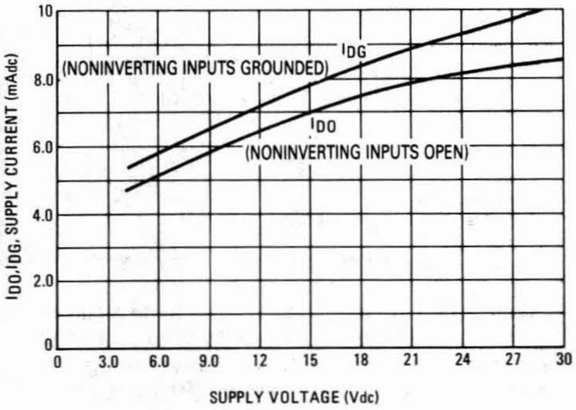


**FIGURE 5 — LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE**

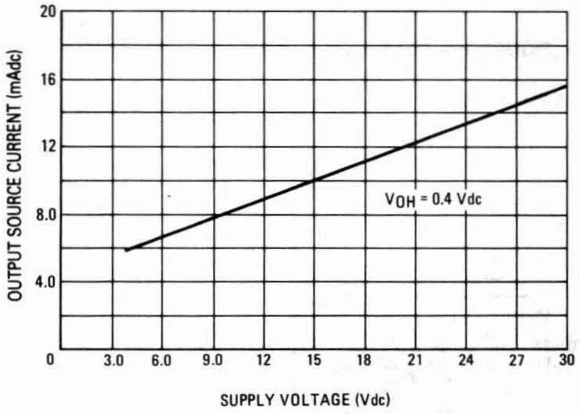
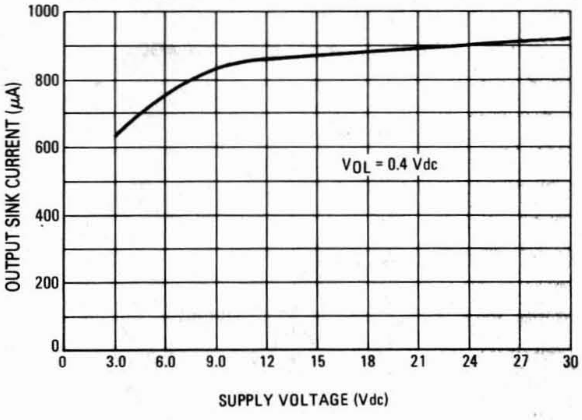


**FIGURE 6 — LINEAR SINK CURRENT versus SUPPLY VOLTAGE**

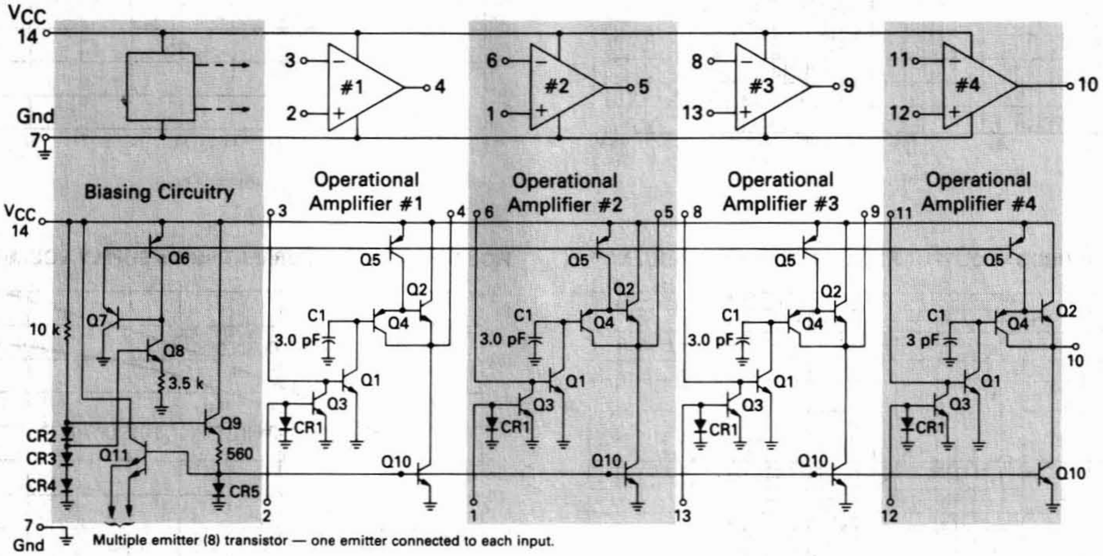


## OPERATION AND APPLICATIONS

### BASIC AMPLIFIER

The basic amplifier is the common emitter stage shown in Figures 7 and 8. The active load $I_1$ is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased Class A by the current source $I_2$. The magnitude of $I_2$ (specified $I_{sink}$) is a limiting factor in capacitively coupled linear operation at the output. The sink current of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 volt resulting in an increase in the distortion appearing at the output. Closed-loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 10 on the following page. No external compensation is required.

FIGURE 7 — BLOCK DIAGRAM


VCC
14
Gnd
7
3
2
#1
4
6
1
#2
5
8
13
#3
9
11
12
#4
10
Biasing Circuitry
Operational Amplifier #1
Operational Amplifier #2
Operational Amplifier #3
Operational Amplifier #4
Q6
Q7
Q8
10 k
3.5 k
Q9
560
CR2
CR3
CR4
CR5
Q11
Q5
Q2
C1
3.0 pF
3 pF
Q4
Q1
Q3
CR1
Q10
Multiple emitter (8) transistor — one emitter connected to each input.

A noninverting input is obtained by adding a current mirror as shown in Figure 9. Essentially all current which enters the noninverting input, $I_{in}+$, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to $I_{in}+$. Since the alpha current gain of Q3 ≈ 1, its collector current is approximately equal to $I_{in}+$ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 8 — A BASIC GAIN STAGE

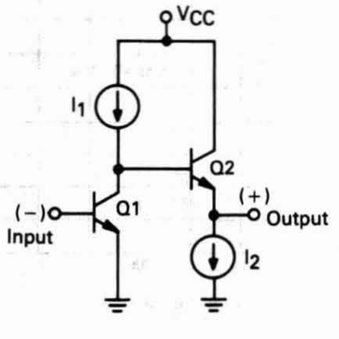
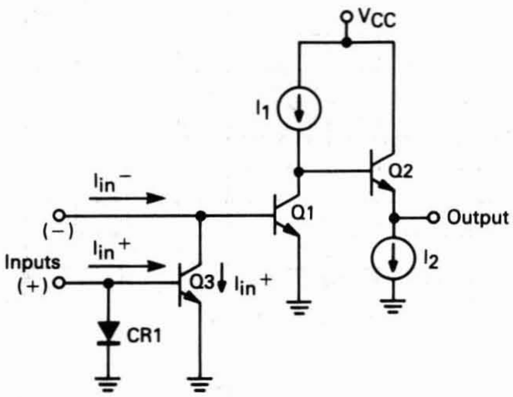

VCC
I1
Q2
Q1
(−)
Input
(+)
Output
I2

FIGURE 9 — OBTAINING A NONINVERTING INPUT


VCC
I1
Iin−
Q2
Q1
Output
(−)
Iin+
Inputs
(+)
Q3
Iin+
CR1
I2

## OPERATION AND APPLICATIONS (continued)

### BIASING CIRCUITRY

The circuitry common to all four amplifiers is shown in Figure 11. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the $V_{BE}$ of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the $V_{BE}$ drops of transistor Q9 and diode CR5 thus the current set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 7) provides circuit protection from signals that are negative with respect to ground.

FIGURE 10 — A BASIC OPERATIONAL AMPLIFIER

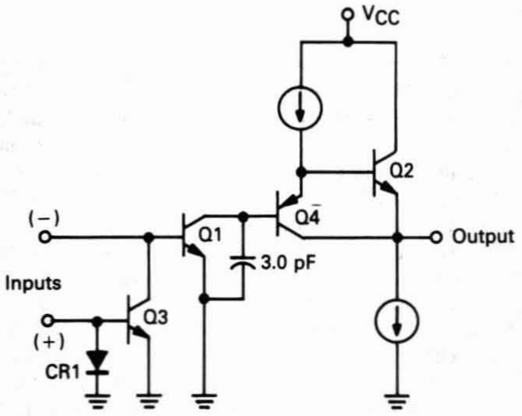
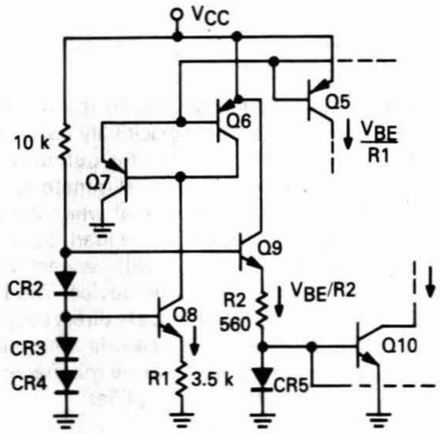


FIGURE 11 — BIASING CIRCUITRY



## NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing

   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing; as shown in Figures 12 and 13 (see the first page of this specification). The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μA to 200 μA range.

   B. $V_{CC}$ Reference Voltage (see Figures 12 and 13)

   The noninverting input is normally returned to the $V_{CC}$ voltage (which should be well filtered) through a resistor, $R_r$, allowing the input current, $I_{in}+$, to be within the range of 10 μA to 200 μA. Choosing the feedback resistor, $R_f$, to be equal to ½ $R_r$ will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows the maximum dynamic range of the output voltage.

   C. Reference Voltage other than $V_{CC}$ (see Figure 14)

   The biasing resistor $R_r$ may be returned to a voltage ($V_r$) other than $V_{CC}$. By setting $R_f = R_r$, (still keeping $I_{in}+$ between 10 μA and 200 μA) the output dc level will be equal to $V_r$. The expression for determining $V_{Odc}$ is:

$$V_{Odc} = \frac{(A_i)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_i\right) \phi$$

   where $\phi$ is the $V_{BE}$ drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). $A_i$ is the current mirror gain.

FIGURE 12 — INVERTING AMPLIFIER

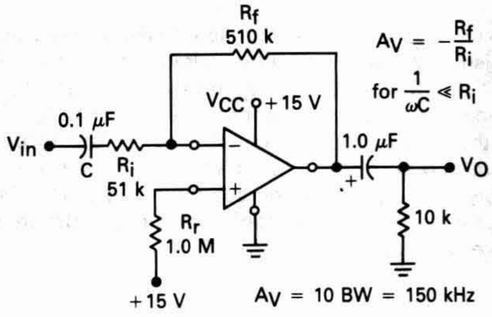
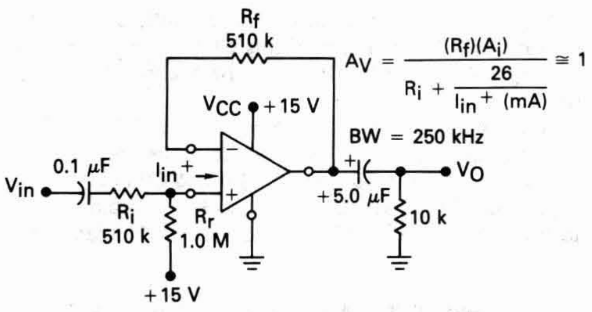

Rf
510 k
AV = −Rf/Ri
for 1/ωC ≪ Ri
VCC +15 V
0.1 μF
Vin
C
Ri
51 k
1.0 μF
VO
Rr
1.0 M
10 k
+15 V
AV = 10 BW = 150 kHz

FIGURE 13 — NONINVERTING AMPLIFIER


Rf
510 k
AV = (Rf)(Ai) / (Ri + 26/(Iin+ (mA))) ≅ 1
VCC +15 V
BW = 250 kHz
0.1 μF
Iin+
Vin
VO
+5.0 μF
Ri
510 k
Rr
1.0 M
10 k
+15 V

2. Gain Determination

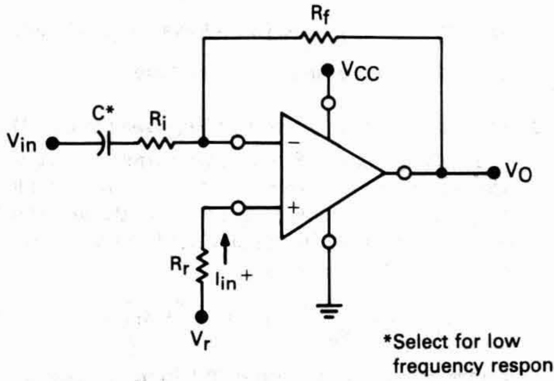
A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of $I_{sink}$ becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of $R_f$ to $R_i$, in the same manner as for a conventional operational amplifier:

$$A_V = \frac{R_f}{R_i}$$

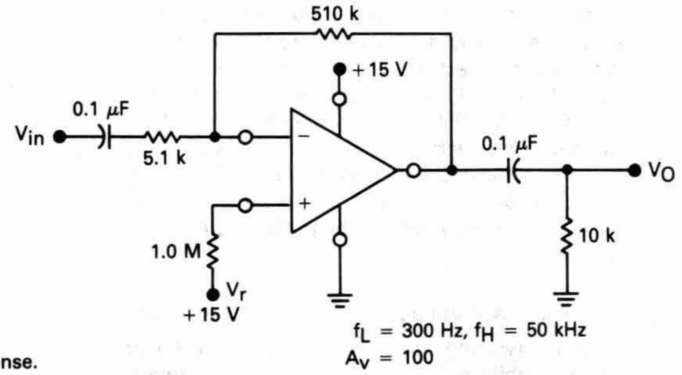
The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 4.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 400 kHz with 20 dB of closed-loop gain or 40 kHz with 40 dB of closed-loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed-loop gain intercepts the open-loop response curve. The inverting input capacity is typically 3.0 pF.

FIGURE 14 — INVERTING AMPLIFIER WITH ARBITRARY REFERENCE


Rf
VCC
Vin
C*
Ri
VO
Rr
Iin+
Vr

*Select for low frequency response.

FIGURE 15 — INVERTING AMPLIFIER WITH $A_V$ = 100 AND $V_r$ = $V_{CC}$


510 k
+15 V
0.1 μF
Vin
5.1 k
0.1 μF
VO
1.0 M
Vr
+15 V
10 k
fL = 300 Hz, fH = 50 kHz
AV = 100

B. Noninverting Amplifier

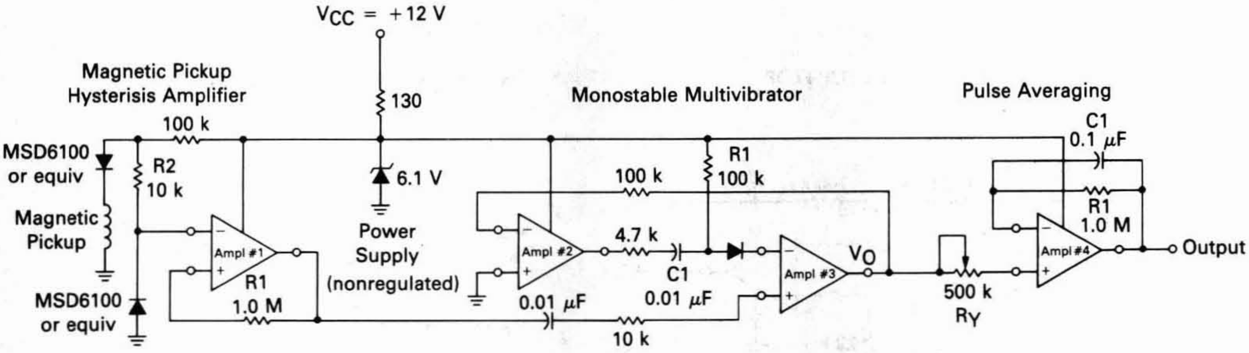
These devices may be used in the noninverting mode (see Figure 13). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_{in}{}^{+}}$ ohms, where $I_{in}{}^{+}$ is input current in milliamperes. The noninverting ac gain expression is given by:

$$A_V = \frac{(R_f)(A_i)}{R_i + \frac{26}{I_{in}{}^{+}\ (mA)}}$$

The bandwidth of the noninverting configuration for a given $R_f$ value is essentially independent of the gain chosen. For $R_f = 510\ k\Omega$ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

## TYPICAL APPLICATIONS

FIGURE 16 — TACHOMETER CIRCUIT


VCC = +12 V
Magnetic Pickup
Hysterisis Amplifier
130
Monostable Multivibrator
Pulse Averaging
100 k
MSD6100
or equiv
R2
10 k
Magnetic
Pickup
Ampl #1
R1
1.0 M
MSD6100
or equiv
6.1 V
Power
Supply
(nonregulated)
100 k
R1
100 k
Ampl #2
4.7 k
C1
0.01 µF
0.01 µF
10 k
Ampl #3
VO
500 k
RY
C1
0.1 µF
R1
1.0 M
Ampl #4
Output

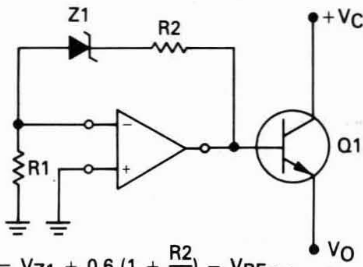
Hysterisis Voltage for Switching

$$V_H = \frac{A_iR2}{R1}(V_{CC} - 1.6)$$

Timing Interval: t ≈ 0.7 R1 C1

$$V_{p\text{-}p} \cong \frac{(V_O - 0.6) \cdot A_i \cdot t}{R_YC1}$$

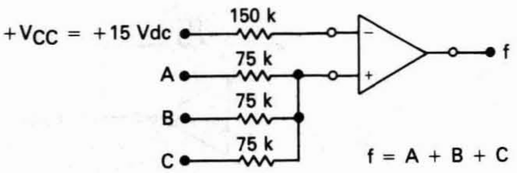
FIGURE 17 — VOLTAGE REGULATOR


Z1
R2
+VCC
R1
Q1
VO

$$V_O = V_{Z1} + 0.6\left(1 + \frac{R2}{R1}\right) - V_{BE_{Q1}}$$

NOTE:
For positive $T_C$ zeners R2 and R1 can be selected to give $T_C$ output.

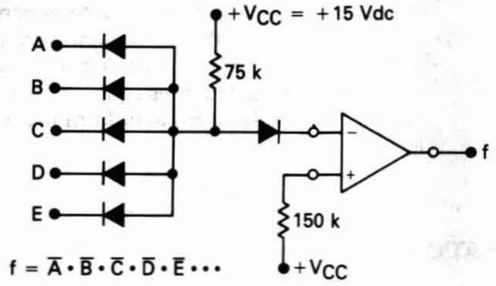
FIGURE 18 — LOGIC "OR" GATE


+VCC = +15 Vdc
150 k
A
75 k
B
75 k
C
75 k
f

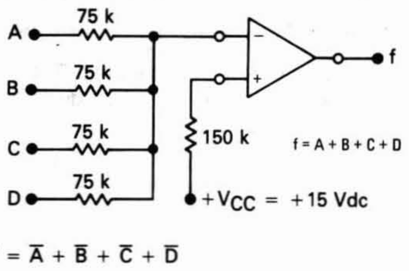
f = A + B + C

## TYPICAL APPLICATIONS (continued)

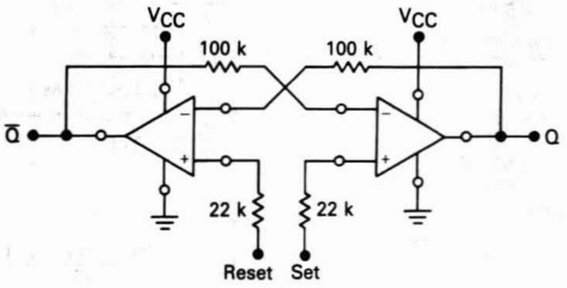
### FIGURE 19 — LOGIC "NAND" GATE (Large Fan-In)


+$V_{CC}$ = +15 Vdc
A
B
C
D
E
75 k
150 k
+$V_{CC}$
f
f = $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdots$

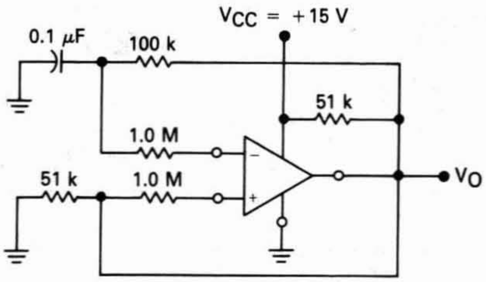
### FIGURE 20 — LOGIC "NOR" GATE


A
B
C
D
75 k
75 k
75 k
75 k
150 k
f
f = A + B + C + D
+$V_{CC}$ = +15 Vdc
f = $\overline{A} + \overline{B} + \overline{C} + \overline{D}$

### FIGURE 21 — R-S FLIP-FLOP

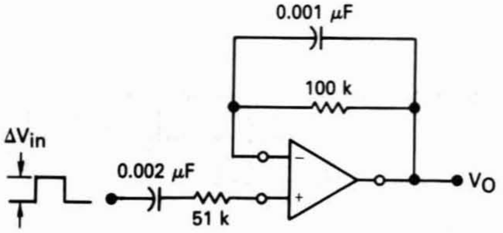

$V_{CC}$
$V_{CC}$
100 k
100 k
$\overline{Q}$
Q
22 k
22 k
Reset
Set

### FIGURE 22 — ASTABLE MULTIVIBRATOR

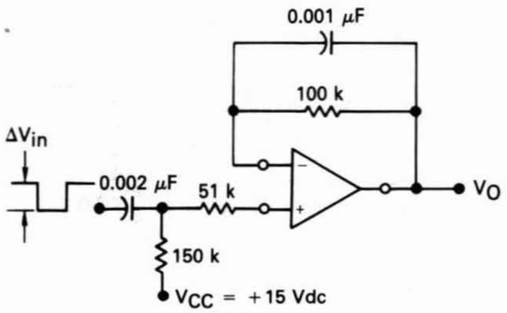

$V_{CC}$ = +15 V
0.1 μF
100 k
51 k
1.0 M
51 k
1.0 M
$V_O$

### FIGURE 23 — POSITIVE-EDGE DIFFERENTIATOR

Output Rise Time ≈ 0.22 ms
Input Change Time Constant ≈ 1.0 ms

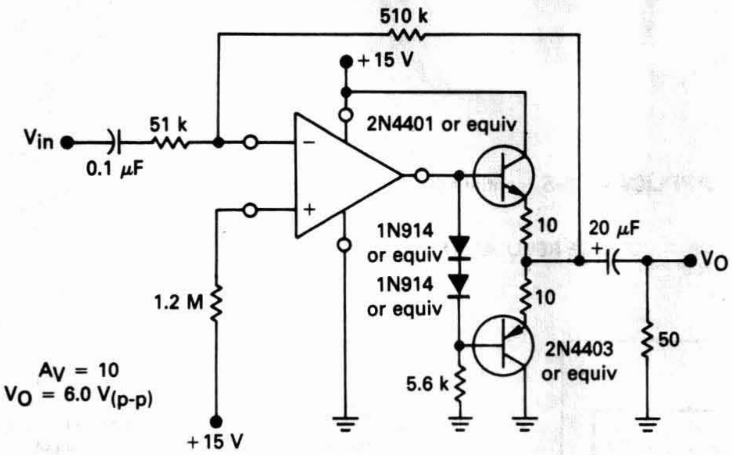

0.001 μF
100 k
ΔV$_{in}$
0.002 μF
51 k
$V_O$

### FIGURE 24 — NEGATIVE-EDGE DIFFERENTIATOR


0.001 μF
100 k
ΔV$_{in}$
0.002 μF
51 k
150 k
$V_O$
$V_{CC}$ = +15 Vdc

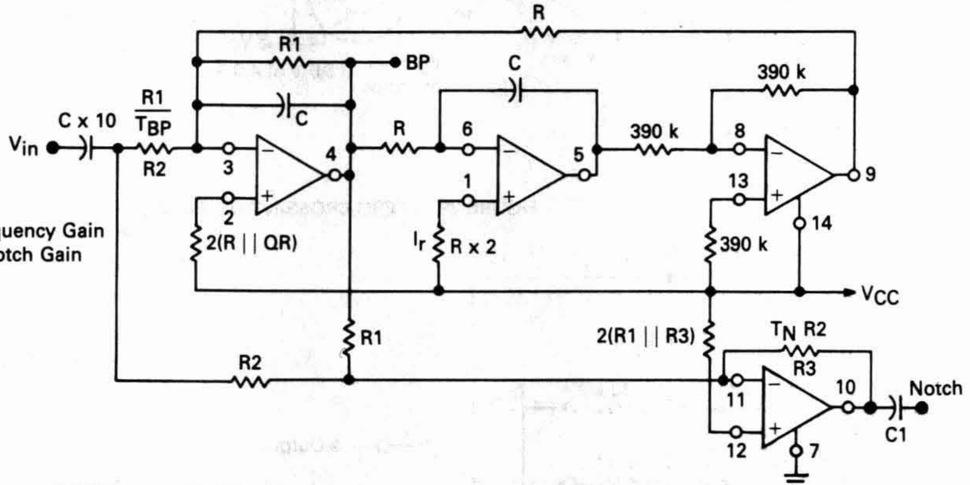
$V_{O(dc)}$ ≈ 7.0 Vdc
Output Rise Time ≈ 0.22 ms
Input Change Time Constant ≈ 1.0 ms

**FIGURE 25 — AMPLIFIER AND DRIVER FOR A 50-OHM LINE**


510 k
+15 V
$V_{in}$
0.1 μF
51 k
2N4401 or equiv
1N914
or equiv
1N914
or equiv
10
20 μF
10
$V_O$
1.2 M
50
2N4403
or equiv
5.6 k
+15 V

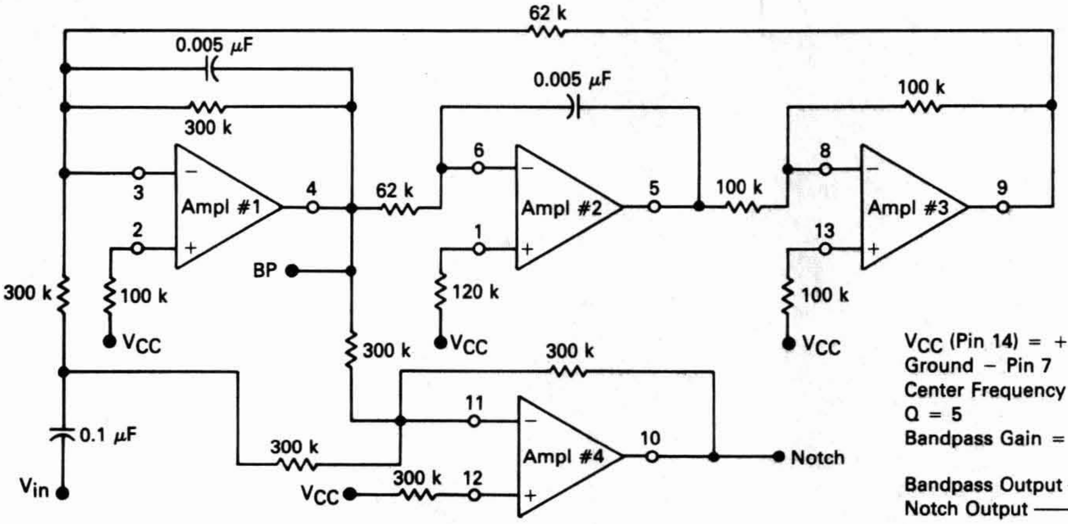
$A_V = 10$
$V_O = 6.0\ V_{(p-p)}$

**FIGURE 26 — BASIC BANDPASS AND NOTCH FILTER**


R
R1
BP
C
390 k
$\frac{R1}{T_{BP}}$
C x 10
C
$V_{in}$
R2
3
4
R
6
5
390 k
8
9
2
1
13
14
2(R || QR)
$I_r$
R x 2
390 k
$V_{CC}$
R1
2(R1 || R3)
$T_N$ R2
R3
R2
11
10
Notch
12
7
C1

$T_{BP}$ = Center Frequency Gain
$T_N$ = Passband Notch Gain
$\omega 0 = \frac{1}{RC}$
R1 = QR
$R2 = \frac{R1}{T_{BP}}$
R3 = $T_N$ R2

**FIGURE 27 — BANDPASS AND NOTCH FILTER**

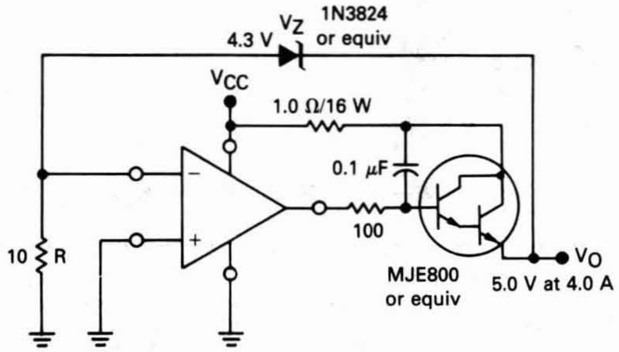

62 k
0.005 μF
0.005 μF
100 k
300 k
6
8
3
Ampl #1
4
62 k
Ampl #2
5
100 k
Ampl #3
9
2
1
13
BP
300 k
100 k
120 k
100 k
$V_{CC}$
$V_{CC}$
$V_{CC}$
300 k
300 k
11
0.1 μF
300 k
10
Ampl #4
Notch
$V_{in}$
$V_{CC}$
300 k
12

$V_{CC}$ (Pin 14) = +12 Volts
Ground – Pin 7
Center Frequency 500 Hz
Q = 5
Bandpass Gain = 1

Bandpass Output →Pin 4
Notch Output ——→ Pin 10

## TYPICAL APPLICATIONS (continued)

### FIGURE 28 — VOLTAGE REGULATOR

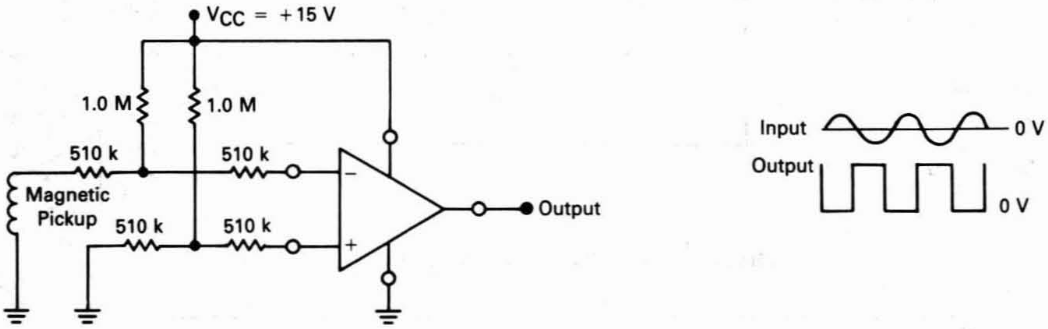

4.3 V
$V_Z$
1N3824
or equiv
$V_{CC}$
1.0 Ω/16 W
0.1 µF
100
−
+
10
R
MJE800
or equiv
$V_O$
5.0 V at 4.0 A

$V_O = V_Z + 0.6$ Vdc

NOTE 1: R is used to bias the zener.

NOTE 2: If the Zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈2.0 mV/°C), the output is zero-TC. A 7.0 Volt Zener will give approximately zero-TC.

### FIGURE 29 — ZERO CROSSING DETECTOR


$V_{CC} = +15$ V
1.0 M
1.0 M
510 k
510 k
510 k
510 k
Magnetic
Pickup
−
+
Output
Input
0 V
Output
0 V

**MOTOROLA**

# MC3403
# MC3503
# MC3303

## Specifications and Applications Information

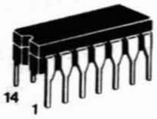
## QUAD LOW POWER OPERATIONAL AMPLIFIERS

The MC3503 is a low-cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741. However, the MC3503 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one third of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ±1.5 to ±18 Volts
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741
- Industry Standard Pinouts

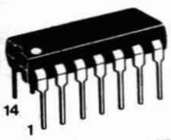
## QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT



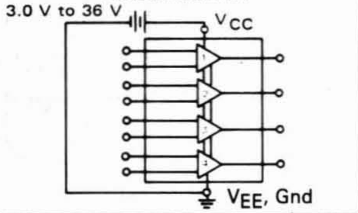
**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA

**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14

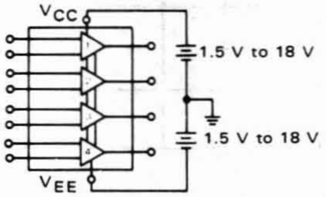


**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05
(MC3403 and MC3303 only)

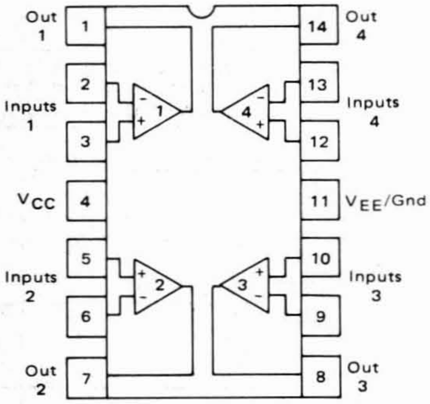
SINGLE SUPPLY



SPLIT SUPPLIES



PIN CONNECTIONS



(Top View)

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltages | | | Vdc |
| Single Supply | $V_{CC}$ | 36 | |
| Split Supplies | $V_{CC}$<br>$V_{EE}$ | +18<br>-18 | |
| Input Differential Voltage Range (1) | $V_{IDR}$ | ±36 | Vdc |
| Input Common Mode Voltage Range (1) (2) | $V_{ICR}$ | ±18 | Vdc |
| Storage Temperature Range | $T_{stg}$ | | °C |
| Ceramic Package | | -65 to +150 | |
| Plastic Package | | -55 to +125 | |
| Operating Ambient Temperature Range | $T_A$ | | °C |
| MC3503 | | -55 to +125 | |
| MC3403 | | 0 to +70 | |
| MC3303 | | -40 to +85 | |
| Junction Temperature | $T_J$ | | °C |
| Ceramic Package | | 175 | |
| Plastic Package | | 150 | |

(1) Split Power Supplies.
(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

### ORDERING INFORMATION

| Type | Temperature Range | Package |
|---|---|---|
| MC3303L | −40°C to +85°C | Ceramic DIP |
| MC3303P | −40°C to +85°C | Plastic DIP |
| MC3403D | 0°C to +70°C | SO-14 |
| MC3403L | 0°C to +70°C | Ceramic DIP |
| MC3403P | 0°C to +70°C | Plastic DIP |
| MC3503L | −55°C to +125°C | Ceramic DIP |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V for MC3503, MC3403; $V_{CC}$ = +14 V, $V_{EE}$ = Gnd for MCC3303. $T_A$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | MC3503 | | | MC3403 | | | MC3303 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage<br>$T_A = T_{high}$ to $T_{low}$ (1) | $V_{IO}$ | –<br>– | 2.0<br>– | 5.0<br>6.0 | –<br>– | 2.0<br>– | 10<br>12 | –<br>– | 2.0<br>– | 8.0<br>10 | mV |
| Input Offset Current<br>$T_A = T_{high}$ to $T_{low}$ | $I_{IO}$ | –<br>– | 30<br>– | 50<br>200 | –<br>– | 30<br>– | 50<br>200 | –<br>– | 30<br>– | 75<br>250 | nA |
| Large Signal Open-Loop Voltage Gain<br>$V_O = \pm 10$ V, $R_L = 2.0$ kΩ,<br>$T_A = T_{high}$ to $T_{low}$ | $A_{VOL}$ | 50<br>25 | 200<br>– | –<br>– | 20<br>15 | 200<br>– | –<br>– | 20<br>15 | 200<br>– | –<br>– | V/mV |
| Input Bias Current<br>$T_A = T_{high}$ to $T_{low}$ | $I_{IB}$ | –<br>– | -200<br>-300 | -500<br>-1500 | –<br>– | -200<br>– | -500<br>-800 | –<br>– | -200<br>– | -500<br>-1000 | nA |
| Output Impedance<br>f = 20 Hz | $z_o$ | – | 75 | – | – | 75 | – | – | 75 | – | Ω |
| Input Impedance<br>f = 20 Hz | $z_i$ | 0.3 | 1.0 | – | 0.3 | 1.0 | – | 0.3 | 1.0 | – | MΩ |
| Output Voltage Range<br>$R_L$ = 10 kΩ<br>$R_L$ = 2.0 kΩ<br>$R_L$ = 2.0 kΩ, $T_A = T_{high}$ to $T_{low}$ | $V_{OR}$ | ±12<br>±10<br>±10 | ±13.5<br>±13<br>– | –<br>–<br>– | ±12<br>±10<br>±10 | ±13.5<br>±13<br>– | –<br>–<br>– | +12<br>+10<br>+10 | +12.5<br>+12<br>– | –<br>–<br>– | V |
| Input Common-Mode Voltage Range | $V_{ICR}$ | +13 V $-V_{EE}$ | +13.5 V $-V_{EE}$ | – | +13 V $-V_{EE}$ | +13.5 V $-V_{EE}$ | – | +12 V $-V_{EE}$ | +12.5 V $-V_{EE}$ | – | V |
| Common-Mode Rejection Ratio<br>$R_S \leq 10$ kΩ | CMRR | 70 | 90 | – | 70 | 90 | – | 70 | 90 | – | dB |
| Power Supply Current ($V_o$ = 0)<br>$R_L = \infty$ | $I_{CC}, I_{EE}$ | – | 2.8 | 4.0 | – | 2.8 | 7.0 | – | 2.8 | 7.0 | mA |
| Individual Output Short-Circuit Current (2) | $I_{OS\pm}$ | ±10 | ±30 | ±45 | ±10 | ±20 | ±45 | ±10 | ±30 | ±45 | mA |
| Positive Power Supply Rejection Ratio | PSRR+ | – | 30 | 150 | – | 30 | 150 | – | 30 | 150 | μV/V |
| Negative Power Supply Rejection Ratio | PSRR− | – | 30 | 150 | – | 30 | 150 | – | – | – | μV/V |
| Average Temperature Coefficient of Input Offset Current<br>$T_A = T_{high}$ to $T_{low}$ | $\Delta I_{IO}/\Delta T$ | – | 50 | – | – | 50 | – | – | 50 | – | pA/°C |
| Average Temperature Coefficient of Input Offset Voltage<br>$T_A = T_{high}$ to $T_{low}$ | $\Delta V_{IO}/\Delta T$ | – | 10 | – | – | 10 | – | – | 10 | – | μV/°C |
| Power Bandwidth<br>$A_V = 1$, $R_L = 2.0$ kΩ, $V_o$ = 20 V(p-p),<br>THD = 5% | $BW_p$ | – | 9.0 | – | – | 9.0 | – | – | 9.0 | – | kHz |
| Small-Signal Bandwidth<br>$A_V = 1$, $R_L = 10$ kΩ, $V_o$ = 50 mV | BW | – | 1.0 | – | – | 1.0 | – | – | 1.0 | – | MHz |
| Slew Rate<br>$A_V = 1$, $V_i$ = −10 V to +10 V | SR | – | 0.6 | – | – | 0.6 | – | – | 0.6 | – | V/μs |
| Rise Time<br>$A_V = 1$, $R_L = 10$ kΩ, $V_o$ = 50 mV | $t_{TLH}$ | – | 0.35 | – | – | 0.35 | – | – | 0.35 | – | μs |
| Fall Time<br>$A_V = 1$, $R_L = 10$ kΩ, $V_o$ = 50 mV | $t_{THL}$ | – | 0.35 | – | – | 0.35 | – | – | 0.35 | – | μs |
| Overshoot<br>$A_V = 1$, $R_L = 10$ kΩ, $V_o$ = 50 mV | OS | – | 20 | – | – | 20 | – | – | 20 | – | % |
| Phase Margin<br>$A_V = 1$, $R_L = 2.0$ kΩ, $C_L$ = 200 pF | $\phi m$ | – | 60 | – | – | 60 | – | – | 60 | – | Degrees |
| Crossover Distortion<br>($V_{in}$ = 30 mVp-p, $V_{out}$ = 2.0 Vp-p,<br>f = 10 kHz) | – | – | 1.0 | – | – | 1.0 | – | – | 1.0 | – | % |

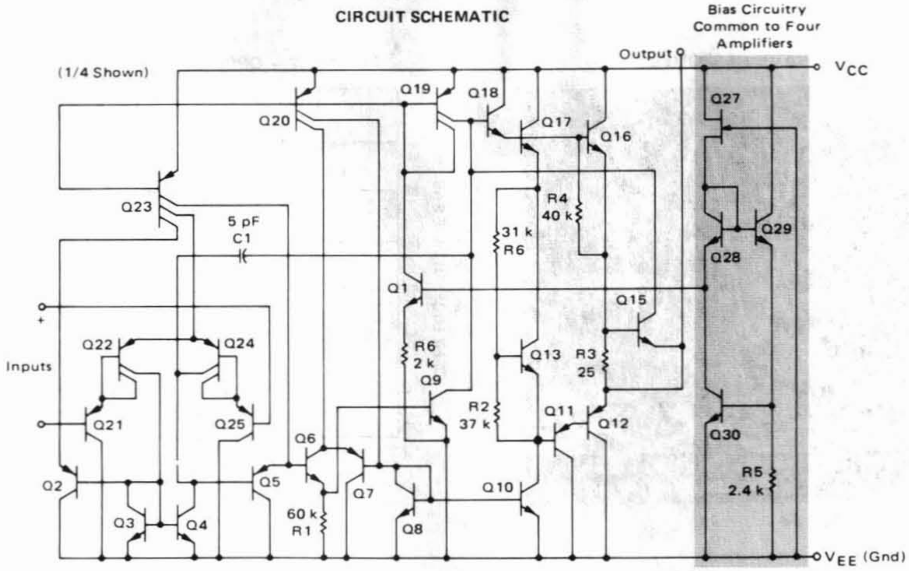
(1) $T_{high}$ = 125°C for MC3503, 70°C for MC3403, 85°C for MC3303
$T_{low}$ = −55°C for MC3503, 0°C for MC3403, −40°C for MC3303

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = Gnd, $T_A$ = 25°C unless otherwise noted.)

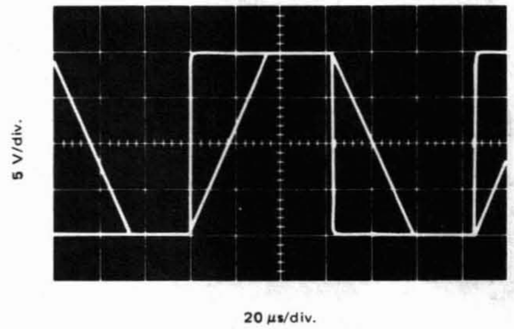
| Characteristic | Symbol | MC3503 | | | MC3403 | | | MC3303 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{IO}$ | – | 2.0 | 5.0 | – | 2.0 | 10 | – | – | 10 | mV |
| Input Offset Current | $I_{IO}$ | – | 30 | 50 | – | 30 | 50 | – | – | 75 | nA |
| Input Bias Current | $I_{IB}$ | – | -200 | -500 | – | -200 | -500 | – | – | -500 | nA |
| Large-Signal Open-Loop Voltage Gain<br>$R_L$ = 2.0 kΩ | $A_{VOL}$ | 10 | 200 | – | 10 | 200 | – | 10 | 200 | – | V/mV |
| Power Supply Rejection Ratio | PSRR | – | – | 150 | – | – | 150 | – | – | 150 | μV/V |
| Output Voltage Range (3)<br>$R_L$ = 10 kΩ, $V_{CC}$ = 5.0 V<br>$R_L$ = 10 kΩ, 5.0 V $\leq V_{CC} \leq$ 30 V | $V_{OR}$ | 3.3<br>$V_{CC} - 2.0$ | 3.5<br>$V_{CC} - 1.7$ | –<br>– | 3.3<br>$V_{CC} - 2.0$ | 3.5<br>$V_{CC} - 1.7$ | –<br>– | 3.3<br>$V_{CC} - 2.0$ | 3.5<br>$V_{CC} - 1.7$ | –<br>– | Vp-p |
| Power Supply Current | $I_{CC}$ | – | 2.5 | 4.0 | – | 2.5 | 7.0 | – | 2.5 | 7.0 | mA |
| Channel Separation<br>f = 1.0 kHz to 20 kHz (Input Referenced) | – | – | -120 | – | – | -120 | – | – | -120 | – | dB |

(2) Not to exceed maximum package power dissipation.
(3) Output will swing to ground

CIRCUIT SCHEMATIC


(1/4 Shown)
Bias Circuitry Common to Four Amplifiers
Output
VCC
Q19
Q18
Q20
Q17
Q16
Q27
Q23
R4 40 k
5 pF C1
31 k R6
Q29
Q28
Q1
Q15
+
Inputs
Q22
Q24
R6 2 k
Q9
Q13
R3 25
Q21
Q25
R2 37 k
Q11
Q12
Q30
Q6
R5 2.4 k
Q2
Q5
Q7
Q10
Q3
Q4
60 k R1
Q8
VEE (Gnd)

INVERTER PULSE RESPONSE



### CIRCUIT DESCRIPTION

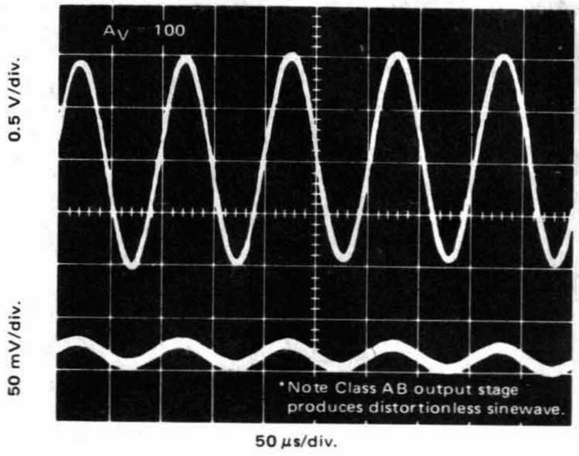
The MC3503/3403/3303 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

## TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE



*Note Class AB output stage produces distortionless sinewave.

FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

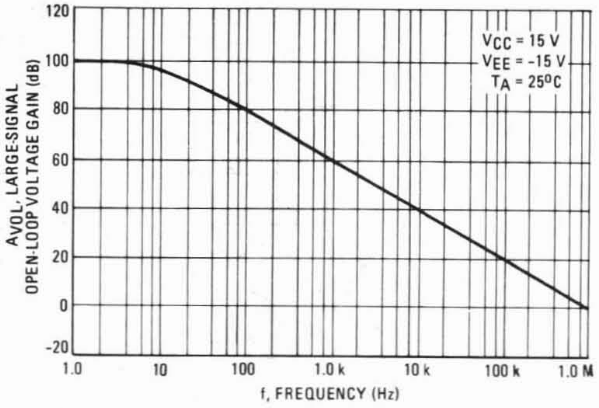


FIGURE 3 – POWER BANDWIDTH

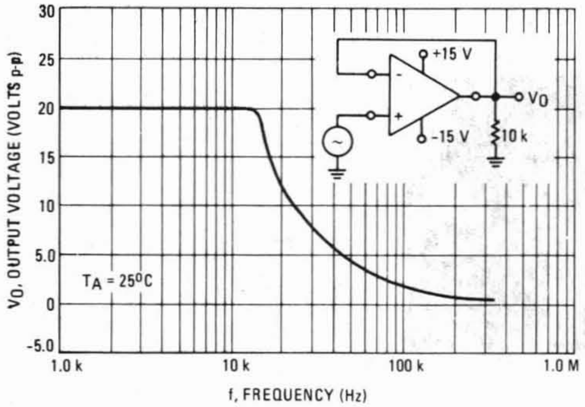


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

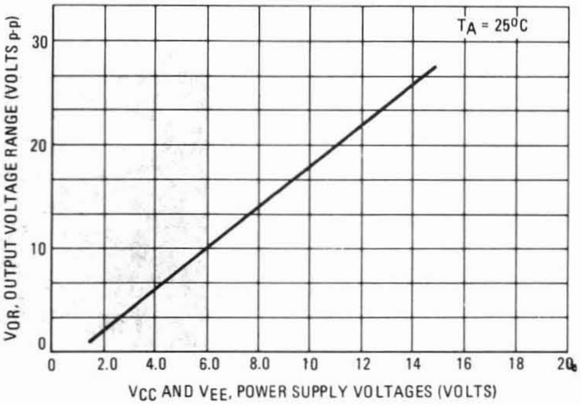


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

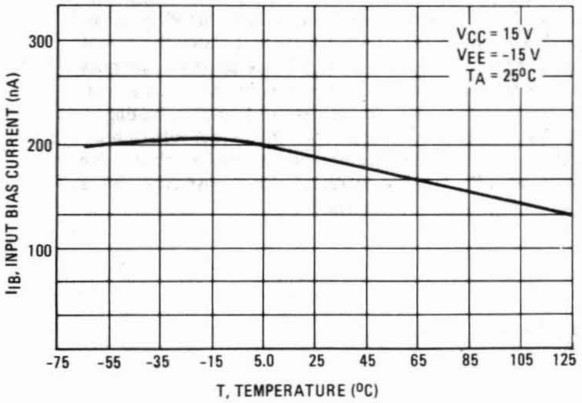
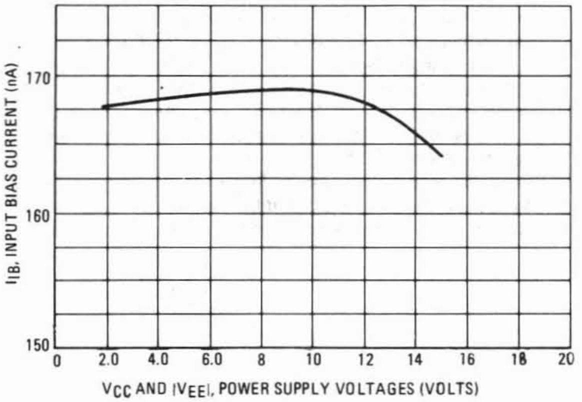
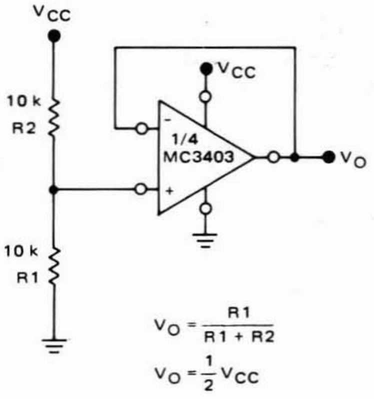


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



## APPLICATIONS INFORMATION

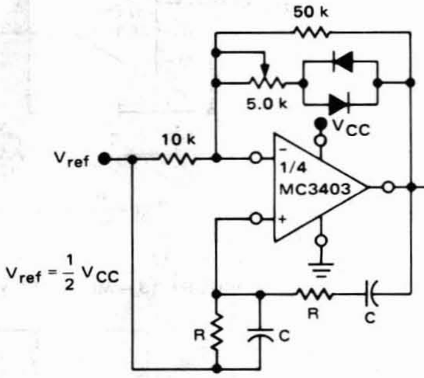
### FIGURE 7 – VOLTAGE REFERENCE


VCC
10 k
R2
10 k
R1
VCC
1/4
MC3403
VO

$V_O = \frac{R1}{R1 + R2}$

$V_O = \frac{1}{2} V_{CC}$

### FIGURE 8 — WIEN BRIDGE OSCILLATOR

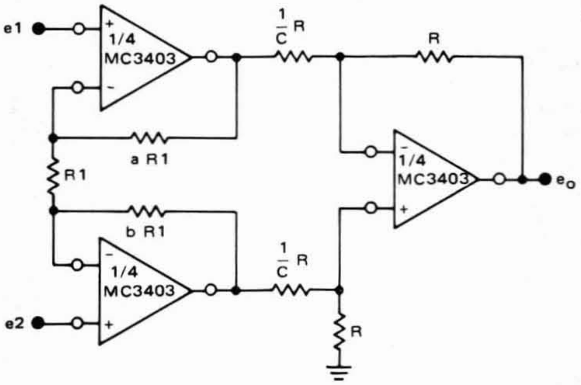

50 k
5.0 k
VCC
10 k
Vref
1/4
MC3403
VO
R
C
R
C

$V_{ref} = \frac{1}{2} V_{CC}$

$f_o = \frac{1}{2 \pi RC}$

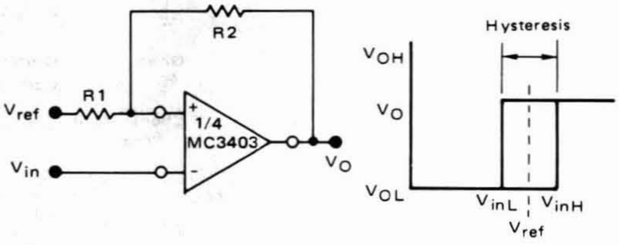
For $f_o = 1$ kHz
$R = 16\ k\Omega$
$C = 0.01\ \mu F$

### FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


e1
1/4
MC3403
$\frac{1}{C}$ R
R
a R1
R1
b R1
1/4
MC3403
e2
1/4
MC3403
$\frac{1}{C}$ R
R
1/4
MC3403
eo

$e_o = C\ (1 + a + b)\ (e2 - e1)$

### FIGURE 10 – COMPARATOR WITH HYSTERESIS

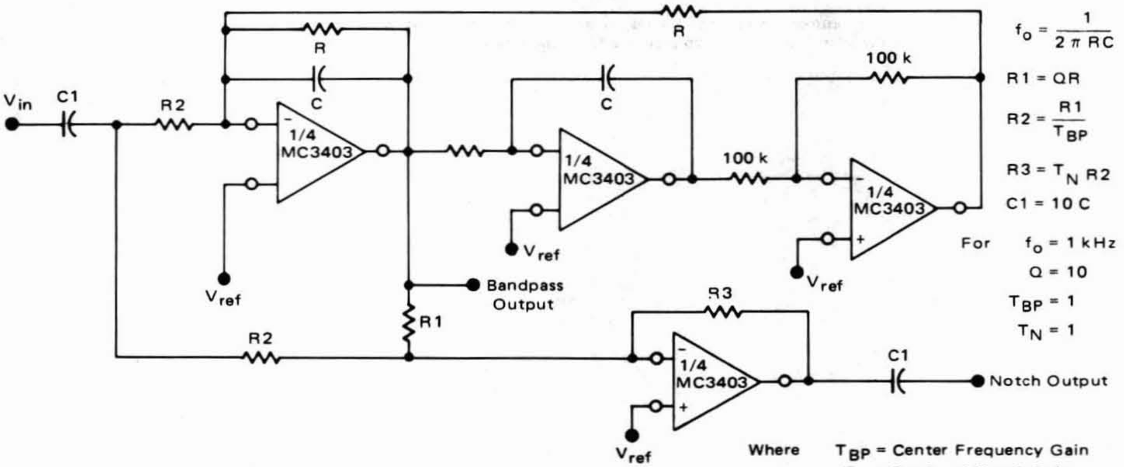

R2
R1
Vref
Vin
1/4
MC3403
VO
Hysteresis
VOH
VO
VOL
VinL
VinH
Vref

$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$

$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$

$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$

### FIGURE 11 – BI-QUAD FILTER


R
R
Vin
C1
R2
C
1/4
MC3403
Vref
C
1/4
MC3403
Vref
100 k
100 k
1/4
MC3403
Vref
Bandpass
Output
R1
R2
R3
1/4
MC3403
Vref
C1
Notch Output

$f_o = \frac{1}{2 \pi RC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N\ R2$

$C1 = 10\ C$

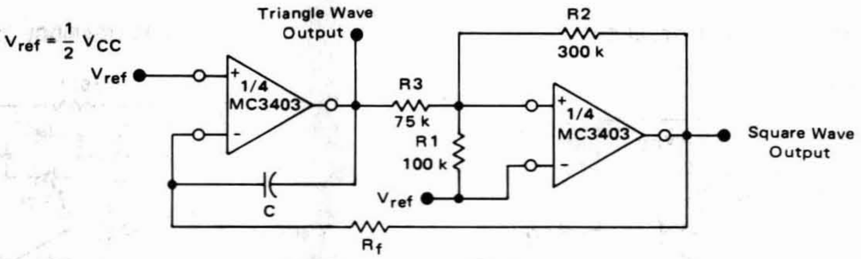
$V_{ref} = \frac{1}{2} V_{CC}$

For $f_o = 1$ kHz
$Q = 10$
$T_{BP} = 1$
$T_N = 1$

$R = 160\ k\Omega$
$C = 0.001\ \mu F$
$R1 = 1.6\ M\Omega$
$R2 = 1.6\ M\Omega$
$R3 = 1.6\ M\Omega$

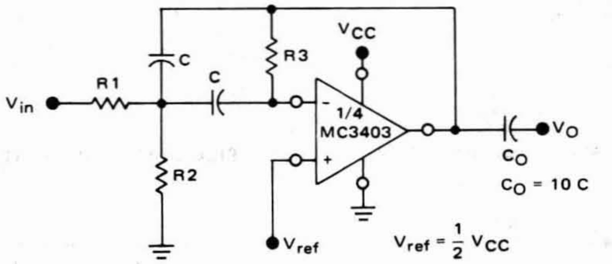
Where $T_{BP}$ = Center Frequency Gain
$T_N$ = Passband Notch Gain

FIGURE 12 – FUNCTION GENERATOR


$V_{ref} = \frac{1}{2} V_{CC}$
$V_{ref}$
Triangle Wave Output
1/4 MC3403
R3
75 k
R1
100 k
R2
300 k
1/4 MC3403
Square Wave Output
$V_{ref}$
C
$R_f$

$$f = \frac{R1 + RC}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER


$V_{in}$
R1
C
C
R3
R2
$V_{CC}$
1/4 MC3403
$V_O$
$C_O$
$C_O = 10\ C$
$V_{ref}$
$V_{ref} = \frac{1}{2} V_{CC}$

Given $f_o$ = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value $f_o$, C
Then:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\ R5}{4Q^2\,R1 - R5}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1$$ Where $f_o$ and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

**MOTOROLA**

# MC3405
# MC3505

## DUAL OPERATIONAL AMPLIFIER AND DUAL VOLTAGE COMPARATOR

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

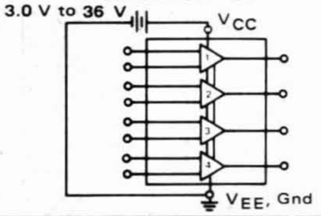
### DUAL OPERATIONAL AMPLIFIER AND DUAL COMPARATOR

The MC3405/3505 contains two differential-input operational amplifiers and two comparators, each set capable of single supply operation. This operational amplifier-comparator circuit fulfills its applications as a general purpose product for automotive and consumer circuits as well as an industrial building block.

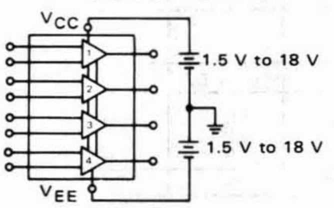
The MC3405 is specified over the commercial operating temperature range of 0 to +70°C, while the MC3505 is specified over the military operating range of −55 to +125°C.

- Operational Amplifiers Equivalent in Performance to MC3403/3503
- Comparators Similar in Performance to LM339/139
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ±1.5 to ±18 Volts
- Low Supply Current Drain
- Operational Amplifiers Are Internally Frequency Compensated
- Comparators TTL and CMOS Compatible

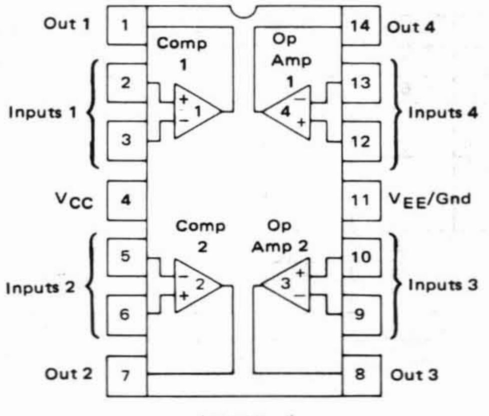
**SINGLE SUPPLY**


3.0 V to 36 V
VCC
1
2
3
4
VEE, Gnd

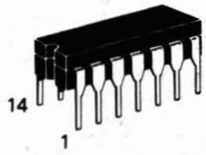
**SPLIT SUPPLIES**


VCC
1.5 V to 18 V
1.5 V to 18 V
1
2
3
4
VEE

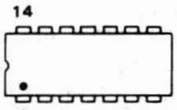
**PIN CONNECTIONS**


Out 1
1
Comp
1
Op
Amp
1
14
Out 4
Inputs 1
2
3
13
12
Inputs 4
VCC
4
11
VEE/Gnd
Comp
2
Op
Amp 2
Inputs 2
5
6
10
9
Inputs 3
Out 2
7
8
Out 3

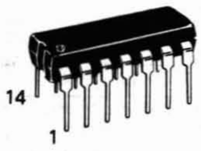
(Top View)



**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA



(Top View)



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

(MC3405 only)

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC3405L | 0 to +70°C | Ceramic DIP |
| MC3405P | 0 to +70°C | Plastic DIP |
| MC3505L | −55 to +125°C | Ceramic DIP |

## OPERATIONAL AMPLIFIER SECTION

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage—Single Supply<br>Split Supplies | $V_{CC}$<br>$V_{CC}, V_{EE}$ | 36<br>±18 | Vdc |
| Input Differential Voltage Range | $V_{IDR}$ | ±36 | Vdc |
| Input Common Mode Voltage Range | $V_{ICR}$ | ±18 | Vdc |
| Operating Ambient Temperature Range—MC3505<br>MC3405 | $T_A$ | -55 to +125<br>0 to +70 | °C |
| Storage Temperature Range—Ceramic Package<br>Plastic Package. | $T_{stg}$ | -65 to +150<br>-55 to +125 | °C |
| Operating Junction Temperature Range—Ceramic Package<br>Plastic Package | $T_J$ | 175<br>150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = Gnd, $T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | MC3505 | | | MC3405 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{IO}$ | – | 2.0 | 5.0 | – | 2.0 | 10 | mV |
| Input Offset Current | $I_{IO}$ | – | 30 | 50 | – | 30 | 50 | nA |
| Input Bias Current | $I_{IB}$ | – | -200 | -500 | – | -200 | -500 | nA |
| Large-Signal Open-Loop Voltage Gain<br>($R_L$ = 2.0 kΩ) | $A_{VOL}$ | 20 | 200 | – | 20 | 200 | – | V/mV |
| Power Supply Rejection Ratio | PSRR | – | – | 150 | – | – | 150 | µV/V |
| Output Voltage Range (Note 1)<br>($R_L$ = 10 kΩ, $V_{CC}$ = 5.0 V)<br>($R_L$ = 10 kΩ, 5.0 V ≤ $V_{CC}$ ≤ 30 V) | $V_{OR}$ | <br>3.3<br>$V_{CC}-2.0$ | <br>3.5<br>$V_{CC}-1.7$ | <br>–<br>– | <br>3.3<br>$V_{CC}-2.0$ | <br>3.5<br>$V_{CC}-1.7$ | <br>–<br>– | Vp-p |
| Power Supply Current (Notes 2 and 3) | $I_{CC}$ | – | 2.5 | 4.0 | – | 2.5 | 7.0 | mA |
| Channel Separation<br>f = 1.0 kHz to 20 kHz<br>(Input Referenced) | – | – | -120 | – | – | -120 | – | dB |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = -15 V, $T_A$ = 25°C unless otherwise noted)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage<br>($T_A$ = $T_{low}$ to $T_{high}$) (Note 4) | $V_{IO}$ | –<br>– | 2.0<br>– | 5.0<br>6.0 | –<br>– | 2.0<br>– | 10<br>12 | mV |
| Average Temperature Coefficient of Input Offset Voltage | $\Delta V_{IO}/\Delta T$ | – | 15 | – | – | 15 | – | µV/°C |
| Input Offset Current<br>($T_A$ = $T_{low}$ to $T_{high}$) (Note 4) | $I_{IO}$ | –<br>– | –<br>– | 50<br>200 | –<br>– | –<br>– | 50<br>200 | nA |
| Input Bias Current<br>($T_A$ = $T_{low}$ to $T_{high}$ (Note 4) | $I_{IB}$ | –<br>– | -200<br>-300 | -500<br>-1500 | –<br>– | -200<br>– | -500<br>-800 | nA |
| Input Common Mode Voltage Range | $V_{ICR}$ | +13 -$V_{EE}$ | – | – | +13-$V_{EE}$ | – | – | Vdc |
| Large Signal Open Loop Voltage Gain<br>($V_O$ = ±10 V, $R_L$ = 2.0 kΩ)<br>($T_A$ = $T_{low}$ to $T_{high}$) (Note 4) | $A_{VOL}$ | <br>50<br>25 | <br>200<br>100 | <br>–<br>– | <br>20<br>15 | <br>200<br>100 | <br>–<br>– | V/mV |
| Common Mode Rejection Ratio | CMRR | 70 | 90 | – | 70 | 90 | – | dB |
| Power Supply Rejection Ratio | PSRR | – | 30 | 150 | – | 30 | 150 | µV/V |
| Output Voltage<br>($R_L$ = 10 kΩ)<br>($R_L$ = 2.0 kΩ)<br>($R_L$ = 2.0 kΩ, $T_A$ = $T_{low}$ to $T_{high}$)<br>(Note 4) | $V_O$ | <br>±12<br>±10<br>±10 | <br>±13.5<br>±13<br>– | <br>–<br>–<br>– | <br>±12<br>±10<br>±10 | <br>±13.5<br>±13<br>– | <br>–<br>–<br>– | Vdc |
| Output Short-Circuit Current | $I_{OS}$ | ±10 | ±30 | ±45 | ±10 | ±20 | ±45 | mA |
| Power Supply Current (Notes 2 and 3) | $I_{CC}, I_{EE}$ | – | 2.8 | 4.0 | – | 2.8 | 7.0 | mA |
| Phase Margin | $\phi m$ | – | 60 | – | – | 60 | – | Degrees |
| Small-Signal Bandwidth<br>($A_V$ = 1, $R_L$ = 10 kΩ, $V_O$ = 50 mV) | BW | – | 1.0 | – | – | 1.0 | – | MHz |
| Power Bandwidth<br>($A_V$ = 1, $R_L$ = 2.0 kΩ, $V_O$ = 20 V (p-p), THD = 5%) | $BW_P$ | – | 9.0 | – | – | 9.0 | – | kHz |
| Rise Time/Fall Time | $t_{TLH}, t_{THL}$ | – | 0.35 | – | – | 0.35 | – | µs |
| Overshoot ($A_V$ = 1, $R_L$ = 10 kΩ, $V_O$ = 50 mV) | OS | – | 20 | – | – | 20 | – | % |
| Slew Rate | SR | – | 0.6 | – | – | 0.6 | – | V/µs |

**NOTES:**
1. Output will swing to ground
2. Not to exceed maximum package power dissipation.
3. For Operational Amplifier and Comparator.
4. $T_{low}$ = -55°C for MC3505 $T_{high}$ = +125°C for MC3505
= 0°C for MC3405 = +70°C for MC3405

## COMPARATOR SECTION

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage—Single Supply | $V_{CC}$ | 36 | Vdc |
| Split Supplies | $V_{CC}, V_{EE}$ | ±18 | |
| Input Differential Voltage Range | $V_{IDR}$ | ±36 | Vdc |
| Input Common Mode Voltage Range | $V_{ICR}$ | −0.3 to +36 | Vdc |
| Sink Current | $I_{sink}$ | 20 | mA |
| Operating Ambient Temperature Range—MC3505 | $T_A$ | −55 to +125 | °C |
| MC3405 | | 0 to +70 | |
| Storage Temperature Range—Ceramic Package | $T_{stg}$ | −65 to +150 | °C |
| Plastic Package | | −55 to +125 | |
| Operating Junction Temperature Range—Ceramic Package | $T_J$ | 175 | °C |
| Plastic Package | | 150 | |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = Gnd, $T_A$ = 25°C unless otherwise noted)

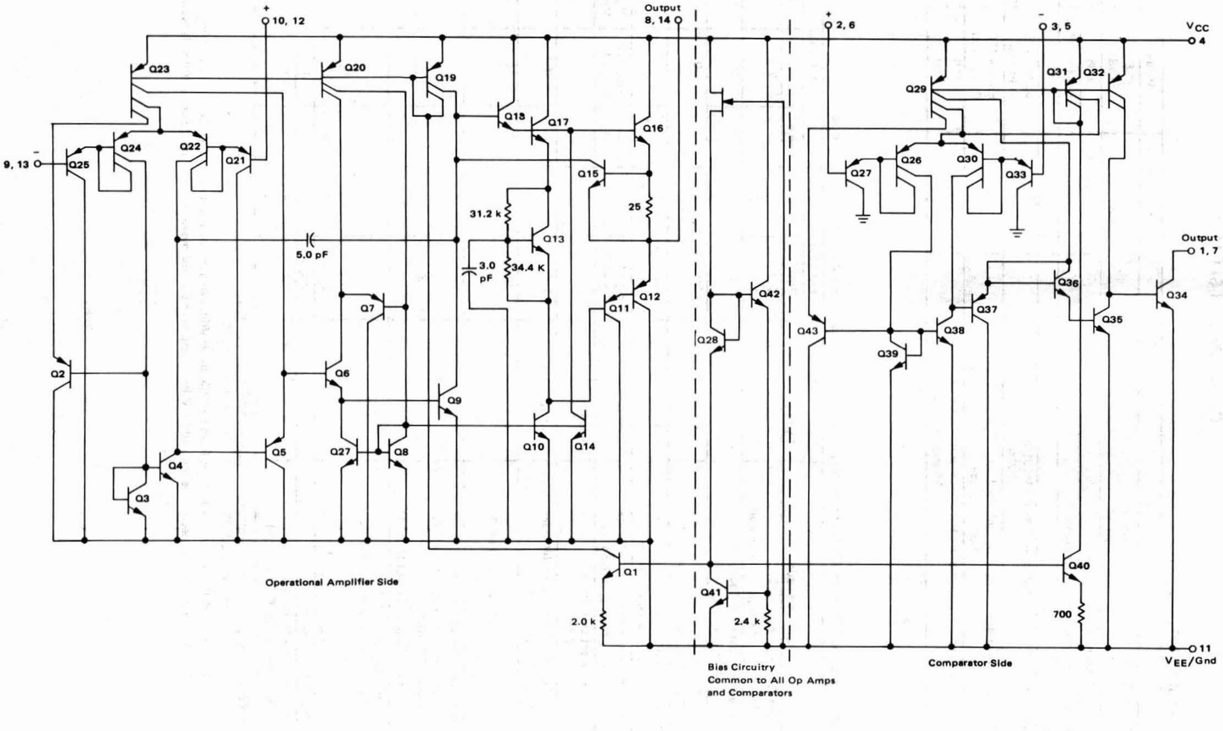
| Characteristic | Symbol | MC3505 | | | MC3405 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{IO}$ | – | 2.0 | 5.0 | – | 2.0 | 10 | mV |
| ($T_A$ = $T_{low}$ to $T_{high}$) (Notes 1 and 2) | | – | – | 9.0 | – | – | 12 | |
| Average Temperature Coefficient of Input Offset Voltage | $\Delta V_{IO}/\Delta T$ | – | 15 | – | – | 15 | – | μV/°C |
| Input Offset Current | $I_{IO}$ | – | 50 | 75 | – | 50 | 100 | nA |
| ($T_A$ = $T_{low}$ to $T_{high}$) (Note 1) | | – | – | 150 | – | – | 200 | |
| Input Bias Current | $I_{IB}$ | – | −125 | −500 | – | −125 | −500 | nA |
| ($T_A$ = $T_{low}$ to $T_{high}$) (Note 1) | | – | – | −1500 | – | – | −800 | |
| Input Common Mode Voltage Range | $V_{ICR}$ | 0 | $V_{CC}$ −1.5 | $V_{CC}$ −1.7 | 0 | $V_{CC}$ −1.5 | $V_{CC}$ −1.7 | Vp-p |
| ($T_A$ = $T_{low}$ to $T_{high}$) (Note 1) | | 0 | $V_{CC}$ −1.7 | $V_{CC}$ −2.0 | 0 | $V_{CC}$ −1.7 | $V_{CC}$ −2.0 | |
| Input Differential Voltage (All $V_{in} \geqslant 0$ Vdc) | $V_{ID}$ | – | – | 36 | – | – | 36 | V |
| Large-Signal Open-Loop Voltage Gain ($R_L$ = 15 kΩ) | $A_{VOL}$ | – | 200 | – | – | 200 | – | V/mV |
| Output Sink Current ($V_{in}(-) \geqslant 1.0$ Vdc, $V_{in}(+) = 0$, $V_O \leqslant 1.5$ V) | $I_{sink}$ | 6.0 | 16 | – | 6.0 | 16 | – | mA |
| Low Level Output Voltage ($V_{in}(+) = 0$ V, $V_{in}(-) = 1.0$ V, $I_{sink}$ = 4.0 mA) | $V_{OL}$ | – | 350 | 500 | – | 350 | 500 | mV |
| ($T_A$ = $T_{low}$ to $T_{high}$) (Note 1) | | – | – | 700 | – | – | 700 | |
| Output Leakage Current ($V_{in}(+) \geqslant 1.0$ Vdc, $V_{in}(-) = 0$, $V_O$ = 5.0 Vdc) | $I_{OL}$ | – | 0.1 | 1.0 | – | 0.1 | 1.0 | μA |
| ($T_A$ = $T_{low}$ to $T_{high}$) (Note 1) | | – | 0.1 | 1.0 | – | 0.1 | 1.0 | |
| Large-Signal Response | – | – | 300 | – | – | 300 | – | ns |
| Response Time (Note 3) ($V_{RL}$ = 5.0 Vdc, $R_L$ = 5.1 kΩ) | – | – | 1.3 | – | – | 1.3 | – | μs |

**NOTES:** 1. $T_{low}$ = −55°C for MC3505 $T_{high}$ = +125°C for MC3505
= 0°C for MC3405 = +70°C for MC3405

2. $V_O \cong 1.4$ V, $R_S$ = 0 Ω with $V_{CC}$ from 5.0 Vdc to 30 Vdc, and over the input common mode range 0 to $V_{CC}$ − 1.7 V.

3. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals 300 ns is typical.

## CIRCUIT SCHEMATIC
## (1/2 OF CIRCUIT SHOWN)


+
10, 12
Output
8, 14
+
2, 6
−
3, 5
VCC
4
Q23
Q20
Q19
Q18
Q17
Q16
Q29
Q31
Q32
−
9, 13
Q25
Q24
Q22
Q21
Q15
Q27
Q26
Q30
Q33
31.2 k
25
Q13
5.0 pF
3.0 pF
34.4 K
Output
1, 7
Q7
Q11
Q12
Q42
Q36
Q34
Q37
Q35
Q43
Q38
Q28
Q39
Q2
Q6
Q9
Q10
Q14
Q5
Q27
Q8
Q4
Q3
Q1
Q40
Operational Amplifier Side
Q41
2.0 k
2.4 k
700
11
VEE/Gnd
Bias Circuitry
Common to All Op Amps
and Comparators
Comparator Side

## OPERATIONAL AMPLIFIER SECTION

### TYPICAL PERFORMANCE CURVES

**FIGURE 1 – SINE WAVE RESPONSE**

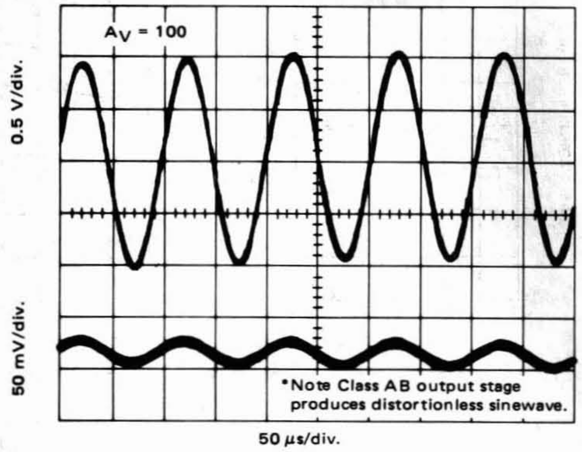


**FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE**

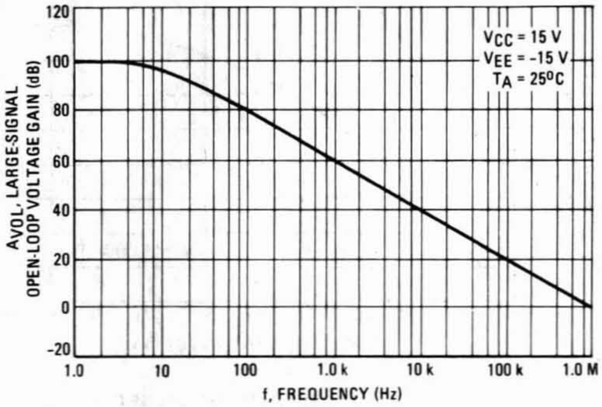


**FIGURE 3 – POWER BANDWIDTH**

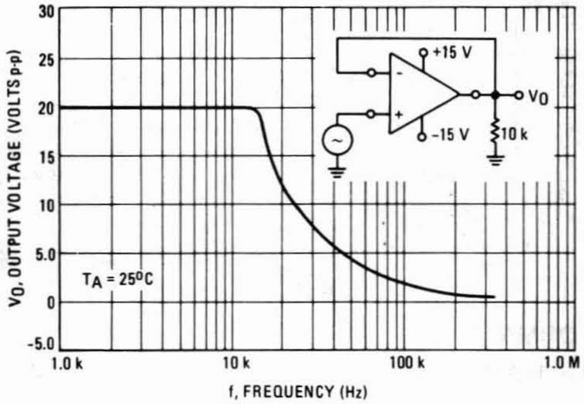


**FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE**

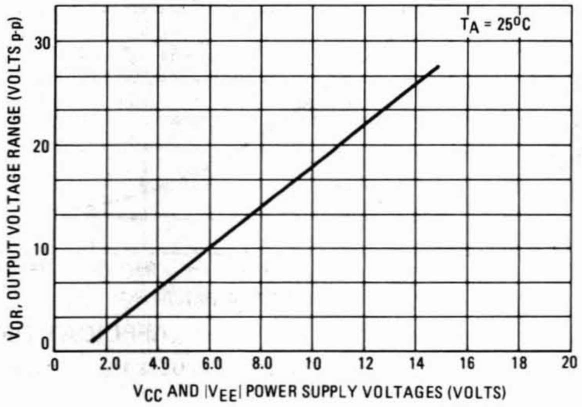


**FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE**

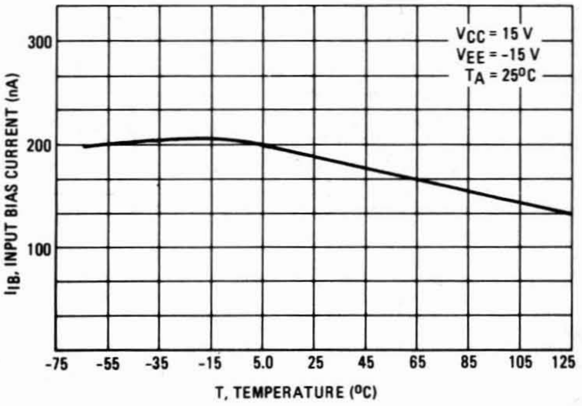
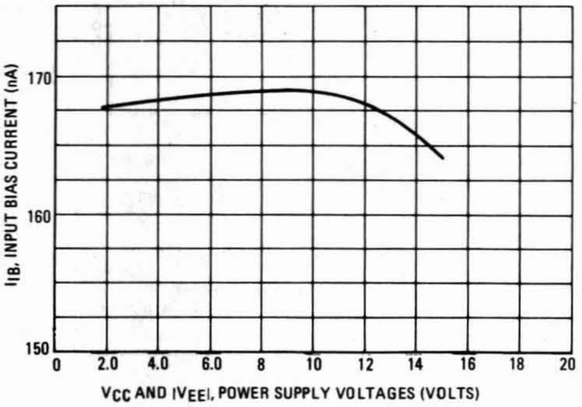


**FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE**



## COMPARATOR SECTION

### TYPICAL PERFORMANCE CURVES

FIGURE 7 – NORMALIZED INPUT OFFSET VOLTAGE

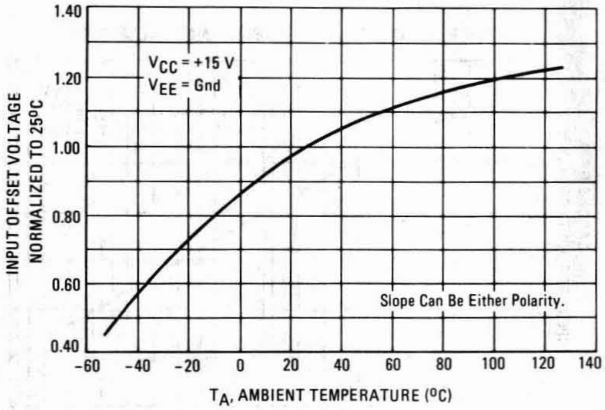


FIGURE 8 – INPUT BIAS CURRENT

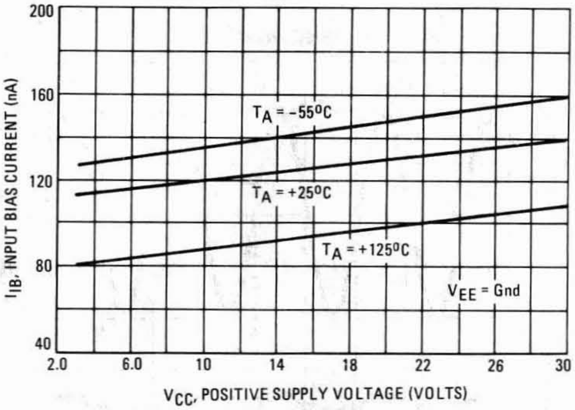


FIGURE 9 – NORMALIZED INPUT OFFSET CURRENT

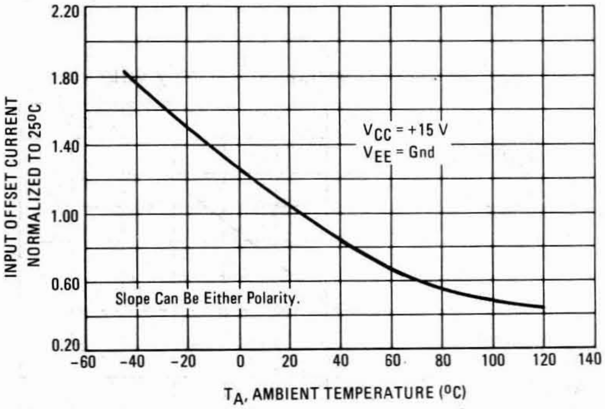
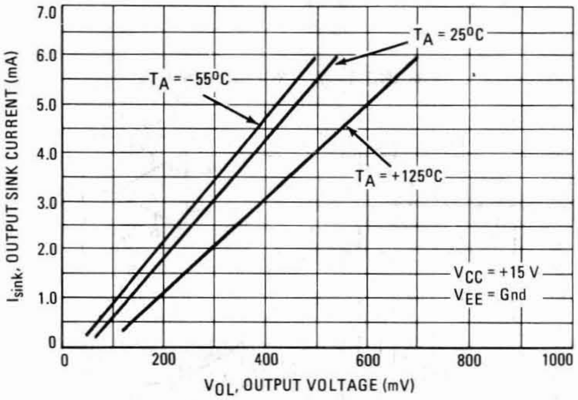
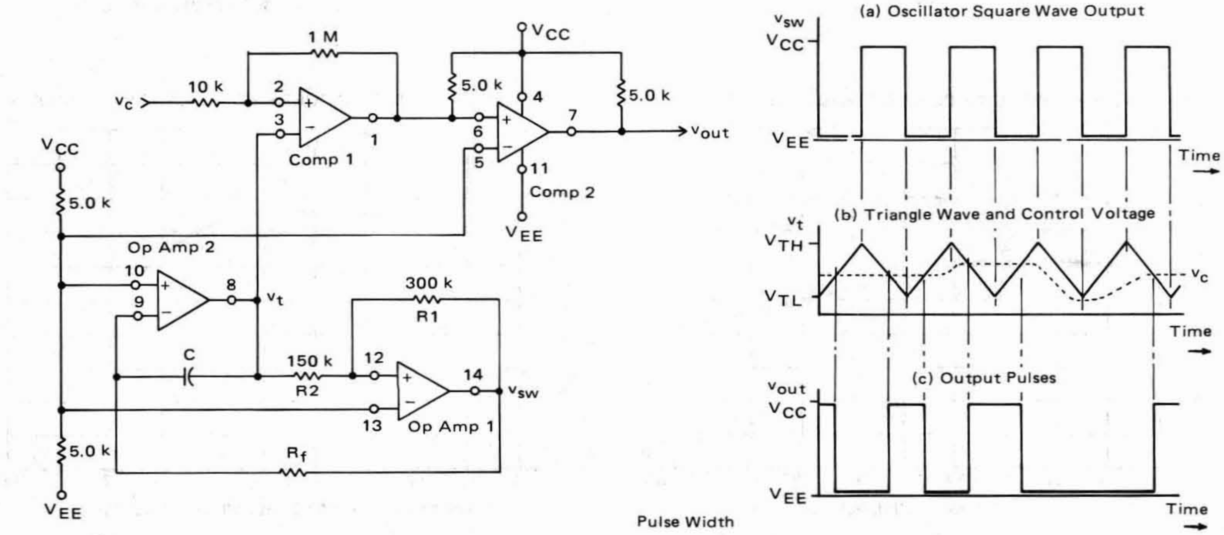


FIGURE 10 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



## APPLICATIONS INFORMATION

FIGURE 11 – PULSE WIDTH MODULATOR SCHEMATIC AND WAVEFORMS


1 M
10 k
$v_c$
2
3
Comp 1
1
$V_{CC}$
5.0 k
4
5.0 k
6
5
7
11
$v_{out}$
Comp 2
$V_{EE}$
$V_{CC}$
5.0 k
Op Amp 2
10
9
8
$v_t$
300 k
R1
C
150 k
R2
12
14
$v_{sw}$
13
Op Amp 1
5.0 k
$R_f$
$V_{EE}$
(a) Oscillator Square Wave Output
$v_{sw}$
$V_{CC}$
$V_{EE}$
Time
(b) Triangle Wave and Control Voltage
$v_t$
$V_{TH}$
$V_{TL}$
$v_c$
Time
(c) Output Pulses
$v_{out}$
$V_{CC}$
$V_{EE}$
Time

$V_{TH} = \frac{1}{2}V_S(1 + R2/R1) + V_{EE}$ $\quad V_S = V_{CC} - V_{EE}$

$V_{TL} = \frac{1}{2}V_S(1 - R2/R1) + V_{EE}$

Oscillator Frequency

$$f = \frac{R1}{4R_fCR2}$$

Pulse Width

$$P.W. = \left(\frac{1}{f}\right)\left(\frac{v_c - V_{TL}}{V_{TH} - V_{TL}}\right) \quad \text{When: } V_{TL} < V_C < V_{TH}$$

Duty Cycle in %

$$D.C. = \left(\frac{v_c - V_{TL}}{V_{TH} - V_{TL}}\right)(100)$$

FIGURE 12 – WINDOW COMPARATOR

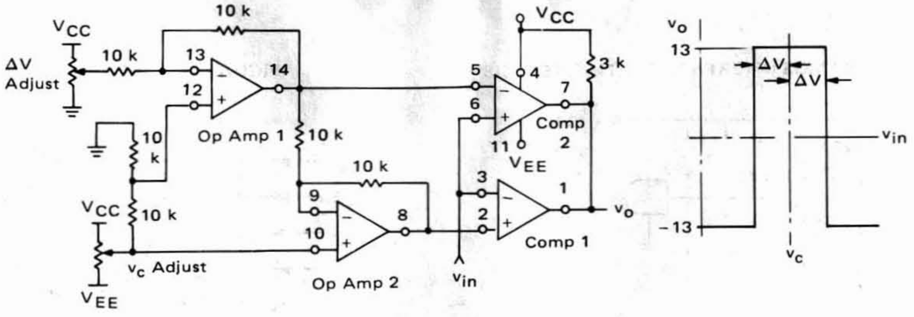
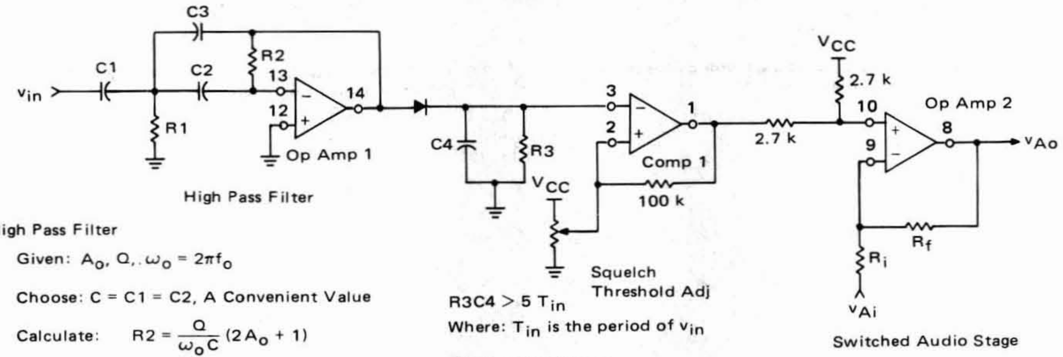

VCC
ΔV Adjust
10 k
13
12
14
Op Amp 1
10 k
10 k
10 k
VCC
vc Adjust
VEE
9
10
8
Op Amp 2
5
6
4
7
Comp 2
11
VEE
3 k
3
2
1
Comp 1
vin
vo
13
ΔV
ΔV
vin
−13
vc

FIGURE 13 – SQUELCH CIRCUIT FOR AM OR FM


vin
C1
C3
C2
R2
13
12
14
R1
Op Amp 1
High Pass Filter
C4
R3
VCC
Squelch Threshold Adj
3
2
1
Comp 1
100 k
VCC
2.7 k
2.7 k
10
9
8
Op Amp 2
vAo
Rf
Ri
vAi
Switched Audio Stage

High Pass Filter

Given: $A_o$, Q, $\omega_o = 2\pi f_o$

Choose: C = C1 = C2, A Convenient Value

Calculate: $R2 = \frac{Q}{\omega_o C}(2A_o + 1)$

$C3 = \frac{C}{A_o}$

$R1 = \frac{A_o}{Q\omega_o C(2A_o + 1)}$

$R3C4 > 5\ T_{in}$

Where: $T_{in}$ is the period of $v_{in}$

Q = Quality Factor

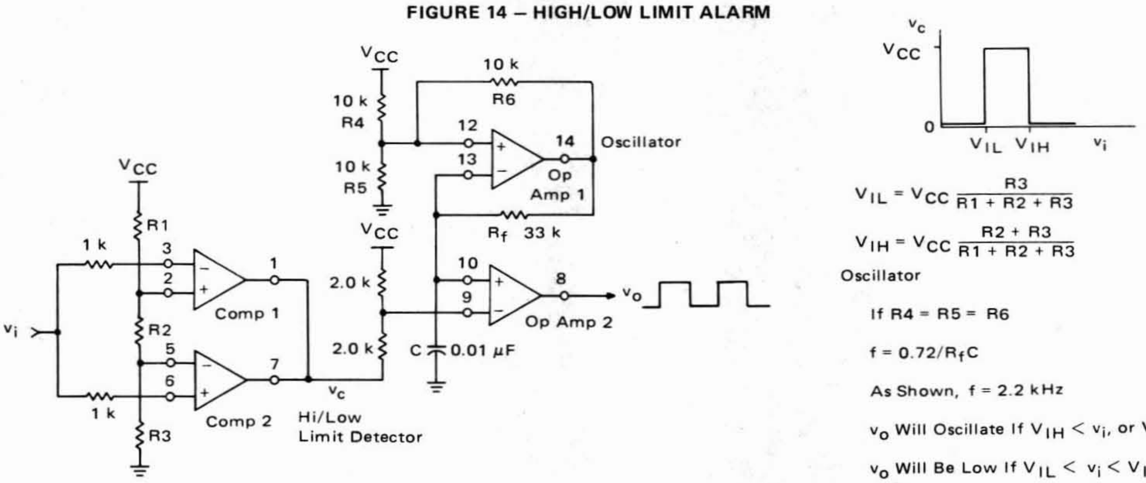
$A_o$ = High Frequency Gain

$\omega_o$ = Break Frequency

Gain of Audio Stage

$A_{cl} = -\frac{R_f}{R_i}$

FIGURE 14 – HIGH/LOW LIMIT ALARM


VCC
10 k R4
10 k R5
10 k R6
12
13
14
Oscillator
Op Amp 1
Rf 33 k
VCC
2.0 k
2.0 k
C 0.01 μF
10
9
8
Op Amp 2
vo
VCC
R1
1 k
3
2
1
Comp 1
vi
R2
5
6
7
Comp 2
1 k
R3
vc
Hi/Low Limit Detector
vc
VCC
0
VIL
VIH
vi

$V_{IL} = V_{CC}\frac{R3}{R1 + R2 + R3}$

$V_{IH} = V_{CC}\frac{R2 + R3}{R1 + R2 + R3}$

Oscillator

If R4 = R5 = R6

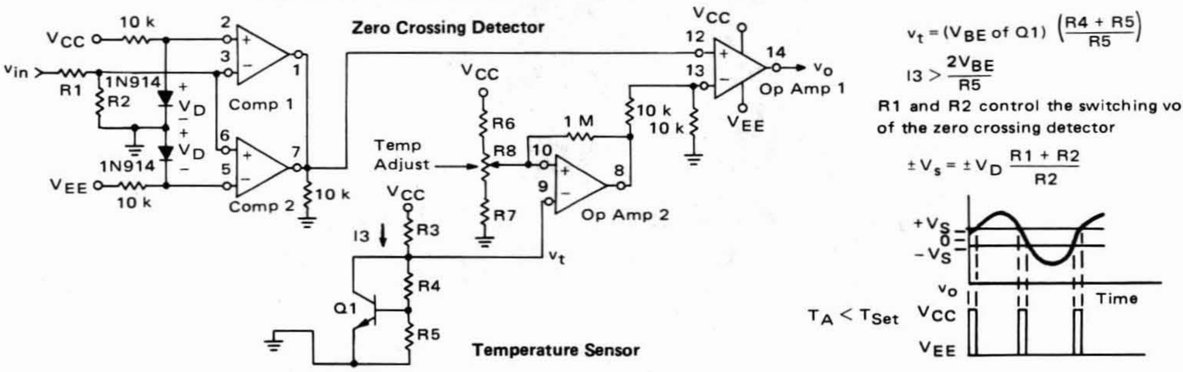
$f = 0.72/R_fC$

As Shown, f = 2.2 kHz

$v_o$ Will Oscillate If $V_{IH} < v_i$, or $V_{IL} > v_i$

$v_o$ Will Be Low If $V_{IL} < v_i < V_{IH}$

FIGURE 15 – ZERO CROSSING DETECTOR WITH TEMPERATURE SENSOR


Zero Crossing Detector
VCC
10 k
vin
R1
1N914
R2
VD
VD
1N914
VEE
10 k
2
3
1
Comp 1
6
5
7
Comp 2
10 k
VCC
R6
Temp Adjust
R8
R7
1 M
10
9
8
Op Amp 2
10 k
10 k
VCC
12
13
14
vo
Op Amp 1
VEE
VCC
I3
R3
R4
R5
Q1
vt
Temperature Sensor
+VS
0
−VS
vo
TA < TSet
VCC
VEE
Time

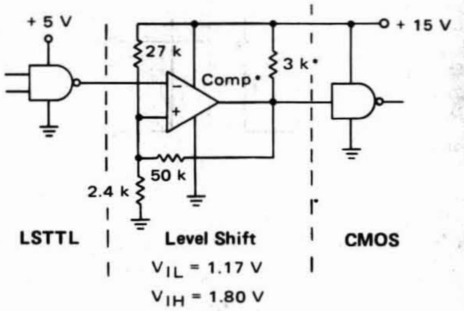
$v_t = (V_{BE}\text{ of Q1})\left(\frac{R4 + R5}{R5}\right)$

$I3 > \frac{2V_{BE}}{R5}$

R1 and R2 control the switching voltage of the zero crossing detector

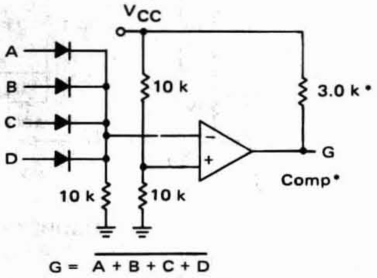
$\pm V_s = \pm V_D\,\frac{R1 + R2}{R2}$

**FIGURE 16 – LSTTL to CMOS INTERFACE WITH HYSTERESIS**


+5 V
27 k
3 k*
Comp*
+15 V
50 k
2.4 k
LSTTL
Level Shift
CMOS
$V_{IL}$ = 1.17 V
$V_{IH}$ = 1.80 V

*The same configuration may be used with an Op Amp if the 3 k resistor is removed.

**FIGURE 17 – "NOR" GATE**


$V_{CC}$
A
B
C
D
10 k
3.0 k*
G
Comp*
10 k
10 k
$G = \overline{A + B + C + D}$

*The same configuration may be used with an Op Amp if the 3 k resistor is removed.

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC3358P1 | −40°C to +85°C | Plastic DIP |
| MC3458D | 0°C to +70°C | SO-8 |
| MC3458G | 0°C to +70°C | Metal Can |
| MC3458P1 | 0°C to +70°C | Plastic DIP |
| MC3458U | 0°C to +70°C | Ceramic DIP |
| MC3558G | −55°C to +125°C | Metal Can |
| MC3558U | −55°C to +125°C | Ceramic DIP |

# MC3458
# MC3558
# MC3358

## Specifications and Applications Information

### DUAL LOW POWER OPERATIONAL AMPLIFIERS

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/$V_{EE}$, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The MC3558 Series is equivalent to one-half of a MC3503.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Class AB Output Stage for Minimum Crossover Distortion
- Single and Split Supply Operations Available
- Similar Performance to the Popular MC1558

**MAXIMUM RATINGS**

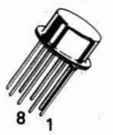
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltages | | | Vdc |
| Single Supply | $V_{CC}$ | 36 | |
| Split Supplies | $V_{CC}$ | +18 | |
| | $V_{EE}$ | −18 | |
| Input Differential Voltage Range (1) | $V_{IDR}$ | ±30 | Vdc |
| Input Common Mode Voltage Range (2) | $V_{ICR}$ | ±15 | Vdc |
| Input Forward Current ($V_I < -0.3$ V) | $I_{IF}$ | 50 | mA |
| Junction Temperature | $T_J$ | | °C |
| Ceramic and Metal Packages | | 175 | |
| Plastic Package | | 150 | |
| Storage Temperature Range | $T_{stg}$ | | °C |
| Ceramic and Metal Packages | | −65 to +150 | |
| Plastic Package | | −55 to +125 | |
| Operating Ambient Temperature Range | $T_A$ | | °C |
| MC3558 | | −55 to +125 | |
| MC3458 | | 0 to +70 | |
| MC3358 | | −40 to +85 | |

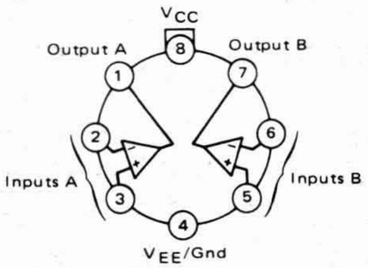
(1) Split Power Supplies.
(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

### DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

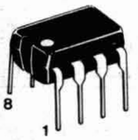
**SILICON MONOLITHIC INTEGRATED CIRCUIT**

**G SUFFIX**
METAL PACKAGE
CASE 601-04



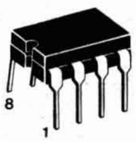


(Top View)

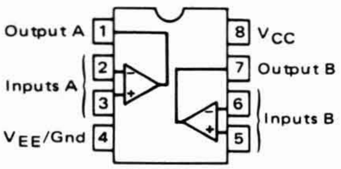


**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(MC3458, MC3358 only)

**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02



**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8



(Top View)

**ELECTRICAL CHARACTERISTICS** (For MC3558, MC3458, $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = 25°C unless otherwise noted.) (For MC3358, $V_{CC}$ = +14 V, $V_{EE}$ = Gnd, $T_A$ = 25°C, unless otherwise noted.)

| Characteristic | Symbol | MC3558 | | | MC3458 | | | MC3358 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage<br>$T_A = T_{high}$ to $T_{low}$ (1) | $V_{IO}$ | –<br>– | 2.0<br>– | 5.0<br>6.0 | –<br>– | 2.0<br>– | 10<br>12 | –<br>– | 2.0<br>– | 8.0<br>10 | mV |
| Input Offset Current<br>$T_A = T_{high}$ to $T_{low}$ | $I_{IO}$ | –<br>– | 30<br>– | 50<br>200 | –<br>– | 30<br>– | 50<br>200 | –<br>– | 30<br>– | 75<br>250 | nA |
| Large Signal Open-Loop Voltage Gain<br>$V_O = \pm 10$ V, $R_L = 2.0$ kΩ,<br>$T_A = T_{high}$ to $T_{low}$ | $A_{VOL}$ | <br>50<br>25 | <br>200<br>300 | <br>–<br>– | <br>20<br>15 | <br>200<br>– | <br>–<br>– | <br>20<br>15 | <br>200<br>– | <br>–<br>– | V/mV |
| Input Bias Current<br>$T_A = T_{high}$ to $T_{low}$ | $I_{IB}$ | –<br>– | -200<br>-300 | -500<br>-1500 | –<br>– | -200<br>– | -500<br>-800 | –<br>– | -200<br>– | -500<br>-1000 | nA |
| Output Impedance<br>f = 20 Hz | $z_o$ | – | 75 | – | – | 75 | – | – | 75 | – | Ω |
| Input Impedance<br>f = 20 Hz | $z_i$ | 0.3 | 1.0 | – | 0.3 | 1.0 | – | 0.3 | 1.0 | – | MΩ |
| Output Voltage Range<br>$R_L = 10$ kΩ<br>$R_L = 2.0$ kΩ<br>$R_L = 2.0$ kΩ, $T_A = T_{high}$ to $T_{low}$ | $V_{OR}$ | <br>±12<br>±10<br>±10 | <br>±13.5<br>±13<br>– | <br>–<br>–<br>– | <br>±12<br>±10<br>±10 | <br>±13.5<br>±13<br>– | <br>–<br>–<br>– | <br>12<br>10<br>10 | <br>12.5<br>12<br>– | <br>–<br>–<br>– | V |
| Input Common-Mode Voltage Range | $V_{ICR}$ | +13 V $-V_{EE}$ | +13.5 V $-V_{EE}$ | – | +13 V $-V_{EE}$ | +13.5 V $-V_{EE}$ | – | +12 V $-V_{EE}$ | +12.5 V $-V_{EE}$ | – | V |
| Common-Mode Rejection Ratio<br>$R_S \leq 10$ kΩ | CMRR | 70 | 90 | – | 70 | 90 | – | 70 | 90 | – | dB |
| Power Supply Current ($V_o$ = 0)<br>$R_L = \infty$ | $I_{CC}, I_{EE}$ | – | 1.6 | 2.2 | – | 1.6 | 3.7 | – | 1.6 | 3.7 | mA |
| Individual Output Short-Circuit Current (2) | $I_{OS}$ | ±10 | ±30 | ±45 | ±10 | ±20 | ±45 | ±10 | ±30 | ±45 | mA |
| Positive Power Supply Rejection Ratio | PSRR+ | – | 30 | 150 | – | 30 | 150 | – | 30 | 150 | µV/V |
| Negative Power Supply Rejection Ratio | PSRR− | – | 30 | 150 | – | 30 | 150 | – | – | – | µV/V |
| Average Temperature Coefficient of Input Offset Current<br>$T_A = T_{high}$ to $T_{low}$ | $\Delta I_{IO}/\Delta T$ | – | 50 | – | – | 50 | – | – | 50 | – | pA/°C |
| Average Temperature Coefficient of Input Offset Voltage<br>$T_A = T_{high}$ to $T_{low}$ | $\Delta V_{IO}/\Delta T$ | – | 10 | – | – | 10 | – | – | 10 | – | µV/°C |
| Power Bandwidth<br>$A_V = 1$, $R_L = 2.0$ kΩ, $V_o = 20$ V(p-p), THD = 5% | $BW_p$ | – | 9.0 | – | – | 9.0 | – | – | 9.0 | – | kHz |
| Small-Signal Bandwidth<br>$A_V = 1$, $R_L = 10$ kΩ, $V_o = 50$ mV | BW | – | 1.0 | – | – | 1.0 | – | – | 1.0 | – | MHz |
| Slew Rate<br>$A_V = 1$, $V_i = -10$ V to +10 V | SR | – | 0.6 | – | – | 0.6 | – | – | 0.6 | – | V/µs |
| Rise Time<br>$A_V = 1$, $R_L = 10$ kΩ, $V_o = 50$ mV | $t_{TLH}$ | – | 0.35 | – | – | 0.35 | – | – | 0.35 | – | µs |
| Fall Time<br>$A_V = 1$, $R_L = 10$ kΩ, $V_o = 50$ mV | $t_{THL}$ | – | 0.35 | – | – | 0.35 | – | – | 0.35 | – | µs |
| Overshoot<br>$A_V = 1$, $R_L = 10$ kΩ, $V_o = 50$ mV | OS | – | 20 | – | – | 20 | – | – | 20 | – | % |
| Phase Margin<br>$A_V = 1$, $R_L = 2.0$ kΩ, $C_L = 200$ pF | $\phi m$ | – | 60 | – | – | 60 | – | – | 60 | – | Degrees |
| Crossover Distortion<br>($V_{in}$ = 30 mVp-p, $V_{out}$ = 2.0 Vp-p, f = 10 kHz) | – | – | 1.0 | – | – | 1.0 | – | – | 1.0 | – | % |

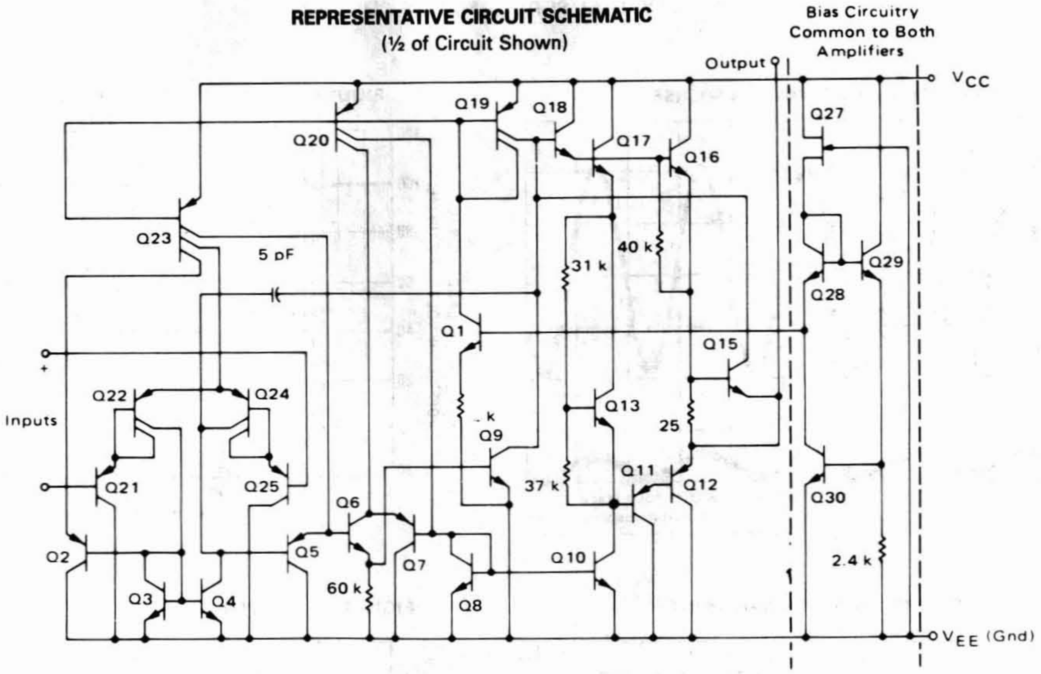
(1) $T_{high}$ = 125°C for MC3558, 70°C for MC3458, 85°C for MC3358.
$T_{low}$ = -55°C for MC3558, 0°C for MC3458, -40°C for MC3358.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = Gnd, $T_A$ = 25°C unless otherwise noted.)

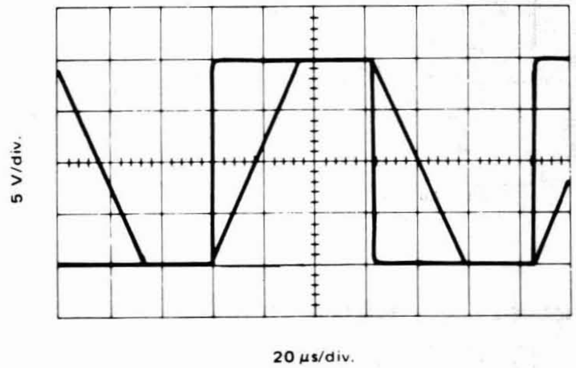
| Characteristic | Symbol | MC3558 | | | MC3458 | | | MC3358 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{IO}$ | – | 2.0 | 5.0 | – | 2.0 | 10 | – | 2.0 | 10 | mV |
| Input Offset Current | $I_{IO}$ | – | 30 | 50 | – | 30 | 50 | – | – | 75 | nA |
| Input Bias Current | $I_{IB}$ | – | -200 | -500 | – | -200 | -500 | – | – | -500 | nA |
| Large-Signal Open-Loop Voltage Gain<br>$R_L = 2.0$ kΩ | $A_{VOL}$ | 20 | 200 | – | 20 | 200 | – | 20 | 200 | – | V/mV |
| Power Supply Rejection Ratio | PSRR | – | – | 150 | – | – | 150 | – | – | 150 | µV/V |
| Output Voltage Range (3)<br>$R_L = 10$ kΩ, $V_{CC} = 5.0$ V<br>$R_L = 10$ kΩ, 5.0 V $\leq V_{CC} \leq$ 30 V | $V_{OR}$ | <br>3.3<br>– | <br>3.5<br>$V_{CC}$ − 1.7 V | <br>–<br>– | <br>3.3<br>– | <br>3.5<br>$V_{CC}$ − 1.7 V | <br>–<br>– | <br>3.3<br>– | <br>3.5<br>$V_{CC}$ − 1.7 V | <br>–<br>– | Vp-p |
| Power Supply Current | $I_{CC}$ | – | 2.5 | 4.0 | – | 2.5 | 7.0 | – | 2.5 | 4.0 | mA |
| Channel Separation<br>f = 1.0 kHz to 20 kHz (Input Referenced) | – | – | -120 | – | – | -120 | – | – | -120 | – | dB |

(2) Not to exceed maximum package power dissipation.
(3) Output will swing to ground

**REPRESENTATIVE CIRCUIT SCHEMATIC**
(½ of Circuit Shown)


Bias Circuitry
Common to Both
Amplifiers
Output
VCC
Q19
Q18
Q20
Q17
Q16
Q27
Q23
5 pF
40 k
31 k
Q29
Q28
Q1
Q15
+
Inputs
Q22
Q24
Q13
k
Q9
25
Q21
Q25
37 k
Q11
Q12
Q30
Q6
Q2
Q5
Q7
Q10
2.4 k
60 k
Q3
Q4
Q8
VEE (Gnd)

INVERTER PULSE RESPONSE



## CIRCUIT DESCRIPTION

The MC3558 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

## TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

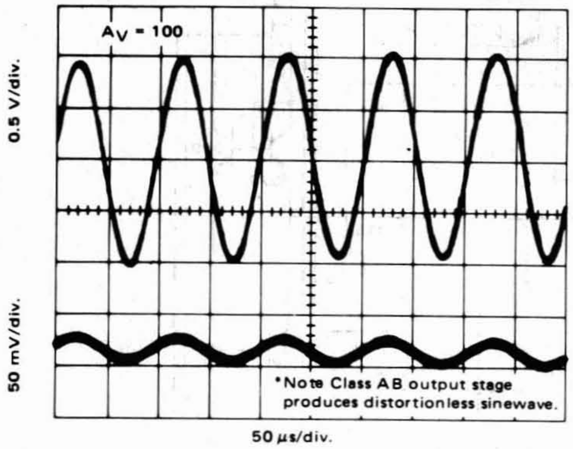


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

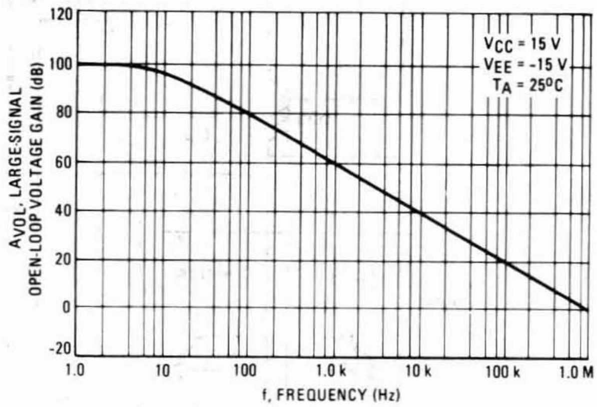


FIGURE 3 – POWER BANDWIDTH

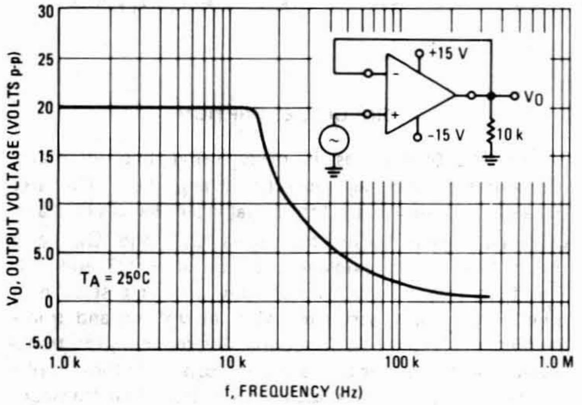


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

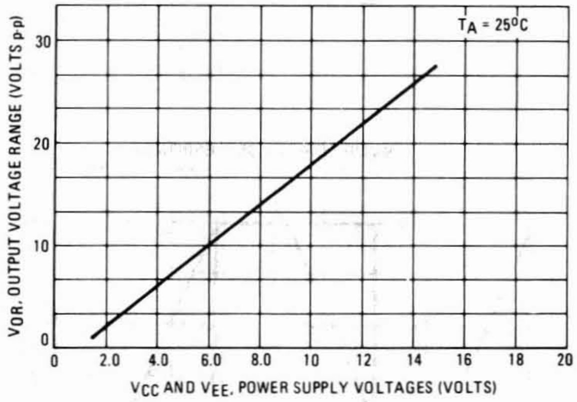


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

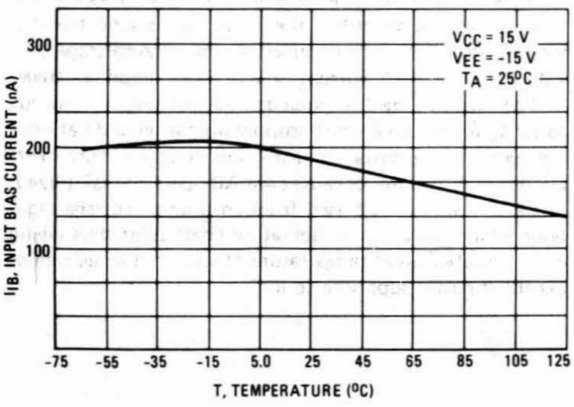
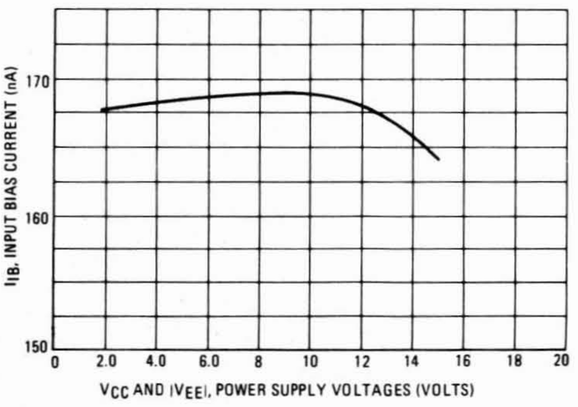
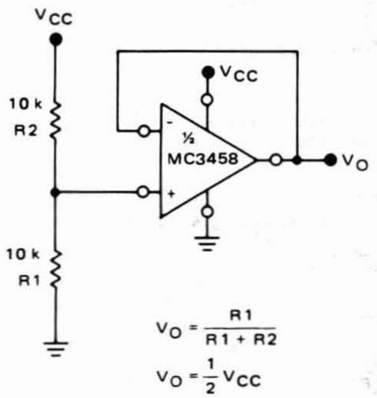


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



## APPLICATIONS INFORMATION

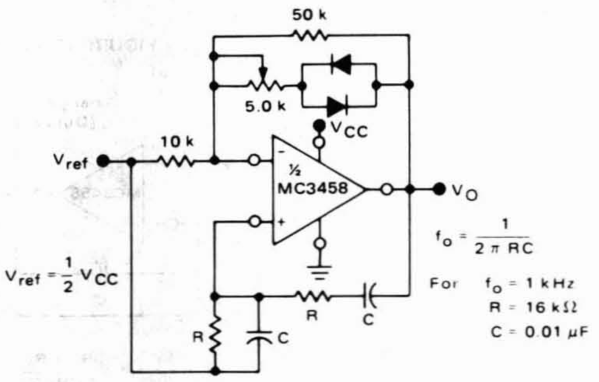
FIGURE 7 – VOLTAGE REFERENCE


VCC
10 k
R2
10 k
R1
VCC
½
MC3458
VO

$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

FIGURE 8 – WIEN BRIDGE OSCILLATOR

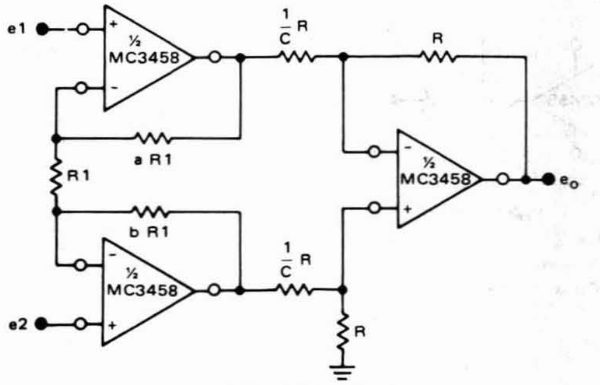

50 k
5.0 k
VCC
10 k
Vref
½
MC3458
VO
R
C
R
C

$V_{ref} = \frac{1}{2} V_{CC}$

$$f_o = \frac{1}{2 \pi RC}$$

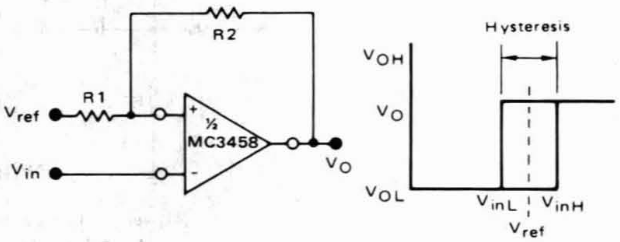
For $f_o$ = 1 kHz
R = 16 kΩ
C = 0.01 µF

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


e1
½
MC3458
1/C R
R
a R1
R1
b R1
½
MC3458
eo
½
MC3458
1/C R
e2
R

$e_o = C\ (1 + a + b)\ (e2 - e1)$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

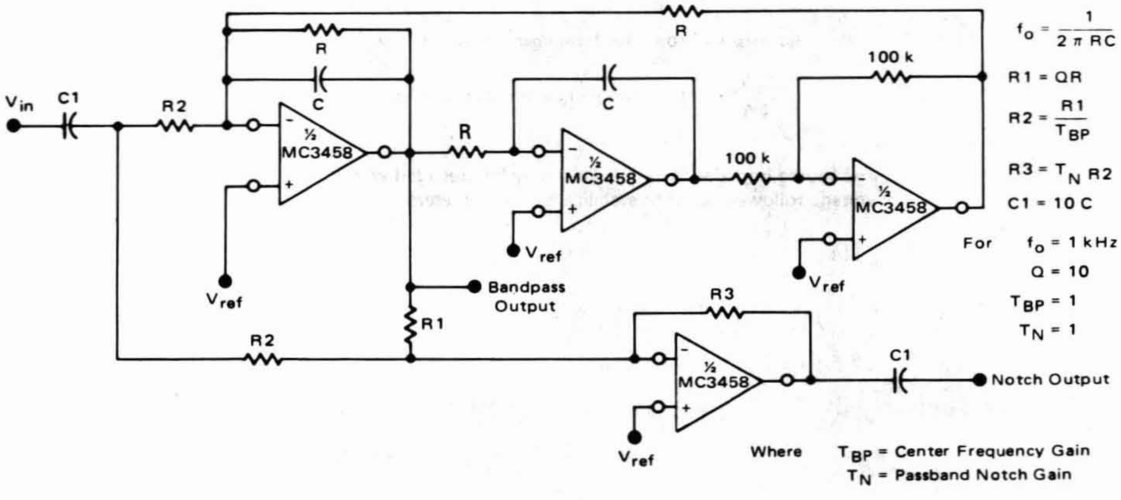

R2
R1
Vref
Vin
½
MC3458
VO
Hysteresis
VOH
VO
VOL
VinL
VinH
Vref

$$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER


Vin
C1
R2
R
C
R
½
MC3458
R
C
½
MC3458
100 k
100 k
½
MC3458
Vref
Vref
Vref
Bandpass Output
R1
R3
R2
½
MC3458
C1
Notch Output
Vref

$$f_o = \frac{1}{2 \pi RC}$$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N\ R2$

$C1 = 10\ C$

$V_{ref} = \frac{1}{2} V_{CC}$

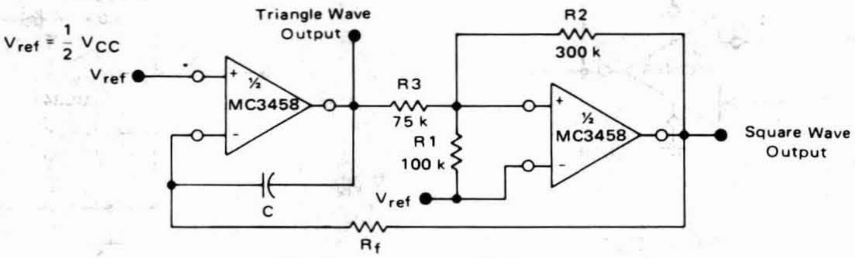
For $f_o$ = 1 kHz
Q = 10
$T_{BP} = 1$
$T_N = 1$

R = 160 kΩ
C = 0.001 µF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

Where $T_{BP}$ = Center Frequency Gain
$T_N$ = Passband Notch Gain

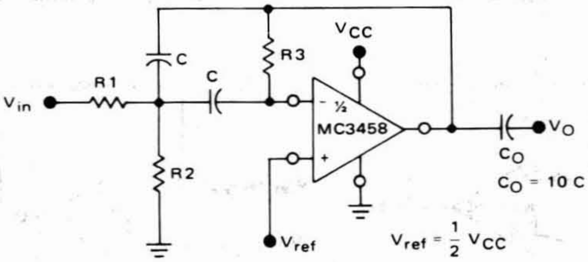
## APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR


Vref = 1/2 VCC
Vref
Triangle Wave Output
+
-
½ MC3458
R3
75 k
R1
100 k
Vref
C
Rf
R2
300 k
+
-
½ MC3458
Square Wave Output

$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER


VCC
C
R3
R1
C
Vin
-
+
½ MC3458
R2
Vref
VO
CO
CO = 10 C
Vref = 1/2 VCC

Given $f_o$ = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value $f_o$, C
Then:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2A(f_o)}$$

$$R2 = \frac{R1\ R3}{4Q^2\ R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1$$ Where $f_o$ and BW are expressed in Hz.

**If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.**

**MOTOROLA**

# MC3476

## LOW-COST PROGRAMMABLE OPERATIONAL AMPLIFIER

### SILICON MONOLITHIC INTEGRATED CIRCUIT

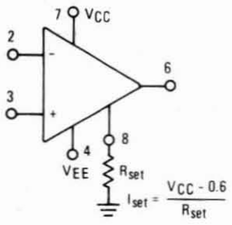
## LOW-COST PROGRAMMABLE OPERATIONAL AMPLIFIER

The MC3476 is a low-cost selection of the popular, industry-standard MC1776 programmable operational amplifier. This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the $I_{set}$ input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ±6.0 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

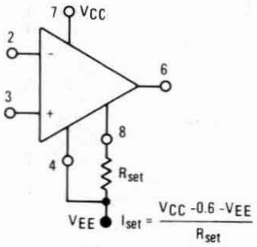
**RESISTIVE PROGRAMMING** (See Figure 1.)

**$R_{set}$ to GROUND**


7 VCC
2
3
6
8
4
VEE
Rset
Iset = (VCC - 0.6)/Rset

| Typical $R_{set}$ Values | | |
|---|---|---|
| $V_{CC}$, $V_{EE}$ | $I_{set}$ = 10 µA | $I_{set}$ = 15 µA |
| ±6.0 V | 560 kΩ | 360 kΩ |
| ±9.0 V | 820 kΩ | 560 kΩ |
| ±12 V | 1.0 MΩ | 750 kΩ |
| ±15 V | 1.5 MΩ | 1.0 MΩ |

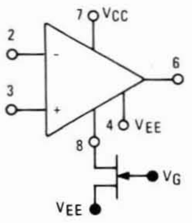
**$R_{set}$ to NEGATIVE SUPPLY**


7 VCC
2
3
6
8
4
Rset
VEE
Iset = (VCC -0.6 -VEE)/Rset

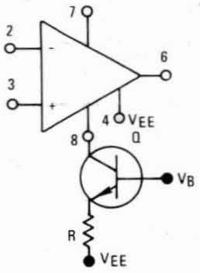
| Typical $R_{set}$ Values | | |
|---|---|---|
| $V_{CC}$, $V_{EE}$ | $I_{set}$ = 10 µA | $I_{set}$ = 15 µA |
| ±6.0 V | 1.0 MΩ | 820 kΩ |
| ±9.0 V | 1.8 MΩ | 1.2 MΩ |
| ±12 V | 2.2 MΩ | 1.5 MΩ |
| ±15 V | 2.7 MΩ | 2.0 MΩ |

**ACTIVE PROGRAMMING**

**FET CURRENT SOURCE**

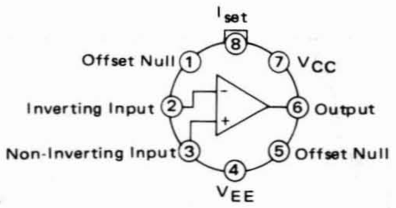

7 VCC
2
3
6
4 VEE
8
VG
VEE

**BIPOLAR CURRENT SOURCE**


7
2
3
6
4 VEE
8
Q
VB
R
VEE

Pins not shown are not connected.

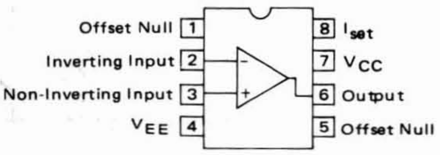
**G SUFFIX**
METAL PACKAGE
CASE 601-04


Iset
8
Offset Null 1
7 VCC
Inverting Input 2
6 Output
Non-Inverting Input 3
5 Offset Null
4
VEE

(Top View)

**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04

**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02


Offset Null 1
Inverting Input 2
Non-Inverting Input 3
VEE 4
8 Iset
7 VCC
6 Output
5 Offset Null

(Top View)

**ORDERING INFORMATION**

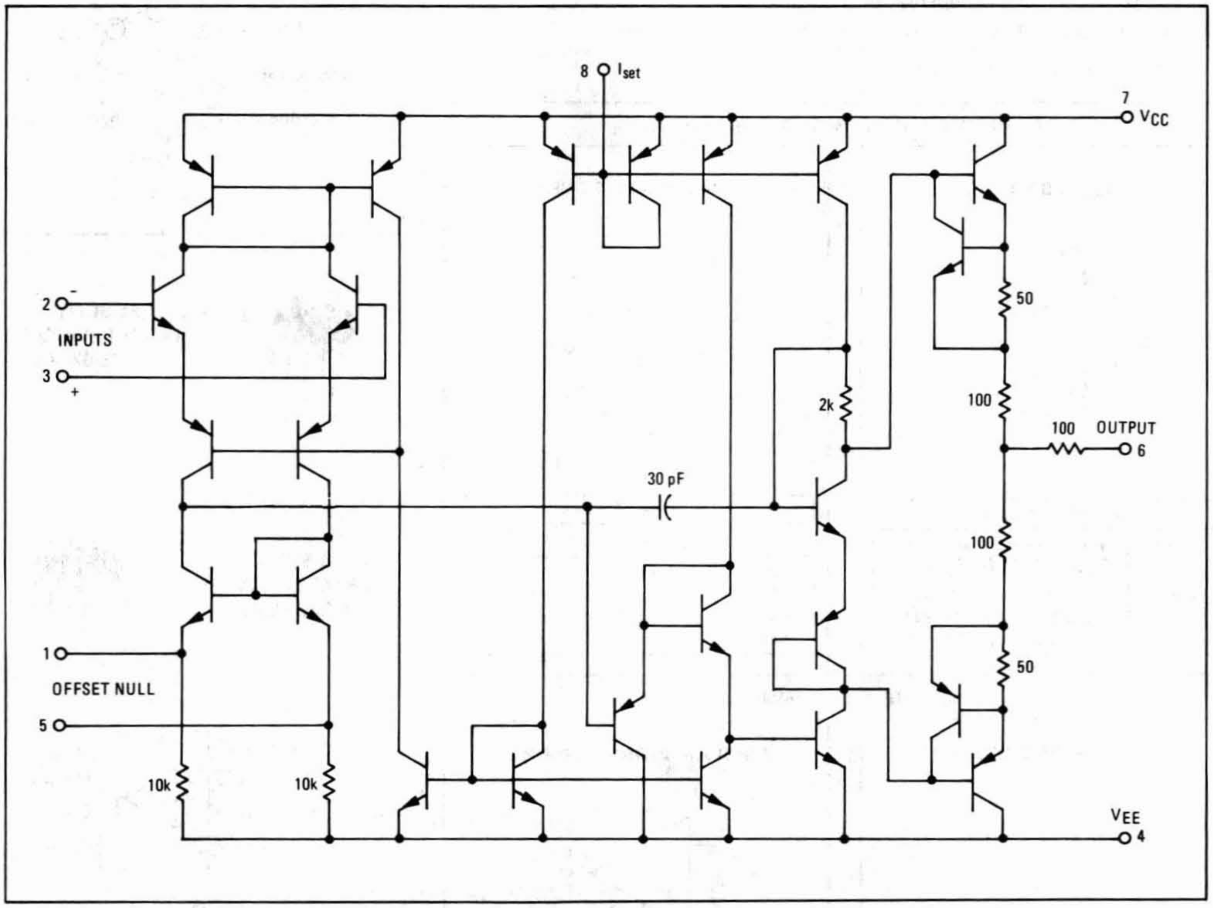
| Device | Temperature Range | Package |
|---|---|---|
| MC3476G | 0 to +70°C | Metal Can |
| MC3476P1 | 0 to +70°C | Plastic DIP |
| MC3476U | 0 to +70°C | Ceramic DIP |

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltages | $V_{CC}, V_{EE}$ | ±18 | Vdc |
| Input Differential Voltage Range | $V_{IDR}$ | ±30 | Vdc |
| Input Common-Mode Voltage Range | $V_{ICR}$ | $V_{CC}, V_{EE}$ | Vdc |
| Offset Null to $V_{EE}$ Voltage | $V_{off}-V_{EE}$ | ±0.5 | Vdc |
| Programming Current | $I_{set}$ | 200 | µA |
| Programming Voltage<br>(Voltage from $I_{set}$ terminal to ground) | $V_{set}$ | ($V_{CC}$−0.6 V)<br>to<br>$V_{CC}$ | Vdc |
| Output Short-Circuit Duration* | $t_S$ | Indefinite | s |
| Operating Ambient Temperature Range | $T_A$ | 0 to 70 | °C |
| Storage Temperature Range<br>Metal and Ceramic Packages<br>Plastic Package | $T_{stg}$ | <br>−65 to +150<br>−55 to +125 | °C |
| Junction Temperature<br>Metal and Ceramic Packages<br>Plastic Package | $T_J$ | <br>175<br>150 | °C |

*Short-Circuit to ground with $I_{set} \leq 15\ \mu A$. Rating applies up to ambient temperature of +70°C.

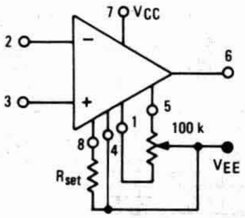
EQUIVALENT SCHEMATIC DIAGRAM



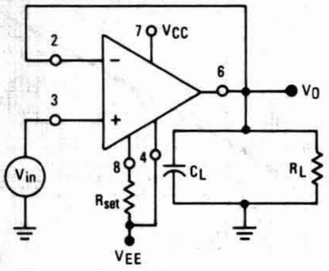
**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $I_{set}$ = 15 μA, $T_A$ = +25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Offset Voltage ($R_S \leqslant 10$ kΩ) | $V_{IO}$ | | | | mV |
| $T_A$ = +25°C | | – | 2.0 | 6.0 | |
| 0°C ⩽ $T_A$ ⩽ 70°C | | – | – | 7.5 | |
| Offset Voltage Adjustment Range | $V_{IOR}$ | – | 18 | – | mV |
| Input Offset Current | $I_{IO}$ | | | | nA |
| $T_A$ = +25°C | | – | 2.0 | 25 | |
| $T_A$ = 70°C | | – | – | 25 | |
| $T_A$ = 0°C | | – | – | 40 | |
| Input Bias Current | $I_{IB}$ | | | | nA |
| $T_A$ = +25°C | | – | 15 | 50 | |
| $T_A$ = 70°C | | – | – | 50 | |
| $T_A$ = 0°C | | – | – | 100 | |
| Input Resistance | $r_i$ | – | 5.0 | – | MΩ |
| Input Capacitance | $C_i$ | – | 2.0 | – | pF |
| Input Common-Mode Voltage Range<br>0°C ⩽ $T_A$ ⩽ 70°C | $V_{ICR}$ | ±10 | – | – | V |
| Large Signal Voltage Gain | $A_{VOL}$ | | | | V/V |
| $R_L \geqslant 10$ kΩ, $V_O$ = ±10 V, $T_A$ = +25°C | | 50 k | 400 k | – | |
| $R_L \geqslant 10$ kΩ, $V_O$ = ±10 V, 0°C ⩽ $T_A$ ⩽ 70°C | | 25 k | – | – | |
| Output Voltage Range | $V_{OR}$ | | | | V |
| $R_L \geqslant 10$ kΩ, $T_A$ = +25°C | | ±12 | ±13 | – | |
| $R_L \geqslant 10$ kΩ, 0°C ⩽ $T_A$ ⩽ 70°C | | ±12 | – | – | |
| Output Resistance | $r_o$ | – | 1.0 | – | kΩ |
| Output Short-Circuit Current | $I_{os}$ | – | 12 | – | mA |
| Common-Mode Rejection Ratio<br>$R_S \leqslant 10$ kΩ, 0°C ⩽ $T_A$ ⩽ 70°C | CMRR | 70 | 90 | – | dB |
| Supply Voltage Rejection Ratio<br>$R_S \leqslant 10$ kΩ, 0°C ⩽ $T_A$ ⩽ 70°C | PSRR | – | 25 | 200 | μV/V |
| Supply Current | $I_{CC}$, $I_{EE}$ | | | | μA |
| $T_A$ = +25°C | | – | 160 | 200 | |
| 0°C ⩽ $T_A$ ⩽ 70°C | | – | – | 225 | |
| Power Dissipation | $P_D$ | | | | mW |
| $T_A$ = +25°C | | – | 4.8 | 6.0 | |
| 0°C ⩽ $T_A$ ⩽ 70°C | | – | – | 6.75 | |
| Transient Response (Unity Gain)<br>$V_{in}$ = 20 mV, $R_L \geqslant 10$ kΩ, $C_L$ = 100 pF | | | | | |
| Rise Time | $t_{TLH}$ | – | 0.35 | – | μs |
| Overshoot | OS | – | 10 | – | % |
| Slew Rate ($R_L \geqslant 10$ kΩ) | SR | – | 0.8 | – | V/μs |

**VOLTAGE OFFSET NULL CIRCUIT**



**TRANSIENT-RESPONSE TEST CIRCUIT**



Pins not shown are not connected.

## TYPICAL CHARACTERISTICS

($T_A$ = +25°C unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

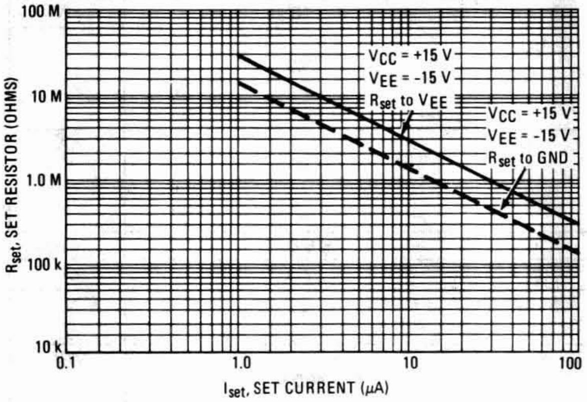


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

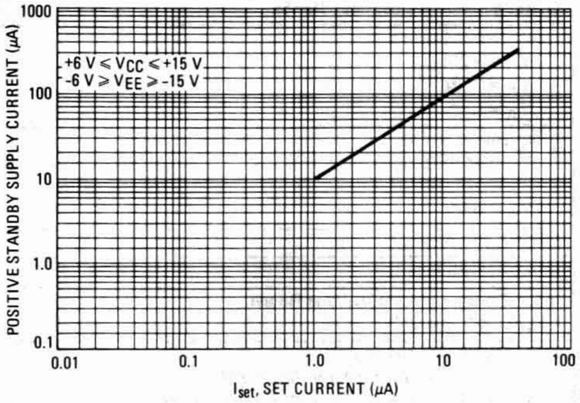


FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

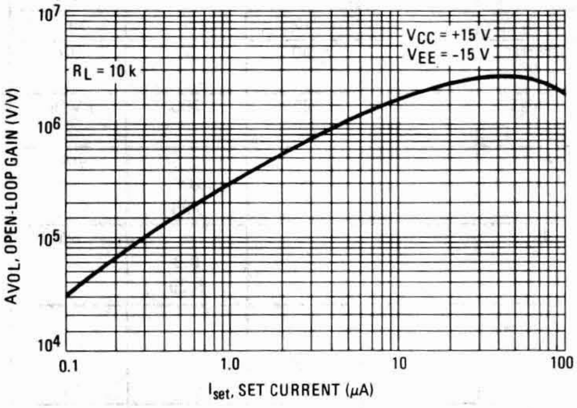


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

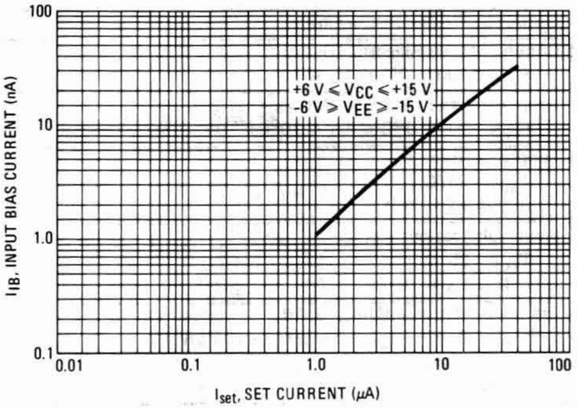


FIGURE 5 – SLEW RATE versus SET CURRENT

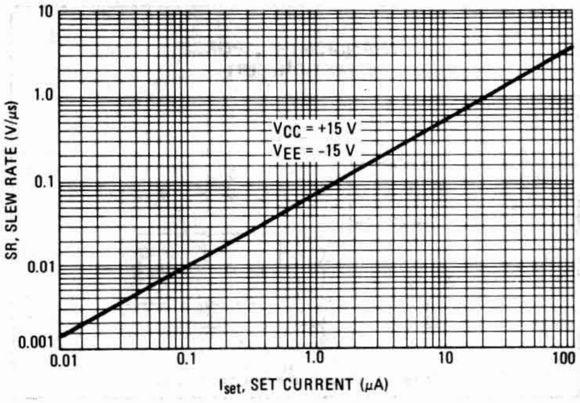
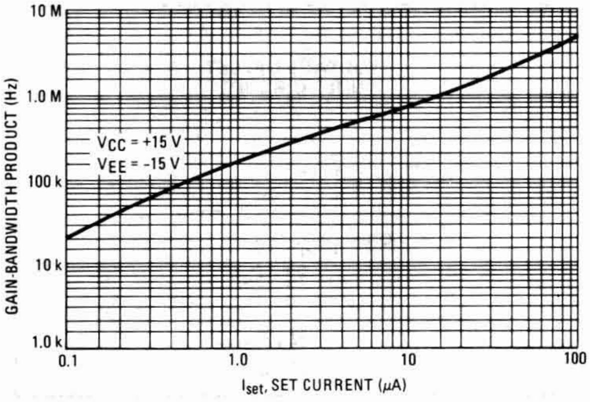


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



## TYPICAL CHARACTERISTICS (continued)

($T_A$ = +25°C unless otherwise noted.)

FIGURE 7 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

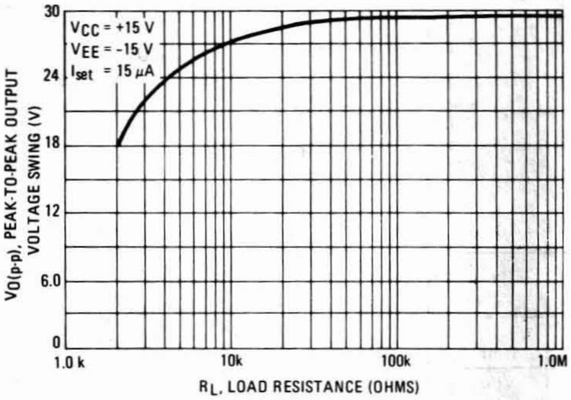
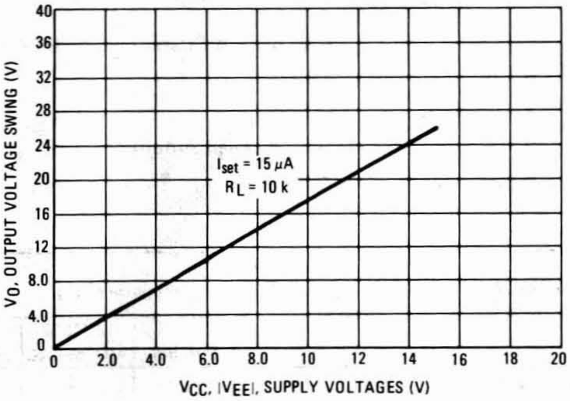


FIGURE 8 – OUTPUT SWING versus SUPPLY VOLTAGE



**MOTOROLA**

# MC4558, MC4558AC, MC4558C

## DUAL WIDEBAND OPERATIONAL AMPLIFIER

The MC4558, MC4558AC, and MC4558C combine all the outstanding features of the MC1458 and, in addition, possess three times the unity gain bandwidth of the industry standard.

- **2.5 MHz Unity Gain Bandwidth Guaranteed on MC4558 and MC4558AC**
- **2 MHz Unity Gain Bandwidth Guaranteed on MC4558C**
- Internally Compensated
- Short-Circuit Protection
- Gain and Phase Match between Amplifiers
- Low Power Consumption

### MAXIMUM RATINGS ($T_A = +25°C$ unless otherwise noted)

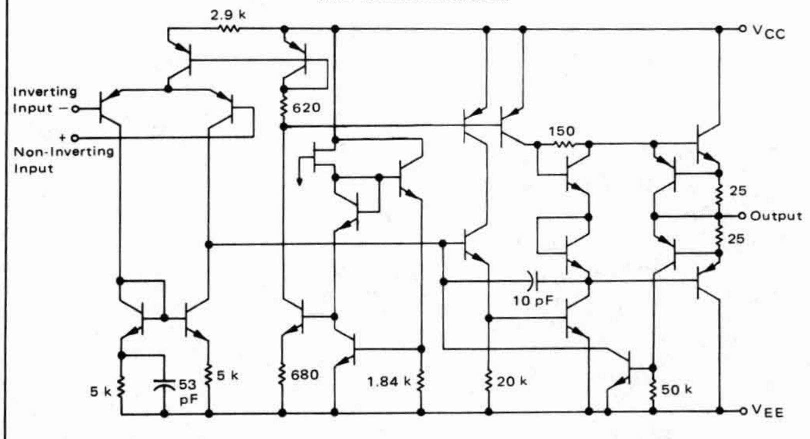
| Rating | Symbol | MC4558<br>MC4558AC | MC4558C | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +22<br>−22 | +18<br>−18 | Vdc<br>Vdc |
| Input Differential Voltage | $V_{ID}$ | ±30 | | Volts |
| Input Common Mode Voltage (Note 1) | $V_{ICM}$ | ±15 | | Volts |
| Output Short-Circuit Duration (Note 2) | $t_S$ | Continuous | | |
| Operating Ambient Temperature Range | $T_A$ | See Ordering Information Below | | |
| Storage Temperature Range<br>Metal and Ceramic Packages<br>Plastic Package | $T_{stg}$ | <br>−65 to +150<br>−55 to +125 | | °C |
| Junction Temperature<br>Metal and Ceramic Packages<br>Plastic Package | $T_J$ | <br>175<br>150 | | °C |

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Short circuit may be to ground or either supply.

### EQUIVALENT CIRCUIT SCHEMATIC

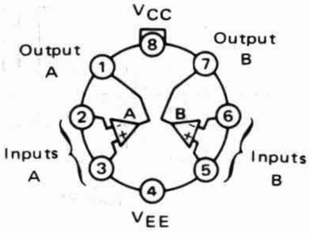
(1/2 of Circuit Shown)


2.9 k
$V_{CC}$
Inverting Input −
+
Non-Inverting Input
620
150
25
Output
25
10 pF
5 k
53 pF
5 k
680
1.84 k
20 k
50 k
$V_{EE}$

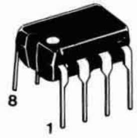
## DUAL WIDE BANDWIDTH OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

**G SUFFIX**
METAL PACKAGE
CASE 601-04

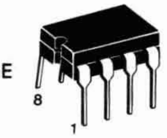

$V_{CC}$
Output A
Output B
8
1
7
2
A
B
6
Inputs A
Inputs B
3
5
4
$V_{EE}$

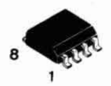
(Top View)



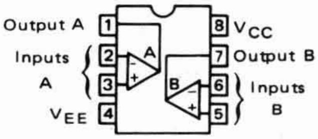
**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04

**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02





**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8


Output A 1
Inputs A 2
3
$V_{EE}$ 4
8 $V_{CC}$
7 Output B
6 Inputs B
5
A
B

(Top View)

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC4558G | −55 to +125°C | Metal Can |
| MC4558U | | Ceramic DIP |
| MC4558CD | 0 to +70°C | SO-8 |
| MC4558CG | | Metal Can |
| MC4558ACP1, CP1 | | Plastic DIP |
| MC4558CU | | Ceramic DIP |

**FREQUENCY CHARACTERISTICS** ($V_{CC}$ = 15 V, $V_{EE}$ = −15 V, $T_A$ = 25°C)

| Characteristic | Symbol | MC4558, MC4558AC | | | MC4558C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Unity Gain Bandwidth | BW | 2.5 | 2.8 | – | 2.0 | 2.8 | – | MHz |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $V_{EE}$ = −15 V, $T_A$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | MC4558, MC4558AC Min | Typ | Max | MC4558C Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage ($R_S \leq 10$ kΩ) | $V_{IO}$ | – | 1.0 | 5.0 | – | 2.0 | 6.0 | mV |
| Input Offset Current | $I_{IO}$ | – | 20 | 200 | – | 20 | 200 | nA |
| Input Bias Current† | $I_{IB}$ | – | 80 | 500 | – | 80 | 500 | nA |
| Input Resistance | $r_i$ | 0.3 | 2.0 | – | 0.3 | 2.0 | – | MΩ |
| Input Capacitance | $C_i$ | – | 1.4 | – | – | 1.4 | – | pF |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±12 | ±13 | – | ±12 | ±13 | – | V |
| Large Signal Voltage Gain ($V_O$ = ±10 V, $R_L$ = 2.0 kΩ) | $A_v$ | 50 | 200 | – | 20 | 200 | – | V/mV |
| Output Resistance | $r_o$ | – | 75 | – | – | 75 | – | Ω |
| Common Mode Rejection Ratio ($R_S \leq 10$ kΩ) | CMRR | 70 | 90 | – | 70 | 90 | – | dB |
| Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ) | PSRR | – | 30 | 150 | – | 30 | 150 | μV/V |
| Output Voltage Swing | $V_O$ | | | | | | | V |
| ($R_L \geq 10$ kΩ) | | ±12 | ±14 | – | ±12 | ±14 | – | |
| ($R_L \geq 2$ kΩ) | | ±10 | ±13 | – | ±10 | ±13 | – | |
| Output Short-Circuit Current | $I_{os}$ | 10 | 20 | 40 | 10 | 20 | 40 | mA |
| Supply Currents (Both Amplifiers) | $I_D$ | – | 2.3 | 5.0 | – | 2.3 | 5.6 | mA |
| Power Consumption (Both Amplifiers) | $P_C$ | – | 70 | 150 | – | 70 | 170 | mW |
| Transient Response (Unity Gain) | | | | | | | | |
| ($V_I$ = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Rise Time | $t_{TLH}$ | – | 0.3 | – | – | 0.3 | – | μs |
| ($V_I$ = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Overshoot | os | – | 15 | – | – | 15 | – | % |
| ($V_I$ = 10 V, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Slew Rate | SR | 1.5 | 1.6 | – | 1.0 | 1.6 | – | V/μs |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $V_{EE}$ = −15 V, $T_A$ = *$T_{high}$ to $T_{low}$ unless otherwise noted).

| Characteristic | Symbol | MC4558, MC4558AC Min | Typ | Max | MC4558C Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage ($R_S \leq 10$ kΩ) | $V_{IO}$ | – | 1.0 | 6.0 | – | – | 7.5 | mV |
| Input Offset Current | $I_{IO}$ | | | | | | | nA |
| ($T_A = T_{high}$) | | – | 7.0 | 200 | – | – | – | |
| ($T_A = T_{low}$) | | – | 85 | 500 | – | – | – | |
| ($T_A$ = 0°C to +70°C) | | – | – | – | – | – | 300 | |
| Input Bias Current | $I_{IB}$ | | | | | | | nA |
| ($T_A = T_{high}$) | | – | 30 | 500 | – | – | – | |
| ($T_A = T_{low}$) | | – | 300 | 1500 | – | – | – | |
| ($T_A$ = 0°C to +70°C) | | – | – | – | – | – | 800 | |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±12 | ±13 | – | – | – | – | V |
| Large Signal Voltage Gain ($V_O$ = ±10 V, $R_L$ = 2 kΩ) | $A_v$ | 25 | – | – | 15 | – | – | V/mV |
| Common Mode Rejection Ratio ($R_S \leq 10$ kΩ) | CMRR | 70 | 90 | – | – | – | – | dB |
| Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ) | PSRR | – | 30 | 150 | – | – | – | μV/V |
| Output Voltage Swing | $V_O$ | | | | | | | V |
| ($R_L \geq 10$ kΩ) | | ±12 | ±14 | – | ±12 | ±14 | – | |
| ($R_L \geq 2$ kΩ) | | ±10 | ±13 | – | ±10 | ±13 | – | |
| Supply Currents (Both Amplifiers) | $I_D$ | | | | | | | mA |
| ($T_A = T_{high}$) | | – | – | 4.5 | – | – | 5.0 | |
| ($T_A = T_{low}$) | | – | – | 6.0 | – | – | 6.7 | |
| Power Consumption (Both Amplifiers) | $P_C$ | | | | | | | mW |
| ($T_A = T_{high}$) | | – | – | 135 | – | – | 150 | |
| ($T_A = T_{low}$) | | – | – | 180 | – | – | 200 | |

*$T_{high}$ = 125°C for MC4558 and 70°C for MC4558C and MC4558AC.
$T_{low}$ = −55°C for MC4558 and 0°C for MC4558C and MC4558AC.
† $I_{IB}$ is out of the amplifier due to PNP input transistors.

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

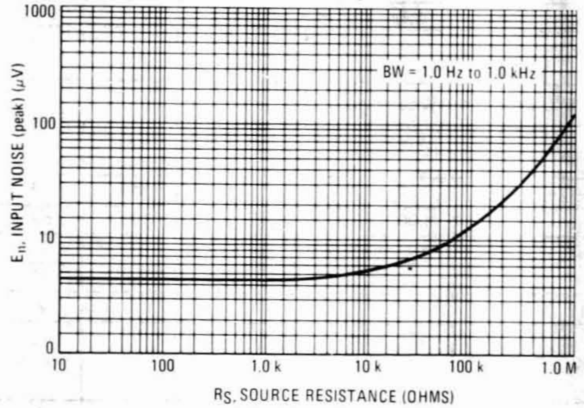


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

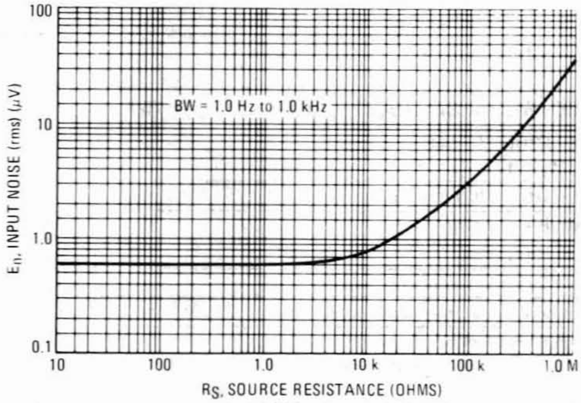


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

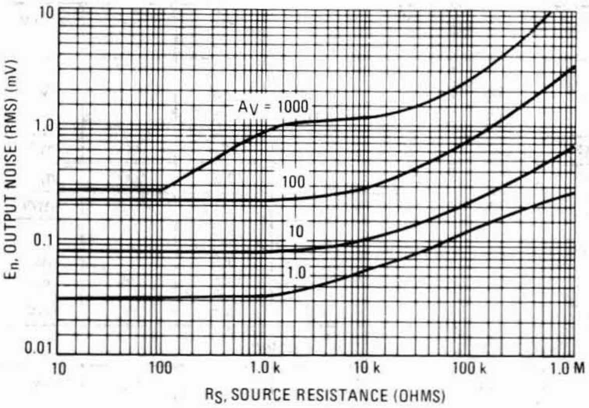


FIGURE 4 – SPECTRAL NOISE DENSITY

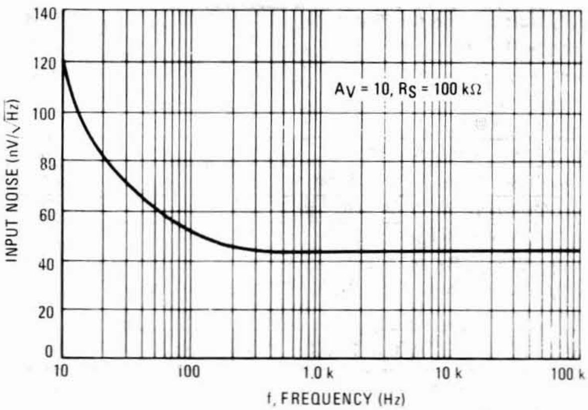
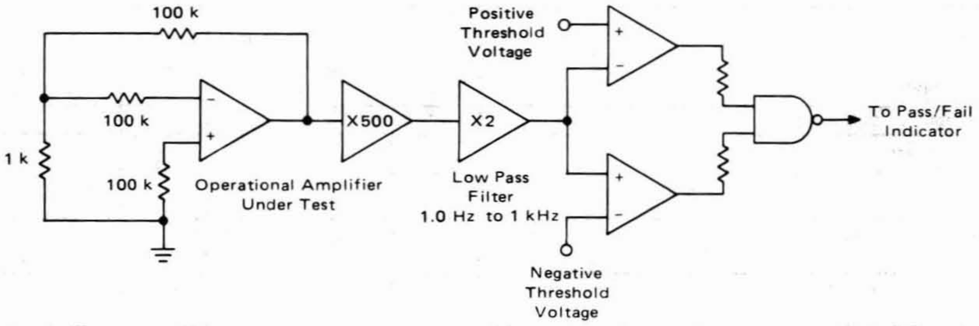


FIGURE 5 – BURST NOISE TEST CIRCUIT



100 k
100 k
1 k
100 k
Operational Amplifier Under Test
X500
X2
Low Pass Filter 1.0 Hz to 1 kHz
Positive Threshold Voltage
Negative Threshold Voltage
To Pass/Fail Indicator

Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 µV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

FIGURE 6 – OPEN LOOP FREQUENCY RESPONSE

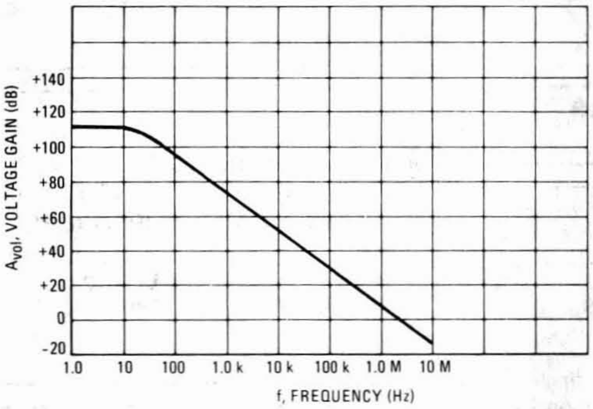


FIGURE 7 – PHASE MARGIN versus FREQUENCY

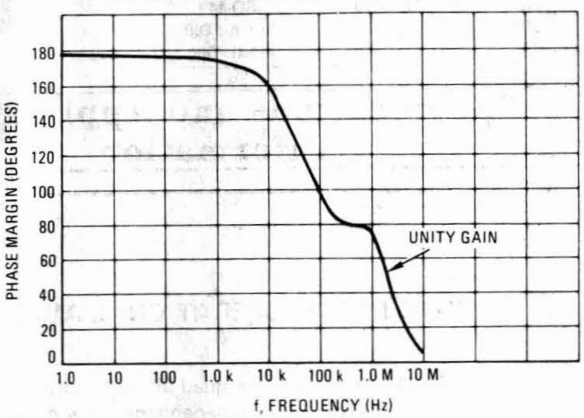


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

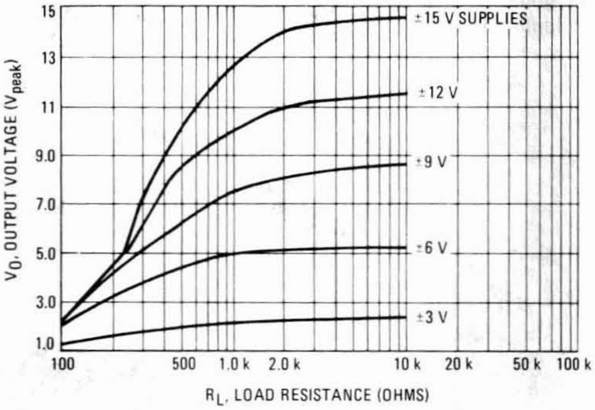


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

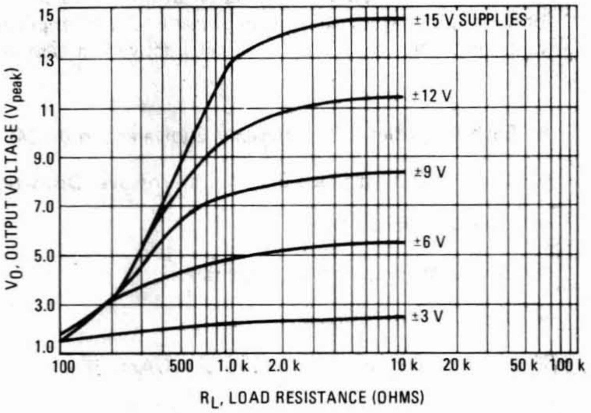


FIGURE 10 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)

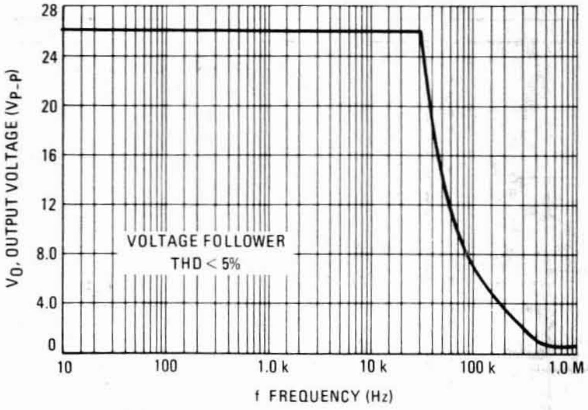
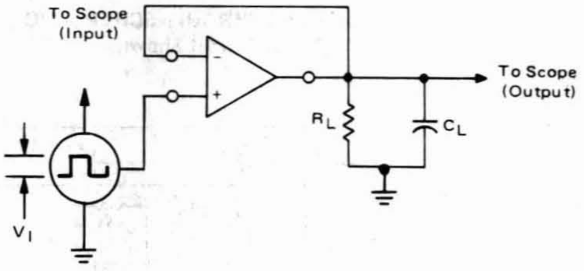


FIGURE 11 – TRANSIENT RESPONSE TEST CIRCUIT



**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC4741L | −55°C to +125°C | Ceramic DIP |
| MC4741CD | 0°C to +70°C | SO-14 |
| MC4741CL | 0°C to +70°C | Ceramic DIP |
| MC4741CP | 0°C to +70°C | Plastic DIP |

# MC4741
# MC4741C

## Specifications and Applications Information

## QUAD MC1741 DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

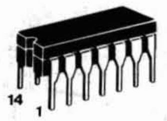
### SILICON MONOLITHIC INTEGRATED CIRCUIT

## QUAD MC1741 OPERATIONAL AMPLIFIERS

The MC4741 series is a true quad MC1741. Integrated on a single monolithic chip are four independent, low-power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance.

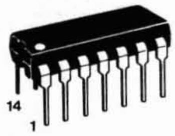
The MC4741 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Class AB Output Stage Eliminates Crossover Distortion
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)



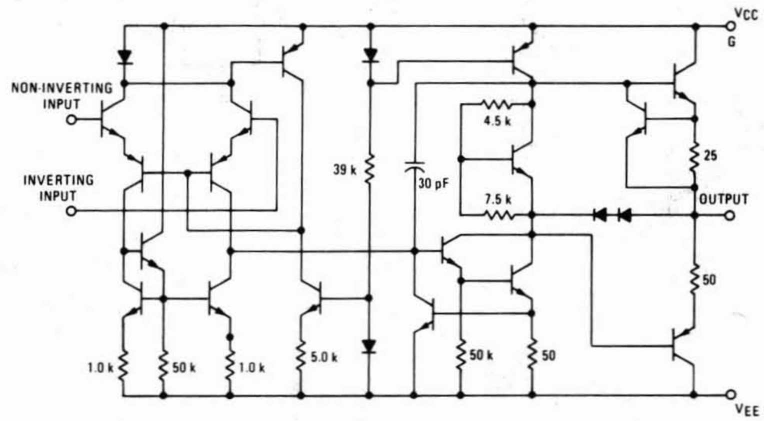
**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA

**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14

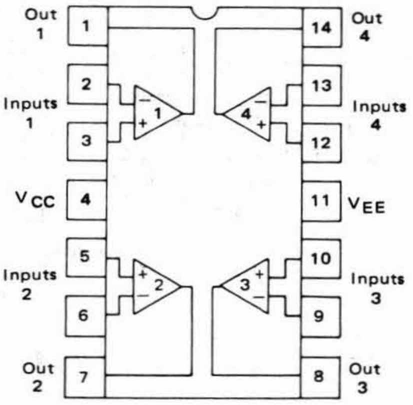


**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

**EQUIVALENT CIRCUIT SCHEMATIC**
**(1/4 of Circuit Shown)**


VCC
G
NON-INVERTING INPUT
INVERTING INPUT
4.5 k
39 k
30 pF
7.5 k
25
OUTPUT
50
1.0 k
50 k
1.0 k
5.0 k
50 k
50
VEE

**PIN CONNECTIONS**


Out 1
1
Inputs 1
2
3
VCC
4
Inputs 2
5
6
Out 2
7
Out 4
14
Inputs 4
13
12
11
VEE
Inputs 3
10
9
Out 3
8
1
2
3
4

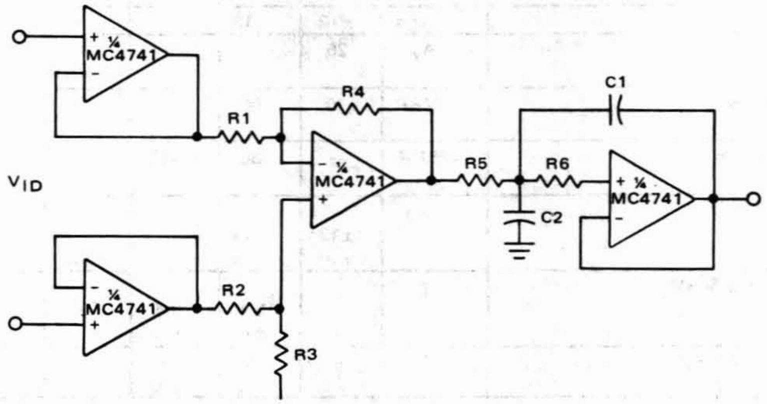
(Top View)

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted).

| Rating | Symbol | MC4741 | MC4741C | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +22<br>-22 | +18<br>-18 | Vdc<br>Vdc |
| Input Differential Voltage | $V_{ID}$ | ±44 | ±36 | Volts |
| Input Common Mode Voltage | $V_{ICM}$ | ±22 | ±18 | Volts |
| Output Short Circuit Duration | $t_S$ | Continuous | | |
| Operating Ambient Temperature Range | $T_A$ | -55 to +125 | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | | | °C |
| Ceramic Package | | -65 to +150 | | |
| Plastic Package | | -55 to +125 | | |
| Junction Temperature | $T_J$ | | | °C |
| Ceramic Package | | 175 | | |
| Plastic Package | | 150 | | |

## TYPICAL APPLICATION

### HIGH IMPEDANCE INSTRUMENTATION BUFFER/FILTER



## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = 25°C unless otherwise noted).

| Characteristic | Symbol | MC4741 |  |  | MC4741C |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage ($R_S \leqslant 10$ k) | $V_{IO}$ | – | 1.0 | 5.0 | – | 2.0 | 6.0 | mV |
| Input Offset Current | $I_{IO}$ | – | 20 | 200 | – | 20 | 200 | nA |
| Input Bias Current | $I_{IB}$ | – | 80 | 500 | – | 80 | 500 | nA |
| Input Resistance | $r_i$ | 0.3 | 2.0 | – | 0.3 | 2.0 | – | MΩ |
| Input Capacitance | $C_i$ | – | 1.4 | – | – | 1.4 | – | pF |
| Offset Voltage Adjustment Range | $V_{IOR}$ | – | ±15 | – | – | ±15 | – | mV |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±12 | ±13 | – | ±12 | ±13 | – | V |
| Large Signal Voltage Gain ($V_O$ = ±10 V, $R_L \geqslant 2.0$ k) | $A_v$ | 50 | 200 | – | 20 | 200 | – | V/mV |
| Output Resistance | $r_o$ | – | 75 | – | – | 75 | – | Ω |
| Common Mode Rejection Ratio ($R_S \leqslant 10$ k) | CMRR | 70 | 90 | – | 70 | 90 | – | dB |
| Supply Voltage Rejection Ratio ($R_S \leqslant 10$ k) | PSRR | – | 30 | 150 | – | 30 | 150 | µV/V |
| Output Voltage Swing | $V_O$ |  |  |  |  |  |  | V |
| ($R_L \geqslant 10$ k) |  | ±12 | ±14 | – | ±12 | ±14 | – |  |
| ($R_L \geqslant 2$ k) |  | ±10 | ±13 | – | ±10 | ±13 | – |  |
| Output Short-Circuit Current | $I_{os}$ | – | 20 | – | – | 20 | – | mA |
| Supply Current – (All Amplifiers) | $I_D$ | – | 2.4 | 4.0 | – | 3.5 | 7.0 | mA |
| Power Consumption (All Amplifiers) | $P_C$ | – | 72 | 120 | – | 105 | 210 | mW |
| Transient Response (Unity Gain – Non-Inverting) |  |  |  |  |  |  |  |  |
| ($V_I$ = 20 mV, $R_L \geqslant 2$ k, $C_L \leqslant 100$ pF) Rise Time | $t_{TLH}$ | – | 0.3 | – | – | 0.3 | – | µs |
| ($V_I$ = 20 mV, $R_L \geqslant 2$ k, $C_L \leqslant 100$ pF) Overshoot | os | – | 15 | – | – | 15 | – | % |
| ($V_I$ = 10 V, $R_L \geqslant 2$ k, $C_L \leqslant 100$ pF) Slew Rate | SR | – | 0.5 | – | – | 0.5 | – | V/µs |

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = *$T_{high}$ to $T_{low}$ unless otherwise noted.)

| Characteristic | Symbol | MC4741 |  |  | MC4741C |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage ($R_S \leqslant 10$ kΩ) | $V_{IO}$ | – | 1.0 | 6.0 | – | – | 7.5 | mV |
| Input Offset Current | $I_{IO}$ |  |  |  |  |  |  | nA |
| ($T_A$ = 125°C) |  | – | 7.0 | 200 | – | – | – |  |
| ($T_A$ = −55°C) |  | – | 85 | 500 | – | – | – |  |
| ($T_A$ = 0°C to +70°C) |  | – | – | – | – | – | 300 |  |
| Input Bias Current | $I_{IB}$ |  |  |  |  |  |  | nA |
| ($T_A$ = 125°C) |  | – | 30 | 500 | – | – | – |  |
| ($T_A$ = −55°C) |  | – | 300 | 1500 | – | – | – |  |
| ($T_A$ = 0°C to +70°C) |  | – | – | – | – | – | 800 |  |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±12 | ±13 | – | – | – | – | V |
| Large Signal Voltage Gain ($R_L \geqslant 2$ k, $V_{out}$ = ±10 V) | $A_v$ | 25 | – | – | 15 | – | – | V/mV |
| Common Mode Rejection Ratio ($R_S \leqslant 10$ k) | CMRR | 70 | 90 | – | – | – | – | dB |
| Supply Voltage Rejection Ratio ($R_S \leqslant 10$ k) | PSRR | – | 30 | 150 | – | – | – | µV/V |
| Output Voltage Swing | $V_O$ |  |  |  |  |  |  | V |
| ($R_L \geqslant 10$ k) |  | ±12 | ±14 | – | – | – | – |  |
| ($R_L \geqslant 2$ k) |  | ±10 | ±13 | – | ±10 | ±13 | – |  |
| Supply Currents – (All Amplifiers) | $I_D$ |  |  |  |  |  |  | mA |
| ($T_A$ = 125°C) |  | – | 2.4 | 3.4 | – | – | – |  |
| ($T_A$ = −55°C) |  | – | 3.6 | 5.0 | – | – | – |  |
| Power Consumption ($T_A$ = +125°C) | $P_C$ | – | 72 | 102 | – | – | – | mW |
| (All Amplifiers) ($T_A$ = −55°C) |  | – | 108 | 150 | – | – | – |  |

*$T_{high}$ = 125°C for MC4741 and 70°C for MC4741C
$T_{low}$ = −55°C for MC4741 and 0°C for MC4741C

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $V_{EE}$ = −15 Vdc, $T_A$ = +25°C unless otherwise noted).

**FIGURE 1 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)**

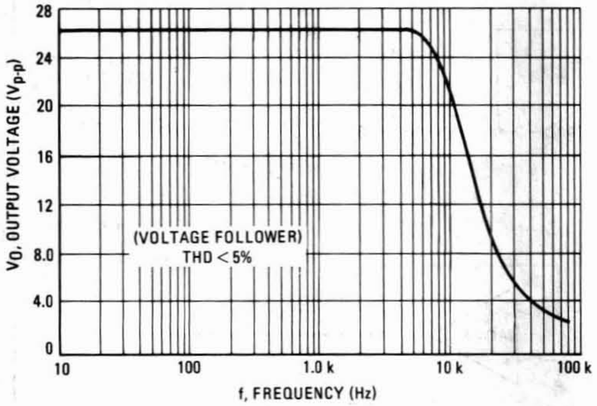


**FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE**

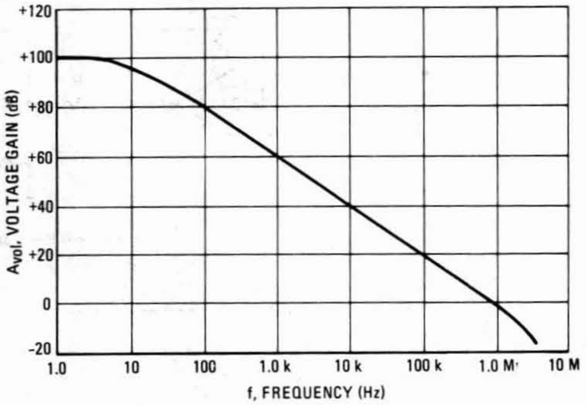


**FIGURE 3 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE**

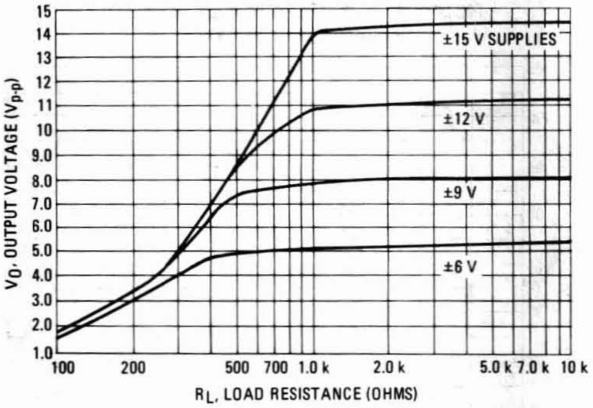


**FIGURE 4 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE**

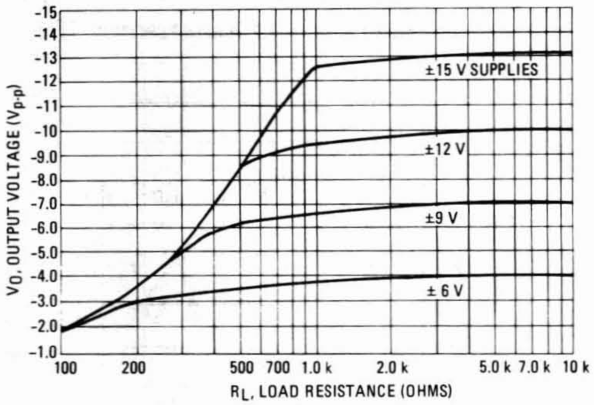


**FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)**

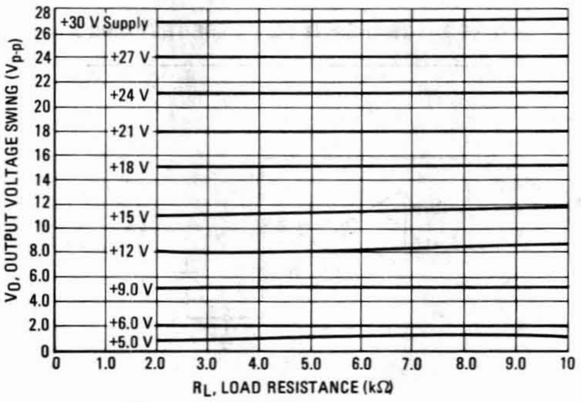
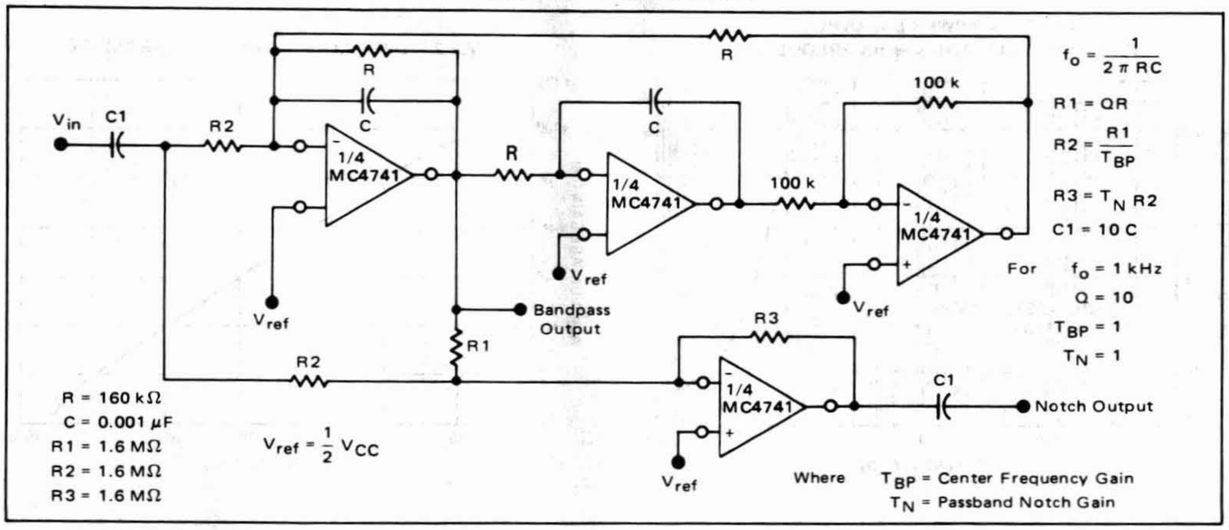


FIGURE 6 — BI-QUAD FILTER



Vin
C1
R2
R
C
1/4 MC4741
Vref
R
C
1/4 MC4741
Vref
100 k
100 k
1/4 MC4741
Vref
R
Bandpass Output
R1
R2
R3
1/4 MC4741
Vref
C1
Notch Output
$f_o = \frac{1}{2\pi RC}$
R1 = QR
$R2 = \frac{R1}{T_{BP}}$
$R3 = T_N R2$
C1 = 10 C
For $f_o$ = 1 kHz
Q = 10
$T_{BP}$ = 1
$T_N$ = 1
R = 160 kΩ
C = 0.001 μF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ
$V_{ref} = \frac{1}{2} V_{CC}$
Where $T_{BP}$ = Center Frequency Gain
$T_N$ = Passband Notch Gain

FIGURE 7 — NONINVERTING PULSE RESPONSE

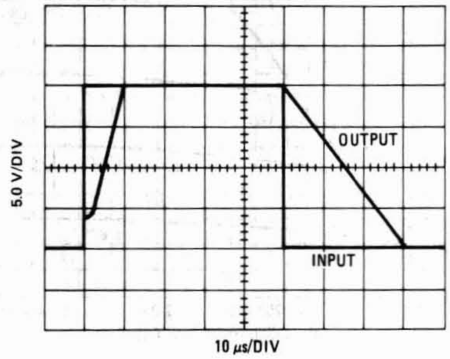


FIGURE 8 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

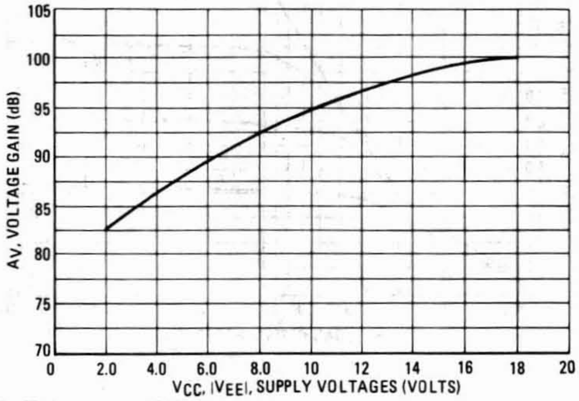
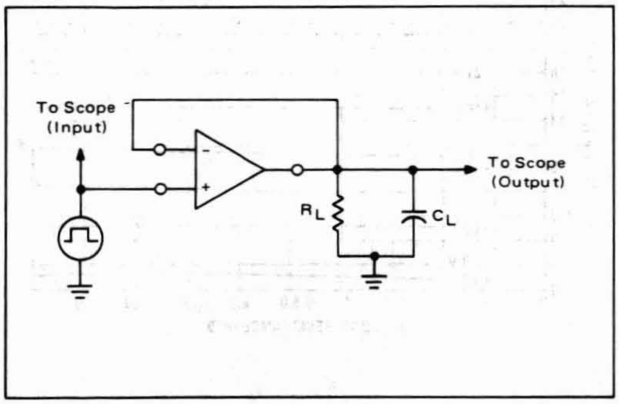
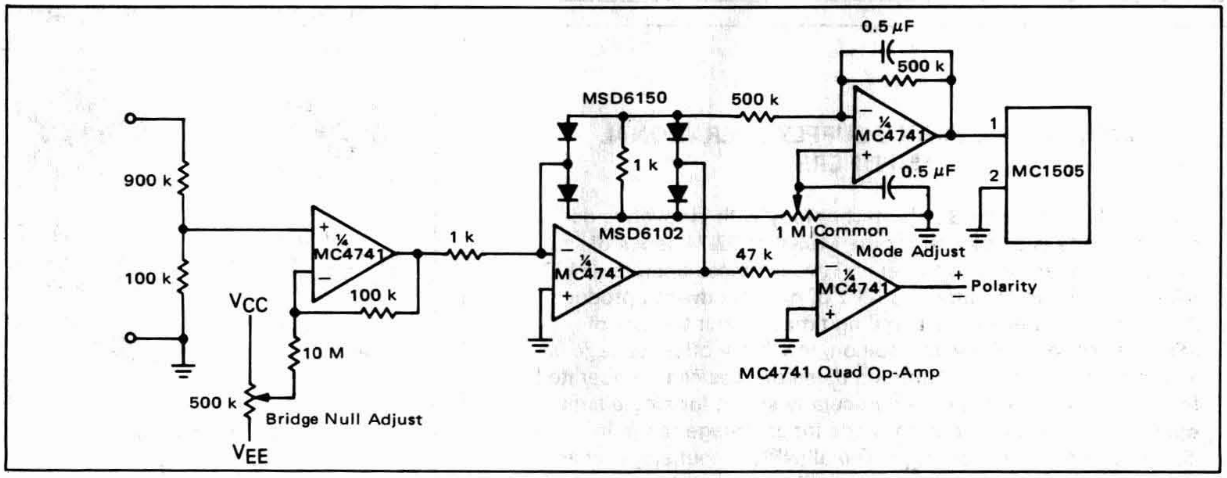


FIGURE 9 — TRANSIENT RESPONSE TEST CIRCUIT



To Scope (Input)
-
+
RL
CL
To Scope (Output)

FIGURE 10 – ABSOLUTE VALUE DVM FRONT END


0.5 µF
500 k
MSD6150
500 k
¼
MC4741
1
900 k
1 k
0.5 µF
2
MC1505
+
¼
MC4741
1 k
MSD6102
1 M
Common
Mode Adjust
100 k
VCC
100 k
¼
MC4741
47 k
¼
MC4741
Polarity
10 M
MC4741 Quad Op-Amp
500 k
Bridge Null Adjust
VEE

**MOTOROLA**

# MC33171, MC35171
# MC33172, MC35172
# MC33174, MC35174

## Advance Information

## LOW POWER, SINGLE SUPPLY OPERATIONAL AMPLIFIERS

A standard low-cost Bipolar technology with innovative design concepts is employed for the MC33171/72/74 series of monolithic operational amplifiers. These devices operate at 180 µA per amplifier and offer 1.8 MHz of gain bandwidth product, 2.1 V/µs slew rate, and fast settling time without the use of JFET device technology. In addition, low input offset voltage is economically achieved. Although these devices can be operated from split supplies, they are particularly suited for single supply operation, since the common mode input voltage range includes ground potential ($V_{EE}$). The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, also provides high capacitive drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC33171/72/74 series of devices are available specified over industrial/vehicular or military temperature ranges.

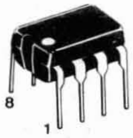
- Low Supply Current: 180 µA (Per Amplifier)
- Wide Supply Operating Range: +3.0 to +44 V or ±1.5 to ±22 V
- Wide Input Common Mode Range Including Ground ($V_{EE}$)
- Wide Bandwidth: 1.8 MHz
- High Slew Rate: 2.1 V/µs
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: 28.4 Vp-p for $V_S$ = ±15 V
- Low T.H.D. Distortion: 0.03%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 15 dB

**ORDERING INFORMATION**

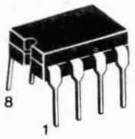
| Op Amp Function | Device | Temperature Range | Package |
|---|---|---|---|
| Single | MC33171D<br>MC35171U<br>MC33171P | −40 to +85°C<br>−55 to +125°C<br>−40 to +85°C | SO-8 Plastic DIP<br>Ceramic DIP<br>Plastic DIP |
| Dual | MC33172D<br>MC35172U<br>MC33172P | −40 to +85°C<br>−55 to +125°C<br>−40 to +85°C | SO-8 Plastic DIP<br>Ceramic DIP<br>Plastic DIP |
| Quad | MC33174D<br>MC35174L<br>MC33174P | −40 to +85°C<br>−55 to +125°C<br>−40 to +85°C | SO-14 Plastic DIP<br>Ceramic DIP<br>Plastic DIP |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

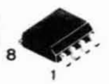
## LOW POWER, SINGLE SUPPLY OPERATIONAL AMPLIFIERS



**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

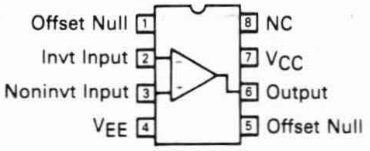


**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02

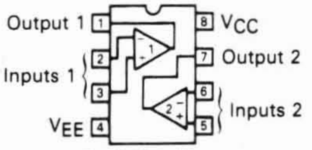


**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8

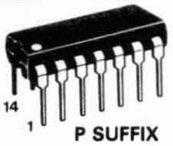
**PIN ASSIGNMENTS**



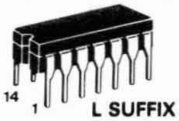
Single, Top View



Dual, Top View



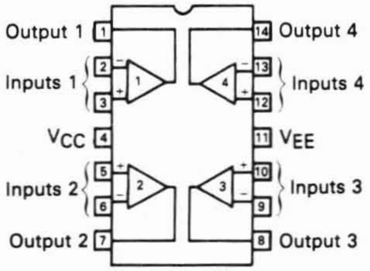
**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05



**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA
(TO-116)

**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14

**PIN ASSIGNMENTS**



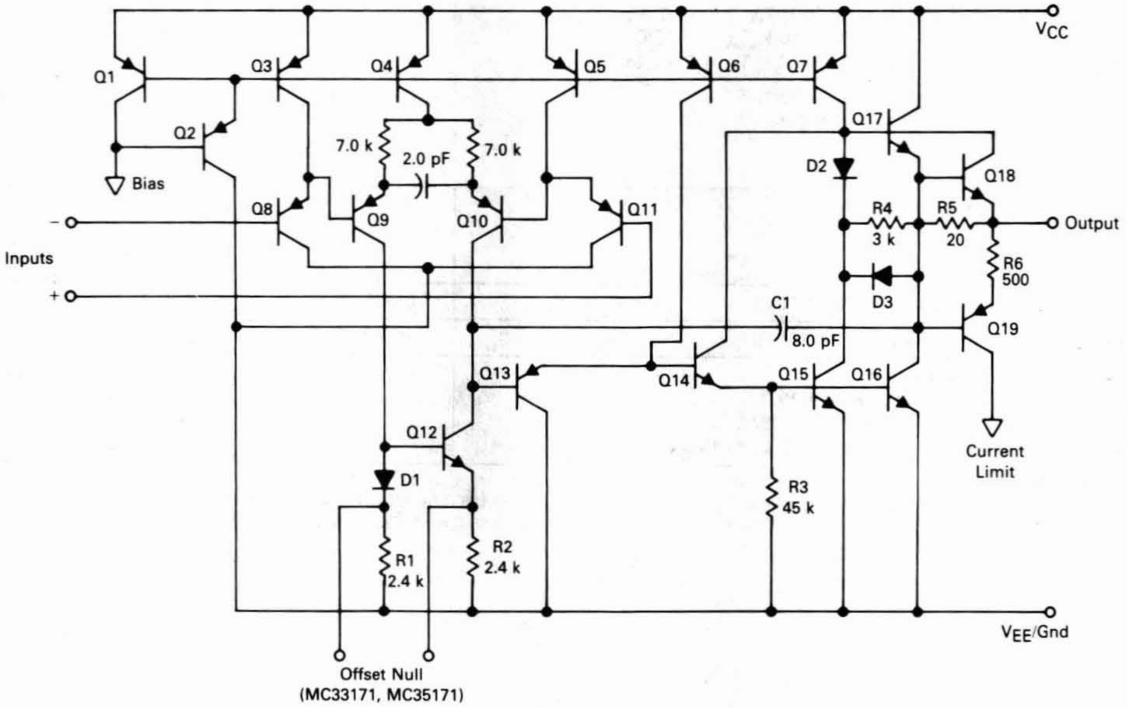
Quad, Top View

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage (from $V_{CC}$ to $V_{EE}$) | $V_S$ | +44 | Volts |
| Input Differential Voltage Range | $V_{IDR}$ | Note 1 | Volts |
| Input Voltage Range | $V_{IR}$ | Note 1 | Volts |
| Output Short-Circuit Duration (Note 2) | $t_S$ | Indefinite | Seconds |
| Operating Ambient Temperature Range<br>MC35171/MC35172/MC35174<br>MC33171/MC33172/MC33174 | $T_A$ | <br>−55 to +125<br>−40 to +85 | °C |
| Operating Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range<br>Ceramic Package<br>Plastic Package | $T_{stg}$ | <br>−65 to +150<br>−55 to +125 | °C |

Notes: 1. Either or both input voltages must not exceed the magnitude of $V_{CC}$ or $V_{EE}$.
2. Power dissipation must be considered to ensure maximum junction temperature ($T_J$) is not exceeded.

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)


VCC
Q1
Q2
Bias
Q3
Q4
Q5
Q6
Q7
Q17
7.0 k
2.0 pF
7.0 k
D2
Q18
Q8
Q9
Q10
Q11
R4
3 k
R5
20
Output
−
Inputs
+
R6
500
D3
C1
8.0 pF
Q19
Q13
Q14
Q15
Q16
Q12
D1
R3
45 k
Current
Limit
R1
2.4 k
R2
2.4 k
VEE/Gnd
Offset Null
(MC33171, MC35171)

**DC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ connected to ground, $T_A$ = $T_{low}$ to $T_{high}$ [Note 3] unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Offset Voltage ($V_{CM}$ = 0 V) | $V_{IO}$ | | | | mV |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C | | — | 2.0 | 4.5 | |
| $V_{CC}$ = +5 V, $V_{EE}$ = 0 V, $T_A$ = +25°C | | — | 2.5 | 5.0 | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = $T_{low}$ to $T_{high}$ | | — | — | 6.5 | |
| Average Temperature Coefficient of Offset Voltage | $\Delta V_{IO}/\Delta T$ | — | 10 | — | μV/°C |
| Input Bias Current ($V_{CM}$ = 0 V) | $I_{IB}$ | | | | nA |
| $T_A$ = +25°C | | — | 20 | 100 | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | — | — | 200 | |
| Input Offset Current ($V_{CM}$ = 0 V) | $I_{IO}$ | | | | nA |
| $T_A$ = +25°C | | — | 5.0 | 20 | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | — | — | 40 | |
| Large Signal Voltage Gain ($V_O$ = ±10 V, $R_L$ = 10 k) | $A_{VOL}$ | | | | V/mV |
| $T_A$ = +25°C | | 50 | 500 | — | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | 25 | — | — | |
| Output Voltage Swing | $V_{OH}$ | | | | V |
| $V_{CC}$ = +5.0 V, $V_{EE}$ = 0 V, $R_L$ = 10 k, $T_A$ = +25°C | | 3.5 | 4.3 | — | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ = 10 k, $T_A$ = +25°C | | 13.6 | 14.2 | — | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ = 10 k, $T_A$ = $T_{low}$ to $T_{high}$ | | 13.3 | — | — | |
| $V_{CC}$ = +5.0 V, $V_{EE}$ = 0 V, $R_L$ = 10 k, $T_A$ = +25°C | $V_{OL}$ | — | 0.05 | 0.15 | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ = 10 k, $T_A$ = +25°C | | — | −14.2 | −13.6 | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ = 10 k, $T_A$ = $T_{low}$ to $T_{high}$ | | — | — | −13.3 | |
| Output Short-Circuit Current ($T_A$ = +25°C) | $I_{SC}$ | | | | mA |
| Input Overdrive = 1.0 V, Output to Ground | | | | | |
| Source | | 3.0 | 5.0 | — | |
| Sink | | 15 | 27 | — | |
| Input Common Mode Voltage Range | $V_{ICR}$ | | | | V |
| $T_A$ = +25°C | | $V_{EE}$ to ($V_{CC}$ − 1.8) | | | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | $V_{EE}$ to ($V_{CC}$ − 2.2) | | | |
| Common Mode Rejection Ratio ($R_S$ ≤ 10 k) | CMRR | 80 | 90 | — | dB |
| Power Supply Rejection Ratio ($R_S$ = 100 Ω) | PSRR | 80 | 100 | — | dB |
| Power Supply Current (Per Amplifier) | $I_D$ | | | | μA |
| $V_{CC}$ = +5.0 V, $V_{EE}$ = 0 V, $T_A$ = +25°C | | — | 180 | 250 | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C | | — | 220 | 250 | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = $T_{low}$ to $T_{high}$ | | — | — | 300 | |

Notes: (continued)

3. $T_{low}$ = −55°C for MC35171/MC35172/MC35174
= −40°C for MC33171/MC33172/MC33174

$T_{high}$ = +125°C for MC35171/MC35172/MC35174
= +85°C for MC33171/MC33172/MC33174

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ connected to ground, $T_A$ = +25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Slew Rate ($V_{in}$ = −10 V to +10 V, $R_L$ = 10 k, $C_L$ = 100 pF) | SR | | | | V/µs |
| $A_V$ + 1 | | 1.6 | 2.1 | — | |
| $A_V$ − 1 | | — | 2.1 | — | |
| Gain Bandwidth Product (f = 100 kHz) | GBW | 1.4 | 1.8 | — | MHz |
| Power Bandwidth<br>$A_V$ = +1.0, $R_L$ = 10 k, $V_O$ = 20 $V_{p-p}$, THD = 5% | $BW_p$ | — | 35 | — | kHz |
| Phase Margin | $\phi m$ | | | | Degrees |
| $R_L$ = 10 k | | — | 60 | — | |
| $R_L$ = 10 k, $C_L$ = 100 pF | | — | 45 | — | |
| Gain Margin | $A_m$ | | | | dB |
| $R_L$ = 10 k | | — | 15 | — | |
| $R_L$ = 10 k, $C_L$ = 100 pF | | — | 5.0 | — | |
| Equivalent Input Noise Voltage<br>$R_S$ = 100 Ω, f = 1.0 kHz | $e_n$ | — | 32 | — | nV/$\sqrt{Hz}$ |
| Equivalent Input Noise Current (f = 1.0 kHz) | $i_n$ | — | 0.2 | — | pA/$\sqrt{Hz}$ |
| Input Capacitance | $C_i$ | — | 0.8 | — | pF |
| Total Harmonic Distortion<br>$A_V$ = +10, $R_L$ = 10 k, 2.0 $V_{p-p}$ ≤ $V_O$ ≤ 20 $V_{p-p}$, f = 10 kHz | THD | — | 0.03 | — | % |
| Channel Separation (f = 10 kHz) | — | — | 120 | — | dB |
| Open-Loop Output Impedance (f = 1.0 MHz) | $z_o$ | — | 100 | — | Ω |

## TYPICAL PERFORMANCE CURVES

FIGURE 1 — INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

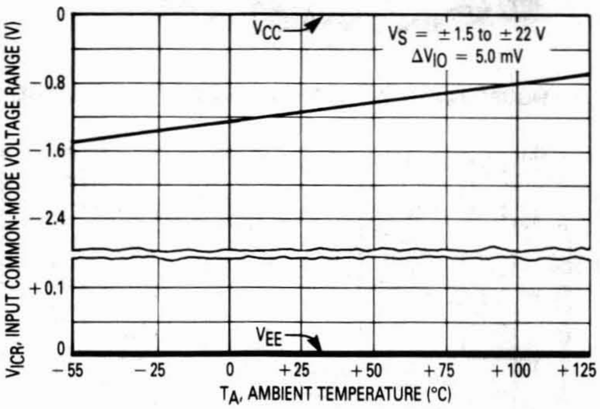


FIGURE 2 — SPLIT SUPPLY OUTPUT SATURATION versus LOAD CURRENT

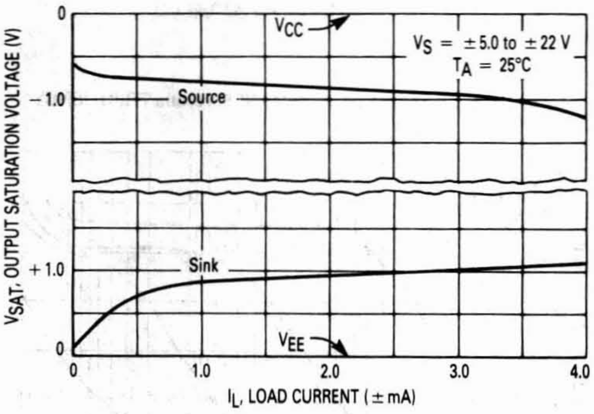


**FIGURE 3 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY**

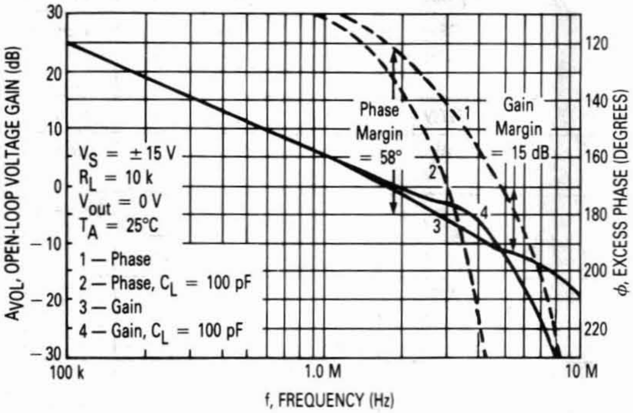


**FIGURE 4 — PHASE MARGIN AND PERCENT OVERSHOOT versus LOAD CAPACITANCE**

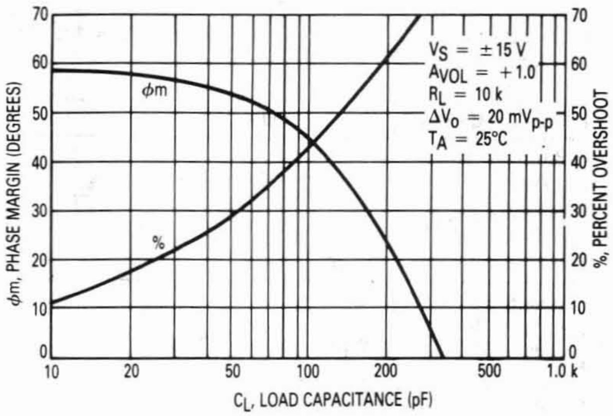


**FIGURE 5 — NORMALIZED GAIN BANDWIDTH PRODUCT AND SLEW RATE versus TEMPERATURE**

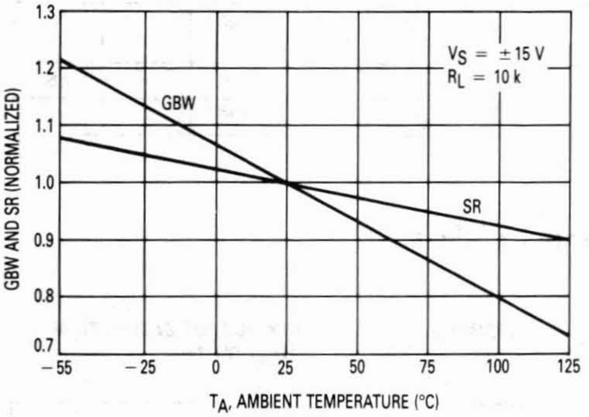


**FIGURE 6 — SMALL AND LARGE SIGNAL TRANSIENT RESPONSE**

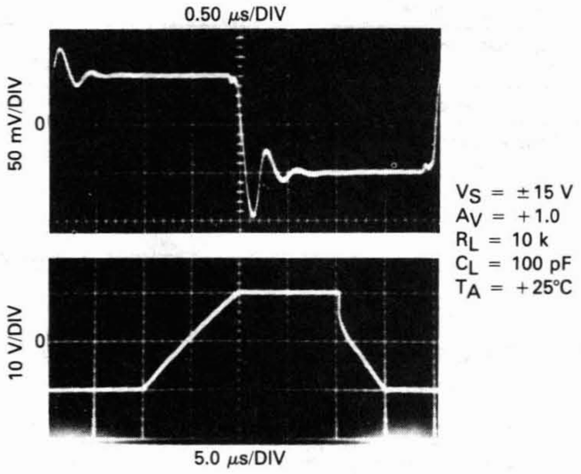


**FIGURE 7 — OUTPUT IMPEDANCE versus FREQUENCY**

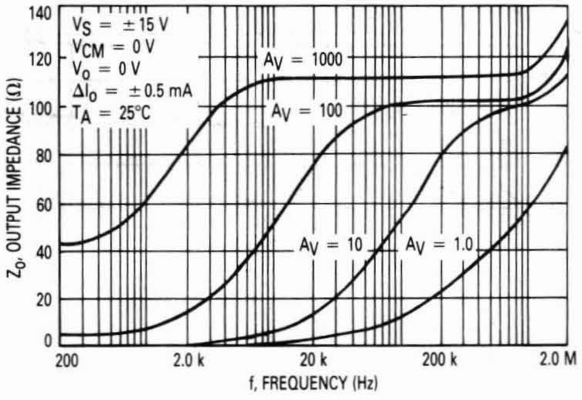
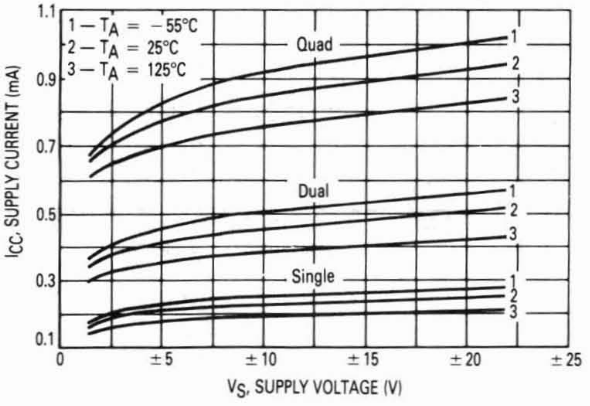


**FIGURE 8 — SUPPLY CURRENT versus SUPPLY VOLTAGE**



## APPLICATIONS INFORMATION
## CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC33171/72/74 amplifier family is similar to low power op amp products utilizing JFET input devices, these amplifiers offer additional advantages as a result of the PNP transistor differential inputs and an all NPN transistor output stage.

Because the input common mode voltage range of this input stage includes the $V_{EE}$ potential, single supply operation is feasible to as low as 3.0 volts with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 volts, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between $V_{CC}$ and $V_{EE}$ supply voltages as shown by the maximum rating table. In practice, although *not recommended,* the input voltages can exceed the $V_{CC}$ voltage by approximately 3.0 volts and decrease below the $V_{EE}$ voltage by 0.3 volts without causing product damage, although output phase reversal may occur. It is also possible to source up to 5.0 mA of current from $V_{EE}$ through either input's clamping diode without damage or latching, but phase reversal may again occur. If at least one input is within the common mode input voltage range and the other input is within the maximum input voltage range, no phase reversal will occur. If both inputs exceed the upper common mode input voltage limit, the output will be forced to its lowest voltage state.

Since the input capacitance associated with the small geometry input device is substantially lower (0.8 pF) than that of a typical JFET (3.0 pF), the frequency response for a given input source resistance is greatly enhanced. This becomes evident in D-to-A current to voltage conversion applications where the feedback resistance can form a pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DAC's). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 10 kΩ of feedback resistance, the MC33171/72/74 family can typically settle to within 1/2 LSB of 8 bits in 4.2 µs, and within 1/2 LSB of 12 bits in 4.8 µs for a 10 volt step. In a standard inverting unity gain fast settling configuration, the symmetrical slew rate is typically ±2.1 volts/µs. In the classic non-inverting unity gain configuration the typical output positive slew rate is also 2.1 volts/µs, and the corresponding negative slew rate will usually exceed the positive slew rate as a function of the fall time of the input waveform.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can typically swing within 0.8 volt of the positive rail ($V_{CC}$) and negative rail ($V_{EE}$), providing a 28.4 Vp-p swing from ±15 volt supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q7, the $V_{BE}$ of the NPN pull up transistor Q17, and the voltage drop associated with the short circuit resistance, $R_5$. For sink currents less than 0.4 mA, the negative swing is limited by the saturation voltage of the pull-down transistor Q15, and the voltage drop across $R_4$ and $R_5$. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of $V_{EE}$. For sink currents (> 0.4 mA), diode D3 clamps the voltage across $R_4$. Thus the negative swing is limited by the saturation voltage of Q15, plus the forward diode drop of D3 ($\approx V_{EE} + 1.0$ V). Therefore an unprecedented peak-to-peak output voltage swing is possible for a given supply voltage as indicated by the output swing specifications.

If the load resistance is referenced to $V_{CC}$ instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to $V_{CC}$ during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter-follower transistor has been eliminated, the MC33171/72/74 family offers a 15 mA minimum current sink capability, typically to an output voltage of ($V_{EE}$ + 1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for high current switching applications.

In addition, the all NPN transistor output stage is inherently faster than PNP types, contributing to the bipolar amplifier's improved gain-bandwidth product. The associated high frequency low output impedance (200 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 to 400 pF without oscillation in the non-inverting unity gain configuration. The 60° phase margin and 15 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The ac characteristics of the MC33171/72/74 family also allow excellent active filter capability, especially for low voltage single supply applications.

Although the single supply specification is defined at 5.0 volts, these amplifiers are functional to at least 3.0 volts @ 25°C. However slight changes in parametrics such as bandwidth, slew rate, and dc gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 volt supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

FIGURE 9 — AC COUPLED NONINVERTING AMPLIFIER WITH SINGLE +5.0 V SUPPLY

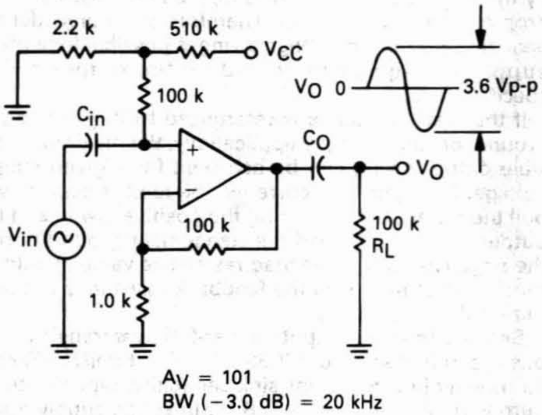

2.2 k
510 k
$V_{CC}$
100 k
$C_{in}$
$C_O$
$V_O$
$V_O$ 0
3.6 Vp-p
100 k
100 k
$R_L$
$V_{in}$
1.0 k
$A_V$ = 101
BW (−3.0 dB) = 20 kHz

FIGURE 10 — AC COUPLED INVERTING AMPLIFIER WITH SINGLE +5.0 V SUPPLY

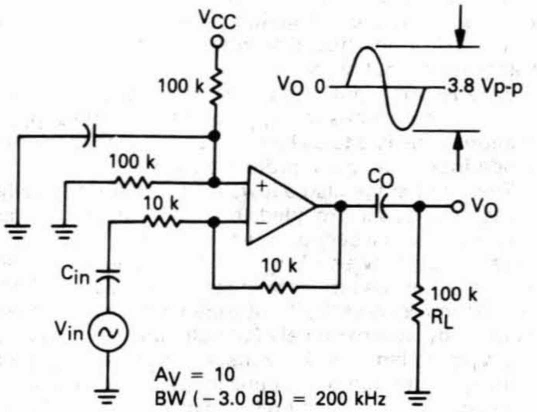

$V_{CC}$
100 k
$V_O$ 0
3.8 Vp-p
100 k
10 k
$C_O$
$V_O$
$C_{in}$
10 k
100 k
$R_L$
$V_{in}$
$A_V$ = 10
BW (−3.0 dB) = 200 kHz

FIGURE 11 — DC COUPLED INVERTING AMPLIFIER MAXIMUM OUTPUT SWING WITH SINGLE +5.0 V SUPPLY

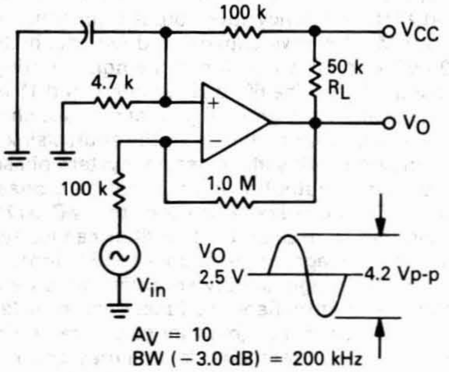
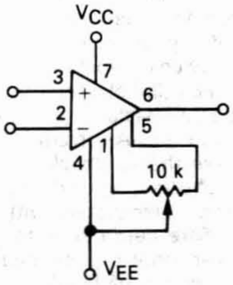

100 k
$V_{CC}$
50 k
$R_L$
4.7 k
$V_O$
100 k
1.0 M
$V_O$
2.5 V
4.2 Vp-p
$V_{in}$
$A_V$ = 10
BW (−3.0 dB) = 200 kHz

FIGURE 12 — OFFSET NULLING CIRCUIT


$V_{CC}$
3
7
2
6
5
4
1
10 k
$V_{EE}$

Offset Nulling range is approximately ±80 mV with a 10 k potentiometer, MC33171/MC35171 only.

FIGURE 13 — ACTIVE HIGH-Q NOTCH FILTER

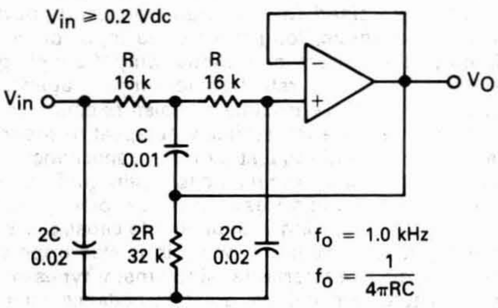
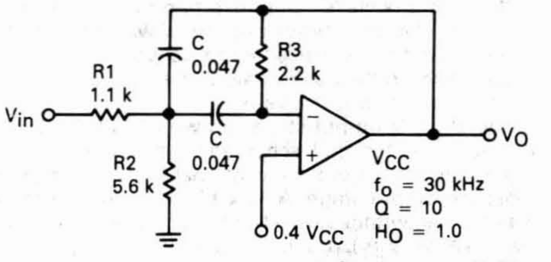

$V_{in} \geq 0.2$ Vdc
R
16 k
R
16 k
$V_{in}$
$V_O$
C
0.01
2C
0.02
2R
32 k
2C
0.02
$f_o$ = 1.0 kHz
$f_o = \frac{1}{4\pi RC}$

FIGURE 14 — ACTIVE BANDPASS FILTER


C
0.047
R3
2.2 k
R1
1.1 k
$V_{in}$
C
0.047
$V_O$
R2
5.6 k
$V_{CC}$
0.4 $V_{CC}$
$f_o$ = 30 kHz
Q = 10
$H_O$ = 1.0

Given $f_O$ = Center Frequency
$A_O$ = Gain at Center Frequency
Choose Value $f_o$, Q, $A_o$, C
Then

$$R1 = \frac{R3}{2\,H_o} \qquad R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

$$R3 = \frac{Q}{\pi f_o C} \qquad \frac{Q_o\,f_o}{GBW} < 0.1$$

For less than 10% error from operational amplifier
Where $f_o$ and GBW are expressed in Hz.

**MOTOROLA**

# MC34001, MC35001
# MC34002, MC35002
# MC34004, MC35004

## JFET-INPUT OPERATIONAL AMPLIFIERS

These low cost JFET-Input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

The Motorola BIFET family offers single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices. The MC35001/35002/35004 series are specified over the military operating temperature range of −55°C to +125°C and the MC34001/34002/34004 series are specified from 0°C to +70°C.

- Input Offset Voltage Options of 2.0, 5.0, and 10 mV Maximum
- Low Input Bias Current — 40 pA
- Low Input Offset Current — 10 pA
- Wide Gain Bandwidth — 4.0 MHz
- High Slew Rate — 13 V/μs
- Low Supply Current — 1.8 mA per Amplifier
- High Input Impedance — $10^{12}$ Ω
- High Common-Mode and Supply Voltage Rejection Ratios — 100 dB
- Industry Standard Pinouts

## ORDERING INFORMATION

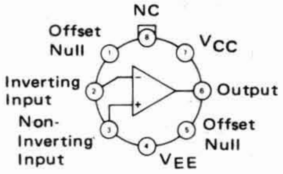
| Op Amp Function | Device | Temperature Range | Package |
|---|---|---|---|
| Single | MC34001AD, BD, D | 0 to +70 | SO-8 |
| | MC34001AG, BG, G | | Metal Can |
| | MC34001AP, BP, P | | Plastic DIP |
| | MC34001AU, BU, U | | Ceramic DIP |
| | MC35001AG, BG, G | −55 to +125°C | Metal Can |
| | MC35001AU, BU, U | | Ceramic DIP |
| Dual | MC34002AD, BD, D | 0 to +70°C | SO-8 |
| | MC34002AG, BG, G | | Metal Can |
| | MC34002AP, BP, P | | Plastic DIP |
| | MC34002AU, BU, U | | Ceramic DIP |
| | MC35002AG, BG, G | −55 to +125°C | Metal Can |
| | MC35002AU, BU, U | | Ceramic DIP |
| Quad | MC34004BD, D | 0 to +70°C | SO-14 |
| | MC34004BL, L | | Ceramic DIP |
| | MC34004BP, P | | Plastic DIP |
| | MC35004BL, L | −55 to +125°C | Ceramic DIP |

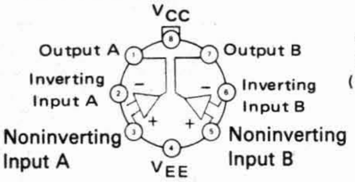
## JFET-INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

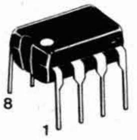
**G SUFFIX**
METAL PACKAGE
CASE 601-04

MC34001, MC35001
(Top View)

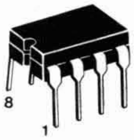

NC
Offset Null
Vcc
Inverting Input
Output
Non-Inverting Input
Offset Null
VEE
1
2
3
4
5
6
7
8


VCC
Output A
Output B
Inverting Input A
Inverting Input B
Noninverting Input A
Noninverting Input B
VEE
1
2
3
4
5
6
7
8

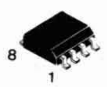
MC34002, MC35002
(Top View)



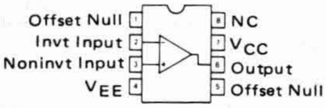
**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04



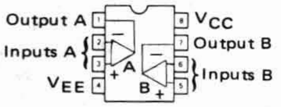
**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02



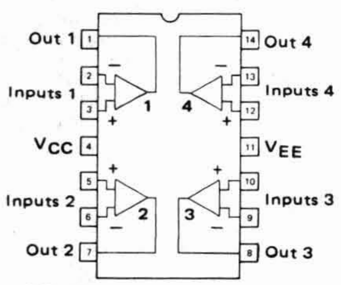
**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8


Offset Null
Invt Input
Noninvt Input
VEE
NC
VCC
Output
Offset Null
1
2
3
4
5
6
7
8

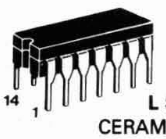
MC34001, MC35001 (Top View)


Output A
Inputs A
VEE
VCC
Output B
Inputs B
A
B
1
2
3
4
5
6
7
8

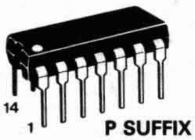
MC34002, MC35002 (Top View)


Out 1
Inputs 1
VCC
Inputs 2
Out 2
Out 4
Inputs 4
VEE
Inputs 3
Out 3
1
2
3
4
1
2
3
4
5
6
7
8
9
10
11
12
13
14

MC34004, MC35004 (Top View)



**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA



**P SUFFIX**
PLASTIC PACKAGE
CAE 646-05

**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14

## MAXIMUM RATINGS

| Rating | Symbol | MC35001<br>MC35002<br>MC35004 | MC34001<br>MC34002<br>MC34004 | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +22<br>−22 | +18<br>−18 | V |
| Differential Input Voltage | $V_{ID}$ | ±40 | ±30 | V |
| Input Voltage Range | $V_{IDR}$ | ±20 | ±16 | V |
| Output Short-Circuit Duration | $t_S$ | Continuous | | |
| Operating Ambient Temperature Range | $T_A$ | −55 to +125 | 0 to +70 | °C |
| Operating Junction Temperature | $T_J$ | | | °C |
| Metal and Ceramic Packages | | 150 | 115 | |
| Plastic Packages | | — | 115 | |
| Storage Temperature Range | $T_{stg}$ | | | °C |
| Metal and Ceramic Packages | | −65 to +150 | −65 to +150 | |
| Plastic Packages | | — | −55 to +125 | |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = 25° unless otherwise noted).

| Characteristic | Symbol | MC35001/35002/35004 | | | MC34001/34002/34004 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($R_S$ ≤ 10 k) | $V_{IO}$ | | | | | | | mV |
| MC3500XA, MC3400XA | | — | 1.0 | 2.0 | — | 1.0 | 2.0 | |
| MC3500XB, MC3400XB | | — | 3.0 | 5.0 | — | 3.0 | 5.0 | |
| MC3500X, MC3400X | | — | 5.0 | 10 | — | 5.0 | 10 | |
| Average Temperature Coefficient of Input Offset Voltage $R_S$ ≤ 10 k, $T_A$ = $T_{low}$ to $T_{high}$ (Note 1) | $\Delta V_{IO}/\Delta T$ | — | 10 | — | — | 10 | — | μV/°C |
| Input Offset Current ($V_{CM}$ = 0) (Note 2) | $I_{IO}$ | | | | | | | pA |
| MC3500XA, MC3400XA | | — | 10 | 25 | — | 25 | 50 | |
| MC3500XB, MC3400XB | | — | 10 | 50 | — | 25 | 100 | |
| MC3500X, MC3400X | | — | 25 | 100 | — | 25 | 100 | |
| Input Bias Current ($V_{CM}$ = 0) (Note 2) | $I_{IB}$ | | | | | | | pA |
| MC3500XA, MC3400XA | | — | 40 | 75 | — | 50 | 100 | |
| MC3500XB, MC3400XB | | — | 40 | 100 | — | 50 | 200 | |
| MC3500X, MC3400X | | — | 50 | 200 | — | 50 | 200 | |
| Input Resistance | $r_i$ | — | $10^{12}$ | — | — | $10^{12}$ | — | Ω |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±11 | +15<br>−12 | — | ±11 | +15<br>−12 | — | V |
| Large Signal Voltage Gain ($V_O$ = ±10 V, $R_L$ = 2.0 k) | $A_{VOL}$ | | | | | | | V/mV |
| MC3500XA, MC3400XA | | 50 | 150 | — | 50 | 150 | — | |
| MC3500XB, MC3400XB | | 50 | 150 | — | 50 | 150 | — | |
| MC3500X, MC3400X | | 25 | 100 | — | 25 | 100 | — | |
| Output Voltage Swing | $V_O$ | | | | ±12 | ±14 | — | V |
| ($R_L$ ≥ 10 k) | | ±12 | ±14 | — | ±10 | ±13 | — | |
| ($R_L$ ≥ 2.0 k) | | ±10 | ±13 | — | | | | |
| Common Mode Rejection Ratio ($R_S$ ≤ 10 k) | CMRR | | | | | | | dB |
| MC3500XA, MC3400XA | | 80 | 100 | — | 80 | 100 | — | |
| MC3500XB, MC3400XB | | 80 | 100 | — | 80 | 100 | — | |
| MC3500X, MC3400X | | — | — | — | 70 | 100 | — | |
| Supply Voltage Rejection Ratio ($R_S$ ≤ 10 k) (Note 3) | PSRR | | | | | | | dB |
| MC3500XA, MC3400XA | | 80 | 100 | — | 80 | 100 | — | |
| MC3500XB, MC3400XB | | 80 | 100 | — | 80 | 100 | — | |
| MC3500X, MC3400X | | 70 | 100 | — | 70 | 100 | — | |
| Supply Current (Each Amplifier) | $I_D$ | | | | | | | mA |
| MC3500XA, MC3400XA | | — | 1.4 | 2.5 | — | 1.4 | 2.5 | |
| MC3500XB, MC3400XB | | — | 1.4 | 2.5 | — | 1.4 | 2.5 | |
| MC3500X, MC3400X | | — | 1.4 | 2.7 | — | 1.4 | 2.7 | |
| Slew Rate ($A_V$ = 1) | SR | — | 13 | — | — | 13 | — | V/μs |
| Gain-Bandwidth Product | GBW | — | 4.0 | — | — | 4.0 | — | MHz |
| Equivalent Input Noise Voltage ($R_S$ = 100 Ω, f = 1000 Hz) | $e_n$ | — | 25 | — | — | 25 | — | $nV/\sqrt{Hz}$ |
| Equivalent Input Noise Current (f = 1000 Hz) | $i_n$ | — | 0.01 | — | — | 0.01 | — | $pA/\sqrt{Hz}$ |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = $T_{low}$ to $T_{high}$ [Note 1]).

| Characteristic | Symbol | MC35001/35002/35004 Min | MC35001/35002/35004 Typ | MC35001/35002/35004 Max | MC34001/34002/34004 Min | MC34001/34002/34004 Typ | MC34001/34002/34004 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage ($R_S$ ≤ 10 k) | $V_{IO}$ | | | | | | | mV |
| MC3500XA, MC3400XA | | — | — | 4.0 | — | — | 4.0 | |
| MC3500XB, MC3400XB | | — | — | 7.0 | — | — | 7.0 | |
| MC3500X, MC3400X | | — | — | 14 | — | — | 13 | |
| Input Offset Current ($V_{CM}$ = 0) (Note 2) | $I_{IO}$ | | | | | | | nA |
| MC3500XA, MC3400XA | | — | — | 20 | — | — | 2.0 | |
| MC3500XB, MC3400XB | | — | — | 40 | — | — | 4.0 | |
| MC3500X, MC3400X | | — | — | 40 | — | — | 4.0 | |
| Input Bias Current ($V_{CM}$ = 0) (Note 2) | $I_{IB}$ | | | | | | | nA |
| MC3500XA, MC3400XA | | — | — | 50 | — | — | 4.0 | |
| MC3500XB, MC3400XB | | — | — | 50 | — | — | 8.0 | |
| MC3500X, MC3400X | | — | — | 50 | — | — | 8.0 | |
| Common Mode Input Voltage Range | $V_{ICR}$ | ±11 | — | — | ±11 | — | — | V |
| Large Signal ($V_O$ = ±10 V, $R_L$ = 2.0 k) | $A_{VOL}$ | | | | | | | V/mV |
| MC3500XA, MC3400XA | | 25 | — | — | 25 | — | — | |
| MC3500XB, MC3400XB | | 25 | — | — | 25 | — | — | |
| MC3500X, MC3400X | | 15 | — | — | 15 | — | — | |
| Output Voltage Swing | $V_O$ | | | | | | | V |
| ($R_L$ ≥ 10 k) | | ±12 | — | — | ±12 | — | — | |
| ($R_L$ ≥ 2.0 k) | | ±10 | — | — | ±10 | — | — | |
| Common Mode Rejection Ratio ($R_S$ ≤ 10 k) | CMRR | | | | | | | dB |
| MC3500XA, MC3400XA | | 80 | — | — | 80 | — | — | |
| MC3500XB, MC3400XB | | 80 | — | — | 80 | — | — | |
| MC3500X, MC3400X | | 70 | — | — | 70 | — | — | |
| Supply Voltage Rejection Ratio ($R_S$ ≤ 10 k) (Note 3) | PSRR | | | | | | | dB |
| MC3500XA, MC3400XA | | 80 | — | — | 80 | — | — | |
| MC3500XB, MC3400XB | | 80 | — | — | 80 | — | — | |
| MC3500X, MC3400X | | 70 | — | — | 70 | — | — | |
| Supply Current (Each Amplifier) | $I_D$ | | | | | | | mA |
| MC3500XA, MC3400XA | | — | — | 2.8 | — | — | 2.8 | |
| MC3500XB, MC3400XB | | — | — | 2.8 | — | — | 2.8 | |
| MC3500X, MC3400X | | — | — | 3.0 | — | — | 3.0 | |

**NOTES:**

(1) $T_{low}$ = −55°C for MC35001/MC35001A/35001B
MC35002/MC35002A/35002B
MC35004/35004B
= 0°C for MC34001/34001A/34001B
MC34002/34002A/34002B
MC34004/34004B
$T_{high}$ = +125°C for MC35001/MC35001A/35001B
MC35002/MC35002A/35002B
MC35004/35004B
= +70°C for MC34001/34001A/34001B
MC34002/34002A/34002B
MC34004/34004B

(2) The input bias currents approximately double for every 10°C rise in junction temperature, $T_J$. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

(4) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

## TYPICAL PERFORMANCE CHARACTERISTICS

**FIGURE 1 — INPUT BIAS CURRENT versus TEMPERATURE**

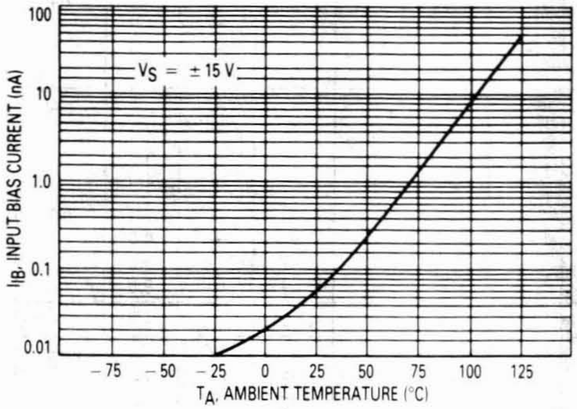


**FIGURE 2 — OUTPUT VOLTAGE SWING versus FREQUENCY**

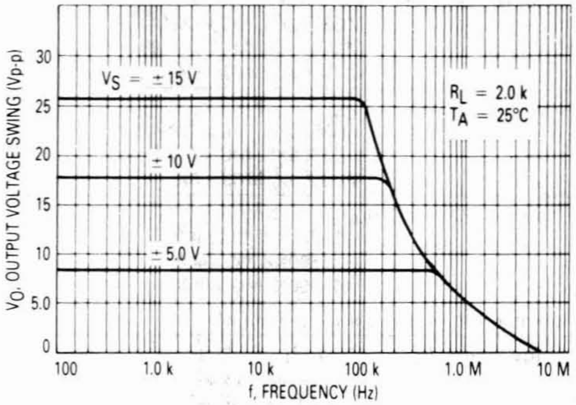


**FIGURE 3 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE**

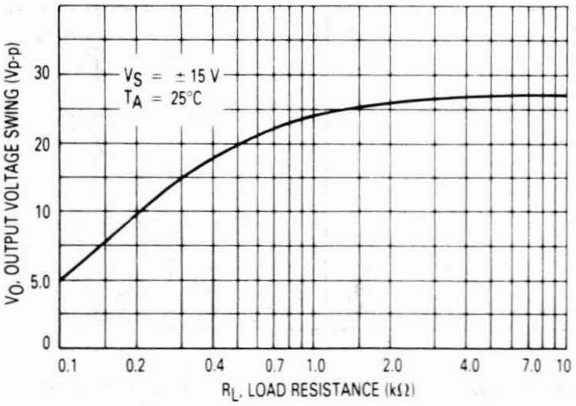


**FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE**

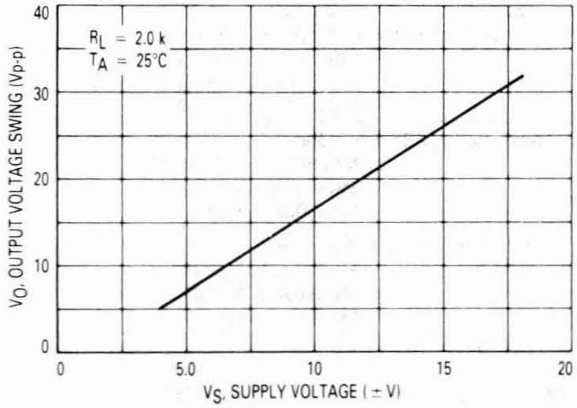


**FIGURE 5 — OUTPUT VOLTAGE SWING versus TEMPERATURE**

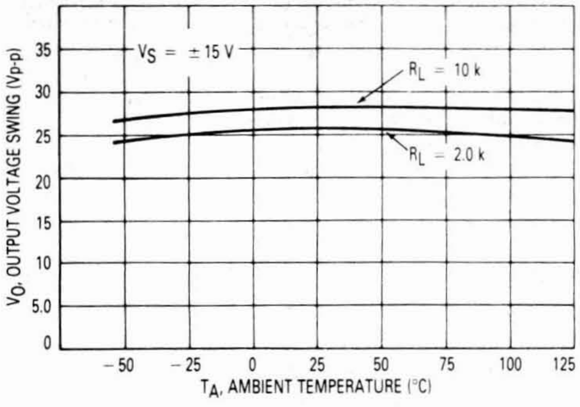


**FIGURE 6 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE**

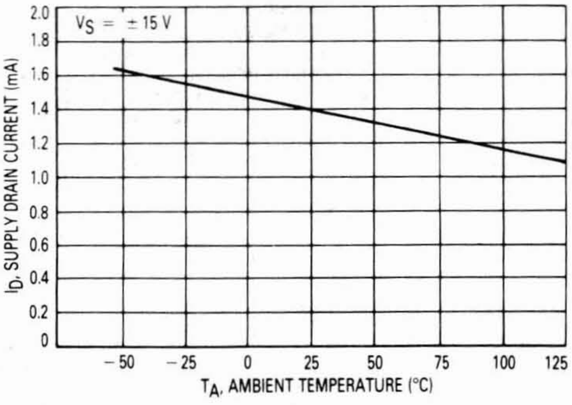


FIGURE 7 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

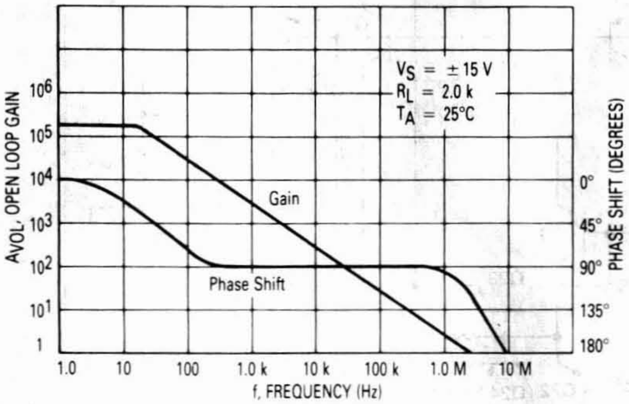


FIGURE 8 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

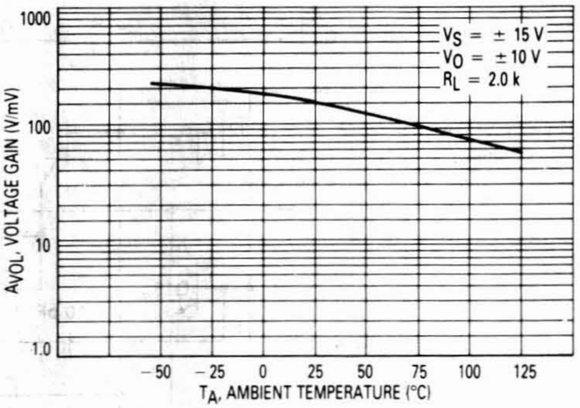


FIGURE 9 — NORMALIZED SLEW RATE versus TEMPERATURE

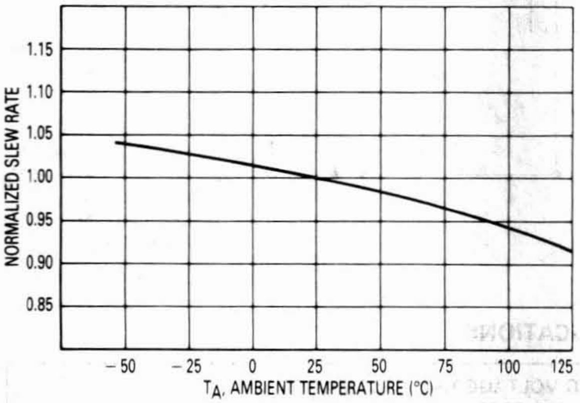


FIGURE 10 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

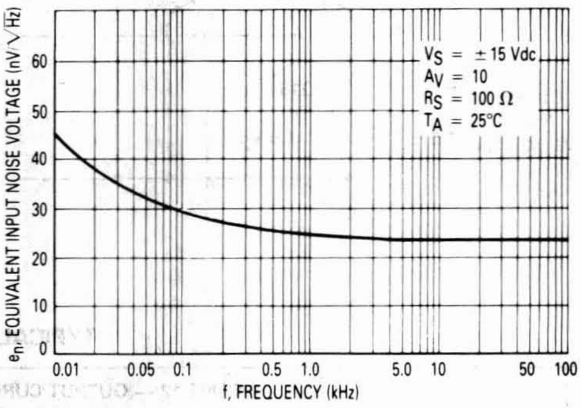
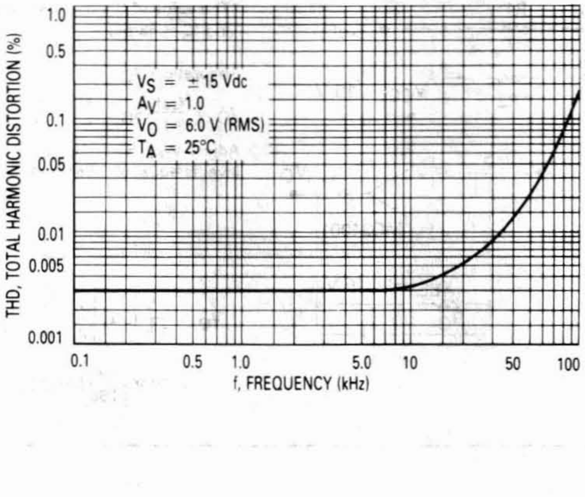
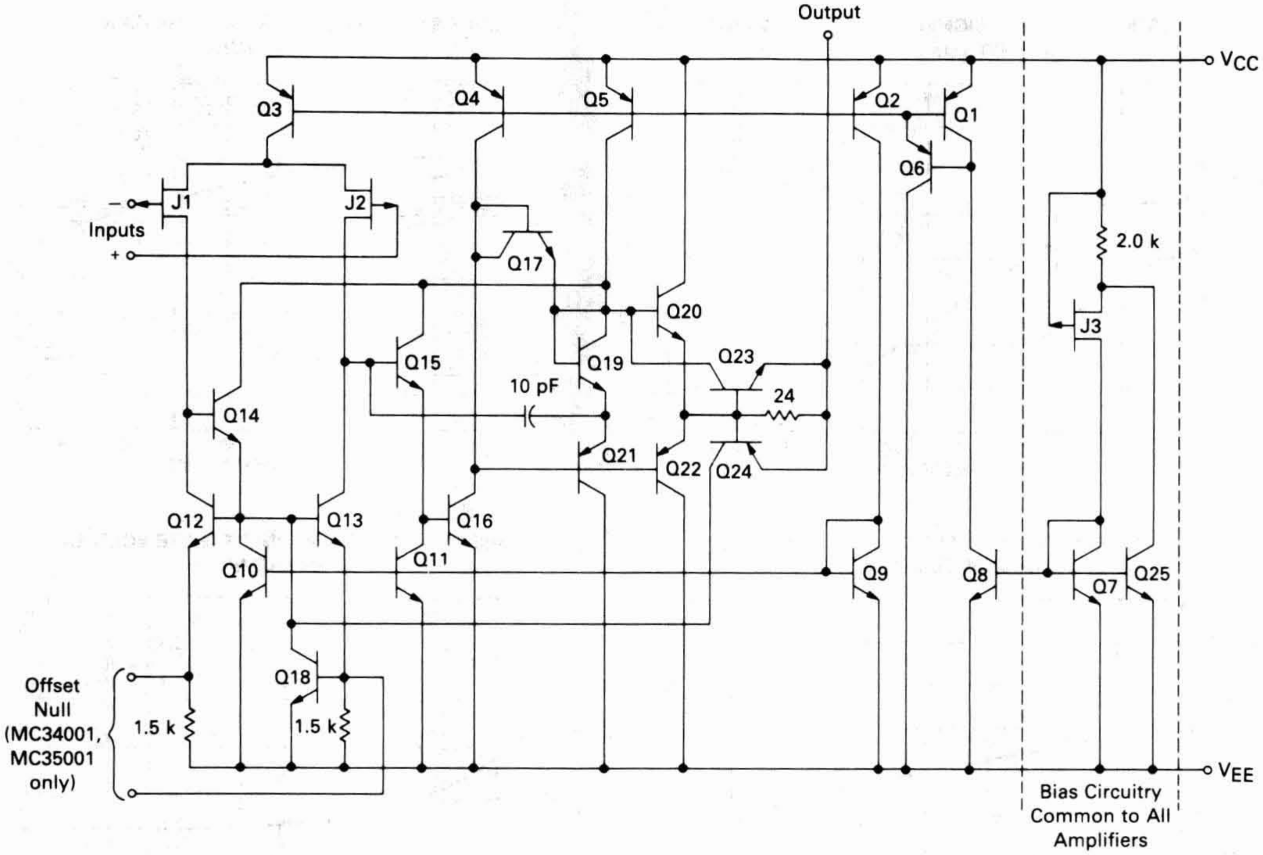


FIGURE 11 — TOTAL HARMONIC DISTORTION versus FREQUENCY



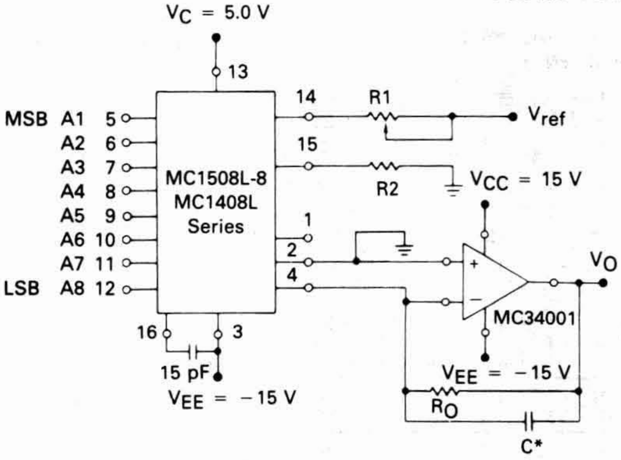
### REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)



Output
VCC
VEE
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
J1
J2
J3
−
Inputs
+
10 pF
24
2.0 k
1.5 k
1.5 k
Offset Null (MC34001, MC35001 only)
Bias Circuitry Common to All Amplifiers

## TYPICAL APPLICATIONS

### FIGURE 12 — OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



VC = 5.0 V
13
14
15
R1
Vref
R2
VCC = 15 V
MSB A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
LSB A8 12
MC1508L-8
MC1408L
Series
1
2
4
16
3
15 pF
VEE = −15 V
+
−
VO
MC34001
VEE = −15 V
RO
C*

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 µs from the time all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical $V_O$

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

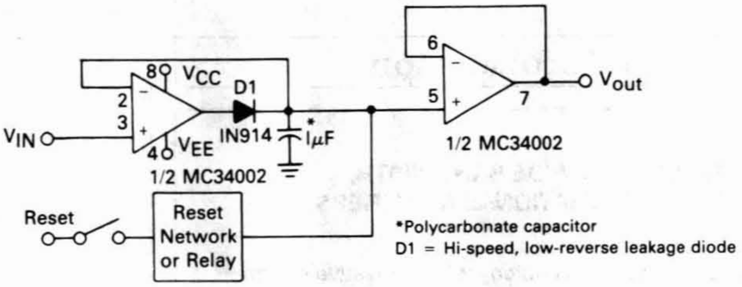
Adjust $V_{ref}$, R1 or $R_O$ so that $V_O$ with all digital inputs at high level is equal to 9.961 volts.

$V_{ref}$ = 2.0 Vdc
R1 = R2 ≈ 1.0 kΩ
$R_O$ = 5.0 kΩ

$$V_O = \frac{2\text{ V}}{1\text{ k}}(5\text{ k})\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10\text{ V}\left[\frac{255}{256}\right] = 9.961\text{ V}$$

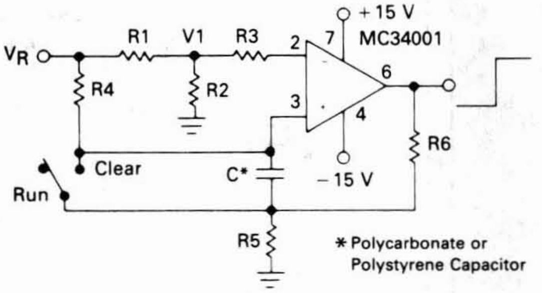
FIGURE 13 — POSITIVE PEAK DETECTOR



8
$V_{CC}$
D1
2
3
$V_{IN}$
4
$V_{EE}$
IN914
$1\mu F$
1/2 MC34002
6
5
7
$V_{out}$
1/2 MC34002
Reset
Reset Network or Relay

*Polycarbonate capacitor
D1 = Hi-speed, low-reverse leakage diode

FIGURE 14 — LONG INTERVAL RC TIMER



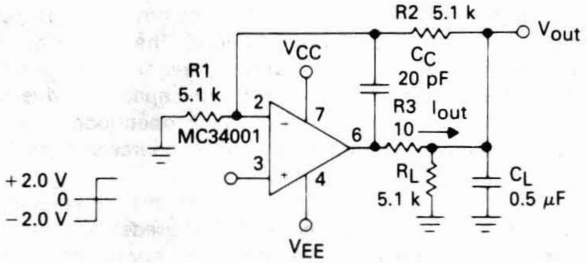
+15 V
$V_R$
R1
V1
R3
2
7
MC34001
6
R4
R2
3
4
R6
Clear
Run
C*
−15 V
R5

* Polycarbonate or Polystyrene Capacitor

Time (t) = R4 C ln $(V_R/V_R-V_I)$, $R_3 = R_4$, $R_5 = 0.1\ R_6$
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer
$V_R$ = 10 v  C = 1.0 μF  R3 = R4 = 144 M
R6 = 20 k  R5 = 2.0 k  R1 = R2 = 1.0 k

FIGURE 15 — ISOLATING LARGE CAPACITIVE LOADS

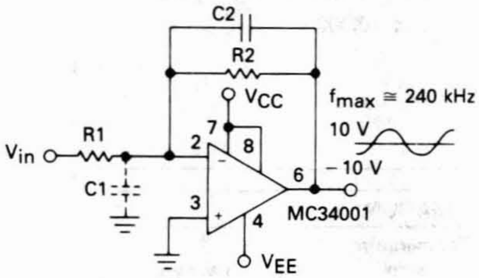


R2 5.1 k
$V_{out}$
$V_{CC}$
$C_C$
20 pF
R1
5.1 k
2
7
MC34001
R3
$I_{out}$
10
6
3
4
$R_L$
5.1 k
$C_L$
0.5 μF
+2.0 V
0
−2.0 V
$V_{EE}$

- Overshoot <10%
- $t_s$ = 10 μs
- When driving large $C_L$, the $V_{out}$ slew rate is determined by $C_L$ and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} = \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

FIGURE 16 — WIDE BW, LOW NOISE, LOW DRIFT AMPLIFIER



C2
R2
$V_{CC}$
$f_{max}$ ≅ 240 kHz
10 V
−10 V
R1
$V_{in}$
7
2
8
6
C1
3
4
MC34001
$V_{EE}$

- Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \cong 240$ kHz
- Parasitic input capacitance (C1 ≅ 3 pF plus any additional layout capacitance) interacts with feedback elements and creates undesirable high-frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

**MOTOROLA**

# MC34071, MC34072
# MC35071, MC35072
# MC33071, MC33072

## Advance Information

### HIGH SLEW RATE, WIDE BANDWIDTH, SINGLE SUPPLY OPERATIONAL AMPLIFIERS

A standard low-cost Bipolar technology with innovative design concepts are employed for the MC34071/MC34072 series of monolithic operational amplifiers. These devices offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate, and fast settling time without the use of JFET device technology. In addition, low input offset voltage can economically be achieved. Although these devices can be operated from split supplies, they are particularly suited for single supply operation, since the common mode input voltage range includes ground potential ($V_{EE}$). The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, also provides high capacitive drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC34071/MC34072 series of devices are available in standard or prime performance (A Suffix) grades and specified over commercial, industrial/vehicular or military temperature ranges.

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.10%
- Wide Single Supply Operating Range: 3.0 to 44 Volts
- Wide Input Common Mode Range Including Ground ($V_{EE}$)
- Low Input Offset Voltage: 1.5 mV Maximum (A Suffix)
- Large Output Voltage Swing: $-14.7$ V to $+14.0$ V for $V_S = \pm 15$ V
- Large Capacitance Drive Capability: 0 to 10,000 pF
- Low T.H.D. Distortion: 0.02%
- Excellent Phase Margins: 60°
- Excellent Gain Margin: 12 dB

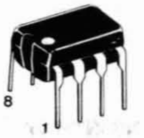
**ORDERING INFORMATION**

| Op Amp Function | Device | Temperature Range | Package |
|---|---|---|---|
| Single | MC35071U,AU | −55 to +125°C | Ceramic DIP |
| | MC33071U,AU | −40 to +85°C | Ceramic DIP |
| | MC33071P,AP | −40 to +85°C | Plastic DIP |
| | MC34071,D | 0 to +70°C | SO-8 |
| | MC34071U,AU | 0 to +70°C | Ceramic DIP |
| | MC34071P,AP | 0 to +70°C | Plastic DIP |
| Dual | MC35072U,AU | −55 to +125°C | Ceramic DIP |
| | MC33072U,AU | −40 to +85°C | Ceramic DIP |
| | MC33072P,AP | −40 to +85°C | Plastic DIP |
| | MC34072D | 0 to +70°C | SO-8 |
| | MC34072U,AU | 0 to +70°C | Ceramic DIP |
| | MC34072P,AP | 0 to +70°C | Plastic DIP |
| Quad | MC34074 Series | Refer to MC34074 Data Sheet | |

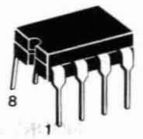
This document contains information on a new product. Specifications and information herein are subject to change without notice.

**HIGH PERFORMANCE SINGLE SUPPLY OPERATIONAL AMPLIFIERS**

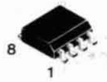
**SILICON MONOLITHIC INTEGRATED CIRCUIT**



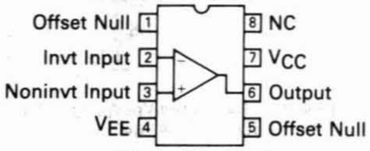
**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04



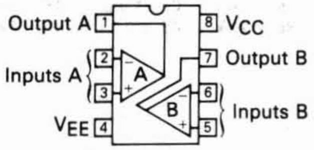
**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02



**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8

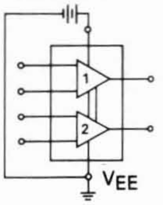


Single, Top View

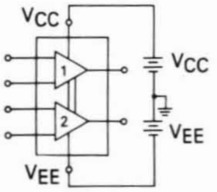


Dual, Top View

**SINGLE SUPPLY**
3.0 V to 44 V



**SPLIT SUPPLY**



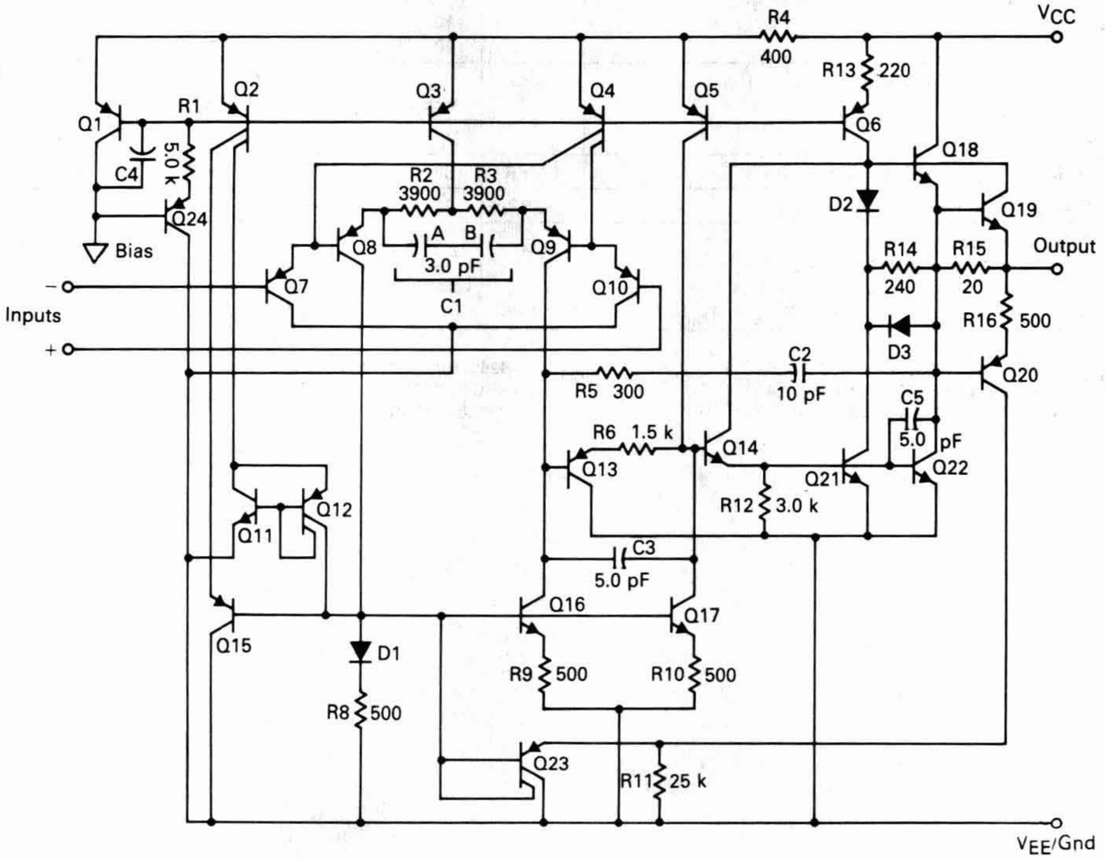
## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage (from $V_{CC}$ to $V_{EE}$) | $V_S$ | +44 | Volts |
| Input Differential Voltage Range | $V_{IDR}$ | Note 1 | Volts |
| Input Voltage Range | $V_{IR}$ | Note 1 | Volts |
| Output Short-Circuit Duration (Note 2) | $t_S$ | Indefinite | Seconds |
| Operating Ambient Temperature Range | $T_A$ | | °C |
| MC35071,A/MC35072,A | | −55 to +125 | |
| MC33071,A/MC33072,A | | −40 to +85 | |
| MC34071,A/MC34072,A | | 0 to +70 | |
| Operating Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range | $T_{stg}$ | | °C |
| Ceramic Package | | −65 to +150 | |
| Plastic Package | | −55 to +125 | |

**NOTES:**

1. Either or both input voltages must not exceed the magnitude of $V_{CC}$ or $V_{EE}$.
2. Power dissipation must be considered to ensure maximum junction temperature ($T_J$) is not exceeded.

**EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)**



$V_{CC}$
R4
400
R13
220
Q1
Q2
Q3
Q4
Q5
Q6
R1
C4
5.0 k
Q24
Bias
Q18
Q19
R2
3900
R3
3900
A
B
Q8
Q9
3.0 pF
C1
D2
R14
240
R15
20
Output
−
+
Inputs
Q7
Q10
R16
500
D3
C2
10 pF
R5
300
Q20
C5
5.0 pF
R6
1.5 k
Q14
Q13
Q21
Q22
R12
3.0 k
Q11
Q12
C3
5.0 pF
Q16
Q17
Q15
D1
R9
500
R10
500
R8
500
Q23
R11
25 k
$V_{EE}$/Gnd

**DC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ connected to ground, $T_A$ = $T_{low}$ to $T_{high}$ [Note 3] unless otherwise noted)

| | | MC3507_A/MC3407_A/ MC3307_A | | | MC3507_/MC3407_/ MC3307_ | | | |
|---|---|---|---|---|---|---|---|---|
| **Characteristic** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Input Offset Voltage ($V_{CM}$ = 0) | $V_{IO}$ | | | | | | | mV |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C | | — | 0.5 | 1.5 | — | 1.0 | 3.5 | |
| $V_{CC}$ = +5.0 V, $V_{EE}$ = 0 V, $T_A$ = +25°C | | — | 0.5 | 2.0 | — | 1.5 | 4.0 | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = $T_{low}$ to $T_{high}$ | | — | — | 3.5 | — | — | 5.5 | |
| Average Temperature Coefficient of Offset Voltage | $\Delta V_{IO}/\Delta T$ | — | 10 | — | — | 10 | — | μV/°C |
| Input Bias Current ($V_{CM}$ = 0) | $I_{IB}$ | | | | | | | nA |
| $T_A$ = +25°C | | — | 100 | 500 | — | 100 | 500 | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | — | — | 700 | — | — | 700 | |
| Input Offset Current ($V_{CM}$ = 0) | $I_{IO}$ | | | | | | | nA |
| $T_A$ = +25°C | | — | 6.0 | 50 | — | 6.0 | 75 | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | — | — | 300 | — | — | 300 | |
| Large Signal Voltage Gain<br>$V_O$ = ±10 V, $R_L$ = 2.0 k | $A_{VOL}$ | 50 | 100 | — | 25 | 100 | — | V/mV |
| Output Voltage Swing | $V_{OH}$ | | | | | | | V |
| $V_{CC}$ = +5.0 V, $V_{EE}$ = 0 V, $R_L$ = 2.0 k, $T_A$ = +25°C | | 3.7 | 4.0 | — | 3.7 | 4.0 | — | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ = 10 k, $T_A$ = +25°C | | 13.7 | 14 | — | 13.7 | 14 | — | |
| $V_{CC}$ = +15 V, $V_{EE}$ −15 V, $R_L$ = 2.0 k, $T_A$ = $T_{low}$ to $T_{high}$ | | 13.5 | — | — | 13.5 | — | — | |
| | $V_{OL}$ | | | | | | | |
| $V_{CC}$ = +5.0 V, $V_{EE}$ = 0 V, $R_L$ = 2.0 k, $T_A$ = +25°C | | — | 0.1 | 0.2 | — | 0.1 | 0.2 | |
| $V_{CC}$ = +15 V, $V_{EE}$ + −15 V, $R_L$ = 10 k, $T_A$ = +25°C | | — | −14.7 | −14.4 | — | −14.7 | −14.4 | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ = 2.0 k, $T_A$ = $T_{low}$ to $T_{high}$ | | — | — | −13.8 | — | — | −13.8 | |
| Output Short-Circuit Current ($T_A$ = +25°C)<br>Input Overdrive = 1.0 V, Output to Ground | $I_{SC}$ | | | | | | | mA |
| Source | | 10 | 30 | — | 10 | 30 | — | |
| Sink | | 20 | 47 | — | 20 | 47 | — | |
| Input Common Mode Voltage Range | $V_{ICR}$ | | | | | | | V |
| $T_A$ = +25°C | | $V_{EE}$ to ($V_{CC}$ − 1.8) | | | $V_{EE}$ to ($V_{CC}$ − 1.8) | | | |
| $T_A$ = $T_{low}$ to $T_{high}$ | | $V_{EE}$ to ($V_{CC}$ − 2.2) | | | $V_{EE}$ to ($V_{CC}$ − 2.2) | | | |
| Common Mode Rejection Ratio ($R_S$ ≤ 10 k) | CMRR | 80 | 97 | — | 70 | 97 | — | dB |
| Power Supply Rejection Ratio ($R_S$ = 100 Ω) | PSRR | 80 | 97 | — | 70 | 97 | — | dB |
| Power Supply Current (Per Amplifier) | $I_D$ | | | | | | | mA |
| $V_{CC}$ = +5.0 V, $V_{EE}$ = 0 V, $T_A$ = +25°C | | — | 1.6 | 2.0 | — | 1.6 | 2.0 | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C | | — | 1.9 | 2.5 | — | 1.9 | 2.5 | |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = $T_{low}$ to $T_{high}$ | | — | — | 2.8 | — | — | 2.8 | |

**NOTES:** (continued)

3. $T_{low}$ = −55°C for MC35071,A/MC35072,A
= −40°C for MC33071,A/MC33072,A
= 0°C for MC34071,A/MC34072,A

$T_{high}$ = +125°C for MC35071,A/35072,A
= +85°C for MC33071,A/33072,A
= +70°C for MC34071,A/34072,A

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ connected to ground, $T_A$ = +25°C unless otherwise noted)

| Characteristic | Symbol | MC3507_A/MC3407_A/ MC3307_A | | | MC3507_/MC3407_/ MC3307_ | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Slew Rate ($V_{in}$ = −10 V to +10 V, $R_L$ = 2.0 k, $C_L$ = 500 pF) | SR | | | | | | | V/µs |
| $A_V$ + 1.0 | | 8.0 | 10 | — | — | 10 | — | |
| $A_V$ − 1.0 | | — | 13 | — | — | 13 | — | |
| Settling Time (10 V Step, $A_V$ = −1.0) | $t_s$ | | | | | | | µs |
| To 0.10% (±1/2 LSB of 9-Bits) | | — | 1.1 | — | — | 1.1 | — | |
| To 0.01% (±1/2 LSB of 12-Bits) | | — | 2.2 | — | — | 2.2 | — | |
| Gain Bandwidth Product (f = 100 kHz) | GBW | 3.5 | 4.5 | — | | 4.5 | — | MHz |
| Power Bandwidth $A_V$ = +1.0, $R_L$ = 2.0 k, $V_O$ = 20 $V_{p-p}$, THD = 5.0% | BWp | — | 200 | — | — | 200 | — | kHz |
| Phase Margin | $\phi m$ | | | | | | | Degrees |
| $R_L$ = 2.0 k | | — | 60 | — | — | 60 | — | |
| $R_L$ = 2.0 k, $C_L$ = 300 pF | | — | 40 | — | — | 40 | — | |
| Gain Margin | $A_m$ | | | | | | | dB |
| $R_L$ = 2.0 k | | — | 12 | — | — | 12 | — | |
| $R_L$ = 2.0 k, $C_L$ = 300 pF | | — | 4.0 | — | — | 4.0 | — | |
| Equivalent Input Noise Voltage $R_S$ = 100 Ω, f = 1.0 kHz | $e_n$ | — | 32 | — | — | 32 | — | nV/ $\sqrt{Hz}$ |
| Equivalent Input Noise Current (f = 1.0 kHz) | $I_n$ | — | 0.22 | — | — | 0.22 | — | pA/ $\sqrt{Hz}$ |
| Input Capacitance | $C_i$ | — | 0.8 | — | — | 0.8 | — | pF |
| Total Harmonic Distortion $A_V$ = +10, $R_L$ = 2.0 k, 2.0 ≤ $V_O$ ≤ 20 $V_{p-p}$, f = 10 kHz | THD | — | 0.02 | — | — | 0.02 | — | % |
| Channel Separation (f = 10 kHz, MC34072,A Only) | — | — | 120 | — | — | 120 | — | dB |
| Open-Loop Output Impedance (f = 1.0 MHz) | $z_o$ | — | 30 | — | — | 30 | — | Ω |

**For typical performance curves and applications information refer to MC34074 series data sheet.**

**MOTOROLA**

# MC34074,A
# MC35074,A
# MC33074,A

## HIGH SLEW RATE, WIDE BANDWIDTH, SINGLE SUPPLY QUAD OPERATIONAL AMPLIFIER

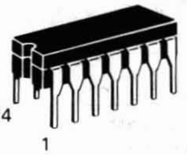
A standard low-cost Bipolar technology with innovative design concepts is employed for the MC34074 series of monolithic quad operational amplifiers. These devices offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate, and fast settling time without the use of JFET device technology. In addition, low input offset voltage can economically be achieved. Although these devices can be operated from split supplies, they are particularly suited for single supply operation, since the common mode input voltage range includes ground potential ($V_{EE}$). The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, also provides high capacitive drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC34074/33074/35074 series of devices are available in standard or prime performance (A Suffix) grades and specified over commercial, industrial/vehicular or military temperature ranges.

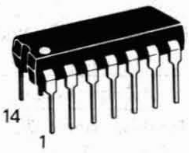
- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.10%
- Wide Single Supply Operating Range: 3.0 to 44 Volts
- Wide Input Common Mode Range Including Ground ($V_{EE}$)
- Low Input Offset Voltage: 2.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14.0 V for $V_S = \pm 15$ V
- Large Capacitance Drive Capability: 0 to 10,000 pF
- Low T.H.D. Distortion: 0.02%
- Excellent Phase Margins: 60°
- Excellent Gain Margin: 12 dB

## QUAD HIGH PERFORMANCE SINGLE SUPPLY OPERATIONAL AMPLIFIERS

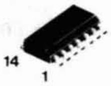
### SILICON MONOLITHIC INTEGRATED CIRCUIT



**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
TO-116
(MO-001 AA)

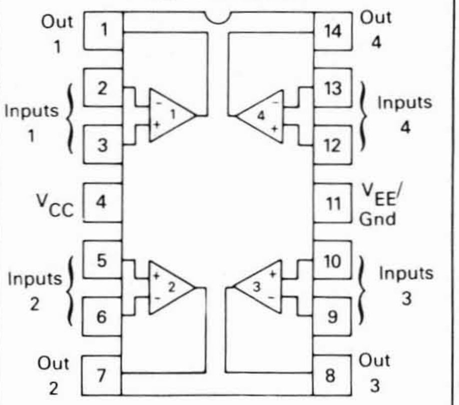


**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05



**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14

**PIN CONNECTIONS**

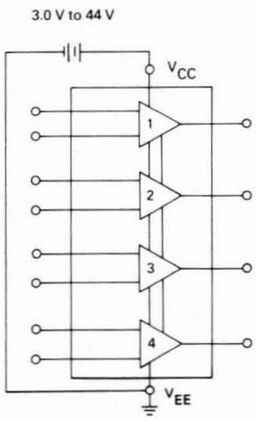


(Top View)

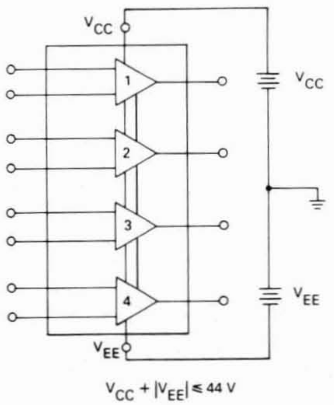
**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC35074L,AL | −55 to +125°C | Ceramic DIP |
| MC33074L,AL | −40 to +85°C | Ceramic DIP |
| MC33074P,AP | −40 to +85°C | Plastic DIP |
| MC34074L,AL | 0 to +70°C | Ceramic DIP |
| MC34074P,AP | 0 to +70°C | Plastic DIP |
| MC34074D,AD | 0 to +70°C | SO-14 |

**SINGLE SUPPLY**



**SPLIT SUPPLIES**



## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage (from $V_{CC}$ to $V_{EE}$) | $V_S$ | +44 | Volts |
| Input Differential Voltage Range | $V_{IDR}$ | Note 1 | Volts |
| Input Voltage Range | $V_{IR}$ | Note 1 | Volts |
| Output Short-Circuit Duration (Note 2) | $t_S$ | Indefinite | Seconds |
| Operating Ambient Temperature Range<br>MC35074,A<br>MC33074,A<br>MC34074,A | $T_A$ | <br>−55 to +125<br>−40 to +85<br>0 to +70 | °C |
| Operating Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range<br>Ceramic Package<br>Plastic Package | $T_{stg}$ | <br>−65 to +150<br>−55 to +125 | °C |

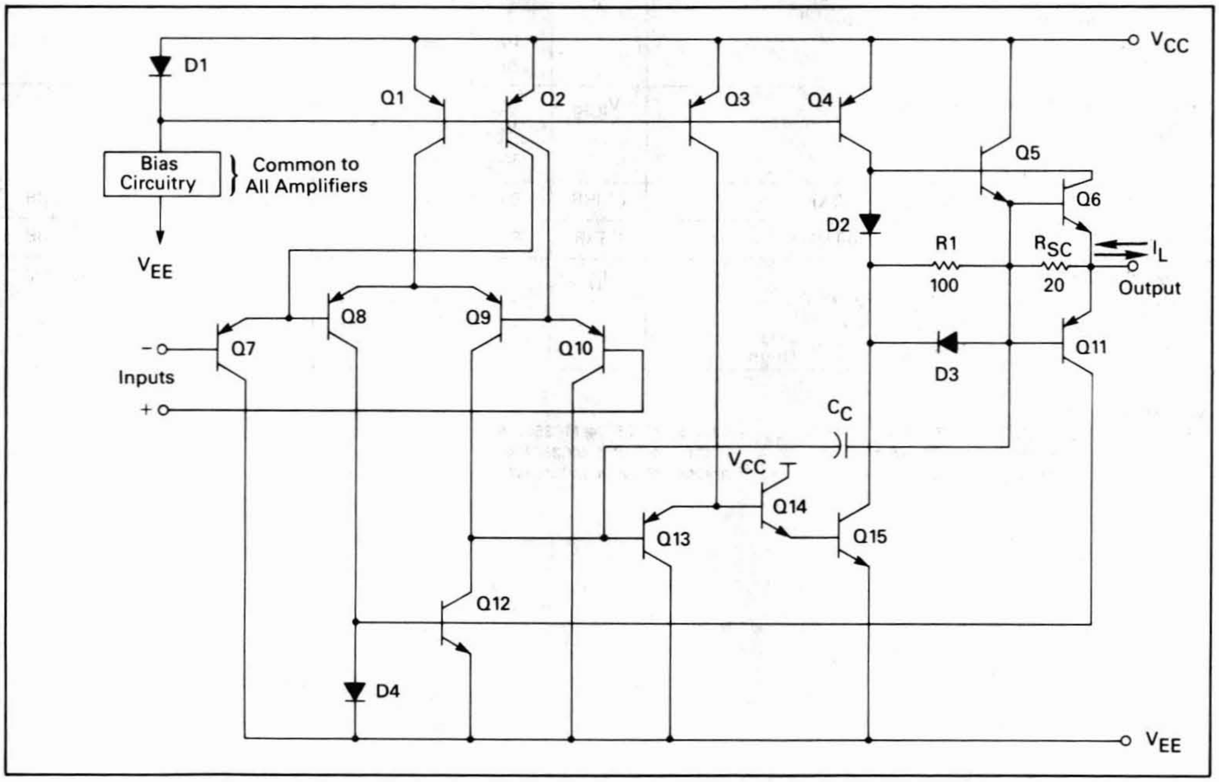
## MAXIMUM DEVICE POWER DISSIPATION

| Ambient Temperature | +25°C | +70°C | +85°C | +125°C | °C |
|---|---|---|---|---|---|
| Power Dissipation | 1250 | 800 | 650 | 250 | mW |

**NOTES:**

1. Either or both input voltages must not exceed the magnitude of $V_{CC}$ or $V_{EE}$.
2. Power dissipation must be considered to ensure maximum junction temperature ($T_J$) is not exceeded.

**EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)**


$V_{CC}$
D1
Q1
Q2
Q3
Q4
Q5
Q6
Bias Circuitry
Common to All Amplifiers
$V_{EE}$
D2
R1
100
$R_{SC}$
20
$I_L$
Output
Q8
Q9
−
Q7
Q10
Q11
Inputs
+
D3
$C_C$
$V_{CC}$
Q14
Q13
Q15
Q12
D4
$V_{EE}$

**DC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ connected to ground, $T_A$ = $T_{low}$ to $T_{high}$ [Note 3] unless otherwise noted)

| Characteristic | Symbol | MC35074A/34074A/ 33074A |  |  | MC35074/34074/33074 |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage ($V_{CM}$ = 0) | $V_{IO}$ |  |  |  |  |  |  | mV |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C |  | — | 0.5 | 2.0 | — | 2.0 | 4.5 |  |
| $V_{CC}$ = +5.0 V, $V_{EE}$ = 0 V, $T_A$ = +25°C |  | — | 0.5 | 2.5 | — | 2.5 | 5.0 |  |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = $T_{low}$ to $T_{high}$ |  | — | — | 4.0 | — | — | 6.5 |  |
| Average Temperature Coefficient of Offset Voltage | $\Delta V_{IO}/\Delta T$ | — | 10 | — | — | 10 | — | μV/°C |
| Input Bias Current ($V_{CM}$ = 0) | $I_{IB}$ |  |  |  |  |  |  | nA |
| $T_A$ = +25°C |  | — | 100 | 500 | — | 100 | 500 |  |
| $T_A$ = $T_{low}$ to $T_{high}$ |  | — | — | 700 | — | — | 700 |  |
| Input Offset Current ($V_{CM}$ = 0) | $I_{IO}$ |  |  |  |  |  |  | nA |
| $T_A$ = +25°C |  | — | 6.0 | 50 | — | 6.0 | 75 |  |
| $T_A$ = $T_{low}$ to $T_{high}$ |  | — | — | 300 | — | — | 300 |  |
| Large Signal Voltage Gain<br>$V_O$ = ±10 V, $R_L$ = 2.0 k | $A_{VOL}$ | 50 | 100 | — | 25 | 100 | — | V/mV |
| Output Voltage Swing | $V_{OH}$ |  |  |  |  |  |  | V |
| $V_{CC}$ = +5.0 V, $V_{EE}$ = 0 V, $R_L$ = 2.0 k, $T_A$ = +25°C |  | 3.7 | 4.0 | — | 3.7 | 4.0 | — |  |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ = 10 k, $T_A$ = +25°C |  | 13.7 | 14 | — | 13.7 | 14 | — |  |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ = 2.0 k, $T_A$ = $T_{low}$ to $T_{high}$ |  | 13.5 | — | — | 13.5 | — | — |  |
| $V_{CC}$ = +5.0 V, $V_{EE}$ = 0 V, $R_L$ = 2.0 k, $T_A$ = +25°C | $V_{OL}$ | — | 0.1 | 0.2 | — | 0.1 | 0.2 |  |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ = 10 k, $T_A$ = +25°C |  | — | −14.7 | −14.4 | — | −14.7 | −14.4 |  |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ = 2.0 k, $T_A$ = $T_{low}$ to $T_{high}$ |  | — | — | −13.8 | — | — | −13.8 |  |
| Output Short-Circuit Current ($T_A$ = +25°C)<br>Input Overdrive = 1.0 V, Output to Ground | $I_{SC}$ |  |  |  |  |  |  | mA |
| Source |  | 10 | 30 | — | 10 | 30 | — |  |
| Sink |  | 20 | 47 | — | 20 | 47 | — |  |
| Input Common Mode Voltage Range | $V_{ICR}$ |  |  |  |  |  |  | V |
| $T_A$ = +25°C |  | $V_{EE}$ to ($V_{CC}$ − 1.8) |  |  | $V_{EE}$ to ($V_{CC}$ − 1.8) |  |  |  |
| $T_A$ = $T_{low}$ to $T_{high}$ |  | $V_{EE}$ to ($V_{CC}$ − 2.2) |  |  | $V_{EE}$ to ($V_{CC}$ − 2.2) |  |  |  |
| Common Mode Rejection Ratio ($R_S$ ≤ 10 k) | CMRR | 80 | 97 | — | 70 | 97 | — | dB |
| Power Supply Rejection Ratio ($R_S$ = 100 Ω) | PSRR | 80 | 97 | — | 70 | 97 | — | dB |
| Power Supply Current | $I_D$ |  |  |  |  |  |  | mA |
| $V_{CC}$ = +5.0 V, $V_{EE}$ = 0 V, $T_A$ = +25°C |  | — | 6.5 | 8.0 | — | 6.5 | 8.0 |  |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C |  | — | 7.5 | 10 | — | 7.5 | 10 |  |
| $V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = $T_{low}$ to $T_{high}$ |  | — | — | 11 | — | — | 11 |  |

**NOTES**: (continued)

3. $T_{low}$ = −55°C for MC35074, MC35074A $T_{high}$ = +125°C for MC35074, MC35074A
= −40°C for MC33074, MC33074A = +85°C for MC33074, MC33074A
= 0°C for MC34074, MC34074A = +70°C for MC34074, MC34074A

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $R_L$ connected to ground, $T_A$ = +25°C unless otherwise noted)

| Characteristic | Symbol | MC35074A/34074A/ 33074A | | | MC35074/34074/33074 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Slew Rate ($V_{in}$ = −10 V to +10 V, $R_L$ = 2.0 k, $C_L$ = 500 pF) | SR | | | | | | | V/μs |
| $A_V$ +1 | | 8.0 | 10 | — | — | 10 | — | |
| $A_V$ −1 | | — | 13 | — | — | 13 | — | |
| Settling Time (10 V Step, $A_V$ = −1.0) | $t_s$ | | | | | | | μs |
| To 0.10% (± ½ LSB of 9-Bits) | | — | 1.1 | — | — | 1.1 | — | |
| To 0.01% (± ½ LSB of 12-Bits) | | — | 2.2 | — | — | 2.2 | — | |
| Gain Bandwidth Product (f = 100 kHz) | GBW | 3.5 | 4.5 | — | — | 4.5 | — | MHz |
| Power Bandwidth ($A_V$ = +1.0, $R_L$ = 2.0 k, $V_O$ = 20 $V_{P-P}$, THD = 5.0%) | BWp | — | 200 | — | — | 200 | — | kHz |
| Phase Margin | φm | | | | | | | Degrees |
| $R_L$ = 2.0 k | | — | 60 | — | — | 60 | — | |
| $R_L$ = 2.0 k, $C_L$ = 300 pF | | — | 40 | — | — | 40 | — | |
| Gain Margin | $A_m$ | | | | | | | dB |
| $R_L$ = 2.0 k | | — | 12 | — | — | 12 | — | |
| $R_L$ = 2.0 k, $C_L$ = 300 pF | | — | 4.0 | — | — | 4.0 | — | |
| Equivalent Input Noise Voltage $R_S$ = 100 Ω, f = 1.0 kHz | $e_n$ | — | 32 | — | — | 32 | — | nV/ $\sqrt{Hz}$ |
| Equivalent Input Noise Current (f = 1.0 kHz) | $I_n$ | — | 0.22 | — | — | 0.22 | — | pA/ $\sqrt{Hz}$ |
| Input Capacitance | $C_i$ | — | 0.8 | — | — | 0.8 | — | pF |
| Total Harmonic Distortion $A_V$ = +10, $R_L$ = 2.0 k, 2.0 ≤ $V_O$ ≤ 20 $V_{P-P}$, f = 10 kHz | THD | — | 0.02 | — | — | 0.02 | — | % |
| Channel Separation (f = 10 kHz) | — | — | 120 | — | — | 120 | — | dB |
| Open-Loop Output Impedance (f = 1.0 MHz) | $z_o$ | — | 30 | — | — | 30 | — | Ω |

**TYPICAL PERFORMANCE CURVES**

**FIGURE 1—INPUT OFFSET VOLTAGE versus TEMPERATURE FOR REPRESENTATIVE UNITS**

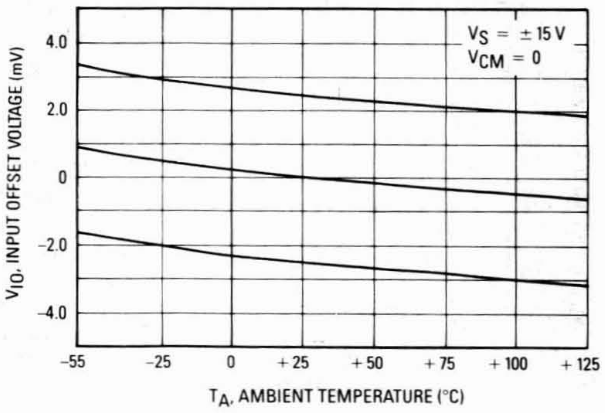


**FIGURE 2—INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE**

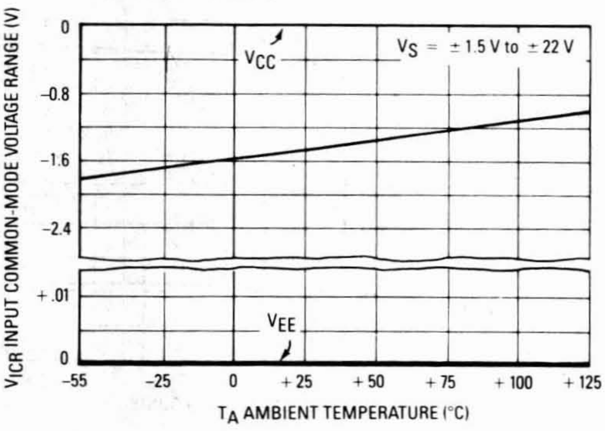


FIGURE 3—NORMALIZED INPUT BIAS CURRENT versus TEMPERATURE

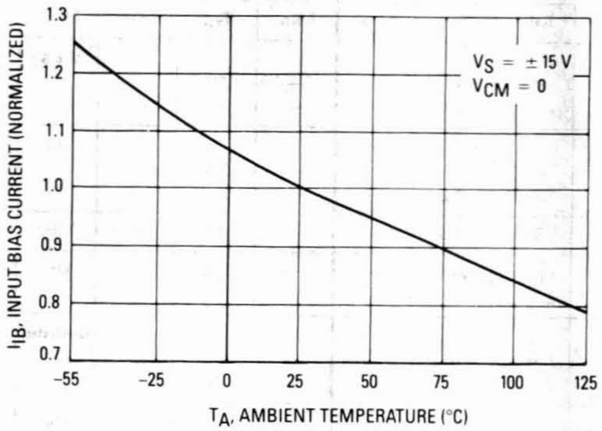


FIGURE 4—NORMALIZED INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

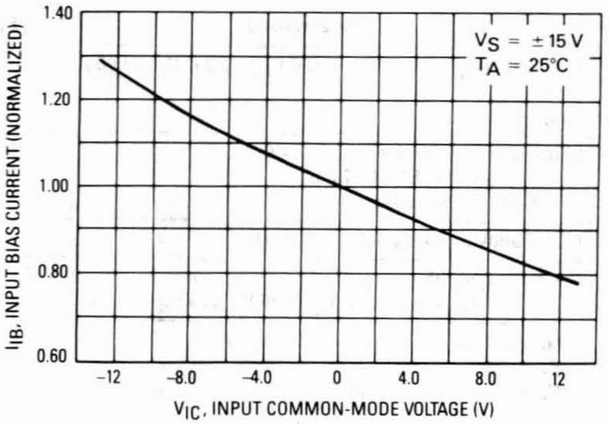


FIGURE 5—SPLIT SUPPLY OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

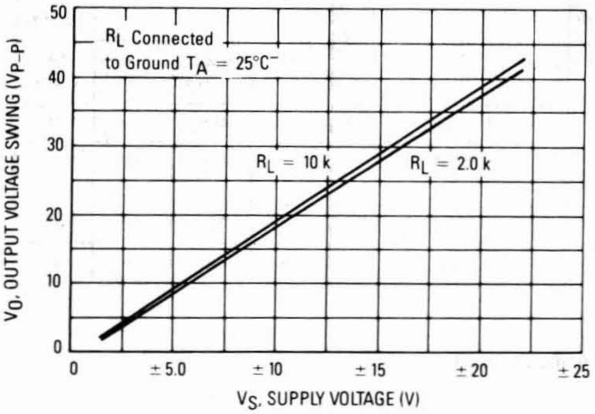


FIGURE 6—SPLIT SUPPLY OUTPUT SATURATION versus LOAD CURRENT

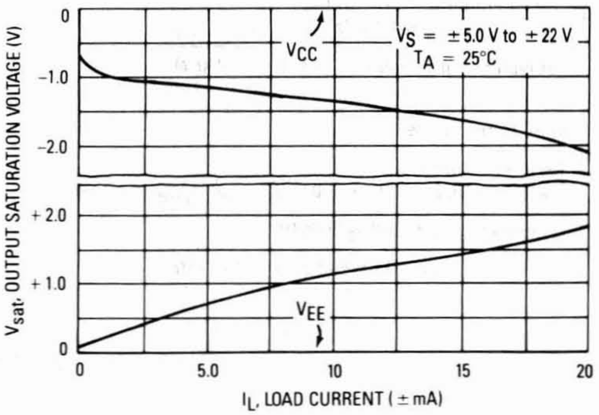


FIGURE 7—SINGLE SUPPLY OUTPUT SATURATION versus LOAD RESISTANCE TO GROUND

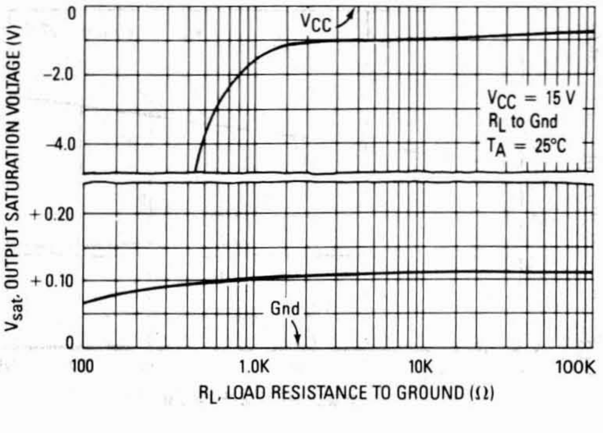


FIGURE 8—SINGLE SUPPLY OUTPUT SATURATION versus LOAD RESISTANCE TO $V_{CC}$

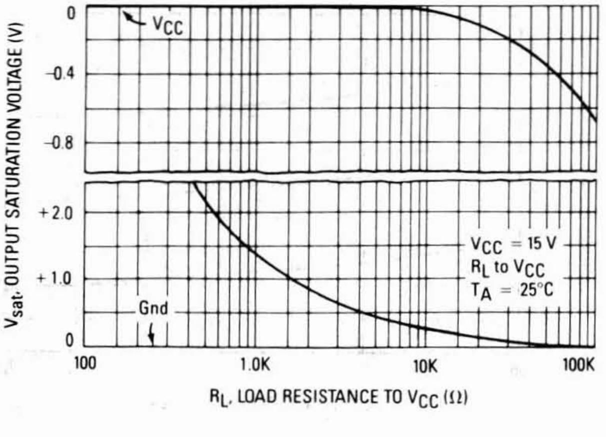


**FIGURE 9—OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE**

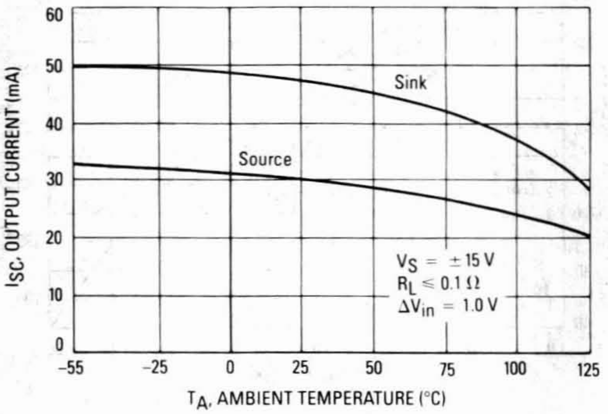


**FIGURE 10—OUTPUT IMPEDANCE versus FREQUENCY**

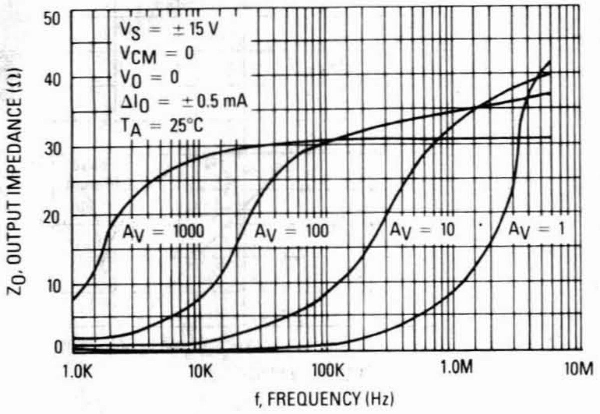


**FIGURE 11—OUTPUT VOLTAGE SWING versus FREQUENCY**

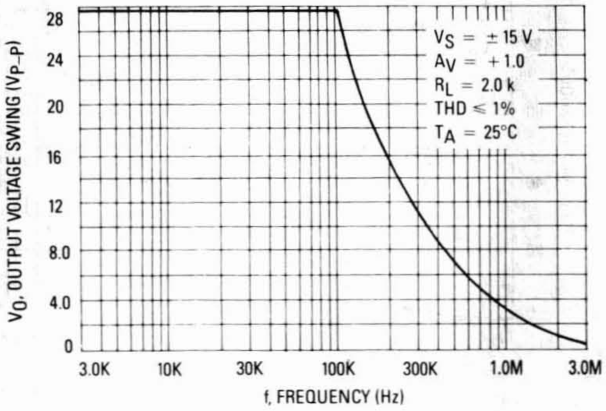


**FIGURE 12—OUTPUT DISTORTION versus FREQUENCY**

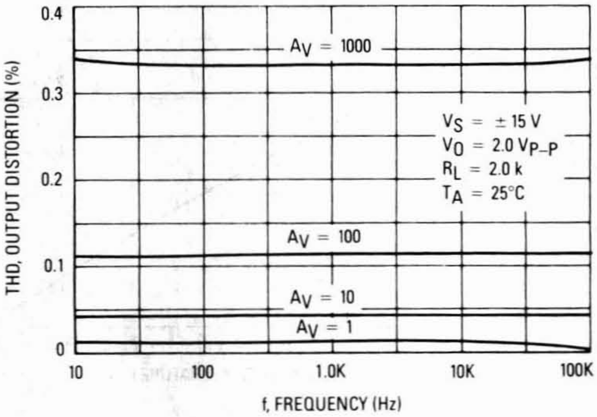


**FIGURE 13—OUTPUT DISTORTION versus OUTPUT VOLTAGE SWING**

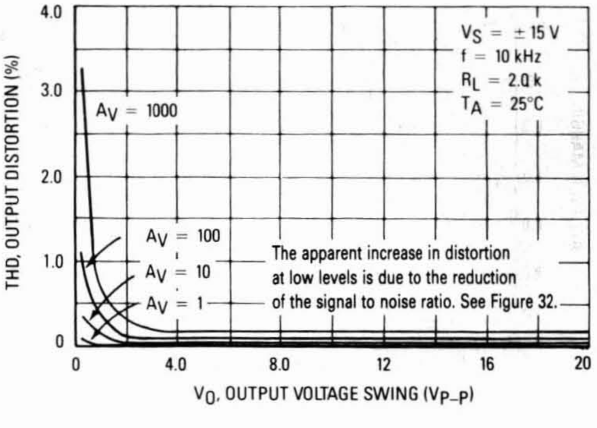


**FIGURE 14—OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE**

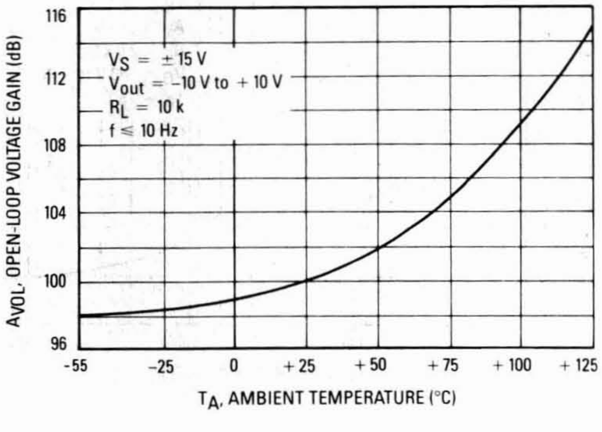


**FIGURE 15—OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY**

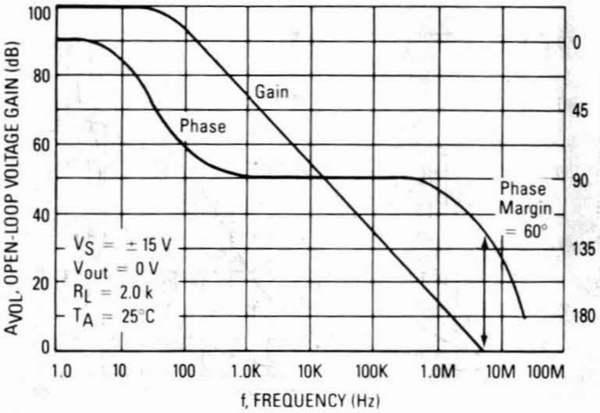


**FIGURE 16—OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY**

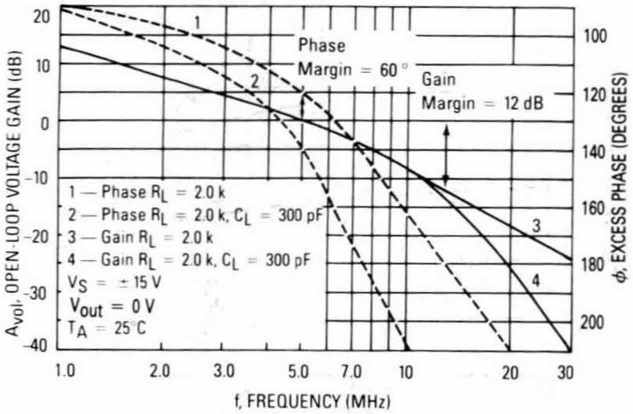


**FIGURE 17—NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE**

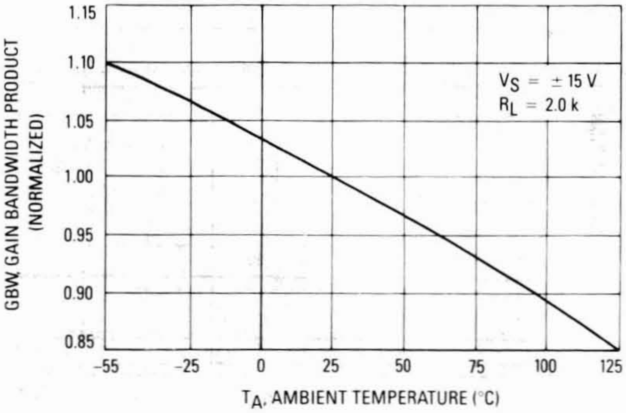


**FIGURE 18—PERCENT OVERSHOOT versus LOAD CAPACITANCE**

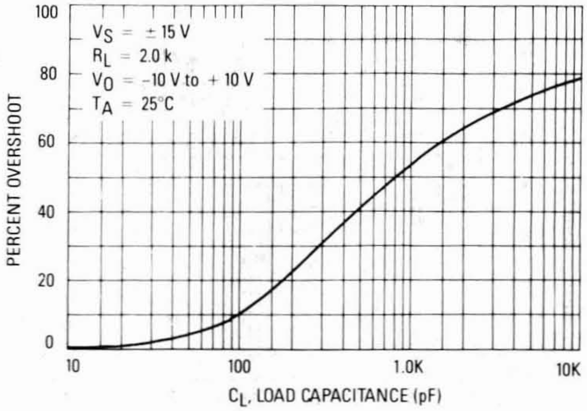


**FIGURE 19—PHASE MARGIN versus LOAD CAPACITANCE**

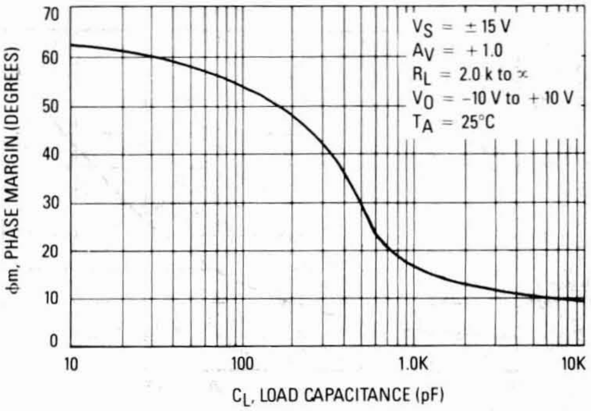


**FIGURE 20—GAIN MARGIN versus LOAD CAPACITANCE**

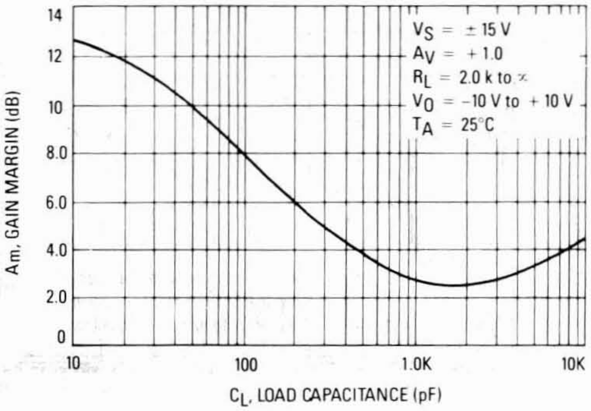


FIGURE 21—PHASE MARGIN versus TEMPERATURE

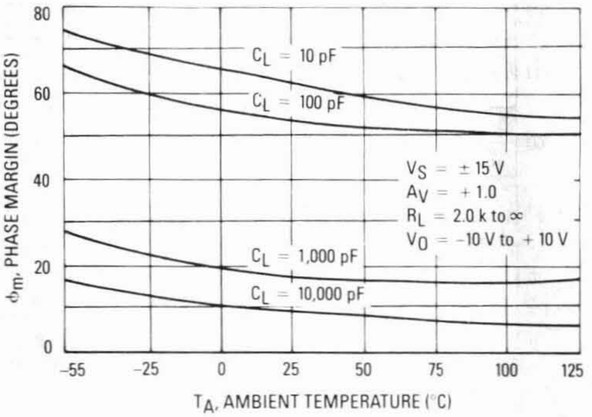


FIGURE 22—GAIN MARGIN versus TEMPERATURE

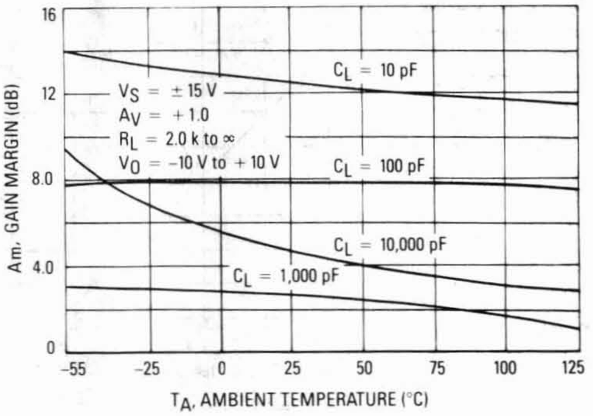


FIGURE 23—NORMALIZED SLEW RATE versus TEMPERATURE

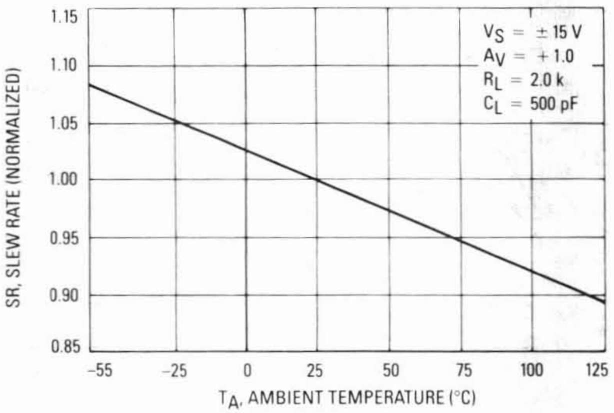


FIGURE 24—OUTPUT SETTLING TIME

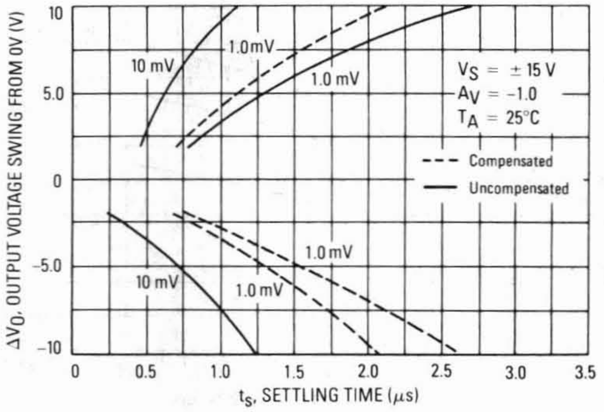


FIGURE 25—SMALL-SIGNAL TRANSIENT RESPONSE

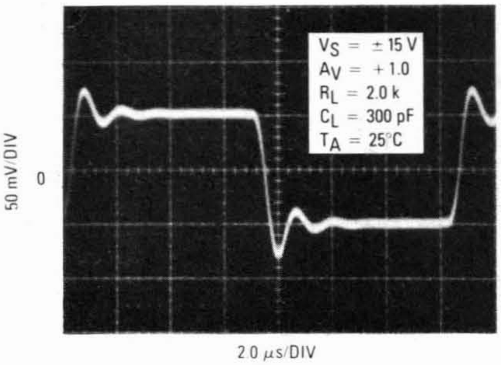


FIGURE 26—LARGE-SIGNAL TRANSIENT RESPONSE

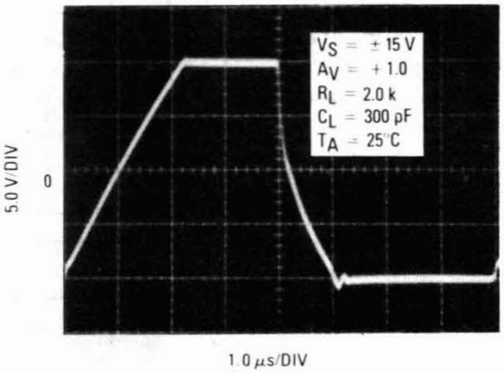


**FIGURE 27—COMMON-MODE REJECTION RATIO versus FREQUENCY**

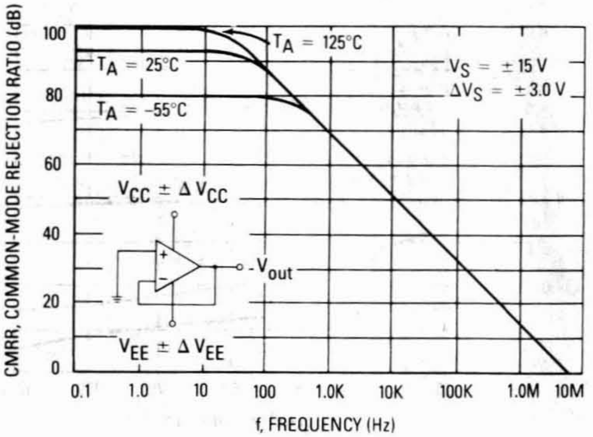


**FIGURE 28—POWER SUPPLY REJECTION RATIO versus FREQUENCY**

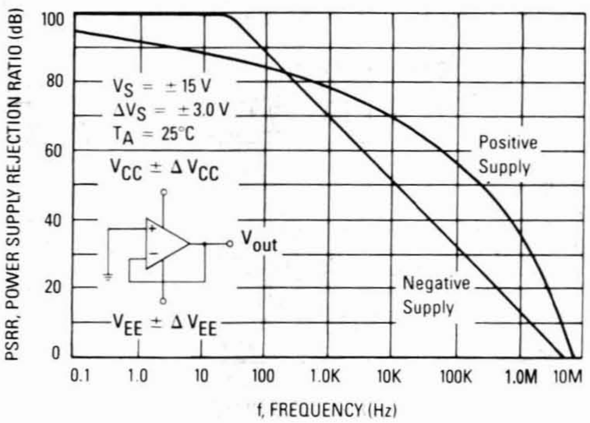


**FIGURE 29—SUPPLY CURRENT versus SUPPLY VOLTAGE**

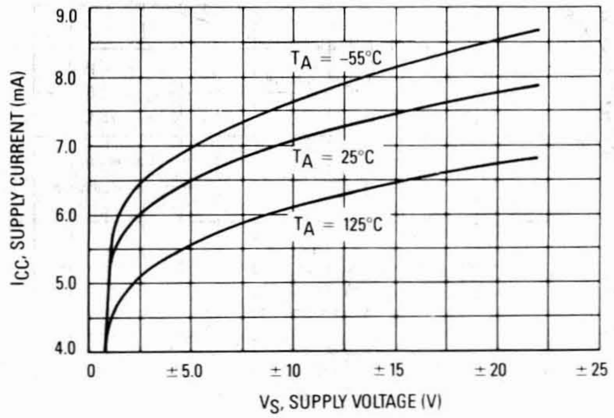


**FIGURE 30—POWER SUPPLY REJECTION RATIO versus TEMPERATURE**

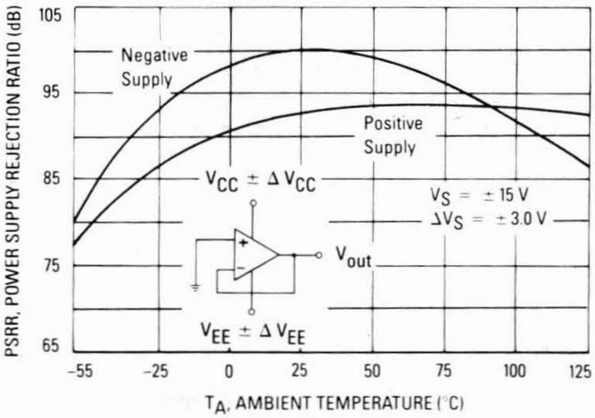


**FIGURE 31—CHANNEL SEPARATION versus FREQUENCY**

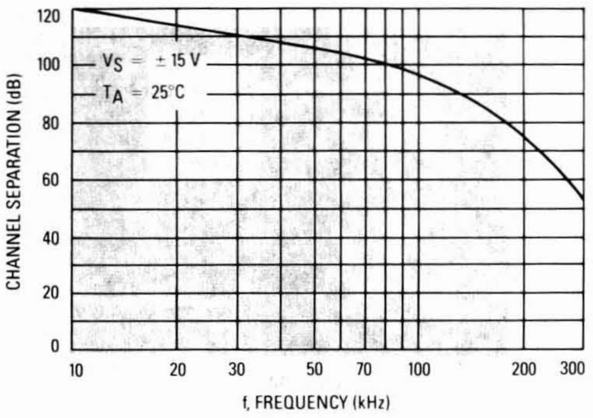
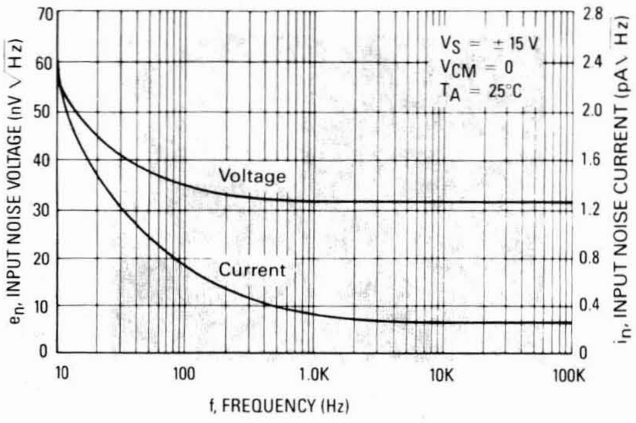


**FIGURE 32—SPECTRAL NOISE DENSITY**



## APPLICATIONS INFORMATION
## CIRCUIT DESCRIPTION/PERFORMANCE FEATURES OF THE MC34074 FAMILY

Although the bandwidth, slew rate, and settling time of the MC34074 amplifier family is similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the $V_{EE}$ potential, single supply operation is feasible to as low as 3.0 volts with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 volts, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between $V_{EE}$ and $V_{CC}$ supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the $V_{CC}$ voltage by approximately 3.0 volts and decrease below the $V_{EE}$ voltage by 0.3 volts without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from $V_{EE}$ through either input's clamping diode without damage or latching, although phase reversal may again occur.

If at least one input is within the common mode input voltage range and the other input is within the maximum input voltage range, no phase reversal will occur. If both inputs exceed the upper common mode input voltage limit, the output will be forced to its lowest voltage state.

Since the input capacitance associated with the small geometry input device is substantially lower (0.8 pF) than the typical JFET input gate capacitance (3.0 pF), better frequency response for a given input source resistance can be achieved using the MC34074 amplifiers. This performance feature becomes evident, for example, in fast settling D-to-A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DAC's). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 kΩ of feedback resistance, the MC34074 family can typically settle to within 1/2 LSB of 8 bits in 1.0 µs, and within 1/2 LSB of 12 bits in 2.2 µs for a 10 volt step. In a typical inverting unity gain fast settling configuration, the typical symmetrical slew rate is ±13 volts/µs. In the classic non-inverting unity gain configuration the typical output positive slew rate is +10 volts/µs, and the corresponding negative slew rate will typically exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are typically superior to that of JFETs, a low untrimmed maximum offset voltage of 2.0 mV prime and 4.5 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low-cost precision, high-speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can typically swing within 1.0 volt of the positive rail ($V_{CC}$), and within 0.3 volts of the negative rail ($V_{EE}$), providing a 28.7 Vp-p swing from ±15 volt supplies. This large output swing becomes most noticable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q4, and $V_{BE}$ of the NPN pull up transistor Q5, and the voltage drop associated with the short circuit resistance, $R_{SC}$. The negative swing is limited by the saturation voltage of the pull-down transistor Q15, the voltage drop $I_L R_1$, and the voltage drop associated with resistance $R_{SC}$, where $I_L$ is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of $V_{EE}$. For large valued sink currents (>5.0 mA), diode D3 clamps the voltage across $R_1$, thus limiting the negative swing to the saturation voltage of Q15, plus the forward diode drop of D3 ($\approx V_{EE} + 1.0$ V). Thus for a given supply voltage, unprecedented peak-to-peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to $V_{CC}$ instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to $V_{CC}$ during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter-follower transistor has been eliminated, the MC34074 family offers a 20 mA minimum current sink capability, typically to an output voltage of ($V_{EE}$ + 1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain-bandwidth product and fast settling capability. The associated high frequency low output impedance (30 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 to 10,000 pF without oscillation in the unity closed loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34074 family also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specification is defined at 5.0 volts, these amplifiers are functional to at least 3.0 volts @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and dc gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

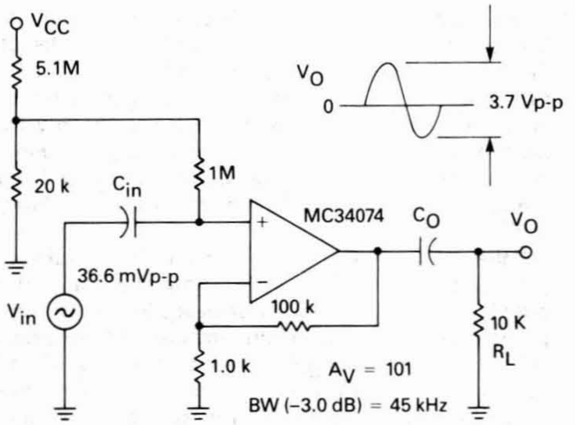
Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ± 15 volt supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

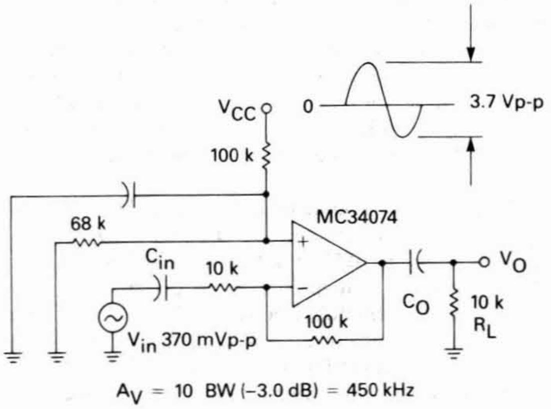
## TYPICAL SINGLE SUPPLY APPLICATIONS $V_{CC}$ = 5.0 VOLTS

FIGURE 33 — AC COUPLED NONINVERTING AMPLIFIER



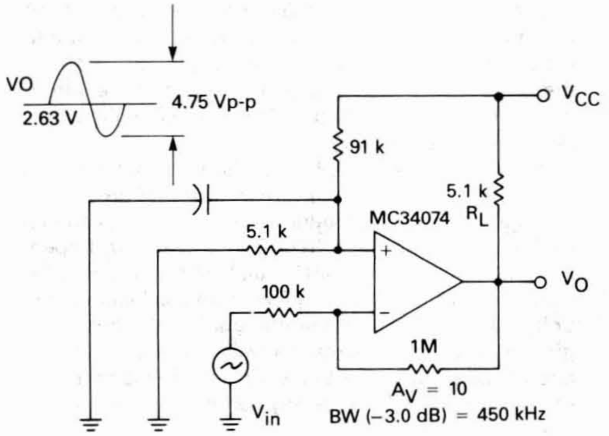
VCC
5.1M
VO
0
3.7 Vp-p
20 k
Cin
1M
MC34074
CO
VO
36.6 mVp-p
Vin
100 k
10 K
RL
1.0 k
AV = 101
BW (-3.0 dB) = 45 kHz

FIGURE 34 — AC COUPLED INVERTING AMPLIFIER



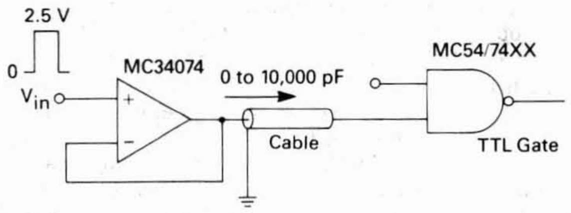
VCC
0
3.7 Vp-p
100 k
68 k
MC34074
Cin
10 k
VO
CO
10 k
RL
100 k
Vin 370 mVp-p
AV = 10 BW (-3.0 dB) = 450 kHz

FIGURE 35 — DC COUPLED INVERTING AMPLIFIER MAXIMUM OUTPUT SWING



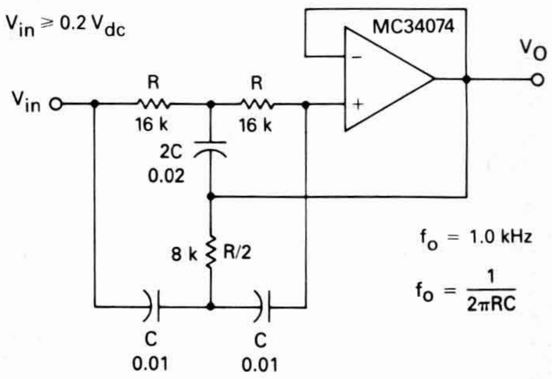
VO
2.63 V
4.75 Vp-p
VCC
91 k
5.1 k
RL
5.1 k
MC34074
100 k
VO
1M
AV = 10
Vin
BW (-3.0 dB) = 450 kHz

FIGURE 36 — UNITY GAIN BUFFER TTL DRIVER



2.5 V
0
Vin
MC34074
0 to 10,000 pF
Cable
MC54/74XX
TTL Gate

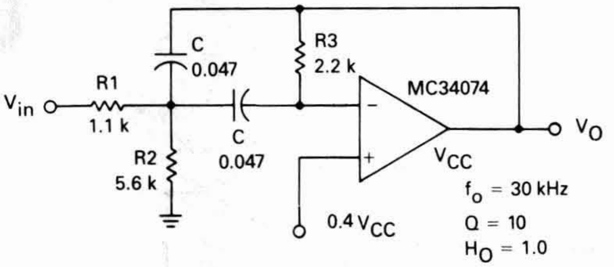
FIGURE 37 — ACTIVE HIGH-Q NOTCH FILTER


$V_{in} \geq 0.2\ V_{dc}$
MC34074
$V_O$
$V_{in}$
R
16 k
R
16 k
2C
0.02
8 k
R/2
C
0.01
C
0.01

$f_o = 1.0$ kHz

$$f_o = \frac{1}{2\pi RC}$$

FIGURE 38 — ACTIVE BANDPASS FILTER


C
0.047
R3
2.2 k
R1
1.1 k
$V_{in}$
MC34074
$V_O$
R2
5.6 k
C
0.047
$V_{CC}$
$0.4\ V_{CC}$
$f_o = 30$ kHz
Q = 10
$H_O = 1.0$

Given $f_O$ = Center Frequency
$A_O$ = Gain at Center Frequency
Choose Value $f_o$, Q, $A_o$, C
Then

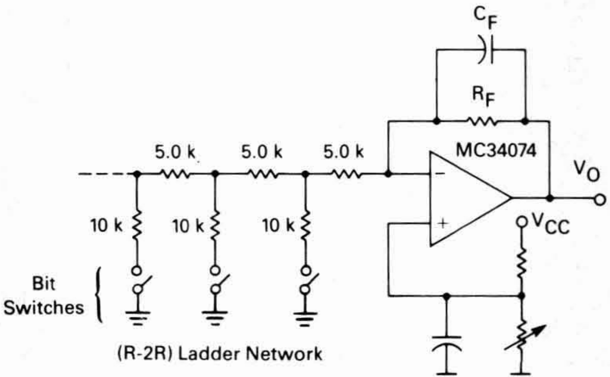
$$R3 = \frac{Q}{\pi f_o C} \quad R1 = \frac{R3}{2 H_o} \quad R2 = \frac{R1\ R3}{4Q^2\ R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{GBW} < 0.1$$

Where $f_o$ and GBW are expressed in Hz.
GBW = 4.5 MHz Typ.

FIGURE 39 — LOW VOLTAGE FAST D/A CONVERTER


$C_F$
$R_F$
5.0 k
5.0 k
5.0 k
MC34074
$V_O$
10 k
10 k
10 k
$V_{CC}$
Bit Switches
(R-2R) Ladder Network

Settling Time
1.0 μs (8 Bits, ½ LSB)

FIGURE 40 — HIGH SPEED LOW VOLTAGE COMPARATOR

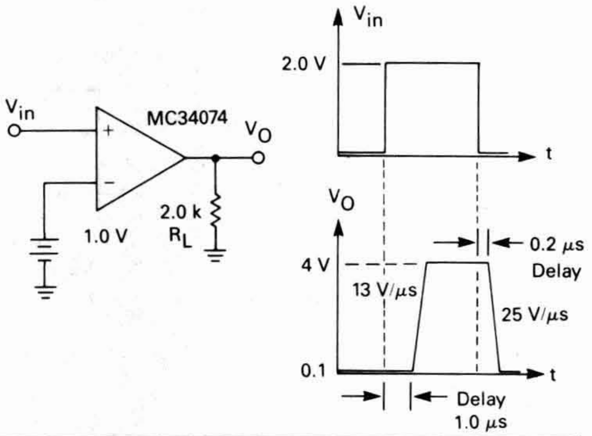

$V_{in}$
MC34074
$V_O$
2.0 k
$R_L$
1.0 V
$V_{in}$
2.0 V
t
$V_O$
0.2 μs Delay
4 V
13 V/μs
25 V/μs
0.1
t
Delay 1.0 μs

FIGURE 41 — LED DRIVER

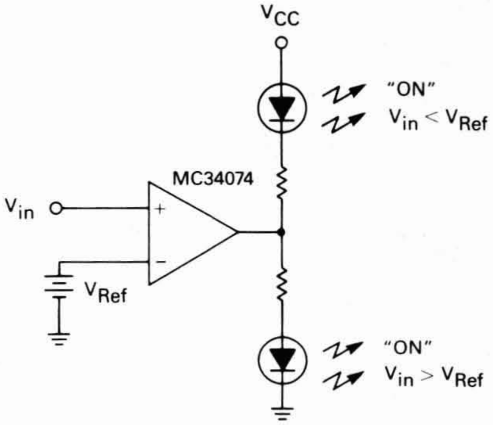
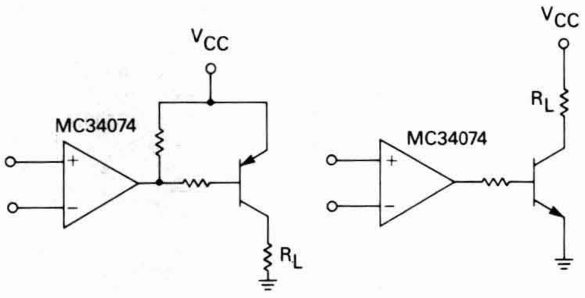

$V_{CC}$
"ON" $V_{in} < V_{Ref}$
MC34074
$V_{in}$
$V_{Ref}$
"ON" $V_{in} > V_{Ref}$

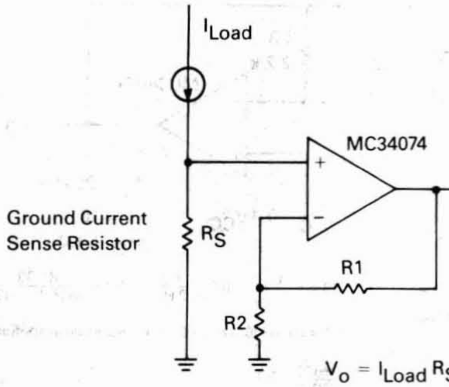
FIGURE 42 — TRANSISTOR DRIVER


$V_{CC}$
MC34074
$R_L$
$V_{CC}$
$R_L$
MC34074

(A) PNP

(B) NPN

FIGURE 43 — AC/DC GROUND CURRENT MONITOR



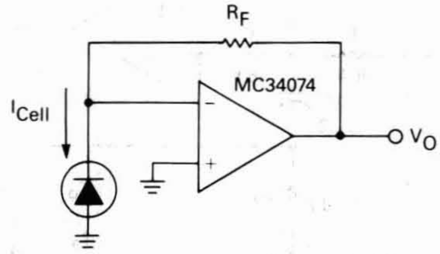
$I_{Load}$
MC34074
$V_O$
Ground Current
Sense Resistor
$R_S$
R1
R2

$$V_o = I_{Load} R_S \left(1 + \frac{R1}{R2}\right)$$

For $V_O > 0.1$ V

$$BW\ (-3.0\ dB) = GBW \left(\frac{R2}{R1 + R2}\right)$$

FIGURE 44 — PHOTOVOLTAIC CELL AMPLIFIER



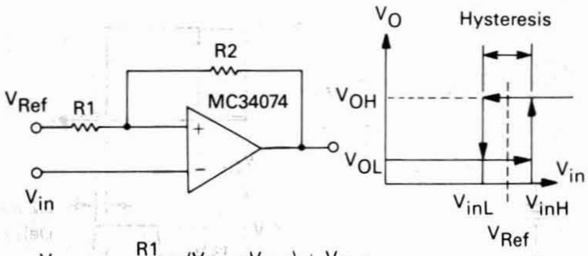
$R_F$
MC34074
$I_{Cell}$
$V_O$

$V_{Cell} = 0$ V

$V_O = I_{Cell} R_F$

$V_O > 0.1$ V

FIGURE 45 — LOW INPUT VOLTAGE COMPARATOR WITH HYSTERESIS



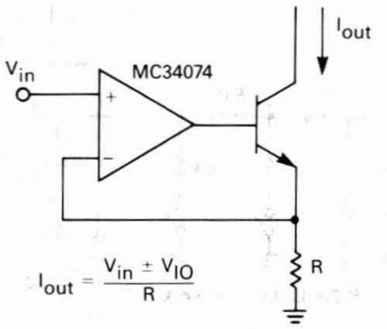
R2
$V_{Ref}$
R1
MC34074
$V_{in}$
$V_O$
Hysteresis
$V_{OH}$
$V_{OL}$
$V_{in}$
$V_{inL}$
$V_{inH}$
$V_{Ref}$

$$V_{inL} = \frac{R1}{R1 + R2}(V_{OL} - V_{Ref}) + V_{Ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}(V_{OH} - V_{Ref}) + V_{Ref}$$

$$V_H = \frac{R1}{R1 + R}(V_{OH} - V_{OL})$$

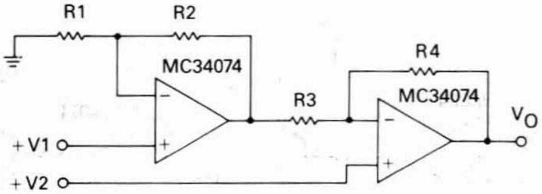
FIGURE 46 — HIGH COMPLIANCE VOLTAGE TO SINK CURRENT CONVERTER



$I_{out}$
$V_{in}$
MC34074
R

$$I_{out} = \frac{V_{in} \pm V_{IO}}{R}$$

FIGURE 47 — HIGH INPUT IMPEDANCE DIFFERENTIAL AMPLIFIER



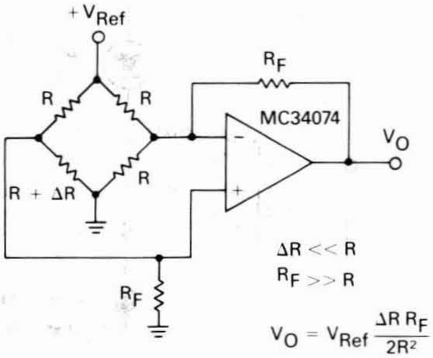
R1
R2
MC34074
R4
R3
MC34074
$V_O$
+V1
+V2

$$\frac{R2}{R1} = \frac{R4}{R3}\ \text{(Critical to CMRR)}$$

$$V_O = 1\left(+\frac{R4}{R3}\right)\left(V2 - V1\frac{R4}{R3}\right)$$

For $(V2 \geq V1)$, $V > 0$

FIGURE 48 — BRIDGE CURRENT AMPLIFIER



$+V_{Ref}$
R
R
R + ΔR
R
$R_F$
MC34074
$V_O$
$R_F$

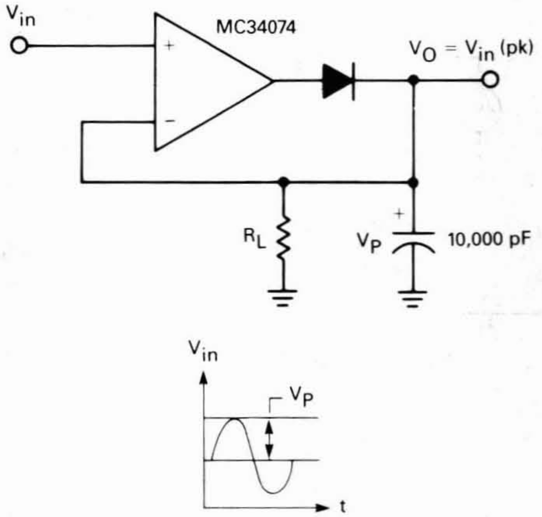
$\Delta R << R$

$R_F >> R$

$$V_O = V_{Ref}\frac{\Delta R\, R_F}{2R^2}$$

$(V_O \geq 0.1\ V)$

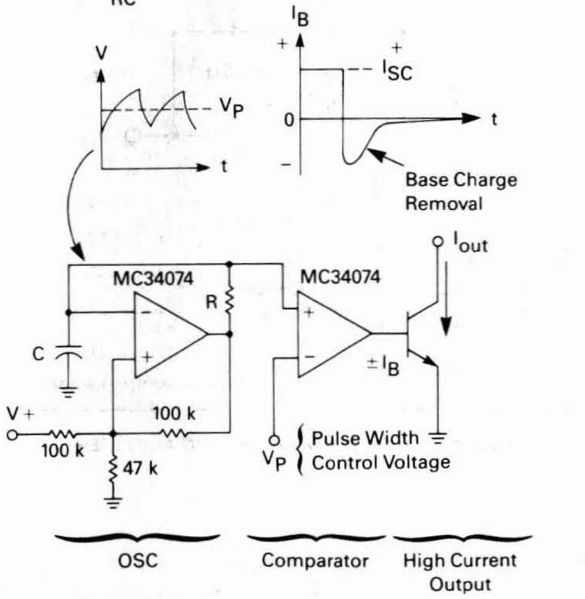
**FIGURE 49 — LOW VOLTAGE PEAK DETECTOR**



$V_{in}$
MC34074
+
−
$V_O = V_{in}$ (pk)
$R_L$
$V_P$
+
10,000 pF
$V_{in}$
$V_P$
t

**FIGURE 50 — HIGH FREQUENCY PULSE WIDTH MODULATION**

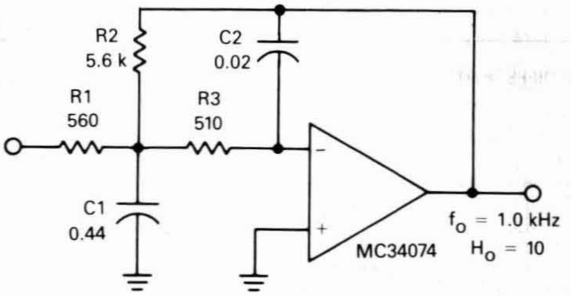
$f_{OSC} \cong \frac{0.85}{RC}$



V
$V_P$
t
$I_B$
+
0
−
+
$I_{SC}$
t
Base Charge Removal
$I_{out}$
MC34074
R
MC34074
C
−
+
+
−
$\pm I_B$
V+
100 k
100 k
47 k
$V_P$
Pulse Width Control Voltage
OSC
Comparator
High Current Output

**GENERAL ADDITIONAL APPLICATIONS INFORMATION $V_S = \pm 15$ VOLTS**

**FIGURE 51 — SECOND ORDER LOW-PASS ACTIVE FILTER**



R2
5.6 k
C2
0.02
R1
560
R3
510
C1
0.44
−
+
MC34074
$f_o = 1.0$ kHz
$H_o = 10$

Choose: $f_o$, $H_o$, C2

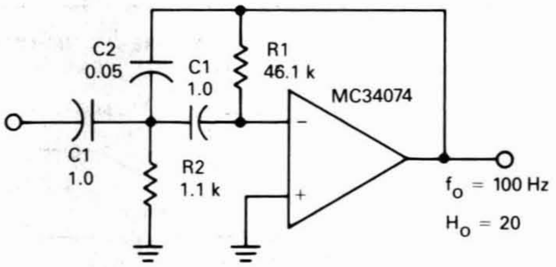
Then: $C1 = 2C2\,(H_o + 1)$

$$R2 = \frac{\sqrt{2}}{4\pi f_o C2}$$

$$R3 = \frac{R2}{H_o + 1}$$

$$R1 = \frac{R2}{H_o}$$

**FIGURE 52 — SECOND ORDER HIGH-PASS ACTIVE FILTER**



C2
0.05
C1
1.0
R1
46.1 k
MC34074
C1
1.0
R2
1.1 k
−
+
$f_o = 100$ Hz
$H_o = 20$

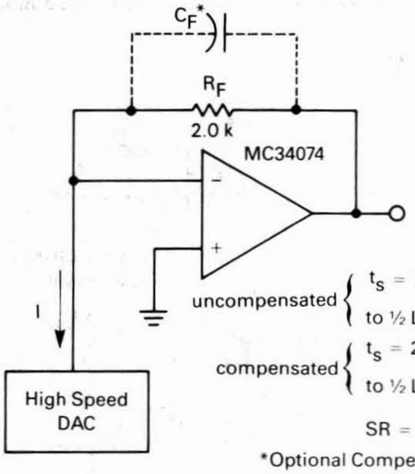
Choose: $f_o$, $H_o$, C1

$$\text{Then: } R1 = \frac{H_o + 0.5}{\pi f_o C1 \sqrt{2}}$$

$$R2 = \frac{\sqrt{2}}{2\pi f_o C1\,(1/H_o + 2)}$$

$$C2 = \frac{C1}{H_o}$$

FIGURE 53 — FAST SETTLING INVERTER


$C_F$*
$R_F$
2.0 k
MC34074
$V_O$
I
High Speed DAC

$V_O$ = 10 V Step

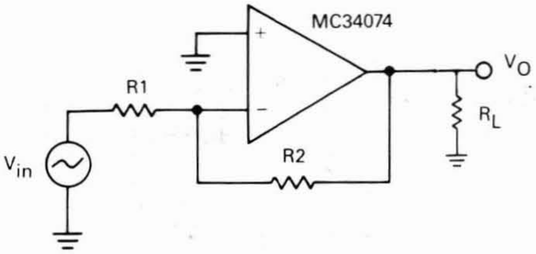
uncompensated { $t_s$ = 1.0 μs, to ½ LSB (8 Bits)

compensated { $t_s$ = 2.2 μs, to ½ LSB (12 Bits)

SR = 13 V/μs

*Optional Compensation

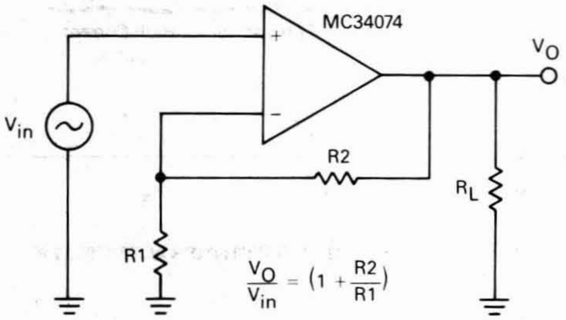
FIGURE 54 — BASIC INVERTING AMPLIFIER


MC34074
$V_O$
R1
$R_L$
R2
$V_{in}$

$$\frac{V_O}{V_{in}} = \frac{R2}{R1} \qquad BW\ (-3.0\ dB) = GBW \left[\frac{R1}{R1 + R2}\right]$$

SR = 13 V/μs

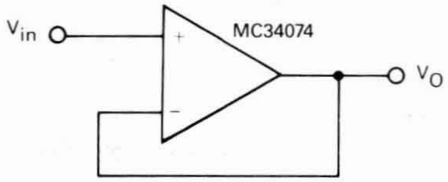
FIGURE 55 — BASIC NON-INVERTING AMPLIFIER


MC34074
$V_O$
$V_{in}$
R2
$R_L$
R1

$$\frac{V_O}{V_{in}} = \left(1 + \frac{R2}{R1}\right)$$

$$BW\ (-3.0\ dB) = GBW \left[\frac{R1}{R1 + R2}\right]$$

FIGURE 56 — UNITY GAIN BUFFER ($A_V$ = +1)

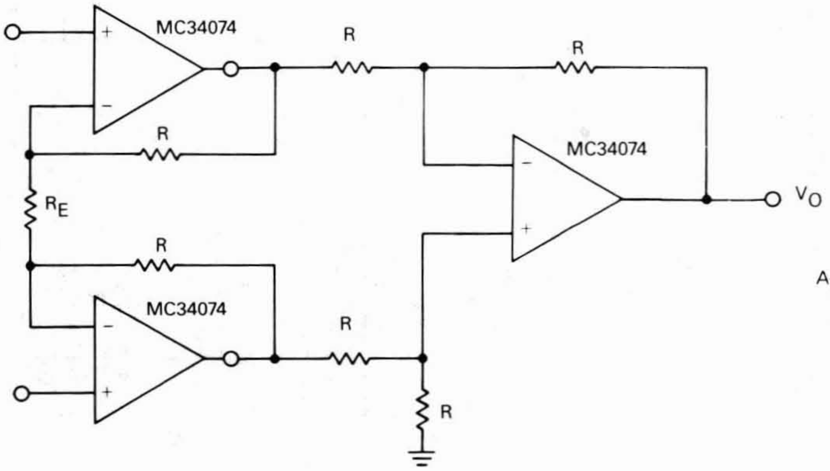

$V_{in}$
MC34074
$V_O$

$BW_P$ = 200 kHz

$V_O$ = 20 Vp-p

SR = 10 V/μs

FIGURE 57 — HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


MC34074
R
R
R
MC34074
$V_O$
$R_E$
R
MC34074
R
R

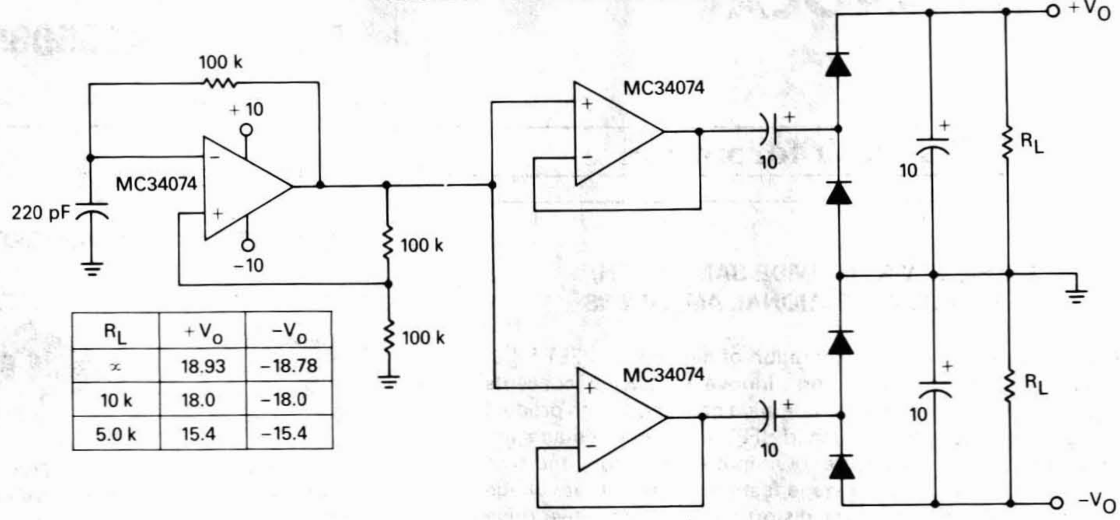
Example:
Let: R = $R_E$ = 12 k

Then: $A_V$ = 3

BW = 1.5 MHz

$$A_V = \left[1 + 2\frac{R}{R_E}\right]$$

FIGURE 58 — DUAL VOLTAGE DOUBLER


100 k
+10
MC34074
220 pF
−10
100 k
100 k
MC34074
MC34074
10
10
10
10
$R_L$
$R_L$
$+V_O$
$-V_O$

| $R_L$ | $+V_O$ | $-V_O$ |
|---|---|---|
| ∞ | 18.93 | −18.78 |
| 10 k | 18.0 | −18.0 |
| 5.0 k | 15.4 | −15.4 |

**MOTOROLA**

# MC34080/MC35080
# thru
# MC34085/MC35085

## HIGH PERFORMANCE JFET-INPUT OPERATIONAL AMPLIFIERS

## Advance Information

### HIGH SLEW RATE, WIDE BANDWIDTH, JFET INPUT OPERATIONAL AMPLIFIERS

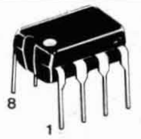
These devices are a new generation of high-speed JFET input monolithic operational amplifiers. Innovative design concepts along with JFET technology provide wide gain bandwidth product and high slew rate. Well matched JFET input devices and advanced trim techniques ensure low input offset errors and bias currents. The all NPN output stage features large output voltage swing, no deadband crossover distortion, high capacitive drive capability, excellent phase and gain margins, low open-loop output impedance, and symmetrical source/sink ac frequency response.

This series of devices are available in standard or prime performance (A suffix) grades, fully compensated or decompensated ($A_{VCL} \geq 2$) and are specified over commercial or Military temperature ranges. They are pin compatible with existing Industry standard operational amplifiers, and allow the designer to easily upgrade the performance of existing designs.

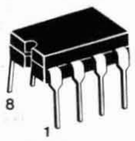
- Wide Gain Bandwidth: 8.0 MHz for Fully Compensated Devices
  16 MHz for Decompensated Devices
- High Slew Rate: 25 V/μs for Fully Compensated Devices
  50 V/μs for Decompensated Devices
- High Input Impedance: $10^{12}$ Ω
- Input Offset Voltage: 0.5 mV Maximum (Single Amplifier)
- Large Output Voltage Swing: −14.7 V to +14 V for $V_S = \pm 15$ V
- Low Open-Loop Output Impedance: 30 Ω @ 1.0 MHz
- Low THD Distortion: 0.01%
- Excellent Phase/Gain Margins: 55°/7.6 dB for Fully Compensated Devices

### ORDERING INFORMATION

| Op Amp Function | Fully Compensated | $A_{VCL} \geq 2$ Decompensated | Temperature Range | Package |
|---|---|---|---|---|
| Single | MC35081U,AU | MC35080U,AU | −55 to +125°C | Ceramic DIP |
| | MC34081D,AD | MC34080D,AD | 0 to +70°C | SO-8 Plastic DIP |
| | MC34081P,AP | MC34080P,AP | 0 to +70°C | Plastic DIP |
| Dual | MC34082P,AP | MC34083P,AP | 0 to +70°C | Plastic DIP |
| Quad | MC35084L,AL | MC35085L,AL | −55 to +125°C | Ceramic DIP |
| | MC34084P,AP | MC34085P,AP | 0 to +70°C | Plastic DIP |



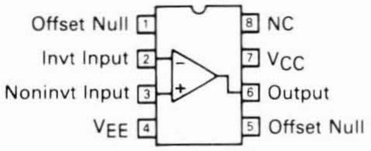
**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04



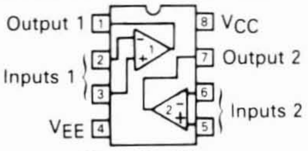
**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02

**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8

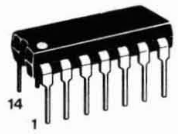
**PIN ASSIGNMENTS**



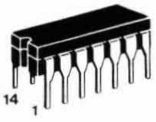
Single, Top View



Dual, Top View

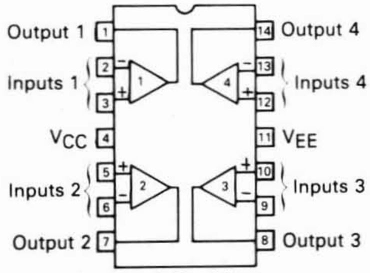


**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05



**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA
(TO-116)

**PIN ASSIGNMENTS**



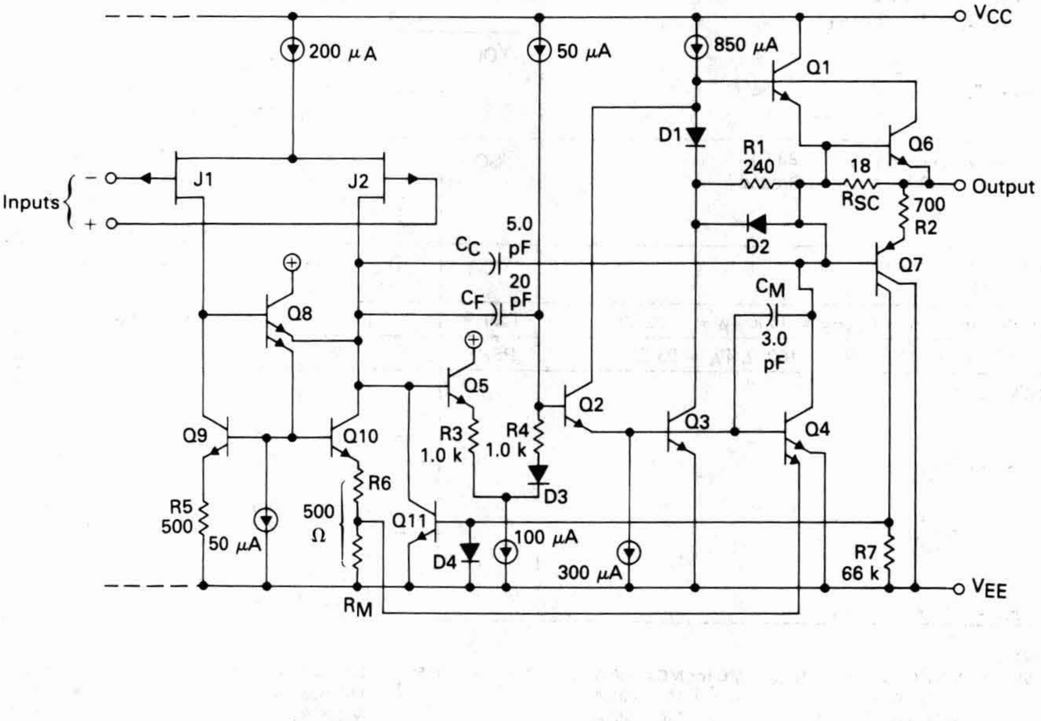
Quad, Top View

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage (from $V_{CC}$ to $V_{EE}$) | $V_S$ | +44 | Volts |
| Input Differential Voltage Range | $V_{IDR}$ | Note 1 | Volts |
| Input Voltage Range | $V_{IR}$ | Note 1 | Volts |
| Output Short-Circuit Duration (Note 2) | $t_S$ | Indefinite | Seconds |
| Operating Ambient Temperature Range<br>MC35XXX<br>MC34XXX | $T_A$ | <br>−55 to +125<br>0 to +70 | °C |
| Operating Junction Temperature<br>Ceramic Package<br>Plastic Package | $T_J$ | <br>+165<br>+125 | °C |
| Storage Temperature Range<br>Ceramic Package<br>Plastic Package | $T_{stg}$ | <br>−65 to +165<br>−55 to +125 | °C |

NOTES:
1. Either or both input voltages must not exceed the magnitude of $V_{CC}$ or $V_{EE}$.
2. Power dissipation must be considered to ensure maximum junction temperature ($T_J$) is not exceeded.

**EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)**


VCC
200 μA
50 μA
850 μA
Q1
Q6
D1
R1
240
18
RSC
Output
700
R2
Inputs
−
+
J1
J2
5.0
CC
pF
20
CF
pF
D2
Q7
CM
3.0
pF
Q8
Q5
Q2
Q3
Q4
Q9
Q10
R3
1.0 k
R4
1.0 k
D3
R6
R5
500
50 μA
500
Ω
Q11
D4
100 μA
300 μA
R7
66 k
VEE
RM

**DC ELECTRICAL CHARACTERISTICS** ($V_S$ = ±15 V, $T_A$ = $T_{low}$ to $T_{high}$ [Note 3], unless otherwise noted)

| Characteristic | Symbol | A Suffix |  |  | Non-Suffix |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage | $V_{IO}$ |  |  |  |  |  |  | mV |
| Single |  |  |  |  |  |  |  |  |
| $T_A$ = +25°C |  | — | 0.3 | 0.5 | — | 0.5 | 1.0 |  |
| $T_A$ = 0°C to +70°C (MC34080, MC34081) |  | — | — | 2.5 | — | — | 3.0 |  |
| $T_A$ = −55°C to +125°C (MC35080, MC35081) |  | — | — | 3.5 | — | — | 4.0 |  |
| Dual |  |  |  |  |  |  |  |  |
| $T_A$ = +25°C |  | — | 0.6 | 1.0 | — | 1.0 | 3.0 |  |
| $T_A$ = 0°C to +70°C (MC34082, MC34083) |  | — | — | 3.0 | — | — | 5.0 |  |
| $T_A$ = −55°C to +125°C (MC35082, MC35083) |  | — | — | 4.0 | — | — | 6.0 |  |
| Quad |  |  |  |  |  |  |  |  |
| $T_A$ = +25°C |  | — | 3.0 | 6.0 | — | 6.0 | 12 |  |
| $T_A$ = 0°C to +70°C (MC34084, MC34085) |  | — | — | 8.0 | — | — | 14 |  |
| $T_A$ = −55°C to +125°C (MC35084, MC35085) |  | — | — | 9.0 | — | — | 15 |  |
| Average Temperature Coefficient of Offset Voltage | $\Delta V_{IO}/\Delta T$ | — | 10 | — | — | 10 | — | µV/°C |
| Input Bias Current ($V_{CM}$ = 0 Note 4) | $I_{IB}$ |  |  |  |  |  |  | nA |
| $T_A$ = +25°C |  | — | 0.06 | 0.2 | — | 0.06 | 0.2 |  |
| $T_A$ = 0°C to +70°C |  | — | — | 4.0 | — | — | 4.0 |  |
| $T_A$ = −55°C to +125°C |  | — | — | 50 | — | — | 50 |  |
| Input Offset Current ($V_{CM}$ = 0 Note 4) | $I_{IO}$ |  |  |  |  |  |  | nA |
| $T_A$ = +25°C |  | — | 0.02 | 0.1 | — | 0.02 | 0.1 |  |
| $T_A$ = 0°C to +70°C |  | — | — | 2.0 | — | — | 20 |  |
| $T_A$ = −55°C to +125°C |  | — | — | 25 | — | — | 25 |  |
| Large Signal Voltage Gain ($V_O$ = ±10 V, $R_L$ = 2.0 k) | $A_{VOL}$ |  |  |  |  |  |  | V/mV |
| $T_A$ = +25°C |  | 50 | 80 | — | 25 | 80 | — |  |
| $T_A$ = $T_{low}$ to $T_{high}$ |  | 25 | — | — | 15 | — | — |  |
| Output Voltage Swing | $V_{OH}$ |  |  |  |  |  |  | V |
| $R_L$ = 2.0 k, $T_A$ = +25°C |  | 13.2 | 13.7 | — | 13.2 | 13.7 | — |  |
| $R_L$ = 10 k, $T_A$ = +25°C |  | 13.4 | 13.9 | — | 13.4 | 13.9 | — |  |
| $R_L$ = 10 k, $T_A$ = $T_{low}$ to $T_{high}$ |  | 13.4 | — | — | 13.4 | — | — |  |
|  | $V_{OL}$ |  |  |  |  |  |  |  |
| $R_L$ = 2.0 k, $T_A$ = +25°C |  | — | −14.1 | −13.5 | — | −14.1 | −13.5 |  |
| $R_L$ = 10 k, $T_A$ = +25°C |  | — | −14.7 | −14.1 | — | −14.7 | −14.1 |  |
| $R_L$ = 10 k, $T_A$ = $T_{low}$ to $T_{high}$ |  | — | — | −14.0 | — | — | −14.0 |  |
| Output Short-Circuit Current ($T_A$ = +25°C) | $I_{SC}$ |  |  |  |  |  |  | mA |
| Input Overdrive = 1.0 V, Output to Ground |  |  |  |  |  |  |  |  |
| Source |  | 20 | 31 | — | 20 | 31 | — |  |
| Sink |  | 20 | 28 | — | 20 | 28 | — |  |
| Input Common Mode Voltage Range<br>$T_A$ = +25°C | $V_{ICR}$ | ($V_{EE}$ + 4.0) to<br>($V_{CC}$ − 2.0) |  |  | ($V_{EE}$ + 4.0) to<br>($V_{CC}$ − 2.0) |  |  | V |
| Common Mode Rejection Ratio ($R_S$ ≤ 10 k, $T_A$ = +25°C) | CMRR | 75 | 90 | — | 70 | 90 | — | dB |
| Power Supply Rejection Ratio ($R_S$ = 100 Ω, $T_A$ = 25°C) | PSRR | 75 | 86 | — | 70 | 86 | — | dB |
| Power Supply Current | $I_D$ |  |  |  |  |  |  | mA |
| Single |  |  |  |  |  |  |  |  |
| $T_A$ = +25°C |  | — | 2.5 | 3.4 | — | 2.5 | 3.4 |  |
| $T_A$ = $T_{low}$ to $T_{high}$ |  | — | — | 4.2 | — | — | 4.2 |  |
| Dual |  |  |  |  |  |  |  |  |
| $T_A$ = +25°C |  | — | 4.9 | 6.0 | — | 4.9 | 6.0 |  |
| $T_A$ = $T_{low}$ to $T_{high}$ |  | — | — | 7.5 | — | — | 7.5 |  |
| Quad |  |  |  |  |  |  |  |  |
| $T_A$ = +25°C |  | — | 9.7 | 11 | — | 9.7 | 11 |  |
| $T_A$ = $T_{low}$ to $T_{high}$ |  | — | — | 13 | — | — | 13 |  |

NOTES: (CONTINUED)

3.

| $T_{low}$ = −55°C for | $T_{low}$ = 0°C for | $T_{high}$ = +125°C for | $T_{high}$ = +70°C for |
|---|---|---|---|
| MC35080,A | MC34080,A | MC35080,A | MC34080,A |
| MC35081,A | MC34081,A | MC35081,A | MC34081,A |
| MC35082,A | MC34082,A | MC35082,A | MC34082,A |
| MC35083,A | MC34083,A | MC35083,A | MC34083,A |
| MC35084,A | MC34084,A | MC35084,A | MC34084,A |
| MC35085,A | MC34085,A | MC35085,A | MC34085,A |

4. Limits at $T_A$ = +25° are guaranteed by high temperature ($T_{high}$) testing.

**AC ELECTRICAL CHARACTERISTICS** ($V_S$ = ±15 V, $T_A$ = +25°C unless otherwise noted)

| Characteristic | Symbol | A Suffix | | | Non-Suffix | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Slew Rate ($V_{in}$ = −10 V to +10 V, $R_L$ = 2.0 k, $C_L$ = 100 pF) | SR | | | | | | | V/µs |
| Compensated $A_V$ = +1.0 | | 20 | 25 | — | 20 | 25 | — | |
| $A_V$ = −1.0 | | — | 30 | — | — | 30 | — | |
| Decompensated $A_V$ = +2.0 | | 40 | 50 | — | 40 | 50 | — | |
| $A_V$ = −1.0 | | — | 50 | — | — | 50 | — | |
| Settling Time (10 V Step, $A_V$ = −1.0) | $t_s$ | | | | | | | µs |
| To 0.10% (± ½ LSB of 9-Bits) | | — | 0.72 | — | — | 0.72 | — | |
| To 0.01% (± ½ LSB of 12-Bits) | | — | 1.6 | — | — | 1.6 | — | |
| Gain Bandwidth Product (f = 200 kHz) | GBW | | | | | | | MHz |
| Compensated | | 6.0 | 8.0 | — | 6.0 | 8.0 | — | |
| Decompensated | | 12 | 16 | — | 12 | 16 | — | |
| Power Bandwidth ($R_L$ = 2.0 k, $V_O$ = 20 $V_{p-p}$, THD = 5.0%) | BWp | | | | | | | kHz |
| Compensated $A_V$ = +1.0 | | — | 400 | — | — | 400 | — | |
| Decompensated $A_V$ = −1.0 | | — | 800 | — | — | 800 | — | |
| Phase Margin (Compensated) | $\phi m$ | | | | | | | Degrees |
| $R_L$ = 2.0 k | | — | 55 | — | — | 55 | — | |
| $R_L$ = 2.0 k, $C_L$ = 100 pF | | — | 39 | — | — | 39 | — | |
| Gain Margin (Compensated) | $A_m$ | | | | | | | dB |
| $R_L$ = 2.0 k | | — | 7.6 | — | — | 7.6 | — | |
| $R_L$ = 2.0 k, $C_L$ = 100 pF | | — | 4.5 | — | — | 4.5 | — | |
| Equivalent Input Noise Voltage $R_S$ = 100 Ω, f = 1.0 kHz | $e_n$ | — | 30 | — | — | 30 | — | nV/ $\sqrt{Hz}$ |
| Equivalent Input Noise Current (f = 1.0 kHz) | $I_n$ | — | 0.01 | — | — | 0.01 | — | pA/ $\sqrt{Hz}$ |
| Input Capacitance | $C_i$ | — | 5.0 | — | — | 5.0 | — | pF |
| Input Resistance | $r_i$ | — | $10^{12}$ | — | — | $10^{12}$ | — | Ω |
| Total Harmonic Distortion $A_V$ = +10, $R_L$ = 2.0 k, 2.0 ≤ $V_O$ ≤ 20 $V_{p-p}$, f = 10 kHz | THD | — | 0.05 | — | — | 0.05 | — | % |
| Channel Separation (f = 10 kHz) | — | — | 120 | — | — | 120 | — | dB |
| Open-Loop Output Impedance (f = 1.0 MHz) | $z_o$ | — | 35 | — | — | 35 | — | Ω |

## TYPICAL PERFORMANCE CURVES

**FIGURE 1 — INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE**

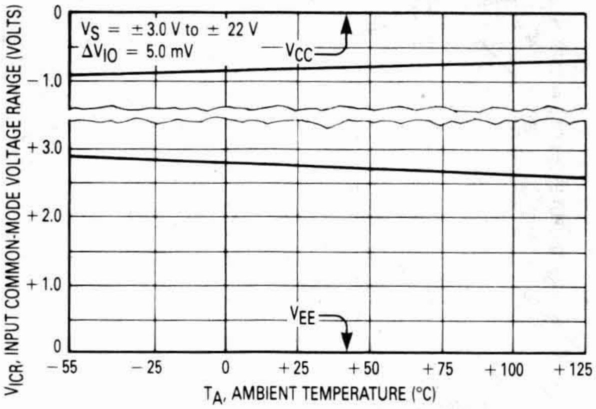


**FIGURE 2 — INPUT BIAS CURRENT versus TEMPERATURE**

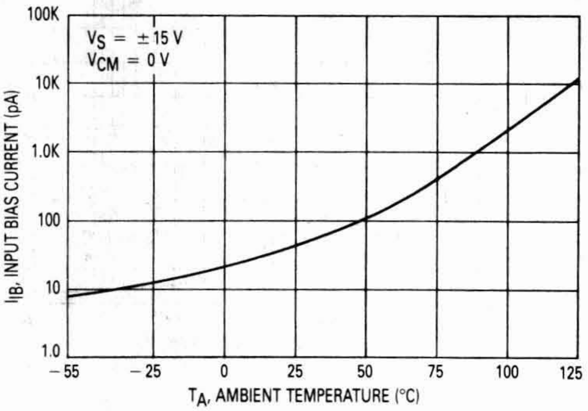


**FIGURE 3 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE**

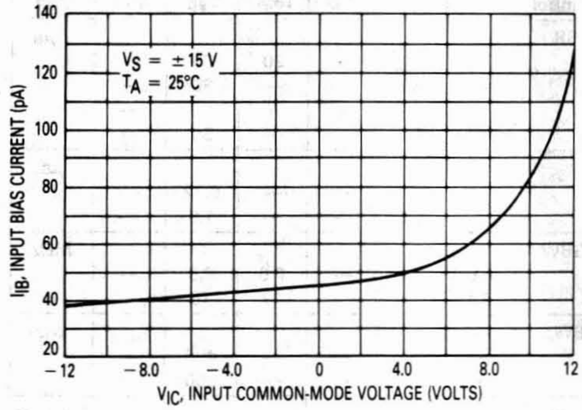


**FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE**

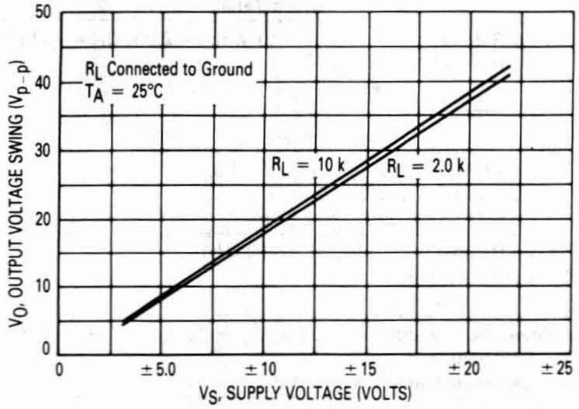


**FIGURE 5 — OUTPUT SATURATION versus LOAD CURRENT**

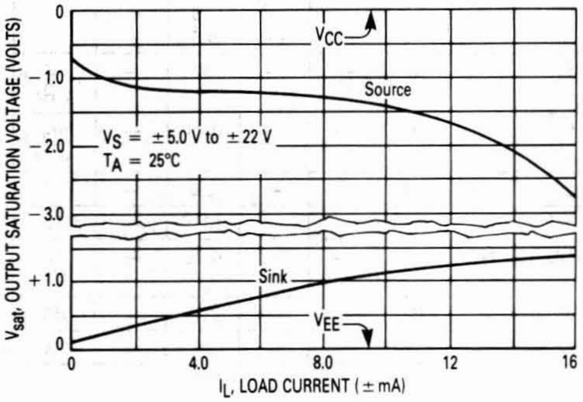


**FIGURE 6 — OUTPUT SATURATION versus LOAD RESISTANCE TO GROUND**

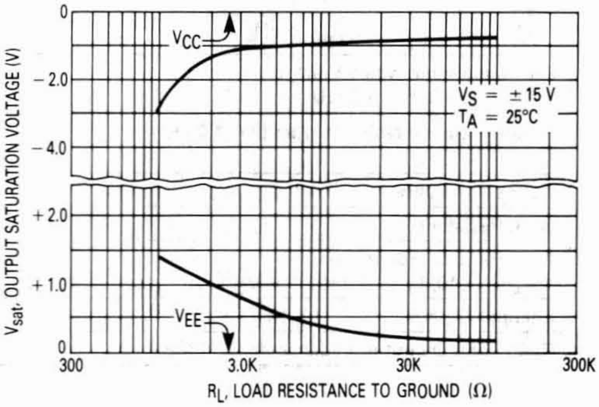


**FIGURE 7 — OUTPUT SATURATION versus LOAD RESISTANCE TO $V_{CC}$**

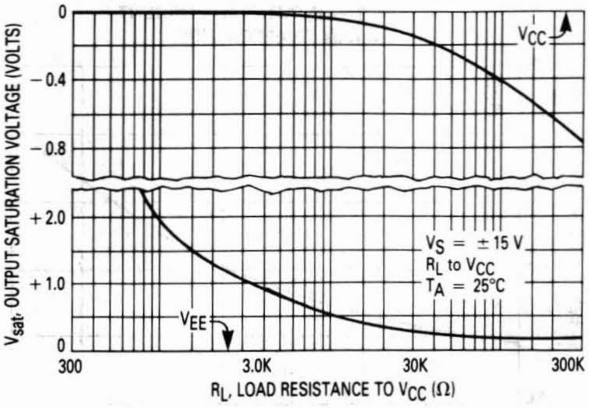


**FIGURE 8 — OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE**

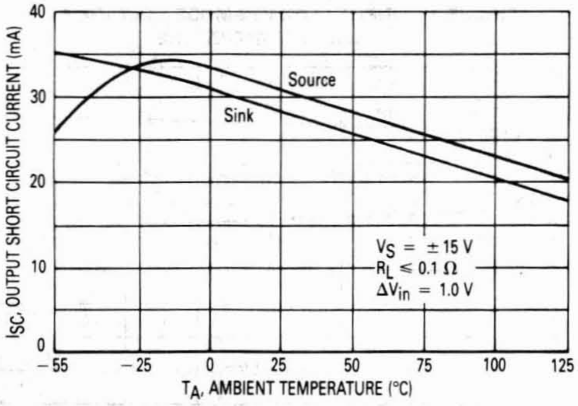


FIGURE 9 — OUTPUT IMPEDANCE versus FREQUENCY

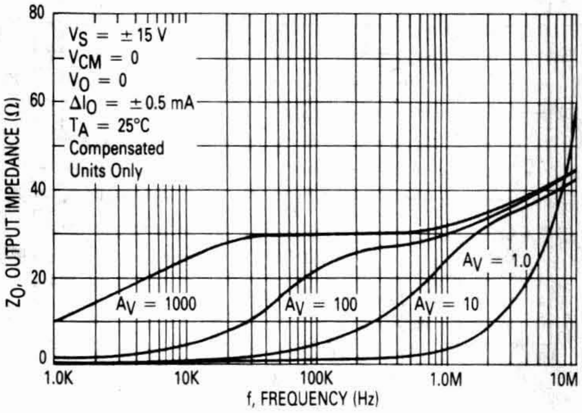


FIGURE 10 — OUTPUT IMPEDANCE versus FREQUENCY

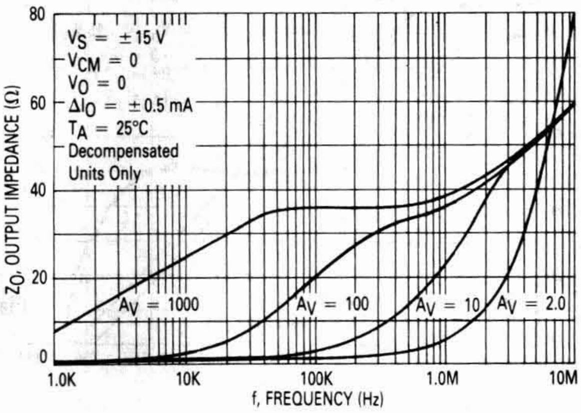


FIGURE 11 — OUTPUT VOLTAGE SWING versus FREQUENCY

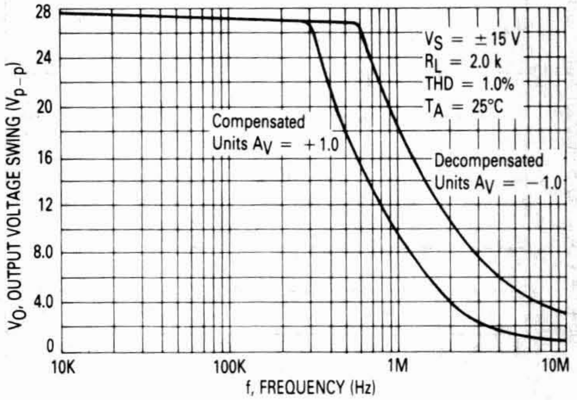


FIGURE 12 — OUTPUT DISTORTION versus FREQUENCY

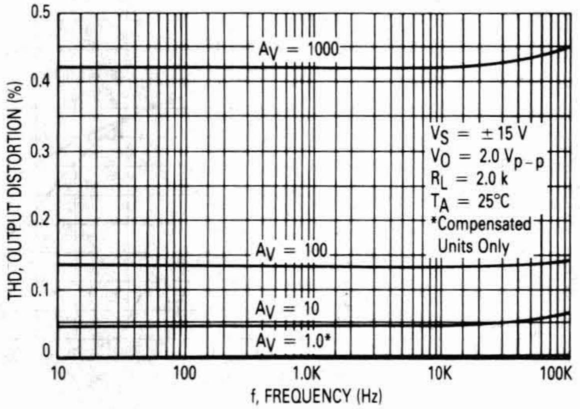


FIGURE 13 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

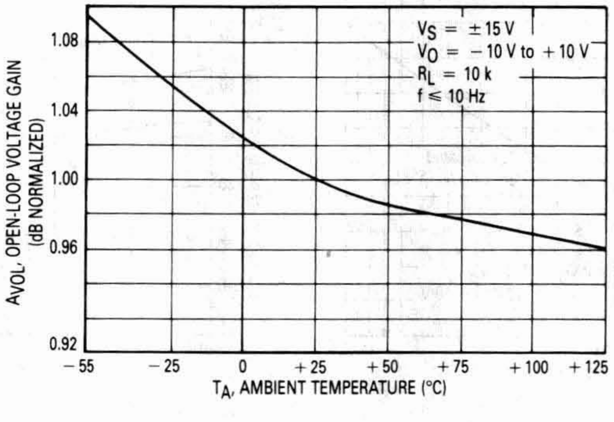


**FIGURE 14 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY**

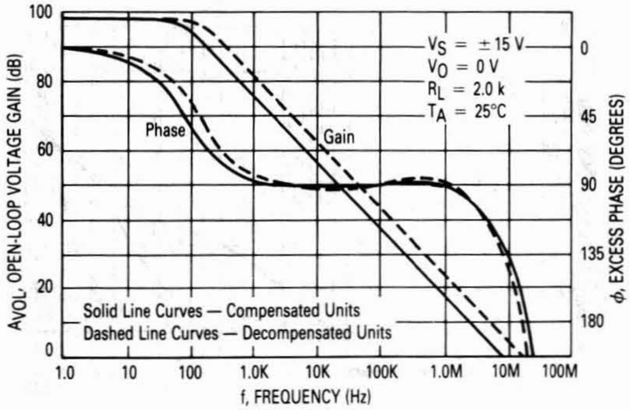


**FIGURE 15 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY**

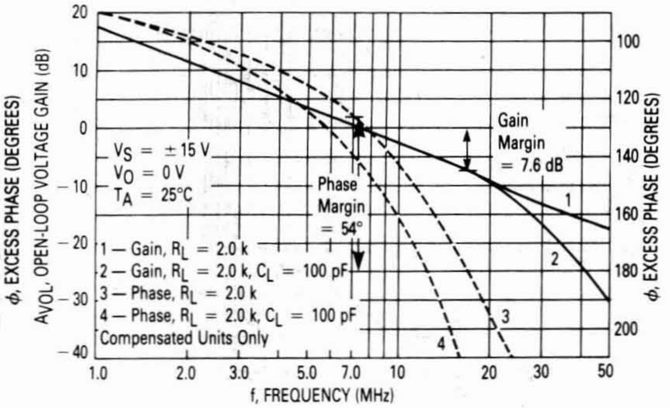


**FIGURE 16 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY**

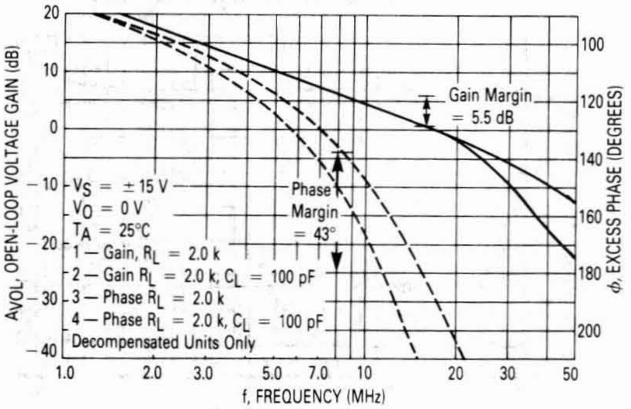


**FIGURE 17 — NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE**

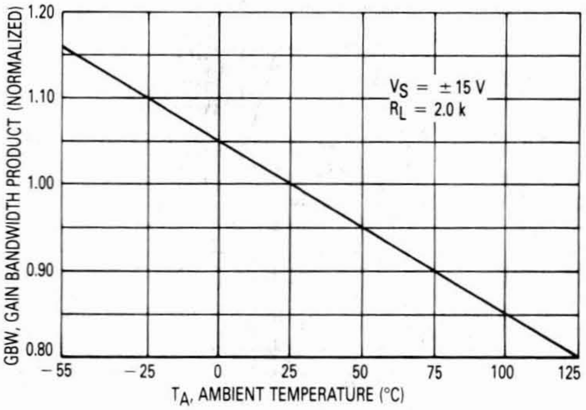


**FIGURE 18 — PERCENT OVERSHOOT versus LOAD CAPACITANCE**

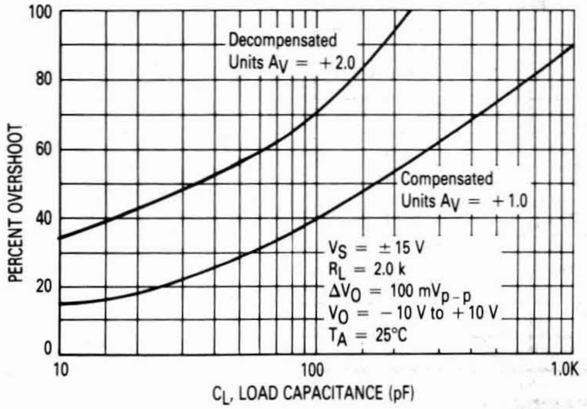


**FIGURE 19 — PHASE MARGIN versus LOAD CAPACITANCE**

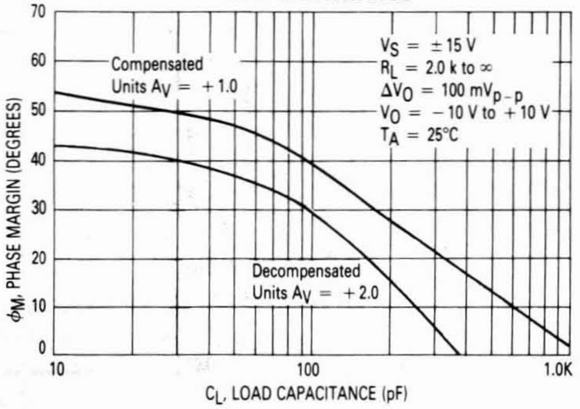


FIGURE 20 — GAIN MARGIN versus LOAD CAPACITANCE

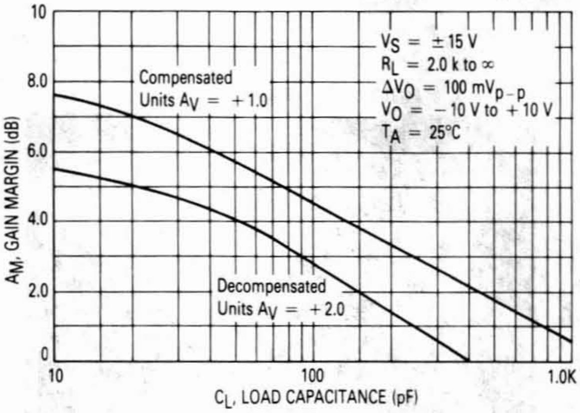


FIGURE 21 — PHASE-MARGIN versus TEMPERATURE

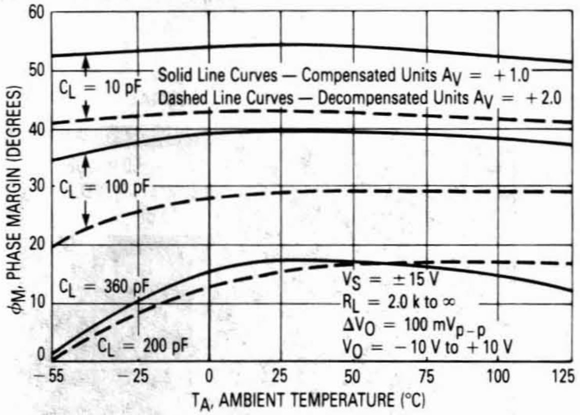


FIGURE 22 — GAIN MARGIN versus TEMPERATURE

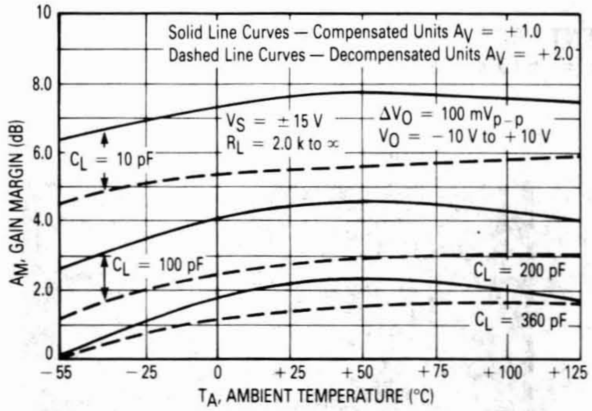
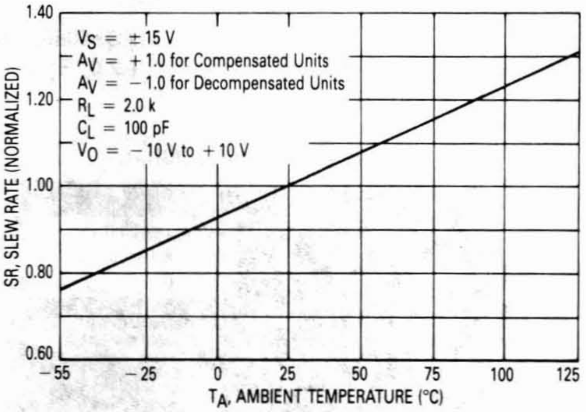


FIGURE 23 — NORMALIZED SLEW RATE versus TEMPERATURE



## MC34084 TRANSIENT RESPONSE
**$A_V = +1.0, R_L = 2.0\text{ k}, V_S = \pm 15\text{ V}, T_A = 25°\text{C}$**

FIGURE 24 — SMALL-SIGNAL

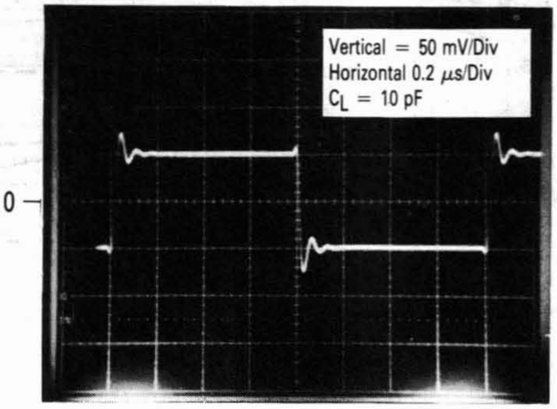
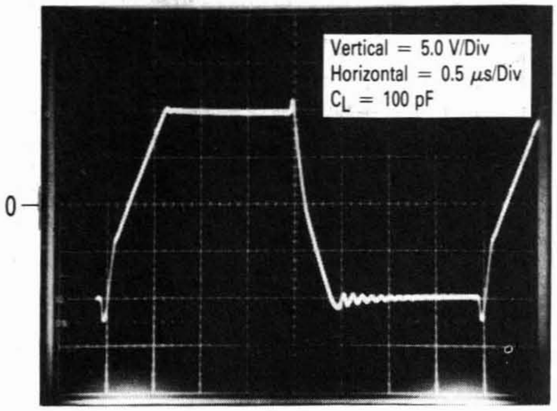


FIGURE 25 — LARGE-SIGNAL



## MC34085 TRANSIENT RESPONSE
**$A_V = +2.0, R_L$ 2.0 k, $V_S = \pm 15\text{ V}, T_A = 25°\text{C}$**

FIGURE 26 — SMALL-SIGNAL

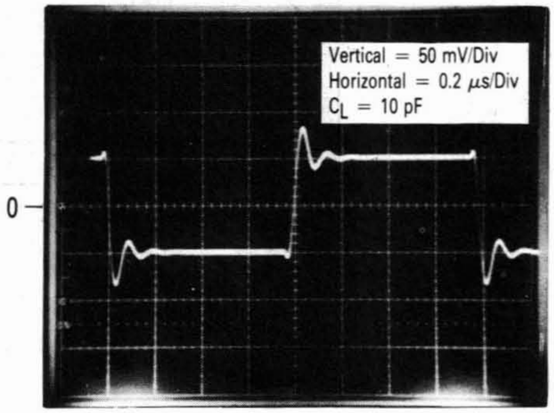


FIGURE 27 — LARGE-SIGNAL

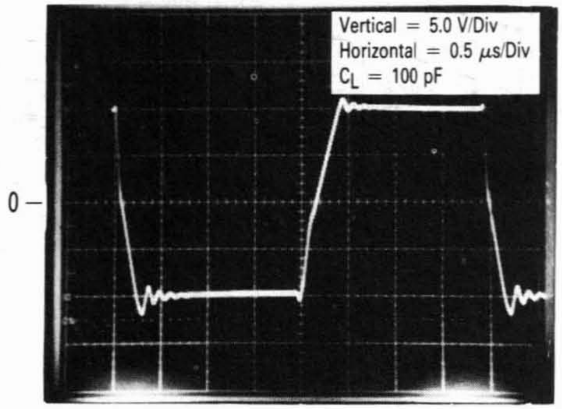


FIGURE 28 — COMMON-MODE REJECTION RATIO versus FREQUENCY

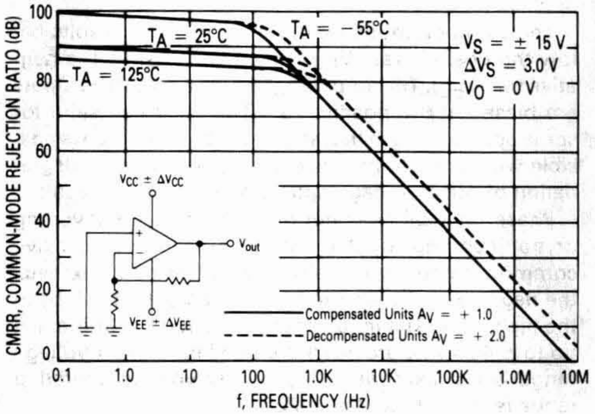


FIGURE 29 — POWER SUPPLY REJECTION RATIO versus FREQUENCY

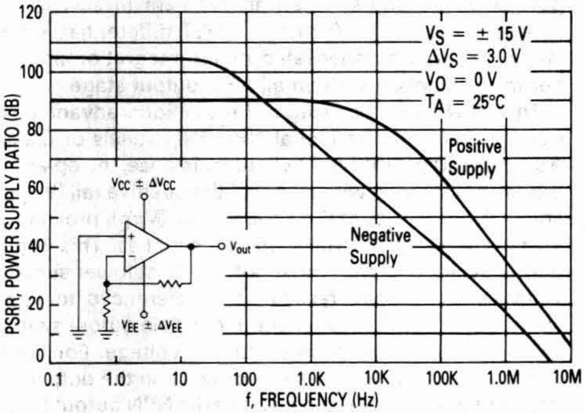


FIGURE 30 — POWER SUPPLY REJECTION RATIO versus TEMPERATURE

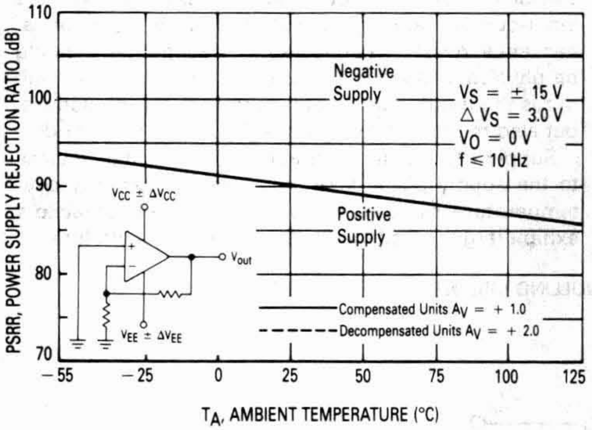


FIGURE 31 — NORMALIZED SUPPLY CURRENT versus SUPPLY VOLTAGE

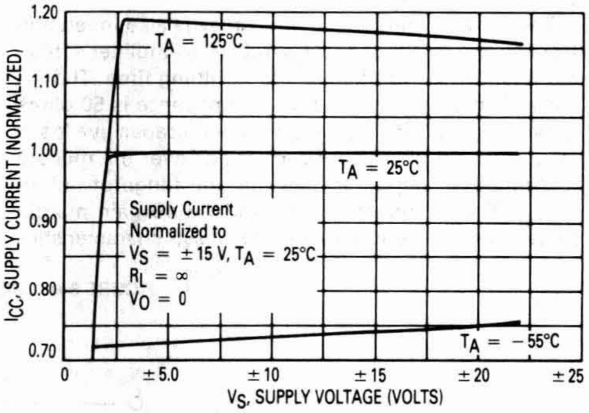


FIGURE 32 — CHANNEL SEPARATION versus FREQUENCY

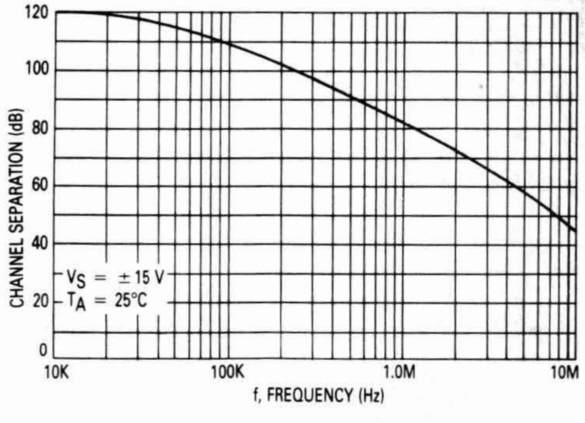
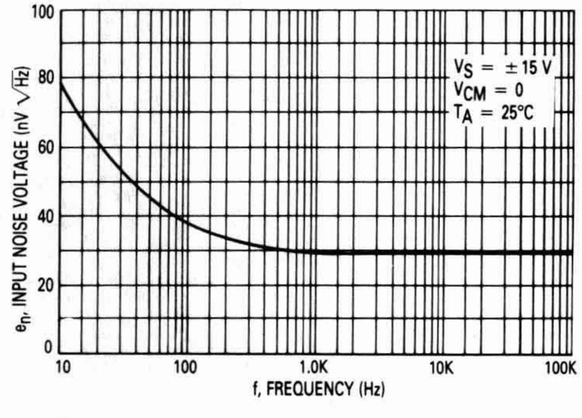


FIGURE 33 — SPECTRAL NOISE DENSITY



## APPLICATIONS INFORMATION

The bandwidth and slew rate of the MC34080 series is nearly double that of currently available general purpose JFET op-amps. This improvement in ac performance is due to the P-channel JFET differential input stage driving a compensated miller integration amplifier in conjunction with an all NPN output stage.

The all NPN output stage offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. With a 10 k load resistance, the op-amp can typically swing within l.0 V of the positive rail ($V_{CC}$), and within 0.3 volts of the negative rail ($V_{EE}$), providing a 28.7 Vp − p swing from ± 15 volt supplies. This large output swing becomes most noticeable at lower supply voltages. If the load resistance is referenced to $V_{CC}$ instead of ground, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to $V_{CC}$ during the positive swing and the NPN output transistor will pull the output very near $V_{EE}$ during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull-up capability.

The all NPN transistor output stage is also inherently fast, contributing to the operational amplifier's high gain-bandwidth product and fast settling time. The associated high frequency output impedance is 50 ohms (typical) at 8.0 MHz. This allows driving capacitive loads from 0 to 300 pF without oscillations over the military temperature range, and over the full range of output swing. The 55° phase margin and 7.6 dB gain margin as well as the general gain and phase characteristics are virtually independent of the sink/source output swing conditions. The high frequency characteristics of the MC34080 series is especially useful for active filter applications.

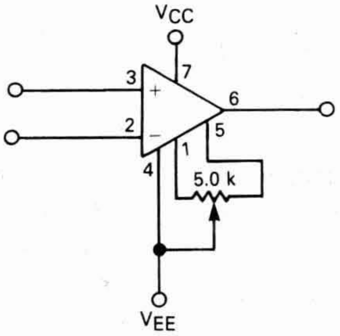
The common mode input range is from 2.0 volts below the positive rail ($V_{CC}$) to 4.0 volts above the negative rail ($V_{EE}$). The amplifier remains active if the inputs are biased at the positive rail. This may be useful for some applications in that single supply operation is possible with a single negative supply. However, a degradation of offset voltage and voltage gain may result.

Phase reversal does not occur if either the inverting or noninverting input (or both) exceeds the positive common mode limit. If either input (or both) exceeds the negative common mode limit, the output will be in the high state. The input stage also allows a differential up to ± 44 volts, provided the maximum input voltage range is not exceeded. The supply voltage operating range is from ± 5.0 V to ± 22 V.

For optimum frequency performance and stability careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to reduce the input capacitance, resistors connected to the input pins should be physically close to these pins. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pickup" at this node.

Supply decoupling with adequate capacitance close to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit large impedance changes over temperature.

FIGURE 34 — OFFSET NULLING CIRCUIT



**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| NE592D | 0 to 70°C | SO-14 |
| NE592N | 0 to 70°C | Plastic DIP |
| NE592H | 0 to 70°C | Metal Can |
| NE592F | 0 to 70°C | Ceramic DIP |
| SE592H | −55 to +125°C | Metal Can |
| SE592F | −55 to +125°C | Ceramic DIP |

# NE592
# SE592

## VIDEO AMPLIFIER

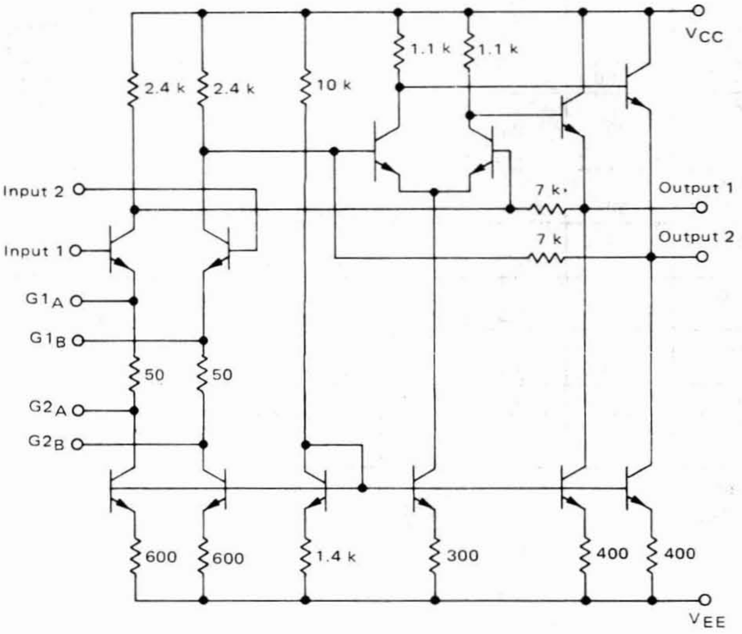
SILICON MONOLITHIC
INTEGRATED CIRCUIT

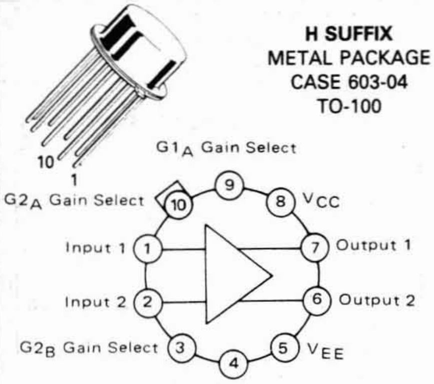
## DIFFERENTIAL TWO-STAGE VIDEO AMPLIFIER

The SE/NE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. The 592 is a pin-for-pin replacement for the MC1733.

- 90 MHz Bandwidth
- Adjustable Gains From 0 to 400
- Adjustable Pass Band
- No Frequency Compensation Required

CIRCUIT SCHEMATIC

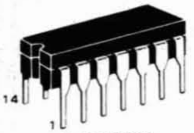

2.4 k
2.4 k
10 k
1.1 k
1.1 k
$V_{CC}$
7 k
Output 1
7 k
Output 2
Input 2
Input 1
$G1_A$
$G1_B$
50
50
$G2_A$
$G2_B$
600
600
1.4 k
300
400
400
$V_{EE}$


10
1
$G1_A$ Gain Select
$G2_A$ Gain Select
10
9
8
$V_{CC}$
Input 1
1
7
Output 1
Input 2
2
6
Output 2
$G2_B$ Gain Select
3
4
5
$V_{EE}$
$G1_B$ Gain Select

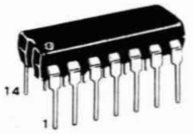
**H SUFFIX**
METAL PACKAGE
CASE 603-04
TO-100

(Top View)

Pin 5 connected to case

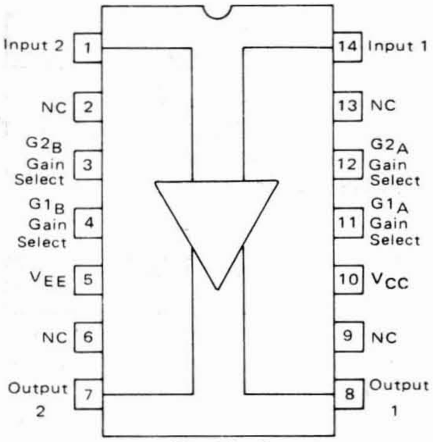


**F SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA



**N SUFFIX**
PLASTIC PACKAGE
CASE 646-05

**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14


Input 2
1
NC
2
$G2_B$ Gain Select
3
$G1_B$ Gain Select
4
$V_{EE}$
5
NC
6
Output 2
7
14
Input 1
13
NC
12
$G2_A$ Gain Select
11
$G1_A$ Gain Select
10
$V_{CC}$
9
NC
8
Output 1

(Top View)

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +8.0<br>−8.0 | Volts |
| Differential Input Voltages | $V_{ID}$ | ±5.0 | Volts |
| Common-Mode Input Voltage | $V_{IC}$ | ±6.0 | Volts |
| Output Current | $I_o$ | 10 | mA |
| Operating Ambient Temperature Range<br>SE592<br>NE592 | $T_A$ | <br>−55 to +125<br>0 to +70 | °C |
| Operating Junction Temperature Range<br>Metal and Ceramic Packages<br>Plastic Package | $T_J$ | <br>175<br>150 | °C |
| Storage Temperature Range<br>Metal and Ceramic Packagee<br>Plastic Package | $T_{stg}$ | <br>−65 to +150<br>−55 to +125 | °C |

**ELECTRICAL CHARACTERISTICS $T_A$ = 25°C unless otherwise noted.** ($V_{CC}$ = +6.0 V, $V_{EE}$ = −6.0 V, $V_{CM}$ = 0)

| Characteristic | Symbol | SE592 | | | NE592 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential Voltage Gain – Figure 3<br>($R_L$ = 2 k$\Omega$, $e_{out}$ = 3 Vp-p)<br>(Gain 1, Note 1)<br>(Gain 2, Note 2) | $A_{vd}$ | <br><br>300<br>90 | <br><br>400<br>100 | <br><br>500<br>110 | <br><br>250<br>80 | <br><br>400<br>100 | <br><br>600<br>120 | V/V |
| Bandwidth – Figure 3<br>(Gain 1, Note 1)<br>(Gain 1, Note 2) | BW | <br>–<br>– | <br>40<br>90 | <br>–<br>– | <br>–<br>– | <br>40<br>90 | <br>–<br>– | MHz |
| Rise Time – Figure 3<br>(Gain 1, $e_{out}$ = 1 Vp-p, Note 1)<br>(Gain 2, $e_{out}$ = 1 Vp-p, Note 2) | <br>$t_{TLH}$<br>$t_{THL}$ | <br>–<br>– | <br>10.5<br>4.5 | <br>–<br>10 | <br>–<br>– | <br>10.5<br>4.5 | <br>–<br>12 | ns |
| Propagation Delay – Figure 3<br>(Gain 1, $e_{out}$ = 1 Vp-p, Note 1)<br>(Gain 2, $e_{out}$ = 1 Vp-p, Note 2) | <br>$t_{PLH}$<br>$t_{PHL}$ | <br>–<br>– | <br>7.5<br>6.0 | <br>–<br>10 | <br>–<br>– | <br>7.5<br>6.0 | <br>–<br>10 | ns |
| Input Resistance<br>(Gain 1, Note 1)<br>(Gain 2, Note 2) | $R_{in}$ | <br>–<br>20 | <br>4.0<br>30 | <br>–<br>– | <br>–<br>10 | <br>4.0<br>30 | <br>–<br>– | k$\Omega$ |
| Input Capacitance<br>(Gain 2, Note 2) | $C_{in}$ | – | 2.0 | – | – | 2.0 | – | pF |
| Input Offset Current (Gain 3, Note 3) – Fig. 2 | $I_{IO}$ | – | 0.4 | 3.0 | – | 0.4 | 5.0 | $\mu$A |
| Input Bias Current (Gain 3, Note 3) – Fig. 2 | $I_{IB}$ | – | 9.0 | 20 | – | 9.0 | 30 | $\mu$A |
| Input Noise Voltage (Gain 1 and Gain 2)<br>(BW = 1 kHz to 10 MHz) – Figure 1 | $V_n$ | – | 12 | – | – | 12 | – | $\mu$V(rms) |
| Input Voltage Range (Gain 2, Note 2) – Fig. 3 | $V_{in}$ | ±1.0 | – | – | ±1.0 | – | – | V |
| Common-Mode Rejection Ratio – Figure 3<br>(Gain 2, $V_{CM}$ = ±1 V, f $\leq$ 100 kHz)<br>(Gain 2, $V_{CM}$ = ±1 V, f = 5 MHz) | CMRR | <br>60<br>– | <br>86<br>60 | <br>–<br>– | <br>60<br>– | <br>86<br>60 | <br>–<br>– | dB |
| Supply Voltage Rejection Ratio – Figure 2<br>(Gain 2, $\Delta V_s$ = ±0.5 V) | PSRR | 50 | 70 | – | 50 | 70 | – | dB |
| Output Offset Voltage – Figure 2<br>(Gain 3, $R_L$ = ∞, Note 3) | $V_{OO}$ | – | 0.35 | 0.75 | – | 0.35 | 0.75 | V |
| Output Common-Mode Voltage – Figure 2<br>($R_L$ = ∞, Gain 3, Note 3) | $V_{CMO}$ | 2.4 | 2.9 | 3.4 | 2.4 | 2.9 | 3.4 | V |
| Output Voltage Swing – Figure 3<br>($R_L$ = 2k, Gain 2, Note 2) | $V_O$ | 3.0 | 4.0 | – | 3.0 | 4.0 | – | Vp-p |
| Output Resistance | $r_o$ | – | 20 | – | – | 20 | – | Ω |
| Power Supply Current – Figure 2<br>($R_L$ = ∞, Gain 2, Note 2) | $I_D$ | – | 18 | 24 | – | 18 | 24 | mA |

Note 1. Gain select pins $G1_A$ and $G1_B$ connected together.

Note 2. Gain select pins $G2_A$ and $G2_B$ connected together.

Note 3. All gain select pins open.

**ELECTRICAL CHARACTERISTICS $T_A = T_{high}$ to $T_{low}$ unless otherwise noted.*** ($V_{CC}$ = +6.0 Vdc, $V_{EE}$ = -6.0 Vdc, $V_{CM}$ = 0)

| Characteristic | Symbol | SE592 | | | NE592 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential Voltage Gain – Figure 3 ($R_L$ = 2 kΩ, $e_{out}$ = 3 Vp-p) | $A_{vd}$ | | | | | | | V/V |
| (Gain 1, Note 1) | | 200 | – | 600 | 250 | – | 600 | |
| (Gain 2, Note 2) | | 80 | – | 120 | 80 | – | 120 | |
| Input Resistance (Gain 2) | $R_{in}$ | 8.0 | – | – | 8.0 | – | – | kΩ |
| Input Offset Current (Gain 3) – Figure 2 | $\|I_{IO}\|$ | – | – | 5.0 | – | – | 6.0 | μA |
| Input Bias Current (Gain 3) – Figure 2 | $I_{IB}$ | – | – | 40 | – | – | 40 | μA |
| Input Voltage Range (Gain 2) – Figure 3 | $V_{in}$ | ±1.0 | – | – | ±1.0 | – | – | V |
| Common-Mode Rejection Ratio – Figure 3 (Gain 2, $V_{CM}$ = ±1 V, f ≤ 100 kHz) | CMRR | 50 | – | – | 50 | – | – | dB |
| Supply Voltage Rejection Ratio – Figure 2 (Gain 2, Δ $V_s$ = ±0.5 V) | PSRR | 50 | – | – | 50 | – | – | dB |
| Output Offset Voltage (Gain 3) – Figure 2 | $V_{OO}$ | – | – | 1.2 | – | – | 1.5 | V |
| Output Voltage Swing (Gain 2) – Figure 3 | $V_O$ | 2.5 | – | – | 2.5 | – | – | Vp-p |
| Power Supply Current (Gain 2) – Figure 2 | $I_D$ | – | – | 27 | – | – | 27 | mA |

*$T_{low}$ = 0°C for NE592, -55°C for SE592
$T_{high}$ = +70°C for NE592, +125°C for SE592

## GENERAL TEST CIRCUITS

FIGURE 1

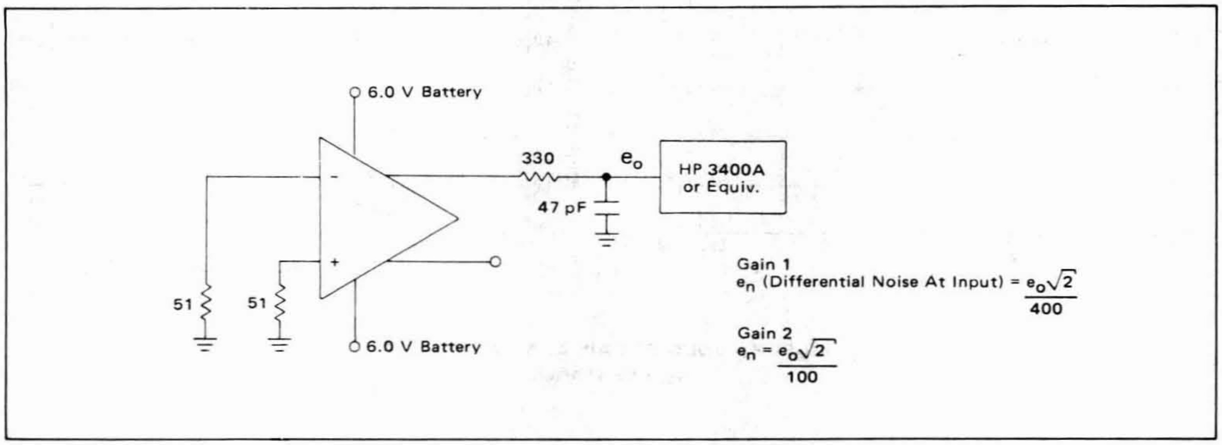

6.0 V Battery
330
$e_o$
HP 3400A or Equiv.
47 pF
51
51
6.0 V Battery
Gain 1
$e_n$ (Differential Noise At Input) = $\frac{e_o\sqrt{2}}{400}$
Gain 2
$e_n = \frac{e_o\sqrt{2}}{100}$

FIGURE 2

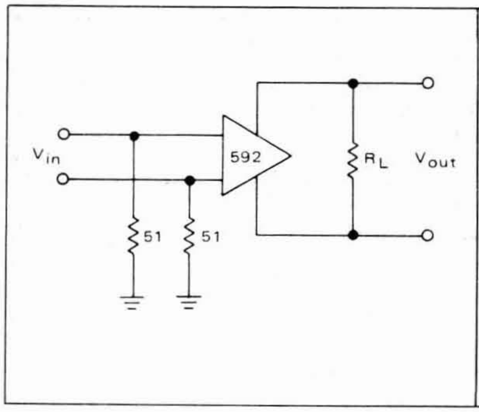

$V_{in}$
592
$R_L$
$V_{out}$
51
51

FIGURE 3

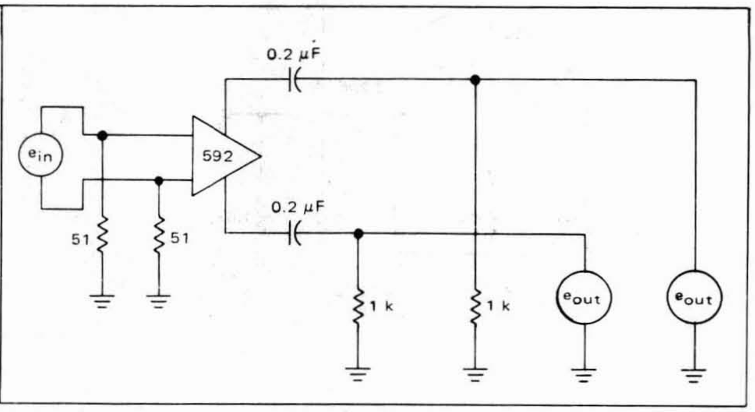

0.2 μF
$e_{in}$
592
0.2 μF
51
51
1 k
1 k
$e_{out}$
$e_{out}$

FIGURE 4 – GAIN 1 versus FREQUENCY

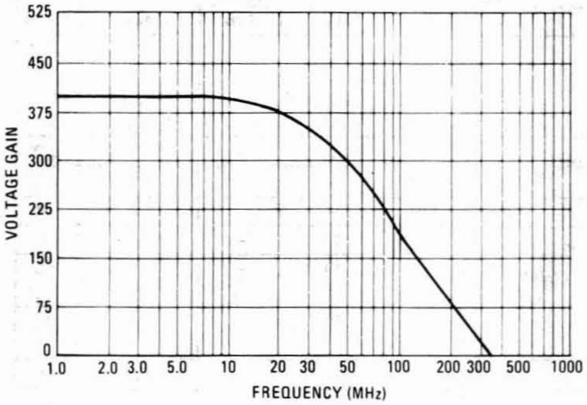


FIGURE 5 – GAIN 2 versus FREQUENCY

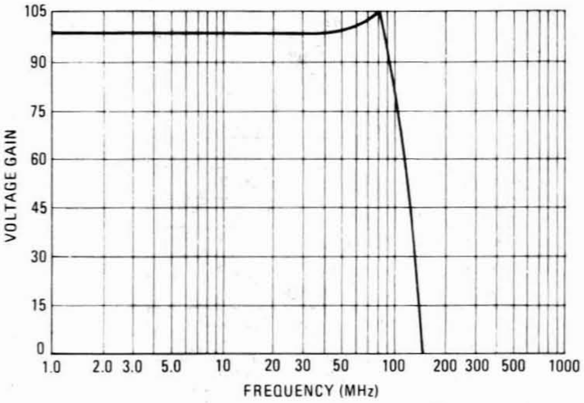


FIGURE 6 – OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

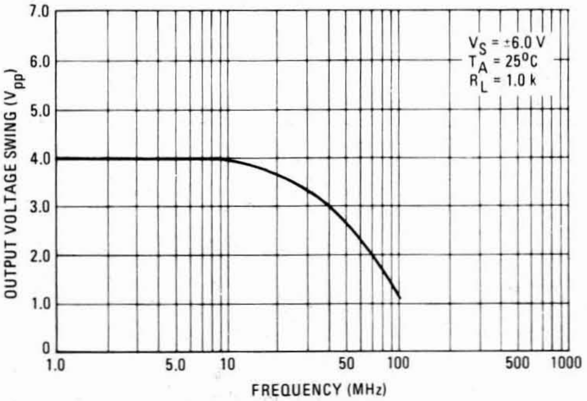


FIGURE 7 – OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

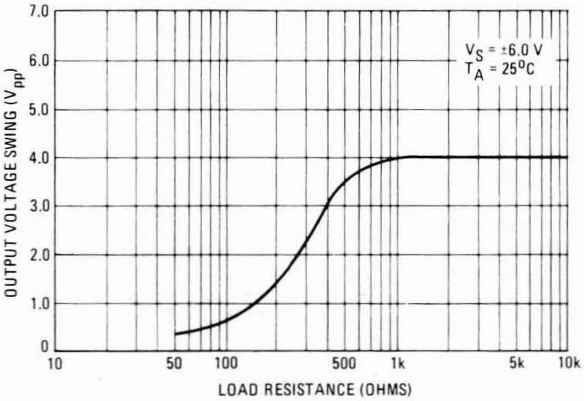


FIGURE 8 – VOLTAGE GAIN AS A FUNCTION OF $R_{adj}$ RESISTANCE

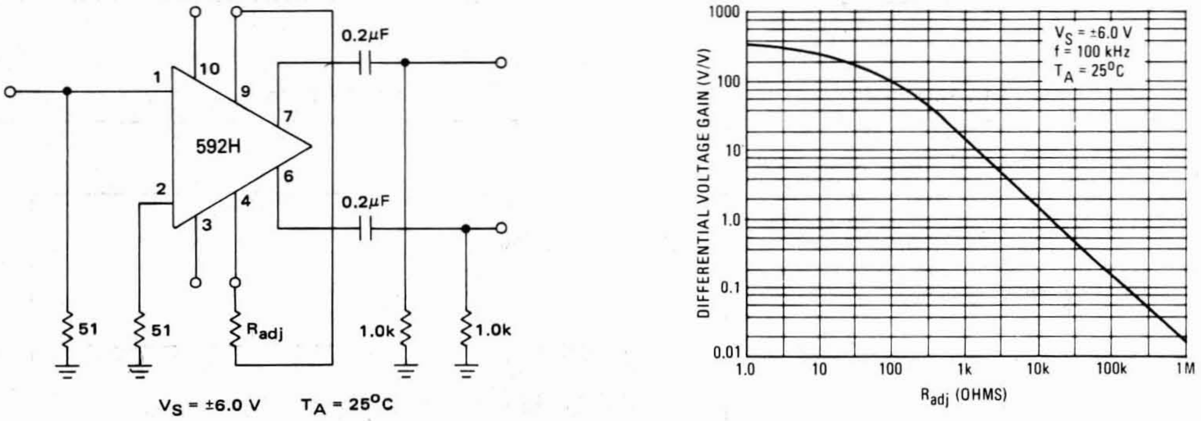

1
10
9
7
592H
6
2
4
3
0.2μF
0.2μF
51
51
Radj
1.0k
1.0k
VS = ±6.0 V TA = 25°C
1000
100
10
1.0
0.1
0.01
DIFFERENTIAL VOLTAGE GAIN (V/V)
VS = ±6.0 V
f = 100 kHz
TA = 25°C
1.0 10 100 1k 10k 100k 1M
Radj (OHMS)

FIGURE 9 – DISK/TAPE PHASE MODULATED READBACK SYSTEMS

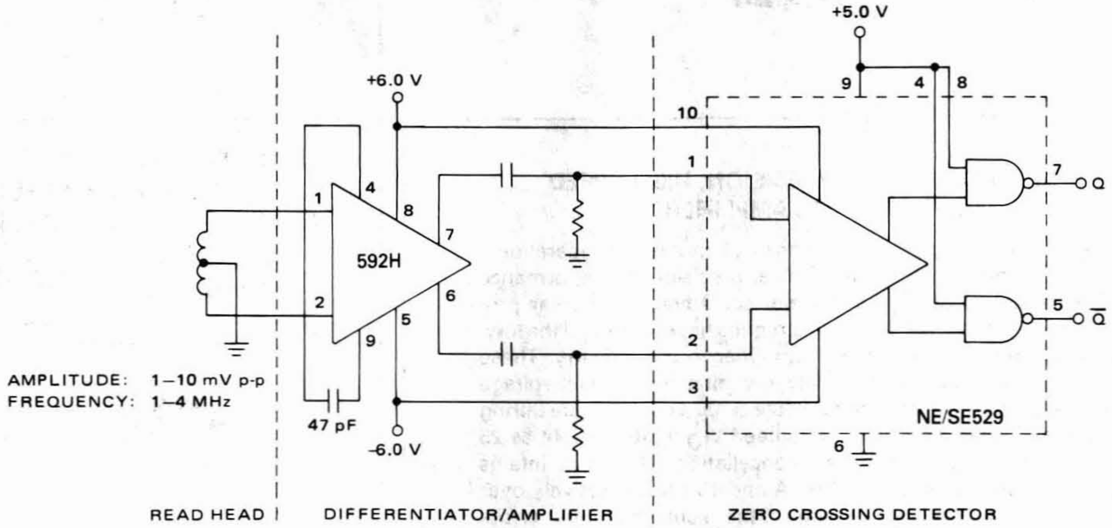
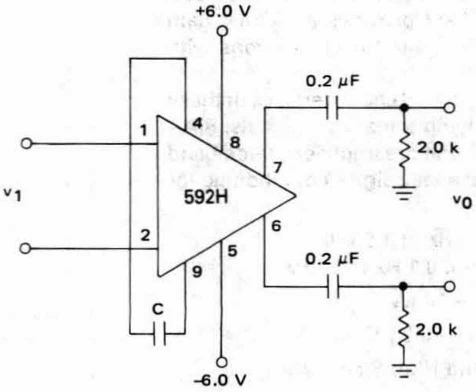

+5.0 V
+6.0 V
9
4
8
10
1
4
8
7
592H
6
2
5
9
1
2
3
7
Q
5
Q̄
NE/SE529
6
47 pF
-6.0 V
AMPLITUDE: 1–10 mV p-p
FREQUENCY: 1–4 MHz
READ HEAD
DIFFERENTIATOR/AMPLIFIER
ZERO CROSSING DETECTOR

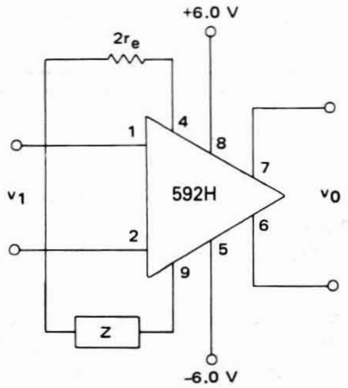
FIGURE 10 – DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION


+6.0 V
0.2 μF
1
4
8
2.0 k
7
v1
592H
vO
2
6
5
9
0.2 μF
C
2.0 k
-6.0 V

FOR FREQUENCY $f_1 << 1/2\,\pi\,(32)\,C$

$$v_O \cong 1.4 \times 10^4 C \frac{d_{v1}}{dt}$$

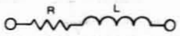
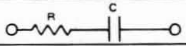
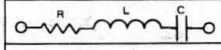
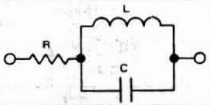
FIGURE 11 – FILTER NETWORKS


+6.0 V
2re
1
4
8
7
v1
592H
vO
2
6
5
9
Z
-6.0 V

$$\frac{v_O\,(s)}{v_1\,(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

BASIC CONFIGURATION

| Z NETWORK | FILTER TYPE | $\frac{v_O\,(s)}{v_1\,(s)}$ TRANSFER FUNCTION |
|---|---|---|
|  | Low Pass | $\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$ |
|  | High Pass | $\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$ |
|  | Band Pass | $\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\,s + 1/LC}\right]$ |
|  | Band Reject | $\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$ |

NOTE:
In the networks above, the R value used is assumed to include $2\,r_e$, or approximately 30 Ohms.

**MOTOROLA**

# OP-27
# OP-37

## ULTRA-LOW NOISE PRECISION, HIGH SPEED OPERATIONAL AMPLIFIERS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

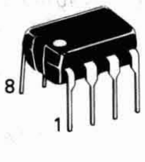
## ULTRA-LOW NOISE PRECISION, HIGH SPEED OPERATIONAL AMPLIFIERS

The OP-27 and OP-37 are a series of monolithic operational amplifiers which combine low-noise, precision dc performance and wide bandwidth all in one device. Advanced Bipolar processing and innovative design techniques have produced the lowest noise precision operational amplifier in the industry. These devices are trimmed for extremely low initial input offset voltage by utilizing a highly stable and reliable zener zap technique during factory testing which yields guaranteed $V_{IO}$ limits as tight as 25 µV. A unique input bias current cancellation scheme maintains low $I_{IB}$ and $I_{IO}$ to typically ±20 nA and 15 nA respectively over the full military temperature range. Other sources of input errors are reduced in excess of −120 dB due to extremely high common-mode and power supply rejection ratios.

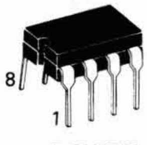
Also impressive, are the slew rate and bandwidth of these devices. The OP-27 has a gain bandwidth product of 8.0 MHz and slew rate of 2.8 V/µs. While the OP-37 provides a 63 MHz gain bandwidth product and 17 V/µs slew rate for applications with closed loop gains ≥5.

The precision, low noise and high speed characteristics of these devices make them ideal for amplifying transducer signals, RIAA phono, NAB tape head and microphone preamplifiers, wide band instrumentation amplifiers and high speed signal conditioning for data acquisition systems.

- Extremely Low-Noise — 3.0 nV/$\sqrt{\text{Hz}}$ at 1.0 kHz
  80 nVp-p, 0.1 Hz to 10 Hz
- Low Initial Input Offset Voltage — 10 µV
- Ultra Stable Input Offset Voltage — 0.2 µV/mo.
- Wide Gain Bandwidth Product and High Slew Rate:
  OP-27 — 8.0 MHz, 2.8 V/µs
  OP-37 — 63 MHz, 17 V/µs
- High Open-Loop Gain — 1.8 Million
- High Common-Mode Rejection — 126 dB
- Replaces OP-05, OP-06, OP-07, AD510, AD517, µA725 and NE5534

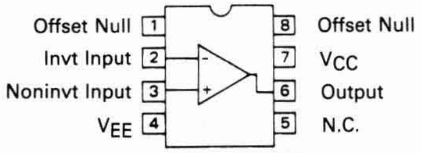


**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04



**Z SUFFIX**
CERAMIC PACKAGE
CASE 693-02

(Top View)



**ORDERING INFORMATION**

| Slew Rate | Device | | | Temperature Range | Package |
|---|---|---|---|---|---|
| | $V_{IO} \le 25\ \mu V$ | $V_{IO} \le 60\ \mu V$ | $V_{IO} \le 100\ \mu V$ | | |
| ≥ 1.7 V/µs | OP-27AZ | OP-27BZ | OP-27CZ | −55 to + 125°C | Ceramic DIP |
| | OP-27EZ | OP-27FZ | OP-27GZ | −25 to +85°C | Ceramic DIP |
| | OP-27EP | OP-27FP | OP-27GP | 0 to +70°C | Plastic DIP |
| ≥ 11 V/µs | OP-37AZ | OP-37BZ | OP-37CZ | −55 to +125°C | Ceramic DIP |
| | OP-37EZ | OP-37FZ | OP-37GZ | −25 to +85°C | Ceramic DIP |
| | OP-37EP | OP-37FP | OP-37GP | 0 to +70°C | Plastic DIP |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +22<br>−22 | V |
| Input Voltage Range (Note 1) | $V_{IDR}$ | ±22 | V |
| Differential Input Voltage (Note 2) | $V_{ID}$ | ±0.7 | V |
| Differential Input Current (Note 2) | $I_{ID}$ | ±25 | mA |
| Output Short-Circuit Duration | $t_s$ | Indefinite | |
| Power Dissipation and Thermal Characteristics<br>Plastic Package (P Suffix) $T_A = +36°C$ | $P_D$ | 500 | mW |
| Derate above $T_A = +62°C$ | $1/R_{\theta JA}$ | 5.6 | mW/°C |
| Ceramic Package (Z Suffix) $T_A = +75°C$ | $P_D$ | 500 | mW |
| Derate above $T_A = +75°C$ | $1/R_{\theta JA}$ | 6.7 | mW/°C |
| Operating Ambient Temperature<br>OP-27 and OP-37 A,B and C Grades | $T_A$ | −55 to +125 | °C |
| OP-27 and OP-37 E,F and G Grades (Ceramic Package) | | −25 to +85 | |
| OP-27 and OP-37EP, FP and GP Grades (Plastic Package) | | 0 to +70 | |
| Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range<br>Ceramic Package<br>Plastic Package | $T_{stg}$ | <br>−65 to +150<br>−65 to +125 | °C |

NOTES:

1. For supply voltages less than ±22 V, the absolute maximum input voltage range is equal to the supply voltage.
2. The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7 V, the input current must be limited to 25 mA.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C unless otherwise noted.)

| | | OP-27A/E/EP<br>OP-37A/E/EP | | | OP-27B/F/FP<br>OP-37B/F/FP | | | OP-27C/G/GP<br>OP-37C/G/GP | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Characteristic** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Input Offset Voltage | $V_{IO}$ | — | 10 | 25 | — | 20 | 60 | — | 30 | 100 | μV |
| Long Term Input Offset Voltage Stability (Note 3) | $V_{IO}/t$ | — | 0.2 | 1.0 | — | 0.3 | 1.5 | — | 0.4 | 2.0 | μV/mo |
| Input Offset Current | $I_{IO}$ | — | 7.0 | 35 | — | 9.0 | 50 | — | 12 | 75 | nA |
| Input Bias Current | $I_{IB}$ | — | ±10 | ±40 | — | ±12 | ±55 | — | ±15 | ±80 | nA |
| Input Noise Voltage 0.1 to 10 Hz (Note 4) | $e_{np-p}$ | — | 0.08 | 0.18 | — | 0.08 | 0.18 | — | 0.09 | 0.25 | $\mu V_{p-p}$ |
| Input Noise Voltage Density | $e_n$ | | | | | | | | | | $nV/\sqrt{Hz}$ |
| $f_o$ = 10 Hz | | — | 3.5 | 5.5 | — | 3.5 | 5.5 | — | 3.8 | 8.0 | |
| $f_o$ = 30 Hz | | — | 3.1 | 4.5 | — | 3.1 | 4.5 | — | 3.3 | 5.6 | |
| $f_o$ = 1000 Hz<br>(Note 4) | | — | 3.0 | 3.8 | — | 3.0 | 3.8 | — | 3.2 | 4.5 | |
| Input Noise Current Density | $i_n$ | | | | | | | | | | $pA/\sqrt{Hz}$ |
| $f_o$ = 10 Hz | | — | 1.7 | 4.0 | — | 1.7 | 4.0 | — | 1.7 | — | |
| $f_o$ = 30 Hz | | — | 1.0 | 2.3 | — | 1.0 | 2.3 | — | 1.0 | — | |
| $f_o$ = 1000 Hz<br>(Note 4) | | — | 0.4 | 0.6 | — | 0.4 | 0.6 | — | 0.4 | 0.6 | |
| Input Resistance — Differential Mode | $r_i$ | 1.5 | 6.0 | — | 1.2 | 5.0 | — | 0.8 | 4.0 | — | MΩ |
| Input Resistance — Common Mode | $R_{incm}$ | — | 3.0 | — | — | 2.5 | — | — | 2.0 | — | GΩ |
| Input Voltage Range | $V_{IR}$ | ±11.0 | ±12.3 | — | ±11.0 | ±12.3 | — | ±11.0 | ±12.3 | — | V |

(continued)

**ELECTRICAL CHARACTERISTICS (continued)**

| Characteristic | Symbol | OP-27A/E/EP<br>OP-37A/E/EP | | | OP-27B/F/FP<br>OP-37B/F/FP | | | OP-27C/G/GP<br>OP-37C/G/GP | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Common Mode Rejection Ratio<br>$V_{CM} = \pm 11$ V | CMRR | 114 | 126 | — | 106 | 123 | — | 100 | 120 | — | dB |
| Power Supply Rejection Ratio<br>$V_S = \pm 4.0$ V to ±18 V | PSRR | 100 | 120 | — | 100 | 120 | — | 94 | 114 | — | dB |
| Large-Signal Voltage Gain | $A_{VOL}$ | | | | | | | | | | V/mV |
| $R_L \geq 2.0$ kΩ, $V_O = \pm 10$ V | | 1000 | 1800 | — | 1000 | 1800 | — | 700 | 1500 | — | |
| $R_L \geq 1.0$ kΩ, $V_O = \pm 10$ V | | 800 | 1500 | — | 800 | 1500 | — | — | 1500 | — | |
| $R_L = 600$ Ω, $V_O = \pm 1.0$ V,<br>$V_S = \pm 4.0$ V | | — | 700 | — | — | 700 | — | — | 500 | — | |
| Output Voltage Swing | $V_O$ | | | | | | | | | | V |
| $R_L \geq 2.0$ kΩ | | ±12 | ±13.8 | — | ±12 | ±13.8 | — | ±11.5 | ±13.5 | — | |
| $R_L \geq 600$ Ω | | ±10 | ±11.5 | — | ±10 | ±11.5 | — | ±10 | ±11.5 | — | |
| Slew Rate, $R_L \geq 2.0$ kΩ | SR | | | | | | | | | | V/μs |
| OP-27, OP-24 | | 1.7 | 2.8 | — | 1.7 | 2.8 | — | 1.7 | 2.8 | — | |
| OP-37, OP-34 | | 11 | 17 | — | 11 | 17 | — | 11 | 17 | — | |
| Gain Bandwidth Product | GBW | | | | | | | | | | MHz |
| OP-27, OP-24 | | 5.0 | 8.0 | — | 5.0 | 8.0 | — | 5.0 | 8.0 | — | |
| OP-37, OP-34, Av ≥ 5.0 | | | | | | | | | | | |
| $f_o = 10$ kHz | | 4.5 | 63 | — | 4.5 | 63 | — | 4.5 | 63 | — | |
| $f_o = 1.0$ MHz | | — | 40 | — | — | 40 | — | — | 40 | — | |
| Open Loop Output Resistance<br>$V_O = 0$, $I_O = 0$ | $r_o$ | — | 70 | — | — | 70 | — | — | 70 | — | Ω |
| Power Dissipation<br>$V_O = 0$, No Load | $P_D$ | — | 90 | 140 | — | 90 | 140 | — | 100 | 170 | mW |
| Offset Adjustment Range<br>$R_P = 10$ kΩ | | — | ±4.0 | — | — | ±4.0 | — | — | ±4.0 | — | mV |

NOTES (continued)

3. Long term input offset voltage stability for the OP-27 and OP-37 series, refers to the average trend line of $V_{IO}$ versus time over extended periods after the first 30 days of operation. Excluding the first hour of operation, changes in $V_{IO}$ during the first 30 days are typically 2.5 μV.
4. Sample tested.

**ELECTRICAL CHARACTERISTICS** ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = T_{low}$ to $T_{high}$ [Note 5])

| Characteristic | Symbol | OP-27A<br>OP-37A | | | OP-27B<br>OP-37B | | | OP-27C<br>OP-37C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{IO}$ | — | 30 | 60 | — | 50 | 200 | — | 70 | 300 | μV |
| Average Input Offset Drift<br>(Note 6) | $TCV_{IO}$ | — | 0.2 | 0.6 | — | 0.3 | 1.3 | — | 0.4 | 1.8 | μV/°C |
| Input Offset Current | $I_{IO}$ | — | 15 | 50 | — | 22 | 85 | — | 30 | 135 | nA |
| Input Bias Current | $I_{IB}$ | — | ±20 | ±60 | — | ±28 | ±95 | — | ±35 | ±150 | nA |
| Input Voltage Range | $V_{IR}$ | ±10.3 | ±11.5 | — | ±10.3 | ±11.5 | — | ±10.2 | ±11.5 | — | V |
| Common Mode Rejection Ratio<br>$V_{CM} = \pm 10$ V | CMRR | 108 | 122 | — | 100 | 119 | — | 94 | 116 | — | dB |
| Power Supply Rejection Ratio<br>$V_S = \pm 4.5$ V to ±18 V | PSRR | 96 | 114 | — | 94 | 114 | — | 86 | 108 | — | dB |
| Large-Signal Voltage Gain<br>$R_L \geq 2.0$ kΩ, $V_O = \pm 10$ V | $A_{VOL}$ | 600 | 1200 | — | 500 | 1000 | — | 300 | 800 | — | V/mV |
| Output Voltage Swing<br>$R_L \geq 2.0$ kΩ | $V_O$ | ±11.5 | ±13.5 | — | ±11.0 | ±13.2 | — | ±10.5 | ±13.0 | — | V |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = $T_{low}$ to $T_{high}$ [Note 5])

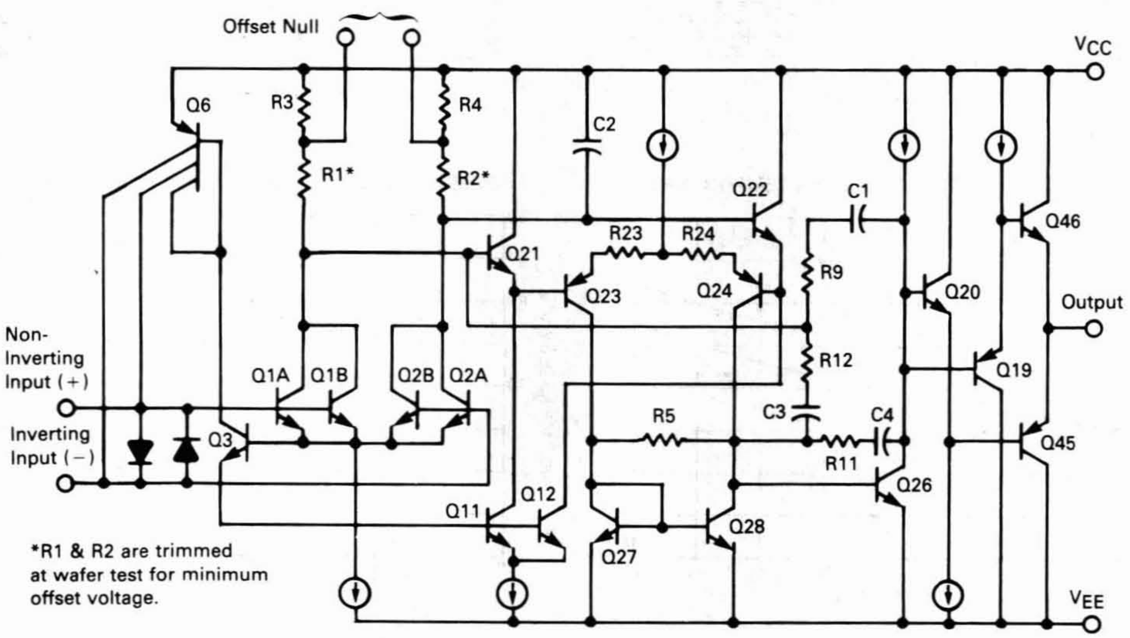
| Characteristic | Symbol | OP-27E/EP<br>OP-37E/EP |  |  | OP-27F/FP<br>OP-37F/FP |  |  | OP-27G/GP<br>OP-37G/GP |  |  | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage | $V_{IO}$ | — | 20 | 50 | — | 40 | 140 | — | 55 | 220 | µV |
| Average Input Offset Drift (Note 6) | $TCV_{IO}$ | — | 0.2 | 0.6 | — | 0.3 | 1.3 | — | 0.4 | 1.8 | µV/°C |
| Input Offset Current | $I_{IO}$ | — | 10 | 50 | — | 14 | 85 | — | 20 | 135 | nA |
| Input Bias Current | $I_{IB}$ | — | ±14 | ±60 | — | ±18 | ±95 | — | ±25 | ±150 | nA |
| Input Voltage Range | $V_{IR}$ | ±10.5 | ±11.8 | — | ±10.5 | ±11.8 | — | ±10.5 | ±11.8 | — | V |
| Common Mode Rejection Ratio $V_{CM}$ = ±10 V | CMRR | 110 | 124 | — | 102 | 121 | — | 96 | 118 | — | dB |
| Power Supply Rejection Ratio $V_S$ = ±4.5 V to ±18 V | PSRR | 97 | 114 | — | 96 | 114 | — | 90 | 114 | — | dB |
| Large-Signal Voltage Gain $R_L \geq 2.0$ kΩ, $V_O$ = ±10 V | $A_{VOL}$ | 750 | 1500 | — | 700 | 1300 | — | 450 | 1000 | — | V/mV |
| Output Voltage Swing $R_L \geq 2.0$ kΩ | $V_O$ | ±11.7 | ±13.6 | — | ±11.4 | ±13.5 | — | ±11 | ±13.3 | — | V |

NOTES (continued)

5. $T_{low}$ = −55°C for OP-27A/OP-37A, OP-27B/OP-37B, OP-27C/OP-37C; = −25°C for OP-27E/OP-37E, OP-27F/OP-37F, OP-27G/OP-37G; = 0°C for OP-27EP/OP-37EP, OP-27FP/OP-37FP, OP-27GP/OP-37GP

   $T_{high}$ = +125°C for OP-27A/OP-37A, OP-27B/OP-37B, OP-27C/OP-37C; = +85°C for OP-27E/OP-37E, OP-27F/OP-37F, OP-27G/OP-37G; = +70°C for OP-27EP/OP-37EP, OP-27FP/OP-37FP, OP-27GP/OP-37GP
6. $TCV_{IO}$ performance is within specifications unnulled or when nulled with a potentiometer Rp = 8 kΩ to 20 kΩ.

## ABBREVIATED CIRCUIT SCHEMATIC



Offset Null
$V_{CC}$
Q6
R3
R4
C2
R1*
R2*
Q22
C1
Q46
Q21
R23
R24
R9
Q23
Q24
Q20
Output
Non-Inverting Input (+)
Q1A
Q1B
Q2B
Q2A
R12
Q19
Inverting Input (−)
Q3
R5
C3
C4
Q45
R11
Q26
Q12
Q11
Q28
Q27
$V_{EE}$

*R1 & R2 are trimmed at wafer test for minimum offset voltage.

## TYPICAL CHARACTERISTICS

(Performance curves are for both OP-27 and OP-37 devices unless otherwise noted.)

**FIGURE 1 — 0.1 Hz TO 10 Hz P-P NOISE TESTER FREQUENCY RESPONSE**

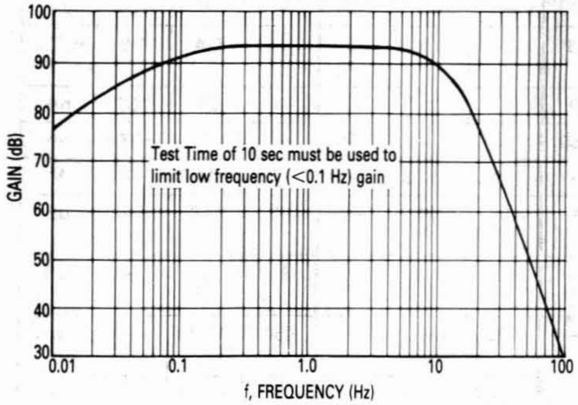


**FIGURE 2 — VOLTAGE NOISE versus FREQUENCY**

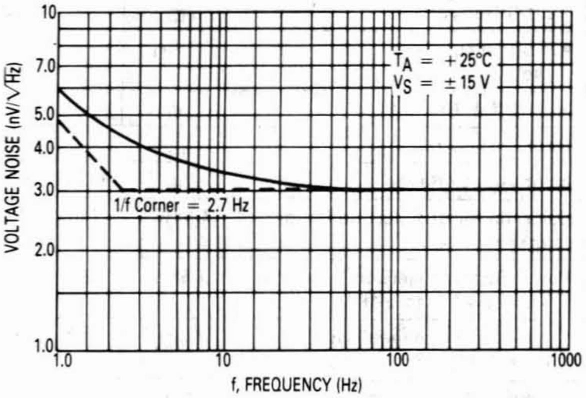


**FIGURE 3 — INPUT WIDEBAND VOLTAGE NOISE versus BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)**

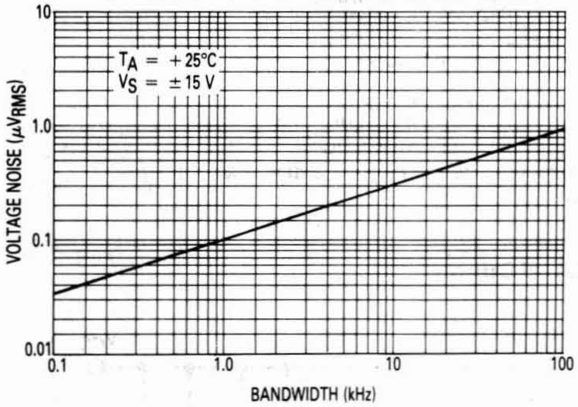


**FIGURE 4 — TOTAL NOISE versus SOURCE RESISTANCE**

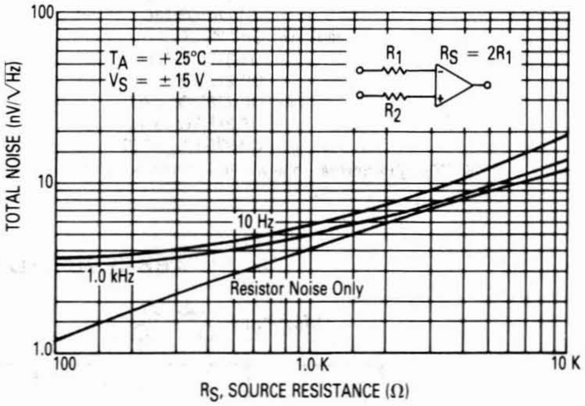


**FIGURE 5 — VOLTAGE NOISE versus TEMPERATURE**

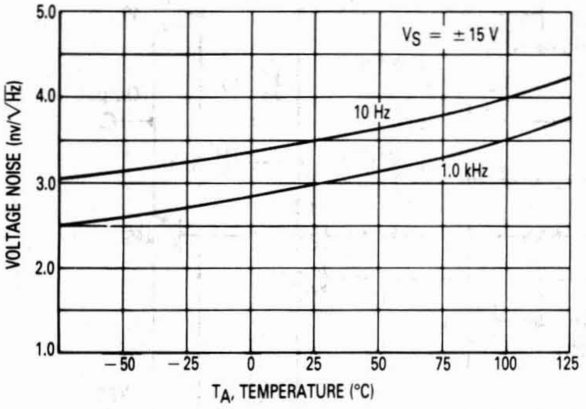


**FIGURE 6 — VOLTAGE NOISE versus SUPPLY VOLTAGE**

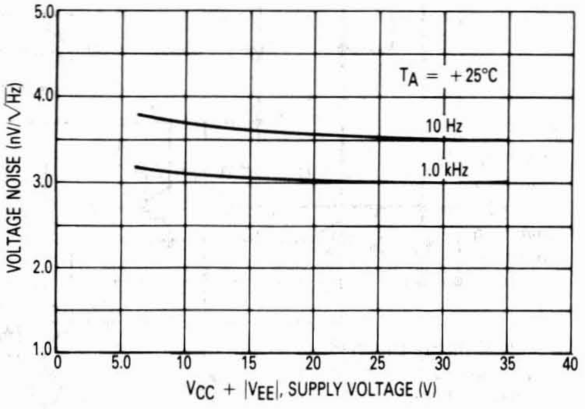


FIGURE 7 — CURRENT NOISE versus FREQUENCY

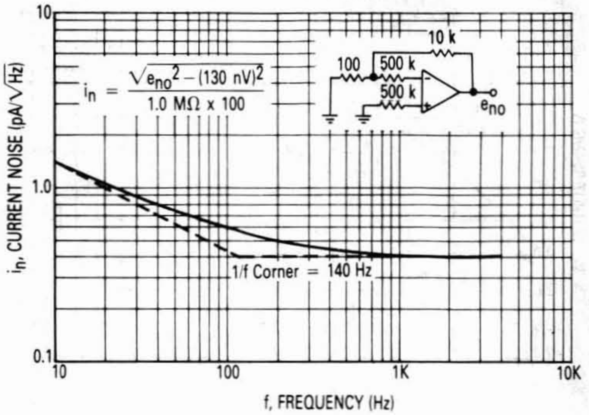


FIGURE 8 — SUPPLY CURRENT versus SUPPLY VOLTAGE

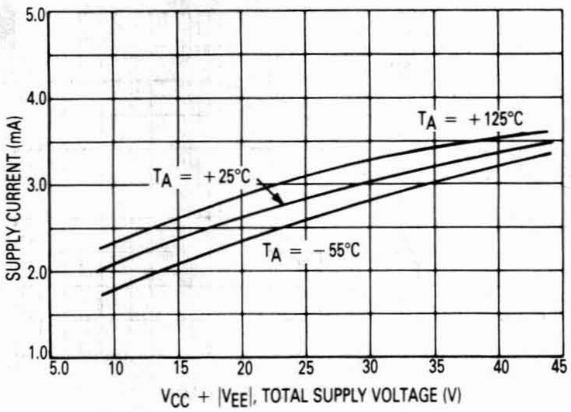


FIGURE 9 — INPUT BIAS CURRENT versus TEMPERATURE

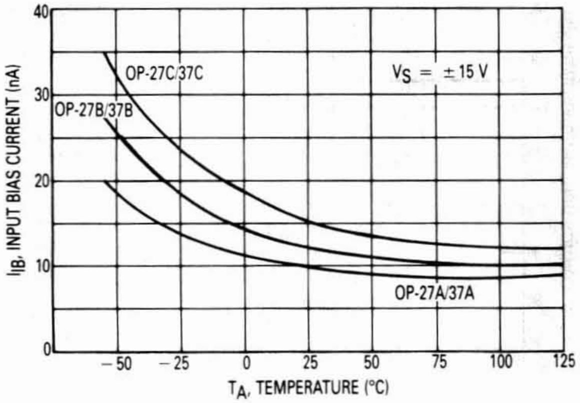


FIGURE 10 — INPUT OFFSET CURRENT versus TEMPERATURE

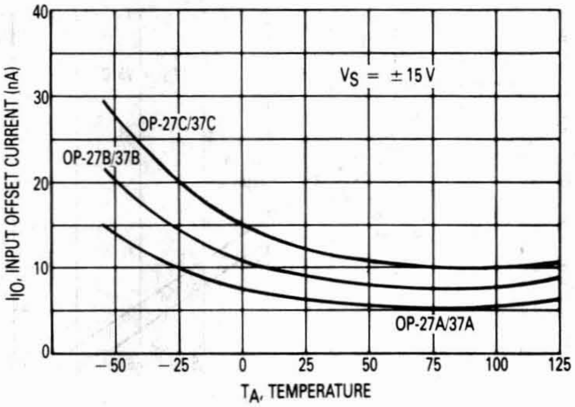


FIGURE 11 — COMMON MODE INPUT RANGE versus SUPPLY VOLTAGE

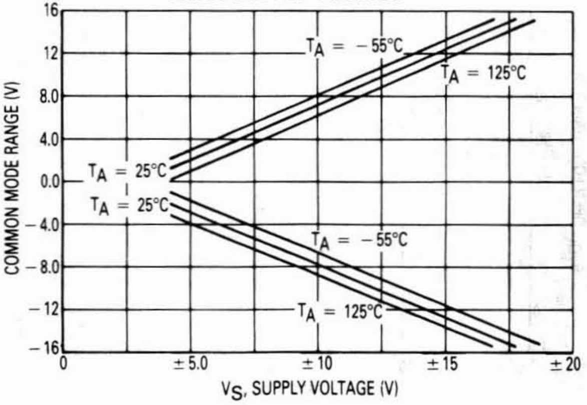


FIGURE 12 — OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

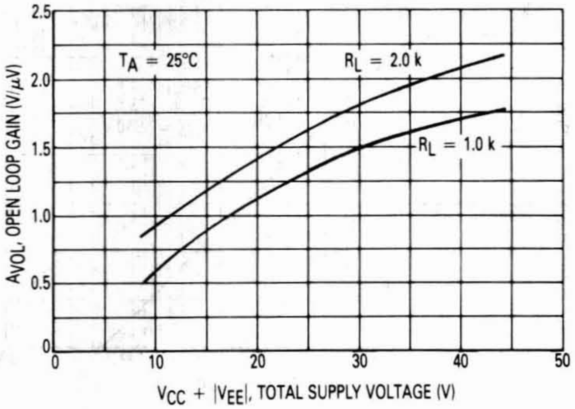


**FIGURE 13 — OPEN LOOP VOLTAGE GAIN versus LOAD RESISTANCE**

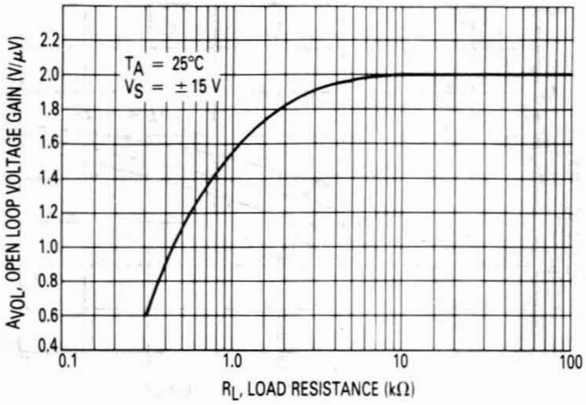


**FIGURE 14 — MAXIMUM OUTPUT SWING versus RESISTIVE LOAD**

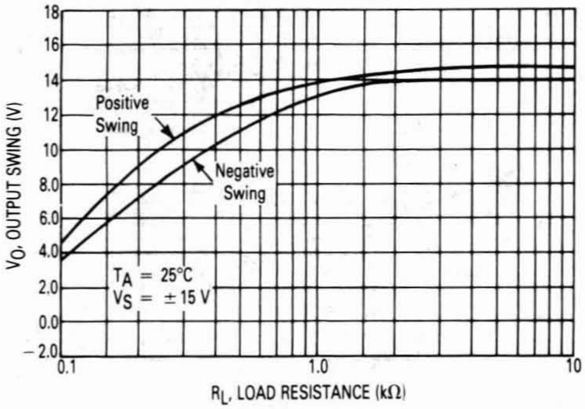


**FIGURE 15 — POWER SUPPLY REJECTION RATIO versus FREQUENCY**

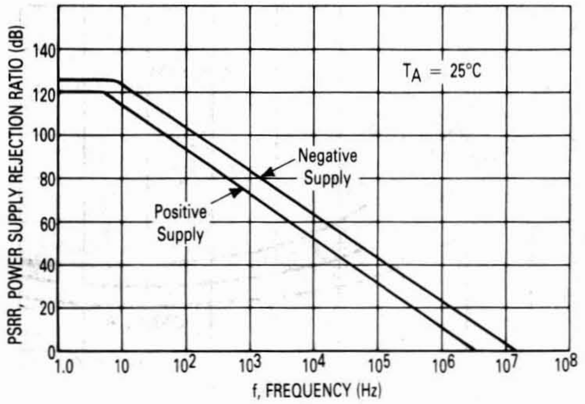


**FIGURE 16 — OP-27 COMMON MODE REJECTION RATIO versus FREQUENCY**

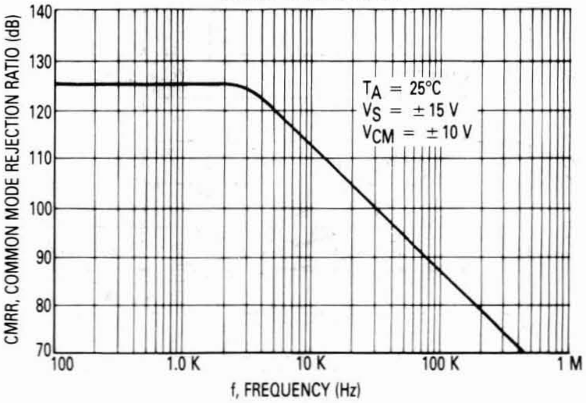


**FIGURE 17 — OP-37 COMMON MODE REJECTION RATIO versus FREQUENCY**

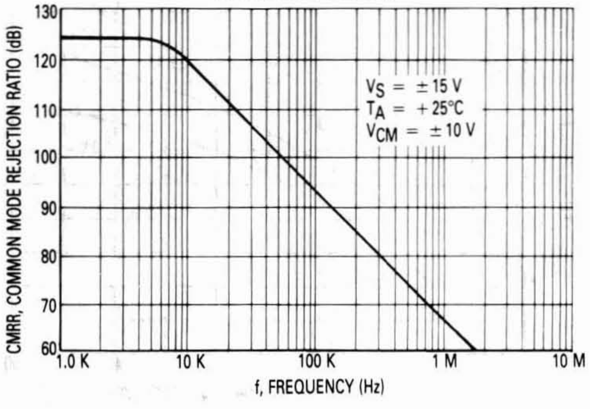


**FIGURE 18 — OP-27 OPEN LOOP GAIN versus FREQUENCY**

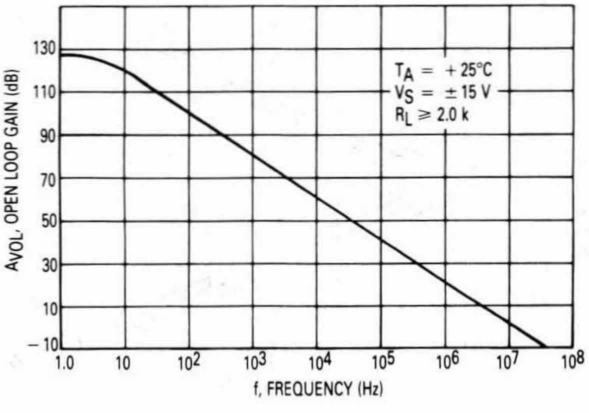


FIGURE 19 — OP-37 OPEN LOOP GAIN versus FREQUENCY

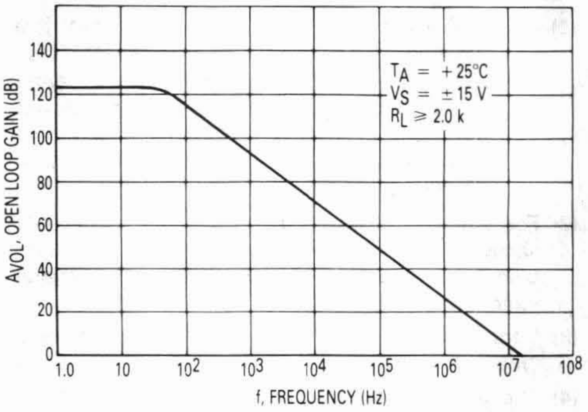


FIGURE 20 — OP-27 MAXIMUM UNDISTORTED OUTPUT versus FREQUENCY

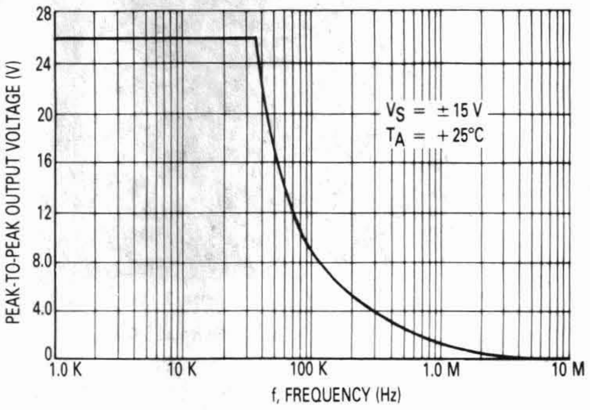


FIGURE 21 — OP-37 MAXIMUM UNDISTORTED OUTPUT versus FREQUENCY

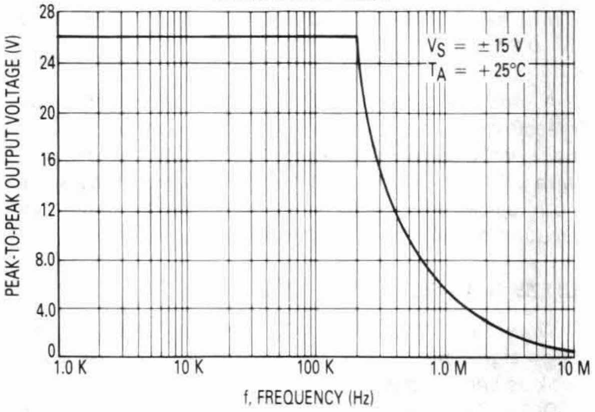
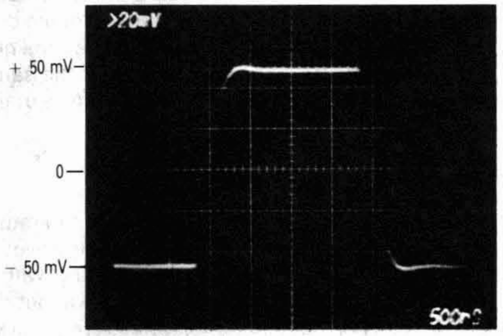


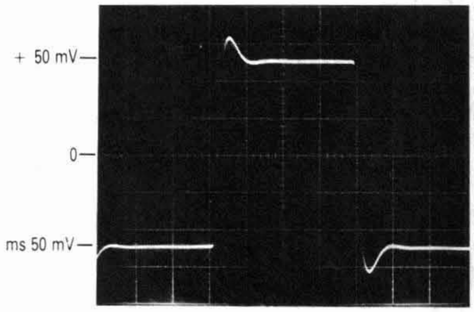
FIGURE 22 — OP-27 SMALL-SIGNAL TRANSIENT RESPONSE



$A_V$ = +1.0
$T_A$ = +25°C
$V_S$ = ±15 V
$C_L$ = 12 pF
$R_L$ = ∞

Vertical: 20 mV/cm
Horizontal: 500 ns/cm

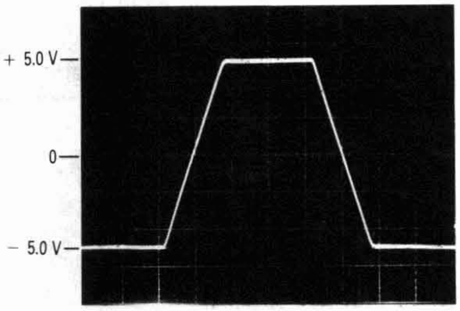
FIGURE 23 — OP-37 SMALL-SIGNAL TRANSIENT RESPONSE



$A_V$ = +5.0
$T_A$ = +25°C
$V_S$ = ±15 V
$C_L$ = 27 pF
$R_L$ = ∞

Vertical: 20 mV/cm
Horizontal: 200 ns/cm

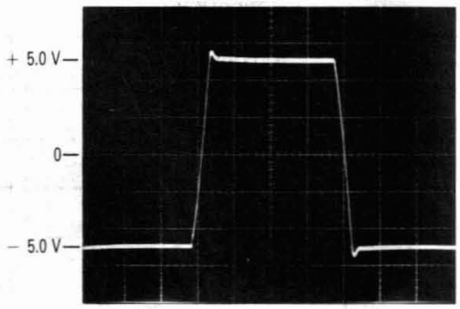
FIGURE 24 — OP-27 LARGE-SIGNAL TRANSIENT RESPONSE



$A_V$ = +1.0
$T_A$ = +25°C
$V_S$ = ±15 V
$C_L$ = 12 pF
$R_L$ = ∞

Vertical: 2.0 V/cm
Horizontal: 2.0 μS/cm

FIGURE 25 — OP-37 LARGE-SIGNAL TRANSIENT RESPONSE



$A_V = +5.0$
$T_A = +25°C$
$V_S = \pm 15$ V
$C_L = 27$ pF
$R_L = \infty$

Vertical: 2.0 V/cm
Horizontal: 500 μs/cm

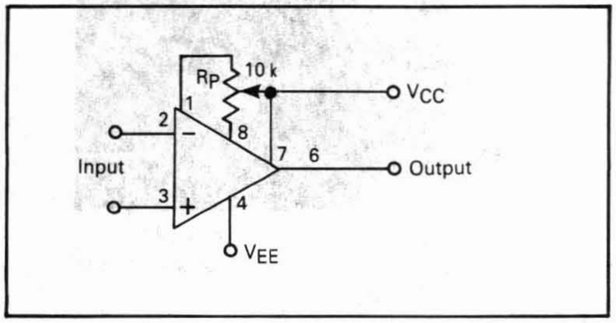
## APPLICATIONS INFORMATION

The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

### OFFSET VOLTAGE ADJUSTMENT

The input offset voltage and drift over temperature are permanently trimmed at wafer testing. However, if further adjustment of $V_{IO}$ is required, nulling with a 10 kΩ potentiometer as shown in Figure 26 will not degrade $TCV_{IO}$. Other potentiometer values from 1.0 kΩ to 1.0 MΩ can be used with a slight degradation (0.1 to 0.2 μV/°C) of $TCV_{IO}$. Trimming to a value other than zero creates a drift of ($V_{IO}$/300) μV/°C, e.g. if $V_{IO}$ is adjusted to 100 μV, the change in $TCV_{IO}$ will be 0.33 μV/°C. The offset voltage adjustment range with a 10 kΩ potentiometer is ±4.0 mV. If a smaller adjustment range is required, the sensitivity and/or resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors.

FIGURE 26 — OFFSET NULLING CIRCUIT



### NOISE MEASUREMENTS

The extremely low noise of these devices can make accurate measurement a difficult task. In order to realize the 80 nV peak-to-peak noise specification of the op amp in the 0.1 Hz to 10 Hz frequency range, the following guidelines must be observed:

(1) The device has to be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 4.0 μV due to its chip temperature increasing 14 to 20°C from the moment the power supplies are turned on. In the 10 sec measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(2) For similar reasons, the device has to be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of several nanovolts.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10 sec. As shown in the noise tester frequency response curve (Figure 1) the 0.1 Hz corner is defined by only one zero. The test time of 10 sec acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10 Hz noise-voltage density measurement will correlate well with a 0.1 Hz-to-10 Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

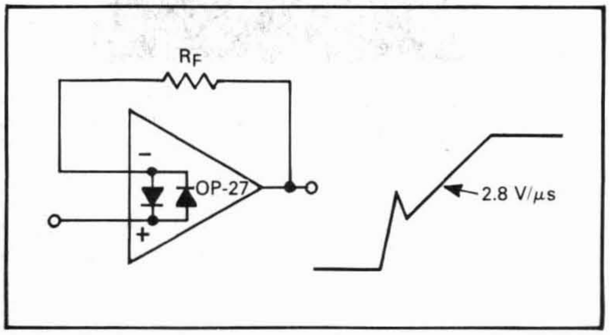
### UNITY GAIN BUFFER APPLICATIONS FOR OP-27

When $R_F \leq 100\ \Omega$ and the input is driven with a fast, large signal pulse (> 1.0 V), the output waveform will look as shown in Figure 27.

During the initial fast input step, the input protection diodes effectively short the output to the input and current limit only by the output short circuit protection of the signal generator. With $R_F \geq 500\ \Omega$, the output is capable of handling the current requirements ($I_L \leq 20$ mA at 10 V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_F > 2.0$ kΩ, a pole will be created with $R_F$ and the amplifier's input capacitance (8.0 pF), creating additional phase shift and reducing the phase margin. A small capacitor (20 to 50 pF) in parallel with $R_F$ will eliminate this problem.

FIGURE 27 — PULSED OPERATION



**MOTOROLA**

# TL071
# TL072
# TL074

## Specifications and Applications Information

## LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

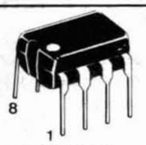
**SILICON MONOLITHIC INTEGRATED CIRCUITS**

### LOW-NOISE JFET INPUT OPERATIONAL AMPLIFIERS

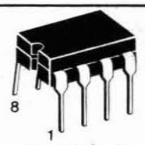
These low-noise JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, the devices exhibit low-noise and low harmonic distortion making them ideal for use in high-fidelity audio amplifier applications.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products. Devices with an "M" suffix are specified over the military operating temperature range of −55°C to +125°C and those with a "C" suffix are specified from 0°C to +70°C.

- Low Input Noise Voltage — 18 nV/$\sqrt{\text{Hz}}$ Typ
- Low Harmonic Distortion — 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance — $10^{12}$ Ω Typ
- High Slew Rate — 13 V/µs Typ
- Wide Gain Bandwidth — 4.0 MHz Typ
- Low Supply Current — 1.4 mA per Amp

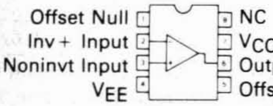


**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

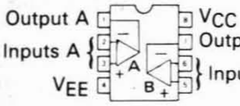


**JG SUFFIX**
CERAMIC PACKAGE
CASE 693-02

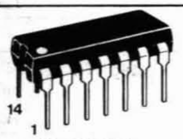
**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8



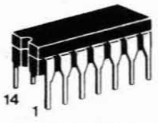
TL071
(Top View)



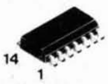
TL072
(Top View)



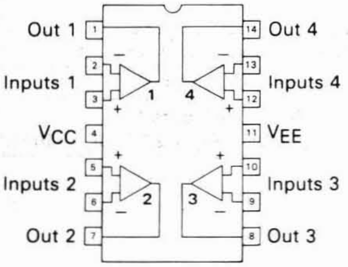
**N SUFFIX**
PLASTIC PACKAGE
CASE 646-05
(TL074 only)



**J SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA
(TL074 only)



**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14



TL074 (Top View)

### ORDERING INFORMATION

| Op Amp Function | Device | Temperature Range | Package |
|---|---|---|---|
| Single | TL071ACD, BCD, CD | 0 to +70°C | SO-8 |
| | TL071ACJG, BCJG, CJG | | Ceramic DIP |
| | TL071ACP, BCP, CP | | Plastic DIP |
| | TL071MJG | −55 to +125°C | Ceramic DIP |
| Dual | TL072ACD, BCD, CD | 0 to +70°C | SO-8 |
| | TL072ACJG, BCJG, CJG | | Ceramic DIP |
| | TL072ACP, BCP, CP | | Plastic DIP |
| | TL072MJG | −55 to +125°C | Ceramic DIP |
| Quad | TL074ACD, BCD, CD | 0 to +70°C | SO-14 |
| | TL074ACJ, BCJ, CJ | | Ceramic DIP |
| | TL074ACN, BCN, CN | | Plastic DIP |
| | TL074MJ | −55 to +125°C | Ceramic DIP |

## MAXIMUM RATINGS

| Rating | Symbol | TL07_ M | TL07_ C<br>TL07_ AC<br>TL07_ BC | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>−18 | +18<br>−18 | V |
| Differential Input Voltage | $V_{ID}$ | ±30 | ±30 | V |
| Input Voltage Range (Note 1) | $V_{IDR}$ | ±15 | ±15 | V |
| Output Short-Circuit Duration (Note 2) | $t_S$ | Continuous | | |
| Power Dissipation | | | | |
| Plastic Package (N,P) | $P_D$ | — | 680 | mW |
| Derate above $T_A$ = +47°C | $1/\theta_{JA}$ | — | 10 | mW/°C |
| Ceramic Package (J, JG) | $P_D$ | 680 | 680 | mW |
| Derate above $T_A$ = +82°C | $1/\theta_{JA}$ | 10 | 10 | mW/°C |
| Operating Ambient Temperature Range | $T_A$ | −55 to +125 | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | −65 to +150 | °C |

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 volts, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25° unless otherwise noted).

| Characteristic | Symbol | TL07_ M | | | TL07_ C<br>TL07_ AC<br>TL07_ BC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($R_S$ ≤ 10 k, $V_{CM}$ = 0) | $V_{IO}$ | | | | | | | mV |
| TL071, TL072 | | — | 3.0 | 6.0 | — | 3.0 | 10 | |
| TL074 | | — | 3.0 | 9.0 | — | 3.0 | 10 | |
| TL07_ A | | — | — | — | — | 3.0 | 6.0 | |
| TL07_ B | | — | — | — | — | 2.0 | 3.0 | |
| Average Temperature Coefficient of Input Offset Voltage $R_S$ = 50 Ω, $T_A$ = $T_{low}$ to $T_{high}$ (Note 3) | $\Delta V_{IO}/\Delta T$ | — | 10 | — | — | 10 | — | μV/°C |
| Input Offset Current ($V_{CM}$ = 0) (Note 4) | $I_{IO}$ | | | | | | | pA |
| TL07_ | | — | 5.0 | 50 | — | 5.0 | 50 | |
| TL07_ A, TL07_ B | | — | — | — | — | 5.0 | 50 | |
| Input Bias Current ($V_{CM}$ = 0) (Note 4) | $I_{IB}$ | | | | | | | pA |
| TL07_ | | — | 30 | 200 | — | 30 | 200 | |
| TL07_ A, TL07_ B | | — | — | — | — | 30 | 200 | |
| Input Resistance | $r_i$ | — | $10^{12}$ | — | — | $10^{12}$ | — | Ω |
| Common Mode Input Voltage Range | $V_{ICR}$ | | | | | | | V |
| TL07_ | | ±11 | +15, −12 | — | ±10 | +15, −12 | — | |
| TL07_ A, TL07_ B | | — | — | — | ±11 | +15, −12 | — | |
| Large-Signal Voltage Gain ($V_O$ = ±10 V, $R_L$ ≥, 2.0 k) | $A_{VOL}$ | | | | | | | V/mV |
| TL07_ | | 35 | 150 | — | 25 | 150 | — | |
| TL07_ A, TL07_ B | | — | — | — | 50 | 150 | — | |
| Output Voltage Swing (Peak-to-Peak) ($R_L$ = 10 k) | $V_O$ | 24 | 28 | — | 24 | 28 | — | V |
| Common Mode Rejection Ratio ($R_S$ ≤ 10 k) | CMRR | | | | | | | dB |
| TL07_ | | 80 | 100 | — | 70 | 100 | — | |
| TL07_ A, TL07_ B | | — | — | — | 80 | 100 | — | |
| Supply Voltage Rejection Ratio ($R_S$ ≤ 10 k) | PSRR | | | | | | | dB |
| TL07_ | | 80 | 100 | — | 70 | 100 | — | |
| TL07_ A, TL07_ B | | — | — | — | 80 | 100 | — | |
| Supply Current (Each Amplifier) | $I_D$ | — | 1.4 | 2.5 | — | 1.4 | 2.5 | mA |
| Unity Gain Bandwidth | BW | — | 4.0 | — | — | 4.0 | — | MHz |
| Slew Rate (See Figure 1) $V_{in}$ = 10 V, $R_L$ = 2.0 k, $C_L$ = 100 pF | SR | 10 | 13 | — | — | 13 | — | V/μs |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25° unless otherwise noted).

| | | TL07_ M | | | TL07_ C<br>TL07_ AC<br>TL07_ BC | | | |
|---|---|---|---|---|---|---|---|---|
| **Characteristic** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Rise Time (See Figure 1) | $t_r$ | — | 0.1 | — | — | 0.1 | — | µs |
| Overshoot Factor<br>$V_{in}$ = 20 mV, $R_L$ = 2.0 k, $C_L$ = 100 pF | — | — | 10 | — | — | 10 | — | % |
| Equivalent Input Noise Voltage<br>$R_S$ = 100 Ω, f = 1000 Hz | $e_n$ | — | 18 | — | — | 18 | — | nV/√Hz |
| Equivalent Input Noise Current<br>$R_S$ = 100 Ω, f = 1000 Hz | $i_n$ | — | 0.01 | — | — | 0.01 | — | pA/√Hz |
| Total Harmonic Distortion<br>$V_O$ (RMS) = 10 V, $R_S \leq$ 1.0 k<br>$R_L \geq$ 2.0 k, f = 1000 Hz | THD | — | 0.01 | — | — | 0.01 | — | % |
| Channel Separation<br>$A_V$ = 100 | — | — | 120 | — | — | 120 | — | dB |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = $T_{high}$ to $T_{low}$ [Note 3]).

| | | TL07_ M | | | TL07_ C<br>TL07_ AC<br>TL07_ BC | | | |
|---|---|---|---|---|---|---|---|---|
| **Characteristic** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Input Offset Voltage ($R_S \leq$ 10 k, $V_{CM}$ = 0) | $V_{IO}$ | | | | | | | mV |
| TL071, TL072 | | — | — | 9.0 | — | — | 13 | |
| TL074 | | — | — | 15 | — | — | 13 | |
| TL07_ A | | — | — | — | — | — | 7.5 | |
| TL07_ B | | — | | — | | — | 5.0 | |
| Input Offset Current ($V_{CM}$ = 0) (Note 4) | $I_{IO}$ | | | | | | | nA |
| TL07_ | | — | — | 20 | — | — | 2.0 | |
| TL07_ A, TL07_ B | | — | — | — | — | — | 2.0 | |
| Input Bias Current ($V_{CM}$ = 0) (Note 4) | $I_{IB}$ | | | | | | | nA |
| TL07_ | | — | — | 50 | — | — | 7.0 | |
| TL07_ A, TL07_ B | | — | — | — | — | — | 7.0 | |
| Large-Signal Voltage Gain ($V_O$ = ±10 V, $R_L \geq$ 2.0 k) | $A_{VOL}$ | | | | | | | V/mV |
| TL07_ | | 20 | — | — | 15 | — | — | |
| TL07_ A, TL07_ B | | — | — | — | 25 | — | — | |
| Output Voltage Swing (Peak-to-Peak) | $V_O$ | | | | | | | V |
| (RL ≥ 10 k) | | 24 | — | — | 24 | — | — | |
| ($R_L \geq$ 2.0 k) | | 20 | — | — | 20 | — | — | |

NOTES (Continued):

3. $T_{low}$ = −55°C for TL071M, TL072M, TL074M
   = 0°C for TL071C, TL071AC, TL071BC
   TL072C, TL072AC, TL072BC
   TL074C, TL074AC

   $T_{high}$ = + 125°C for TL071M, TL072M, TL074M
   = +70°C for TL071C, TL071AC, TL071BC
   TL072C, TL072AC, TL072BC
   TL074C, TL074AC
4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain Junction Temperature as close to ambient temperatures as possible, pulse techniques must be used during test.

## TEST CIRCUITS

**FIGURE 1 — UNITY GAIN VOLTAGE FOLLOWER**

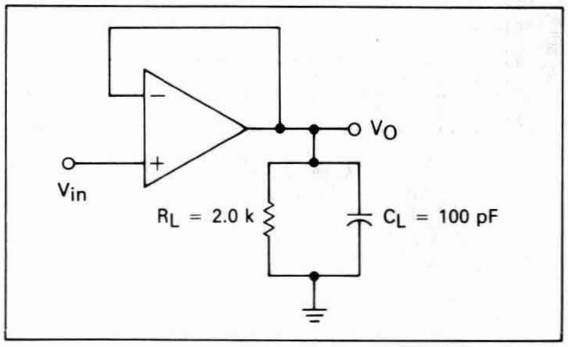


**FIGURE 2 — INVERTING GAIN OF 10 AMPLIFIER**

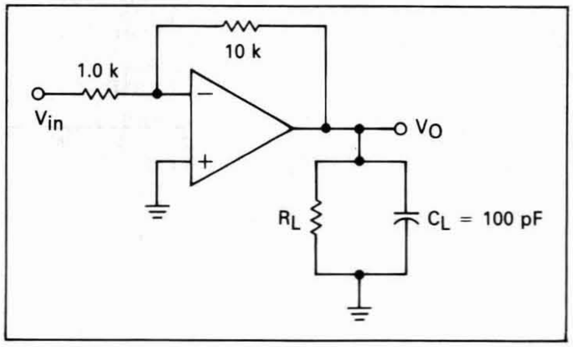


FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

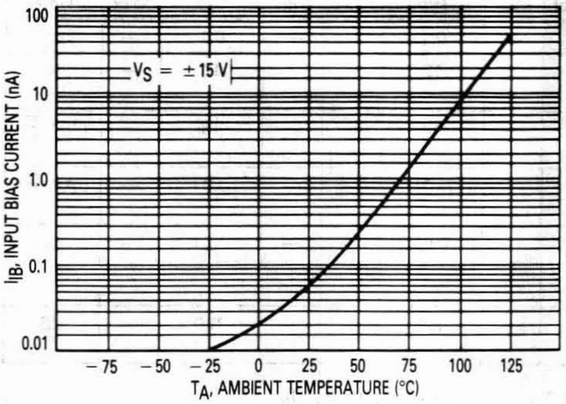


FIGURE 4 — OUTPUT VOLTAGE SWING versus FREQUENCY

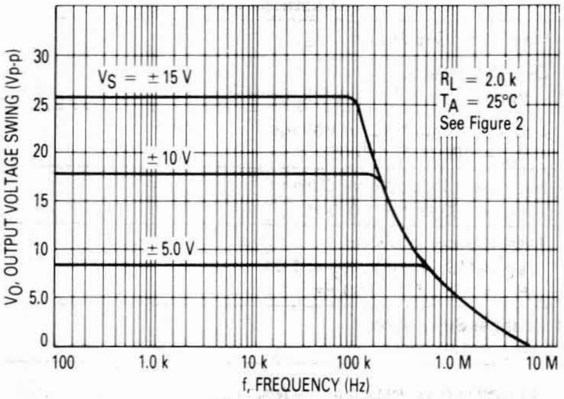


FIGURE 5 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

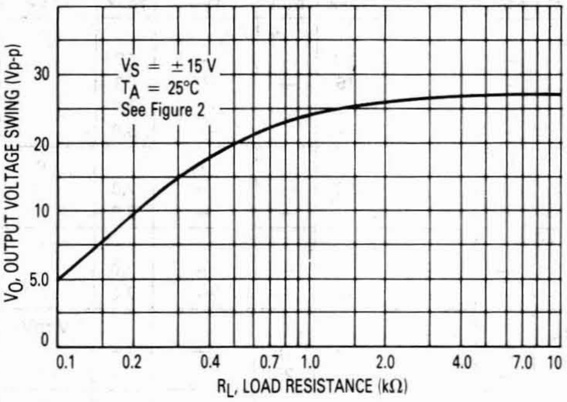


FIGURE 6 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

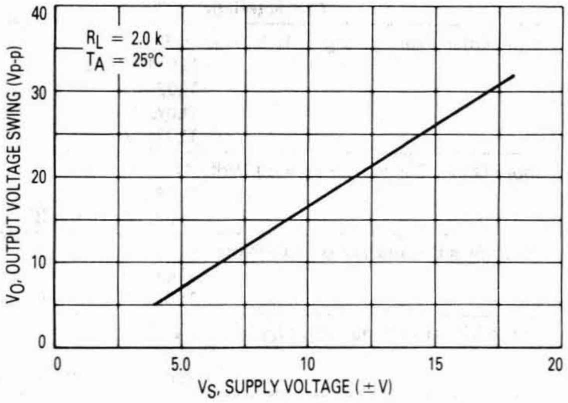


FIGURE 7 — OUTPUT VOLTAGE SWING versus TEMPERATURE

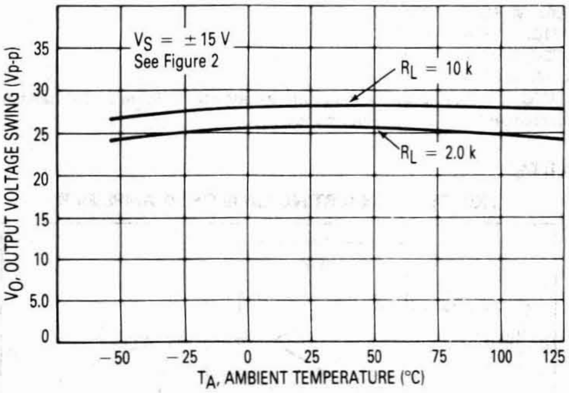


FIGURE 8 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE

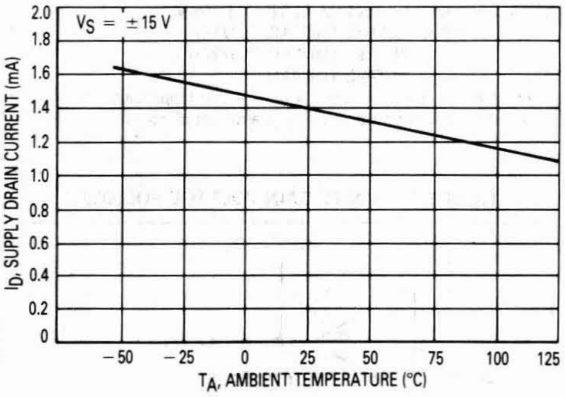


FIGURE 9 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY

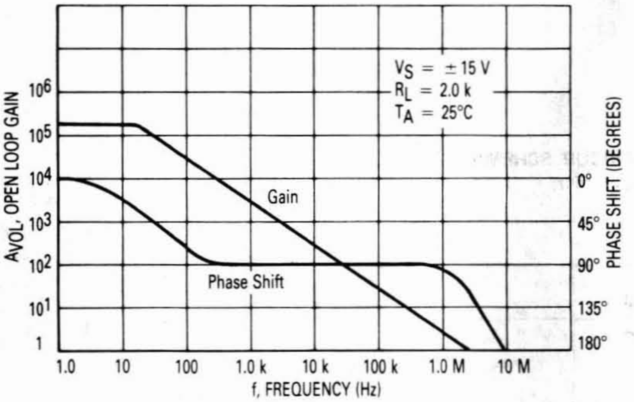


FIGURE 10 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE

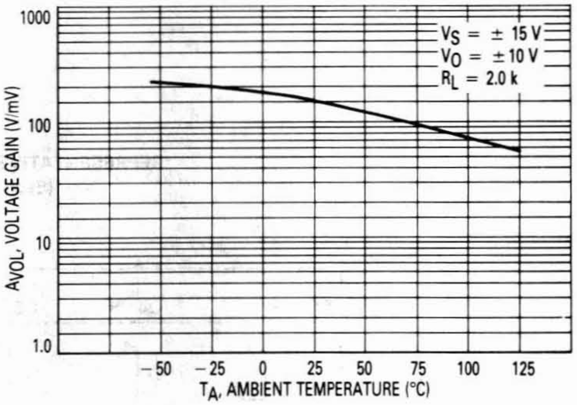


FIGURE 11 — NORMALIZED SLEW RATE versus TEMPERATURE

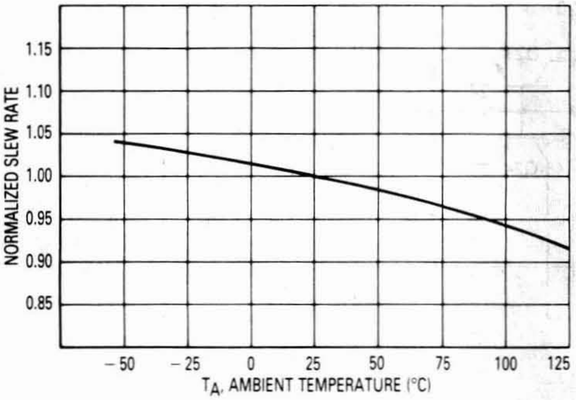


FIGURE 12 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY

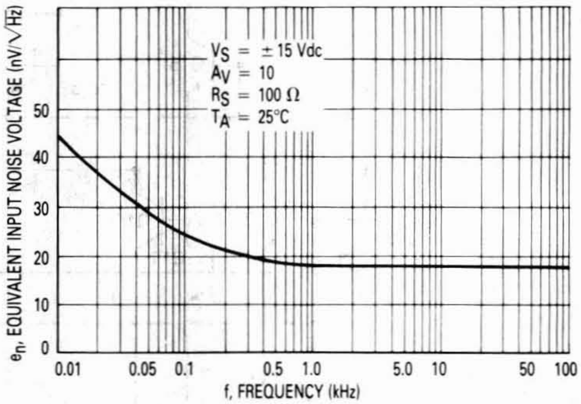
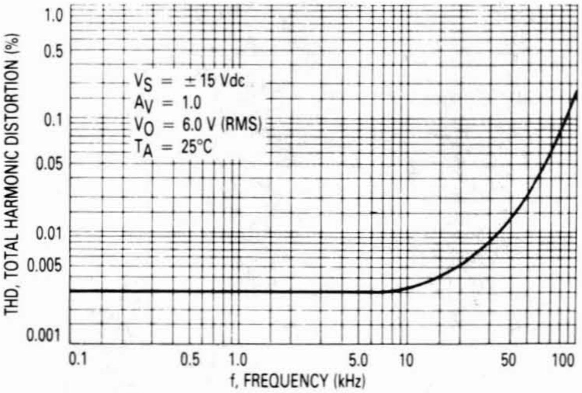


FIGURE 13 — TOTAL HARMONIC DISTORTION versus FREQUENCY



**REPRESENTATIVE CIRCUIT SCHEMATIC**
**(Each Amplifier)**

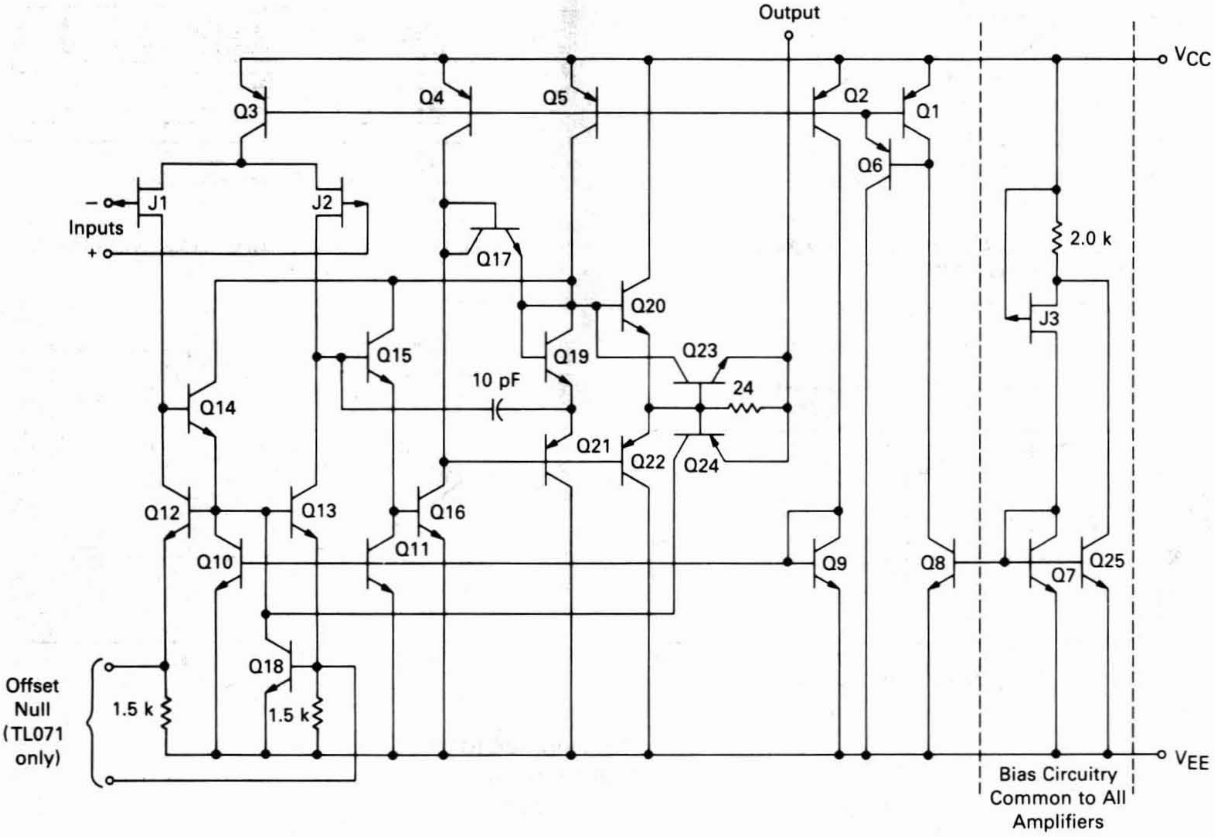
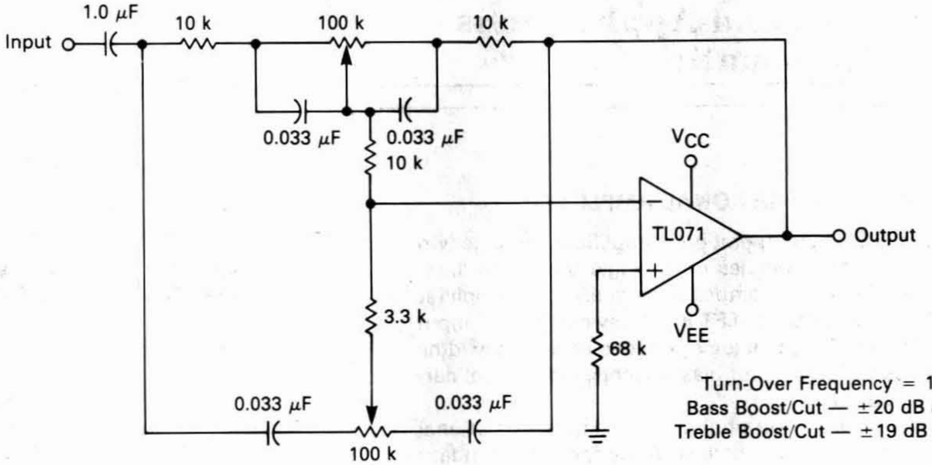
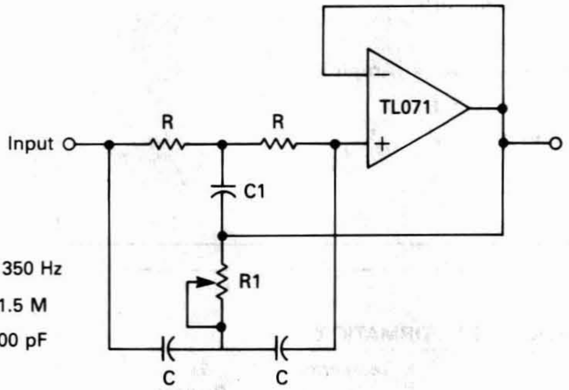

Output
VCC
VEE
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
J1
J2
J3
Inputs
−
+
10 pF
24
2.0 k
1.5 k
1.5 k
Offset Null (TL071 only)
Bias Circuitry Common to All Amplifiers

FIGURE 14 — AUDIO TONE CONTROL AMPLIFIER


1.0 μF
Input
10 k
100 k
10 k
0.033 μF
0.033 μF
10 k
VCC
TL071
Output
3.3 k
VEE
68 k
0.033 μF
0.033 μF
100 k

Turn-Over Frequency = 1.0 kHz
Bass Boost/Cut — ±20 dB at 20 Hz
Treble Boost/Cut — ±19 dB at 20 kHz

FIGURE 15 — HIGH Q NOTCH FILTER


TL071
Input
R
R
C1
R1
C
C

$f_o = \frac{1}{2\pi RC} = 350\text{ Hz}$
$R = 2R1 = 1.5\text{ M}$
$C = \frac{C1}{2} = 300\text{ pF}$

**MOTOROLA**

# TL081
# TL082
# TL084

## Specifications and Applications Information

## JFET-INPUT OPERATIONAL AMPLIFIERS

### SILICON MONOLITHIC INTEGRATED CIRCUITS

### JFET INPUT OPERATIONAL AMPLIFIERS

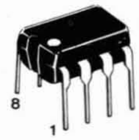
These low-cost JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products. Devices with an "M" suffix are specified over the military operating temperature range of −55°C to +125°C and those with a "C" suffix are specified from 0°C to +70°C.

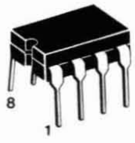
- Input Offset Voltage Options of 3.0, 6.0, and 15 mV Max
- Low Input Bias Current — 30 pA
- Low Input Offset Current — 5.0 pA
- Wide Gain Bandwidth — 3.0 MHz
- High Slew Rate — 13 V/μs
- Low Supply Current — 1.4 mA per Amplifier
- High Input Impedance — $10^{12}$ Ω
- Industry Standard Pinouts

### ORDERING INFORMATION

| Op Amp Function | Device | Temperature Range | Package |
|---|---|---|---|
| Single | TL081ACD, BCD, CD | 0 to +70°C | SO-8 |
| | TL081ACJG, BCJG, CJG | | Ceramic DIP |
| | TL081ACP, BCP, CP | | Plastic DIP |
| | TL081MJG | −55 to +125°C | Ceramic DIP |
| Dual | TL082ACD, BCD, CD | 0 to +70°C | SO-8 |
| | TL082ACJG, BCJG, CJG | | Ceramic DIP |
| | TL082ACP, BCP, CP | | Plastic DIP |
| | TL082MJG | −55 to +125°C | Ceramic DIP |
| Quad | TL084ACD, BCD, CD | 0 to +70°C | SO-14 |
| | TL084ACJ, BCJ, CJ | | Ceramic DIP |
| | TL084ACN, BCN, CN | | Plastic DIP |
| | TL084MJ | −55 to +125°C | Ceramic DIP |

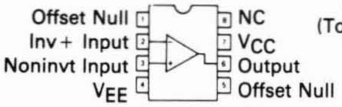


**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

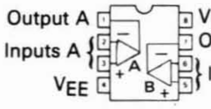


**JG SUFFIX**
CERAMIC PACKAGE
CASE 693-02

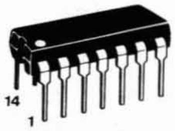
**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8



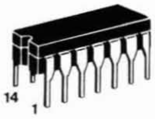
TL081
(Top View)



TL082
(Top View)

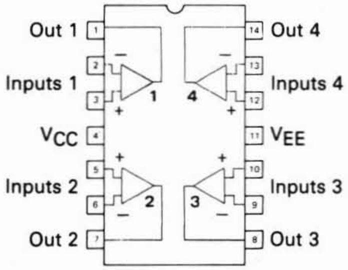


**N SUFFIX**
PLASTIC PACKAGE
CASE 646-05
(TL084 only)



**J SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA
(TL084 only)

**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14



TL084 (Top View)

## MAXIMUM RATINGS

| Rating | Symbol | TL08__M | TL08__C<br>TL08__AC<br>TL08__BC | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>−18 | +18<br>−18 | V |
| Differential Input Voltage | $V_{ID}$ | ±30 | ±30 | V |
| Input Voltage Range (Note 1) | $V_{IDR}$ | ±15 | ±15 | V |
| Output Short-Circuit Duration (Note 2) | $t_S$ | Continuous | | |
| Power Dissipation | | | | |
| Plastic Package (N,P) | $P_D$ | — | 680 | mW |
| Derate above $T_A$ = +47°C | $1/\theta_{JA}$ | — | 10 | mW/°C |
| Ceramic Package (J,JG) | $P_D$ | 680 | 680 | mW |
| Derate above $T_A$ = +82°C | $1/\theta_{JA}$ | 10 | 10 | mW/°C |
| Operating Ambient Temperature Range | $T_A$ | −55 to +125 | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | −65 to +150 | °C |

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 volts, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C unless otherwise noted).

| Characteristic | Symbol | TL08__M | | | TL08__C<br>TL08__AC<br>TL08__BC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage ($R_S$ ≤ 10 k, $V_{CM}$ = 0) | $V_{IO}$ | | | | | | | mV |
| TL081, TL082 | | — | 3.0 | 6.0 | — | 5.0 | 15 | |
| TL084 | | — | 3.0 | 9.0 | — | 5.0 | 15 | |
| TL08__A | | — | — | — | — | 3.0 | 6.0 | |
| TL08__B | | — | — | — | — | 2.0 | 3.0 | |
| Average Temperature Coefficient of Input Offset Voltage $R_S$ = 50 Ω, $T_A$ = $T_{low}$ to $T_{high}$ (Note 3) | $\Delta V_{IO}/\Delta T$ | — | 10 | — | — | 10 | — | μV/°C |
| Input Offset Current ($V_{CM}$ = 0) (Note 4) | $I_{IO}$ | | | | | | | pA |
| TL08__ | | — | 5.0 | 100 | — | 5.0 | 200 | |
| TL08__A, TL08__B | | — | — | — | — | 5.0 | 100 | |
| Input Bias Current ($V_{CM}$ = 0) (Note 4) | $I_{IB}$ | | | | | | | pA |
| TL08__ | | — | 30 | 200 | — | 30 | 400 | |
| TL08__A, TL08__B | | — | — | — | — | 30 | 200 | |
| Input Resistance | $r_i$ | — | $10^{12}$ | — | — | $10^{12}$ | — | Ω |
| Common Mode Input Voltage Range | $V_{ICR}$ | | | | | | | V |
| TL08__ | | ±11 | +15, −12 | — | ±10 | +15, −12 | — | |
| TL08__A, TL08__B | | — | — | — | ±11 | +15, −12 | — | |
| Large-Signal Voltage Gain ($V_O$ = ±10 V, $R_L$≥2.0 k) | $A_{VOL}$ | | | | | | | V/mV |
| TL08__ | | 25 | 150 | — | 25 | 150 | — | |
| TL08__A, TL08__B | | — | — | — | 50 | 150 | — | |
| Output Voltage Swing (Peak-to-Peak) $R_L$ = 10 k | $V_O$ | 24 | 28 | — | 24 | 28 | — | V |
| Common Mode Rejection Ratio ($R_S$≤10 k) | CMRR | | | | | | | dB |
| TL08__ | | 80 | 100 | — | 70 | 100 | — | |
| TL08__A, TL08__B | | — | — | — | 80 | 100 | — | |
| Supply Voltage Rejection Ratio ($R_S$≤10 k) | PSRR | | | | | | | dB |
| TL08__ | | 80 | 100 | — | 70 | 100 | — | |
| TL08__A, TL08__B | | — | — | — | 80 | 100 | — | |
| Supply Current (Each Amplifier) | $I_D$ | — | 1.4 | 2.8 | — | 1.4 | 2.8 | mA |
| Unity Gain Bandwidth | BW | — | 4.0 | — | — | 4.0 | — | MHz |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C unless otherwise noted).

| Characteristic | Symbol | TL08__M |  |  | TL08__C<br>TL08__AC<br>TL08__BC |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Slew Rate (See Figure 1)<br>$V_{in}$ = 10 V, $R_L$ = 2.0 k, $C_L$ = 100 pF | SR | 8.0 | 13 | — | — | 13 | — | V/μs |
| Rise Time (See Figure 1) | $t_r$ | — | 0.1 | — | — | 0.1 | — | μs |
| Overshoot Factor<br>$V_{in}$ = 20 mV, $R_L$ = 2.0 k, $C_L$ = 100 pF | — | — | 10 | — | — | 10 | — | % |
| Equivalent Input Noise Voltage<br>$R_S$ = 100 Ω, f = 1000 Hz | $e_n$ | — | 25 | — | — | 25 | — | nV/√Hz |
| Channel Separation<br>$A_V$ = 100 | — | — | 120 | — | — | 120 | — | dB |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = $T_{low}$ to $T_{high}$ [Note 3].)

| Characteristic | Symbol | TL08__M |  |  | TL08__C<br>TL08__AC<br>TL08__BC |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage ($R_S$ ≤10 k, $V_{CM}$ = 0) | $V_{IO}$ |  |  |  |  |  |  | mV |
| TL081, TL082 |  | — | — | 9.0 | — | — | 20 |  |
| TL084 |  | — | — | 15 | — | — | 20 |  |
| TL08__A |  | — | — | — | — | — | 7.5 |  |
| TL08__B |  | — | — | — | — | — | 5.0 |  |
| Input Offset Current ($V_{CM}$ = 0) (Note 4) | $I_{IO}$ |  |  |  |  |  |  | nA |
| TL08__ |  | — | — | 20 | — | — | 5.0 |  |
| TL08__A, TL08__B |  | — | — | — | — | — | 3.0 |  |
| Input Bias Current ($V_{CM}$ = 0) (Note 4) | $I_{IB}$ |  |  |  |  |  |  | nA |
| TL08__ |  | — | — | 50 | — | — | 10 |  |
| TL08__A, TL08__B |  | — | — | — | — | — | 7.0 |  |
| Large-Signal Voltage Gain ($V_O$ = ±10 V, $R_L$≥2.0 k) | $A_{VOL}$ |  |  |  |  |  |  | V/mV |
| TL08__ |  | 15 | — | — | 15 | — | — |  |
| TL08__A, TL08__B |  | — | — | — | 25 | — | — |  |
| Output Voltage Swing (Peak-to-Peak) | $V_O$ |  |  |  |  |  |  | V |
| ($R_L$≥10 k) |  | 24 | — | — | 24 | — | — |  |
| ($R_L$≥2.0 k) |  | 20 | — | — | 20 | — | — |  |

NOTES (continued):

3. $T_{low}$ = −55°C for TL081M, TL082M, TL084M
   = 0°C for TL081C, TL081AC, TL081BC
   TL082C, TL082AC, TL082BC
   TL084C, TL084AC, TL084BC

   $T_{high}$ = +125°C for TL081M, TL082M, TL084M
   = +70°C for TL081C, TL081AC, TL081BC
   TL082C, TL082AC, TL082BC
   TL084C, TL084AC, TL084BC
4. Input Bias currents of JFET input Op Amps approximately double for every 10°C rise in junction temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during test.

## TEST CIRCUITS

FIGURE 1 — UNITY GAIN VOLTAGE FOLLOWER

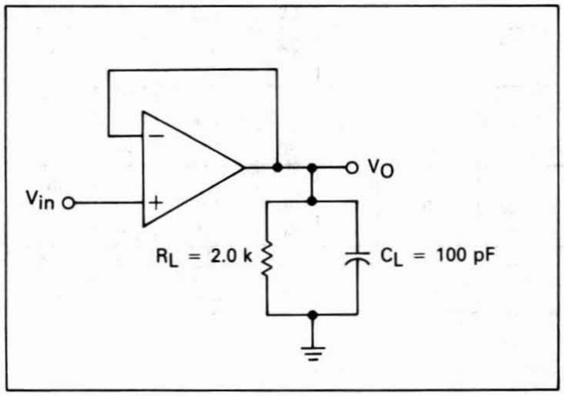


FIGURE 2 — INVERTING GAIN OF 10 AMPLIFIER

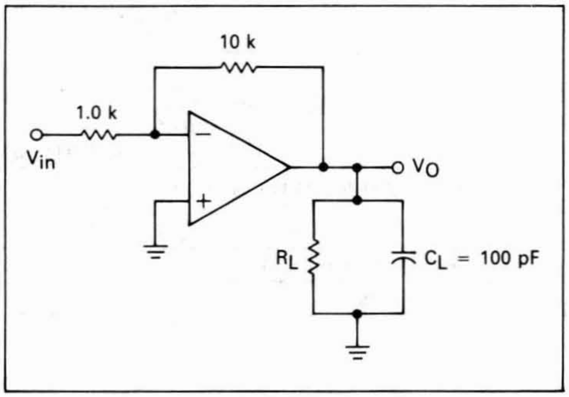


**FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE**

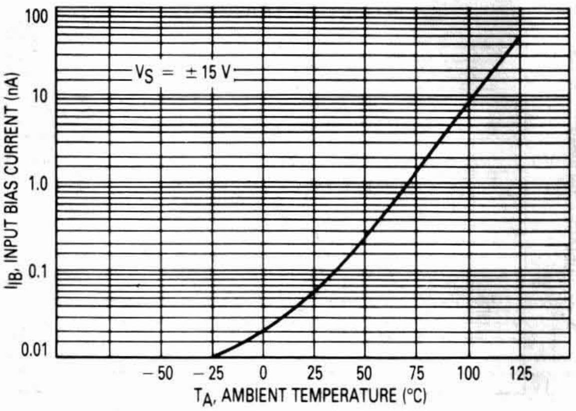


**FIGURE 4 — OUTPUT VOLTAGE SWING versus FREQUENCY**

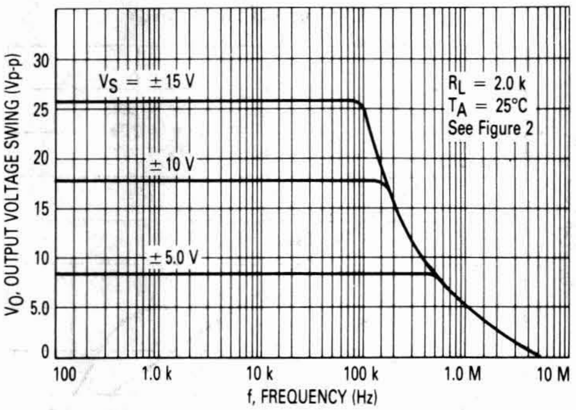


**FIGURE 5 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE**

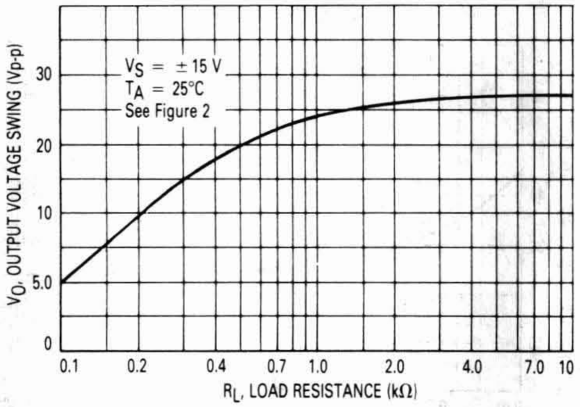


**FIGURE 6 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE**

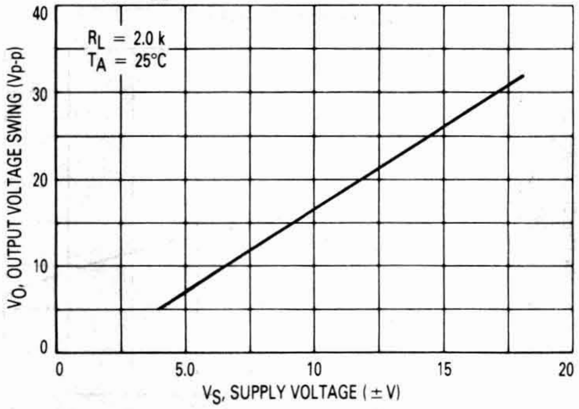


**FIGURE 7 — OUTPUT VOLTAGE SWING versus TEMPERATURE**

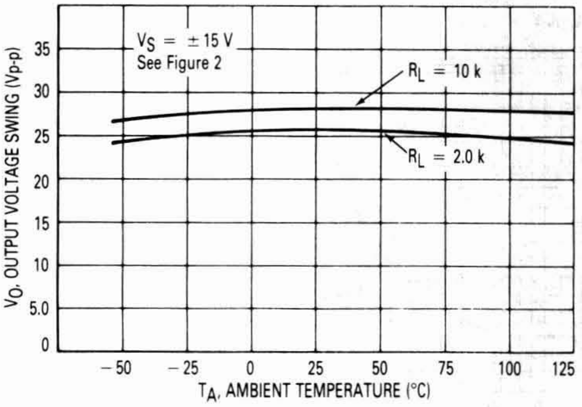


**FIGURE 8 — SUPPLY CURRENT PER AMPLIFIER versus TEMPERATURE**

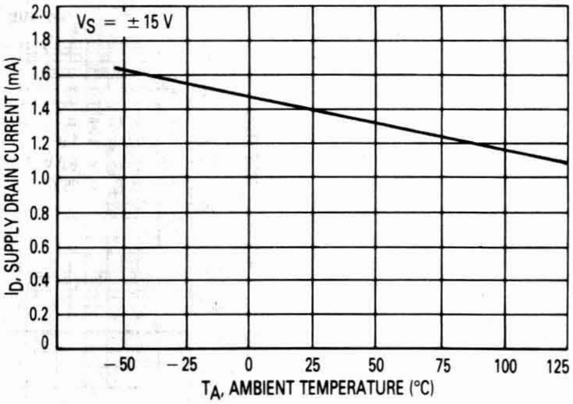


**FIGURE 9 — LARGE-SIGNAL VOLTAGE GAIN AND PHASE SHIFT versus FREQUENCY**

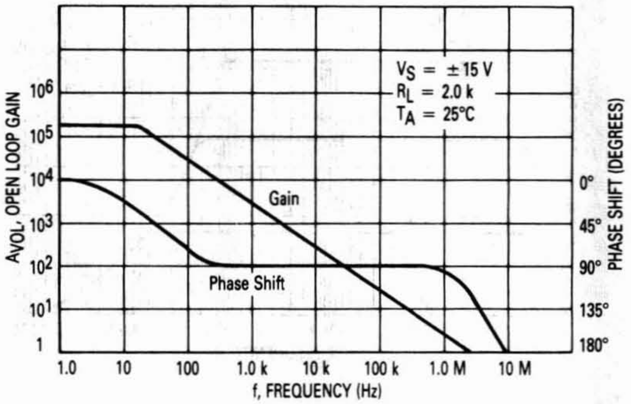


**FIGURE 10 — LARGE-SIGNAL VOLTAGE GAIN versus TEMPERATURE**

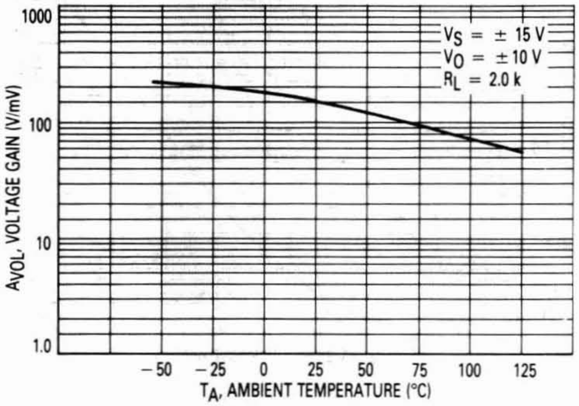


**FIGURE 11 — NORMALIZED SLEW RATE versus TEMPERATURE**

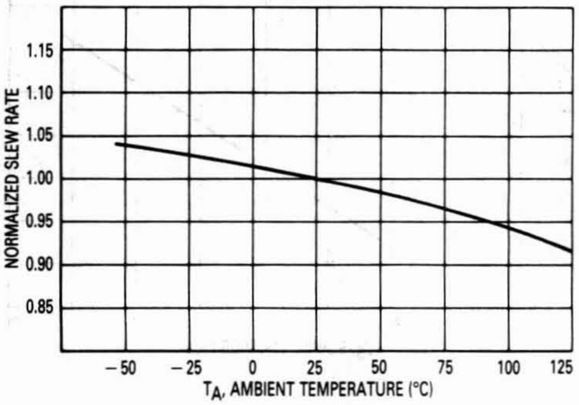


**FIGURE 12 — EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY**

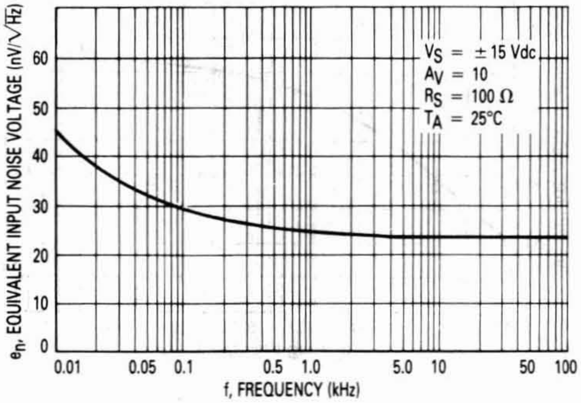
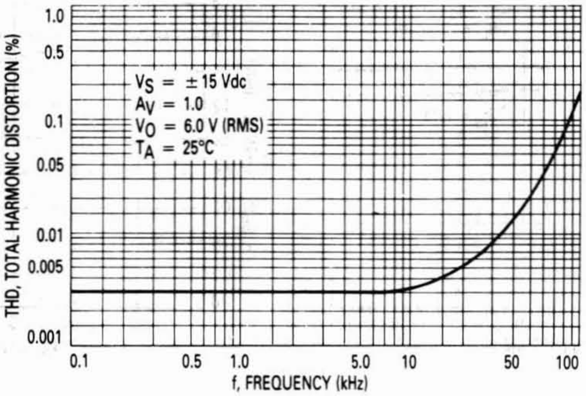
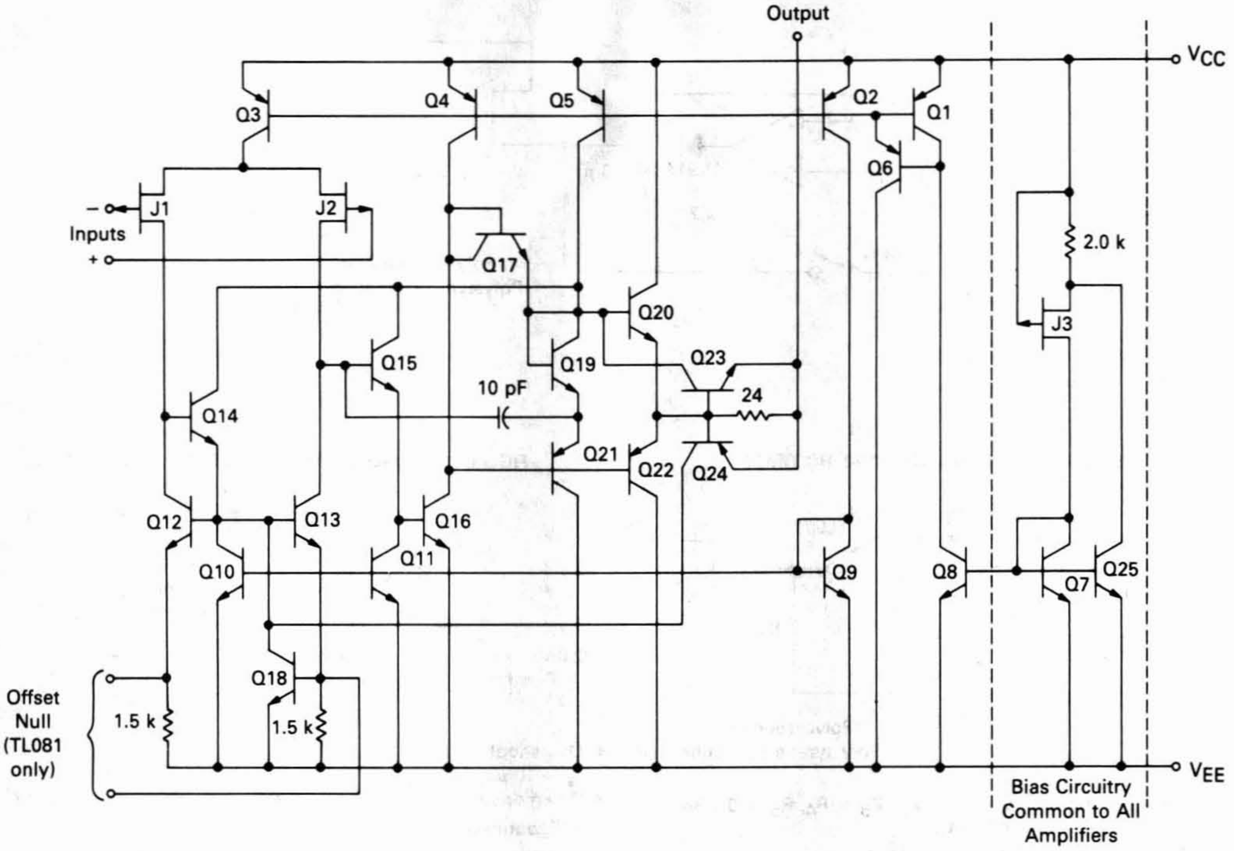


**FIGURE 13 — TOTAL HARMONIC DISTORTION versus FREQUENCY**

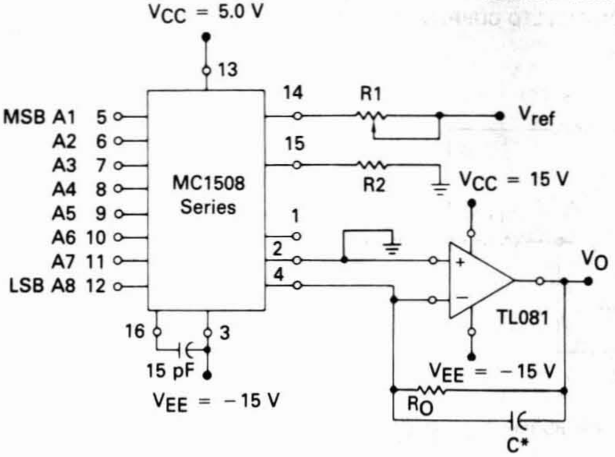


REPRESENTATIVE CIRCUIT SCHEMATIC
(Each Amplifier)


Output
VCC
Q3
Q4
Q5
Q2
Q1
Q6
J1
J2
Inputs
−
+
Q17
2.0 k
J3
Q20
Q15
Q19
Q23
10 pF
24
Q14
Q21
Q22
Q24
Q12
Q13
Q16
Q10
Q11
Q9
Q8
Q7
Q25
Q18
Offset Null (TL081 only)
1.5 k
1.5 k
VEE
Bias Circuitry Common to All Amplifiers

## TYPICAL APPLICATIONS

FIGURE 14 — OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER


VCC = 5.0 V
13
14
R1
Vref
15
R2
VCC = 15 V
MSB A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
LSB A8 12
MC1508 Series
1
2
4
+
−
VO
TL081
16
3
15 pF
VEE = −15 V
VEE = −15 V
RO
C*

Settling time to within ½ LSB (± 19.5 mV) is approximately 4.0 µs from the time all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical $V_O$

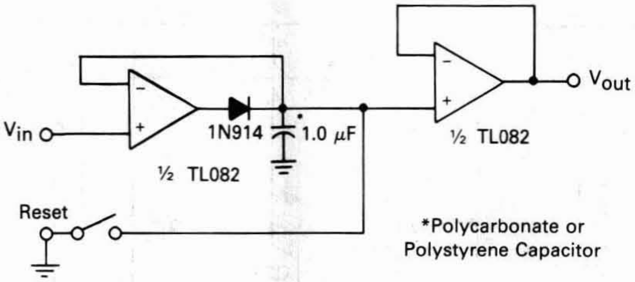
$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust $V_{ref}$, R1 or $R_O$ so that $V_O$ with all digital inputs at high level is equal to 9.961 volts.

$$V_{ref} = 2.0\ \text{Vdc}$$
$$R_1 = R2 \approx 1.0\ \text{k}\Omega$$
$$R_O = 5.0\ \text{k}\Omega$$

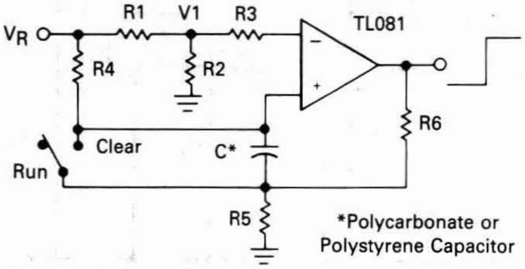
$$V_O = \frac{2.0\ \text{V}}{1.0\ \text{k}}(5.0\ \text{k})\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$
$$= 10\ \text{V}\left[\frac{255}{256}\right] = 9.961\ \text{V}$$

FIGURE 15 — POSITIVE PEAK DETECTOR


Vin
½ TL082
1N914
1.0 µF
*
Reset
½ TL082
Vout

*Polycarbonate or Polystyrene Capacitor

FIGURE 16 — LONG INTERVAL RC TIMER


VR
R1
V1
R3
R4
R2
TL081
R6
Clear
Run
C*
R5

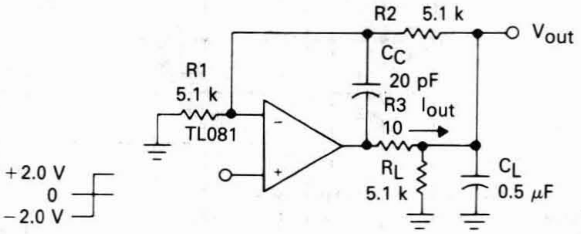
*Polycarbonate or Polystyrene Capacitor

Time (t) = R4 $C\ell n\ (V_R/V_R - V_1)$, $R_3 = R_4$, $R_5 = 0.1\ R6$
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer

$V_R$ = 10 V    C = 1.0 µF    R3 = R4 = 144 M
R6 = 20 k    R5 = 2.0 k    R1 = R2 = 1.0 k

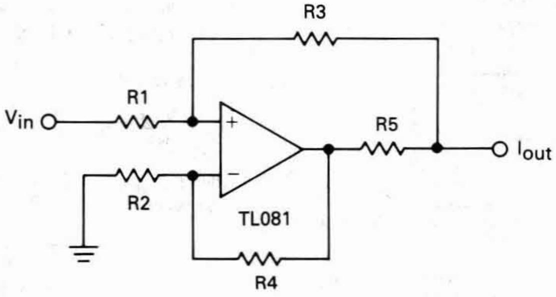
FIGURE 17 — ISOLATING LARGE CAPACITIVE LOADS


R2 5.1 k
Vout
R1
5.1 k
CC
20 pF
R3 Iout
10
TL081
RL
5.1 k
CL
0.5 µF
+2.0 V
0
−2.0 V

- Overshoot < 10%
- $t_s$ = 10 µs
- When driving large $C_L$, the $V_{out}$ slew rate is determined by $C_L$ and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \cong \frac{0.02}{0.5}\ \text{V}/\mu\text{s} = 0.04\ \text{V}/\mu\text{s (with } C_L \text{ shown)}$$

FIGURE 18 — VOLTAGE CONTROLLED CURRENT SOURCE


R3
R1
Vin
R5
Iout
R2
TL081
R4

If R1 through R4 >> R5 then $I_{out} = \frac{V_{in}}{R5}$

**MOTOROLA**

# AD562A

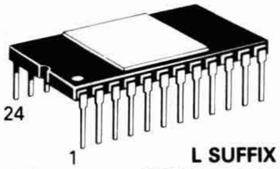
## HIGH-SPEED 12-BIT MULTIPLYING D/A CONVERTER

The improved AD562A is a monolithic 12-bit D/A converter. Active laser trimming of thin-film ladder network, span and bipolar offset resistors at wafer level provide linearity of better than ±1/2 LSB. An innovative bit switching scheme provides fast settling time yet enables selection of CMOS or TTL thresholds which are retained over a wide $V_{CC}$ range from 4.5 to 16.5 volts. Internal precision span resistors allow output voltage options of 0 to 5.0 V, 0 to 10 V, ±2.5 V, ±5.0 V, and ±10 V. The AD562A multiplies in two quadrants when varying the reference input voltage. 12-bit accuracy and fast settling time make this converter ideal for applications such as fast A/D converters, CRT display generation waveform synthesis, precision instruments, data acquisition, and robotics systems.

- True 12-Bit Linearity: ±1/2 LSB Max
- Fast Settling Time: ±1/2 LSB in 400 ns Max
- Fully Monotonic Over Temperature Range
- Low Gain Drift: 5 ppm/°C Max (AD562ASL)
- Binary Coded Inputs
- Selectable Digital Thresholds
- Internal Span Resistors for Generating Output Voltage
- Low Power Consumption: 210 mW

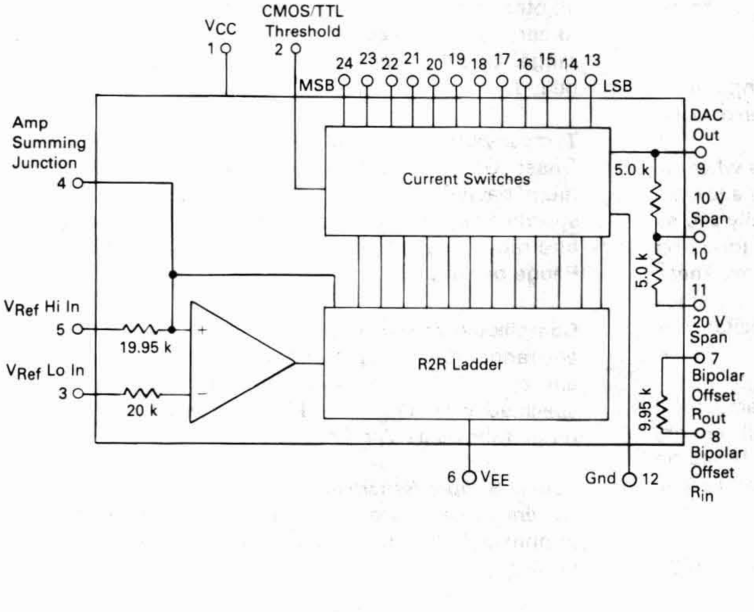
## LASER TRIMMED HIGH-SPEED 12-BIT MULTIPLYING D/A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

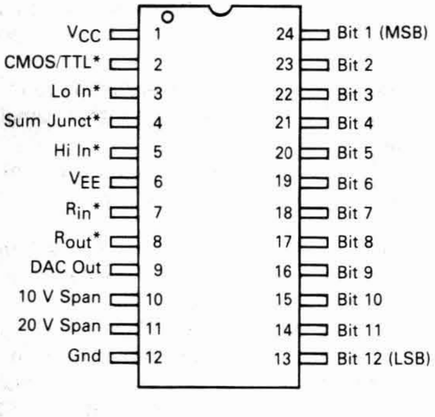


L SUFFIX
CERAMIC PACKAGE
CASE 716-06

### BLOCK DIAGRAM


VCC
1
CMOS/TTL Threshold
2
24 23 22 21 20 19 18 17 16 15 14 13
MSB
LSB
Amp Summing Junction
4
Current Switches
DAC Out
9
5.0 k
10 V Span
10
5.0 k
11
20 V Span
VRef Hi In
5
19.95 k
VRef Lo In
3
20 k
R2R Ladder
7
Bipolar Offset Rout
9.95 k
8
Bipolar Offset Rin
6 VEE
Gnd 12

### PIN CONNECTIONS


VCC 1
CMOS/TTL* 2
Lo In* 3
Sum Junct* 4
Hi In* 5
VEE 6
Rin* 7
Rout* 8
DAC Out 9
10 V Span 10
20 V Span 11
Gnd 12
24 Bit 1 (MSB)
23 Bit 2
22 Bit 3
21 Bit 4
20 Bit 5
19 Bit 6
18 Bit 7
17 Bit 8
16 Bit 9
15 Bit 10
14 Bit 11
13 Bit 12 (LSB)

* Pin 2 = CMOS/TTL Threshold
Pin 3 = $V_{Ref}$ Lo In
Pin 4 = Amp Summing Junction
Pin 5 = $V_{Ref}$ Hi In
Pin 7 = Bipolar Offset $R_{in}$
Pin 8 = Bipolar Offset $R_{out}$

### ORDERING INFORMATION

| Device | Temperature Range | Accuracy @ 25°C |
|---|---|---|
| AD562AKL | 0°C to +70°C | ±1/2 LSB |
| AD562ASL | −55°C to +125°C | ±1/4 LSB |

**MAXIMUM RATING** ($T_A$ = 25°C, Ratings are referred to Ground [Pin 12] unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>−18 | Vdc |
| Digital Input Voltage (Pins 13 to 24) | $V_I$ | −5.0 to +18 | Vdc |
| CMOS/TTL Threshold Select (Pin 2) | — | 0 to $V_{CC}$ | Vdc |
| $V_{Ref}$ Hi In (Pin 5) | — | $V_{EE}$ to $V_{CC}$ | Vdc |
| $V_{Ref}$ Lo In (Pin 3) | — | ±1.0 | Vdc |
| Applied Output Voltage (Pin 9) | $V_O$ | −7.0 to $V_{CC}$ | Vdc |
| Bipolar Offset to Analog Ground (Pin 7 or 8) | — | $V_{EE}$ to $V_{CC}$ | Vdc |
| Ten Volt Span Resistor to Analog Ground (Pin 10) | — | $V_{EE}$ to $V_{CC}$ | Vdc |
| Twenty Volt Span Resistor to Analog Ground (Pin 11) | — | $V_{EE}$ to $V_{CC}$ | Vdc |
| Power Dissipation | $P_D$ | 1000 | mW |
| Operating Temperature Range AD562AKL<br>AD562ASL | $T_A$ | 0 to +70<br>−55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature | $T_J$ | +175 | °C |

## TERMINOLOGY

**Nonlinearity** (Relative Accuracy) — Maximum output deviation from ideal straight line connecting zero and full-scale readings, expressed as a fraction of LSB or percent of full scale.

**Differential Nonlinearity** — Maximum deviation in the readings of any two adjacent input bit codes from the ideal LSB step, expressed in fractions of LSB or percentage of full scale. A differential nonlinearity value greater than 1 LSB may lead to nonmonotonic operation.

**Monotonicity** — For every increase in the input digital word, the output current either remains the same or increases.

The complete AD562A Series is guaranteed to be monotonic over temperature.

**Settling Time** — The elapsed time from the input transition until the output has settled within an error band about its final value.

The worst case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 200 ns for the output to settle to within ±1/2 LSB for 12-bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small (<0.5 V) swing and the external output capacitance is under 10 pF.

**Gain Error** — The difference between the actual full scale range (difference in output between all bits on, and all bits off) and the ideal full scale range. Based on a 0 to 10 V output configuration, the ideal FSR is $\frac{4095}{4096} \times 10 = 9.99756$ V.

Gain error is expressed in percentage of full scale (FS).

**Unipolar Offset Error** — Using the configuration shown in Figure 1, with R1 = 50 ohms and with all bits off, the output voltage reading compared to zero is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

**Bipolar Offset Error** — Using the configuration shown in Figure 2, with R2 = 50 ohms with all bits off, the output voltage reading compared to the ideal negative full scale value is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

**Bipolar Zero Error** — Using the configuration shown in Figure 2, with R1 = R2 = 50 Ω, with the MSB on and all other bits off, the output voltage reading compared to zero is expressed as a percentage of the full-scale range. Offset voltage of the output op amp must be nulled.

**Temperature Coefficients** — (Unipolar Offset, Bipolar Offset, Gain and Differential Nonlinearity). The maximum deviation of the particular parameter over the specified temperature range, divided by the temperature range, expressed in parts per million of Full Scale Range per degree C.

**Compliance Voltage Range** — The output terminal voltage range which will provide specified output resistance and current characteristics. The compliance voltage is specified with $V_{EE}$ = −15. The compliance voltage range follows as $V_{EE}$ is varied.

**Power Supply Sensitivity** — The change in full scale current caused by a change in $V_{EE}$ or $V_{CC}$ expressed in ppm of full scale current per percent change in $V_{EE}$ or $V_{CC}$.

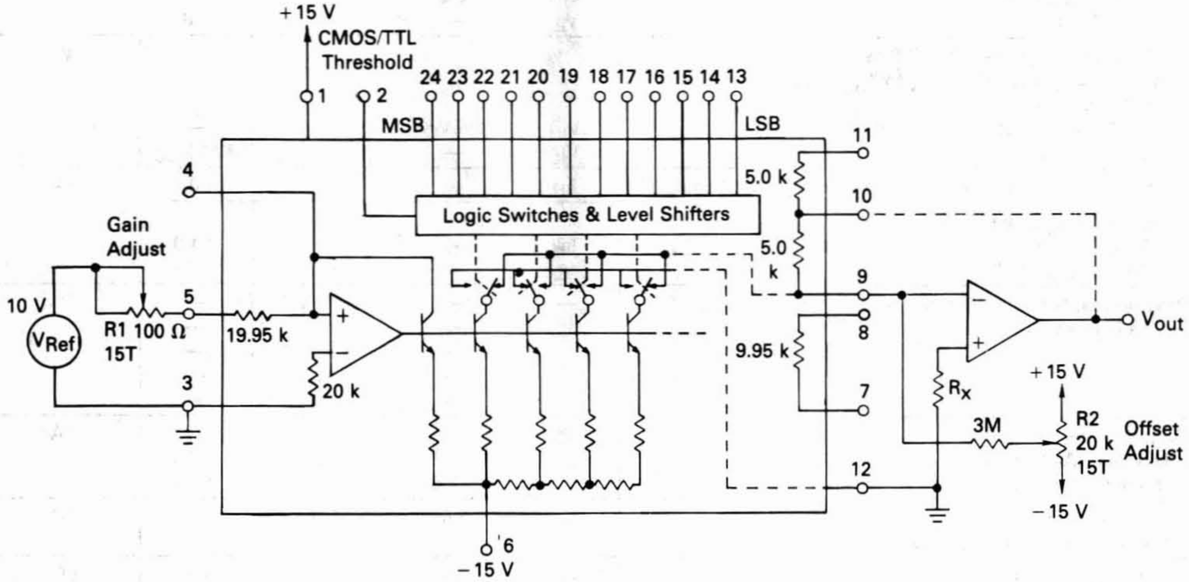
**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $V_{Ref}$ = 10 V, Pin 2 open, $T_A$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TTL Digital Logic Levels (All Bits) | | | | | V |
| (4.5 V ≤ $V_{CC}$ ≤ 16.5 V, $T_{low}$ to $T_{high}$, see Note 1) | | | | | |
| Bit On, Logic "1" | $V_{IH}$ | 2.0 | — | — | |
| Bit Off, Logic "0" | $V_{IL}$ | — | — | 0.8 | |
| CMOS Digital Logic Levels (All Pins) | | | | | V |
| (4.5 V ≤ $V_{CC}$ ≤ 16.5 V, $T_{low}$ to $T_{high}$, see Note 1, Pin 2 tied to Pin 1) | | | | | |
| Bit On, Logic "1" | $V_{IH}$ | 70% $V_{CC}$ | — | — | |
| Bit Off, Logic "0" | $V_{IL}$ | — | — | 30% $V_{CC}$ | |
| Digital Input Current, CMOS/TTL Levels — Bit On, Logic "1" | $I_{IH}$ | — | +0.02 | +0.1 | µA |
| ($T_{low}$ to $T_{high}$, see Note 1) | | | | | |
| Bit On, Logic "1" | $I_{IH}$ | — | — | +1.0 | |
| Bit Off, Logic "0" | $I_{IL}$ | — | −2.0 | −75 | |
| Programmable Output Range (See Figures 1 and 2) | — | — | 0 to +5.0 | — | V |
| | | — | −2.5 to +2.5 | — | |
| | | — | 0 to +10 | — | |
| | | — | −5.0 to +5.0 | — | |
| | | — | −10 to +10 | — | |
| Output Current | $I_O$ | | | | mA |
| Unipolar (All Bits On) | | −1.6 | −2.0 | −2.4 | |
| Bipolar (All Bits On or Off) | | ±0.8 | ±1.0 | ±1.2 | |
| Output Resistance (Exclusive of Span Resistors) | $R_O$ | 1.0 | 5.0 | — | MΩ |
| Output Capacitance | $C_O$ | — | 25 | — | pF |
| Output Compliance Voltage Range ($T_{low}$ to $T_{high}$, see Note 1) | $V_{OC}$ | −5.0 | — | +10 | V |
| Nonlinearity AD562AKL | NL | — | ±1/4 | ±1/2 | LSB |
| AD562ASL | | — | ±1/8 | ±1/4 | |
| Nonlinearity ($T_{low}$ to $T_{high}$, see Note 1) | NL | — | — | ±1.0 | LSB |
| Differential Nonlinearity | — | — | — | ±1/2 | LSB |
| Differential Nonlinearity ($T_{low}$ to $T_{high}$, see Note 1) | Monotonicity Guaranteed | | | | |
| Gain Error — Figure 1, R1 = Fixed 50 Ω | — | — | ±0.05 | ±0.15 | % of FS |
| Offset Error | — | | | | % of FS |
| Unipolar — Figure 1 | | — | ±0.01 | ±0.05 | |
| Bipolar — Figure 2, R2 = Fixed 50 Ω | | — | ±0.05 | ±0.15 | |
| Bipolar Zero Error — Figure 2, R1 = R2 = Fixed 50 Ω | — | — | ±0.05 | ±0.15 | % of FS |
| Gain Adjustment Range — Figure 1 | — | ±0.20 | ±0.25 | — | % of FS |
| Bipolar Offset Adjustment Range — Figure 2 | — | ±0.20 | ±0.25 | — | % of FS |
| Temperature Coefficients ($T_{low}$ to $T_{high}$, see Note 1) | — | | | | ppm/°C |
| Unipolar Zero | | — | 0.2 | 2.0 | |
| Bipolar Zero | | — | 1.0 | 4.0 | |
| Gain — AD562AKL | | — | 4.0 | 10 | |
| — AD562ASL | | — | 2.0 | 5.0 | |
| Differential Nonlinearity | | — | 1.0 | — | |
| Settling Time to 1/2 LSB (see Note 2) All Bits On-to-Off or Off-to-On | $t_s$ | — | 200 | 400 | ns |
| Reference Input Impedance | $Z_{in}$ | 15 | 20 | 25 | kΩ |
| Power Supply Current | | | | | mA |
| ($V_{CC}$ +4.5 to +16.5 Vdc) | $I_{CC}$ | — | 6.0 | 10 | |
| ($V_{EE}$ −10.8 to −16.5 Vdc) | $I_{EE}$ | — | −8.0 | −12 | |
| Power Supply Gain Sensitivity | | | | | ppm of FS/% |
| ($V_{CC}$ +4.5 to 5.5 Vdc) | $PSSI_{FS+}$ | — | — | 2.0 | |
| ($V_{CC}$ +13.5 to +16.5 Vdc) | $PSSI_{FS+}$ | — | — | 2.0 | |
| ($V_{EE}$ −10.8 to −16.5 Vdc) | $PSSI_{FS-}$ | — | — | 6.0 | |

NOTES 1: $T_{low}$ = −55°C for AD562ASL $T_{high}$ = +125°C for AD562ASL
0°C for AD562AKL +70°C for AD562AKL

2: For optimum settling time, case lid should be connected to a low noise ground.

FIGURE 1 — AD562A IN TYPICAL UNIPOLAR CONNECTION SCHEME


+15 V
CMOS/TTL Threshold
1
2
24 23 22 21 20 19 18 17 16 15 14 13
MSB
LSB
4
Gain Adjust
10 V
$V_{Ref}$
R1 100 Ω 15T
5
3
19.95 k
20 k
Logic Switches & Level Shifters
11
5.0 k
10
5.0 k
9
8
9.95 k
7
12
6
−15 V
$V_{out}$
$R_X$
3M
+15 V
R2 20 k 15T
Offset Adjust
−15 V

## UNIPOLAR DAC OPERATION

A typical circuit configuration for unipolar operation of AD562A is shown in Figure 1.

**Step 1 — Output Range**

Determine which output range is required. For +5.0 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier output and short Pin 9 to Pin 11. For +10 Volt FS range, connect Pin 10 to external operational amplifier output, Pin 11 remains unconnected.

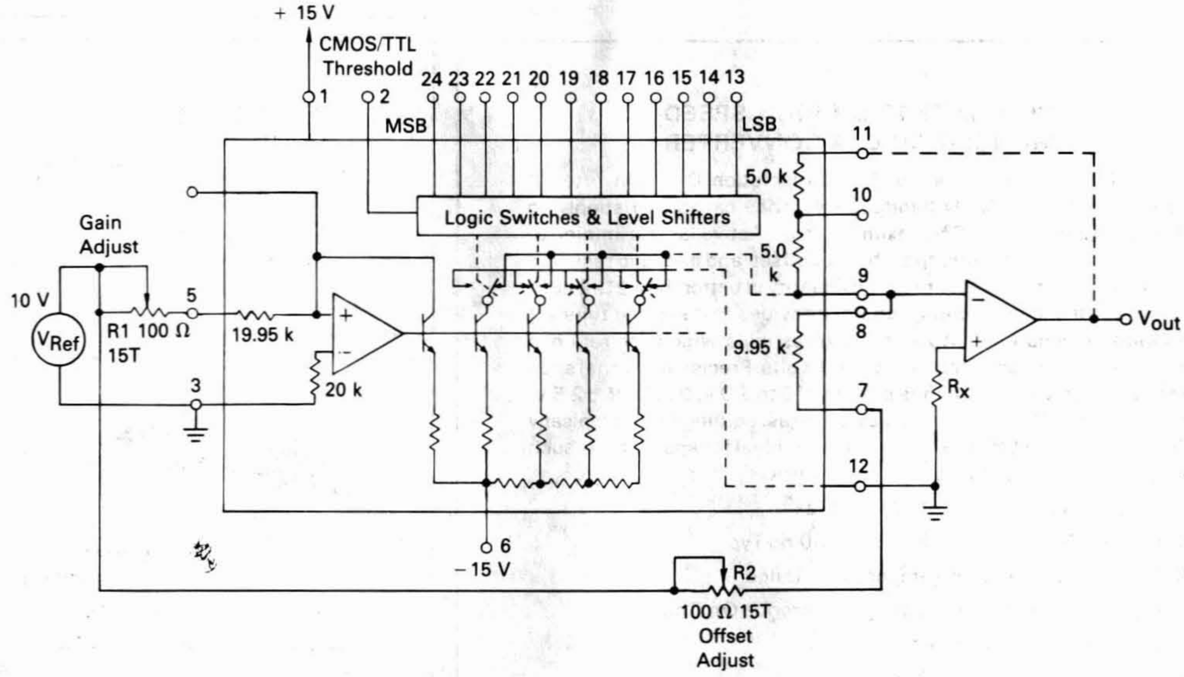
**Step 2 — Zero Adjust**

Turn all bits OFF and adjust R2 until external operational amplifier output is 0 Volts.

**Step 3 — Gain Adjust**

Turn all bits ON. Adjust R1 until operational amplifier output reaches 4.9988 Volts for +5.0 Volt range or 9.9976 for +10 Volt range.

FIGURE 2 — AD562A IN TYPICAL BIPOLAR CONNECTION SCHEME


+ 15 V
CMOS/TTL
Threshold
24 23 22 21 20 19 18 17 16 15 14 13
1
2
MSB
LSB
11
5.0 k
10
Logic Switches & Level Shifters
Gain
Adjust
5.0
k
10 V
9
5
$V_{Ref}$
R1 100 Ω
15T
19.95 k
8
$V_{out}$
9.95 k
3
20 k
7
$R_X$
12
6
−15 V
R2
100 Ω 15T
Offset
Adjust

## BIPOLAR DAC OPERATION

A typical circuit configuration for bipolar operation of AD562A is shown in Figure 2.

**Step 1 — Output Range**

Determine which output range is required. For ±2.5 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier and short Pin 9 to Pin 11. For ±5.0 Volt FS range, connect Pin 10 to output of external operational amplifier, Pin 11 remains unconnected. For ±10 Volt FS range, connect Pin 11 to output of external operational amplifier, Pin 10 remains unconnected.

**Step 2 — Offset Adjust**

Turn all bits OFF and adjust R2 until operational amplifier output is:

−2.5000 Volt for ±2.5 Volt range
−5.0000 Volt for ±5.0 Volt range
−10.0000 Volt for ±10 Volt range

**Step 3 — Gain Adjust (Bipolar Zero)**

Turn MSB ON and all other bits OFF. Adjust R1 until operational amplifier output is 0 Volts.

**NOTES:**

1. For TTL and DTL compatibility, leave Pin 2 open.
2. For high voltage CMOS compatibility, short Pin 2 to Pin 1.
3. Supplies should be bypassed with 0.1 μF capacitors.
4. In unipolar operation, $R_X$ should be made equal to the internal feedback resistor. In bipolar, $R_X$, equals the feedback resistor in parallel with 10 k.

# AD563

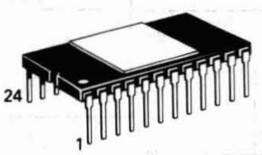
## COMPLETE 12-BIT HIGH-SPEED MONOLITHIC D/A CONVERTER

The AD563 is a monolithic 12-bit resolution D/A converter. It contains a high stability bandgap reference capable of supplying 5.0 mA trimmed to ±1.0% maximum error. Active laser trimming of thin-film ladder network, span, bipolar offset, and bandgap resistors at wafer level provide accuracy and linearity of better than ±1/2 LSB. An innovative bit switching scheme provides fast settling time yet enables selection of CMOS or TTL thresholds which are retained over a wide $V_{CC}$ range from 4.5 to 16.5 volts. Precision internal span resistors allow output voltage options of 0 to 5.0 V, 0 to 10 V, ±2.5 V, ±5.0 V, and ±10 V. 12-bit accuracy and a fast settling time of typically 200 ns (to ±1/2 LSB) make this converter ideal for applications such as a fast A/D building block or display driver.

- True 12-Bit Linearity: ±1/2 LSB Max
- Fast Settling Time: ±1/2 LSB in 200 ns Typ
- Fully Monotonic Over Temperature Range
- High-Stability Bandgap Voltage Reference On Chip
- True Binary Coded Inputs
- Selectable Digital Thresholds
- Internal Span Resistors for Generating Output Voltage
- Low Power Consumption: 210 mW
- Low Cost Monolithic Design

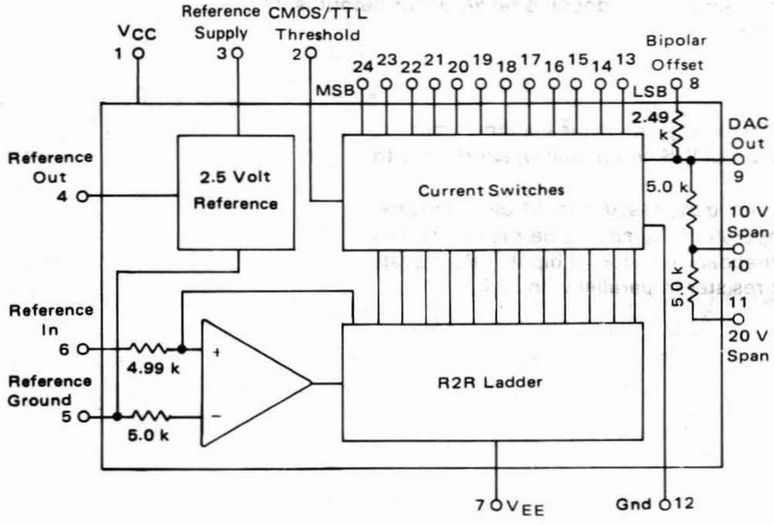
## LASER TRIMMED HIGH-SPEED 12-BIT D/A CONVERTER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

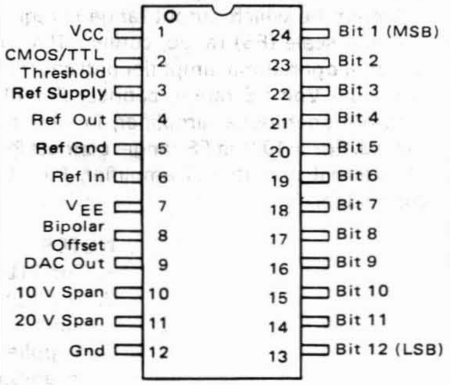


**L SUFFIX**
CERAMIC PACKAGE
CASE 716-06

### BLOCK DIAGRAM


VCC
1
Reference Supply
3
CMOS/TTL Threshold
2
24 23 22 21 20 19 18 17 16 15 14 13
MSB
LSB
Bipolar Offset
8
2.49 k
DAC Out
9
5.0 k
10 V Span
10
5.0 k
11
20 V Span
Reference Out
4
2.5 Volt Reference
Current Switches
Reference In
6
4.99 k
Reference Ground
5
5.0 k
+
−
R2R Ladder
7 VEE
Gnd 12

### PIN CONNECTIONS


VCC 1
CMOS/TTL Threshold 2
Ref Supply 3
Ref Out 4
Ref Gnd 5
Ref In 6
VEE 7
Bipolar Offset 8
DAC Out 9
10 V Span 10
20 V Span 11
Gnd 12
24 Bit 1 (MSB)
23 Bit 2
22 Bit 3
21 Bit 4
20 Bit 5
19 Bit 6
18 Bit 7
17 Bit 8
16 Bit 9
15 Bit 10
14 Bit 11
13 Bit 12 (LSB)

### ORDERING INFORMATION

| Device | Temperature Range | Accuracy @ 25°C | Gain TC (ppm of FS/°C) |
|---|---|---|---|
| AD563JL | 0°C to +70°C | ±1/2 LSB | 30 |
| AD563KL | 0°C to +70°C | ±1/4 LSB | 20 |
| AD563SL | −55°C to +125°C | ±1/4 LSB | 30 |
| AD563TL | −55°C to +125°C | ±1/4 LSB | 10 |

**MAXIMUM RATING** ($T_A$ = 25°C, Ratings are referred to Ground [Pin 12] unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>-18 | Vdc |
| Reference Ground (Pin 5) | $V_{AD}$ | ±1.0 | Vdc |
| Applied Output Voltage (Pin 9) | $V_O$ | -7.0 to +12 | Vdc |
| CMOS/TTL Threshold Select (Pin 2) | — | 0 to $V_{CC}$ | Vdc |
| Digital Input Voltage (Pins 13 to 24) | $V_I$ | -5.0 to +18 | Vdc |
| Reference Input to Reference Ground | $V_{RI}$ | ±12 | Vdc |
| Reference Current | $I_{REF}$ | Short circuit to either Gnd; momentary short circuit to $V_{CC}$ | |
| Bipolar Offset to Reference Ground | — | ±12 | Vdc |
| Ten Volt Span Resistor to Reference Ground | — | ±12 | Vdc |
| Twenty Volt Span Resistor to Reference Ground | — | ±24 | Vdc |
| Power Dissipation | $P_D$ | 1000 | mW |
| Operating Temperature Range AD563JL/AD563KL<br>AD563SL/AD563TL | $T_A$ | 0 to +70<br>-55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Junction Temperature | $T_J$ | +175 | °C |

## TERMINOLOGY

**Nonlinearity** (Relative Accuracy) — Maximum output deviation from ideal straight line connecting zero and full-scale readings, expressed as a fraction of LSB or percent of full scale.

**Differential Nonlinearity** — Maximum deviation in the readings of any two adjacent input bit codes from the ideal LSB step, expressed in fractions of LSB or percentage of full scale. A differential nonlinearity value greater than 1 LSB may lead to nonmonotonic operation.

**Monotonicity** — For every increase in the input digital word, the output current either remains the same or increases.

The AD563 is guaranteed to be monotonic over temperature.

**Settling Time** — The elapsed time from the input transition until the output has settled within an error band about its final value.

The worst case switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 200 ns for the output to settle to within ±1/2 LSB for 12-bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small (<0.5 V) swing and the external output capacitance is under 10 pF.

**Gain Error** — The difference between the actual full scale range (difference in output between all bits on, and all bits off) and the ideal full scale range. Based on a 0 to 10 V output configuration, the ideal FSR is $\frac{4095}{4096} \times 10 = 9.99756$ V.

Gain error is expressed in percentage of full scale (FS).

**Unipolar Offset Error** — Using the configuration shown in Figure 1, with R1 = 10 ohms and with all bits off, the output voltage reading compared to zero is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

**Bipolar Offset Error** — Using the configuration shown in Figure 2, with R2 = 10 ohms with all bits off, the output voltage reading compared to the ideal negative full scale value is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

**Bipolar Zero Error** — Using the configuration shown in Figure 2, with R1 = R2 = 10 Ω, with the MSB on and all other bits off, the output voltage reading compared to zero is expressed as a percentage of the full-scale range. Offset voltage of the output op amp must be nulled.

**Temperature Coefficients** — (Unipolar Offset, Bipolar Offset, Gain and Differential Nonlinearity). The maximum deviation of the particular parameter over the specified temperature range, divided by the temperature range, expressed in parts per million of Full Scale Range per degree C.

**Compliance Voltage Range** — The output terminal voltage range which will provide specified output resistance and current characteristics. The compliance voltage is specified with $V_{EE} = -15$. The compliance voltage range follows as $V_{EE}$ is varied.

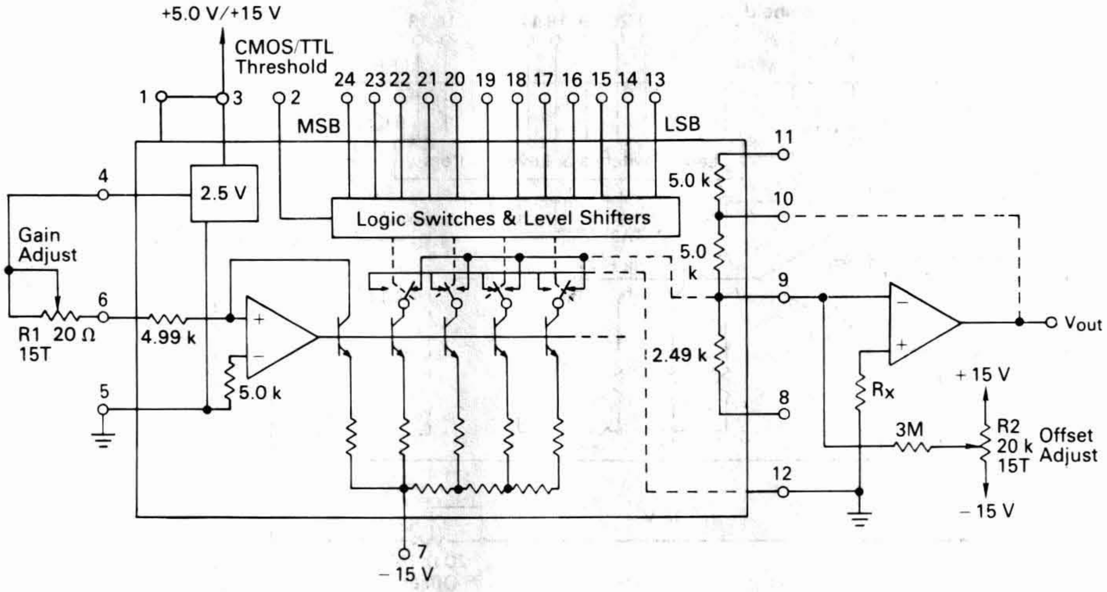
**Power Supply Sensitivity** — The change in full scale current caused by a change in $V_{EE}$ or $V_{CC}$ expressed in ppm of full scale current per percent change in $V_{EE}$ or $V_{CC}$.

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = +5.0 V, $V_{EE}$ = –15 V, Pin 2 open, $T_A$ = 25°C, all tests performed using internal reference, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TTL Digital Logic Levels (All Bits) |  |  |  |  | V |
| (4.5 V ≤ $V_{CC}$ ≤ 16.5 V, $T_{low}$ to $T_{high}$, see Note 1) |  |  |  |  |  |
| Bit On, Logic "1" | $V_{IH}$ | 2.0 | — | — |  |
| Bit Off, Logic "0" | $V_{IL}$ | — | — | 0.8 |  |
| CMOS Digital Logic Levels (All Pins) |  |  |  |  | V |
| (4.5 V ≤ $V_{CC}$ ≤ 16.5 V, $T_{low}$ to $T_{high}$, see Note 1, Pin 2 tied to Pin 1) |  |  |  |  |  |
| Bit On, Logic "1" | $V_{IH}$ | 70% $V_{CC}$ | — | — |  |
| Bit Off, Logic "0" | $V_{IL}$ | — | — | 30% $V_{CC}$ |  |
| Digital Input Current, CMOS/TTL Levels — Bit On, Logic "1" | $I_{IH}$ | — | +0.02 | +0.1 | μA |
| ($T_{low}$ to $T_{high}$, see Note 1) |  |  |  |  |  |
| Bit On, Logic "1" | $I_{IH}$ | — | — | +1.0 |  |
| Bit Off, Logic "0" | $I_{IL}$ | — | -2.0 | -75 |  |
| Programmable Output Range | — | — | 0 to +5.0 | — | V |
| (See Figures 1 and 2) |  | — | -2.5 to +2.5 | — |  |
|  |  | — | 0 to +10 | — |  |
|  |  | — | -5.0 to +5.0 | — |  |
|  |  | — | -10 to +10 | — |  |
| Output Current | $I_O$ |  |  |  | mA |
| Unipolar (All Bits On) |  | -1.6 | -2.0 | -2.4 |  |
| Bipolar (All Bits On or Off) |  | ±0.8 | ±1.0 | ±1.2 |  |
| Output Resistance (Exclusive of Span Resistors) | $R_O$ | 1.0 | 5.0 | — | MΩ |
| Output Capacitance | $C_O$ | — | 25 | — | pF |
| Output Compliance Voltage Range ($T_{low}$ to $T_{high}$, see Note 1) | $V_{OC}$ | -5.0 | — | +10 | V |
| Nonlinearity **AD563KL/AD563SL/AD563TL** | NL | — | — | ±1/4 | LSB |
|  |  | — | — | (0.006) | % of FS |
| **AD563JL** |  | — | — | ±1/2 | LSB |
|  |  | — | — | (0.012) | % of FS |
| Differential Nonlinearity | — | — | — | ±1/2 | LSB |
| Differential Nonlinearity ($T_{low}$ to $T_{high}$, see Note 1) | Monotonicity Guaranteed |  |  |  |  |
| Gain Error — Figure 1, R1 = Fixed 10 Ω | — | — | ±0.1 | — | % of FS |
| Offset Error | — |  |  |  | % of FS |
| Unipolar — Figure 1 |  | — | ±0.01 | ±0.05 |  |
| Bipolar — Figure 2, R2 = Fixed 10 Ω |  | — | ±0.1 | — |  |
| Bipolar Zero Error — Figure 2, R1 = R2 = Fixed 10 Ω | — | — | ±0.1 | — | % of FS |
| Gain Adjustment Range — Figure 1 | — | — | ±0.2 | — | % of FS |
| Bipolar Offset Adjustment Range — Figure 2 | — | — | ±0.2 | — | % of FS |
| Unipolar Zero Temperature Coefficient ($T_{low}$ to $T_{high}$, see Note 1) | — | — | 1.0 | 2.0 | ppm/°C |
| Bipolar Zero Temperature Coefficient ($T_{low}$ to $T_{high}$, see Note 1) | — | — | 5.0 | 10 | ppm/°C |
| Gain Temperature Coefficient, Full Scale ($T_{low}$ to $T_{high}$, see Note 1) | — |  |  |  | ppm/°C |
| **AD563TL** |  | — | — | 10 |  |
| **AD563KL** |  | — | — | 20 |  |
| **AD563JL/AD563SL** |  | — | — | 30 |  |
| Differential Nonlinearity Temperature Coefficient ($T_{low}$ to $T_{high}$, see Note 1) | — | — | 1.0 | — | ppm/°C |
| Settling Time to 1/2 LSB All Bits On-to-Off or Off-to-On | $t_s$ | — | 0.2 | 1.2 | μs |
| Reference Input Impedance | $Z_{in}$ | — | 5 k | — | kΩ |
| Reference Output Voltage | $V_{RO}$ | 2.475 | 2.500 | 2.525 | Volts |
| Reference Output Current | $I_{RO}$ | 5.0 | — | — | mA |
| Power Supply Current |  |  |  |  | mA |
| ($V_{CC}$ +4.5 to +16.5 Vdc) | $I_{CC}$ | — | 6.0 | 10 |  |
| ($V_{EE}$ –10.8 to –16.5 Vdc) | $I_{EE}$ | — | -8.0 | -12 |  |
| Power Supply Gain Sensitivity |  |  |  |  | ppm of FS/% |
| ($V_{CC}$ +4.5 to +5.5 Vdc) | $PSSI_{FS+}$ | — | 2.0 | 10 |  |
| ($V_{CC}$ +13.5 to +16.5 Vdc) | $PSSI_{FS+}$ | — | 2.0 | 10 |  |
| ($V_{EE}$ –10.8 to –16.5 Vdc) | $PSSI_{FS-}$ | — | 10 | 25 |  |

Note 1: $T_{low}$ = –55°C for AD563SL/AD563TL    $T_{high}$ = +125°C for AD563SL/AD563TL
0°C for AD563JL/AD563KL    +70°C for AD563JL/AD563KL

FIGURE 1 — AD563 IN TYPICAL UNIPOLAR CONNECTION SCHEME


+5.0 V/+15 V
CMOS/TTL
Threshold
24 23 22 21 20 19 18 17 16 15 14 13
1
3
2
MSB
LSB
11
4
2.5 V
5.0 k
10
Logic Switches & Level Shifters
Gain
Adjust
5.0
k
9
6
R1 20 Ω
15T
4.99 k
2.49 k
5
5.0 k
8
Vout
+15 V
Rx
3M
R2
20 k
15T
Offset
Adjust
12
−15 V
7
−15 V

## UNIPOLAR DAC OPERATION

A typical circuit configuration for unipolar operation of AD563 is shown in Figure 1.

**Step 1 — Output Range**

Determine which output range is required. For +5.0 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier output and short Pin 9 to Pin 11. For +10 Volt FS range, connect Pin 10 to external operational amplifier output, Pin 11 remains unconnected.

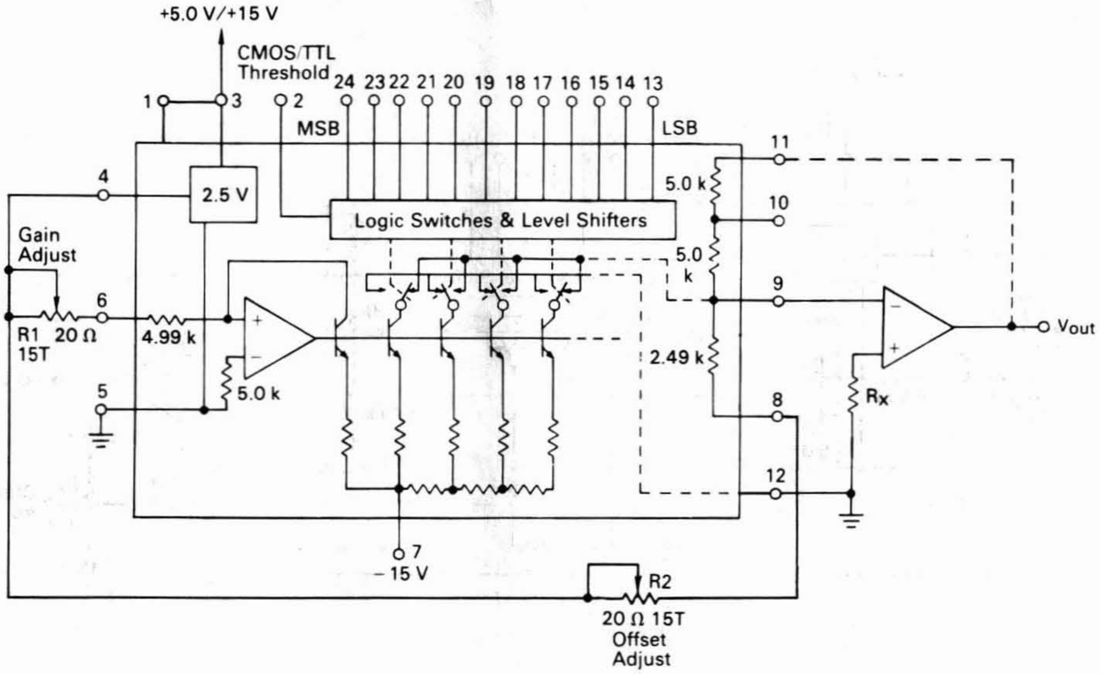
**Step 2 — Zero Adjust**

Turn all bits OFF and adjust R2 until external operational amplifier output is 0 Volts.

**Step 3 — Gain Adjust**

Turn all bits ON. Adjust R1 until operational amplifier output reaches 4.9988 Volts for +5.0 Volt range or 9.9976 for +10 Volt range.

FIGURE 2 — AD563 IN TYPICAL BIPOLAR CONNECTION SCHEME


+5.0 V/+15 V
CMOS/TTL Threshold
24 23 22 21 20 19 18 17 16 15 14 13
1
3
2
MSB
LSB
11
4
2.5 V
5.0 k
10
Logic Switches & Level Shifters
Gain Adjust
5.0 k
9
6
R1 20 Ω 15T
4.99 k
2.49 k
5.0 k
5
8
Rx
Vout
12
7
−15 V
R2
20 Ω 15T Offset Adjust

## BIPOLAR DAC OPERATION

A typical circuit configuration for bipolar operation of AD563 is shown in Figure 2.

**Step 1 — Output Range**

Determine which output range is required. For ±2.5 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier and short Pin 9 to Pin 11. For ±5.0 Volt FS range, connect Pin 10 to output of external operational amplifier, Pin 11 remains unconnected. For ±10 Volt FS range, connect Pin 11 to output of external operational amplifier, Pin 10 remains unconnected.

**Step 2 — Offset Adjust**

Turn all bits OFF and adjust R2 until operational amplifier output is:

-2.5000 Volt for ±2.5 Volt range
-5.0000 Volt for ±5.0 Volt range
-10.0000 Volt for ±10 Volt range

**Step 3 — Gain Adjust (Bipolar Zero)**

Turn MSB ON and all other bits OFF. Adjust R1 until operational amplifier output is 0 Volts.

**NOTES:**

1. For TTL and DTL compatibility, leave Pin 2 open.
2. For CMOS compatibility, short Pin 2 to Pin 1.
3. Supplies should be bypassed with 0.1 $\mu$F capacitors.
4. In unipolar operation, $R_X$ should be made equal to the internal feedback resistor. In bipolar, $R_X$, equals the feedback resistor in parallel with 2.5 k.

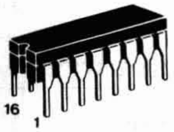
**MOTOROLA**

# DAC-08

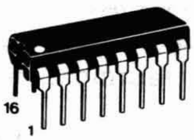
## Specifications and Applications Information

### HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



**Q SUFFIX**
CERAMIC PACKAGE
CASE 620-02



**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

**D SUFFIX**
PLASTIC PACKAGE
CASE 751B-01
SO-16*

***Surface Mount pin-out is different than standard package pin-out for this device. Please refer to Chapter 7 for details.**

### HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

The DAC-08 series is a monolithic 8-bit high speed multiplying digital-to-analog converter, capable of settling to within 1/2 LSB (0.19%) in 85 ns. Monotonic multiplying performance is retained over a wide 40-to-1 reference current range. Full scale and reference currents are matched to within 1 LSB, therefore eliminating the need for full scale trim in most applications.

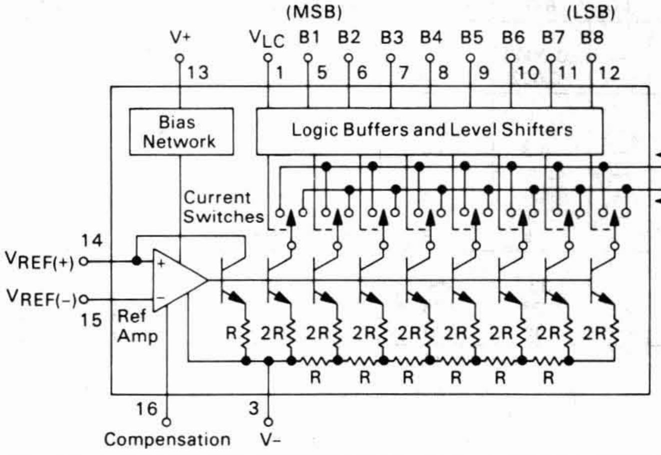
Dual complementry current outputs with high voltage compliance provide added versatility and allow differential mode of operation to effectively double the peak-to-peak output swing. In many applications, output current-to-voltage conversion can be accomplished without requiring an external op amp. Noise-immune inputs permit direct interface with TTL and DTL levels when the logic threshold control, $V_{LC}$, (pin 1) is grounded. All other logic family thresholds are attainable by adjusting the voltage level of pin 1. Performance characteristics are virtually unchanged over the entire ±4.5 V to ±18 V power supply range. Power consumption is typically 33 mW with ±5.0 V supplies.

The DAC-08 is available in several versions, with nonlinearity as tight as ±0.1% (±1/4 LSB) over temperature. All versions are guaranteed monotonic over 8 bits. For an extra margin of performance, Motorola utilizes thin-film resistors permitting very accurate resistive values which are extremely stable over temperature.

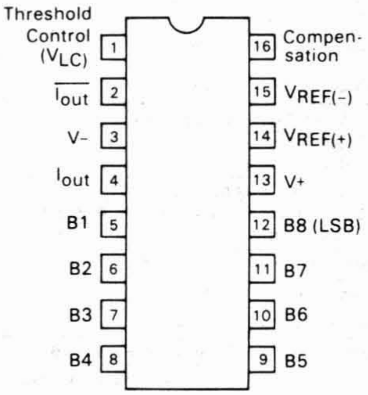
High performance characteristics along with low cost, make the DAC-08 an excellent selection for applications such as CRT displays, waveform generation, high-speed modems, and high-speed analog-to-digital converters.

- Fast Settling Time — 85 ns
- Full Scale Current Prematched to ±1 LSB
- Nonlinearity Over Temperature to ±0.1% Max
- Differential Current Outputs
- High Voltage Compliance Outputs −10 V to +18 V
- Wide Range Multiplying Capability
- Inputs Compatable With TTL, DTL, CMOS, PMOS, ECL, HTL
- Low Full Scale Current Drift
- Wide Power Supply Range ±4.5 V to ±18 V
- Low Power Consumption
- Thin-Film Resistors
- Low Cost

DAC-08 EQUIVALENT CIRCUIT


(MSB)
(LSB)
V+
VLC
B1
B2
B3
B4
B5
B6
B7
B8
13
1
5
6
7
8
9
10
11
12
Bias Network
Logic Buffers and Level Shifters
4
Iout
Iout
2
Current Switches
14
VREF(+)
VREF(−)
15
Ref Amp
R
2R
2R
2R
2R
2R
2R
2R
2R
R
R
R
R
R
R
16
3
Compensation
V−

PINOUT DIAGRAM


Threshold Control (VLC)
1
Iout
2
V−
3
Iout
4
B1
5
B2
6
B3
7
B4
8
16
Compen-sation
15
VREF(−)
14
VREF(+)
13
V+
12
B8 (LSB)
11
B7
10
B6
9
B5

| Device | Nonlinearity | Temperature Range | Package |
|---|---|---|---|
| DAC-08AQ | ±0.1% | −55°C to +125°C | Ceramic |
| DAC-08Q | ±0.19% | | Ceramic |
| DAC-08HQ | ±0.1% | 0°C to +70°C | Ceramic |
| DAC-08EQ | ±0.19% | | Ceramic |
| DAC-08CD | ±0.39% | | SO-16 |
| DAC-08ED | ±0.19% | | SO-16 |
| DAC-08CQ | ±0.39% | | Ceramic |
| DAC-08HP | ±0.1% | | Plastic |
| DAC-08EP | ±0.19% | | Plastic |
| DAC-08CP | ±0.39% | | Plastic |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| V+ Supply to V– Supply | — | 36 | V |
| Logic Inputs | — | V– to V– Plus 36 | V |
| Logic Threshold Control | $V_{LC}$ | V– to V+ | V |
| Analog Current Outputs | $I_{out}$ | See Figure 7 | mA |
| Reference Inputs (V14, V15) | $V_{REF}$ | V– to V+ | V |
| Reference Input Differential Voltage (V14 to V15) | $V_{REF(D)}$ | ±18 | V |
| Reference Input Current (I14) | $I_{REF}$ | 5.0 | mA |
| Operating Temperature Range | $T_A$ | | °C |
| DAC-08AQ, Q | | -55 to +125 | |
| DAC-08HQ, EQ, CQ, HP, EP, CP | | 0 to +70 | |
| Storage Temperature | $T_A$ | -65 to +150 | °C |
| Power Dissipation | $P_D$ | 500 | mW |
| Derate above 100°C | $R_{\theta JA}$ | 10 | mW/°C |

**ELECTRICAL CHARACTERISTICS** ($V_S$ = ±15 V, $I_{REF}$ = 2.0 mA, $T_A$ = -55°C to +125°C, unless otherwise noted.)

| Characteristic | Symbol | DAC-08A | | | DAC-08 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Resolution | — | 8 | 8 | 8 | 8 | 8 | 8 | Bits |
| Monotonicity | — | 8 | 8 | 8 | 8 | 8 | 8 | Bits |
| Nonlinearity, $T_A$ = 0°C to +70°C | NL | — | — | ±0.1 | — | — | ±0.19 | %FS |
| **Settling Time to ±1/2 LSB, Figure 24 (All Bits Switched On or Off, $T_A$ = 25°C)** | $t_s$ | — | 85 | 135 | — | 85 | 150 | ns |
| **Propagation Delay, $T_A$ = 25°C** | | | | | | | | ns |
| **Each Bit** | $t_{PLH}$ | — | 35 | 60 | — | 35 | 60 | |
| **All Bits Switched** | $t_{PHL}$ | — | 35 | 60 | — | 35 | 60 | |
| Full Scale Tempco | $TCI_{FS}$ | — | ±10 | ±50 | — | ±10 | ±80 | ppm/°C |
| Output Voltage Compliance Full Scale Current Change < 1/2 LSB, $R_{out}$ > 20 megohm typ. | $V_{OC}$ | -10 | — | +18 | -10 | — | +18 | V |
| Full Range Current ($V_{REF}$ = 10.000 V; R14, R15 = 5.000 kΩ, $T_A$ = 25°C) | $I_{FR4}$ | 1.984 | 1.992 | 2.000 | 1.94 | 1.99 | 2.04 | mA |
| Full Range Symmetry ($I_{FR4}$ - $I_{FR2}$) | $I_{FRS}$ | — | ±0.5 | ±4.0 | — | ±1.0 | ±8.0 | μA |
| Zero Scale Current | $I_{ZS}$ | — | 0.1 | 1.0 | — | 0.2 | 2.0 | μA |
| Output Current Range | | | | | | | | mA |
| V– = -5.0 V | $I_{OR1}$ | 0 | — | 2.1 | 0 | — | 2.1 | |
| V– = -8.0 V to -18 V | $I_{OR2}$ | 0 | — | 4.2 | 0 | — | 4.2 | |
| Logic Input Levels ($V_{LC}$ = 0 V) | | | | | | | | V |
| Logic "0" | $V_{IL}$ | — | — | 0.8 | — | — | 0.8 | |
| Logic "1" | $V_{IH}$ | 2.0 | — | — | 2.0 | — | — | |
| Logic Input Current ($V_{LC}$ = 0 V) | | | | | | | | μA |
| Logic Input "0" ($V_{in}$ = -10 V to +0.8 V) | $I_{IL}$ | — | -2.0 | -10 | — | -2.0 | -10 | |
| Logic Input "1" ($V_{in}$ = +2.0 V to +18 V) | $I_{IH}$ | — | 0.002 | 10 | — | 0.002 | 10 | |
| Logic Input Swing, V– = -15 V | $V_{IS}$ | -10 | — | +18 | -10 | — | +18 | V |
| Logic Threshold Range, $V_S$ = ±15 V | $V_{THR}$ | -10 | — | +13.5 | -10 | — | +13.5 | V |
| Reference Bias Current | $I_{15}$ | — | -1.0 | -3.0 | — | -1.0 | -3.0 | μA |
| **Reference Input Slew Rate Figure 19** | di/dt | 4.0 | 8.0 | — | 4.0 | 8.0 | — | mA/μs |
| Power Supply Sensitivity ($I_{REF}$ = 1.0 mA) | | | | | | | | %/% |
| V+ = 4.5 V to 18 V | $PSSI_{FS+}$ | — | ±0.0003 | ±0.01 | — | ±0.0003 | ±0.01 | |
| V– = -4.5 V to -18 V | $PSSI_{FS-}$ | — | ±0.002 | ±0.01 | — | ±0.002 | ±0.01 | |
| Power Supply Current | | | | | | | | mA |
| $V_S$ = ±5.0 V, $I_{REF}$ = 1.0 mA | I+ | — | 2.3 | 3.8 | — | 2.3 | 3.8 | |
| | I– | — | -4.3 | -5.8 | — | -4.3 | -5.8 | |
| $V_S$ = +5.0 V, -15 V, $I_{REF}$ = 2.0 mA | I+ | — | 2.4 | 3.8 | — | 2.4 | 3.8 | |
| | I– | — | -6.4 | -7.8 | — | -6.4 | -7.8 | |
| $V_S$ = ±15 V, $I_{REF}$ = 2.0 mA | I+ | — | 2.5 | 3.8 | — | 2.5 | 3.8 | |
| | I– | — | -6.5 | -7.8 | — | -6.5 | -7.8 | |
| Power Dissipation | $P_D$ | | | | | | | mW |
| $V_S$ = ±5.0 V, $I_{REF}$ = 1.0 mA | | — | 33 | 48 | — | 33 | 48 | |
| $V_S$ = +5.0 V, -15 V, $I_{REF}$ = 2.0 mA | | — | 103 | 136 | — | 108 | 136 | |
| $V_S$ = ±15 V, $I_{REF}$ = 2.0 mA | | — | 135 | 174 | — | 135 | 174 | |

**ELECTRICAL CHARACTERISTICS** ($V_S$ = ±15 V, $I_{REF}$ = 2.0 mA, $T_A$ = 0°C to 70°C, unless otherwise noted.)

| | | DAC-08H | | | DAC-08E | | | DAC-08C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Characteristic** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Resolution | — | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | Bits |
| Monotonicity | — | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | Bits |
| Nonlinearity, $T_A$ = 0°C to +70°C | NL | — | — | ±0.1 | — | — | ±0.19 | — | — | ±0.39 | %FS |
| Settling Time to ±1/2 LSB (All Bits Switched On or Off, ($T_A$ = 25°C) Figure 24 | $t_s$ | — | 85 | 135 | — | 85 | 150 | — | 85 | 150 | ns |
| Propagation Delay, $T_A$ = 25°C | | | | | | | | | | | ns |
| Each Bit | $t_{PLH}$ | — | 35 | 60 | — | 35 | 60 | — | 35 | 60 | |
| All Bits Switched | $t_{PHL}$ | — | 35 | 60 | — | 35 | 60 | — | 35 | 60 | |
| Full Scale Tempco | $TCI_{FS}$ | — | ±10 | ±50 | — | ±10 | ±50 | — | ±10 | ±80 | ppm/°C |
| Output Voltage Compliance Full Scale Current Change < 1/2 LSB, $R_{out}$ > 20 megohm typ. | $V_{OC}$ | −10 | — | +18 | −10 | — | +18 | −10 | — | +18 | V |
| Full Range Current ($V_{REF}$ = 10.000 V; R14, R15 = 5.000 kΩ) $T_A$ = 25°C | $I_{FR4}$ | 1.984 | 1.992 | 2.000 | 1.94 | 1.99 | 2.04 | 1.94 | 1.99 | 2.04 | mA |
| Full Range Symmetry ($I_{FR4}$ - $I_{FR2}$) | $I_{FRS}$ | — | ±0.5 | ±4.0 | — | ±1.0 | ±8.0 | — | ±2.0 | ±16.0 | μA |
| Zero Scale Current | $I_{ZS}$ | — | 0.1 | 1.0 | — | 0.2 | 2.0 | — | 0.2 | 4.0 | μA |
| Output Current Range | | | | | | | | | | | mA |
| V− = −5.0 V | $I_{OR1}$ | 0 | — | 2.1 | 0 | — | 2.1 | 0 | — | 2.1 | |
| V− = −8.0 V to −18 V | $I_{OR2}$ | 0 | — | 4.2 | 0 | — | 4.2 | 0 | — | 4.2 | |
| Logic Input Levels ($V_{LC}$ = 0 V) | | | | | | | | | | | V |
| Logic "0" | $V_{IL}$ | — | — | 0.8 | — | — | 0.8 | — | — | 0.8 | |
| Logic "1" | $V_{IH}$ | 2.0 | — | — | 2.0 | — | — | 2.0 | — | — | |
| Logic Input Current ($V_{LC}$ = 0 V) | | | | | | | | | | | μA |
| Logic Input "0" ($V_{in}$ = −10 V to +0.8 V) | $I_{IL}$ | — | −2.0 | −10 | — | −2.0 | −10 | — | −2.0 | −10 | |
| Logic Input "1" ($V_{in}$ = +2.0 V to +18 V) | $I_{IH}$ | — | 0.002 | 10 | — | 0.002 | 10 | — | 0.002 | 10 | |
| Logic Input Swing, V− = −15 V | $V_{IS}$ | −10 | — | +18 | −10 | — | +18 | −10 | — | +18 | V |
| Logic Threshold Range, $V_S$ = ±15 V | $V_{THR}$ | −10 | — | +13.5 | −10 | — | +13.5 | −10 | — | +13.5 | V |
| Reference Bias Current | $I_{15}$ | — | −1.0 | −3.0 | — | −1.0 | −3.0 | — | −1.0 | −3.0 | μA |
| Reference Input Slew Rate Figure 19 | dI/dt | 4.0 | 8.0 | — | 4.0 | 8.0 | — | 4.0 | 8.0 | — | mA/μs |
| Power Supply Sensitivity ($I_{REF}$ = 1.0 mA) | | | | | | | | | | | %/% |
| V+ = 4.5 V to 18 V | $PSSI_{FS+}$ | — | ±0.0003 | ±0.01 | — | ±0.0003 | ±0.01 | — | ±0.0003 | ±0.01 | |
| V− = −4.5 V to −18 V | $PSSI_{FS-}$ | — | ±0.002 | ±0.01 | — | ±0.002 | ±0.01 | — | ±0.002 | ±0.01 | |
| Power Supply Current | | | | | | | | | | | mA |
| $V_S$ = ±5.0 V, $I_{REF}$ = 1.0 mA | I+ | — | 2.3 | 3.8 | — | 2.3 | 3.8 | — | 2.3 | 3.8 | |
| | I− | — | −4.3 | −5.8 | — | −4.3 | −25.8 | — | −4.3 | −5.8 | |
| $V_S$ = +5.0 V, −15 V, $I_{REF}$ = 2.0 mA | I+ | — | 2.4 | 3.8 | — | 2.4 | 3.8 | — | 2.4 | 3.8 | |
| | I− | — | −6.4 | −7.8 | — | −6.4 | −7.8 | — | −6.4 | −7.8 | |
| $V_S$ = ±15 V, $I_{REF}$ = 2.0 mA | I+ | — | 2.5 | 3.8 | — | 2.5 | 3.8 | — | 2.5 | 3.8 | |
| | I− | — | −6.5 | −7.8 | — | −6.5 | −7.8 | — | −6.5 | −7.8 | |
| Power Dissipation | $P_D$ | | | | | | | | | | mW |
| $V_S$ = ±5.0 V, $I_{REF}$ = 1.0 mA | | — | 33 | 48 | — | 33 | 48 | — | 33 | 48 | |
| $V_S$ = +5.0 V, −15 V, $I_{REF}$ = 2.0 mA | | — | 108 | 136 | — | 108 | 136 | — | 108 | 136 | |
| $V_S$ = ±15 V, $I_{REF}$ = 2.0 mA | | — | 135 | 174 | — | 135 | 174 | — | 135 | 174 | |

## TYPICAL PERFORMANCE CURVES

**FIGURE 1 — FULL SCALE CURRENT versus REFERENCE CURRENT**

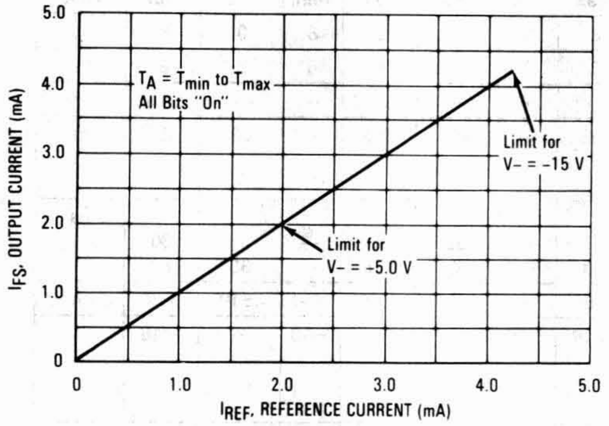
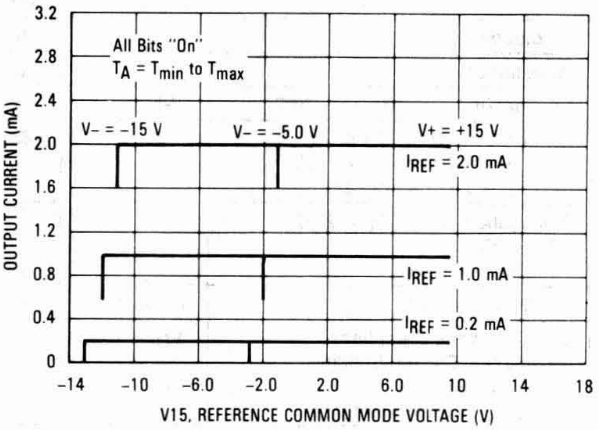
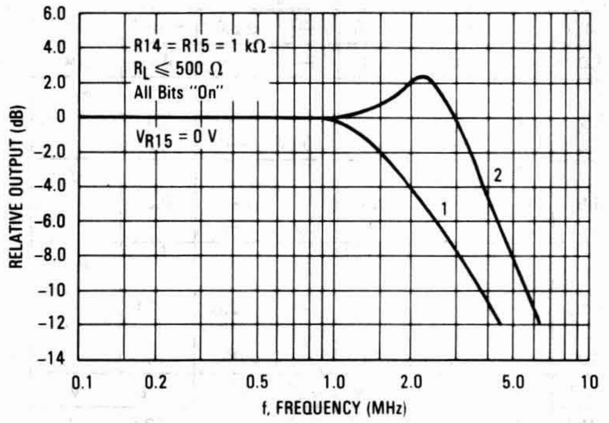


**FIGURE 2 — REFERENCE AMP COMMON MODE RANGE**



NOTE: Positive Common Mode Range is Always (V+) −1.5 V

**FIGURE 3 — REFERENCE INPUT FREQUENCY RESPONSE**



Curve 1 — $C_c$ = 15 pF, $V_{in}$ = 2.0 V p-p Centered at +1.0 V (Large-Signal)
Curve 2 — $C_c$ = 15 pF, $V_{in}$ = 50 mV p-p Centered at +200 mV (Small-Signal)

**FIGURE 4 — LSB PROPAGATION DELAY versus $I_{FS}$**

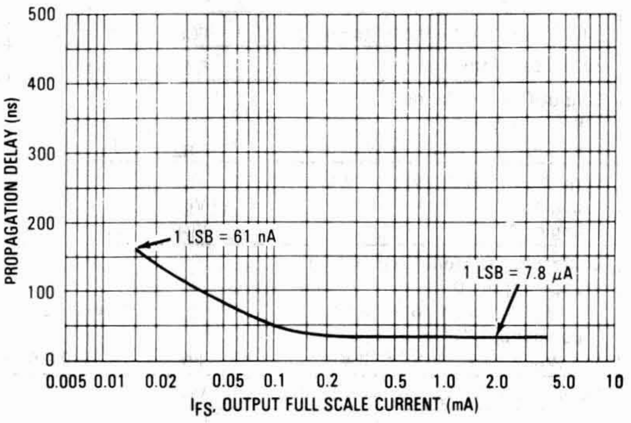


**FIGURE 5 — LOGIC INPUT CURRENT versus INPUT VOLTAGE**

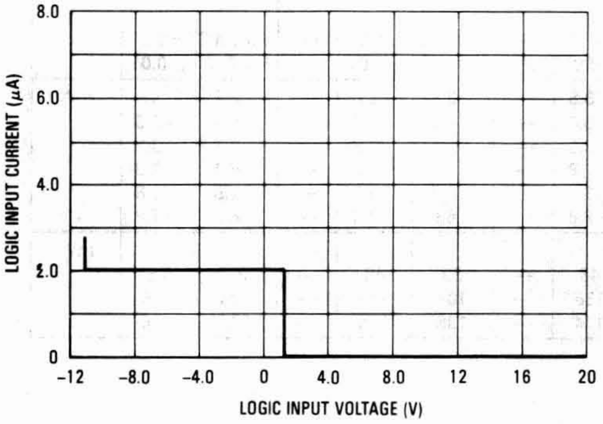
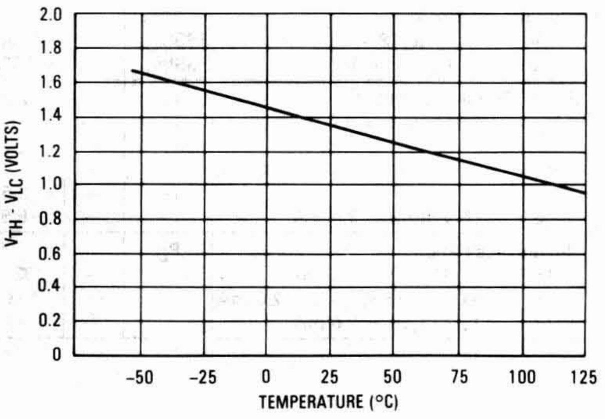


**FIGURE 6 — $V_{TH}$ - $V_{LC}$ versus TEMPERATURE**



## TYPICAL PERFORMANCE CURVES

**FIGURE 7 — OUTPUT CURRENT versus OUTPUT VOLTAGE (Output Voltage Compliance)**

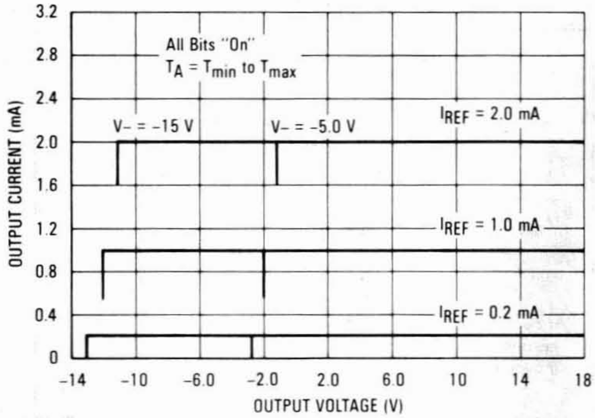


**FIGURE 8 — OUTPUT VOLTAGE COMPLIANCE versus TEMPERATURE**

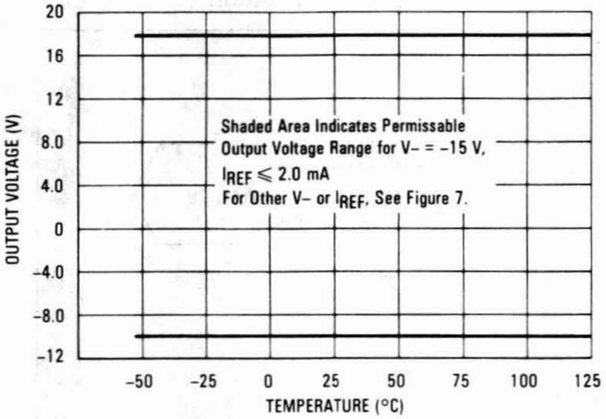
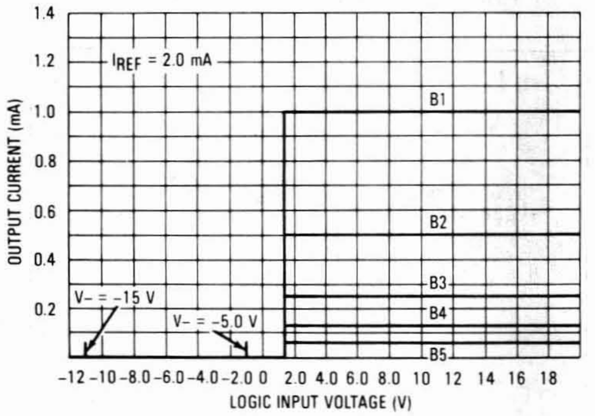


**FIGURE 9 — BIT TRANSFER CHARACTERISTICS**



NOTE: B1–B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 V and 2.0 V over operating temperature range ($V_{LC}$ = 0 V).

**FIGURE 10 — POWER SUPPLY CURRENT versus V+**

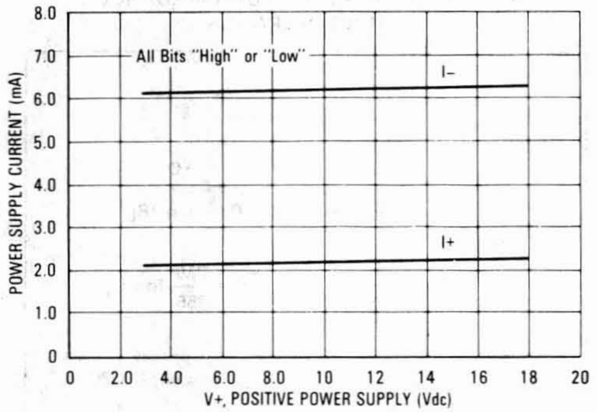


**FIGURE 11 — POWER SUPPLY CURRENT versus V–**

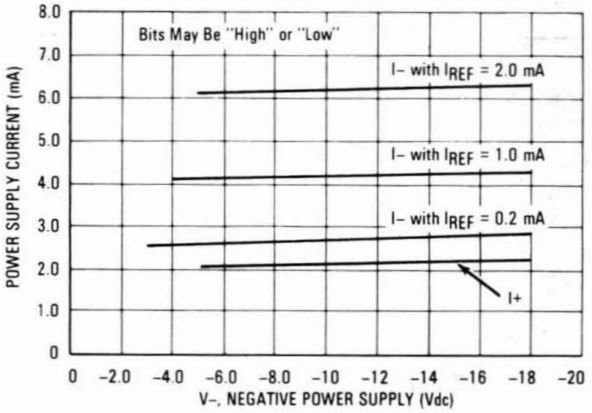
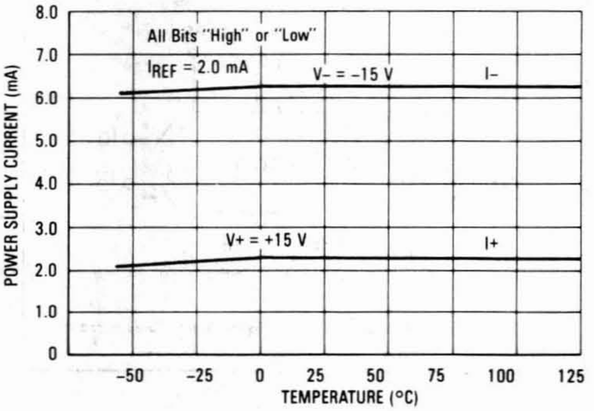


**FIGURE 12 — POWER SUPPLY CURRENT versus TEMPERATURE**



## BASIC CIRCUIT CONFIGURATIONS

FIGURE 13 — RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

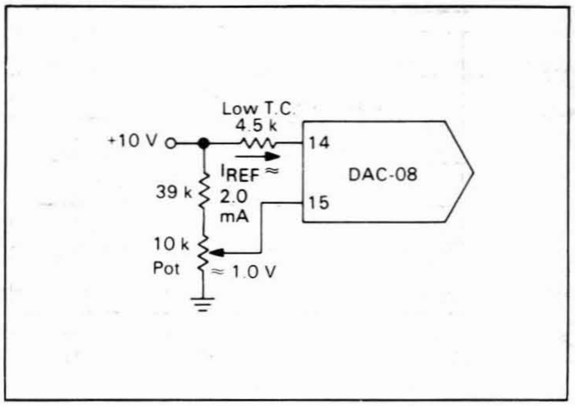
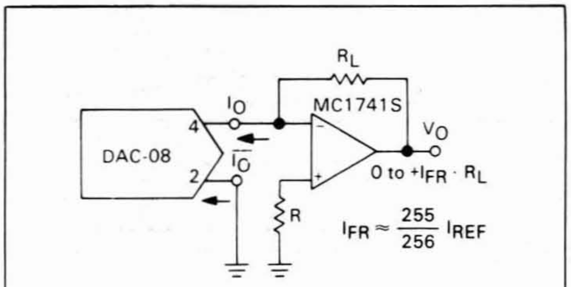

+10 V
Low T.C.
4.5 k
$I_{REF} \approx$ 2.0 mA
39 k
10 k
Pot
≈ 1.0 V
14
15
DAC-08

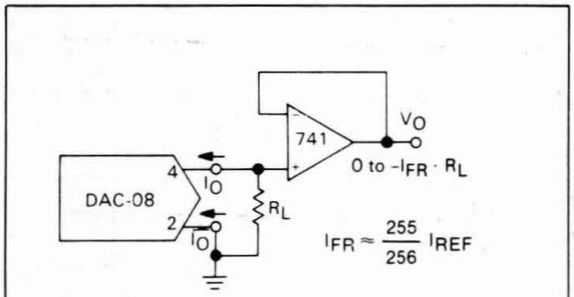
FIGURE 14 — POSITIVE LOW IMPEDANCE OUTPUT OPERATION


$R_L$
$I_O$
MC1741S
$V_O$
DAC-08
4
2
$\overline{I_O}$
0 to $+I_{FR} \cdot R_L$
R

$$I_{FR} \approx \frac{255}{256} I_{REF}$$

If complementry output (Negative Logic DAC) operation is desired, connect inverting input of op amp to $\overline{I_O}$ (Pin 2) and ground $I_O$ (Pin 4).

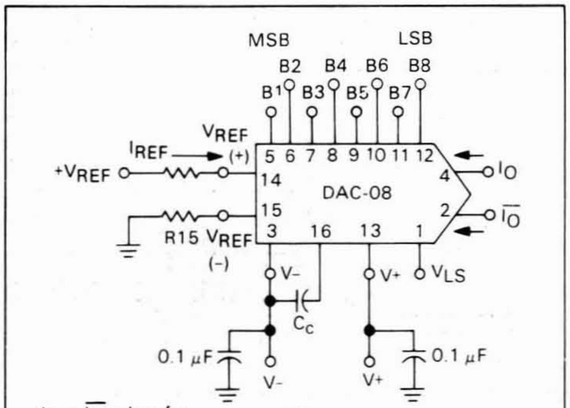
FIGURE 15 — NEGATIVE LOW IMPEDANCE OUTPUT OPERATION


741
$V_O$
0 to $-I_{FR} \cdot R_L$
DAC-08
4
2
$I_O$
$\overline{I_O}$
$R_L$

$$I_{FR} \approx \frac{255}{256} I_{REF}$$

If complementry output (Negative Logic DAC) is desired, connect noninverting input of op amp to $\overline{I_O}$ (Pin 2) and ground $I_O$ (Pin 4).

FIGURE 16 — BASIC POSITIVE REFERENCE OPERATION


MSB
LSB
B2 B4 B6 B8
B1 B3 B5 B7
$V_{REF}$
$I_{REF}$
(+)
$+V_{REF}$
5 6 7 8 9 10 11 12
14
DAC-08
15
3 16 13 1
4
2
$I_O$
$\overline{I_O}$
R15 $V_{REF}$
(-)
V−
V+
$V_{LS}$
$C_C$
0.1 µF
V−
V+
0.1 µF

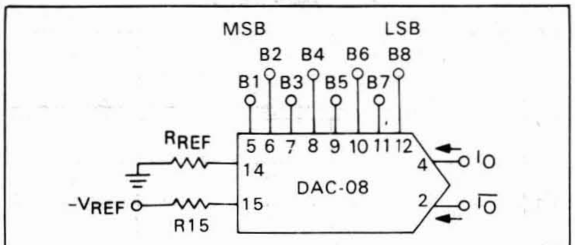
$I_O + \overline{I_O} = I_{FR}$ for all logic states

$$I_{FR} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

For fixed reference, TTL operation, typical values are

| | |
|---|---|
| $V_{REF}$ = +10.000 V | $C_c$ = 0.01 µF |
| $R_{REF}$ = 5.000 k | $V_{LC}$ = 0 V (Ground) |
| R15 ≈ $R_{REF}$ | |

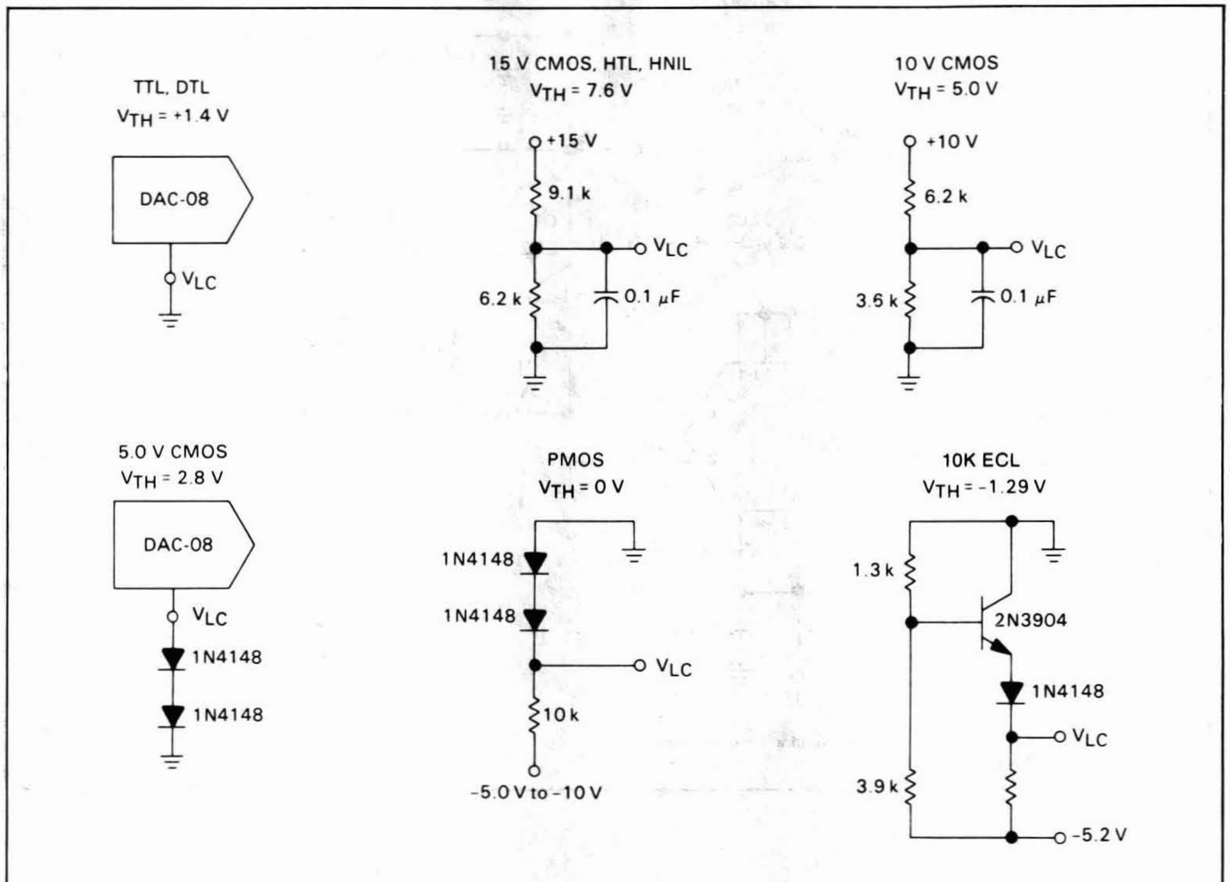
FIGURE 17 — BASIC NEGATIVE REFERENCE OPERATION


MSB
LSB
B2 B4 B6 B8
B1 B3 B5 B7
$R_{REF}$
5 6 7 8 9 10 11 12
14
DAC-08
15
4
2
$I_O$
$\overline{I_O}$
$-V_{REF}$
R15

$$I_{FR} \approx \left| \frac{-V_{REF}}{R_{REF}} \right| \times \frac{255}{256}$$

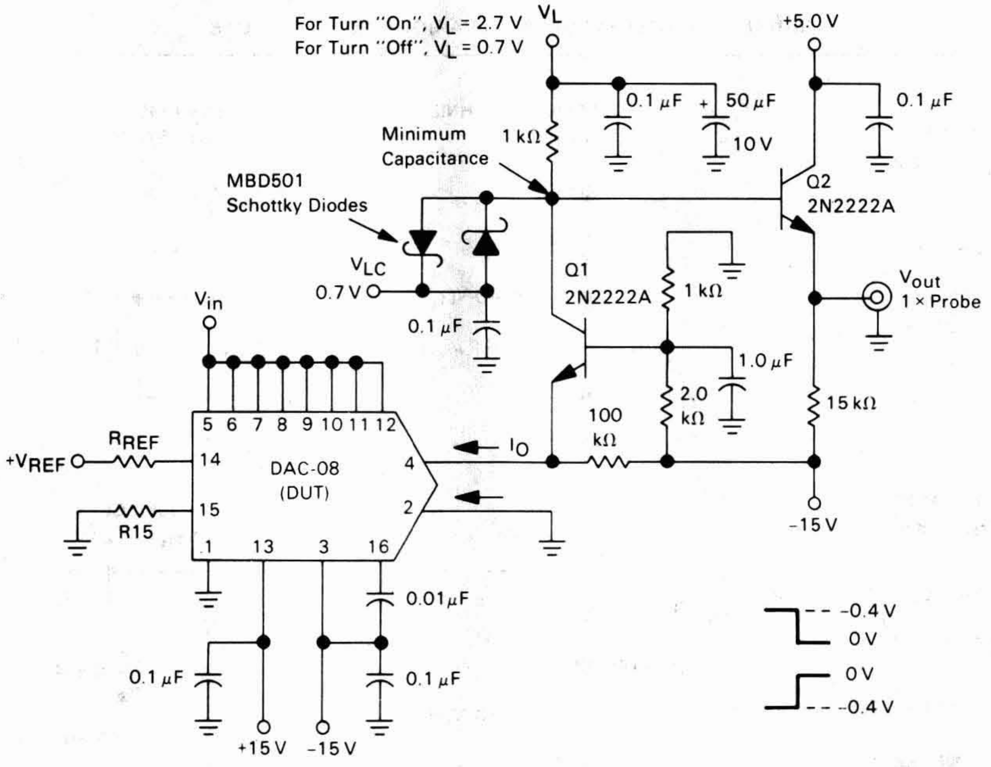
NOTE: $R_{REF}$ sets full scale current $I_{FR}$; R15 is for bias current cancellation.

FIGURE 23 — INTERFACING WITH VARIOUS LOGIC FAMILIES


TTL, DTL
VTH = +1.4 V
DAC-08
VLC
15 V CMOS, HTL, HNIL
VTH = 7.6 V
+15 V
9.1 k
VLC
6.2 k
0.1 μF
10 V CMOS
VTH = 5.0 V
+10 V
6.2 k
VLC
3.6 k
0.1 μF
5.0 V CMOS
VTH = 2.8 V
DAC-08
VLC
1N4148
1N4148
PMOS
VTH = 0 V
1N4148
1N4148
VLC
10 k
-5.0 V to -10 V
10K ECL
VTH = -1.29 V
1.3 k
2N3904
1N4148
VLC
3.9 k
-5.2 V

NOTE: Do not exceed negative logic input range of DAC.
$V_{TH} = V_{LC} + 1.4\ V$

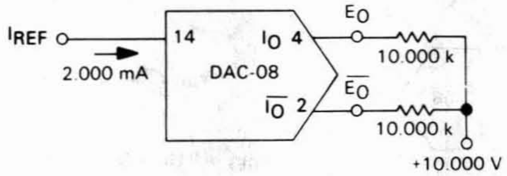
FIGURE 24 — SETTLING TIME MEASUREMENT CIRCUIT


For Turn "On", $V_L$ = 2.7 V
For Turn "Off", $V_L$ = 0.7 V
$V_L$
+5.0 V
0.1 µF
50 µF
10 V
0.1 µF
Minimum Capacitance
1 kΩ
MBD501 Schottky Diodes
Q2 2N2222A
$V_{LC}$
0.7 V
0.1 µF
Q1 2N2222A
1 kΩ
$V_{out}$
1 × Probe
$V_{in}$
1.0 µF
2.0 kΩ
100 kΩ
15 kΩ
$R_{REF}$
$+V_{REF}$
5 6 7 8 9 10 11 12
14
DAC-08 (DUT)
4
$I_O$
15
2
R15
1 13 3 16
-15 V
0.01 µF
0.1 µF
0.1 µF
+15 V -15 V
-0.4 V
0 V
0 V
-0.4 V

NOTE: Oscilloscope bandwidth for settling time measurement ⩾ 50 MHz

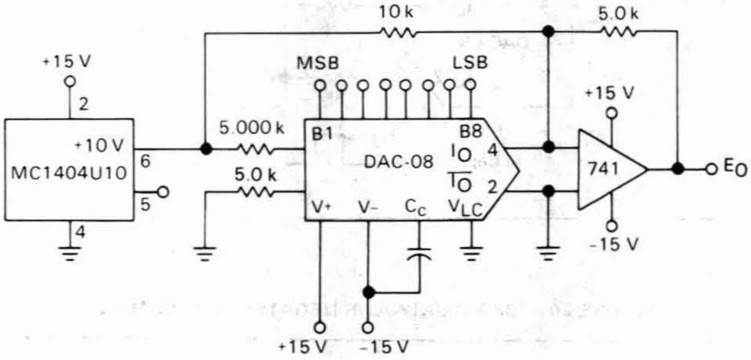
## BASIC CIRCUIT CONFIGURATIONS

FIGURE 21 — BASIC BIPOLAR OUTPUT OPERATION


$I_{REF}$
2.000 mA
14
$I_O$ 4
DAC-08
$\overline{I_O}$ 2
$E_O$
10.000 k
$\overline{E_O}$
10.000 k
+10.000 V

| | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | $E_O$ | $\overline{E_O}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Pos Full Range | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -9.920 | +10.000 |
| Pos Full Range -LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | -9.840 | +9.920 |
| Zero Scale +LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -0.080 | +0.160 |
| Zero Scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.000 | +0.080 |
| Zero Scale -LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +0.080 | 0.000 |
| Neg Full Scale +LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +9.920 | -9.840 |
| Neg Full Scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +10.000 | -9.920 |

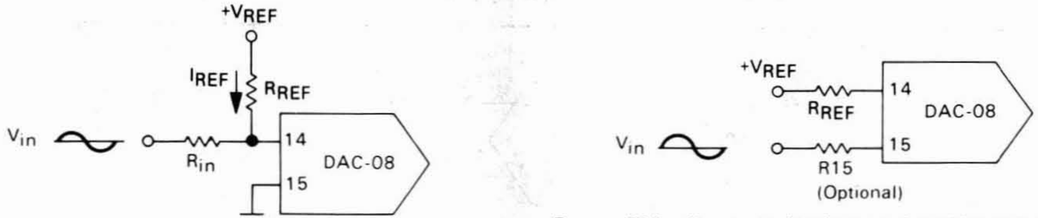
FIGURE 22 — OFFSET BINARY OPERATION


10 k
5.0 k
+15 V
2
MSB
LSB
+15 V
+10 V
MC1404U10
6
5
4
5.000 k
5.0 k
B1
B8
DAC-08
$I_O$ 4
$\overline{I_O}$ 2
V+
V-
$C_C$
$V_{LC}$
741
-15 V
$E_O$
+15 V
-15 V

| | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | $E_O$ |
|---|---|---|---|---|---|---|---|---|---|
| Pos Full Range | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -4.960 |
| Zero Scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.000 |
| Neg Full Scale +1 LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -4.960 |
| Neg Full Scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -5.000 |

## BASIC CIRCUIT CONFIGURATIONS

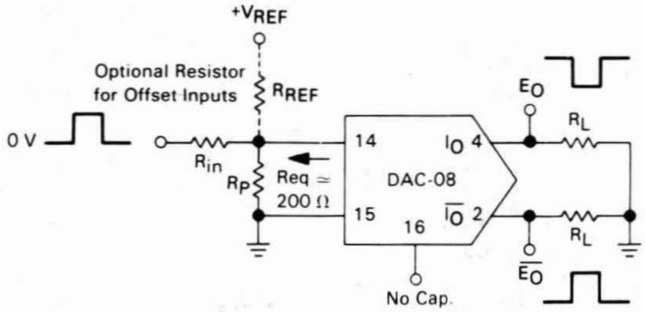
FIGURE 18 — ACCOMMODATING BIPOLAR REFERENCES


+$V_{REF}$
$I_{REF}$
$R_{REF}$
$V_{in}$
$R_{in}$
14
15
DAC-08
+$V_{REF}$
$R_{REF}$
14
DAC-08
$V_{in}$
15
R15
(Optional)

$I_{REF} \geqslant$ Peak Negative Swing of $I_{in}$

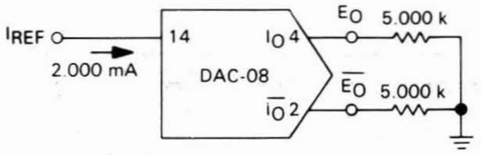
$R_{REF} \approx$ R15 +$V_{REF}$ must be above peak positive swing of $V_{in}$

FIGURE 19 — PULSED REFERENCE OPERATION


+$V_{REF}$
Optional Resistor for Offset Inputs
$R_{REF}$
0 V
$R_{in}$
$R_P$
Req ≈ 200 Ω
14
15
16
DAC-08
$I_O$ 4
$\overline{I_O}$ 2
No Cap.
$E_O$
$R_L$
$R_L$
$\overline{E_O}$

Typical Values: $R_{in}$ 5.0 k, +$V_{in}$ = 10 V

FIGURE 20 — BASIC UNIPOLAR NEGATIVE OPERATION


$I_{REF}$
2.000 mA
14
DAC-08
$I_O$ 4
$\overline{I_O}$ 2
$E_O$ 5.000 k
$\overline{E_O}$ 5.000 k

| | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | $I_O$ mA | $\overline{I_O}$ mA | $E_O$ | $\overline{E_O}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Full Range | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1.992 | 0.000 | -9.960 | -0.000 |
| Half Scale +LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.008 | 0.984 | -5.040 | -4.920 |
| Half Scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.000 | 0.992 | -5.000 | -4.960 |
| Half Scale -LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.992 | 1.000 | -4.960 | -5.000 |
| Zero Scale + LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.008 | 1.984 | -0.040 | -9.920 |
| Zero Scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.000 | 1.992 | 0.000 | -9.960 |

**MOTOROLA**

# MC1406L
# MC1506L

## Specifications and Applications Information

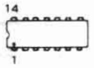
### SIX BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of a six-bit digital word and an analog input voltage.

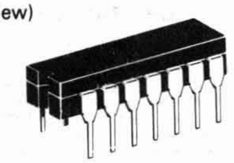
- Digital Inputs are MDTL and MTTL Compatible
- Relative Accuracy – ±0.78% Error maximum
- Low Power Dissipation – 85 mW typical @ ±5.0 V
- Adjustable Output Current Scaling
- Fast Settling Time – 150 ns typical
- Standard Supply Voltage: +5.0 V and -5.0 V to -15 V

SIX BIT, MULTIPLYING
DIGITAL-TO-ANALOG
CONVERTER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



(Top View)



CERAMIC PACKAGE
CASE 632-02
MO-001AA

FIGURE 1 – OUTPUT CURRENT SETTLING TIME (ALL BITS SWITCHED, $R_L$ = 50 Ω)

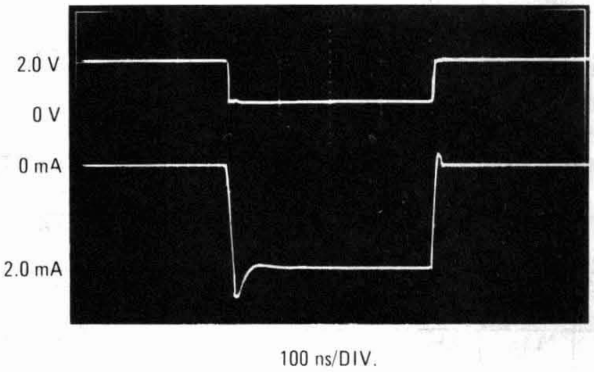
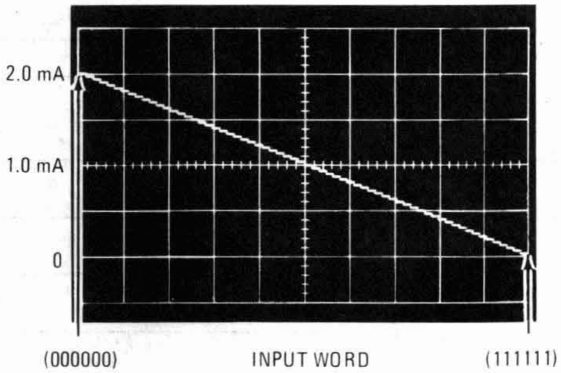


FIGURE 2 – D-to-A TRANSFER CHARACTERISTICS



### TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- Digital-to-Analog Meter Readout
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- Digital Varicap Tuning
- Video Systems
- Stepping Motor Drive
- CRT Character Generation
- Digital Addition and Subtraction
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Programmable Power Supplies
- Speech Encoding

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +5.5<br>-16.5 | Vdc |
| Digital Input Voltage | $V_5$ thru $V_{10}$ | +8.0, $V_{EE}$ | Vdc |
| Applied Output Voltage | $V_O$ | ±5.0 | Vdc |
| Reference Current | $I_{12}$ | 5.0 | mA |
| Reference Amplifier Inputs | $V_{12}$, $V_{13}$ | $V_{CC}$, $V_{EE}$ | Vdc |
| Power Dissipation (Package Limitation)<br>Ceramic Package<br>Derate above $T_A$ = +25°C | $P_D$ | <br>1000<br>6.7 | <br>mW<br>mW/°C |
| Operating Temperature Range<br>MC1506L<br>MC1406L | $T_A$ | <br>-55 to +125<br>0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $V_{EE}$ = −15 Vdc, $\frac{V_{ref}}{R12}$ = 2.0 mA, all logic inputs in low logic state, $T_A$ = $T_{high}$ to $T_{low}$, unless otherwise noted.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Relative Accuracy (Error relative to full scale $I_O$) | 10 | $E_r$ | – | – | ±0.78 | % |
| Settling Time (within 1/2 LSB [includes $t_d$] $T_A$ = +25°C) | 9 | $t_S$ | – | 150 | – | ns |
| Propagation Delay Time<br>$T_A$ = +25°C | 9 | $t_{PHL}$,<br>$t_{PLH}$ | – | 10 | 50 | ns |
| Output Full Scale Current Drift | | $\lvert TCI_O \rvert$ | – | 80 | – | PPM/°C |
| Digital Input Logic Levels<br>High Level, Logic "1"<br>Low Level, Logic "0" | 3,14 | <br>$V_{IH}$<br>$V_{IL}$ | <br>2.4<br>– | <br>–<br>– | <br>–<br>0.8 | Vdc |
| Digital Input Current<br>High Level, $V_{IH}$ = 5.0 V<br>Low Level, $V_{IL}$ = 0.8 V | 3,13 | <br>$I_{IH}$<br>$I_{IL}$ | <br>–<br>– | <br>0<br>-0.7 | <br>+0.01<br>-1.5 | mA |
| Reference Input Bias Current (Pin 13) | 3 | $I_{13}$ | – | -0.002 | -0.01 | mA |
| Output Current Range<br>$V_{EE}$ = −5.0 V<br>$V_{EE}$ = −15 V, $T_A$ = +25°C | 3 | $I_{OR}$ | <br>0<br>0 | <br>2.0<br>2.0 | <br>2.1<br>4.2 | mA |
| Output Current<br>$V_{ref}$ = 2.000 V, $R_{12}$ = 1.000 kΩ | 3 | $I_O$ | 1.9 | 1.97 | 2.1 | mA |
| Output Current<br>(all bits high) | 3 | $I_O$(min) | – | 0 | 10 | μA |
| Output Voltage Compliance<br>($E_r \leqslant \pm 0.78\%$ at $T_A$ = +25°C) | 3,4,5 | $V_{O+}$<br>$V_{O-}$ | –<br>– | +0.25<br>-0.45 | +0.1<br>-0.3 | Vdc |
| Reference Current Slew Rate<br>($T_A$ = +25°C) | 8,15 | SR $I_{ref}$ | – | 2.0 | – | mA/μs |
| Output Current Power Supply Sensitivity | 10 | PSRR (–) | – | 0.002 | 0.010 | mA/V |
| Power Supply Current<br>A1 thru A6; $V_{IL}$ = 0.8 V<br>A1 thru A6; $V_{IH}$ = 2.4 V | 3,11,12 | <br>$I_{CC}$<br>$I_{EE}$ | <br>–<br>– | <br>+7.2<br>-9.0 | <br>+11<br>-11 | mA |
| Power Dissipation (all bits high)<br>$V_{EE}$ = -5.0 Vdc<br>$V_{EE}$ = −15 Vdc | | $P_D$ | <br>–<br>– | <br>85<br>175 | <br>120<br>240 | mW |

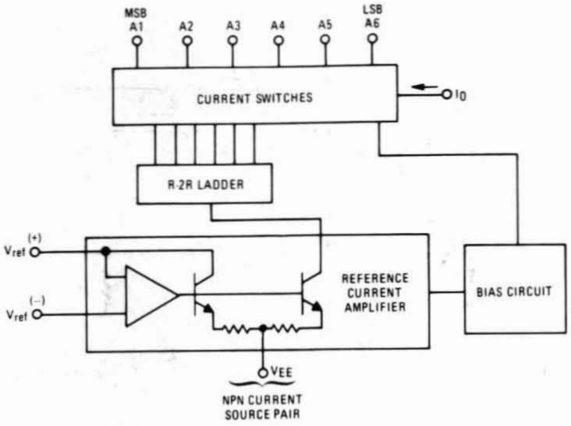
*$T_{high}$ = +70°C for MC1406L  $T_{low}$ = 0°C for MC1406L
= +125°C for MC1506L  = -55°C for MC1506L

The MC1506L consists of a reference current amplifier, an R-2R ladder, and six high-speed current switches. For many applications, only a reference resistor and a reference supply voltage need be added.

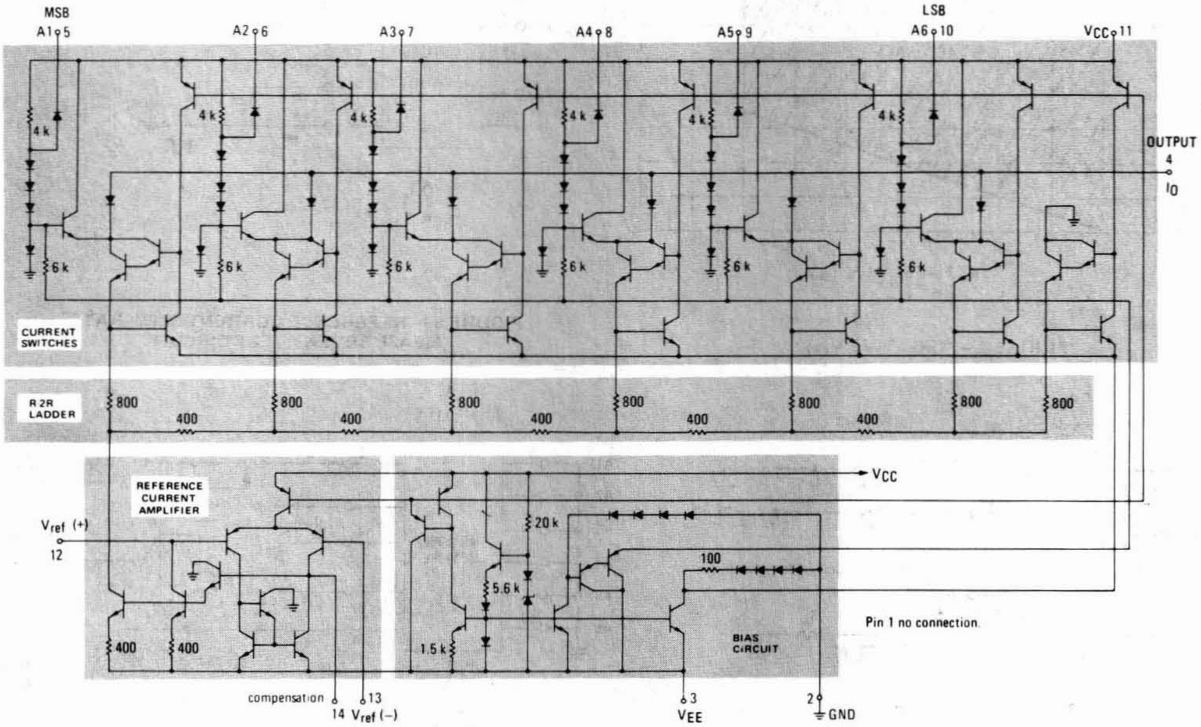
The switches are inverting in operation, therefore a low state at the input turns on the specified output current component. The switches use a current steering technique for high speed and a termination amplifier that consists of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components which are fed to the switches. Note that there is always a remainder current that is equal to the least significant bit. This current is shunted to ground, and the maximum current is 63/64 of the reference amplifier current, or 1.969 mA for a 2.0 mA reference current if the NPN current source pair is perfectly matched.

**BLOCK DIAGRAM**

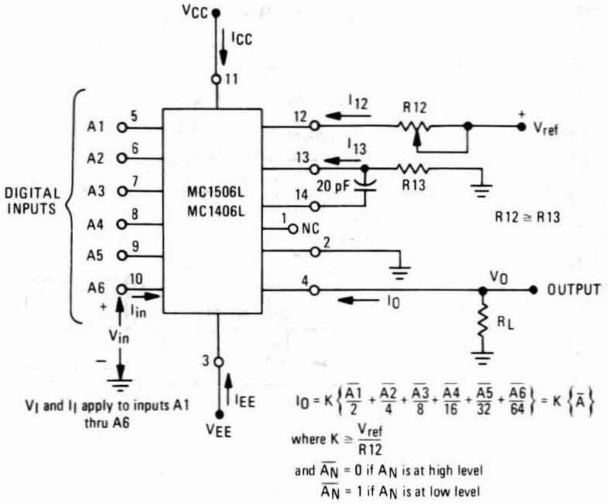

MSB
A1
A2
A3
A4
A5
LSB
A6
CURRENT SWITCHES
$I_O$
R-2R LADDER
$V_{ref}$ (+)
$V_{ref}$ (−)
REFERENCE CURRENT AMPLIFIER
BIAS CIRCUIT
VEE
NPN CURRENT SOURCE PAIR

**COMPLETE CIRCUIT SCHEMATIC**
(Digital Inputs; pins 5,6,7,8,9,10)


MSB
A1 5
A2 6
A3 7
A4 8
A5 9
LSB
A6 10
$V_{CC}$ 11
OUTPUT
4
$I_O$
4 k
6 k
CURRENT SWITCHES
R 2R LADDER
800
400
REFERENCE CURRENT AMPLIFIER
$V_{CC}$
$V_{ref}$ (+)
12
20 k
100
5.6 k
1.5 k
400
BIAS CIRCUIT
Pin 1 no connection.
compensation
13
14 $V_{ref}$ (−)
3
$V_{EE}$
2
GND

## TEST CIRCUITS AND TYPICAL CHARACTERISTICS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT


VCC
ICC
11
DIGITAL INPUTS
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
MC1506L
MC1406L
I12
R12
12
13
I13
R13
+ Vref
20 pF
14
1 NC
2
R12 ≅ R13
4
VO
OUTPUT
IO
RL
+ Iin
Vin
3
IEE
VEE
VI and II apply to inputs A1 thru A6

$I_O = K\left\{\frac{\overline{A1}}{2} + \frac{\overline{A2}}{4} + \frac{\overline{A3}}{8} + \frac{\overline{A4}}{16} + \frac{\overline{A5}}{32} + \frac{\overline{A6}}{64}\right\} = K\left\{\overline{A}\right\}$

where $K \cong \frac{V_{ref}}{R12}$

and $\overline{A_N} = 0$ if $A_N$ is at high level

$\overline{A_N} = 1$ if $A_N$ is at low level

FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE

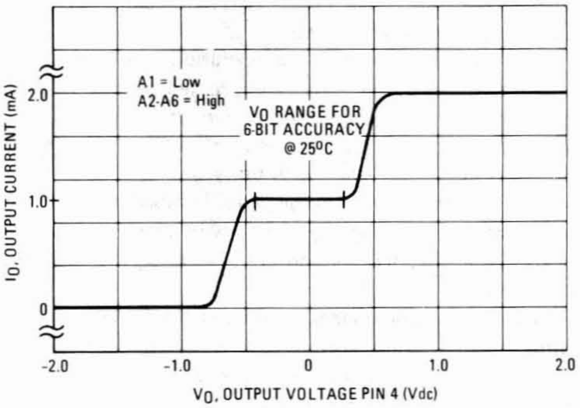


FIGURE 5 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE

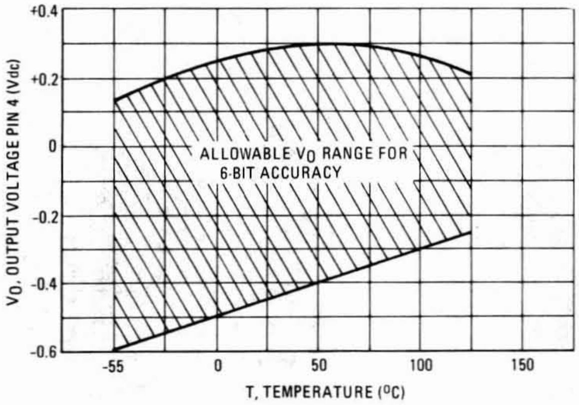


FIGURE 6 – POSITIVE $V_{ref}$

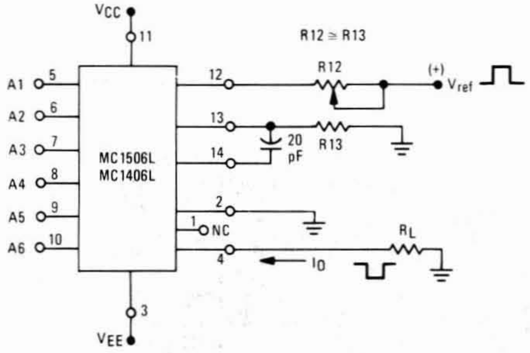

VCC
11
R12 ≅ R13
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
MC1506L
MC1406L
12
R12
(+) Vref
13
R13
20 pF
14
2
1 NC
4
IO
RL
3
VEE

FIGURE 7 – NEGATIVE $V_{ref}$

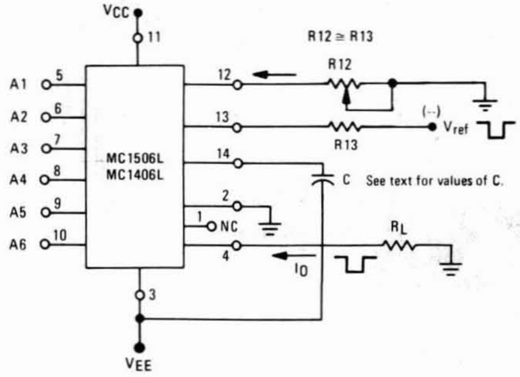
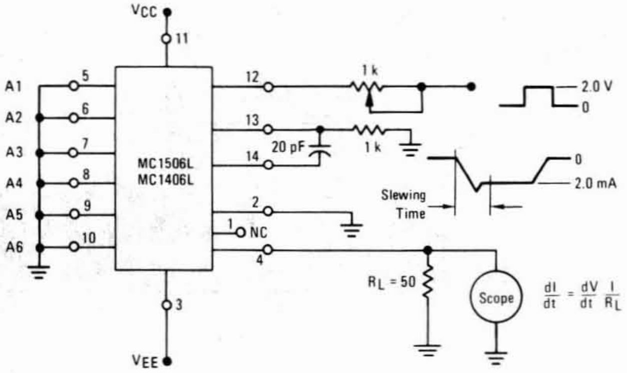
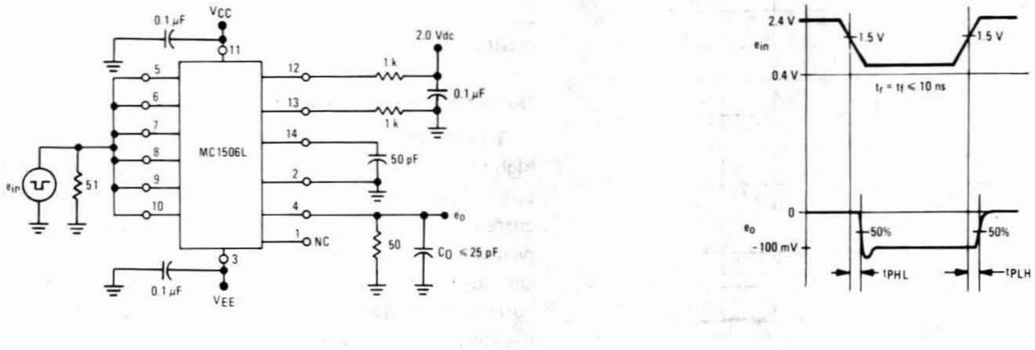

VCC
11
R12 ≅ R13
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
MC1506L
MC1406L
12
R12
13
R13
(–) Vref
14
C See text for values of C.
2
1 NC
4
IO
RL
3
VEE

FIGURE 8 – REFERENCE CURRENT SLEW RATE MEASUREMENT TEST CIRCUIT

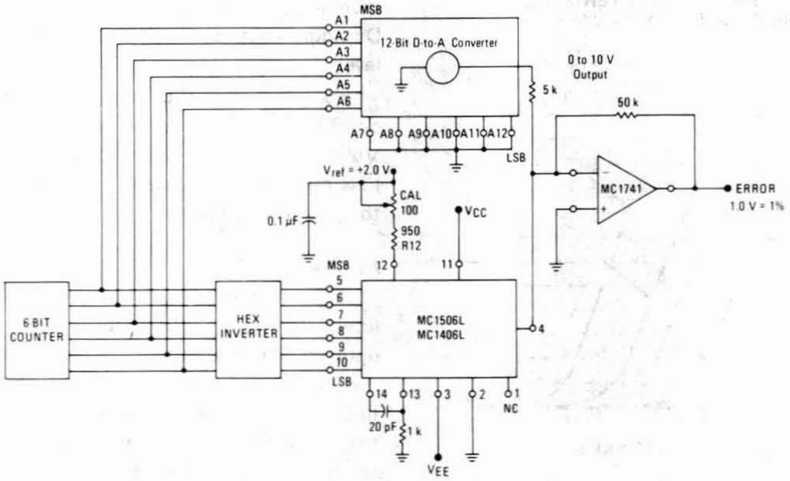

VCC
11
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
MC1506L
MC1406L
12
1 k
2.0 V
0
13
1 k
14
20 pF
0
2.0 mA
Slewing Time
2
1 NC
4
RL = 50
Scope
dI/dt = dV/dt 1/RL
3
VEE

## TEST CIRCUITS and TYPICAL CHARACTERISTICS (continued)

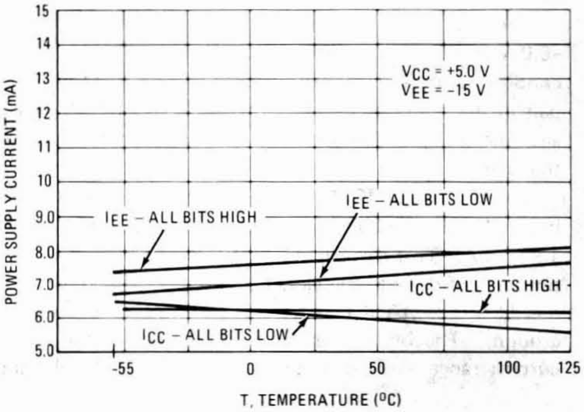
### FIGURE 9 – TRANSIENT RESPONSE


0.1 µF
VCC
11
2.0 Vdc
5
6
7
8
9
10
12
13
14
2
4
1
NC
1 k
1 k
0.1 µF
50 pF
MC1506L
e_in
51
50
e_o
C_O ≤ 25 pF
3
0.1 µF
VEE
2.4 V
e_in
1.5 V
1.5 V
0.4 V
t_r = t_f ≤ 10 ns
0
e_o
-100 mV
50%
50%
t_PHL
t_PLH

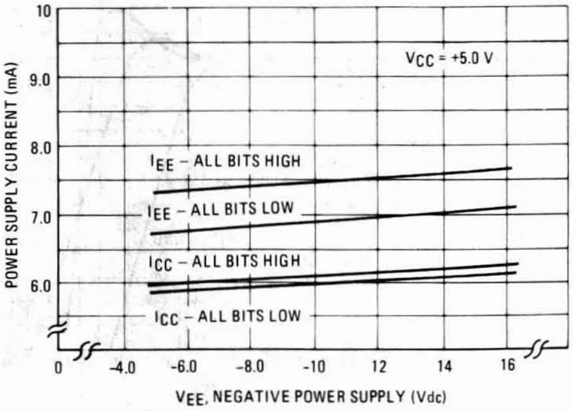
### FIGURE 10 – RELATIVE ACCURACY TEST CIRCUIT


MSB
A1
A2
A3
A4
A5
A6
12-Bit D-to-A Converter
0 to 10 V
Output
5 k
50 k
A7
A8
A9
A10
A11
A12
LSB
V_ref = +2.0 V
CAL
100
950
R12
0.1 µF
VCC
MC1741
ERROR
1.0 V = 1%
MSB
12
11
5
6
7
8
9
10
LSB
6 BIT
COUNTER
HEX
INVERTER
MC1506L
MC1406L
4
14
13
3
2
1
NC
20 pF
1 k
VEE

### FIGURE 11 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE



### FIGURE 12 – TYPICAL POWER SUPPLY CURRENT versus VEE



### TYPICAL CHARACTERISTICS (continued)

**FIGURE 13 – LOGIC INPUT CURRENT versus INPUT VOLTAGE**

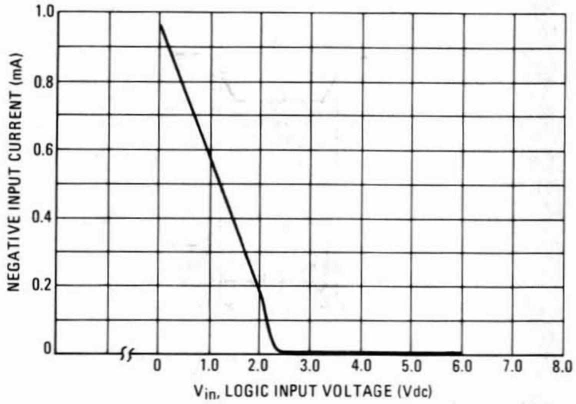


**FIGURE 14 – MSB TRANSFER CHARACTERISTICS versus TEMPERATURE (MSB IS "WORST CASE")**

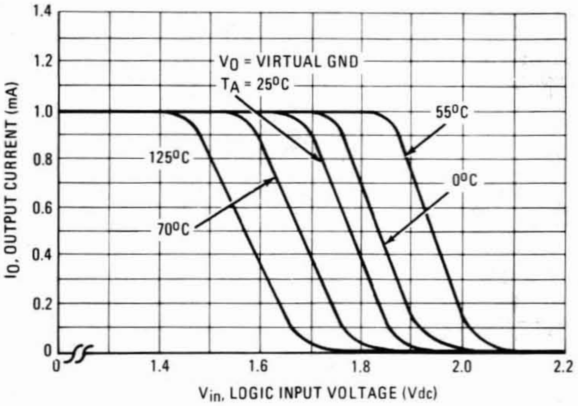
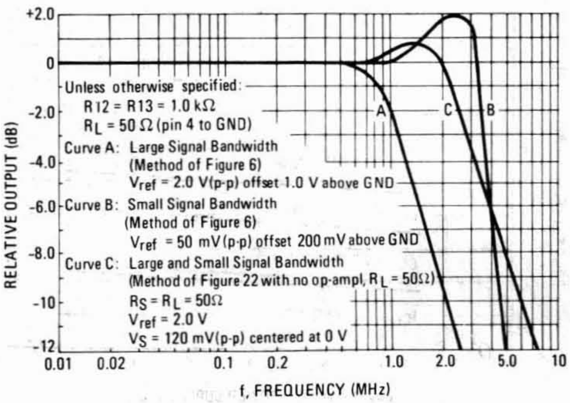


**FIGURE 15 – REFERENCE INPUT FREQUENCY RESPONSE**



### GENERAL INFORMATION

**Output Current Range**

The output current maximum rating of 4.2 mA may be used only for negative supply voltages below -6.0 volts, due to the increased voltage drop across the 400-ohm resistors in the reference current amplifier.

**Output Voltage Compliance**

The MC1506L current switches have been designed for high-speed operation and as a result have a restricted output voltage range, as shown in Figures 4 and 5. When a current switch is turned "off", the follower emitter is near ground and a positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington amplifier is one diode voltage below ground; thus a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

For example, at +25°C the allowable voltage compliance on Pin 4 to maintain six-bit accuracy is +0.1 to -0.3 Volts. With a full scale output current of 2.0 mA, the maximum resistor value that can be connected from Pin 4 to ground is 150 ohms.

**Accuracy**

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1506L is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current.

The best temperature performance is achieved with a -6.0 V supply and a reference voltage of -3.0 volts. These conditions match the voltage across the NPN current source pair in the reference amplifier at the lowest possible voltage, matching and optimizing the output impedance of the pair.

The MC1506L/MC1406L is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.969 mA. This corresponds to a reference amplifier output current drive to the ladder of 2.0 mA, with the loss of one LSB = 31 μA that is the ladder remainder shunted to ground. The input current to Pin 12 has a guaranteed current range value of between 1.9 to 2.1 mA, allowing

## GENERAL INFORMATION (continued)

some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 10. The 12-bit converter is calibrated for a full scale output current of 1.969 mA. This is an optional step since the MC1506L accuracy is essentially the same between 1.5 to 2.5 mA. Then the MC1506L full scale current is trimmed to the same value with R12 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 6-bit D-to-A converters may not be used to construct a 12-bit accurate D-to-A converter. 12-bit accuracy implies a total error of ±1/2 of one part in 4096, or ±0.012%, which is more accurate than the ±0.78% specification provided by the MC1506L.

### Multiplying Accuracy

The MC1506L may be used in the multiplying mode with six-bit accuracy when the reference current is varied over a range of 64:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions these six amplifiers can contribute a total of 6.0 $\mu$A extra current at the output terminal. If the reference current in the multiplying mode ranges from 60 $\mu$A to 4.0 mA, the 6.0 $\mu$A contributes an error of 0.1 LSB. This is well within six-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1506L is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

### Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a high-to-low transition for all bits. This time is typically 150 ns to within ±1/2 LSB, while the turn "off" is typically under 50 ns.

The slowest single switch is the least significant bit, which turns "on" and settles in 50 ns and turns "off" in 30 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 150 ns may be realized.

### Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at Pin 12 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I12, must always flow into Pin 12 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6. The reference voltage source supplies the full current I12. Compensation is accomplished by Miller feedback from Pin 14 to Pin 13. This compensation method yields the best slew rate, typically better than 2.0 mA/$\mu$s, and is independent of the value of R12. R13 must be used to establish the proper impedance for compensation at Pin 13. For bipolar reference signals, as in the multiplying mode, R13 can be tied to a negative voltage corresponding to the minimum input level. Another method is shown in Figure 22.

It is possible to eliminate R13 with only a small sacrifice in accuracy and temperature drift. For instance when high-speed operation is not needed, a capacitor is connected from pin 14 to $V_{EE}$. The capacitor value must be increased when R12 is made larger to maintain a proper phase margin. For R12 values of 1.0, 2.5, and 5.0 kilohms, minimum capacitor values are 50, 125, and 250 pF.

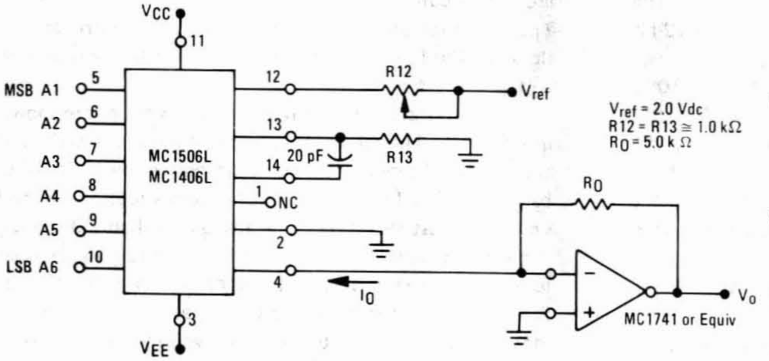
Connections for a negative reference voltage are shown in Figure 7. A high input impedance is the advantage of this method, but Miller feedback cannot be used because it feeds the input signal around the PNP directly into the high impedance node, causing slewing problems and high frequency peaking. Compensation involves a capacitor to $V_{EE}$ on Pin 14, using the values of the previous paragraph. The negative reference voltage must be at least 3.0 V above $V_{EE}$. Bipolar input signals may be handled by connecting R12 to a positive reference voltage equal to the peak positive input level at Pin 13.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0 V logic supply is not recommended as a reference voltage. If a well regulated 5.0 V supply which drives logic is to be used as the reference, R12 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 $\mu$F to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between Pin 12 and ground.

If Pin 12 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, thus decreasing the overall bandwidth.

## APPLICATIONS INFORMATION

FIGURE 16 – OUTPUT CURRENT VOLTAGE CONVERSION


VCC
11
MSB A1
A2
A3
A4
A5
LSB A6
5
6
7
8
9
10
MC1506L
MC1406L
12
13
14
1
2
4
R12
Vref
20 pF
R13
NC
$I_O$
RO
MC1741 or Equiv
Vo
3
VEE

$V_{ref} = 2.0$ Vdc
$R12 = R13 \cong 1.0\ k\Omega$
$R_O = 5.0\ k\ \Omega$

Theoretical $V_O$

$$V_O = \frac{V_{ref}}{R12}(R_O)\left(\frac{\bar{A}1}{2} + \frac{\bar{A}2}{4} + \frac{\bar{A}3}{8} + \frac{\bar{A}4}{16} + \frac{\bar{A}5}{32} + \frac{\bar{A}6}{64}\right) = K\ R_O \left\{ \bar{A} \right\}$$

Adjust $R_{ref}$ so that $V_O$ with all digital inputs at low level is equal to 9.844 volts.

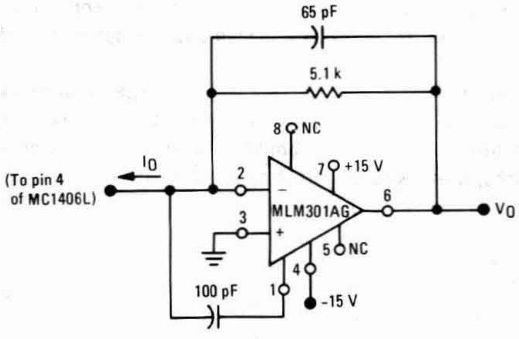
$$V_O = \frac{2\ V}{1\ K}(5\ K)\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64}\right) = 10\ V\left(\frac{63}{64}\right) = 9.844\ V$$

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1506L at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

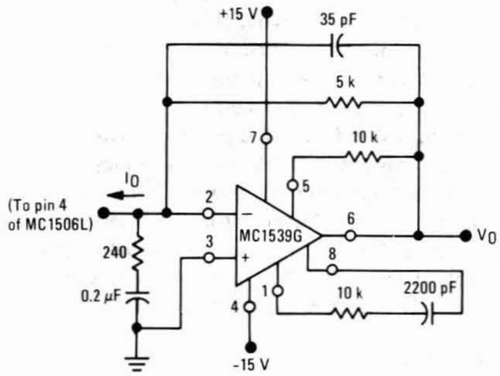
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 µs.

FIGURE 17

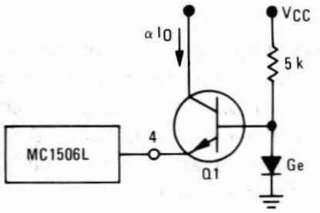

65 pF
5.1 k
8 NC
(To pin 4
of MC1406L)
$I_O$
2
3
7 +15 V
MLM301AG
6
Vo
5 NC
4
100 pF
1
-15 V

An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 µs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 18


+15 V
35 pF
5 k
7
10 k
$I_O$
5
(To pin 4
of MC1506L)
2
3
MC1539G
6
Vo
8
240
0.2 µF
4
1
10 k
2200 pF
-15 V

The positive voltage range may be extended by cascoding the output with a high beta common base transistor, Q1, as shown.


α IO
VCC
5 k
MC1506L
4
Q1
Ge

The output voltage range for this circuit is 0 volts to $BV_{CBO}$ of the transistor. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing.

## APPLICATIONS INFORMATION (continued)

### Combined Output Amplifier and Voltage Reference

For many of its applications the MC1506L requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current, see Figure 19. Instead of powering the MC1723G from a single positive voltage supply, it uses a negative bias as well. Although the reference voltage of the MC1723G is then developed with respect to that negative voltage it appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

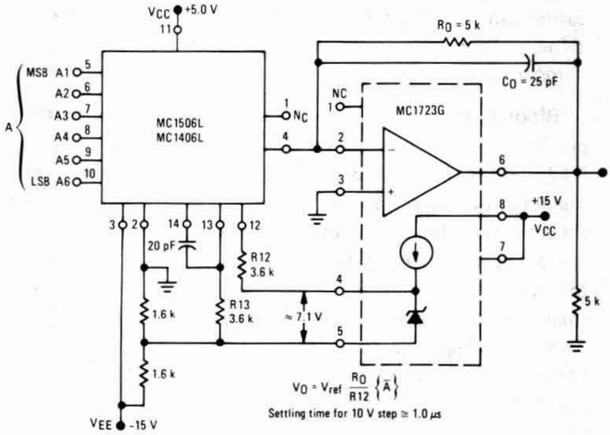
Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

Full scale output may be increased to as much as 32 volts by increasing $R_O$ and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. $C_O$ may be decreased to maintain the same $R_OC_O$ product if maximum speed is desired.

### Programmable Power Supply

The circuit of Figure 19 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +6.3 volts in 0.1-volt increments, ±0.05 volt; or 0 to 31.5 volts in 0.5-volt increments, ±0.25 volt.

FIGURE 19 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



$V_{CC}$ +5.0 V
11
MSB A1 5
A2 6
A3 7
A4 8
A5 9
LSB A6 10
A
MC1506L
MC1406L
1 NC
4
3 2 14 13 12
20 pF
R12 3.6 k
R13 3.6 k
1.6 k
1.6 k
≈ 7.1 V
$R_O$ = 5 k
$C_O$ = 25 pF
NC 1
MC1723G
2
3
4
5
6
7
8
+15 V
$V_{CC}$
5 k
$V_O$
$V_{EE}$ -15 V

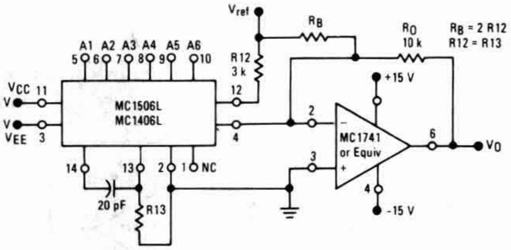
$$V_O = V_{ref}\,\frac{R_O}{R12}\left\{\bar{A}\right\}$$

Settling time for 10 V step ≅ 1.0 μs

### Bipolar or Negative Output Voltage

The circuit of Figure 20 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 6-bit "1's" complement offset binary. $V_{ref}$ may be used as this auxiliary reference. Note that $R_O$ has been doubled to 10 kilohms because of the anticipated 20 V (p-p) output range.

FIGURE 20 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



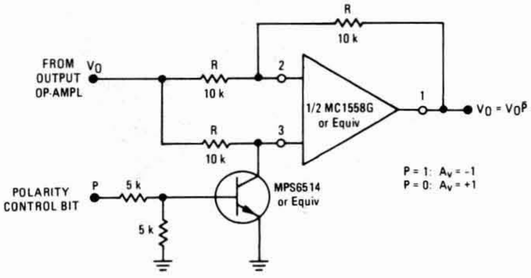
$V_{ref}$
$R_B$
$R_O$ 10 k
$R_B$ = 2 R12
R12 = R13
A1 A2 A3 A4 A5 A6
5 6 7 8 9 10
R12 3 k
12
$V_{CC}$ 11
+5 V
-15 V
$V_{EE}$ 3
MC1506L
MC1406L
4
14 13 2 1 NC
20 pF
R13
+15 V
2
3
MC1741 or Equiv
6
4
-15 V
$V_O$

$$V_O = \frac{V_{ref}}{R12}(R_O)\left(\frac{\bar{A}1}{2}+\frac{\bar{A}2}{4}+\frac{\bar{A}3}{8}+\frac{\bar{A}4}{16}+\frac{\bar{A}5}{32}+\frac{\bar{A}6}{64}\right)-\frac{V_{ref}}{R_B}(R_O)$$

### Polarity Switching Circuit, 6-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 21, gives 6-bits magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and -1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 21 – POLARITY SWITCHING CIRCUIT (6-Bit Magnitude Plus Sign D-to-A Converter)



R 10 k
FROM OUTPUT OP-AMPL $V_O$
R 10 k
R 10 k
2
3
1/2 MC1558G or Equiv
1
$V_O = V_O\bar{P} - V_OP$
POLARITY CONTROL BIT P
5 k
5 k
MPS6514 or Equiv
P = 1: $A_v$ = -1
P = 0: $A_v$ = +1

## APPLICATIONS INFORMATION (continued)

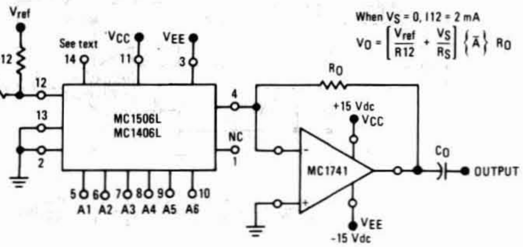
### Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1506L can be applied as a digital attenuator. See Figure 22. One advantage of this technique is that if $R_S$ = 50 ohms, no compensation capacitor is needed and a wide large signal bandwidth is achieved. The small and large signal bandwidths are now identical and are shown in Figure 15.

The best frequency response is obtained by not allowing $I_{12}$ to reach zero. $R_S$ can be set for a ±1.0 mA variation in relation to $I_{12}$. $I_{12}$ can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word that makes ac coupling necessary.

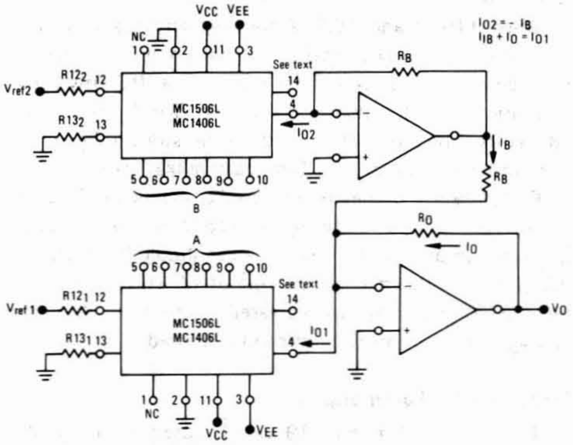
FIGURE 22 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT


Vref
R12
RS
VS
See text
VCC
VEE
14
11
3
12
13
2
MC1506L
MC1406L
4
NC
1
5 6 7 8 9 10
A1 A2 A3 A4 A5 A6
RO
+15 Vdc
VCC
MC1741
CO
OUTPUT
VEE
-15 Vdc

When $V_S = 0$, $I12 = 2$ mA

$$V_O = \left[\frac{V_{ref}}{R12} + \frac{V_S}{R_S}\right]\left\{\bar{A}\right\} R_O$$

FIGURE 24 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION


VCC VEE
NC
1 2 11 3
See text
14
4
Vref2
R12₂ 12
R13₂ 13
MC1506L
MC1406L
IO2
5 6 7 8 9 10
B
IO2 = - IB
IB + IO = IO1
RB
IB
RB
RO
IO
A
5 6 7 8 9 10
See text
14
Vref1
R12₁ 12
R13₁ 13
MC1506L
MC1406L
IO1
4
VO
1 2 11 3
NC
VCC
VEE

$$I_O = I_{O1} - I_{O2} = \frac{V_{ref1}}{R12_1}\left\{\bar{A}\right\} - \frac{V_{ref2}}{R12_2}\left\{\bar{B}\right\}$$

Digital Subtraction:

let $\frac{V_{ref1}}{R12_1} = \frac{V_{ref2}}{R12_2}$

$$V_O = \frac{V_{ref1}}{R12_1} R_O \left[\left\{\bar{A}\right\} - \left\{\bar{B}\right\}\right]$$

Programmable Amplifier:

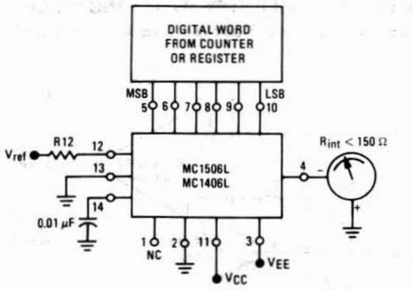
Connect digital inputs so A = B

$$V_O = \left\{\bar{A}\right\}\left[\frac{V_{ref1}}{R12_1} - \frac{V_{ref2}}{R12_2}\right]$$

### Panel Meter Readout

The MC1506L can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R12 or $V_{ref}$.

FIGURE 23 – PANEL METER READOUT CIRCUIT

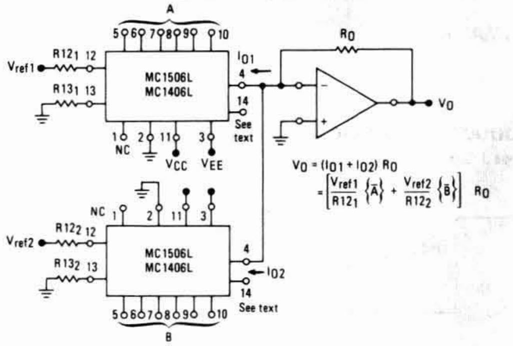

DIGITAL WORD
FROM COUNTER
OR REGISTER
MSB
LSB
5 6 7 8 9 10
Vref
R12
12
13
14
0.01 μF
MC1506L
MC1406L
Rint < 150 Ω
4
1 2 11 3
NC
VCC
VEE

This digital subtraction application is useful for indicating when one digital word is approaching another in value. More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods, or applied differentially to $R12_1$ and $R12_2$ or $R13_1$ and $R13_2$. $V_O$ will be a bipolar signal defined by the above equation. Note that the circuit shown accepts bipolar differential signals but does not have a negative common-mode range. A very useful method is to connect $R12_1$ and $R12_2$ to a positive reference higher than the most positive input, and drive $R13_1$ and $R13_2$. This yields high input impedance, bipolar differential and common-mode range. The compensation depends on the input method used, as shown in previous sections.

## APPLICATIONS INFORMATION (continued)

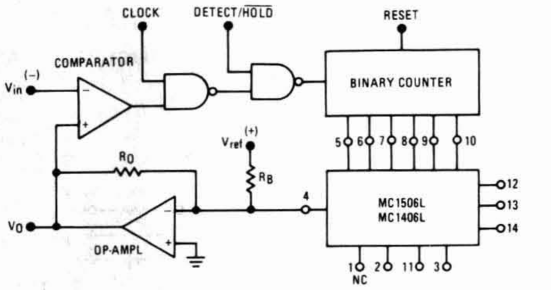
### FIGURE 25 – DIGITAL SUMMING and CHARACTER GENERATION


A
5 6 7 8 9 10
Vref1
R12₁ 12
R13₁ 13
MC1506L
MC1406L
IO1
4
14
See text
1 2 11 3
NC
VCC VEE
RO
VO
VO = (IO1 + IO2) RO
= [Vref1/R12₁ {Ā} + Vref2/R12₂ {B̄}] RO
NC 1 2 11 3
Vref2
R12₂ 12
R13₂ 13
MC1506L
MC1406L
4
IO2
14
See text
5 6 7 8 9 10
B

In a character generation system one MC1506L circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 12-bit D-to-A converter (see Accuracy Section).

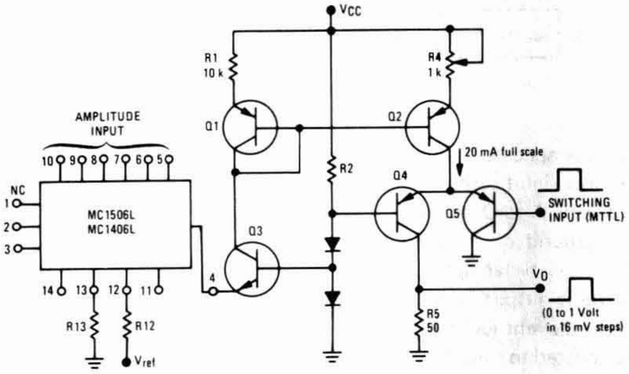
### FIGURE 26 – PEAK DETECTING SAMPLE and HOLD

**(Features infinite hold time and optional digital output.)**


CLOCK
DETECT/HOLD
RESET
COMPARATOR
(–)
Vin
BINARY COUNTER
5 6 7 8 9 10
(+)
Vref
RO
RB
4
VO
OP-AMPL
MC1506L
MC1406L
12
13
14
1 2 11 3
NC

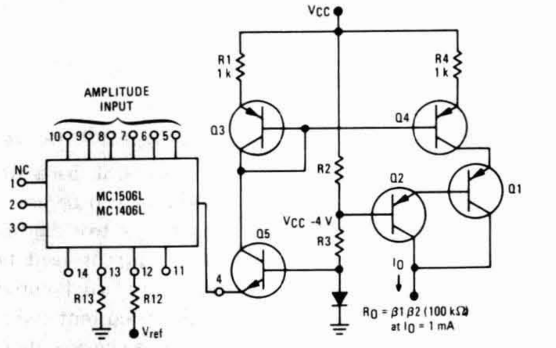
Positive peaks may be detected by inserting a hex inverter between the counter and MC1506L, reversing the comparator inputs, and connecting the output amplifier for unipolar operation.

### FIGURE 27 – PROGRAMMABLE PULSE GENERATOR


VCC
R1
10 k
R4
1 k
AMPLITUDE INPUT
Q1
Q2
20 mA full scale
10 9 8 7 6 5
R2
Q4
NC
1
2
3
MC1506L
MC1406L
Q5
SWITCHING INPUT (MTTL)
Q3
4
VO
14 13 12 11
R13
R12
Vref
R5
50
(0 to 1 Volt in 16 mV steps)

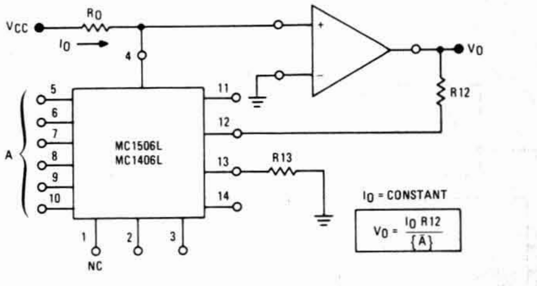
Fast rise and fall times require the use of high speed switching transistors for the differential pair, Q4 and Q5. Linear ramps and sine waves may be generated by the appropriate reference input.

### FIGURE 28 – PROGRAMMABLE CONSTANT CURRENT SOURCE


VCC
R1
1 k
R4
1 k
AMPLITUDE INPUT
10 9 8 7 6 5
Q3
Q4
NC
1
2
3
MC1506L
MC1406L
R2
Q2
Q1
VCC -4 V
R3
Q5
14 13 12 11
R13
R12
Vref
4
IO
RO = β1 β2 (100 kΩ) at IO = 1 mA

Current pulses, ramps, staircases, and sine waves may be generated by the appropriate digital and reference inputs. This circuit is especially useful in curve tracer applications.

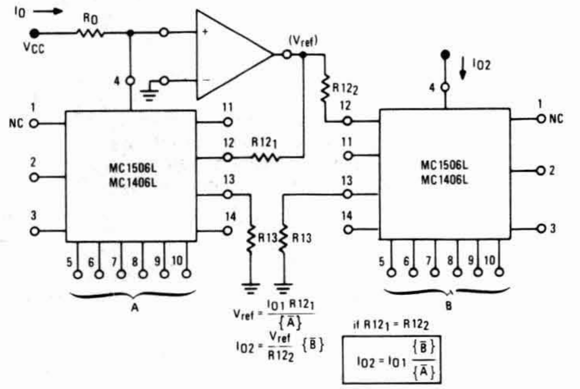
### FIGURE 29 – ANALOG DIVISION BY DIGITAL WORD


VCC
RO
IO
4
VO
5
6
7
8
9
10
A
MC1506L
MC1406L
11
12
R12
13
R13
14
1 2 3
NC
IO = CONSTANT
VO = IO R12 / {Ā}

This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation, $I_O$ can be set at 62 μA so that $I_{12}$ will have a maximum value of 3.938 mA for a digital bit input configuration of 111110.

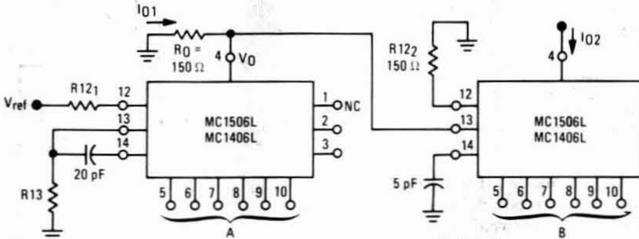
Compensation is necessary for loop stability and depends on the type of operational amplifier used. If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If this cannot be done, the reference amplifier can furnish the dominant pole with extra Miller feedback from pin 14 to 13. If the MC1723 or another wideband amplifier is used, the reference amplifier should always be overcompensated.

### FIGURE 30 – ANALOG QUOTIENT OF TWO DIGITAL WORDS


IO
RO
VCC
(Vref)
IO2
4
R12₂
4
1
NC
MC1506L
MC1406L
11
12 R12₁
13
14
R13
R13
2
3
5 6 7 8 9 10
A
12
11
13
14
MC1506L
MC1406L
1
NC
2
3
5 6 7 8 9 10
B
Vref = IO1 R12₁ / {Ā}
IO2 = Vref / R12₂ {B̄}
if R12₁ = R12₂
IO2 = IO1 {B̄}/{Ā}

## APPLICATIONS INFORMATION (continued)

**FIGURE 31 – ANALOG PRODUCT OF TWO DIGITAL WORDS (High-Speed Operation)**


$I_{01}$
$R_0 = 150\ \Omega$
4
$V_0$
$R12_1$
12
13
14
$V_{ref}$
20 pF
R13
MC1506L
MC1406L
1
NC
2
3
5 6 7 8 9 10
A
$R12_2$
150 Ω
4
$I_{02}$
12
13
14
5 pF
MC1506L
MC1406L
NC
2
3
5 6 7 8 9 10
B

$$V_0 = I_{01} R_0 = \frac{V_{ref1}}{R12_1} \left\{\bar{A}\right\} R_0$$

$$I_{02} = -\frac{\left\{\bar{B}\right\} |V_0|}{R12_2}$$

$$= \frac{\left\{\bar{B}\right\}}{R12_2} \left[R_0 \left(\frac{V_{ref1}}{R12_1}\right) \left\{\bar{A}\right\}\right]$$

since $R_0 = R12_2$ and $K = V_{ref}/R12_1$

$$\boxed{I_{02} = K\left\{\bar{A}\right\}\left\{\bar{B}\right\}}$$

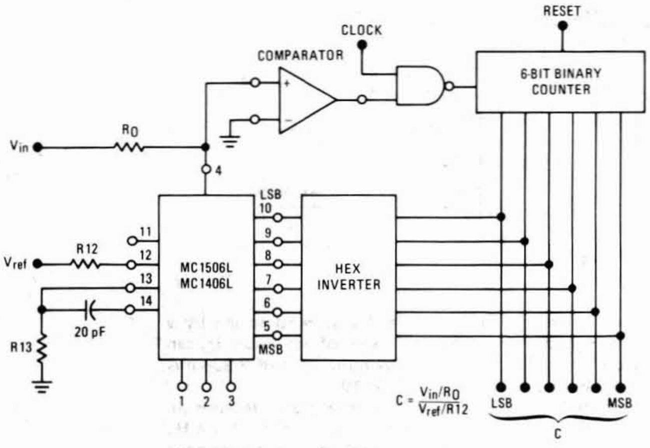
K can be an analog variable.

### Two Digit BCD Conversion

MC1506L parts which meet the specification for 7-bit accuracy can be used for the most significant word when building a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten.

**FIGURE 32 – DIGITAL QUOTIENT of TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION**

The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.


RESET
CLOCK
COMPARATOR
+
–
6-BIT BINARY COUNTER
$V_{in}$
$R_0$
4
LSB
10
9
8
7
6
5
MSB
11
12
13
14
R12
$V_{ref}$
20 pF
R13
MC1506L
MC1406L
HEX INVERTER
1 2 3
LSB
MSB
C

$$C = \frac{V_{in}/R_0}{V_{ref}/R12}$$

**MOTOROLA**

# MC1408
# MC1508

## Specifications and Applications Information

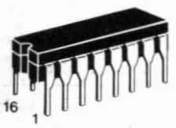
EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

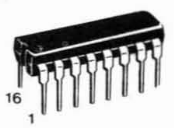
### EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

- Eight-Bit Accuracy Available in Both Temperature Ranges Relative Accuracy: ±0.19% Error maximum (MC1408L8, MC1408P8, MC1508L8)
- Seven and Six-Bit Accuracy Available with MC1408 Designated by 7 or 6 Suffix after Package Suffix
- Fast Settling Time – 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing – +0.4 V to -5.0 V
- High-Speed Multiplying Input Slew Rate 4.0 mA/µs
- Standard Supply Voltages: +5.0 V and -5.0 V to -15 V



**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02



**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

**D SUFFIX**
PLASTIC PACKAGE
CASE 751B-01
SO-16*

***Surface Mount pin-out is different than standard package pin-out for this device. Please refer to Chapter 7 for details.**

FIGURE 1 – D-to-A TRANSFER CHARACTERISTICS

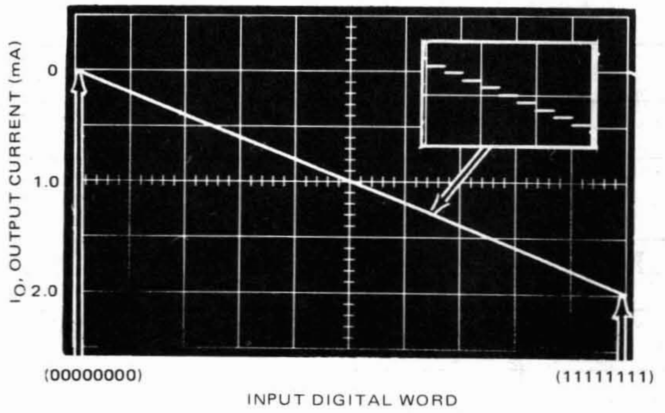
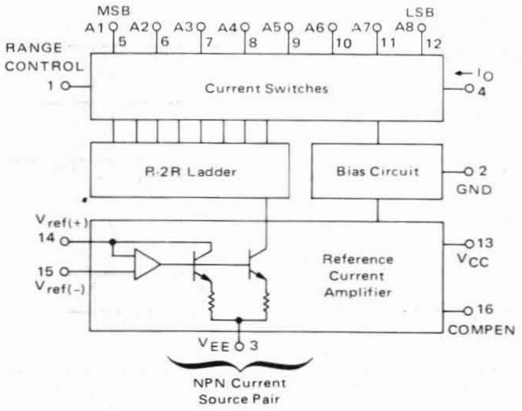


FIGURE 2 – BLOCK DIAGRAM


MSB
LSB
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
RANGE CONTROL
1
Current Switches
I_O
4
R-2R Ladder
Bias Circuit
2
GND
Vref(+)
14
15
Vref(-)
Reference Current Amplifier
13
VCC
16
COMPEN
VEE
3
NPN Current Source Pair

### TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +5.5<br>-16.5 | Vdc |
| Digital Input Voltage | $V_5$ thru $V_{12}$ | 0 to +5.5 | Vdc |
| Applied Output Voltage | $V_O$ | +0.5,-5.2 | Vdc |
| Reference Current | $I_{14}$ | 5.0 | mA |
| Reference Amplifier Inputs | $V_{14}, V_{15}$ | $V_{CC}, V_{EE}$ | Vdc |
| Operating Temperature Range<br>MC1508<br>MC1408 Series | $T_A$ | <br>-55 to +125<br>0 to +75 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

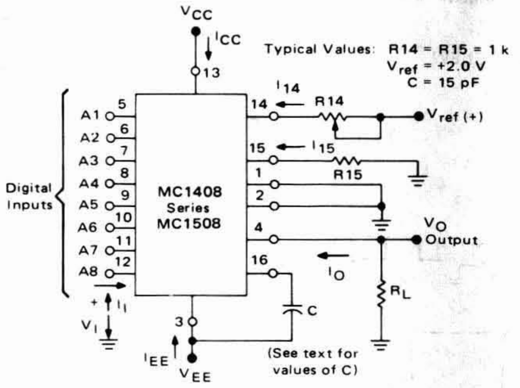
**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $V_{EE}$ = -15 Vdc, $\frac{Vref}{R14}$ = 2.0 mA, MC1508L8: $T_A$ = -55°C to +125°C. MC1408L Series: $T_A$ = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Relative Accuracy (Error relative to full scale $I_O$)<br>MC1508L8, MC1408L8, MC1408P8<br>MC1408P7, MC1408L7, See Note 1<br>MC1408P6, MC1408L6, See Note 1 | 4 | $E_r$ | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>±0.19<br>±0.39<br>±0.78 | % |
| Settling Time to within ±1/2 LSB [includes $t_{PLH}$] ($T_A$=+25°C) See Note 2 | 5 | $t_S$ | – | 300 | – | ns |
| Propagation Delay Time<br>$T_A$ = +25°C | 5 | $t_{PLH}, t_{PHL}$ | – | 30 | 100 | ns |
| Output Full Scale Current Drift | | $TCI_O$ | – | - 20 | – | PPM/°C |
| Digital Input Logic Levels (MSB)<br>High Level, Logic "1"<br>Low Level, Logic "0" | 3 | <br>$V_{IH}$<br>$V_{IL}$ | <br>2.0<br>– | <br>–<br>– | <br>–<br>0.8 | Vdc |
| Digital Input Current (MSB)<br>High Level, $V_{IH}$ = 5.0 V<br>Low Level, $V_{IL}$ = 0.8 V | 3 | <br>$I_{IH}$<br>$I_{IL}$ | <br>–<br>– | <br>0<br>-0.4 | <br>0.04<br>-0.8 | mA |
| Reference Input Bias Current (Pin 15) | 3 | $I_{15}$ | – | -1.0 | -5.0 | µA |
| Output Current Range<br>$V_{EE}$ = -5.0 V<br>$V_{EE}$ = -15 V, $T_A$ = 25°C | 3 | $I_{OR}$ | <br>0<br>0 | <br>2.0<br>2.0 | <br>2.1<br>4.2 | mA |
| Output Current<br>$V_{ref}$ = 2.000 V, R14 = 1000 Ω | 3 | $I_O$ | <br>1.9 | <br>1.99 | <br>2.1 | mA |
| Output Current<br>(All bits low) | 3 | $I_{O(min)}$ | – | 0 | 4.0 | µA |
| Output Voltage Compliance ($E_r \leq$ 0.19% at $T_A$ = +25°C)<br>Pin 1 grounded<br>Pin 1 open, $V_{EE}$ below -10 V | 3 | $V_O$ | <br>–<br>– | <br>–<br>– | <br>-0.55, +0.4<br>-5.0, +0.4 | Vdc |
| Reference Current Slew Rate | 6 | SR $I_{ref}$ | – | 4.0 | – | mA/µs |
| Output Current Power Supply Sensitivity | | PSRR(–) | – | 0.5 | 2.7 | µA/V |
| Power Supply Current<br>(All bits low) | 3 | $I_{CC}$<br>$I_{EE}$ | –<br>– | +13.5<br>-7.5 | +22<br>-13 | mA |
| Power Supply Voltage Range<br>($T_A$ = +25°C) | 3 | $V_{CCR}$<br>$V_{EER}$ | +4.5<br>-4.5 | +5.0<br>-15 | +5.5<br>-16.5 | Vdc |
| Power Dissipation<br>All bits low<br>$V_{EE}$ = -5.0 Vdc<br>$V_{EE}$ = -15 Vdc<br>All bits high<br>$V_{EE}$ = -5.0 Vdc<br>$V_{EE}$ = -15 Vdc | 3 | $P_D$ | <br><br>–<br>–<br><br>–<br>– | <br><br>105<br>190<br><br>90<br>160 | <br><br>170<br>305<br><br>–<br>– | mW |

Note 1. All current switches are tested to guarantee at least 50% of rated output current.
Note 2. All bits switched.

## TEST CIRCUITS

### FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT


VCC
ICC
13
Typical Values: R14 = R15 = 1 k
Vref = +2.0 V
C = 15 pF
I14
14
R14
Vref (+)
15
I15
R15
1
2
4
16
VO
Output
IO
RL
C
(See text for values of C)
Digital Inputs
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
A8 12
MC1408 Series MC1508
II
VI
3
IEE
VEE

$V_I$ and $I_I$ apply to inputs A1 thru A8

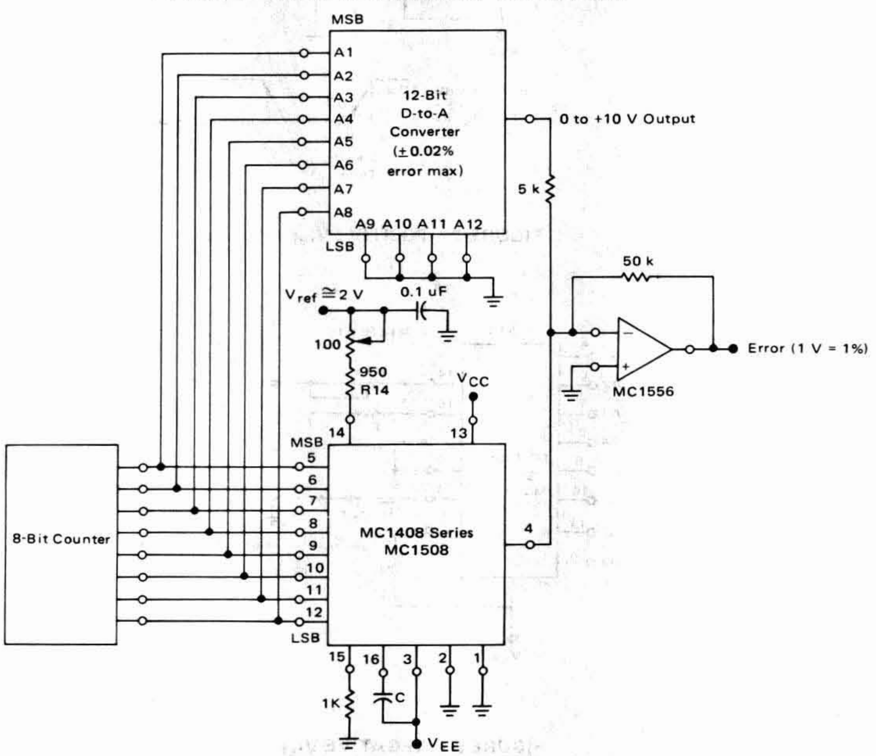
The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right\}$$

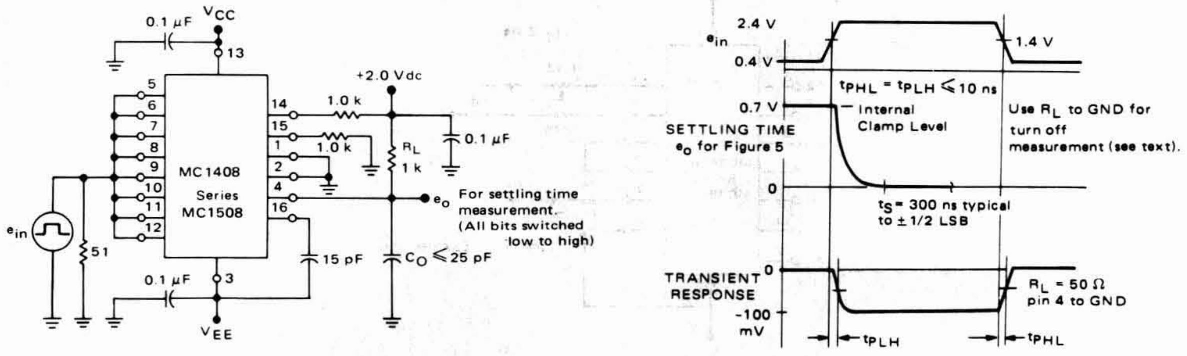
where $K \cong \frac{V_{ref}}{R14}$

and $A_N$ = "1" if $A_N$ is at high level
$A_N$ = "0" if $A_N$ is at low level

### FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

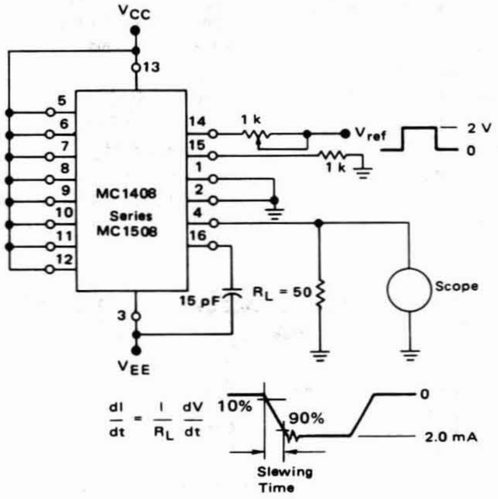

MSB
A1
A2
A3
A4
A5
A6
A7
A8
LSB
A9 A10 A11 A12
12-Bit D-to-A Converter (±0.02% error max)
0 to +10 V Output
5 k
50 k
Error (1 V = 1%)
MC1556
Vref ≅ 2 V
0.1 uF
100
950
R14
VCC
14
13
MSB
5
6
7
8
9
10
11
12
LSB
8-Bit Counter
MC1408 Series MC1508
4
15
16
3
2
1
1K
C
VEE

### FIGURE 5 – TRANSIENT RESPONSE and SETTLING TIME

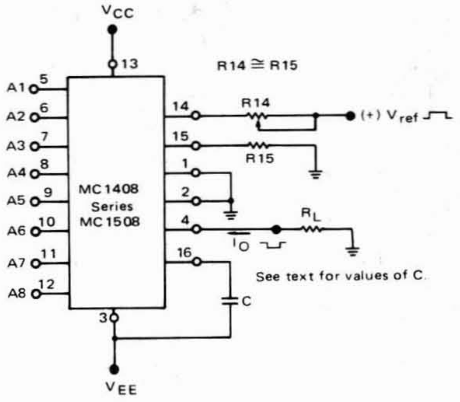

0.1 µF
VCC
13
5
6
7
8
9
10
11
12
MC1408 Series MC1508
14
15
1
2
4
16
1.0 k
1.0 k
+2.0 Vdc
RL 1 k
0.1 µF
eo
For settling time measurement. (All bits switched low to high)
15 pF
CO ≤ 25 pF
0.1 µF
3
VEE
ein
51
2.4 V
ein
0.4 V
1.4 V
tPHL = tPLH ≤ 10 ns
0.7 V
Internal Clamp Level
Use RL to GND for turn off measurement (see text).
SETTLING TIME
eo for Figure 5
0
tS = 300 ns typical to ± 1/2 LSB
TRANSIENT RESPONSE
0
-100 mV
RL = 50 Ω
pin 4 to GND
tPLH
tPHL

## TEST CIRCUITS (continued)

### FIGURE 6 – REFERENCE CURRENT SLEW RATE MEASUREMENT


VCC
13
5
6
7
8
9
10
11
12
MC1408
Series
MC1508
14
15
1
2
4
16
3
1 k
1 k
Vref
2 V
0
15 pF
RL = 50
Scope
VEE
$\frac{dI}{dt} = \frac{I}{R_L}\frac{dV}{dt}$
10%
90%
0
2.0 mA
Slewing
Time

### FIGURE 7 – POSITIVE $V_{ref}$


VCC
13
R14 ≅ R15
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
MC1408
Series
MC1508
14
15
1
2
4
16
3
R14
R15
(+) Vref
RL
IO
See text for values of C.
C
VEE

### FIGURE 8 – NEGATIVE $V_{ref}$

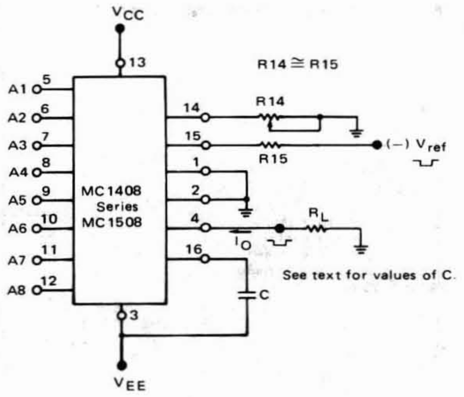
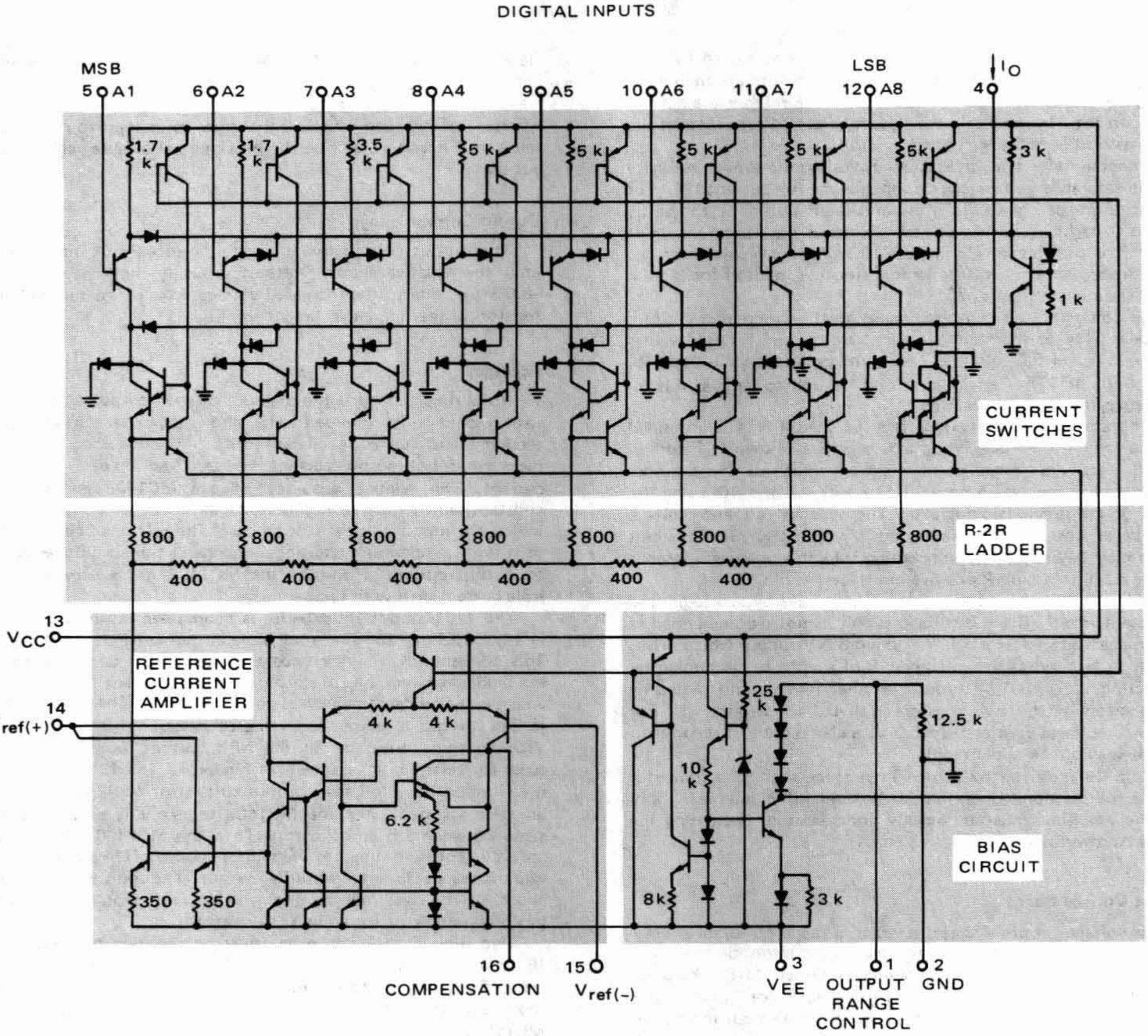

VCC
13
R14 ≅ R15
A1
A2
A3
A4
A5
A6
A7
A8
5
6
7
8
9
10
11
12
MC1408
Series
MC1508
14
15
1
2
4
16
3
R14
R15
(–) Vref
RL
IO
See text for values of C.
C
VEE

FIGURE 9 – MC1408, MC1508 SERIES EQUIVALENT CIRCUIT SCHEMATIC


DIGITAL INPUTS
MSB
5 A1
6 A2
7 A3
8 A4
9 A5
10 A6
11 A7
LSB
12 A8
4
$I_O$
1.7 k
1.7 k
3.5 k
5 k
5 k
5 k
5 k
5k
3 k
1 k
CURRENT SWITCHES
800
800
800
800
800
800
800
800
400
400
400
400
400
400
R-2R LADDER
13
$V_{CC}$
14
$V_{ref(+)}$
REFERENCE CURRENT AMPLIFIER
4 k
4 k
6.2 k
350
350
25 k
12.5 k
10 k
8k
3 k
BIAS CIRCUIT
16
COMPENSATION
15
$V_{ref(-)}$
3
$V_{EE}$
1
OUTPUT RANGE CONTROL
2
GND

## CIRCUIT DESCRIPTION

The MC1408 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

## GENERAL INFORMATION

### Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift. Another method for bipolar inputs is shown in Figure 25.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor should be tied to $V_{EE}$ as this increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to $V_{EE}$ on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0-volts above the $V_{EE}$ supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 µF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

### Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.55 to +0.4 volts at +25°C, due to the current switching methods employed in the MC1408. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1408 may be extended to -5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of $R_L$ up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.2 µs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

### Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages typically more negative than -8.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

### Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1408 has a very low full scale current drift with temperature.

The MC1408/MC1508 Series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 µA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC1408 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the MC1408x8.

### Multiplying Accuracy

The MC1408 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions, these eight amplifiers can contribute a total of 1.6 µA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 µA to 4.0 mA, the 1.6 µA contributes an error of 0.1 LSB. This is well within eight-bit accuracy referenced to 4.0 mA.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1408 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

## GENERAL INFORMATION (Continued)

**Settling Time**

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leqslant 500$ ohms and $C_O \leqslant 25$ pF.

The slowest single switch is the least significant bit, which turns "on" and settles in 250 ns and turns "off" in 80 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 300 ns may be realized. Bit A7 turns "on" in 200 ns and "off" in 80 ns, while bit A6 turns "on" in 150 ns and "off" in 80 ns.

The test circuit of Figure 5 requires a smaller voltage swing for the current switches due to internal voltage clamping in the MC1408. A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 µF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +5.0 V, $V_{EE}$ = -15 V, $T_A$ = +25°C unless otherwise noted.)

FIGURE 10 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

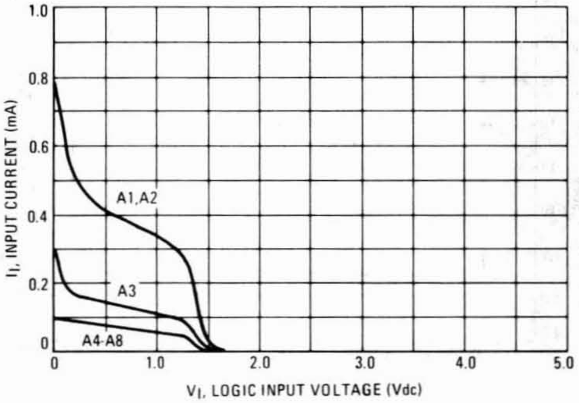


FIGURE 11 – TRANSFER CHARACTERISTIC versus TEMPERATURE (A5 thru A8 thresholds lie within range for A1 thru A4)

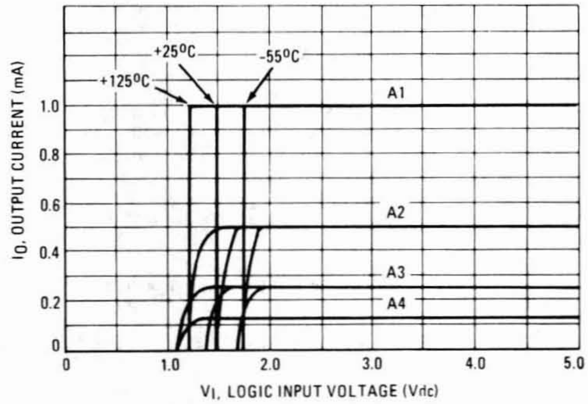


FIGURE 12 – OUTPUT CURRENT versus OUTPUT VOLTAGE (See text for pin 1 restrictions)

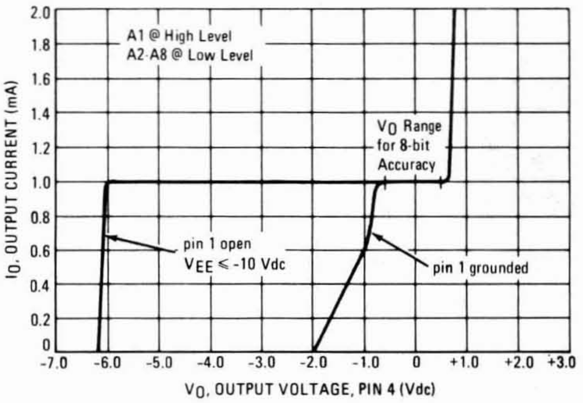
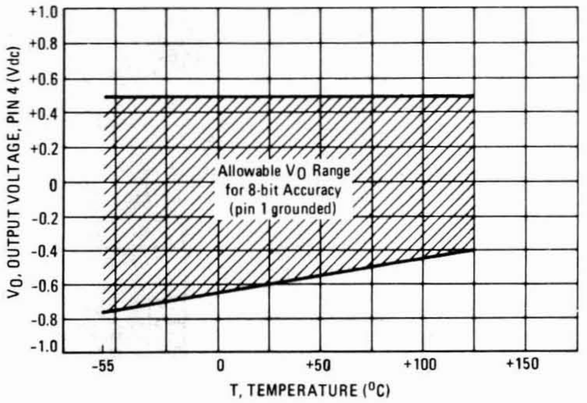


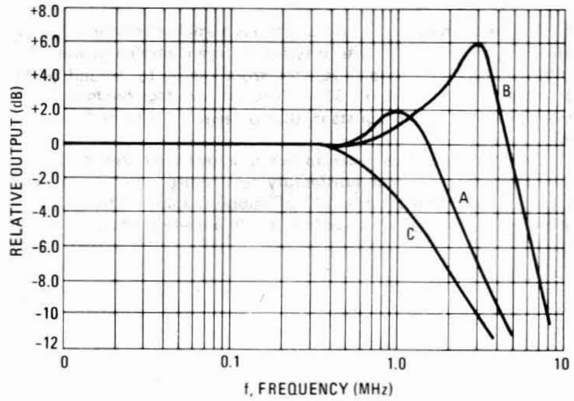
FIGURE 13 – OUTPUT VOLTAGE versus TEMPERATURE (Negative range with pin 1 open is -5.0 Vdc over full temperature range)



## TYPICAL CHARACTERISTICS (continued)

($V_{CC}$ = +5.0 V, $V_{EE}$ = −15 V, $T_A$ = +25°C unless otherwise noted.)

### FIGURE 14 – REFERENCE INPUT FREQUENCY RESPONSE



Unless otherwise specified:

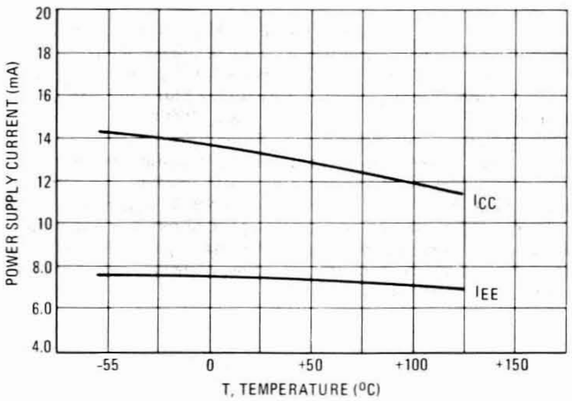
R14 = R15 = 1.0 kΩ
C = 15 pF, pin 16 to $V_{EE}$
$R_L$ = 50 Ω, pin 4 to GND

Curve A: Large Signal Bandwidth
Method of Figure 7
$V_{ref}$ = 2.0 V(p-p) offset 1.0 V above GND

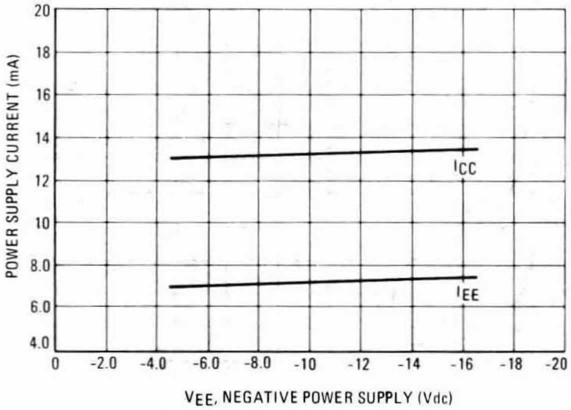
Curve B: Small Signal Bandwidth
Method of Figure 7 $R_L$ = 250 Ω
$V_{ref}$ = 50 mV(p-p) offset 200 mV above GND

Curve C: Large and Small Signal Bandwidth
Method of Figure 25 (no op-ampl, $R_L$ = 50 Ω)
$R_S$ = 50 Ω
$V_{ref}$ = 2.0 V
$V_S$ = 100 mV(p-p) centered at 0 V

### FIGURE 15 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE (all bits low)

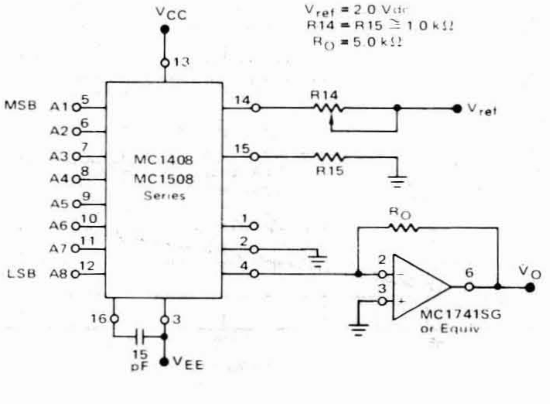


### FIGURE 16 – TYPICAL POWER SUPPLY CURRENT versus $V_{EE}$ (all bits low)



## APPLICATIONS INFORMATION

### FIGURE 17 – OUTPUT CURRENT TO VOLTAGE CONVERSION


VCC
Vref = 2.0 Vdc
R14 = R15 ≅ 1.0 kΩ
RO = 5.0 kΩ
13
MSB A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
LSB A8 12
MC1408
MC1508
Series
14
R14
Vref
15
R15
1
2
4
RO
2
3
6
VO
MC1741SG
or Equiv
16
3
15 pF
VEE

Theoretical $V_O$

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust $V_{ref}$, R14 or $R_O$ so that $V_O$ with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\text{ V}}{1\text{ k}}(5\text{ k})\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\text{ V}\left[\frac{255}{256}\right] = 9.961\text{ V}$$

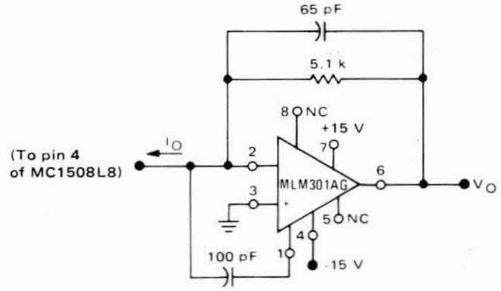
## APPLICATIONS INFORMATION (continued)

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1408 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

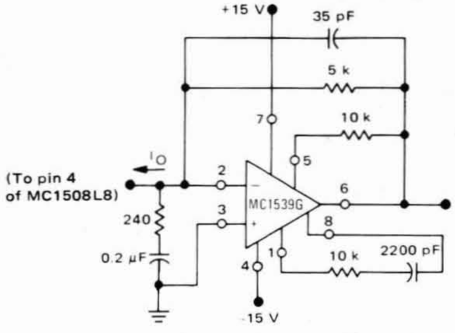
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 µs.

FIGURE 18



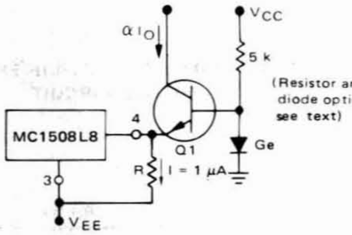
An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 µs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 19



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 20 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to $BV_{CBO}$ of the transistor. If pin 1 is left open, the transistor base may be grounded, eliminating both the resistor and the diode. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because pin 4 is held at a constant voltage. The resistor (R) to $V_{EE}$ maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

### Combined Output Amplifier and Voltage Reference

For many of its applications the MC1408 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current. See Figure 21. The MC1723G uses both a positive and negative power supply. The reference voltage of the MC1723G is then developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

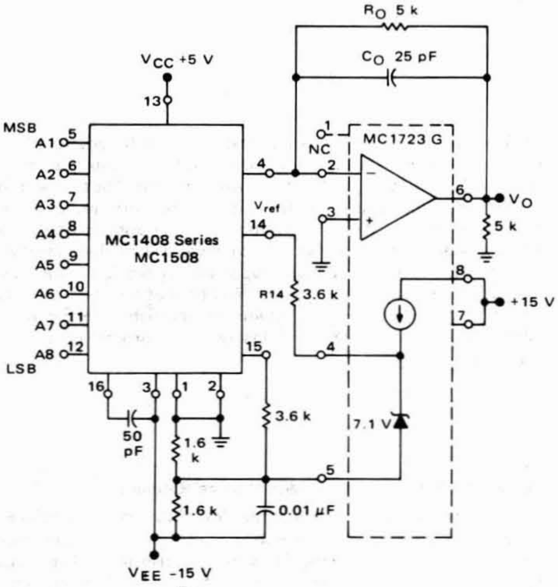
Full scale output may be increased to as much as 32 volts by increasing $R_O$ and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. $C_O$ may be decreased to maintain the same $R_OC_O$ product if maximum speed is desired.

## APPLICATIONS INFORMATION (continued)

**Programmable Power Supply**

The circuit of Figure 21 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +25.5 volts in 0.1-volt increments, ±0.05 volt; or 0 to 5.1 volts in 20 mV increments, ±10 mV.

FIGURE 21 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



$R_O$ 5 k
$C_O$ 25 pF
$V_{CC}$ +5 V
13
MSB
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
A8 12
LSB
MC1408 Series
MC1508
4
$V_{ref}$
14
15
16
3
1
2
NC
MC1723 G
$V_O$
5 k
+15 V
R14 3.6 k
3.6 k
7.1 V
50 pF
1.6 k
1.6 k
0.01 µF
$V_{EE}$ -15 V

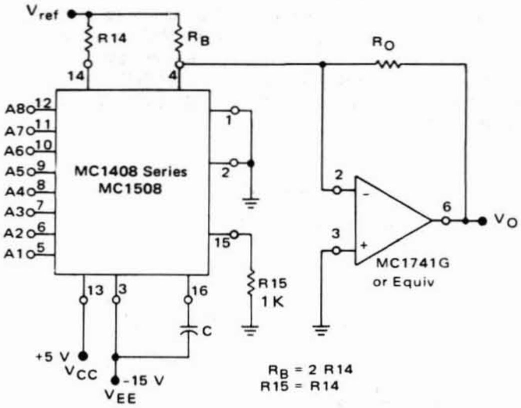
$$V_O = V_{ref} = \frac{R_O}{R14}\{A\}$$

Settling time for a 10-volt step ≅ 1.0 µs

**Bipolar or Negative Output Voltage**

The circuit of Figure 22 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 8-bit "1's" complement offset binary. $V_{ref}$ may be used as this auxiliary reference. Note that $R_O$ has been doubled to 10 kilohms because of the anticipated 20 V(p-p) output range.

FIGURE 22 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT

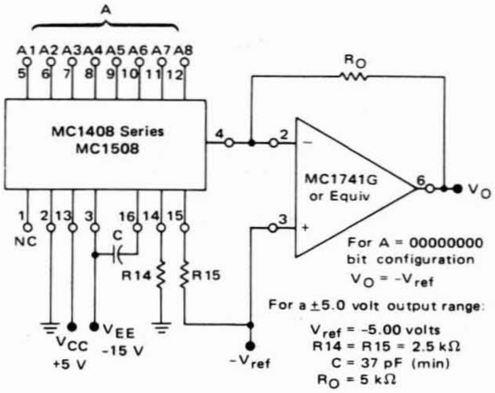


$V_{ref}$
R14
$R_B$
$R_O$
14
4
A8 12
A7 11
A6 10
A5 9
A4 8
A3 7
A2 6
A1 5
MC1408 Series
MC1508
1
2
15
13
3
16
R15
1K
C
2
3
6
$V_O$
MC1741G
or Equiv
+5 V
$V_{CC}$
-15 V
$V_{EE}$

$R_B = 2$ R14
R15 = R14

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right] - \frac{V_{ref}}{R_B}(R_O)$$

FIGURE 23 – BIPOLAR OR INVERTED NEGATIVE OUTPUT VOLTAGE CIRCUIT



A
A1 A2 A3 A4 A5 A6 A7 A8
5 6 7 8 9 10 11 12
$R_O$
MC1408 Series
MC1508
4
2
3
6
$V_O$
MC1741G
or Equiv
1 2 13 3 16 14 15
NC
C
R14
R15
$V_{CC}$
+5 V
$V_{EE}$
-15 V
$-V_{ref}$

For A = 00000000 bit configuration
$V_O = -V_{ref}$

For a ±5.0 volt output range:
$V_{ref}$ = -5.00 volts
R14 = R15 = 2.5 kΩ
C = 37 pF (min)
$R_O$ = 5 kΩ

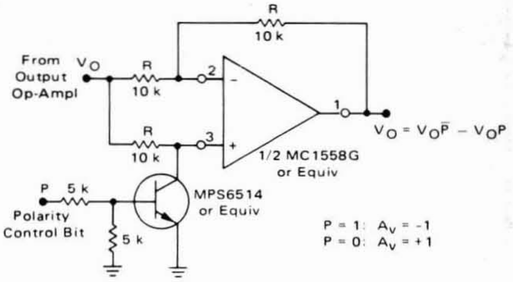
Decrease $R_O$ to 2.5 kΩ for a 0 to -5.0-volt output range. This application provides somewhat lower speed, as previously discussed in the Output Voltage Range section of the General Information.

## APPLICATIONS INFORMATION (continued)

**Polarity Switching Circuit, 8-Bit Magnitude Plus Sign D-to-A Converter**

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 24 gives 8-bit magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and −1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 24 – POLARITY SWITCHING CIRCUIT (8-Bit Magnitude Plus Sign D-to-A Converter)


R
10 k
From Output Op-Ampl
$V_O$
R
10 k
R
10 k
2
3
1
$V_O = V_O\bar{P} - V_OP$
1/2 MC1558G or Equiv
P 5 k
Polarity Control Bit
5 k
MPS6514 or Equiv
P = 1: $A_V$ = −1
P = 0: $A_V$ = +1

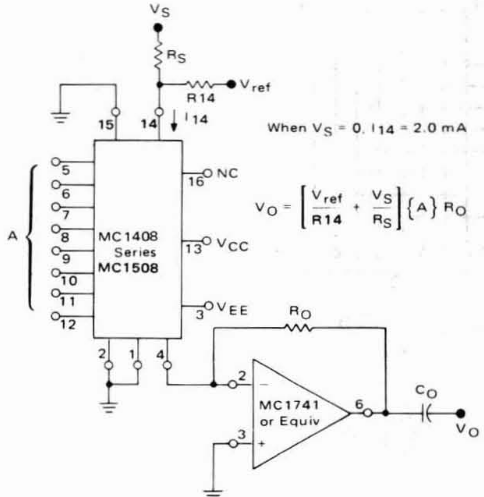
**Programmable Gain Amplifier or Digital Attenuator**

When used in the multiplying mode the MC1408 can be applied as a digital attenuator. See Figure 25. One advantage of this technique is that if $R_S$ = 50 ohms, no compensation capacitor is needed. The small and large signal bandwidths are now identical and are shown in Figure 14.

The best frequency response is obtained by not allowing $I_{14}$ to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. $R_S$ can be set for a ±1.0 mA variation in relation to $I_{14}$. $I_{14}$ can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes ac coupling necessary.

FIGURE 25 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT


$V_S$
$R_S$
$V_{ref}$
R14
$I_{14}$
15
14
When $V_S$ = 0, $I_{14}$ = 2.0 mA
A
5
6
7
8
9
10
11
12
16 NC
13 $V_{CC}$
3 $V_{EE}$
MC1408 Series MC1508
$V_O = \left[\frac{V_{ref}}{R14} + \frac{V_S}{R_S}\right]\{A\} R_O$
2
1
4
$R_O$
MC1741 or Equiv
6
3
$C_O$
$V_O$

**Panel Meter Readout**

The MC1408 can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R14 or $V_{ref}$.

FIGURE 26 – PANEL METER READOUT CIRCUIT

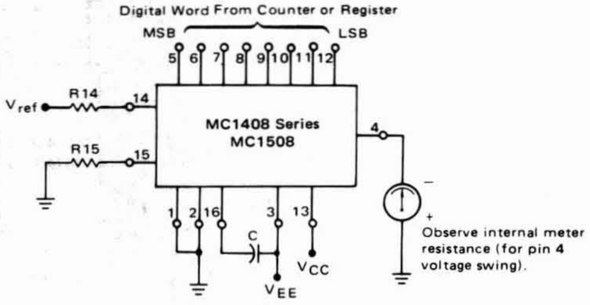
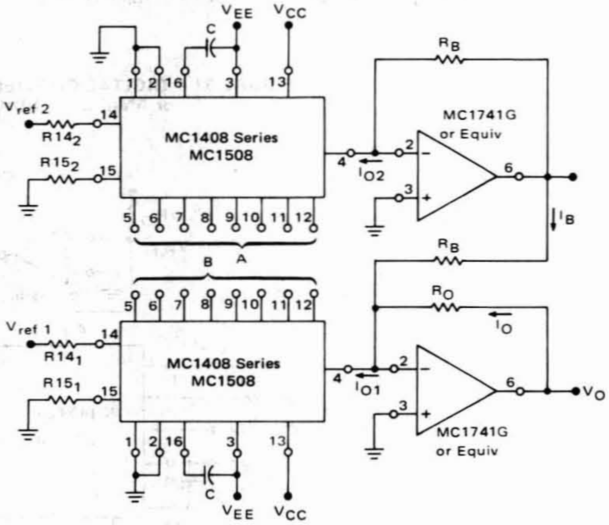

Digital Word From Counter or Register
MSB
LSB
5
6
7
8
9
10
11
12
$V_{ref}$
R14
14
R15
15
MC1408 Series MC1508
4
1
2
16
3
13
C
$V_{CC}$
$V_{EE}$
−
+
Observe internal meter resistance (for pin 4 voltage swing).

FIGURE 27 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION


$V_{EE}$
$V_{CC}$
C
1
2
16
3
13
$R_B$
$V_{ref\ 2}$
14
$R14_2$
$R15_2$
15
MC1408 Series MC1508
4
$I_{O2}$
MC1741G or Equiv
2
3
6
$I_B$
5
6
7
8
9
10
11
12
B
A
$R_B$
$R_O$
$I_O$
$V_{ref\ 1}$
14
$R14_1$
$R15_1$
15
MC1408 Series MC1508
4
$I_{O1}$
2
3
6
$V_O$
MC1741G or Equiv
1
2
16
3
13
C
$V_{EE}$
$V_{CC}$

$$I_O = I_{O\,1} - I_{O\,2} = \frac{V_{ref\ 1}}{R14_1}\{A\} - \frac{V_{ref\ 2}}{R14_2}\{B\}$$

$I_{O\,2} = -I_B$

$I_B + I_O = I_{O\,1}$

Digital Subtraction:

Let $\frac{V_{ref\ 1}}{R14_1} = \frac{V_{ref\ 2}}{R14_2}$

$$\boxed{V_O = \frac{V_{ref\ 1}}{R14_1} R_O\left[\{A\} - \{B\}\right]}$$

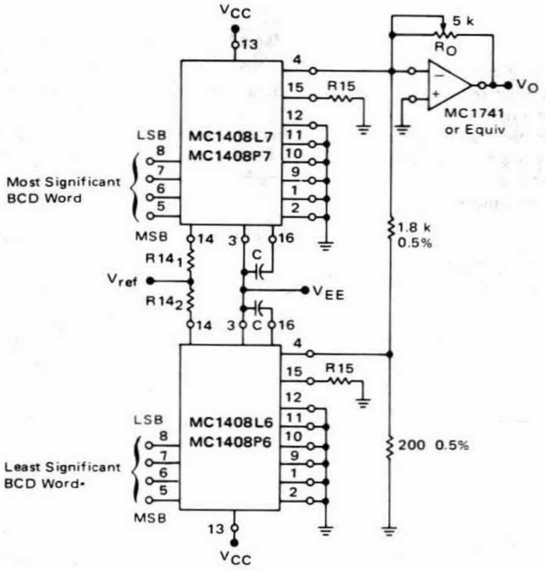
Programmable Amplifier:

Connect Digital Inputs so A = B

$$\boxed{V_O = \{A\}\left[\frac{V_{ref\ 1}}{R14_1} - \frac{V_{ref\ 2}}{R14_2}\right]}$$

## APPLICATIONS INFORMATION (continued)

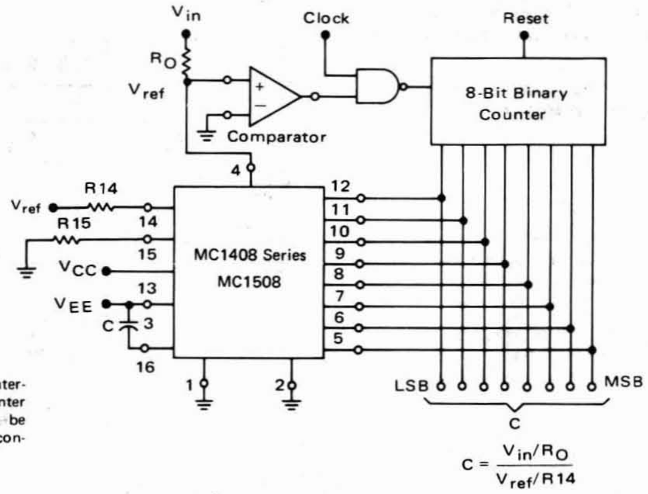
FIGURE 36 – TWO-DIGIT BCD CONVERSION



$V_{CC}$
13
4
15
R15
12
11
10
9
1
2
5 k
$R_O$
$V_O$
MC1741
or Equiv
LSB
8
7
6
5
MC1408L7
MC1408P7
Most Significant
BCD Word
MSB
14
3
16
C
$R14_1$
$V_{ref}$
$R14_2$
$V_{EE}$
1.8 k
0.5%
MC1408L6
MC1408P6
Least Significant
BCD Word
200 0.5%
13
$V_{CC}$

Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an MC1408L6 may be used for the least significant word.

FIGURE 37 – DIGITAL QUOTIENT OF TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION



$V_{in}$
Clock
Reset
$R_O$
$V_{ref}$
Comparator
8-Bit Binary
Counter
4
R14
$V_{ref}$
R15
14
15
$V_{CC}$
13
$V_{EE}$
C
3
16
MC1408 Series
MC1508
12
11
10
9
8
7
6
5
1
2
LSB
MSB
C

$$C = \frac{V_{in}/R_O}{V_{ref}/R14}$$

The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.

**MOTOROLA**

# MC3410
# MC3510 MC3410C

## Specifications and Applications Information

### TEN BIT D TO A CONVERTER

The MC3410 series devices are low-cost, high-accuracy monolithic D/A converter subsystems. Like their MC1408 series predecessors, they provide the logic controlled current switches, the R-2R resistor ladder network and output termination networks. The output buffer amplifier and reference voltage have been omitted from the circuit to allow greatest system speed, flexibility and lowest cost. This device is useful in industrial control and microprocessor based systems.

- Relative Accuracy – ±0.05% Error Maximum (MC3510 and MC3410)
- Fast Settling Time – 250 ns Typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible (from 5 to 15 V CMOS)
- Output Voltage Swing – +0.2 V to –2.5 V
- High Speed Multiplying Input Slew Rate – 20 mA/µs
- Standard Supply Voltages – +5 V and – 15 V
- All Categories Guaranteed Monotonic Across Temperature
- Reference Amplifier Internally Compensated

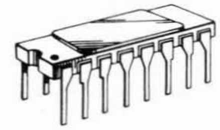
### TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 3-Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Speech Compression and Expansion
- Sample Data Systems

**LASER TRIMMED**

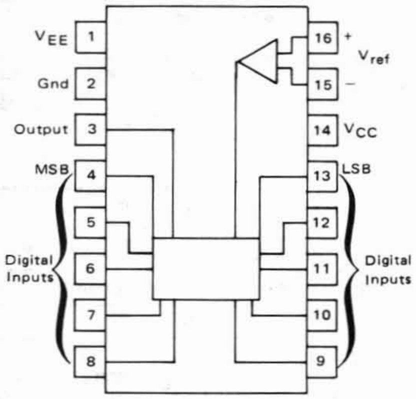
**TEN BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER**

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**L SUFFIX**
CASE 690-13
(CERAMIC PACKAGE)

**PIN CONNECTIONS**



VEE 1
Gnd 2
Output 3
MSB 4
5
6
7
8
Digital Inputs
16 + Vref
15 –
14 VCC
13 LSB
12
11
10
9
Digital Inputs

FIGURE 1 – D-to-A TRANSFER CHARACTERISTICS

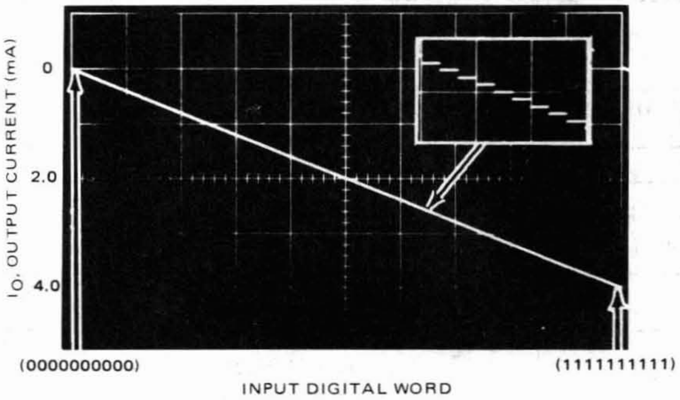
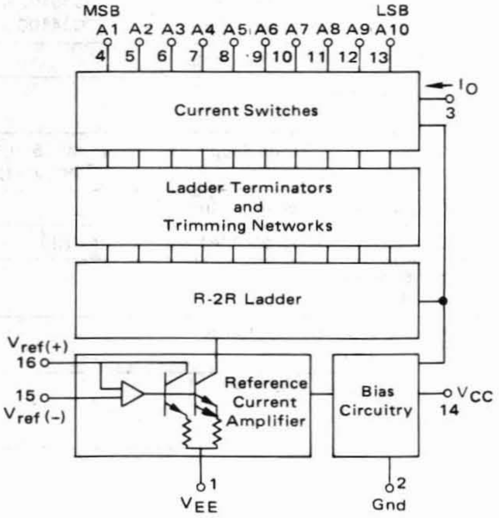


FIGURE 2 – TEN-BIT D/A CONVERTER BLOCK DIAGRAM



MSB
LSB
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
4 5 6 7 8 9 10 11 12 13
IO
3
Current Switches
Ladder Terminators and Trimming Networks
R-2R Ladder
Vref(+) 16
15 Vref (–)
Reference Current Amplifier
Bias Circuitry
VCC 14
1 VEE
2 Gnd

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +7.0<br>−18 | Vdc |
| Digital Input Voltage | $V_I$ | +15 | Vdc |
| Applied Output Voltage | $V_O$ | +0.5, −5.0 | Vdc |
| Reference Current | $I_{REF(16)}$ | 2.5 | mA |
| Reference Amplifier Inputs | $V_{REF}$ | $V_{CC}$, $V_{EE}$ | Vdc |
| Reference Amplifier Differential Inputs | $V_{REF(D)}$ | 0.7 | Vdc |
| Operating Temperature Range | $T_A$ | | °C |
| MC3510 | | −55 to +125 | |
| MC3410,C | | 0 to +70 | |
| Junction Temperature | $T_J$ | | °C |
| Ceramic Package | | +175 | |
| Plastic Package | | +150 | |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $V_{EE}$ = −15 Vdc, $\frac{V_{ref}}{R16}$ = 2.0 mA, MC3510 $T_A$ = −55°C to +125°C. MC3410 Series: $T_A$ = 0 to +70°C unless otherwise noted. All digital inputs at high logic level.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Relative Accuracy (Error relative to full scale $I_O$) $T_A$ = 25°C | $E_r$ | | | | % |
| MC3510, MC3410 | | – | – | ±0.05 | |
| MC3410C | | – | – | ±0.1 | |
| Relative Accuracy Temperature Drift (Relative to Full Scale $I_O$) | $TCE_r$ | – | 2.5 | – | PPM/°C |
| Monotonicity (Full Temperature Range) | – | Monotonic to 10 Bits | | | – |
| Settling Time to within ±1/2 LSB ($T_A$ = 25°C) (All Bits Low to High) | $t_S$ | – | 250 | – | ns |
| Propagation Delay Time $T_A$ = +25°C | $t_{PLH}$<br>$t_{PHL}$ | –<br>– | 35<br>20 | –<br>– | ns |
| Output Full Scale Current Drift MC3410, MC3410C | $TCI_O$ | – | – | 60 | PPM/°C |
| MC3510 | | – | – | 70 | |
| Digital Input Logic Levels (All Bits) | | | | | Vdc |
| High Level, Logic "1" | $V_{IH}$ | 2.0 | – | – | |
| Low Level, Logic "0" | $V_{IL}$ | – | – | 0.8 | |
| Digital Input Current (All Bits) | | | | | mA |
| High Level, $V_{IH}$ = 5.5V | $I_{IH}$ | – | – | 0.04 | |
| Low Level, $V_{IL}$ = 0.8V | $I_{IL}$ | – | 0.05 | 0.4 | |
| Reference Input Bias Current (Pin 15) | $I_{REF(15)}$ | – | −1.0 | −5.0 | μA |
| Output Current Range | $I_{OR}$ | 0 | 4.0 | 5.0 | mA |
| Output Current | $I_O$ | | | | mA |
| $V_{ref}$ = 2.000 V, $R_{16}$ = 1000 Ω | | 3.8 | 3.996 | 4.2 | |
| Output Current (All bits low) ($T_A$ = 25°C) MC3510, MC3410 | $I_{O(min)}$ | – | 0 | 2.0 | μA |
| MC3410C | | – | 0 | 4.0 | |
| Output Voltage Compliance ($T_A$ 25°C) | $V_O$ | | | | Vdc |
| $E_r \leqslant$ 0.05% relative to FS – MC3510, MC3410 | | – | – | -2.5,+0.2 | |
| $E_r \leqslant$ 0.10% relative to FS – MC3410C | | | | -2.5,+0.2 | |
| Reference Amplifier Slew Rate | $SR\ I_{ref}$ | – | 20 | – | mA/μs |
| Reference Amplifier Settling Time (0 to 4.0 mA, ±0.1%) | $STI_{REF}$ | – | 2.0 | – | μs |
| Output Current Power Supply Sensitivity MC3510, MC3410 | PSRR(−) | – | 0.003 | 0.01 | %/% |
| MC3410C | | – | 0.003 | 0.02 | |
| Output Capacitance ($V_O$ = 0) | $C_O$ | – | 25 | – | pF |
| Digital Input Capacitance (All Bits, Inputs High) | $C_I$ | – | 4.0 | – | pF |
| Power Supply Current (All Bits low) | $I_{CC}$<br>$I_{EE}$ | –<br>– | +10<br>−11.4 | +18<br>−20 | mA |
| Power Supply Voltage Range ($T_A$ = +25°C) | $V_{CCR}$<br>$V_{EER}$ | +4.75<br>-14.25 | +5.0<br>−15 | +5.25<br>−15.75 | Vdc |
| Power Consumption | $P_C$ | | | | mW |
| All Bits low | | – | 220 | 380 | |
| All Bits high | | – | 200 | – | |

## TEST CIRCUITS

### FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUITS

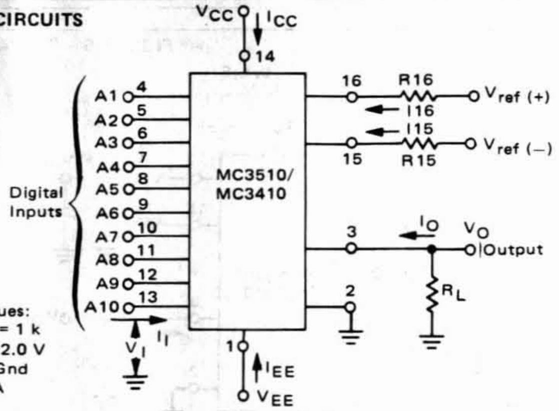
$V_I$ and $I_I$ apply to inputs A1 thru A10

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K \frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} + \frac{A9}{512} + \frac{A10}{1024}$$

where $K \cong \frac{2 V_{ref}}{R16}$

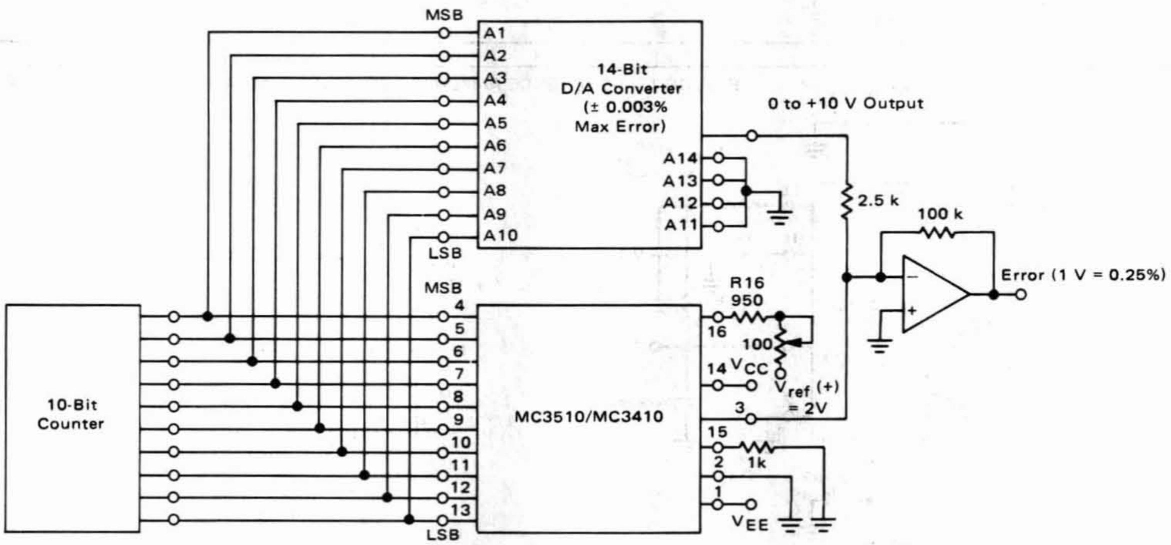
and $A_N$ = "1" if $A_N$ is at high level
$A_N$ = "0" if $A_N$ is at low level



VCC
ICC
14
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
4
5
6
7
8
9
10
11
12
13
Digital Inputs
MC3510/
MC3410
16
R16
Vref (+)
I16
I15
15
R15
Vref (–)
3
IO
VO
Output
2
RL
1
IEE
VEE
VI
II

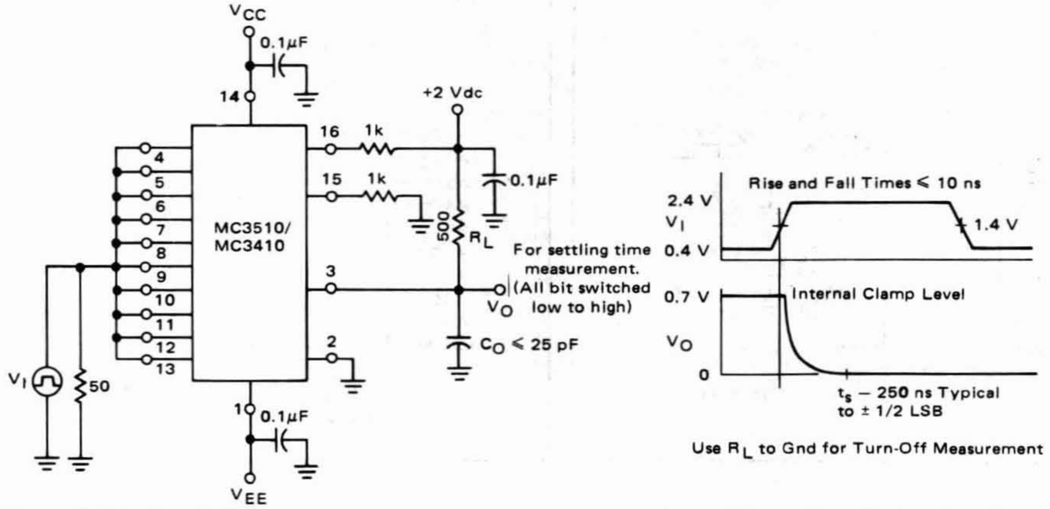
Typical Values:
R15 = R16 = 1 k
$V_{ref}$ (+) = +2.0 V
$V_{ref}$ (–) = Gnd
$I_O$ = 4.0 mA

### FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT



MSB
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
LSB
14-Bit
D/A Converter
(± 0.003%
Max Error)
A14
A13
A12
A11
0 to +10 V Output
2.5 k
100 k
Error (1 V = 0.25%)
10-Bit
Counter
MSB
4
5
6
7
8
9
10
11
12
13
LSB
MC3510/MC3410
R16
950
16
100
14 VCC
Vref (+)
= 2V
3
15
1k
2
1
VEE

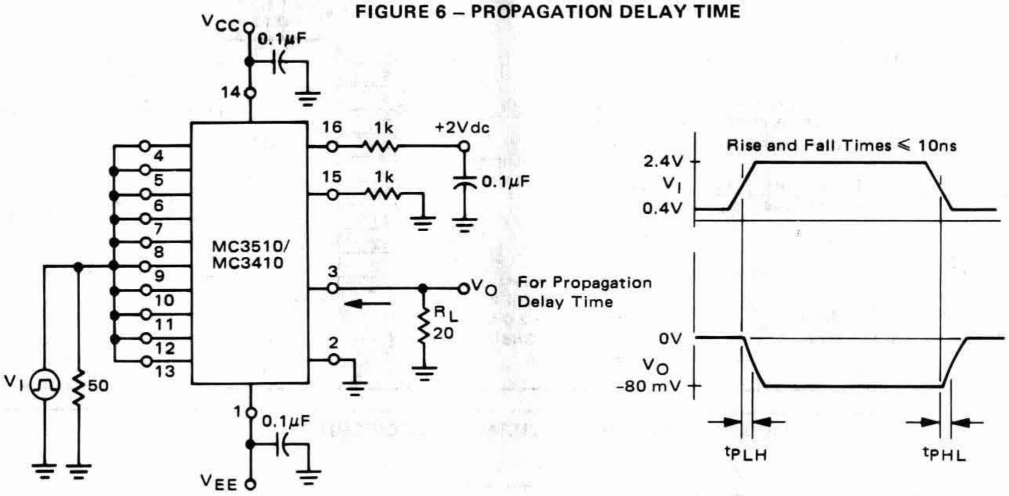
### FIGURE 5 – SETTLING TIME



VCC
0.1µF
14
+2 Vdc
16
1k
15
1k
0.1µF
500
RL
4
5
6
7
8
9
10
11
12
13
MC3510/
MC3410
3
VO
2
CO ≤ 25 pF
VI
50
1
0.1µF
VEE
For settling time
measurement.
(All bit switched
low to high)
Rise and Fall Times ≤ 10 ns
2.4 V
VI
0.4 V
1.4 V
0.7 V
Internal Clamp Level
VO
0
ts – 250 ns Typical
to ± 1/2 LSB
Use RL to Gnd for Turn-Off Measurement

## TEST CIRCUITS (Continued)

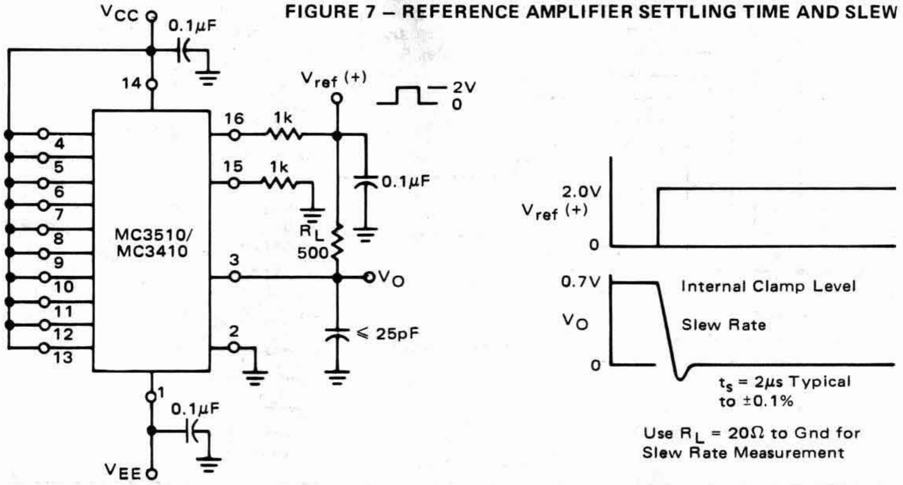
FIGURE 6 – PROPAGATION DELAY TIME


VCC
0.1μF
14
16
1k
+2Vdc
15
1k
0.1μF
4
5
6
7
8
9
10
11
12
13
MC3510/
MC3410
3
VO
RL
20
2
VI
50
1
0.1μF
VEE
2.4V
VI
0.4V
0V
VO
-80 mV
tPLH
tPHL

For Propagation Delay Time

Rise and Fall Times ≤ 10ns

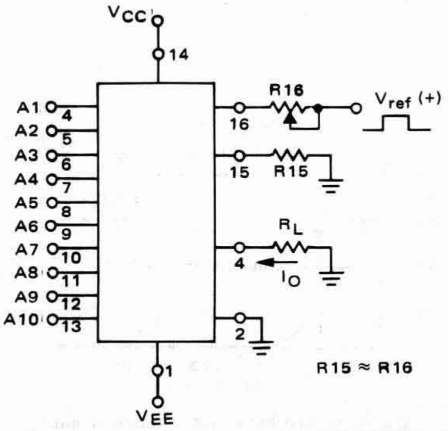
FIGURE 7 – REFERENCE AMPLIFIER SETTLING TIME AND SLEW RATE


VCC
0.1μF
14
Vref (+)
2V
0
16
1k
15
1k
0.1μF
4
5
6
7
8
9
10
11
12
13
MC3510/
MC3410
RL
500
3
VO
2
≤ 25pF
1
0.1μF
VEE
2.0V
Vref (+)
0
0.7V
VO
0
Internal Clamp Level
Slew Rate

$t_s$ = 2μs Typical to ±0.1%

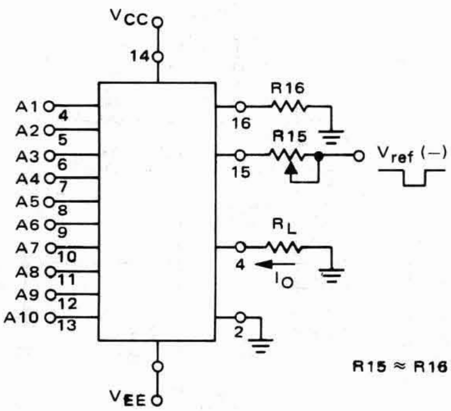
Use $R_L$ = 20Ω to Gnd for Slew Rate Measurement

FIGURE 8 – POSITIVE $V_{ref}$


VCC
14
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
4
5
6
7
8
9
10
11
12
13
R16
16
Vref (+)
15
R15
RL
4
IO
2
1
VEE

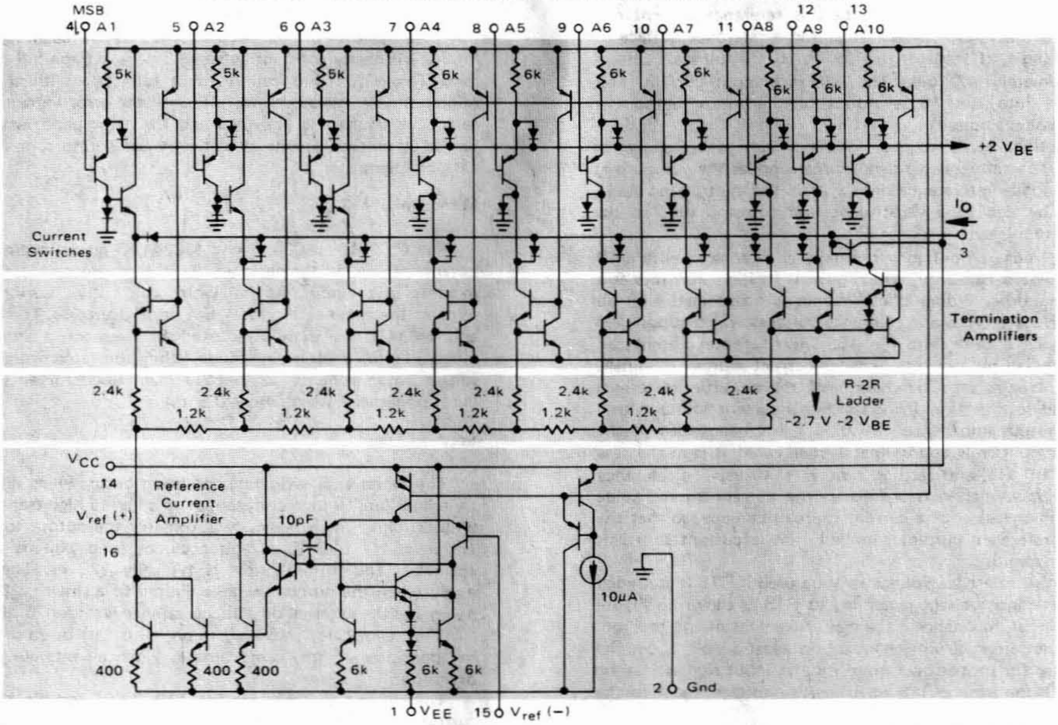
R15 ≈ R16

FIGURE 9 – NEGATIVE $V_{ref}$


VCC
14
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
4
5
6
7
8
9
10
11
12
13
R16
16
R15
15
Vref (−)
RL
4
IO
2
VEE

R15 ≈ R16

FIGURE 10 — MC3410 10-BIT D/A CONVERTER EQUIVALENT CIRCUIT



## CIRCUIT DESCRIPTION

The MC3410 consists of a reference current amplifier, a diffused R-2R ladder, a laser trimming network, and ten high-speed current switches. The trimming method employed makes it possible to improve the linearity attainable with modern diffusion technology by as much as a factor of ten so that a highly linear part results. The trim is performed by cutting aluminum links arranged to give incremental variations in voltage at the ladder termination amplifiers (See Figure 10). This yields a highly stable trim with no increase in fabrication complexity.

The switches are non-inverting in operation, so that a high state on an input turns on the specific component of output current. The switches use current steering for speed, and interface the R-2R ladder through unity gain feedback termination amplifiers, which provide low impedance terminations of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the current switches. The three least-significant bit switches derive their current through emitter scaling from the last leg of the ladder. The remaining current, equal to one LSB, is shunted to $V_{CC}$ at the LSB switch. Therefore, the maximum output current is 1023/1024 of the reference amplifier current, or nominally 3.996 mA for a 2.000 mA reference input current.

### Reference Voltage

To generate the precision voltage reference input for the MC3410, either the MC1403 or the MC1404 may be used. The MC1403 produces a 2.5 V ±1% output voltage while the MC1404 produces a 10 V ±1% output. Both have excellent temperature and long term stability. In order to reduce the effect of reference amplifier offset voltage on overall accuracy, the highest possible stability reference voltage should be used. Therefore, in systems with a +15 V supply, the MC1404 (10 V) is recommended. Where the most positive supply is only +5 V, the MC1403 provides a 2.5 V reference. To set the reference current exactly, a low temperature coefficient potentiometer in series with R1 should be used.

## GENERAL INFORMATION

### Reference Amplifier

The reference amplifier allows the user to provide a voltage and a resistor to Pin 16 to convert the reference voltage to a current. A current mirror doubles this reference current and feeds it to the R-2R ladder. Thus for a reference voltage of 2.0 Volts and 1 kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0 mA. The reference input current, I16, must flow into Pin 16 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 8. The reference voltage source supplies the full current I16. For bipolar refererence signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level.

The reference amplifier is internally compensated with a 10 pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply 2.0 mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0 mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0 MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16 = 1.0 kΩ, and settling time is ≈ 10 µs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5 mA for stability.

A negative reference voltage may be used if R16 is grounded and the reference voltage is applied to R15 as shown in Figure 9. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3 Volts above the $V_{EE}$ supply for proper operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0 V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1 µF capacitor to ground.

### Output Voltage Range

The voltage on Pin 3 is restricted to a range of −2.5 V to +0.2 V due to the current switching methods employed in the MC3410. When a current switch is turned off, the positive voltage at the output terminal can turn on the output diode and increase the output current. When a current switch is on, the negative output voltage range is restricted to the point at which the low current device of the termination amplifier Darlington begins to saturate, resulting in a decrease in output current.

The output voltage compliance is guaranteed at 25°C. Note from Figure 14 that the output compliance of the MC3410 is nearly constant over temperature.

### Accuracy

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full scale current. The relative accuracy of the MC3410 is fairly constant over temperature due to the excellent temperature tracking, of the diffused resistors. The full scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the MC3410 has a low full scale current drift with temperature.

The MC3510 and MC3410 are guaranteed accurate to within ±1/2 LSB at 25°C and at a full scale current of 3.996 mA. Input reference current to Pin 16 is guaranteed to be between 1.9 and 2.1 mA to produce a full scale output current of 3.996 mA. The relative accuracy test circuit is shown in Figure 4. The 14 bit D/A converter is calibrated for a full scale output of 3.996 mA. This is an optional step as the relative accuracy of the MC3410 is nearly constant between 3 mA and 5 mA full scale current. The MC3410 is calibrated at full scale with the 14-bit reference D/A by adjusting R16 until the error voltage goes to zero. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored on a peak detector.

### Monotonicity

The MC3510, MC3410 and MC3410C are all guaranteed to be monotonic at temperature. This guarantees that for every increase in the input digital word, the output current either remains the same or increases, but never decreases. The MC3510 and MC3410 are monotonic over their respective temperature ranges. In the multiplying mode (when the reference current is varied), monotonicity is typically maintained for all values of input reference current above 0.5 mA.

### Settling Time

The worst case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250 ns for the output to settle to within ± 1/2 LSB for 10-bit accuracy, and 200 ns for 8-bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small (< 0.7 Volt) swing and the external output capacitance is under 25 pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

The slowest switches are bit A10 (LSB) and bit A9, which turn on and settle in typically 200 ns, and turn off in 100 ns.

In the test circuit of Figure 5, the output voltage is internally clamped in the MC3410 at about 0.7 Volts above ground. The output is thus limited to a 0.7 Volt swing. If a load resistor of 625 Ohms is connected to ground, allowing the output to swing to −2.5 Volts, the settling time increases to 1.5 µs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100µF supply bypassing, and minimum scope lead length are all necessary.

### MC3510 TERMINOLOGY

RELATIVE ACCURACY – Maximum output deviation from the straight line connecting zero and full scale, expressed as a percentage of full scale.

RELATIVE ACCURACY DRIFT – The average change in linearity error that will occur with a change in ambient temperature, expressed in parts per million of full scale per degree C.

MONOTONICITY – For every increase in the input digital word, the output current either remains the same or increases.

SETTLING TIME – The elapsed time from the input transition until the output has settled within an error band about its final value.

OUTPUT FULL SCALE CURRENT DRIFT – The average change in full scale current between 25°C and either temperature extreme, expressed in parts per million of full scale per degree C.

REFERENCE AMPLIFIER SLEW RATE – The maximum rate of change of the full scale output current expressed in milliamperes per microsecond.

OUTPUT VOLTAGE COMPLIANCE – The maximum voltage that can be applied to the output pin so that the specified change in output current is not exceeded.

POWER SUPPLY SENSITIVITY – The change in full scale current caused by a change in $V_{EE}$, expressed as a percent of full scale current per percent change in $V_{EE}$.

## TYPICAL CHARACTERISTICS

FIGURE 11 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

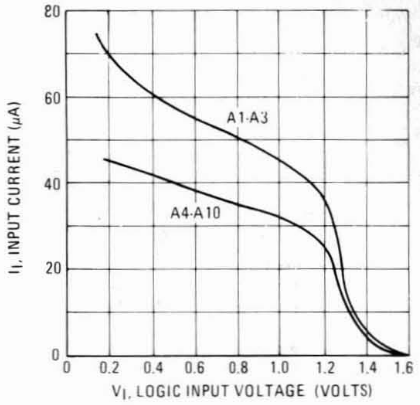


FIGURE 12 – TRANSFER CHARACTERISTIC versus TEMPERATURE

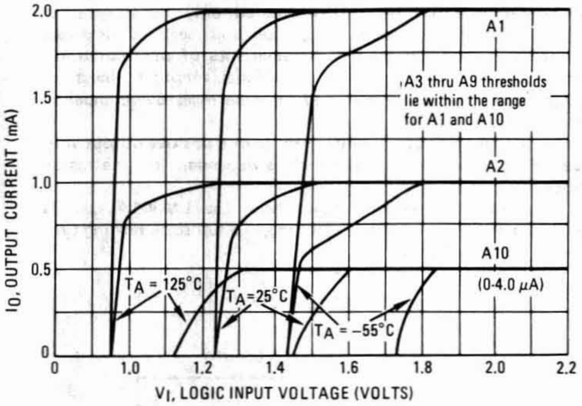


FIGURE 13 – OUTPUT CURRENT versus OUTPUT VOLTAGE (Output Compliance)

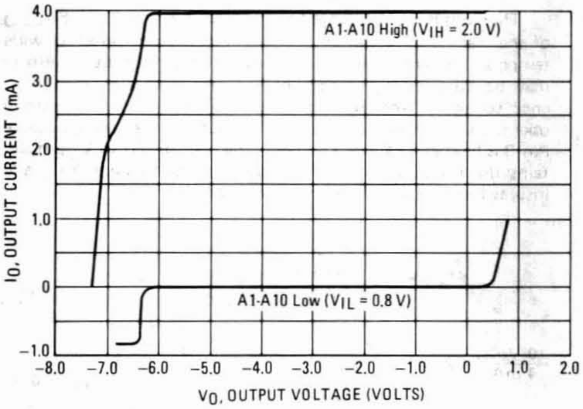


FIGURE 14 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE

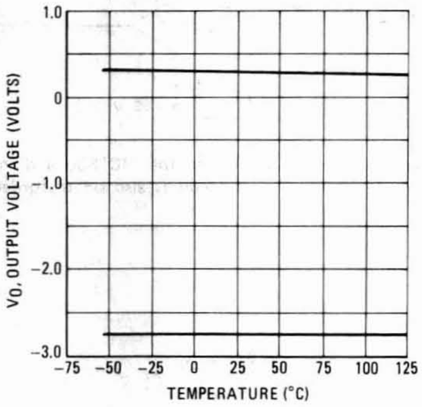


FIGURE 15 – REFERENCE AMPLIFIER FREQUENCY RESPONSE

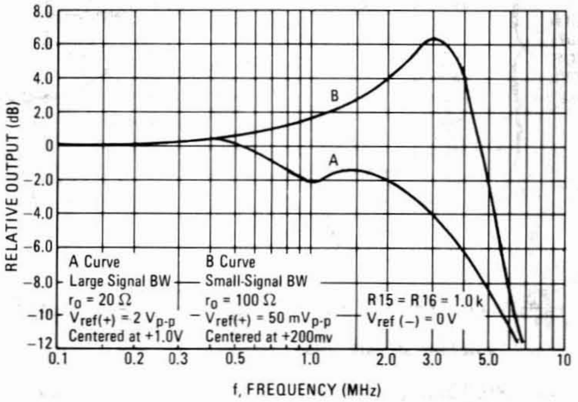
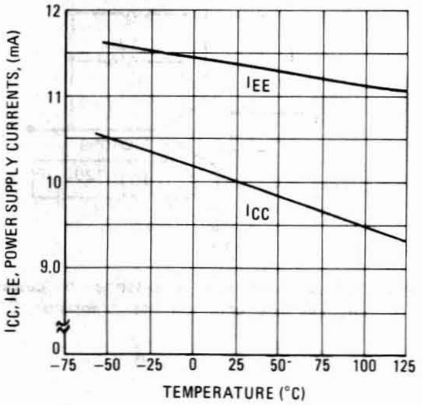


FIGURE 16 – TYPICAL POWER SUPPLY CURRENTS versus TEMPERATURE



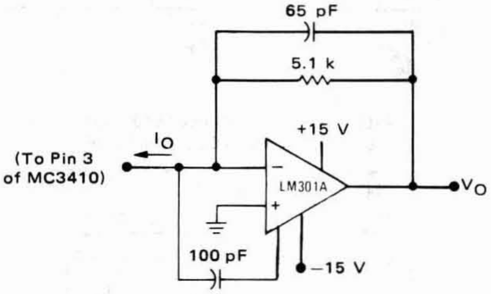
## APPLICATIONS INFORMATION

Voltage outputs are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC3410 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

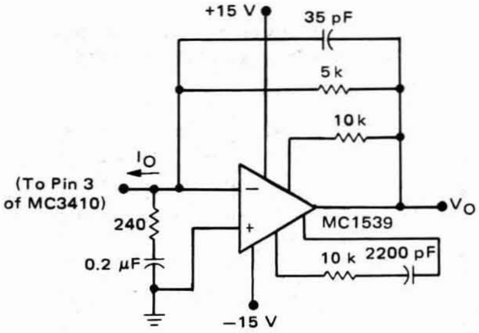
The following circuit shows how the LM301A can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 µs.

FIGURE 17


65 pF
5.1 k
+15 V
$I_O$
(To Pin 3 of MC3410)
LM301A
$V_O$
100 pF
−15 V

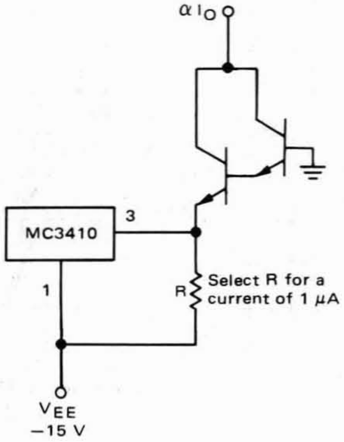
An alternative method is to use the MC1539 and input compensation. Response of this circuit is also on the order of 2.0 µs.

FIGURE 18


+15 V
35 pF
5 k
10 k
$I_O$
(To Pin 3 of MC3410)
240
0.2 µF
MC1539
$V_O$
10 k
2200 pF
−15 V

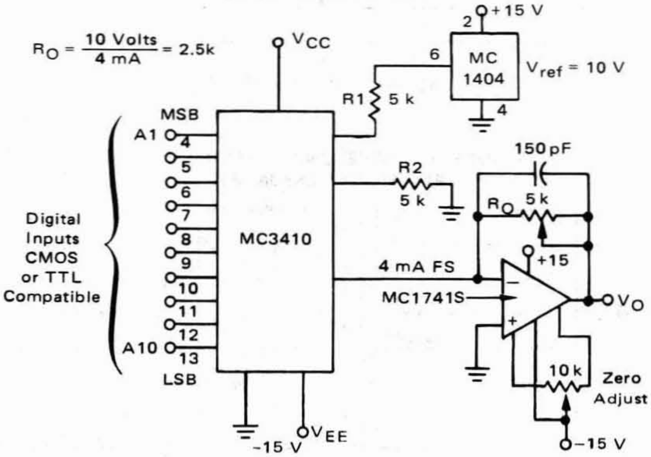
The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 19 – EXTENDING POSITIVE VOLTAGE RANGE


$\alpha I_O$
MC3410
3
1
R
Select R for a current of 1 µA
$V_{EE}$
−15 V

The output voltage range for this circuit is 0 volts to $BV_{CBO}$ of the transistor. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because Pin 3 is held at a constant voltage. The resistor (R) to $V_{EE}$ maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

FIGURE 20 – OUTPUT CURRENT TO VOLTAGE CONVERSION


$R_O = \frac{10\ \text{Volts}}{4\ \text{mA}} = 2.5\text{k}$
$V_{CC}$
+15 V
2
6
MC 1404
$V_{ref} = 10$ V
4
R1
5 k
MSB
A1
4
5
6
7
8
9
10
11
12
13
A10
LSB
Digital Inputs CMOS or TTL Compatible
MC3410
R2
5 k
150 pF
$R_O$
5 k
+15
4 mA FS
MC1741S
$V_O$
10 k
Zero Adjust
−15 V
$V_{EE}$
−15 V

$$V_O = \frac{2R_O}{R_1} V_{ref} \left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} + \frac{A9}{512} + \frac{A10}{1024}\right]$$

for 10 volt fullscale calibration

$$V_O = \frac{2(2.5\ \text{k})}{5.0\ \text{k}} 10\ \text{Volts} \left[\frac{1023}{1024}\right] \qquad V_O = 10\ \text{Volts}\ [0.9990]$$

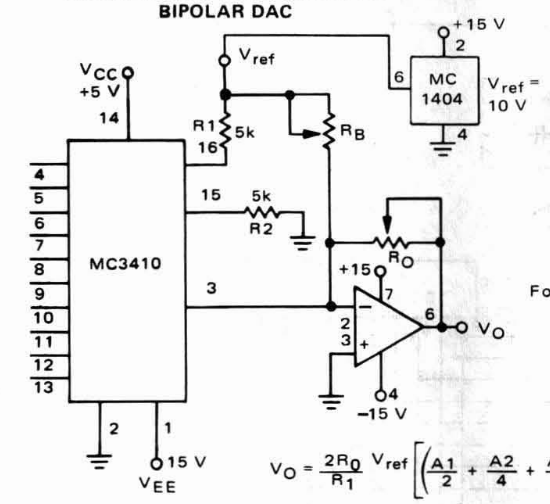
$R_O$ = Full Scale Adjust

## APPLICATIONS INFORMATION (Continued)

### Bipolar or Negative Output Voltage

The circuit in Figure 21 is a variation of the standard output voltage circuit in Figure 20. A negative or offset binary output may be obtained by sourcing current from the reference into the output through $R_B$. If $R_B$ allows 2 mA ($R_B$ = 5 kΩ from 10 Volts) then 1000000000 input will generate zero output voltage.

FIGURE 21 – OFFSET BINARY OR BIPOLAR DAC



+15 V
2
Vref
6
MC 1404
Vref = 10 V
4
VCC +5 V
14
R1 5k
16
RB
15
5k
R2
4
5
6
7
8
9
10
11
12
13
MC3410
3
+15
7
RO
2
3
6
VO
4
−15 V
2
1
15 V
VEE

For Offset Binary Output From +5 V to −5 V

$R_O \cong 2.5\ k\Omega$

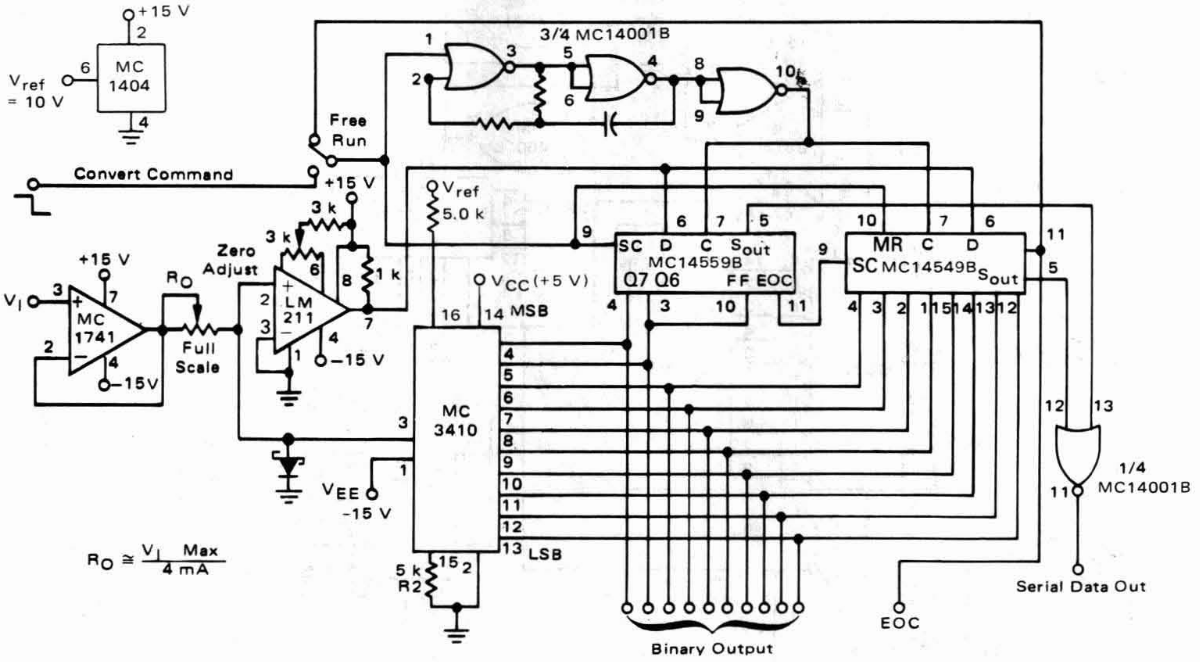
$R_B \cong 5\ k\Omega$

$$V_O = \frac{2R_O}{R_1} V_{ref}\left[\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} + \frac{A9}{512} + \frac{A10}{1024}\right) - \frac{2R_I}{R_B}\right]$$

### Successive Approximation A to D

The fastest and most efficient means of A to D conversion using D to A convertors is successive approximation (SA). Similar in appearance to staircase devices, the SA converter is capable of 100 times faster conversions for a 10-bit result. A complete 10-bit SA coverter using MC3410 and MC14559B/49B successive approximation registers is shown in Figure 22. The complexity which results in higher conversion speeds is contained in the MC14559B/49B registers. Quite simply, the register compares the DAC output resulting from activating each bit with the input voltage. This is done starting with most significant bit and after 10 comparisons generates the 10-bit binary output representing that input. The accuracy of the conversion is fixed by the accuracy of the MC3410 and is not dependent on tolerances of the other components. An EOC outout is available and can be used to latch the parallel output or to synchronize the serial output which is also available. For more details on SA converters, see AN-716.

FIGURE 22 – SUCCESSIVE APPROXIMATION CONVERTER USING MC3410 AND MC1404



+15 V
2
6
MC 1404
Vref = 10 V
4
3/4 MC14001B
1
2
3
5
6
4
8
9
10
Free Run
Convert Command
+15 V
3 k
3 k
Zero Adjust
Vref
5.0 k
+15 V
VI
3
7
MC 1741
2
4
−15V
RO
Full Scale
2
3
LM 211
6
8
1 k
7
1
4
−15 V
VCC (+5 V)
16
14 MSB
9
SC D C Sout
MC14559B
Q7 Q6 FF EOC
6 7 5
4 3 10 11
9
10 7 6
MR C D
SC MC14549B Sout
4 3 2 1 15 14 13 12
11
5
MC 3410
3
1
VEE
−15 V
4 5 6 7 8 9 10 11 12 13 LSB
5 k R2
15 2
12 13
11
1/4 MC14001B
Serial Data Out
EOC
Binary Output

$R_O \cong \frac{V_I\ Max}{4\ mA}$

## APPLICATIONS INFORMATION (Continued)

**Staircase A to D**

**If high conversion speed is not required, a staircase A to D convertor can be built for somewhat lower cost. A complete staircase A/D convertor is shown in Figure 23. Here the complicated SA registers are replaced with simple binary counters. With an input voltage applied, the binary counter is reset by the convert command pulse and the begin accumulating counts. The DAC output steps upward until the comparator detects that the input is equal to the DAC output. The counters are disabled and the conversion result is held at the output until the circuit is reset by the convert command input.**

One advantage of staircase convertors is the ease with which BCD outputs may be obtained. Figure 24 shows a 3-digit panel meter using the staircase technique and an MC14553B 3-decade counter. The circuit function is similar to Figure 23 but Multiplexed BCD output is available from the MC14553B counters. Parallel BCD may be obtained with equal ease using the MC14518B 2-decade CMOS counters.

In both these staircase designs the system accuracy is determined by the specified accuracy of the MC3410.

**FIGURE 23 — 10-BIT STAIRCASE A to D USING MC3410 AND MC1403**

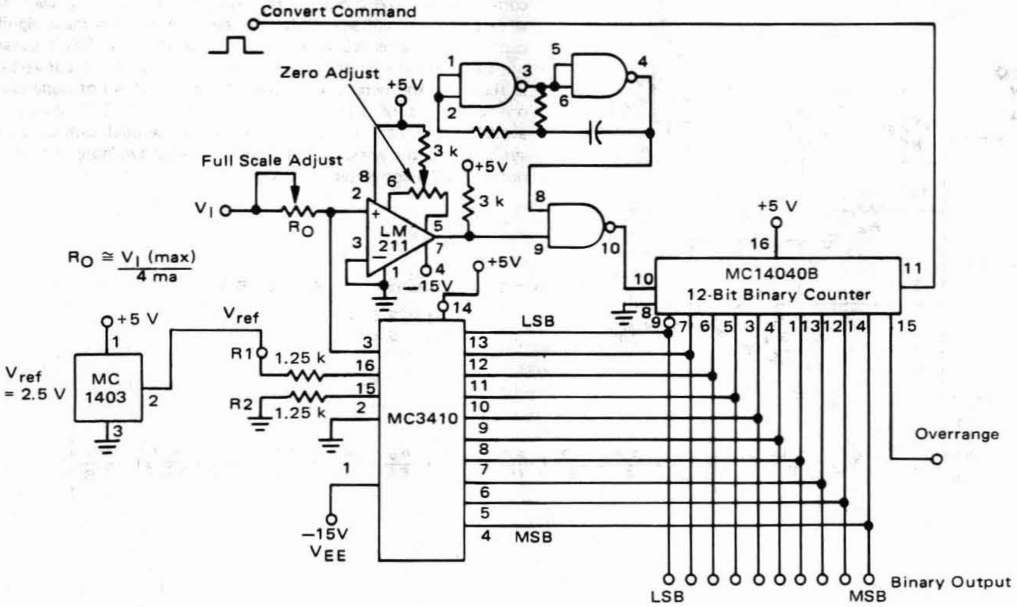
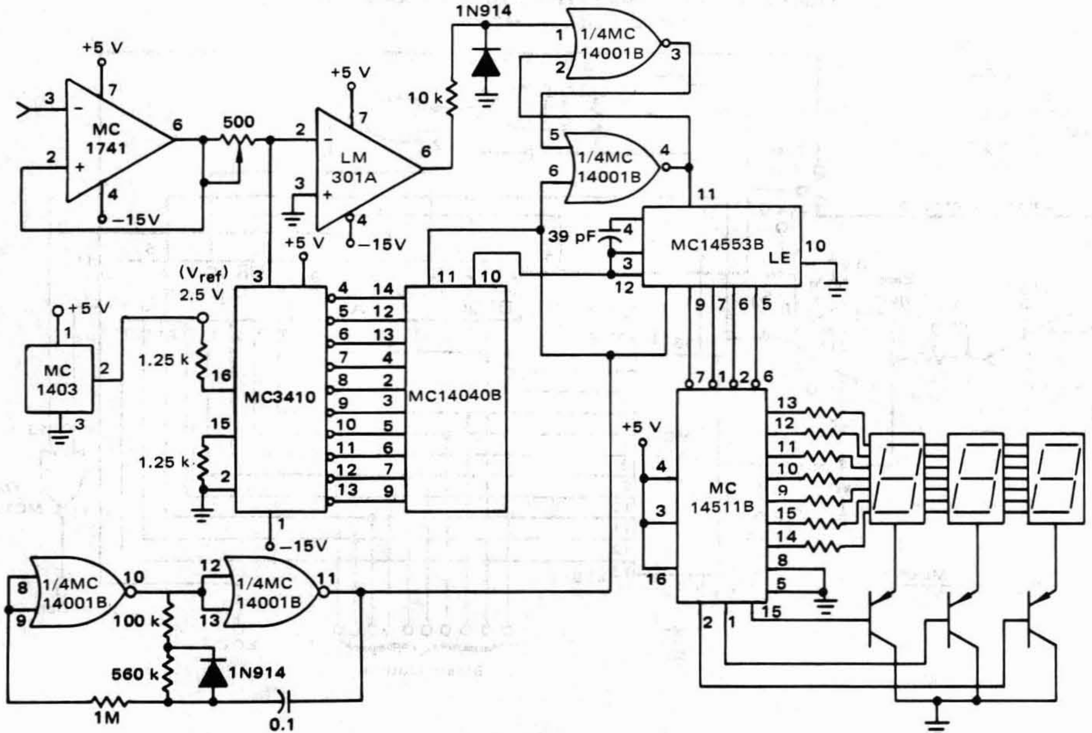
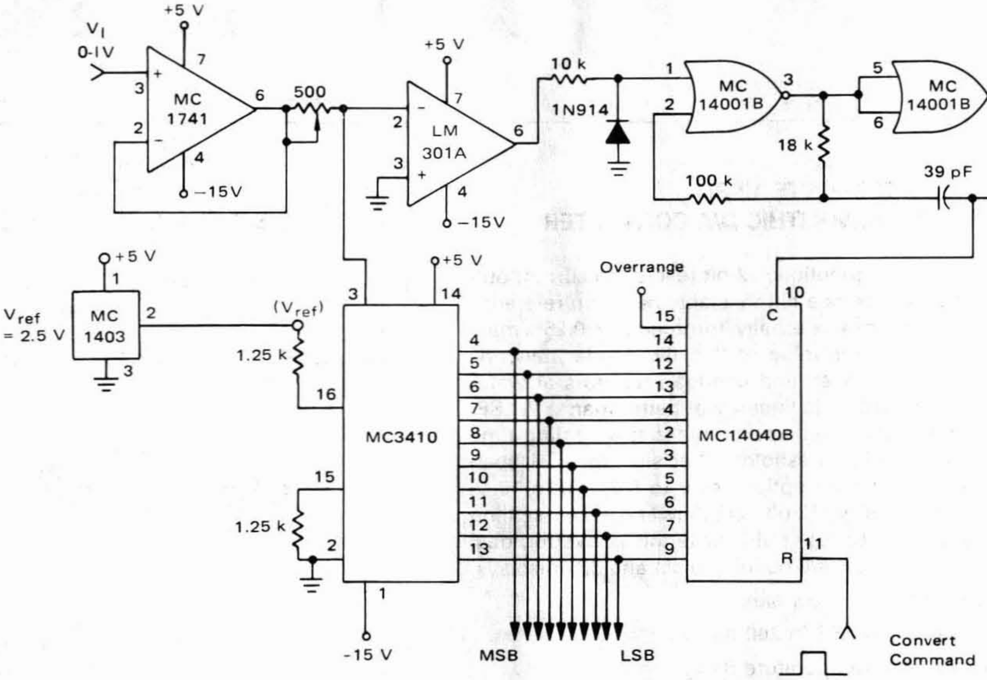

Convert Command
Zero Adjust
+5 V
3 k
Full Scale Adjust
+5V
3 k
V_I
R_O
LM 211
-15V
+5V
R_O ≅ V_I (max) / 4 ma
+5 V
V_ref
V_ref = 2.5 V
MC 1403
R1
1.25 k
R2
1.25 k
MC3410
LSB
MSB
-15V
V_EE
+5 V
MC14040B
12-Bit Binary Counter
Overrange
LSB
MSB
Binary Output

**FIGURE 24 — 3-DIGIT DVM USING MC3410 AND MC1403**


1N914
1/4MC 14001B
+5 V
MC 1741
-15V
500
+5 V
LM 301A
10 k
-15V
1/4MC 14001B
39 pF
MC14553B
LE
(V_ref) 2.5 V
+5 V
MC 1403
1.25 k
1.25 k
MC3410
MC14040B
-15V
+5 V
MC 14511B
1/4MC 14001B
1/4MC 14001B
100 k
560 k
1N914
1M
0.1

## APPLICATIONS INFORMATION (Continued)

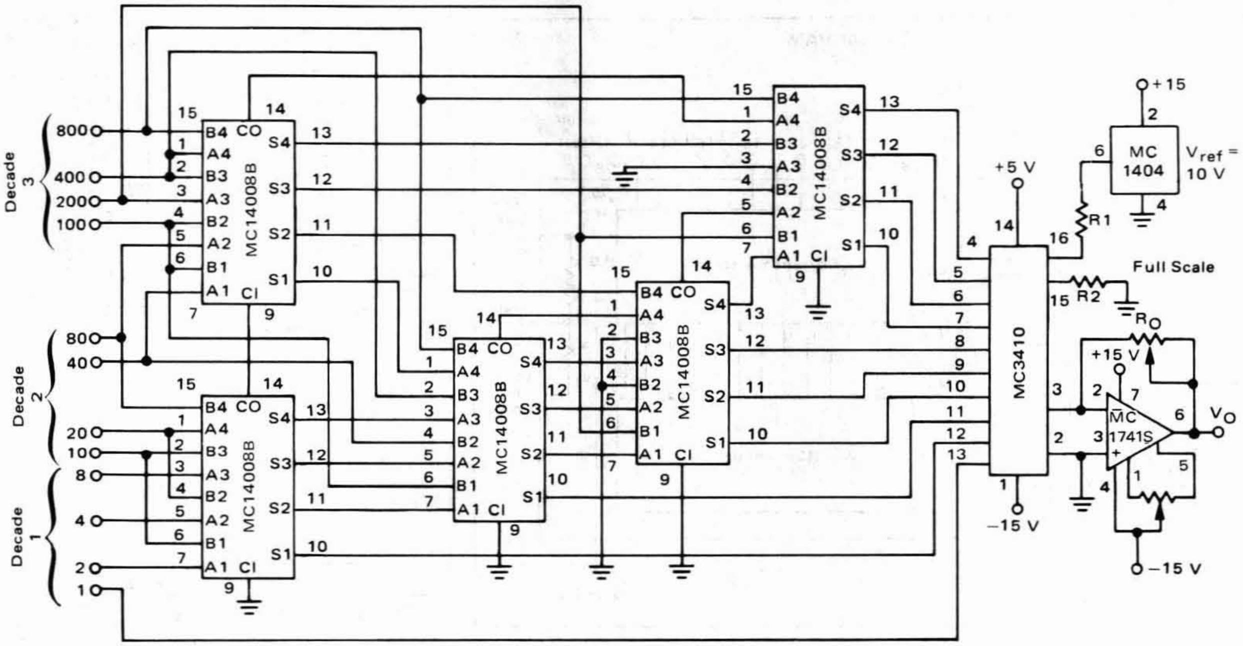
### FIGURE 25 – ALTERNATE APPROACH STAIRCASE A TO D


V<sub>I</sub> 0-1V
+5 V
MC 1741
−15V
500
+5 V
LM 301A
−15V
10 k
1N914
MC 14001B
MC 14001B
18 k
100 k
39 pF
V<sub>ref</sub> = 2.5 V
MC 1403
(V<sub>ref</sub>)
1.25 k
1.25 k
MC3410
-15 V
Overrange
MC14040B
C
R
MSB
LSB
Convert Command

### BCD D to A Converter

BCD output A to D conversions are most easily accomplished by accumulating the digital results in two different counters, but that concept does not extend to BCD D to A techniques. Using the circuit in Figure 26 a three-digit BCD number can be converted to a 10-bit accurate voltage. The MC14008B's perform the combinational BCD-to-Binary conversion. The accuracy of this circuit is also solely dependent on the accuracy of the MC3410.

### FIGURE 26 – 3-DECADE BCD DAC


Decade 3
800
400
200
100
Decade 2
80
40
20
10
Decade 1
8
4
2
1
MC14008B
B4 A4 B3 A3 B2 A2 B1 A1 CO CI S4 S3 S2 S1
MC3410
+5 V
−15 V
+15
MC 1404
V<sub>ref</sub> = 10 V
R1
R2
Full Scale
R<sub>O</sub>
+15 V
MC 1741S
V<sub>O</sub>
−15 V

**MOTOROLA**

# MC3412
# MC3512

## LASER TRIMMED HIGH-SPEED 12-BIT D/A CONVERTER

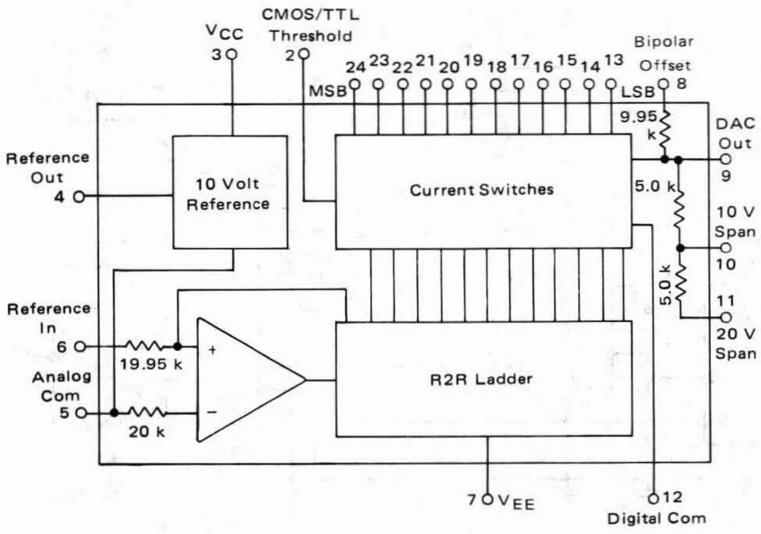
**SILICON MONOLITHIC INTEGRATED CIRCUIT**

## COMPLETE 12-BIT HIGH-SPEED MONOLITHIC D/A CONVERTER

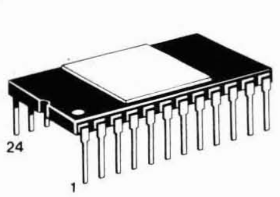
The MC3412/3512 is a monolithic 12-bit resolution current output D/A converter. It contains a highly stable bandgap reference capable of supplying 1.5 mA externally, trimmed to ±0.25% maximum error. Active laser trimming of thin film ladder network, reference, span, bipolar offset, and bandgap resistors at wafer level provide high accuracy and linearity of better than ±½ LSB. An innovative bit switching scheme provides fast settling time with either CMOS or TTL thresholds. Precision internal span resistors allow output voltage options of 0 to 5.0 V, 0 to 10 V, ±2.5 V, ±5.0 V, and ±10 V. 12-bit accuracy and a fast settling time of typically 200 ns (to ±½ LSB) make this converter ideal for applications such as a fast A/D building block and CRT displays.

- True 12-Bit Linearity: ±½ LSB Max
- Fast Settling Time: ±½ LSB in 200 ns Typ
- Fully Monotonic Over Temperature Range
- Highly Stable Bandgap Voltage Reference On Chip
- Linearity Guaranteed Over Temperature
- Low Power Consumption: 210 mW
- Pinout Compatible with AD563 and AD565
- Selectable Digital Thresholds
- Internal Application Resistors for Generating Calibrated Output Voltages

### BLOCK DIAGRAM

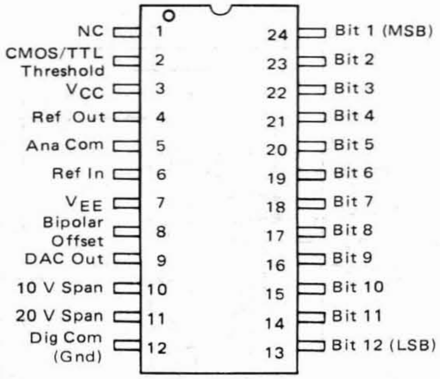


VCC 3
CMOS/TTL Threshold 2
24 23 22 21 20 19 18 17 16 15 14 13
MSB
LSB
Bipolar Offset 8
9.95 k
DAC Out 9
Reference Out 4
10 Volt Reference
Current Switches
5.0 k
10 V Span 10
5.0 k
11
20 V Span
Reference In 6
19.95 k
Analog Com 5
20 k
R2R Ladder
7 VEE
12 Digital Com



**L SUFFIX**
CERAMIC PACKAGE
CASE 716-06

### PIN CONNECTIONS



NC 1
CMOS/TTL Threshold 2
VCC 3
Ref Out 4
Ana Com 5
Ref In 6
VEE 7
Bipolar Offset 8
DAC Out 9
10 V Span 10
20 V Span 11
Dig Com (Gnd) 12
24 Bit 1 (MSB)
23 Bit 2
22 Bit 3
21 Bit 4
20 Bit 5
19 Bit 6
18 Bit 7
17 Bit 8
16 Bit 9
15 Bit 10
14 Bit 11
13 Bit 12 (LSB)

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC3412L | 0°C to +70°C | Ceramic DIP |
| MC3512L | −55°C to +125°C | Ceramic DIP |

**MAXIMUM RATING** ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +18<br>−18 | Vdc |
| Analog Ground to Digital Ground | $V_{AD}$ | ±1.0 | Vdc |
| Applied Output Voltage (Pin 9) | $V_O$ | −7.0 to +12 | Vdc |
| Digital Input Voltage (Pins 13 to 24) | $V_I$ | −5.0 to +18 | Vdc |
| Reference Input to Analog Ground | $V_{RI}$ | ±12 | Vdc |
| Reference Current | $I_{REF}$ | Short circuit to either Com (Ground) or $V_{CC}$ | |
| Bipolar Offset to Analog Ground | | ±12 | Vdc |
| Ten Volt Span Resistor to Analog Ground | | ±12 | Vdc |
| Twenty Volt Span Resistor to Analog Ground | | ±24 | Vdc |
| Power Dissipation | $P_D$ | 1000 | mW |
| Operating Temperature Range MC3412<br>MC3512 | $T_A$ | 0 to 70<br>−55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to 150 | °C |
| Junction Temperature | $T_J$ | +175 | °C |

## TERMINOLOGY

**Nonlinearity** (Relative Accuracy) — Maximum output deviation from ideal straight line connecting zero and full-scale readings, expressed as a fraction of LSB or percent of full scale.

**Differential Nonlinearity** — Maximum deviation in the readings of any two adjacent input bit codes from the ideal LSB step, expressed in fractions of LSB or percentage of full scale. A differential nonlinearity value greater than 1 LSB may lead to non-monitonic operation.

**Monotonicity** — For every increase in the input digital word, the output current either remains the same or increases.

The MC3512 and MC3412 are all guaranteed to be monotonic over temperature.

**Settling Time** — The elapsed time from the input transition until the output has settled within an error band about its final value.

The worst case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 200 ns for the output to settle to within ± ½ LSB for 12 bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small (<0.5 V) swing and the external output capacitance is under 10 pF.

**Gain Error** — The difference between the actual full scale range (difference in output between all bits on, and all bits off) and the ideal full scale range. Based on a 0 to 10 V output configuration, the ideal FSR is $\frac{4095}{4096} \times 10 = 9.99756$ V.

Gain error is expressed in percentage of full scale (FS).

**Unipolar Offset Error** — Using the configuration shown in Figure 1, with R1 = 50 ohms and with all bits off, the output voltage reading compared to zero is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

**Bipolar Offset Error** — Using the configuration shown in Figure 2, with R2 = 50 ohms with all bits off, the output voltage reading compared to the ideal negative full scale value is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

**Bipolar Zero Error** — Using the configuration shown in Figure 2, with R1 = R2 = 50 Ω, with the MSB on and all other bits off, the output voltage reading compared to zero is expressed as a percentage of the full-scale range. Offset voltage of the output op amp must be nulled.

**Temperature Coefficients** — (Unipolar offset, Bipolar offset, Gain and Differential Nonlinearity). The maximum deviation of the particular parameter over the specified temperature range, divided by the temperature range, expressed in parts per million of Full Scale Range per degree C.

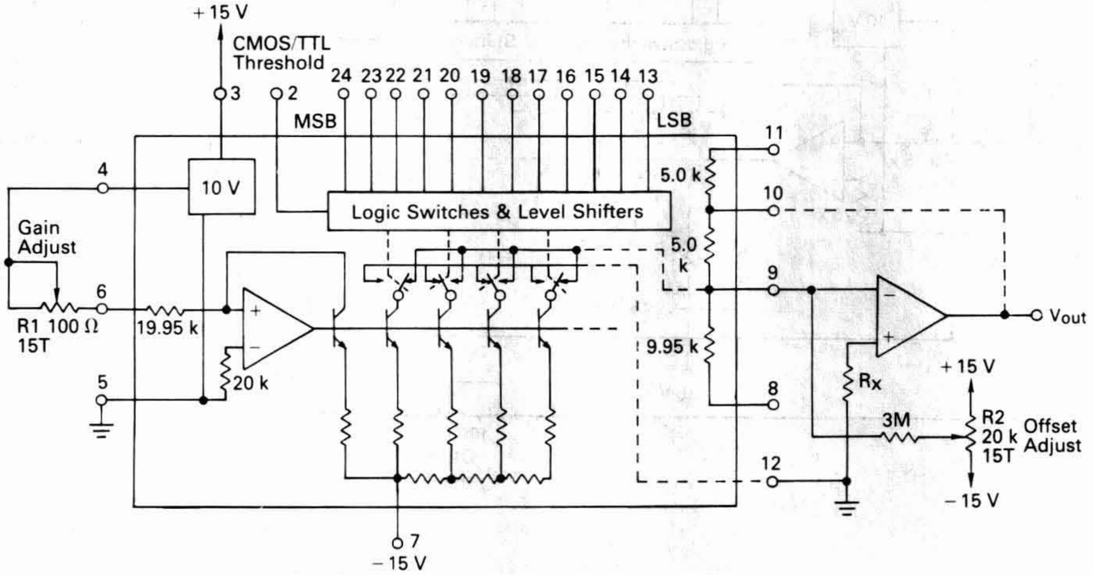
**Compliance Voltage Range** — The output terminal voltage range which will provide specified output resistance and current characteristics. The compliance voltage is specified with $V_{EE} = -15$. The compliance voltage range follows as $V_{EE}$ is varied.

**Power Supply Sensitivity** — The change in full scale current caused by a change in $V_{EE}$ or $V_{CC}$ expressed in ppm of full scale current per percent change in $V_{EE}$ or $V_{CC}$.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, MC3512: $T_A$ = −55 to 125°C, MC3412: $T_A$ = 0 to +70°C All tests performed using internal reference, unless otherwise noted.)

| Characteristic | Symbol | MC3512 | | | MC3412 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| TTL Digital Logic Levels (All Bits)<br>(Pin 2 open circuit)<br>13.5 ≤ $V_{CC}$ ≤ 16.5 V<br>Bit On, Logic "1"<br>Bit Off, Logic "0" | $V_{IH}$<br>$V_{IL}$ | 2.0<br>— | —<br>— | —<br>0.8 | 2.0<br>— | —<br>— | —<br>0.8 | V |
| CMOS Digital Logic Levels (All Pins)<br>(Pin 2 tied to Pin 3)<br>13.5 ≤ $V_{CC}$ ≤ 16.5 V<br>Bit On, Logic "1"<br>Bit Off, Logic "0" | $V_{IH}$<br>$V_{IL}$ | 70% $V_{CC}$<br>— | —<br>— | —<br>30% $V_{CC}$ | 70% $V_{CC}$<br>— | —<br>— | —<br>30% $V_{CC}$ | V |
| Digital Input Current (CMOS/TTL Levels)<br>Bit On, Logic "1"<br>Bit Off, Logic "0" | $I_{IH}$<br>$I_{IL}$ | —<br>— | +0.02<br>−2.0 | +1.0<br>−75 | —<br>— | +0.02<br>−2.0 | +1.0<br>−75 | µA |
| Programmable Output Range<br>See Figures 1 and 2 | | —<br>—<br>—<br>—<br>— | 0 to +5.0<br>−2.5 to +2.5<br>0 to +10<br>−5.0 to +5.0<br>−10 to +10 | —<br>—<br>—<br>—<br>— | —<br>—<br>—<br>—<br>— | 0 to +5.0<br>−2.5 to +2.5<br>0 to +10<br>−5.0 to +5.0<br>−10 to +10 | —<br>—<br>—<br>—<br>— | V |
| Output Current ($T_A$ = 25°C)<br>Unipolar (All Bits On)<br>Bipolar (All Bits On or Off) | $I_O$ | −1.6<br>±0.8 | −2.0<br>±1.0 | −2.4<br>±1.2 | −1.6<br>±0.8 | −2.0<br>±1.0 | −2.4<br>±1.2 | mA |
| Output Resistance ($T_A$ = 25°C)<br>(Exclusive of Span Resistors) | $R_O$ | 1.0 | 5.0 | — | 1.0 | 5.0 | — | MΩ |
| Output Capacitance ($T_A$ = 25°C) | $C_O$ | — | 25 | — | — | 25 | — | pF |
| Output Compliance Voltage Range | $V_{OC}$ | −5.0 | — | +10 | −5.0 | — | +10 | V |
| Nonlinearity ($T_A$ = 25 °C) | NL | —<br>— | ±¼<br>(0.006) | ±½<br>(0.012) | —<br>— | ±¼<br>(0.006) | ±½<br>(0.012) | LSB<br>% of FS |
| Nonlinearity | NL | —<br>— | ±½<br>(0.012) | ±¾<br>(0.018) | —<br>— | ±½<br>(.012) | ±¾<br>(0.018) | LSB<br>% of FS |
| Differential Nonlinearity ($T_A$ = 25°C) | | — | ±½ | ±¾ | — | ±½ | ±¾ | LSB |
| Differential Nonlinearity | Monotonicity Guaranteed | | | | | | | |
| Gain Error — Figure 1, R1 = Fixed 50 Ω<br>($T_A$ = 25°C) | | — | ±0.1 | ±0.25 | — | ±0.1 | ±0.25 | % of FS |
| Offset Error<br>Unipolar — Figure 1<br>Bipolar — Figure 2, R2 = Fixed 50 Ω<br>($T_A$ = 25°C) | | —<br>— | ±0.01<br>±0.05 | ±0.05<br>±0.15 | —<br>— | ±0.01<br>±0.05 | ±0.05<br>±0.15 | % of FS |
| Bipolar Zero Error — Figure 2,<br>R1 = R2 = Fixed 50 Ω ($T_A$ = 25°C) | | — | ±0.05 | ±0.15 | — | ±0.05 | ±0.15 | $ of FS |
| Gain Adjustment Range — Figure 1<br>($T_A$ = 25°C) | | ±0.25 | — | — | ±0.25 | — | — | % of FS |
| Bipolar Offset Adjustment Range —<br>Figure 2 ($T_A$ = 25°C) | | ±0.15 | — | — | ±0.15 | — | — | % of FS |
| Unipolar Zero Temperature Coefficient | | — | 1.0 | 2.0 | — | 1.0 | 2.0 | ppm/°C |
| Bipolar Zero Temperature Coefficient | | — | 5.0 | 10 | — | 5.0 | 10 | ppm/°C |
| Gain Temperature Coefficient, Full Scale | | — | 15 | 30 | — | 15 | 30 | ppm/°C |
| Differential Nonlinearity Temperature Coefficient | | — | 2.0 | — | — | 2.0 | — | ppm/°C |
| Settling Time to ½ LSB ($T_A$ = 25°C)<br>All Bits On-to-Off or Off-to-On | $t_s$ | — | 200 | 400 | — | 200 | 400 | ns |
| Reference Input Impedance<br>($T_A$ = 25°C) | $Z_{in}$ | 15 | 20 | 25 | 15 | 20 | 25 | kΩ |
| Reference Output Voltage ($T_A$ = 25°C) | $V_{RO}$ | 9.950 | 10.00 | 10.050 | 9.950 | 10.00 | 10.050 | Volts |
| Reference Output Current — Available to External Loads ($T_A$ = 25°C) | $I_{RO}$ | 1.5 | 2.5 | — | 1.5 | 2.5 | — | mA |
| Power Supply Current<br>$V_{CC}$ +13.5 to +16.5 Vdc<br>$V_{EE}$ −10.8 to −16.5 Vdc<br>($T_A$ = 25°C) | $I_{CC}$<br>$I_{EE}$ | —<br>— | 6.0<br>−8.0 | 10<br>−12 | —<br>— | 6.0<br>−8.0 | 10<br>−12 | mA |
| Power Supply Gain Sensitivity<br>$V_{CC}$ +13.5 to +16.5 Vdc<br>$V_{EE}$ −10.8 to −16.5 Vdc<br>($T_A$ = 25°C) | $PSSI_{FS+}$<br>$PSSI_{FS-}$ | —<br>— | 0.5<br>2.0 | 10<br>25 | —<br>— | 2.0<br>3.0 | 10<br>25 | ppm of FS/% |

FIGURE 1 — MC3412 IN TYPICAL UNIPOLAR CONNECTION SCHEME


+15 V
CMOS/TTL
Threshold
24 23 22 21 20 19 18 17 16 15 14 13
3
2
MSB
LSB
11
4
10 V
5.0 k
10
Gain
Adjust
Logic Switches & Level Shifters
5.0
k
9
6
R1 100 Ω
15T
19.95 k
9.95 k
Vout
+15 V
5
20 k
8
Rx
3M
R2
20 k
15T
Offset
Adjust
12
−15 V
7
−15 V

## UNIPOLAR DAC OPERATION

A typical circuit configuration for unipolar operation of MC3412 is shown in Figure 1.

### Step 1 — Output Range

Determine which output range is required. For +5.0 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier output and short Pin 9 to Pin 11. For +10 Volt FS range, connect Pin 10 to external operational amplifier output, Pin 11 remains unconnected.

### Step 2 — Zero Adjust

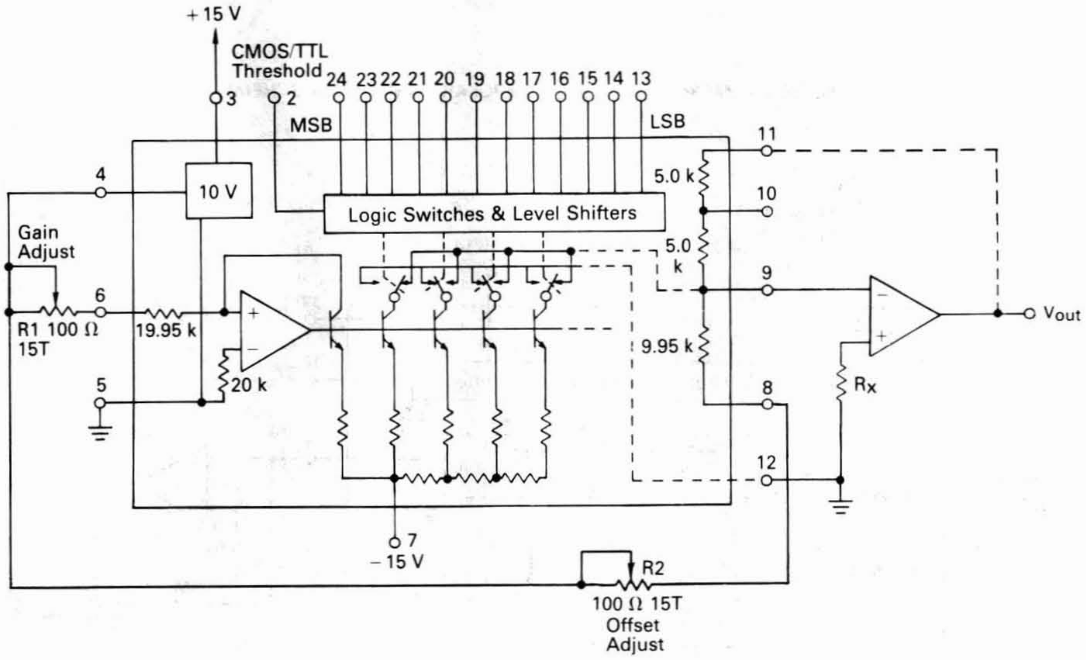
Turn all bits OFF and adjust R2 until external operational amplifier output is 0 Volts.

### Step 3 — Gain Adjust

Turn all bits ON. Adjust R1 until operational amplifier output reaches 4.9988 Volts for +5.0 Volt range or 9.9976 for +10 Volt range.

**See Application Note AN926 for further information.**

FIGURE 2 — MC3412 IN TYPICAL BIPOLAR CONNECTION SCHEME


+15 V
CMOS/TTL Threshold
24 23 22 21 20 19 18 17 16 15 14 13
3
2
MSB
LSB
11
4
10 V
5.0 k
10
Logic Switches & Level Shifters
5.0 k
9
Gain Adjust
6
R1 100 Ω 15T
19.95 k
9.95 k
Vout
5
20 k
8
Rx
12
7
−15 V
R2
100 Ω 15T Offset Adjust

## BIPOLAR DAC OPERATION

A typical circuit configuration for bipolar operation of MC3412 is shown in Figure 2.

**Step 1 — Output Range**

Determine which output range is required. For ±2.5 Volts full scale (FS) range, connect Pin 10 to output of external operational amplifier and short Pin 9 to Pin 11. For ±5.0 Volt FS range, connect Pin 10 to output of external operational amplifier, Pin 11 remains unconnected. For ±10 Volt FS range, connect Pin 11 to output of external operational amplifier, Pin 10 remains unconnected.

**Step 2 — Offset Adjust**

Turn all bits OFF. Adjust R2 until operational amplifier output is:

−2.5000 Volt for ±2.5 Volt range
−5.0000 Volt for ±5.0 Volt range
−10.0000 Volt for ±10 Volt range

**Step 3 — Gain Adjust (Bipolar Zero)**

Turn MSB ON and all other bits OFF. Adjust R1 until operational amplifier output is 0 Volts.

NOTES:

1. For TTL and DTL compatibility, leave Pin 2 open.
2. For high voltage CMOS compatibility, short Pin 2 to Pin 3.
3. Supplies should be bypassed with 0.1 μF capacitors.
4. In unipolar operation, $R_x$ should be made equal to the internal feedback resistor. In bipolar, $R_x$ equals the feedback resistor in parallel with 10 k.

**MOTOROLA**

# MC3417, MC3517
# MC3418, MC3518

## Specifications and Applications Information

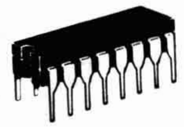
## CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

**LASER-TRIMMED INTEGRATED CIRCUIT**

### CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

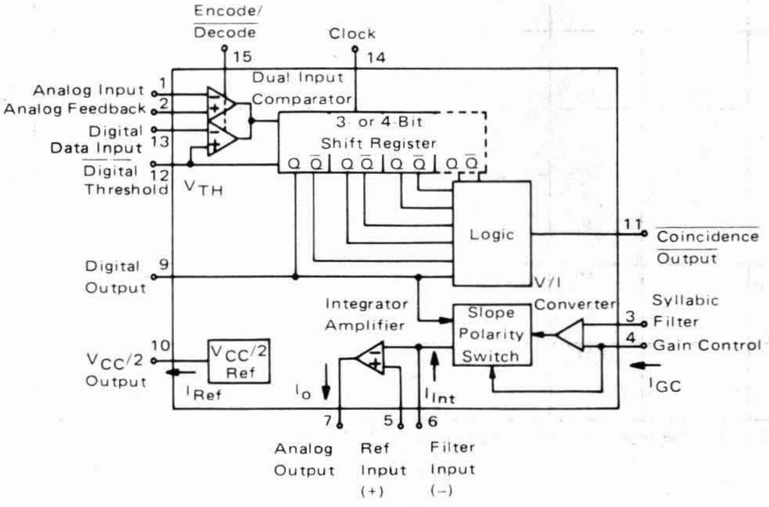
Providing a simplified approach to digital speech encoding/decoding, the MC3517/18 series of CVSDs is designed for military secure communication and commercial telephone applications. A single IC provides both encoding and decoding functions.

- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible $I^2L$ – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- MC3417/MC3517 has a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 has a 4-Bit Algorithm (Commercial Telephone)

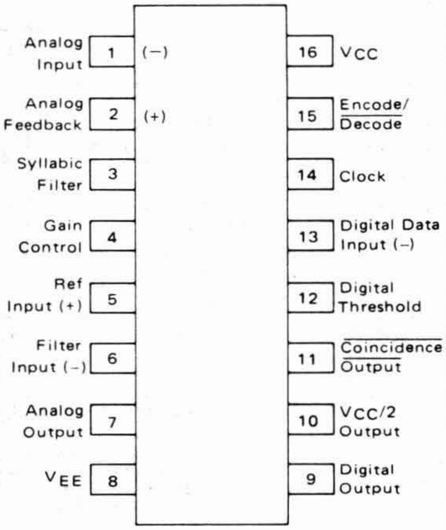


**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

### CVSD BLOCK DIAGRAM


Encode/Decode
15
Clock
14
Dual Input Comparator
Analog Input 1
Analog Feedback 2
Digital Data Input 13
Digital Threshold 12
V_TH
3 or 4 Bit Shift Register
Q Q̄ Q Q̄ Q Q̄ Q Q̄
Logic
11
Coincidence Output
Digital Output 9
V/I Converter
Integrator Amplifier
Slope Polarity Switch
Syllabic Filter 3
Gain Control 4
I_GC
V_CC/2 Output 10
V_CC/2 Ref
I_Ref
I_o
I_Int
7
5
6
Analog Output
Ref Input (+)
Filter Input (−)

### PIN CONNECTIONS


Analog Input 1 (−)
Analog Feedback 2 (+)
Syllabic Filter 3
Gain Control 4
Ref Input (+) 5
Filter Input (−) 6
Analog Output 7
V_EE 8
16 V_CC
15 Encode/Decode
14 Clock
13 Digital Data Input (−)
12 Digital Threshold
11 Coincidence Output
10 V_CC/2 Output
9 Digital Output

## MAXIMUM RATINGS

(All voltages referenced to $V_{EE}$, $T_A = 25^\circ C$ unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | −0.4 to +18 | Vdc |
| Differential Analog Input Voltage | $V_{ID}$ | ±5.0 | Vdc |
| Digital Threshold Voltage | $V_{TH}$ | −0.4 to $V_{CC}$ | Vdc |
| Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$) | $V_{Logic}$ | −0.4 to +18 | Vdc |
| Coincidence Output Voltage | $V_{O(Con)}$ | −0.4 to +18 | Vdc |
| Syllabic Filter Input Voltage | $V_{I(Syl)}$ | −0.4 to $V_{CC}$ | Vdc |
| Gain Control Input Voltage | $V_{I(GC)}$ | −0.4 to $V_{CC}$ | Vdc |
| Reference Input Voltage | $V_{I(Ref)}$ | $V_{CC}/2 - 1.0$ to $V_{CC}$ | Vdc |
| $V_{CC}/2$ Output Current | $I_{Ref}$ | −25 | mA |

## ELECTRICAL CHARACTERISTICS

($V_{CC} = 12$ V, $V_{EE}$ = Gnd, $T_A = 0^\circ C$ to $+70^\circ C$ for MC3417/18, $T_A = -55^\circ C$ to $+125^\circ C$ for MC3517/18 unless otherwise noted.)

| Characteristic | Symbol | MC3417/MC3517 | | | MC3418/MC3518 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Power Supply Voltage Range (Figure 1) | $V_{CCR}$ | 4.75 | 12 | 16.5 | 4.75 | 12 | 16.5 | Vdc |
| Power Supply Current (Figure 1) (Idle Channel) | $I_{CC}$ | | | | | | | mA |
| ($V_{CC}$ = 5.0 V) | | — | 3.7 | 5.0 | — | 3.7 | 5.0 | |
| ($V_{CC}$ = 15 V) | | — | 6.0 | 10 | — | 6.0 | 10 | |
| Clock Rate | SR | — | 16 k | — | — | 32 k | — | Samples/s |
| Gain Control Current Range (Figure 2) | $I_{GCR}$ | 0.001 | — | 3.0 | 0.001 | — | 3.0 | mA |
| Analog Comparator Input Range (Pins 1 and 2) ($4.75\text{ V} \leq V_{CC} \leq 16.5\text{ V}$) | $V_I$ | 1.3 | — | $V_{CC} - 1.3$ | 1.3 | — | $V_{CC} - 1.3$ | Vdc |
| Analog Output Range (Pin 7) ($4.75\text{ V} \leq V_{CC} \leq 16.5\text{ V}$, $I_O = \pm 5.0$ mA) | $V_O$ | 1.3 | — | $V_{CC} - 1.3$ | 1.3 | — | $V_{CC} - 1.3$ | Vdc |
| Input Bias Currents (Figure 3) (Comparator in Active Region) | $I_{IB}$ | | | | | | | µA |
| Analog Input (I1) | | — | 0.5 | 1.5 | — | 0.25 | 1.0 | |
| Analog Feedback (I2) | | — | 0.5 | 1.5 | — | 0.25 | 1.0 | |
| Syllabic Filter Input (I3) | | — | 0.06 | 0.5 | — | 0.06 | 0.3 | |
| Reference Input (I5) | | — | −0.06 | −0.5 | — | −0.06 | −0.3 | |
| Input Offset Current (Comparator in Active Region) | $I_{IO}$ | | | | | | | µA |
| Analog Input/Analog Feedback $\lvert I1 - I2 \rvert$ – Figure 3 | | — | 0.15 | 0.6 | — | 0.05 | 0.4 | |
| Integrator Amplifier $\lvert I5 - I6 \rvert$ – Figure 4 | | — | 0.02 | 0.2 | — | 0.01 | 0.1 | |
| Input Offset Voltage V/I Converter (Pins 3 and 4) – Figure 5 | $V_{IO}$ | — | 2.0 | 6.0 | — | 2.0 | 6.0 | mV |
| Transconductance | gm | | | | | | | mA/mV |
| V/I Converter, 0 to 3.0 mA | | 0.1 | 0.3 | — | 0.1 | 0.3 | — | |
| Integrator Amplifier, 0 to ±5.0 mA Load | | 1.0 | 10 | — | 1.0 | 10 | — | |
| Propagation Delay Times (Note 1) | | | | | | | | µs |
| Clock Trigger to Digital Output | $t_{PLH}$ | — | 1.0 | 2.5 | — | 1.0 | 2.5 | |
| ($C_L$ = 25 pF to Gnd) | $t_{PHL}$ | — | 0.8 | 2.5 | — | 0.8 | 2.5 | |
| Clock Trigger to Coincidence Output | $t_{PLH}$ | — | 1.0 | 3.0 | — | 1.0 | 3.0 | |
| ($C_L$ = 25 pF to Gnd) | $t_{PHL}$ | — | 0.8 | 2.0 | — | 0.8 | 2.0 | |
| ($R_L$ = 4 kΩ to $V_{CC}$) | | | | | | | | |
| Coincidence Output Voltage – Low Logic State ($I_{OL(Con)}$ = 3.0 mA) | $V_{OL(Con)}$ | — | 0.12 | 0.25 | — | 0.12 | 0.25 | Vdc |
| Coincidence Output Leakage Current – High Logic State ($V_{OH}$ = 15.0 V, $0^\circ C \leq T_A \leq 70^\circ C$) | $I_{OH(Con)}$ | — | 0.01 | 0.5 | — | 0.01 | 0.5 | µA |

NOTE 1. All propagation delay times measured 50% to 50% from the negative going (from $V_{CC}$ to +0.4 V) edge of the clock.

## ELECTRICAL CHARACTERISTICS (continued)

| Characteristic | Symbol | MC3417/MC3517 Min | MC3417/MC3517 Typ | MC3417/MC3517 Max | MC3418/MC3518 Min | MC3418/MC3518 Typ | MC3418/MC3518 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Applied Digital Threshold Voltage Range (Pin 12) | $V_{TH}$ | +1.2 | – | $V_{CC} - 2.0$ | +1.2 | – | $V_{CC} - 2.0$ | Vdc |
| Digital Threshold Input Current ($1.2\ V \leq V_{th} \leq V_{CC} - 2.0\ V$) | $I_{I(th)}$ | | | | | | | µA |
| ($V_{IL}$ applied to Pins 13, 14 and 15) | | – | – | 5.0 | – | – | 5.0 | |
| ($V_{IH}$ applied to Pins 13, 14 and 15) | | – | -10 | -50 | – | -10 | -50 | |
| Maximum Integrator Amplifier Output Current | $I_O$ | ±5.0 | – | – | ±5.0 | – | – | mA |
| $V_{CC}/2$ Generator Maximum Output Current (Source only) | $I_{Ref}$ | +10 | – | – | +10 | – | – | mA |
| $V_{CC}/2$ Generator Output Impedance (0 to +10 mA) | $z_{Ref}$ | – | 3.0 | 6.0 | – | 3.0 | 6.0 | Ω |
| $V_{CC}/2$ Generator Tolerance ($4.75\ V \leq V_{CC} \leq 16.5\ V$) | $\epsilon r$ | – | – | ±3.5 | – | – | ±3.5 | % |
| Logic Input Voltage (Pins 13, 14 and 15) | | | | | | | | Vdc |
| Low Logic State | $V_{IL}$ | Gnd | – | $V_{th} - 0.4$ | Gnd | – | $V_{th} - 0.4$ | |
| High Logic State | $V_{IH}$ | $V_{th} + 0.4$ | – | 18.0 | $V_{th} + 0.4$ | – | 18.0 | |
| Dynamic Total Loop Offset Voltage (Note 2) – Figures 3, 4 and 5 | $\Sigma V_{offset}$ | | | | | | | mV |
| $I_{GC} = 12.0\ \mu A$, $V_{CC} = 12\ V$ | | | | | | | | |
| $T_A = 25^{\circ}C$ | | – | – | – | – | ±0.5 | ±1.5 | |
| $0^{\circ}C \leq T_A \leq +70^{\circ}C$ MC3417/18 | | – | – | – | – | ±0.75 | ±2.3 | |
| $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ MC3517/18 | | – | – | – | – | ±1.5 | ±4.0 | |
| $I_{GC} = 33.0\ \mu A$, $V_{CC} = 12\ V$ | | | | | | | | |
| $T_A = 25^{\circ}C$ | | – | ±2.5 | ±5.0 | – | – | – | |
| $0^{\circ}C \leq T_A \leq +70^{\circ}C$ MC3417/18 | | – | ±3.0 | ±7.5 | – | – | – | |
| $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ MC3517/18 | | – | ±4.5 | ±10 | – | – | – | |
| $I_{GC} = 12.0\ \mu A$, $V_{CC} = 5.0\ V$ | | | | | | | | |
| $T_A = 25^{\circ}C$ | | – | – | – | – | ±1.0 | ±2.0 | |
| $0^{\circ}C \leq T_A \leq +70^{\circ}C$ MC3417/18 | | – | – | – | – | ±1.3 | ±2.8 | |
| $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ MC3517/18 | | – | – | – | – | ±2.5 | ±5.0 | |
| $I_{GC} = 33.0\ \mu A$, $V_{CC} = 5.0\ V$ | | | | | | | | |
| $T_A = 25^{\circ}C$ | | – | ±4.0 | ±6.0 | – | – | – | |
| $0^{\circ}C \leq T_A \leq +70^{\circ}C$ MC3417/18 | | – | ±4.5 | ±8.0 | – | – | – | |
| $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ MC3517/18 | | – | ±5.5 | ±10 | – | – | – | |
| Digital Output Voltage | | | | | | | | Vdc |
| ($I_{OL} = 3.6\ mA$) | $V_{OL}$ | – | 0.1 | 0.4 | – | 0.1 | 0.4 | |
| ($I_{OH} = -0.35\ mA$) | $V_{OH}$ | $V_{CC} - 1.0$ | $V_{CC} - 0.2$ | – | $V_{CC} - 1.0$ | $V_{CC} - 0.2$ | – | |
| Syllabic Filter Applied Voltage (Pin 3) (Figure 2) | $V_{I(Syl)}$ | +3.2 | – | $V_{CC}$ | +3.2 | – | $V_{CC}$ | Vdc |
| Integrating Current (Figure 2) | $\lvert I_{Int} \rvert$ | | | | | | | |
| ($I_{GC} = 12.0\ \mu A$) | | 8.0 | 10 | 12 | 8.0 | 10 | 12 | µA |
| ($I_{GC} = 1.5\ mA$) | | 1.45 | 1.50 | 1.55 | 1.45 | 1.50 | 1.55 | mA |
| ($I_{GC} = 3.0\ mA$) | | 2.75 | 3.0 | 3.25 | 2.75 | 3.0 | 3.25 | mA |
| Dynamic Integrating Current Match ($I_{GC} = 1.5\ mA$) Figure 6 | $V_{O(Ave)}$ | – | ±100 | ±250 | – | ±100 | ±250 | mV |
| Input Current – High Logic State ($V_{IH} = 18\ V$) | $I_{IH}$ | | | | | | | µA |
| Digital Data Input | | – | – | +5.0 | – | – | +5.0 | |
| Clock Input | | – | – | +5.0 | – | – | +5.0 | |
| Encode/$\overline{\text{Decode}}$ Input | | – | – | +5.0 | – | – | +5.0 | |
| Input Current – Low Logic State ($V_{IL} = 0\ V$) | $I_{IL}$ | | | | | | | µA |
| Digital Data Input | | – | – | -10 | – | – | -10 | |
| Clock Input | | – | – | -360 | – | – | -360 | |
| Encode/$\overline{\text{Decode}}$ Input | | – | – | -36 | – | – | -36 | |
| Clock Input, $V_{IL} = 0.4\ V$ | | – | – | -72 | – | – | -72 | |

NOTE 2. Dynamic total loop offset ($\Sigma V_{offset}$) equals $V_{IO}$ (comparator) (Figure 3) minus $V_{IOX}$ (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. For the MC3417/MC3517, the clock frequency is 16.0 kHz. For the MC3418/MC3518, the clock frequency is 32.0 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to insure good idle channel performance.

## DEFINITIONS AND FUNCTION OF PINS

**Pin 1 – Analog Input**

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

**Pin 2 – Analog Feedback**

This is the non-inverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be pin 7 or a low pass filter output connected to pin 7. In a decode circuit pin 2 is not used and may be tied to $V_{CC}/2$ on pin 10, ground or left open.

The analog input comparator has bias currents of 1.5 μA max, thus the driving impedances of pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

**Pin 3 – Syllabic Filter**

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between pins 11 and 3. Typical time constant values of 6 ms to 50 ms are used in voice codecs.

**Pin 4 – Gain Control Input**

The syllabic filter voltage appears across $C_S$ of the syllabic filter and is the voltage between $V_{CC}$ and pin 3. The active voltage to current (V-I) converter drives pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into pin 4 ($I_{GC}$) is the syllabic filter voltage divided by the $R_x$ resistance. Figure 6 shows the relationship between $I_{GC}$ (x-axis) and the integrating current, $I_{Int}$ (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The $R_x$ resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

**Pin 5 – Reference Input**

This pin is the non-inverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as pin 1 and is tied to pin 10.

**Pin 6 – Filter Input**

This inverting op amp input is used to connect the integrator external components. The integrating current ($I_{Int}$) flows into pin 6 when the analog input (pin 1) is high with respect to the analog feedback (pin 2) in the encode mode or when the digital data input (pin 13) is high in the decode mode. For the opposite states, $I_{Int}$ flows out of Pin 6. Single integration systems require a capacitor and resistor between pins 6 and 7. Multipole configurations will have different circuitry. The resistance between pins 6 and 7 should always be between 8 kΩ and 13 kΩ to maintain good idle channel characteristics.

**Pin 7 – Analog Output**

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $V_{CC}/2$ to +6 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

**Pin 8 – $V_{EE}$**

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

**Pin 9 – Digital Output**

The digital output provides the results of the delta modulator's conversion. It swings between $V_{CC}$ and $V_{EE}$ and is CMOS or TTL compatible. Pin 9 is inverting with respect to pin 1 and non-inverting with respect to pin 2. It is clocked on the falling edge of pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for $V_{CC}$ = 12 V and $C_L$ = 25 pF to ground.

**Pin 10 – $V_{CC}/2$ Output**

An internal low impedance mid-supply reference is provided for use of the MC3417/18 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6 dBmo signal is expected across a 600 ohm input bias resistor, then pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from pin 10 to $V_{EE}$ is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

**Pin 11 – $\overline{\text{Coincidence Output}}$**

The duty cycle of this pin is proportional to the voltage across $C_S$. The coincidence output will be low whenever the content of the internal shift register is all 1s or all 0s. In the MC3417 the register is 3 bits long

## DEFINITIONS AND FUNCTIONS OF PINS (continued)

while the MC3418 contains a 4 bit register. Pin 11 is an open collector of an NPN device and requires a pull-up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of $R_P$ should be much less than $R_S$. In systems requiring different charge and discharge constants, the charging constant is $R_SC_S$ while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3 mA in any configuration. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for $R_L$ = 4 kΩ to +12 V and $C_L$ = 25 pF to ground.

**Pin 12 – Digital Threshold**

This input sets the switching threshold for pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Often it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above $V_{EE}$ for TTL interface.

**Pin 13 – Digital Data Input**

In a decode application, the digital data stream is applied to pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of pin 15. It is an inverting input with respect to pin 9. When pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 µs before and after the clock trigger for proper clocking.

**Pin 14 – Clock Input**

The clock input determines the data rate of the codec circuit. A 32K bit rate requires a 32 kHz clock. The switching threshold of the clock input is set by pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive-going pulse on the clock input is 300 ns, whereas for a negative-going pulse, it is 900 ns.

**Pin 15 – Encode/$\overline{\text{Decode}}$**

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through pin 13 in an encoder.

**Pin 16 – $V_{CC}$**

The power supply range is from 4.75 to 16.5 volts between pin $V_{CC}$ and $V_{EE}$.

FIGURE 1 – POWER SUPPLY CURRENT

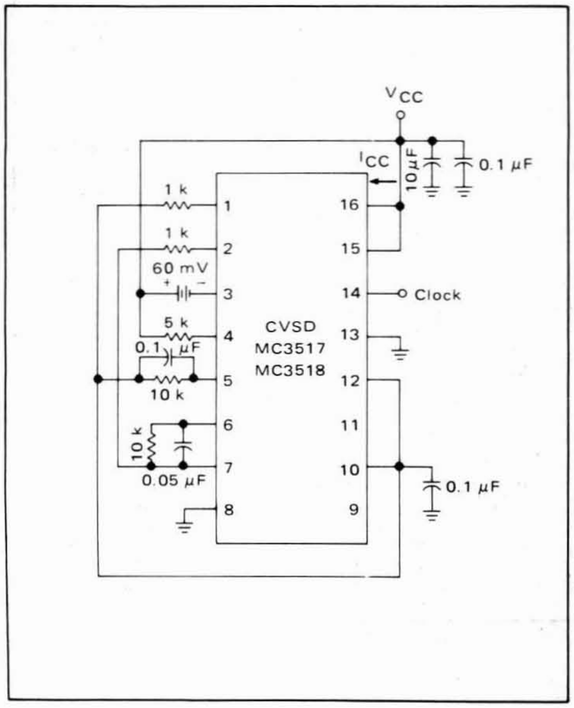
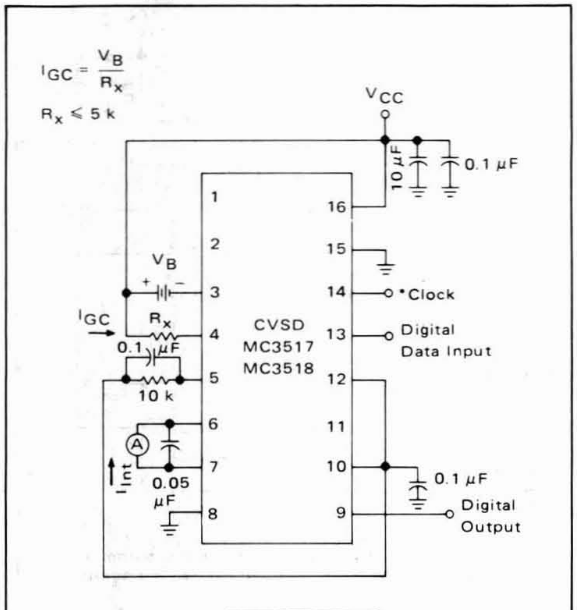


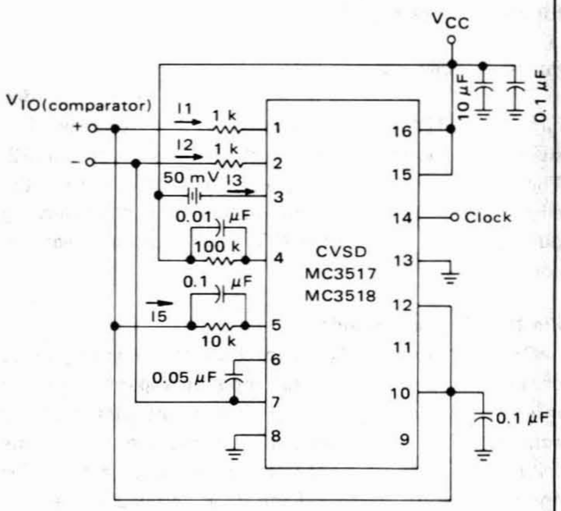
FIGURE 2 – $I_{GCR}$, GAIN CONTROL RANGE and $I_{Int}$ – INTEGRATING CURRENT



Note: Digital Output = $\overline{\text{Digital Data Input}}$

•For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

FIGURE 3 – INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT


VCC
10 µF
0.1 µF
VIO(comparator)
+
–
I1
1 k
I2
1 k
50 mV
I3
0.01 µF
100 k
0.1 µF
I5
10 k
0.05 µF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
Clock
CVSD
MC3517
MC3518
0.1 µF

Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

FIGURE 4 – INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT

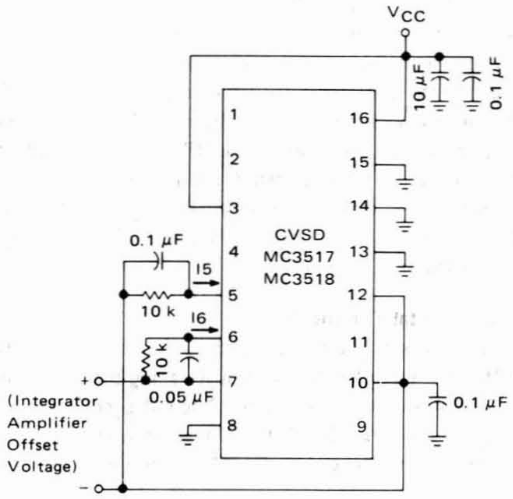
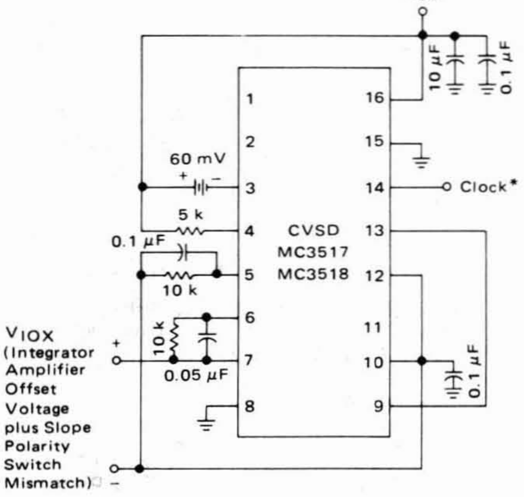

VCC
10 µF
0.1 µF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
CVSD
MC3517
MC3518
0.1 µF
I5
10 k
I6
10 k
0.05 µF
+
(Integrator Amplifier Offset Voltage)
–
0.1 µF

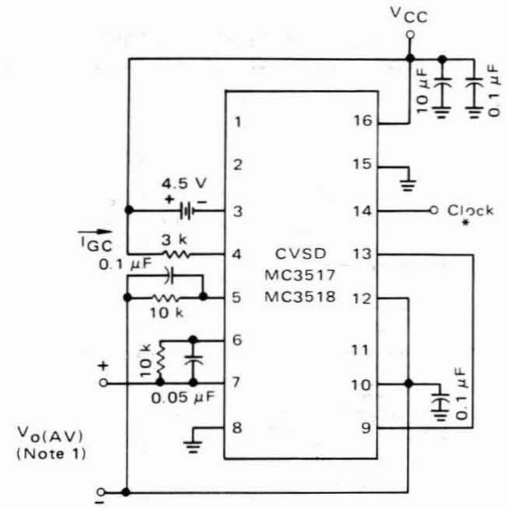
FIGURE 5 – V/I CONVERTER OFFSET VOLTAGE, $V_{IO}$ and $V_{IOX}$

*32 kHz MC3418/MC3518
16 kHz MC3417/MC3517


VCC
10 µF
0.1 µF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
60 mV
+
–
5 k
0.1 µF
10 k
10 k
0.05 µF
CVSD
MC3517
MC3518
Clock*
0.1 µF
VIOX (Integrator Amplifier Offset Voltage plus Slope Polarity Switch Mismatch)
+
–

Note: $V_{IOX}$ is the average voltage of the triangular waveform observed at the measurement points.

FIGURE 6 – DYNAMIC INTEGRATING CURRENT MATCH


VCC
10 µF
0.1 µF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
4.5 V
+
–
IGC
3 k
0.1 µF
10 k
10 k
0.05 µF
+
CVSD
MC3517
MC3518
Clock*
0.1 µF
Vo(AV)
(Note 1)
–

*32 kHz MC3418/MC3518
16 kHz MC3417/MC3517

Notes: 1. $V_{o(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with $I_{GC}$ = 1.5 mA.
2. See Note 2 of the Electrical Characteristics, page 3.

## TYPICAL PERFORMANCE CURVES

FIGURE 7 – TYPICAL $I_{Int}$ versus $I_{GC}$ (Mean ± 2σ)

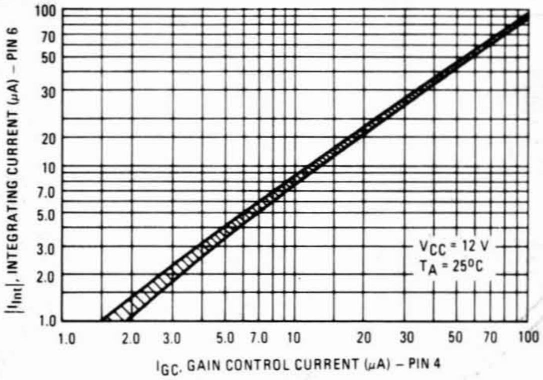


FIGURE 8 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus $V_{CC}$

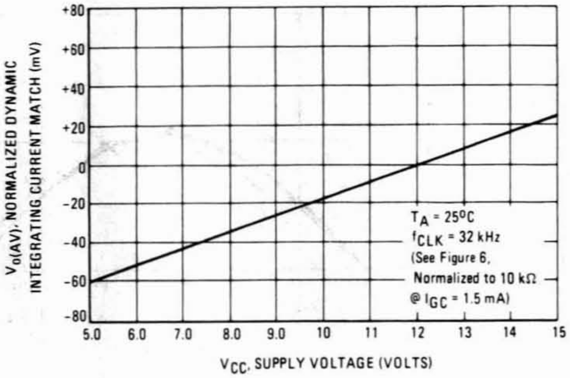


FIGURE 9 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY

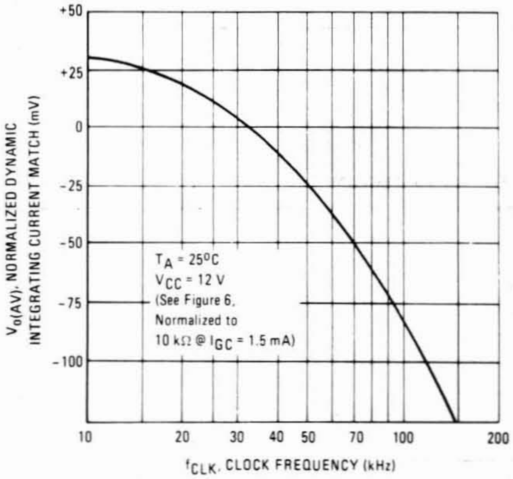


FIGURE 10 – DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY

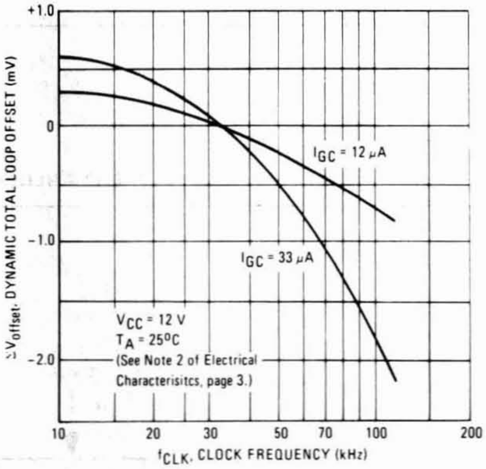
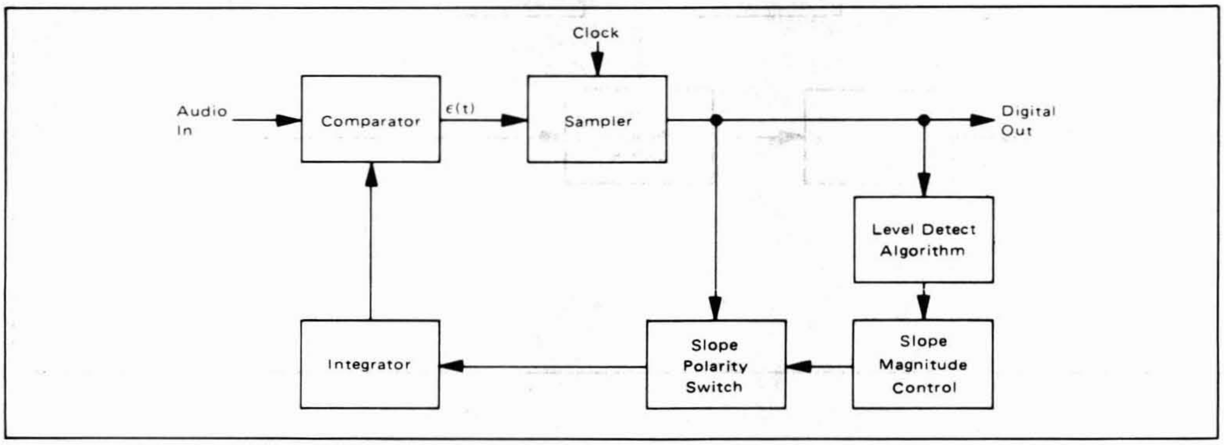


FIGURE 11 – BLOCK DIAGRAM OF THE CVSD ENCODER



Clock
Audio
In
Comparator
ε(t)
Sampler
Digital
Out
Level Detect
Algorithm
Integrator
Slope
Polarity
Switch
Slope
Magnitude
Control

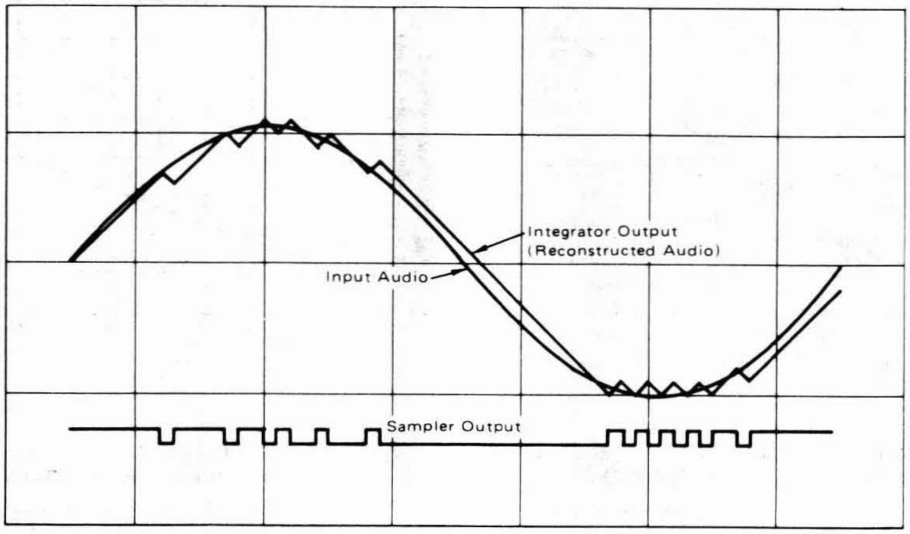


FIGURE 12 – CVSD WAVEFORMS

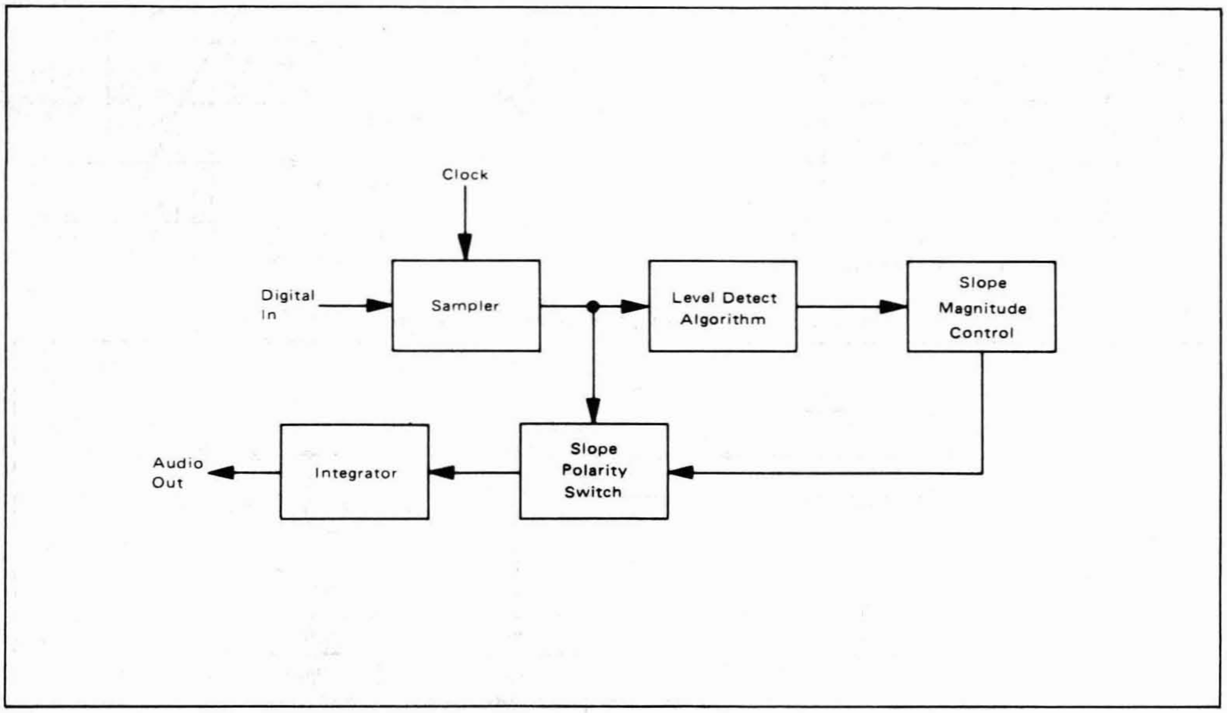
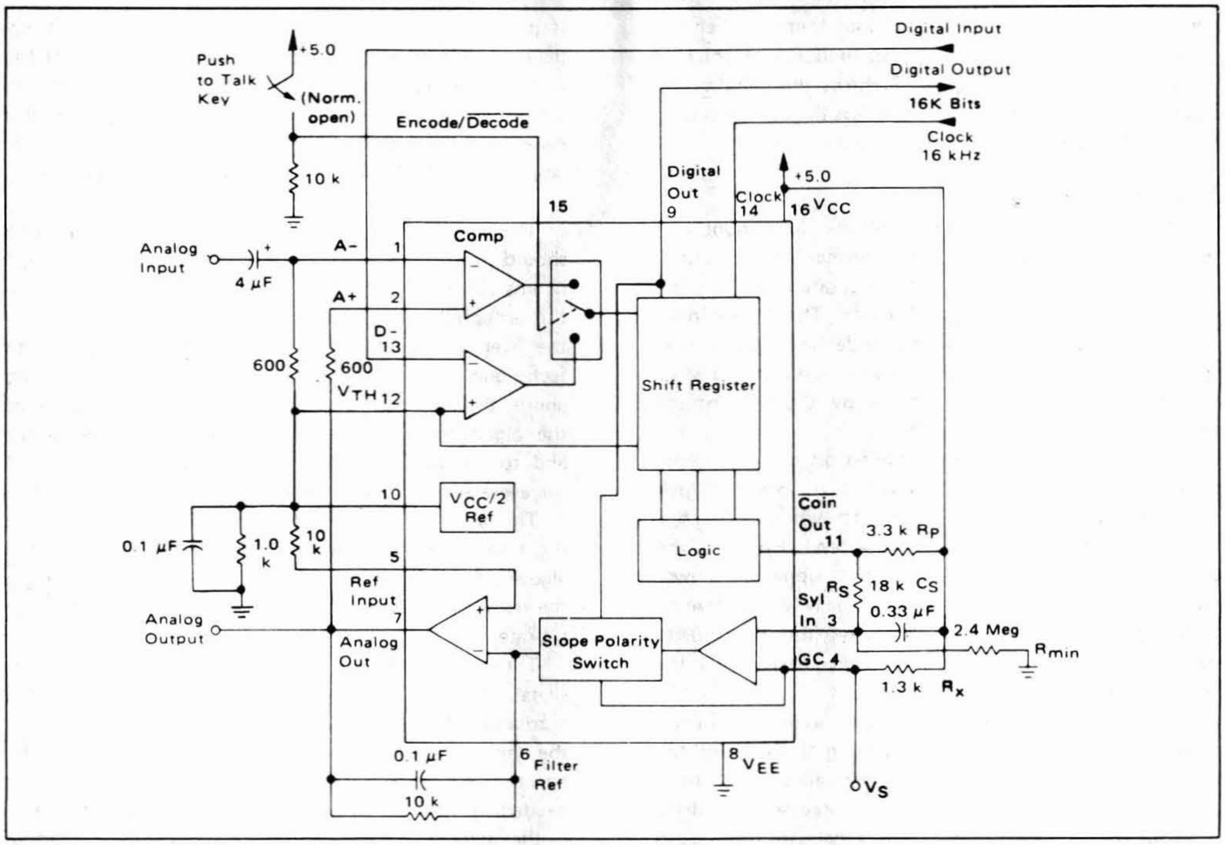

Clock
Digital
In
Sampler
Level Detect
Algorithm
Slope
Magnitude
Control
Slope
Polarity
Switch
Integrator
Audio
Out

FIGURE 13 – BLOCK DIAGRAM OF THE CVSD DECODER

FIGURE 14 – 16 kHz SIMPLEX VOICE CODEC
(Using MC3417, Single Pole Companding and Single Integration)


Push to Talk Key
+5.0
(Norm. open)
10 k
Encode/Decode
15
Digital Input
Digital Output
16K Bits
Clock 16 kHz
Digital Out 9
Clock 14
+5.0
16 VCC
Analog Input
4 μF
A- 1
A+ 2
Comp
D- 13
600
600
VTH 12
Shift Register
10
VCC/2 Ref
0.1 μF
1.0 k
10 k
5
Ref Input 7
Coin Out 11
3.3 k Rp
Logic
RS 18 k CS
Syl In 3
0.33 μF
2.4 Meg
Rmin
GC 4
1.3 k Rx
Analog Output
Analog Out
Slope Polarity Switch
0.1 μF
6 Filter Ref
10 k
8 VEE
VS

## CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

### The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to

## CIRCUIT DESCRIPTION (continued)

zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

**The Companding Algorithm**

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 or 4 bits long depending on the application. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communciations requirements.

## APPLICATIONS INFORMATION

### CVSD DESIGN CONSIDERATIONS

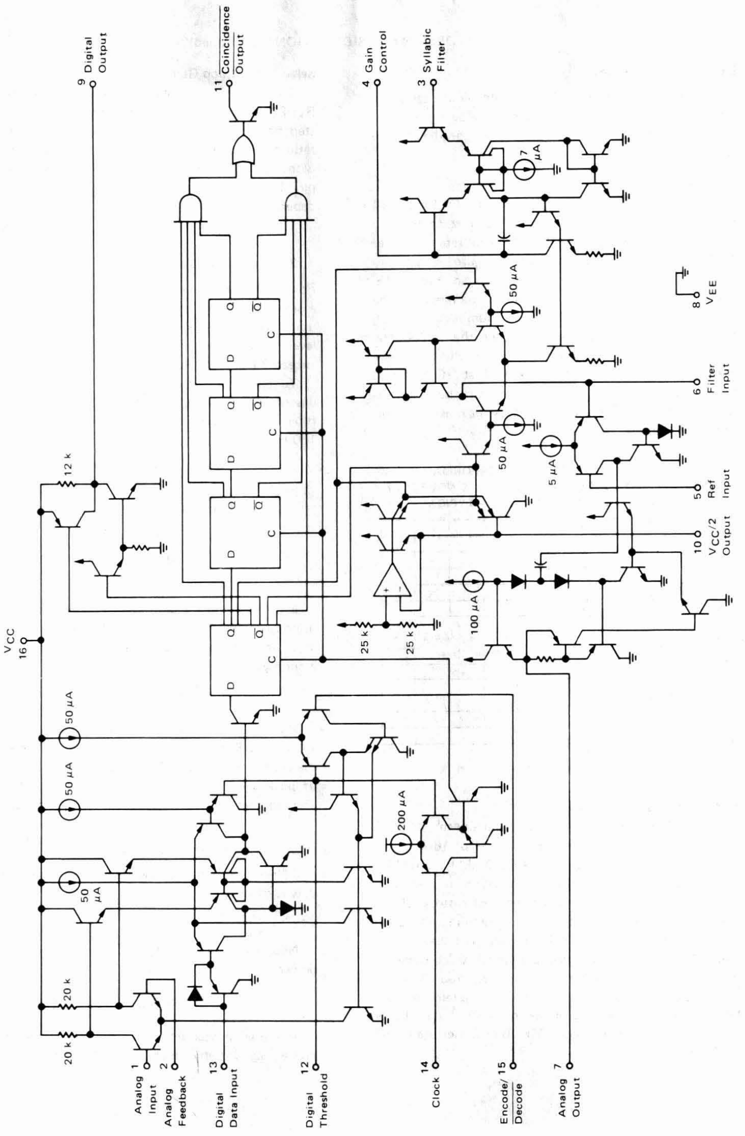
A simple CVSD encoder using the MC3417 or MC3418 is shown in Figure 14. These ICs are general purpose CVSD building blocks which allow the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC3417 and MC3418. There are seven design considerations involved in designing these basic CVSD building blocks into a specific codec application.

These are listed below:

1. Selection of clock rate
2. Required number of shift register bits
3. Selection of loop gain
4. Selection of minimum step size
5. Design of integration filter transfer function
6. Design of syllabic filter transfer function
7. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 5 and 6 are reduced to their simplest form. The syllabic and integration filters are both single pole networks. The selection of items 1 through 4 govern the codec performance.

CVSD CIRCUIT SCHEMATIC


9 Digital Output
11 Coincidence Output
4 Gain Control
3 Syllabic Filter
7 μA
50 μA
8 VEE
6 Filter Input
5 μA
50 μA
5 Ref Input
10 VCC/2 Output
100 μA
12 k
VCC 16
D Q Q̄ C
25 k
25 k
50 μA
50 μA
200 μA
50 μA
20 k
20 k
1 Analog Input
2 Analog Feedback
13 Digital Data Input
12 Digital Threshold
14 Clock
15 Encode/Decode
7 Analog Output

---

## CVSD DESIGN CONSIDERATIONS (continued)

**Minimum Step Size**

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one-zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC3417 is tested to ensure that a 20 mVp-p minimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one-zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1-0 pattern.

To set the idle channel step size, the value of $R_{min}$ must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor ($C_S$) would decay to zero. However, the voltage divider of $R_S$ and $R_{min}$ (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R} + C\frac{dV_o}{dt}$$

For values of $V_o$ near $V_{CC}/2$ the $V_o/R$ term is negligible; thus

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where $\Delta T$ is the clock period and $\Delta V_o$ is the desired peak-to-peak value of the idle output. For a 16K-bit system using the circuit in Figure 14

$$I_i = \frac{0.1\ \mu F\ \ 20\ mV}{62.5\ \mu s} = 33\ \mu A$$

The voltage on $C_S$ which produces a 33 μA current is determined by the value of $R_x$.

$$I_i R_x = V_S\text{min};\ \text{for } 33\ \mu A,\ V_S\text{min} = 41.6\ mV$$

In Figure 14 $R_S$ is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of $R_S$ and $R_{min}$ must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_{Smin} \qquad R_{min} \simeq 2.4\ M\Omega$$

Having established these four parameters — clock rate, number of shift register bits, loop gain and minimum step size — the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

## INCREASING CVSD PERFORMANCE

## CVSD DESIGN CONSIDERATIONS (continued)

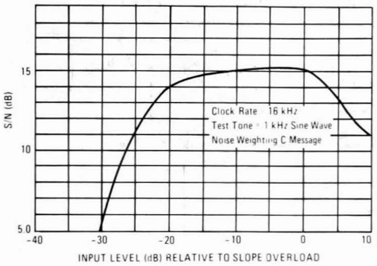
### Layout Considerations

Care should be exercised to isolate all digital signal paths (pins 9, 11, 13, and 14) from analog signal paths (pins 1-7 and 10) in order to achieve proper idle channel performance.

### Clock Rate

With minor modifications the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4-wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above. Other codecs may use bit rates up to 200K bits/sec.

FIGURE 15 – SIGNAL-TO-NOISE PERFORMANCE OF MC3417 WITH SINGLE INTEGRATION, SINGLE-POLE AND COMPANDING AT 16K BITS – TYPICAL



### Shift Register Length (Algorithm)

The MC3417 has a three-bit algorithm and the MC3418 has a four-bit algorithm. For clock rates of 16 kHz and below, the 3-bit algorithm is well suited. For 32 kHz and higher clock rates, the 4-bit system is preferred. Since the algorithm records a fixed past history of the input signal, a longer shift register is required to obtain the same internal hsitory. At 16 bits and below, the 4-bit algorithm will produce a slightly wider dynamic range at the expense of level change response. Basically the MC3417 is designed for low bit rate systems and the MC3418 is intended for high performance, high bit rate system. At bit rates above 64K bits either part will work well.

### Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor $R_X$. $R_X$ must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R = 10\ k\Omega,\ C = 0.1\ \mu F$$

$$\frac{V_O}{I_i} = \frac{1}{C(S + 1/RC)} \equiv \frac{K}{S + \omega_O}$$

$$\omega_O = 2\pi f$$

$$10^3 = \omega_O = 2\pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single-pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_O}{R} + \frac{C_d V_O}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ V}{{}^*2(10\ k\Omega)} + \frac{0.1\ \mu F(1.1)}{0.125\ ms} = 0.935\ mA$$

*The maximum voltage across RI when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_X = 0.25(V_{CC})\ \frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

---

## INCREASING CVSD PERFORMANCE (continued)

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network effects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_O}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_O}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_O{}^2}{\Delta T^2}\ .$$

The calculation of desired gain resistor $R_X$ then proceeds exactly as previously described.

### Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across $C_S/V_{CC}$.

The S/N performance may be improved by modifying

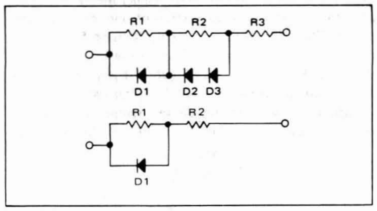
is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of $R_X$ in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor-diode networks are shown in Figure 17.

FIGURE 17 – RESISTOR-DIODE NETWORKS



If the performance of more complex diode networks is desired, the circuit in Figure 18 should be used. It

## TELEPHONE CARRIER QUALITY CODEC USING MC3418 (continued)

### The Active Companding Network

The unique feature of the codec in Figure 18 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across $C_S$ divided by the voltage swing of the coincidence output. In Figure 18, the voltage swing of pin 11 is 6 volts. The operating companding ratio is analoged by the voltage between pins 10 and 4 by means of the virtual short across pins 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

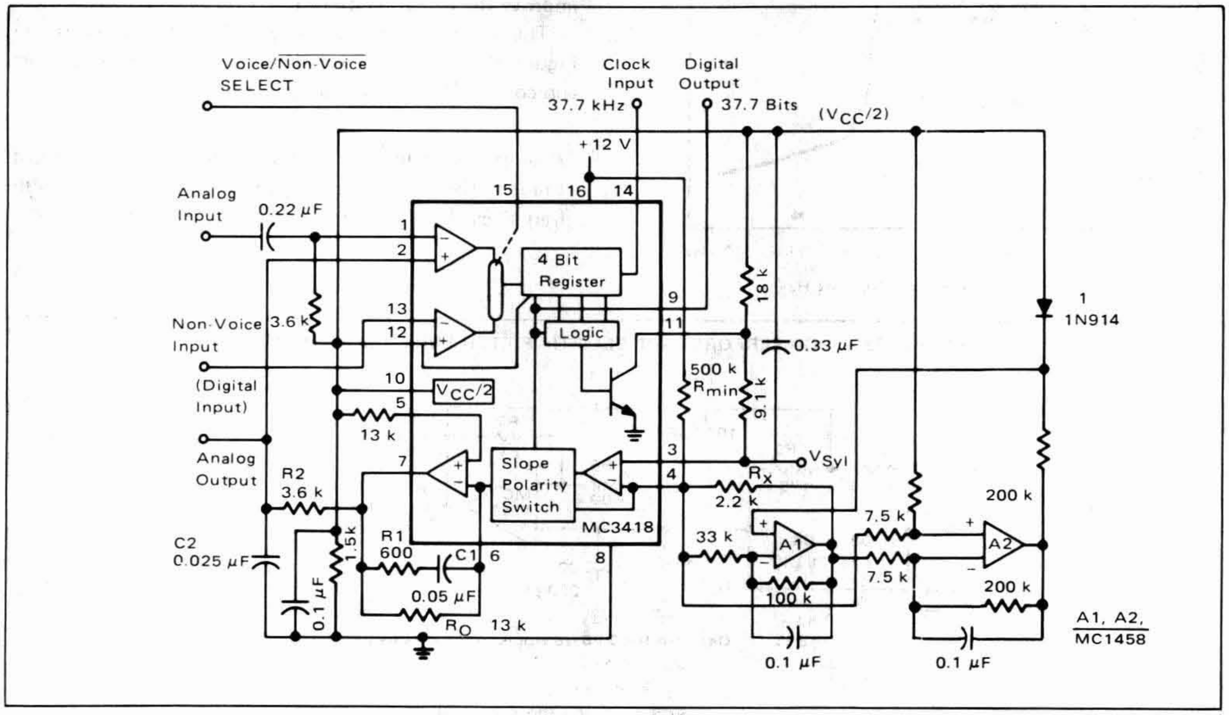
The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is ($V_{CC}/2$ − 0.7). The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6 V).

The present step size of the operating codec is directly related to the voltage across $R_X$, which established the integrator current. In Figure 18, the voltage across $R_X$ is amplified by the differential amplifier A2 whose output is single ended with respect to pin 10 of the IC.

For large signal inputs, the step size is large and the output of A2 is lower than 0.7 volts. Thus D1 is fully on. The present step size is not a factor in the step size control. However, the difference between 12% companding ratio and the instantaneous companding ratio at pin 4 is amplified by A1. The output of A1 changes the voltage across $R_X$ in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on $R_X$, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across $R_X$ and the gain of A2

FIGURE 18 — TELEPHONE QUALITY DELTAMOD CODER
(Both double integration and active companding control are used to obtain improved CVSD performance. Laser trimming of the integrated circuit provides reliable idle channel and step size range characteristics.)

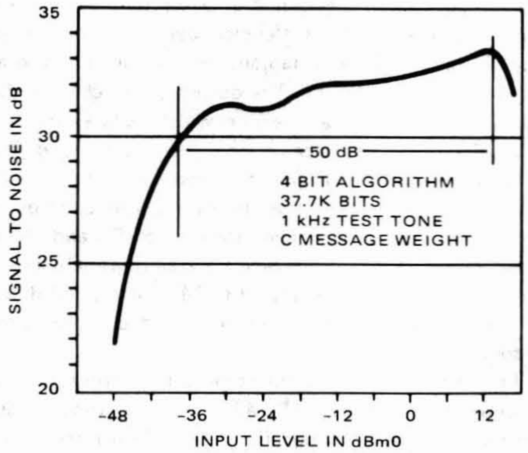


Voice/Non-Voice SELECT
Clock Input
37.7 kHz
Digital Output
37.7 Bits
(VCC/2)
+12 V
Analog Input
0.22 μF
15
16
14
1
2
4 Bit Register
9
18 k
1
1N914
13
12
Logic
11
Non-Voice Input
3.6 k
0.33 μF
(Digital Input)
10
VCC/2
500 k
Rmin
9.1 k
5
13 k
3
VSyl
7
Slope Polarity Switch
4
Rx
2.2 k
Analog Output
R2
3.6 k
7.5 k
200 k
MC3418
33 k
A1
A2
C2
0.025 μF
1.5k
R1
600
C1
6
8
7.5 k
0.1 μF
0.05 μF
100 k
200 k
RO
13 k
0.1 μF
0.1 μF
A1, A2, MC1458

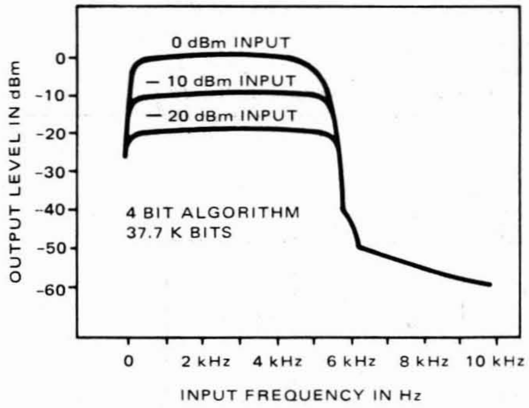
## TELEPHONE CARRIER QUALITY CODEC USING MC3418 (continued)

**FIGURE 19 – SIGNAL-TO-NOISE PERFORMANCE AND FREQUENCY RESPONSE**
**(Showing the improvement realized with the circuit in Figure 18.)**

a. SIGNAL-TO-NOISE PERFORMANCE OF TELEPHONY QUALITY DELTAMODULATOR



b. FREQUENCY RESPONSE versus INPUT LEVEL (SLOPE OVERLOAD CHARACTERISTIC)



and A1. The gain of A2 is also experimentally determined, but once determined, the circuitry is easily repeated.

With no input signal, the companding ratio at pin 4 goes to zero and the voltage across $R_X$ goes to zero. The voltage at the output of A2 becomes zero since there is no drop across $R_X$. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between $V_{CC}$ and $V_{CC}/2$ and is therefore independently selectable.

The signal to noise results of the active companding network are shown in Figure 19. A smooth 2 dB drop is realized from +12 dBm to −24 under the control of A1. At −24 dBm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm.

The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across $R_X$. The curves demonstrate that the level linearity has been maintained or improved.*

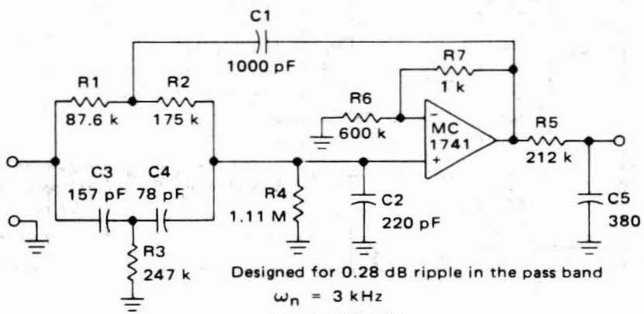
The codec in Figure 18 is designed specifically for 37.7K bit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 18 represents a significant step forward in the art and cost of CVSD codec designs.

---

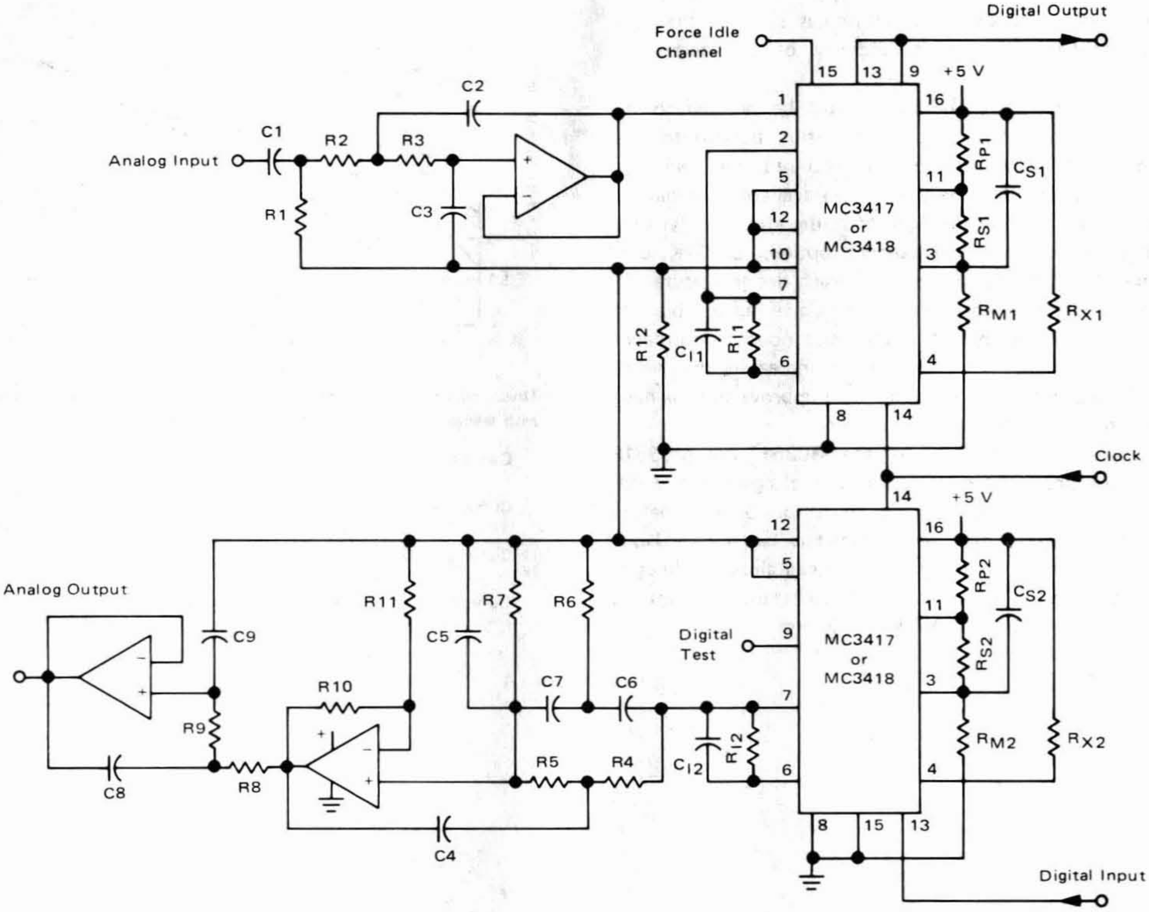
*A larger value for C2 is required in the decoder circuit than in the encoder to adjust the level linearity with frequency. In Figure 18, 0.050 μF would work well.

**FIGURE 20 – HIGH PERFORMANCE ELLIPTIC FILTER FOR CVSD OUTPUT**



Designed for 0.28 dB ripple in the pass band
$\omega_n$ = 3 kHz
$\omega_s$ = ≅ 6 kHz
AdB at $\omega_s$ and above 29.5 dB

**FIGURE 21 – FULL DUPLEX/32K BIT CVSD VOICE CODEC USING MC3517/18 AND MC3503/6 OP AMP**


Digital Output
Force Idle Channel
15
13
9
+5 V
16
1
2
5
12
10
7
6
11
3
4
8
14
C2
C1
R2
R3
Analog Input
R1
C3
MC3417
or
MC3418
$R_{P1}$
$C_{S1}$
$R_{S1}$
$R_{M1}$
$R_{X1}$
R12
$C_{11}$
$R_{11}$
Clock
14
+5 V
12
5
16
11
Analog Output
R11
R7
R6
C9
C5
Digital Test
9
MC3417
or
MC3418
$R_{P2}$
$C_{S2}$
$R_{S2}$
R10
C7
C6
7
3
R9
R5
R4
$C_{12}$
$R_{12}$
6
4
$R_{M2}$
$R_{X2}$
C8
R8
C4
8
15
13
Digital Input

**Codec Components**

$R_{X1}$, $R_{X2}$ – 3.3 kΩ
$R_{P1}$, $R_{P2}$ – 3.3 kΩ
$R_{S1}$, $R_{S2}$ – 100 kΩ
$R_{11}$, $R_{12}$ – 20 kΩ
$R_{12}$ – 1 kΩ
$R_{M1}$, $R_{M2}$ – 5 MΩ (MC3417)
Minimum step size = 20 mV
$R_{M1}$, $R_{M2}$ – 15 MΩ (MC3418)
Minimum step size = 6 mV

$C_{S1}$, $C_{S2}$ – 0.05 µF
$C_{11}$, $C_{12}$ – 0.05 µF

2 MC3417 (or MC3418)
1 MC3403 (or MC3406)

Note: All Res. 5%
All Cap. 5%

**Input Filter Specifications**

12 dB/Octave Rolloff above 3.3 kHz
6 dB/Octave Rolloff below 50 Hz

**Output Filter Specifications**

Break Frequency – 3.3 kHz
Stop Band – 9 kHz
Stop Band Atten. – 50 dB
Rolloff – > 40 dB/Octave

**Filter Components**

R1 – 965 Ω
R2 – 72 kΩ
R3 – 72 kΩ
R4 – 63.46 kΩ
R5 – 127 kΩ
R6 – 365.5 kΩ
R7 – 1.645 MΩ
R8 – 72 kΩ
R9 – 72 kΩ
R10 – 29.5 kΩ
R11 – 72 kΩ

C1 – 3.3 µF
C2 – 837 pF
C3 – 536 pF
C4 – 1000 pF
C5 – 222 pF
C6 – 77 pF
C7 – 38 pF
C8 – 837 pF
C9 – 536 pF

Note: All Res. 0.1% to 1%.
All Cap. 1.0%

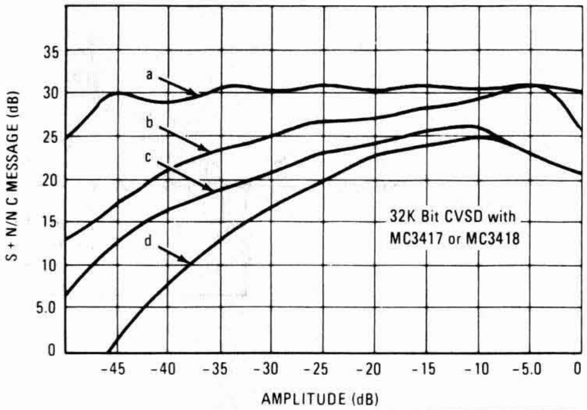
## COMPARATIVE CODEC PERFORMANCE

The salient feature of CVSD codecs using the MC3517 and MC3518 family is versatility. The range of codec complexity tradeoffs and bit rate is so wide that one cannot grasp the interdependency of parameters for voice applications in a few pages.

Design of a specific codec must be tailored to the digital channel bandwidth, the analog bandwidth, the quality of signal transmission required and the cost objectives. To illustrate the choices available, the data in Figure 22 compares the signal-to-noise ratios and dynamic range of various codec design options at 32K bits. Generally, the relative merits of each design feature will remain intact in any application. Lowering the bit rate will reduce the dynamic range and noise performance of all techniques. As the bit rate is increased, the overall performance of each technique will improve and the need for more complex designs diminishes.

Non-voice applications of the MC3517 and MC3518 are also possible. In those cases, the signal bandwidth and amplitude characteristics must be defined before the specification of codec parameters can begin. However, in general, the design can proceed along the lines of the voice applications shown here, taking into account the different signal bandwidth requirements.

**FIGURE 22 — COMPARATIVE CODEC PERFORMANCE — SIGNAL-TO-NOISE RATIO FOR 1 kHz TEST TONE**



These curves demonstrate the improved performance obtained with several codec designs of varying complexity.

Curve a — Complex companding and double integration (Figure 18 — MC3418)
Curve b — Double integration (Figure 21 using Figure 6 — MC3418)
Curve c — Single integration (Figure 21 — MC3418) with 6 mV step size
Curve d — Single integration (Figure 21 — MC3417) with 25 mV step size

MOTOROLA

# MC6108

## Product Preview

### 8-BIT MPU BUS-COMPATIBLE HIGH SPEED A-TO-D CONVERTER

The MC6108 is a microprocessor compatible, 8-bit, high speed analog-to-digital converter. Included are a precision reference, DAC, comparator, SAR, matched scale resistors, 3-state output buffers, and control logic. It is available in a standard 0.600″ wide 28-pin package. Conversion can be completed in under 1.0 μs and input voltage ranges of 0 to +10 V, 0 to +5.0 V, and −5.0 to +5.0 V can be accepted without additional external components. With appropriate external resistors, the converter can accommodate other input voltage ranges. 8-bit linearity and monotonic operation with no missing codes is guaranteed over temperature. Bus compatibility is provided for by the 3-state outputs (latches not required).

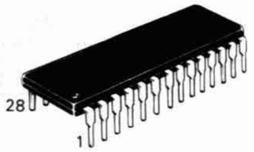
The MC6108 conversion time is short enough to allow most microprocessors to accept the data immediately after requesting a conversion. Applications include process control systems, servo control systems, waveform storage and signal processing, and others. The MC6148, a 24-pin version of the MC6108 (same specifications in a 0.300″ wide package), will be available in the near future.

This device is functionally and pin compatible with the AM6108.

- 1.0 μs Conversion Time (Typ)
- Microprocessor Compatible — Connect Directly to Data Bus
- Trimmed Internal Voltage Reference
- 0.1% Nonlinearity (Typ)
- Low Operating Voltage (+5.0 V, −5.2 V)
- Internal Matched Gain, Reference, and Offset Resistors
- Pin Programmable Unipolar or Bipolar Two's Complement
- Conversion Complete Available as Interrupt or Data Output
- Max Power Dissipation — 375 mW

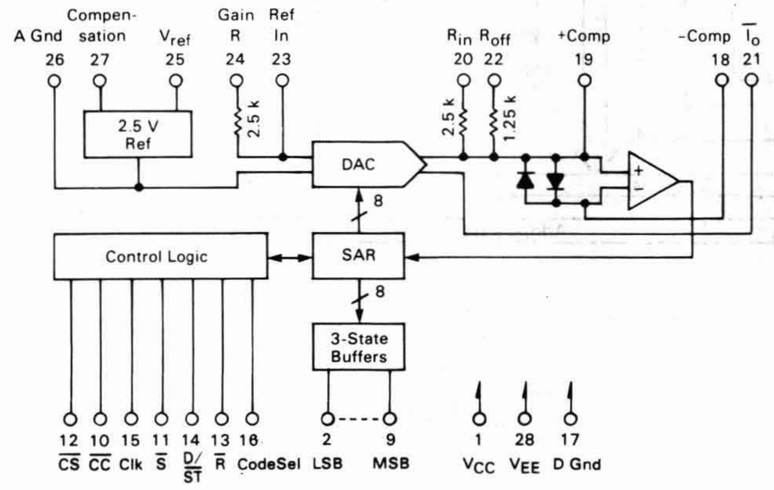
### 8-BIT MPU BUS-COMPATIBLE HIGH SPEED A-TO-D CONVERTER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

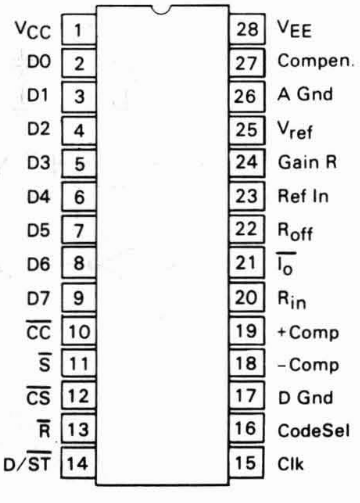


**CASE 710-02**
**CERAMIC**

**BLOCK DIAGRAM**


A Gnd 26
Compensation 27
Vref 25
Gain R 24
Ref In 23
Rin 20
Roff 22
+Comp 19
−Comp 18
Io 21
2.5 V Ref
2.5 k
2.5 k
1.25 k
DAC
8
Control Logic
SAR
8
3-State Buffers
12 CS
10 CC
15 Clk
11 S
14 D/ST
13 R
16 CodeSel
2 LSB
9 MSB
1 VCC
28 VEE
17 D Gnd

**PIN CONNECTIONS**


VCC 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
CC 10
S 11
CS 12
R 13
D/ST 14
28 VEE
27 Compen.
26 A Gnd
25 Vref
24 Gain R
23 Ref In
22 Roff
21 Io
20 Rin
19 +Comp
18 −Comp
17 D Gnd
16 CodeSel
15 Clk

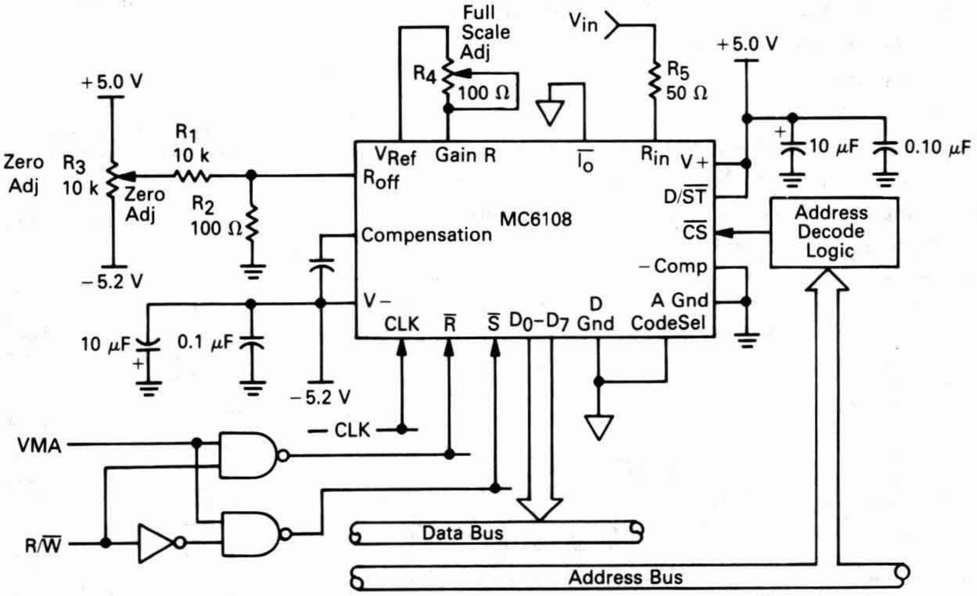
This document contains information on a new product. Specifications and information herein are subject to change without notice.

## PIN DESCRIPTIONS

| Symbol | Pin | Description |
|---|---|---|
| $V_{Ref}$ | 25 | Output of the internal 2.5 volt precision reference. |
| Gain R | 24 | Reference input gain resistor — nominally 2.5 k. Typically 2.5 volts is applied to this pin. |
| Ref In | 23 | This pin bypasses the above mentioned 2.5 k resistor. |
| $R_{in}$ | 20 | Analog input resistor. A 2.5 k resistor at the summing node of the comparator. Input current is compared with the DAC current at the node. |
| $R_{off}$ | 22 | Input offset resistor. A 1.25 k resistor at the comparator summing node. |
| $\overline{I_o}$ | 21 | DAC complementary current output. Must be grounded if unused. |
| −Comp | 18 | Comparator inverting input. Normally grounded — may be used for offset. |
| Clk | 15 | Clock input — TTL level. Used for internal timing. |
| D0–D7 | 2–9 | Data outputs — 3-state outputs. Pin 2 is the LSB, and Pin 9 is the MSB. |
| $V_{CC}$ | 1 | Connect to +5.0 volt (±5.0%) supply. |

| Symbol | Pin | Description |
|---|---|---|
| $V_{EE}$ | 28 | Connect to a −5.2 volt (±5.0%) supply. |
| A Gnd | 26 | Connect to analog ground. |
| +Comp | 19 | Comparator noninverting input. Used for nonstandard scales. |
| Compen | 27 | Reference supply compensation. An external capacitor is connected between Pin 27 and $V_{EE}$. |
| $\overline{CS}$ | 12 | Chip select — enables the MC6108. |
| $\overline{S}$ | 11 | Start conversion — an active low input which resets the SAR. When taken high, a conversion starts. |
| $\overline{R}$ | 13 | Read — an active low input which enables the 3-state outputs on the data bus. |
| D/$\overline{ST}$ | 14 | Data/Status control — When Logic "1", Pins 2–9 provide data. When Logic "0", Pin 9 provides CC status (same as Pin 10). |
| CodeSel | 16 | Code select. A Logic "1" provides data in binary offset format. A Logic "0" provides data in 2's complement. |
| $\overline{CC}$ | 10 | Conversion complete. Active low output indicates the end of a conversion. |
| D Gnd | 17 | Connect to digital ground. |

FIGURE 1 — UNIPOLAR CONFIGURATION


Full Scale Adj
$V_{in}$
+5.0 V
$R_4$
100 Ω
$R_5$
50 Ω
+5.0 V
$R_1$
10 k
Zero Adj
$R_3$
10 k
Zero Adj
$R_2$
100 Ω
−5.2 V
$V_{Ref}$
Gain R
$\overline{I_o}$
$R_{in}$
V+
$R_{off}$
D/$\overline{ST}$
MC6108
Compensation
$\overline{CS}$
−Comp
V−
D Gnd
A Gnd
CLK
$\overline{R}$
$\overline{S}$
$D_0$–$D_7$
CodeSel
10 μF
0.10 μF
Address Decode Logic
10 μF
0.1 μF
−5.2 V
CLK
VMA
R/$\overline{W}$
Data Bus
Address Bus

**MOTOROLA**

# MC6890

## MPU-BUS-COMPATIBLE 8-BIT D-TO-A CONVERTER

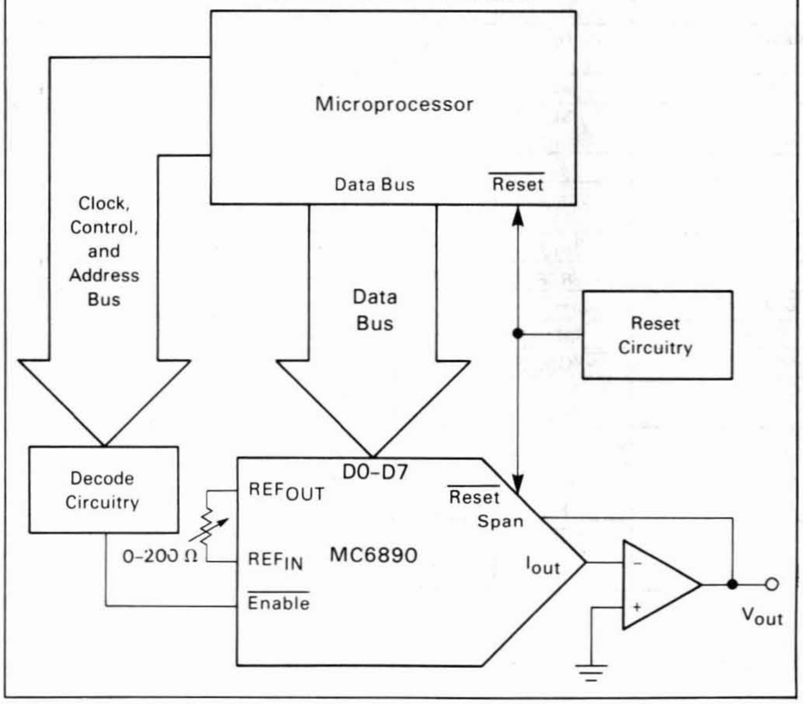
The MC6890 is a self-contained, bus-compatible, 8 bit (±0.19% accuracy) D-to-A converter system capable of interfacing directly with 8-bit microprocessors.

Available in both commercial and military temperature ranges, this monolithic converter contains master/slave registers to prevent transparency to data transitions during active enable; a laser-trimmed, low-TC, 2.5 V precision bandgap reference; and high stability, laser-trimmed, thin-film resistors for both reference input and output span and bipolar offset control.

A reset pin provides for overriding stored data and forcing $I_{out}$ to zero.

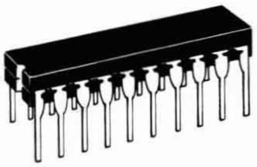
- Direct Data Bus Link with All Popular TTL Level MPU's
- ±1/2 LSB Nonlinearity Over Temperature
- Fast Settling Time: 200 ns Typ
- Internal 2.5-V Precision Laser-Trimmed Voltage Reference (May Also Be Used Externally)
- Minimum $\overline{\text{Enable}}$ Pulse Width: 70 ns
- Fast $\overline{\text{Enable}}$: 10 ns Maximum Data Hold Time
- $\overline{\text{Reset}}$ Pin to Override Data
- Output Voltage Ranges: +5, +10, +20, or ±2.5, ±5, ±10 Volts
- Low Power: 90 mW Typ
- +5 V and −5 V to −15 V Supplies

### OPERATION WITH AN MPU


Microprocessor
Data Bus
Reset
Clock, Control, and Address Bus
Data Bus
Reset Circuitry
Decode Circuitry
D0–D7
REF_OUT
Reset
Span
0–200 Ω
REF_IN
MC6890
I_out
Enable
−
+
V_out

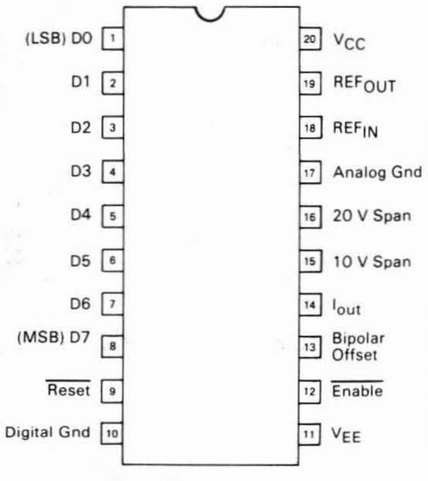
## 8-BIT MPU-BUS-COMPATIBLE DAC

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**L SUFFIX**
CASE 732-03

### PIN CONNECTIONS


(LSB) D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
(MSB) D7 8
Reset 9
Digital Gnd 10
20 V_CC
19 REF_OUT
18 REF_IN
17 Analog Gnd
16 20 V Span
15 10 V Span
14 I_out
13 Bipolar Offset
12 Enable
11 V_EE

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC6890L | 0° to +70°C | Ceramic DIP |
| MC6890AL | −55° to +125°C | Ceramic DIP |

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +7.0<br>−18 | Vdc |
| Digital Input Voltage, Pins 1-8, 12<br>Pin 9 | $V_{in}$ | −3.0 to +7.0<br>0 to +7.0 | Vdc |
| Applied Output Voltage | $V_{14}$ | $V_{EE}$ +2.0 to<br>$V_{EE}$ +24 | Vdc |
| Reference Amplifier Input | $V_{18}$ | ±7.5 | Vdc |
| Operating Temperature Range<br>MC6890L,<br>MC6890AL | $T_A$ | <br>0 to +70<br>−55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature | $T_J$ | +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = −12 V, Pin 18 loaded only by Pin 19 through 100 Ω. Reset high, $T_A = T_{low}$ to $T_{high}$(1), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Digital Input Logic Levels | | | | | Vdc |
| High Level, Logic 1 | $V_{IH}$ | 2.0 | — | — | |
| Low Level, Logic 0 | $V_{IL}$ | — | — | 0.8 | |
| Digital Input Current | | | | | |
| Data ($V_{IH}$ = 3.0 V) | $I_{IH}$ | — | 0.001 | 1.0 | μA |
| ($V_{IL}$ = 0.4 V) | $I_{IL}$ | — | 0.5 | −10 | μA |
| Enable ($V_{IH}$ = 3.0 V) | $I_{IH}$ | — | 0.001 | 1.0 | μA |
| ($V_{IL}$ = 0.4 V) | $I_{IL}$ | — | −6.5 | −100 | μA |
| $\overline{\text{Reset}}$ ($V_{IH}$ = 5.0 V) | $I_{IH}$ | — | 0.001 | 1.0 | μA |
| ($V_{IL}$ = 0.4 V) | $I_{IL}$ | — | −1.0 | −15 | μA |
| Full Scale Output Current — Unipolar | $I_O$ | −1.50 | −1.992 | −2.50 | mA |
| Unipolar Zero Output — All Bits Off ($T_A$ = 25°C) | — | — | 0.010 | 0.20 | μA |
| Output Voltage Temperature Coefficient | $TCV_O$ | | | | ppm of FSR/°C |
| Unipolar Zero | | — | ±1.0 | ±2.0 | |
| Bipolar Zero | | — | ±5.0 | ±15 | |
| Full Scale Range | | — | ±20 | ±50 | |
| Output Voltage, Full Scale Range (See Figure 3) ($T_A$ = 25°C) | $V_O$ | | | | Vdc |
| (10 V Span) | | 9.861 | 9.961 | 10.061 | |
| (20 V Span) | | 19.722 | 19.922 | 20.122 | |
| (5.0 V Span) | | 4.930 | 4.980 | 5.030 | |
| Output Voltage, Bipolar Zero (MSB on) (See Figure 4) ($T_A$ = 25°C) | $V_O$ | | | | mV |
| (10 V Span) | | — | 0 | ±20 | |
| (20 V Span) | | — | 0 | ±40 | |
| (5.0 V Span) | | — | 0 | ±10 | |
| DAC Output Resistance — Exclusive of Span Resistors ($T_A$ = 25°C) (See Figure 5) | $r_o$ | 1.0 | 5.0 | — | MΩ |
| Resolution | — | 8.0 | 8.0 | 8.0 | Bits |
| Nonlinearity — Relative Accuracy (See Terminology) | NL | — | — | ±0.19<br>(±1/2 LSB) | % |
| Differential Nonlinearity | Monotonicity Guaranteed | | | | |
| Differential Nonlinearity ($T_A$ = 25°C) (See Terminology) | — | — | — | ±0.29<br>(±3/4 LSB) | % |
| Reference Input Resistor | $R_{REF}$ | 3800 | 4900 | 6800 | Ω |
| Reference Output Voltage ($T_A$ = 25°C) | $V_{REF}$ | 2.470 | 2.500 | 2.530 | Vdc |
| Reference Output Impedance ($T_A$ = 25°C) $I_{load}$ = 0–3.0 mA | — | — | 0.3 | 1.0 | Ω |
| Reference Short Circuit Current ($T_A$ = 25°C) | $I_{REF}$ | 15 | 30 | 50 | mA |
| Reference Output Voltage Temperature Coefficient | $TCV_{O(REF)}$ | — | ±20 | — | ppm/°C |
| Power Supply Range | $V_{CC}$<br>$V_{EE}$ | 4.5<br>−16.5 | 5.0<br>−12 | 5.5<br>−4.5 | Vdc |
| Power Supply Current — All Bits Low | | | | | mA |
| ($V_{CC}$ = 5.0 V) | $I_{CC}$ | — | 10 | 20 | |
| ($V_{EE}$ = −5.0 V) | $I_{EE}$ | — | −10 | −15 | |
| ($V_{EE}$ = −15 V) | $I_{EE}$ | — | −10 | −15 | |
| Power Supply Rejection ($T_A$ = 25°C) | PSRR | | | | LSB |
| To $V_{CC}$ ($V_{CC}$ = 4.5 to 5.5 V) | | — | 0.010 | ±1/10 | |
| To $V_{EE}$ ($V_{EE}$ = −4.5 V to −16.5 V) | | — | 0.10 | ±1/2 | |
| Power Dissipation — All Bits Low | $P_D$ | | | | mW |
| For $V_{CC}$ = 4.5 V, $V_{EE}$ = −4.5 V | | — | 90 | 158 | |
| For $V_{CC}$ = 5.5 V, $V_{EE}$ = −16.5 V | | — | 220 | 358 | |

NOTE 1: $T_{low}$ = −55°C for MC6890A, 0° for MC6890
$T_{high}$ = +125°C for MC6890A, +70°C for MC6890

**AC SPECIFICATIONS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = −12 V, $T_A$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Current Settling Time<br>(Enable Positive Edge to ±1/2 LSB Output) | $t_s$ | — | 200 | 300* | ns |
| Data Setup Time | $t_{su(D)}$ | 70 | 40 | — | ns |
| Data Hold Time | $t_{h(D)}$ | 10 | 0 | — | ns |
| Pulse Widths<br>$\overline{\text{Enable}}$<br>$\overline{\text{Reset}}$ | <br>$t_{W(\overline{E})}$<br>$t_{W(\overline{R})}$ | <br>70<br>100* | <br>20<br>— | <br>—<br>— | ns |
| Propagation Delays<br>$\overline{\text{Enable}}$, Low to High<br>$\overline{\text{Reset}}$, High to Low<br>($I_O < 1.0\ \mu A$) | <br>$t_{PLH(\overline{E})}$<br>$t_{PHL(\overline{R})}$ | <br>—<br>— | <br>100<br>250 | <br>—<br>— | ns |

*Not 100% tested, guaranteed by design

FIGURE 1 — TIMING DIAGRAM

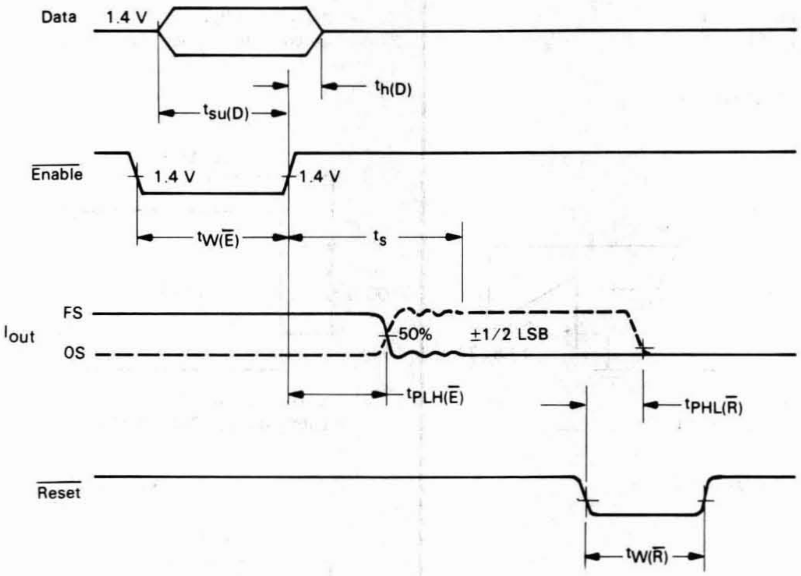
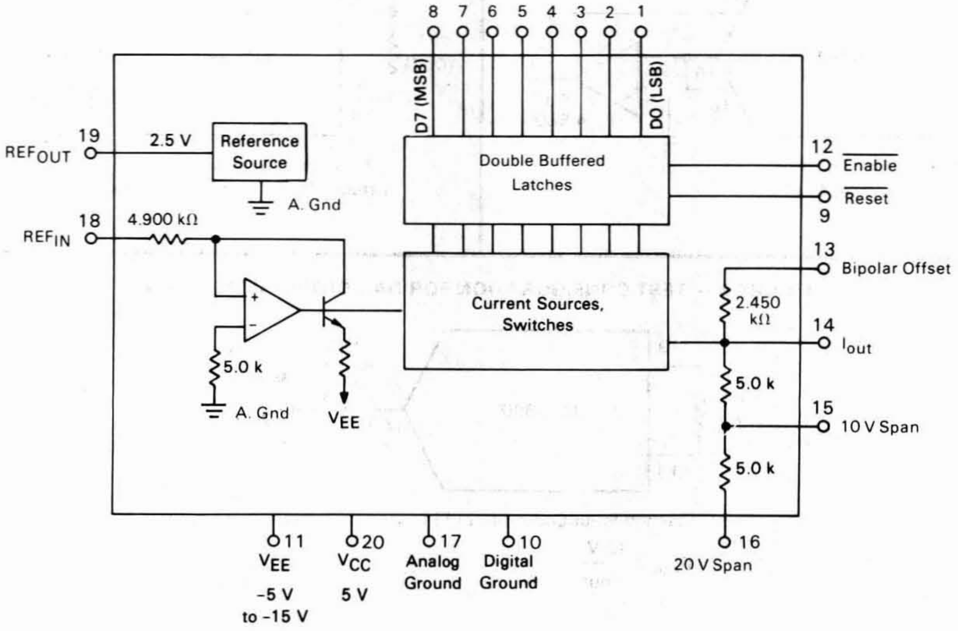

Data
1.4 V
$t_{h(D)}$
$t_{su(D)}$
$\overline{\text{Enable}}$
1.4 V
1.4 V
$t_{W(\overline{E})}$
$t_s$
FS
$I_{out}$
OS
50%
±1/2 LSB
$t_{PLH(\overline{E})}$
$t_{PHL(\overline{R})}$
$\overline{\text{Reset}}$
$t_{W(\overline{R})}$

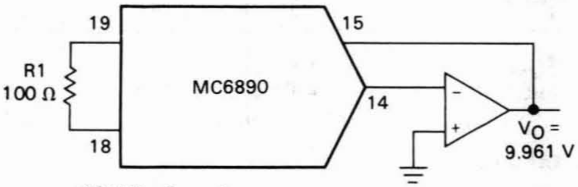
FIGURE 2 — BLOCK DIAGRAM


8 7 6 5 4 3 2 1
D7 (MSB)
D0 (LSB)
19
$REF_{OUT}$
2.5 V
Reference Source
A. Gnd
18
$REF_{IN}$
4.900 kΩ
5.0 k
A. Gnd
$V_{EE}$
Double Buffered Latches
Current Sources, Switches
12
$\overline{\text{Enable}}$
$\overline{\text{Reset}}$
9
13
Bipolar Offset
2.450 kΩ
14
$I_{out}$
5.0 k
15
10 V Span
5.0 k
16
20 V Span
11
$V_{EE}$
−5 V to −15 V
20
$V_{CC}$
5 V
17
Analog Ground
10
Digital Ground

## TEST FIGURES

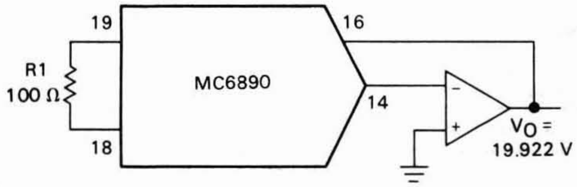
### UNIPOLAR CONFIGURATIONS

**FIGURE 3A**


19
15
R1
100 Ω
MC6890
14
18
$V_O$ =
9.961 V

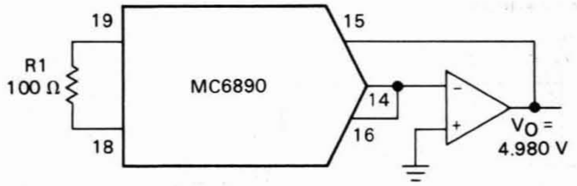
+10 V Configuration
Latched Input Code: 11111111

**FIGURE 3B**


19
16
R1
100 Ω
MC6890
14
18
$V_O$ =
19.922 V

+20 V Configuration
Latched Input Code: 11111111

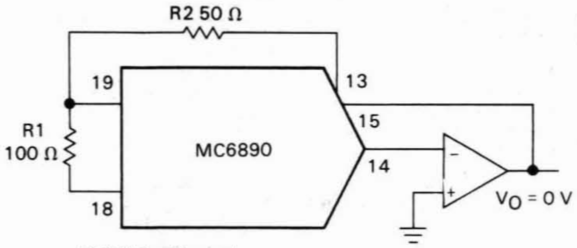
**FIGURE 3C**


19
15
R1
100 Ω
MC6890
14
16
18
$V_O$ =
4.980 V

+5.0 V Configuration
Latched Input Code: 11111111

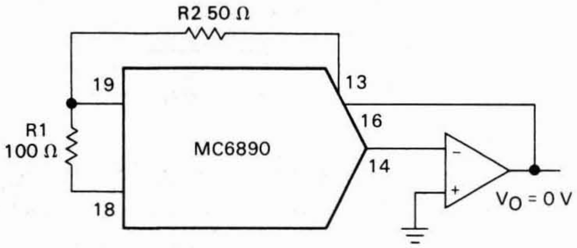
### BIPOLAR CONFIGURATIONS

**FIGURE 4A**


R2 50 Ω
19
13
15
R1
100 Ω
MC6890
14
18
$V_O$ = 0 V

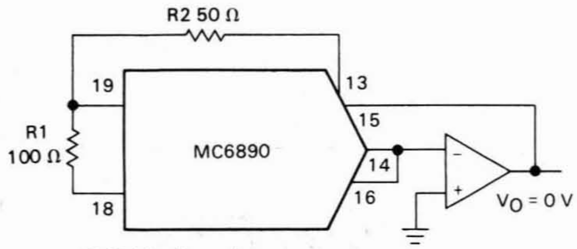
±5.0 V Configuration
Latched Input Code: 10000000

**FIGURE 4B**


R2 50 Ω
19
13
16
R1
100 Ω
MC6890
14
18
$V_O$ = 0 V

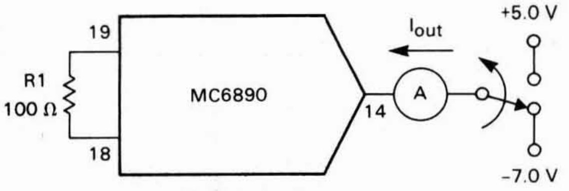
±10 V Configuration
Latched Input Code: 10000000

**FIGURE 4C**


R2 50 Ω
19
13
15
R1
100 Ω
MC6890
14
16
18
$V_O$ = 0 V

±2.5 V Configuration
Latched Input Code: 10000000

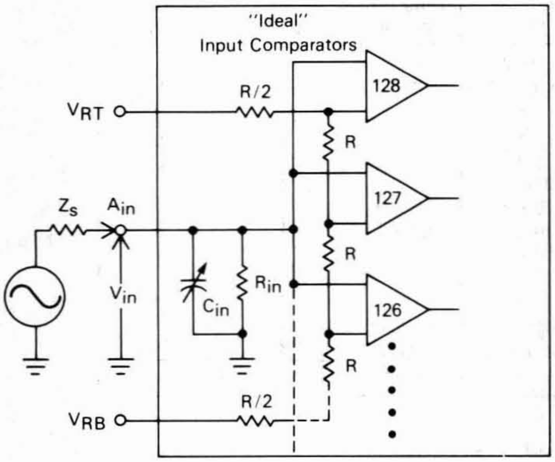
**FIGURE 5 — TEST CONFIGURATION FOR DAC OUTPUT IMPEDANCE**


+5.0 V
19
$I_{out}$
R1
100 Ω
MC6890
A
14
18
-7.0 V

Latched Input Code: 11111111

$$R_{out} = \frac{12\ V}{\Delta I_{out}}$$

FIGURE 2 — EQUIVALENT $R_{in}$ AND $C_{in}$ OF THE ANALOG INPUT


"Ideal"
Input Comparators
R/2
$V_{RT}$
128
R
127
$Z_s$
$A_{in}$
$V_{in}$
$R_{in}$
$C_{in}$
126
R
R/2
$V_{RB}$

$$R_{in} \simeq \frac{|V_{RT}-V_{RB}|}{400\ \mu A}$$

$$^*C_{in} \simeq \frac{30pF}{|V_{RT}-V_{RB}|}\,|V_{in}-V_{RB}| + 40\ pF$$

*Valid for $V_{RT} \geqslant V_{in} \geqslant V_{RB}$

$R \simeq 0.5\,\Omega$

$R_{in}$ — Effective input resistance representing the cumulative bias currents of the 128 input comparators.

$C_{in}$ — Equivalent input capacitance variable as a function of $V_{in}$.

FIGURE 4 — CLOCK INPUT IS STANDARD MECL INPUT WITH EMITTER FOLLOWER

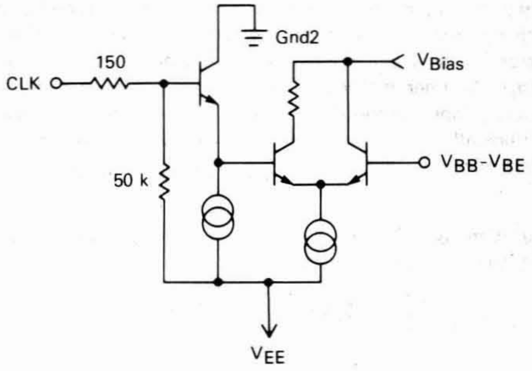
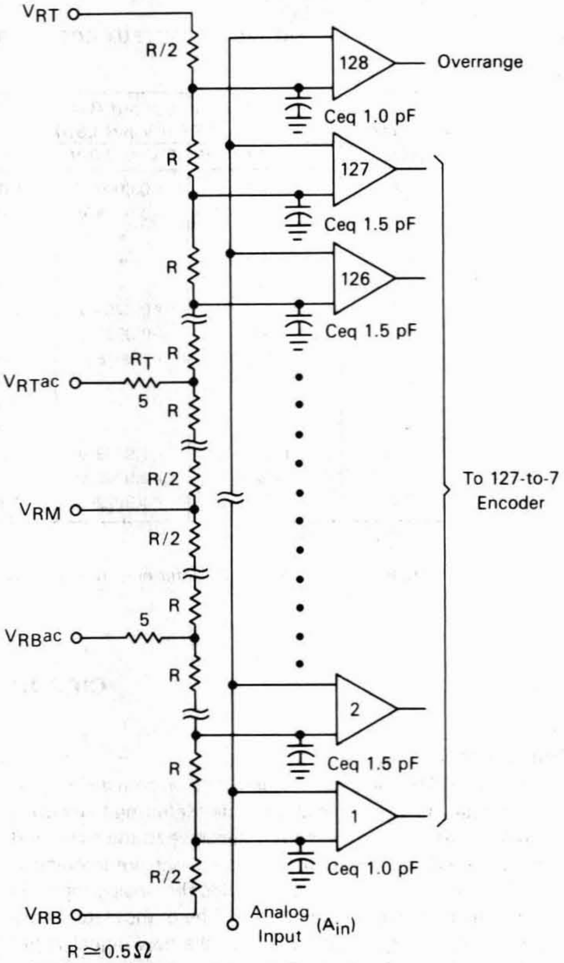

Gnd2
$V_{Bias}$
150
CLK
$V_{BB}$-$V_{BE}$
50 k
$V_{EE}$

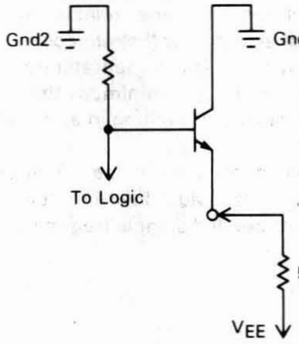
FIGURE 3 — EQUIVALENT CIRCUIT OF REFERENCE RESISTOR LADDER NETWORK


$V_{RT}$
R/2
128
Overrange
Ceq 1.0 pF
R
127
Ceq 1.5 pF
R
126
Ceq 1.5 pF
$R_T$
R
$V_{RT}ac$
5
R
R/2
$V_{RM}$
R/2
R
5
$V_{RB}ac$
R
2
R
Ceq 1.5 pF
1
Ceq 1.0 pF
R/2
$V_{RB}$
Analog Input ($A_{in}$)
To 127-to-7 Encoder

$R \simeq 0.5\,\Omega$

Ceq — The lumped equivalent value of capacitance representing the distributed capacitance for each resistor (R) and the input capacitance for each comparator.

FIGURE 5 — DIGITAL OUTPUTS ARE STANDARD MECL 10K WITH EMITTER FOLLOWERS CAPABLE OF SOURCING 25 mA. EXTERNAL PULL-DOWN RESISTORS ARE REQUIRED ON ALL OUTPUTS.


Gnd2
Gnd1
To Logic
510 Ω*
$V_{EE}$

Gnd1 is equivalent to MECL 10K $V_{CC1}$

Gnd2 is equivalent to MECL 10K $V_{CC2}$

*Recommended value of external pull-down resistors for all outputs.

FIGURE 6 — OUTPUT CODING FOR THE MC10315L/MC10317L DEVICES*

| Comparator Step | Analog Input Range (15.6 mV per LSB) | | | MC10315L Data Bits (D0-D6) | MC10317L Data Bits (D0-D6) | Overrange Bit (OVR) | $\overline{\text{Overrange Bit}}$ ($\overline{\text{OVR}}$) |
|---|---|---|---|---|---|---|---|
| | −2.0 V to 0 V | 0 V to 2.0 V | ±1.0 V | | | | |
| 000 | −2.0000 V | +0.0000 V | −1.0000 V | 0000000 | 0000000 | 0 | 1 |
| 001 | −1.9922 V | +0.0078 V | −0.9922 V | 0000001 | 0000001 | 0 | 1 |
| • | • | • | • | • | • | ↓ | ↓ |
| • | • | • | • | • | • | ↓ | ↓ |
| • | • | • | • | • | • | ↓ | ↓ |
| 063 | −1.0234 V | +0.9766 V | 0.0234 V | 0111111 | 0111111 | ↓ | ↓ |
| 064 | −1.0078 V | +0.9922 V | 0.0078 V | 1000000 | 1000000 | ↓ | ↓ |
| 065 | −0.9922 V | +1.0078 V | +0.0078 V | 1000001 | 1000001 | ↓ | ↓ |
| • | • | • | • | • | • | ↓ | ↓ |
| • | • | • | • | • | • | ↓ | ↓ |
| • | • | • | • | • | • | ↓ | ↓ |
| 126 | −0.0391 V | +1.9609 V | +0.9609 V | 1111110 | 1111110 | ↓ | ↓ |
| 127 | −0.0234 V | +1.9766 V | +0.9766 V | 1111111 | 1111111 | ↓ | ↓ |
| 128 | −0.0078 V | +1.9922 V | +0.9922 V | 1111111 | 0000000 | 1 | 0 |

*The MC10315L and MC10317L differ only in output coding at comparator step 128 where the device is overranged.

## CIRCUIT DESCRIPTION

**Conversion Timing**

The MC10315L/MC10317L performs a conversion and outputs data within a single clock cycle. Referring to Figure 1 will indicate that the clock input is sensitive to the rising and falling clock edges. All significant operations are referenced to the edges. A rising clock edge holds the analog input by latching the (128) input comparators. The output latches are also released to toggle and update to the new digital value. The falling edge of the clock will latch the data outputs. Clock timing must be considered to ensure a valid conversion. With the rising edge of the clock, there will be an aperture delay ($t_{ad}$) which is the time from the threshold of the (50%) edge to the actual time the input comparators latch in the analog value of $A_{in}$. The data valid delay time ($t_{vd}$) is the time interval for valid data to appear at the outputs. $t_{vd}$ is 43 ns from the rising clock edge. After this time, the clock can go low to latch the valid data at the outputs. The clock must remain low a minimum time before another rising edge in order for the input comparators to unlatch and begin to track. This comparator tracking delay time ($t_{cd}$) is 25 ns. After this minimum time, the conversion clock cycle is repeated, latching in a new analog input value.

The minimum recommended clock pulse width high time ($t_{pwH}$) is 44 ns and pulse width low time ($t_{pwL}$) is 25 ns for maximum recommended sample frequency (fs). Rise ($t_r$) and fall ($t_f$) time of the clock edges should be in the range from 2.0 to 7.0 ns to minimize the chance of clocking errors or uncertainty.

**Analog Input ($A_{in}$)**

The dc current drive required by the analog input ($A_{in}$) is a function of the input voltage ($V_{in}$) and is directly attributable to the accumulation of input bias currents for each of the 128 comparators. When $V_{in} \leqslant V_{RB}$, the dc current is zero and when $V_{in} \geqslant V_{RT}$ the current is a maximum of 400 μA. Looking at this current as a function of $V_{in}$ on a large signal basis, it will appear as a straight line approximation.

This input current loading on a driving source impedance can produce a dc gain error. Cancellation of this error is accomplished by utilizing an adjustable voltage reference at $V_{RT}$. If $V_{RT}$ is tied to a fixed reference or grounded, the driving amplifiers offset can be adjusted. However, a zero error will now occur which can be cancelled by adjusting $V_{RB}$. Another method of reducing dc gain error due to analog input current is to use a driving amplifier with sufficiently low output impedance ($Z_S$). This can be determined by:

$$Z_S \leqslant \frac{\text{maximum gain error (V)}}{400\ \mu\text{A}}$$

i.e., with a 1.0 volt analog input range ($V_{RT}$-$V_{RB}$ = 1.0 V), a 1/2 LSB of gain error = 3.9 mV

$$Z_S \leqslant \frac{3.9\text{ mV}}{400\ \mu\text{A}} \leqslant 9.76\,\Omega$$

**Analog Input ($A_{in}$)** (Continued)

The input capacitance ($C_{in}$) is also a function of input voltage ($V_{in}$). For $V_{in} \leqslant V_{RB}$, $C_{in} \simeq 40$ pF; $V_{in} \geqslant V_{RT}$, $C_{in} \simeq 70$ pF. The input capacitance on a large signal basis over the analog input range is a linear function. $C_{in}$ can limit the analog input bandwidth if the driving source impedance is too great. This can introduce an ac gain error if the corner frequency $f_c$ is not sufficiently extended from maximum input frequency ($f_{in}$).

For example, to keep the ac gain error to within 1/2 LSB of 7-bits, the corner frequency ($f_c$) of the effective single pole, low-pass filter created by the driving source impedance ($Z_S$) and the input capacitance ($C_{in}$) should be: $fc \geqslant 11.3\ f_{in}$

$C_{in}$ - analog input capacitance.
$f_{in}$ - maximum input frequency of $A_{in}$
$f_c$ - corner frequency determined by $C_{in}$ and $Z_S$
n - number of bits
$Z_S$ - driving source impedance of the analog input

For single Pole Filter: $$\frac{fc}{f_{in}} \geqslant \frac{1}{\sqrt{\dfrac{1}{\left(\dfrac{2^{n+1}-1}{2^{n+1}}\right)^2} - 1}}$$

If measures have already been taken to keep dc gain error to within 3.9 mV (1/2 LSB for 1.0 V full scale) by providing a low $Z_S$ as described earlier, the calculated $Z_S \leqslant 9.76\ \Omega$ will sufficiently extend the corner frequency of the input pole to $\simeq 233$ MHz.

Figure 2 illustrates the equivalent analog input in terms of an effective variable $C_{in}$ and $R_{in}$.

**Reference Inputs**

As shown in Figure 3, a resistive (divider) ladder comprised of 128 matched resistors with a nominal value of 0.5 Ω each, provides a reference voltage to each of the 128 comparator inputs. Recommended range of reference voltage applied across the resistive ladder ($V_{RT}$ to $V_{RB}$) is 1.0 volt to 2.0 volts. $V_{RT}$ must be kept more positive than $V_{RB}$. $V_{RT}$ must not exceed +2.5 volts above Gnd2 and $V_{RB}$ must not become more negative than −2.5 volts below Gnd2. With 2.0 volts across the reference ladder ($V_{RT}$-$V_{RB}$ = 2.0 V), the ladder network has a common-mode range capability about Gnd2, permitting analog input ($A_{in}$) ranging options such as ± 1.0 volt, 0 to − 2.0 volts and 0 to 2.0 volts. A minimum of 1.0 volt should be maintained across the ladder network to ensure linearity to 7-bits. Less than 1.0 volt will degrade linearity due to comparator offsets becoming a significant factor.

Additional taps on the reference ladder are pinned out, providing access to the middle ($V_{RM}$), 1/4 ($V_{RB}$ac) and 3/4 ($V_{RT}$ac) scale points. $V_{RM}$ can be left open, but if ladder linearity adjustment is required, an appropriate reference voltage can be applied. The $V_{RB}$ac and $V_{RT}$ac pins are intended for ac bypassing if ladder noise presents a problem. Reference voltages can be applied to these pins if tighter ladder linearity is desired. If the reference ladder voltage is to be varied dynamically such as in an AGC application, ac bypassing of any of the reference taps would likely yield undesirable results.

Calibration is accomplished by adjusting $V_{RB}$ and $V_{RT}$ to set the first and 127th comparator thresholds to the desired voltages. If a 0 to −1.0 V input ($A_{in}$) range is desired, continuously strobe the convertor with −0.9961 V on the analog input, adjust $V_{RB}$ for output toggling between codes 0000000 and 0000001. Then apply $A_{in} = -0.0117$ V and adjust $V_{RT}$ for toggling between 1111110 and 1111111 (thresholds 126th and 127th). Rather than adjusting $V_{RT}$, it may be more convenient to connect $V_{RT}$ to Gnd2 and adjust the driving amplifier offset control. $V_{RB}$ can again be used as a gain adjust point to cancel the effects of using the offset control technique.

**Application Information**

8-bits of resolution and accuracy can be obtained by stacking two 7-bit converters and wire ORing the data outputs. Shown in Figure 7 is an MC10315L and MC10317L in an 8-bit A/D configuration. The circuit is quite straightforward with the analog input ($A_{in}$) for each converter tied together, forming a common input. The analog input range is negative unipolar with $V_{RT}$ of the MC10315L grounded (Gnd2) or referenced very near ground. $V_{RB}$ of the MC10315L is connected to $V_{RT}$ of the MC10317L and referenced to $V_{REF}/2$ to ensure this node is midscale. Unit to unit variations in Reference Ladder Resistance of each device can shift this point if a reference is not used, causing linearity errors. Care should be taken when interconnecting $V_{RB}$ and $V_{RT}$ of the MC10315L and MC10317L respectively. Reference ladder current flowing through resistance of printed circuit board runs, sockets and even device pins and bonding wires can establish significant IR drops of several millivolts causing differential non-linearity errors at midscale. A negative reference of −2.000 V is applied to $V_{RB}$ of the MC10317L. The remaining pins $V_{RT}$ac, $V_{RB}$ac and $V_{RM}$ for both devices can be left open or be connected to additional external references if linearity improvements are required. $V_{RT}$ac and $V_{RB}$ac can also be used as ac decoupling points for the resistor ladders to reduce any transients which may exist due to current noise.

The clock (CLK) inputs are driven by a common clock. Depending on the input frequency to be encoded, it may be necessary to skew the rising clock edges to one of the devices to compensate for a slight difference in aperture delay time ($t_{ad}$) which may occur between the two devices.

### Application Information (Continued)

The digital outputs, D0 through D6 are wire ORed. The overrange (OVR) bit of the MC10317L becomes the MSB for the 8-bit word in Binary coding.

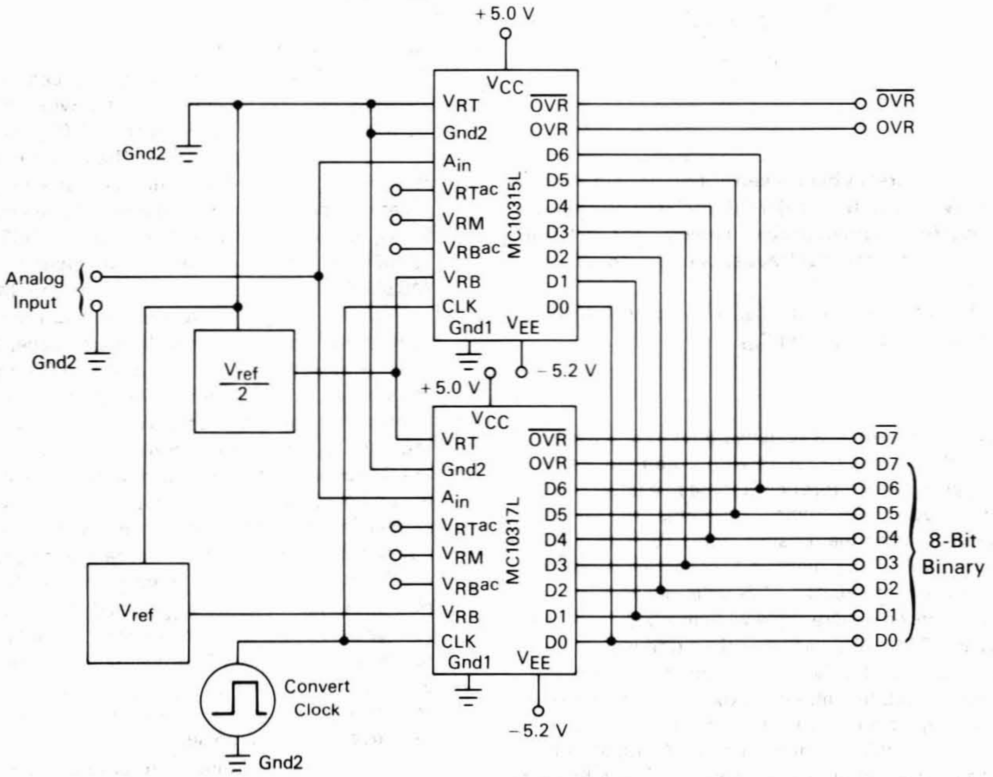
The MC10315L and MC10317L differ only in the method of overranging (see Figure 6, output coding truth table). When the MC10317L input ($A_{in}$) is overranged, the overrange (OVR) bit goes high, all other bits (D0-D6) go low. This enables direct wire ORing of additional A/D outputs to expand to ≥8-bits. When the MC10315L is overranged, OVR goes high and the data bits (D0-D6) remain high. This device provides a true termination of a digital word when the system becomes overranged. Generally the MC10315L will be used in a 7-bit, stand-alone converter scheme, or as the upper scale A/D when stacking two or more devices to expand to ≥7-bits.

Pull-down resistors are required at the digital outputs. A recommended value of 510 Ω will provide proper output fall times in most applications and also hold down device power dissipation. The outputs are capable of sustaining MECL levels when terminated with a 50 Ω (to −2.0 V) characteristic load impedance to minimize reflections. Design rules for MECL 10K should be followed when using these devices.

Care must be taken in PC board ground layout to prevent digital ground currents from flowing through the analog ground. Separate grounds are provided on the MC10315L/MC10317L to help isolate the digital noise from the analog section of a system. Gnd1 is internally connected to only the collectors of the output emitter followers as shown in Figure 5. This provides a separate path for current transients of the switched output loads. All other internal circuitry is referenced to Gnd2.

Low and high frequency power supply bypassing should be provided physically close to the device, with $V_{CC}$ and $V_{EE}$ bypassed to Gnd2.

**FIGURE 7 — CIRCUIT CONFIGURATION UTILIZING A MC10315L AND MC10317L A/D TO PERFORM A HIGH SPEED, 8-BIT CONVERSION**



Note:
Required pull-down resistors at the digital outputs are not shown. All digital outputs should be treated according to MECL 10K design rules.

**See Application Note AN844 and AN848, and AN877 for further information.**

**MOTOROLA**

# MC10318L9
# MC10318L
# MC10318CL7
# MC10318CL6

## Specifications and Applications Information

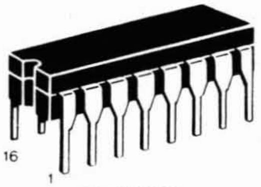
### HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

The MC10318 (Series) is a high-speed D/A converter capable of data conversion rates in excess of 25 MHz. The digital inputs are compatible with MECL 10,000 Series Logic. Complementary current outputs provide up to 56 mA full scale capability. The MC10318 Series is available in 4 accuracy grades (over temperature) to meet the requirements of many applications, including: high-speed instrumentation and test equipment, storage oscilliscopes, display processing, radar systems, and digital video systems (broadcast and receiver applications).

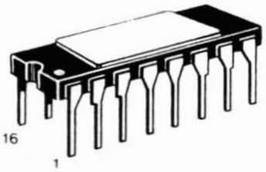
- FAST Settling Time — 10 ns (Typ to ±0.19%)
- Four Accuracy Grades
  - — 9-Bit Linearity (±0.10%) — MC10318L9
  - — 8-Bit Linearity (±0.19%) — MC10318L
  - — 7-Bit Linearity (±0.39%) — MC10318CL7
  - — 6-Bit Linearity (±0.78%) — MC10318CL6
- Inputs MECL 10,000 Compatible
- Complementary Current Outputs
- Output Compliance: −1.3 V to +2.5 V
- Single MECL Supply: −5.2 V
- Standard 16-Pin Dual-In-Line Package
- Evaluation Kit MCK8DA Available

### HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

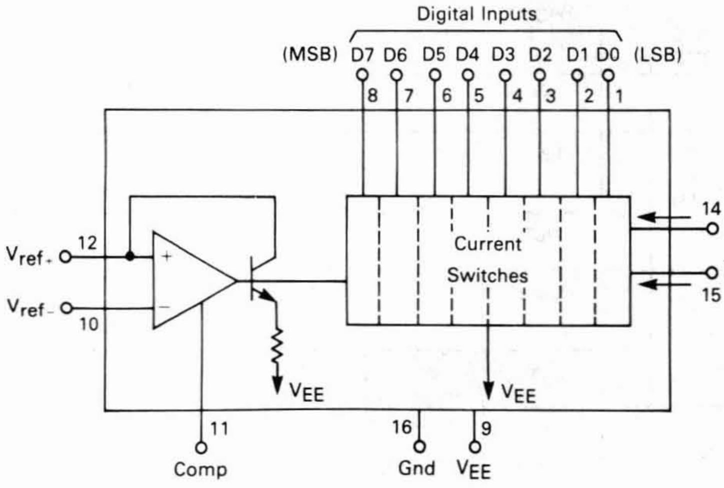


**CL SUFFIX**
CERAMIC PACKAGE
CASE 620-02

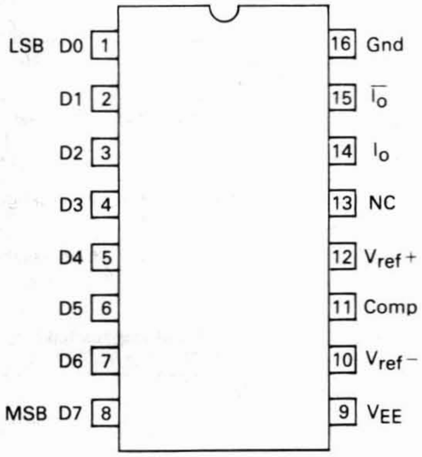


**L SUFFIX**
CERAMIC PACKAGE
CASE 690-13

### BLOCK DIAGRAM


Digital Inputs
(MSB) D7 D6 D5 D4 D3 D2 D1 D0 (LSB)
8 7 6 5 4 3 2 1
$V_{ref+}$ 12
+
−
$V_{ref-}$ 10
Current Switches
14 $I_o$
$\overline{I_o}$ 15
$V_{EE}$
$V_{EE}$
11
Comp
16
Gnd
9
$V_{EE}$

### PIN CONNECTIONS (TOP VIEW)


LSB D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
MSB D7 8
16 Gnd
15 $\overline{I_o}$
14 $I_o$
13 NC
12 $V_{ref+}$
11 Comp
10 $V_{ref-}$
9 $V_{EE}$

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{EE}$ | −6.0 to +0.5 | Vdc |
| Digital Input Voltage | $V_I$ | 0 to $V_{EE}$ | Vdc |
| Applied Output Voltage | $V_O$ | +5.0 to $V_{EE}$ | Vdc |
| Reference Current | $I_{ref}(12)$ | 5.0 | mA |
| Output Current | $I_{FS}$ | −75 | mA |
| Reference Amplifier Input Range | $V_{ref}$ | +0.5 to $V_{EE}$ | Vdc |
| Reference Amplifier Differential Inputs | $V_{ref}(D)$ | ±5.0 | Vdc |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature Ceramic Package | $T_J$ | +175 | °C |
| Thermal Resistance, Still Air<br>Junction to Ambient With 500 LFPM | $R_{\theta JA}$ | 80<br>50 | °C/W |

**DC CHARACTERISTICS** ($V_{EE}$ = −5.2 V, ±5% $T_A$ = 0°C to +70°C after thermal equilibrium is reached.)

| Characteristics | Fig. | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Nonlinearity (Integral) (Pin 14 or 15) (@ $I_{FS}$ = 51 mA, 25.5 mA)<br>MC10318L9<br>MC10318L<br>MC10318CL7<br>MC10318CL6 | | —<br>—<br>—<br>— | —<br>—<br>—<br>— | —<br>—<br>—<br>— | ±0.10<br>±0.19<br>±0.39<br>±0.78 | % FS |
| Zero Scale Output Current (Pin 14 or 15) ($T_A$ = 25°C) | 10 | $I_{ZS}$ | — | 5.0 | 50 | µA |
| Zero Scale Output Current Temperature Drift (Pin 14 or 15)<br>0 < $T_A$ < 25°C<br>25°C < $T_A$ < 70°C | | $I_{ZS/\Delta T}$ | —<br>— | ±17<br>±2.0 | —<br>— | nA/°C |
| Full Scale Output Current (Pin 14 or 15) ($I_{ref}$ = 3.2 mA, D0–D7 = 1) | 10 | $I_{FS}$ | −46.00 | −51.00 | −56.00 | mA |
| Full Scale Output Current Temperature Drift (Pin 14 or 15)<br>0 < $T_A$ < 25°C<br>25°C < $T_A$ < 70°C | | $\Delta I_{FS/°C}$ | —<br>— | ±50<br>±10 | —<br>— | ppm/°C |
| Full Scale Output Sensitivity to Power Supply Variations (Pin 14 or 15) (−4.94 V < $V_{EE}$ < −5.46 V)<br>MC10318L,9<br>MC10318CL6,7 | | $I_{FSPSS}$ | —<br>— | ±0.005<br>±0.005 | ±0.02<br>±0.04 | %/% |
| Full Scale Symmetry ($I_{FS}$ — $\overline{I_{FS}}$) | 10 | $I_{FSS}$ | — | ±21 | ±100 | µA |
| Output Voltage Compliance (Pin 14 or 15) Full Scale Current Change ≤ ½ LSB (Specified Nonlinearity) ($T_A$ = 25°C) | | $V_{OC}$ | −1.3 | — | +2.5 | V |
| Output Resistance (Pin 14 or 15) ($T_A$ = 25°C) | 12 | $R_O$ | — | 69 | — | kΩ |
| Reference Amplifier Offset Voltage ($T_A$ = 25°C) | | $V_{IO}$ | — | ±3.2 | — | mV |
| Reference Amplifier Offset Voltage Temperature Drift<br>0 < $T_A$ < 25°C<br>25°C < $T_A$ < 70°C | | $\Delta V_{IO/\Delta T}$ | —<br>— | ±10<br>±4.0 | —<br>— | µV/°C |
| Reference Amplifier Bias Current (Pin 10) ($I_{ref}$ = 3.2 mA) | | $I_{IB}$ | — | 4.0 | 15 | µA |
| Reference Amplifier Bias Current Temperature Drift ($I_{ref}$ = 3.2 mA)<br>0 < $T_A$ < 25°C<br>25°C < $T_A$ < 70°C | | $\Delta I_{IB/\Delta T}$ | —<br>— | −40<br>−10 | —<br>— | nA/°C |
| Reference Amplifier Common Mode Range ($V_{EE}$ = −5.2 V) ($T_A$ = 25°C) | | $V_{ICR}$ | — | ±1.15 | — | V |
| Reference Amplifier Common Mode Rejection Ratio ($T_A$ = 25°C) ($I_{ref}$ = 3.2 mA, $V_{ICR}$ = 0 to −2.0 V, Pins 1–8 = Logic 1) | | $V_{ICMRR}$ | — | 58 | — | dB |
| Reference Amplifier Input Impedance (Pin 10) ($T_A$ = 25°C) | | $R_{IN}$ | — | 1.0 | — | MΩ |
| Power Supply Current (Pins 1 thru 8 Open, $I_{ref}$ = 3.2 mA, Includes $I_o$ + $\overline{I_o}$) | | $I_{EE}$ | — | 90 | 130 | mA |

**AC CHARACTERISTICS** ($T_A$ = 25°C, $V_{EE}$ = −5.2 V, ±5%)

| Characteristics | Fig. | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Feedthrough Current — All Bits Off | 9 | $I_{FC}$ | | | | μA p-p |
| f = 10 kHz | | | — | 2.0 | — | |
| f = 100 kHz | | | — | 18 | — | |
| Distortion — (@ $I_O$)<br>(Sinewave applied to reference amplifier Input, D0–D7 = Logic 1) | | | | | | % |
| C = 0.01 μF, f = 20 kHz | | THD | — | 1.0 | — | |
| C = 0.01 μF, f = 65 kHz | | THD | — | 5.0 | — | |
| C = 0.001 μF, f = 340 kHz | | THD | — | 1.0 | — | |
| C = 0.001 μF, f = 600 kHz | | THD | — | 2.0 | — | |
| C = 240 pF, f = 600 kHz | | THD | — | 0.8 | — | |
| Reference Amplifier Slew Rate<br>(Step change at Pin 10, all bits on) | 13 | | | | | mA/μs |
| C = 0.01 μF | | | — | 0.5 | — | |
| C = 0.001 μF | | | — | 5.0 | — | |
| C = 240 pF | | | — | 20 | — | |
| Settling Time (to ±0.19% of Full Scale) | 1,22 | $t_s$ | | | | ns |
| 1 LSB Change | | | — | 7.0 | — | |
| All Bits Switched | | | — | 10 | — | |
| Propagation Delay | 2 | $t_p$ | — | 5.0 | — | ns |
| Output Glitch Energy (with De-Skewing Capacitors)<br>(Input Change: 01111111 ⟷ 10000000) | | | — | 50 | — | LSB·ns |
| Glitch Duration | | | — | 5.0 | — | ns |

**DIGITAL INPUT VOLTAGE LEVELS**

**Volts (See Note)**

| $T_A$ | $V_{IH}$max | $V_{IHA}$min | $V_{ILA}$max | $V_{IL}$min |
|---|---|---|---|---|
| 0°C | −0.845 | −1.151 | −1.516 | −1.868 |
| 25°C | −0.810 | −1.105 | −1.505 | −1.850 |
| 70°C | −0.727 | −1.052 | −1.480 | −1.830 |

## FUNCTIONAL PIN DESCRIPTION

**D0–D7 (Pins 1-8)** The eight ECL digital inputs compatible with MECL 10,000 series devices. Logic "0" is nominally −1.8 V, and Logic "1" is nominally −0.9 V.

**$V_{ref-}$ (Pin 10)** The high impendance input of the reference amplifier. This input is normally grounded, but may be used for ac applications involving modulation, digitally controlled gain, etc. Normal operating range is from ground to $V_{EE}$ + 2.9 V (nominally −2.3 V).

**$V_{ref+}$ (Pin 12)** The noninverting input of the reference amplifier. The inverted output of the reference amplifier is internally fed back to this input, thus causing it to track Pin 10. A nominal 3.2 mA is to be supplied to this pin from an external (stable and noise free) voltage source and current setting resistor.

**Comp. (Pin 11)** A nominal 0.01 μF capacitor is connected to this pin and to ground to stabilize the reference amplifier. Lower values of capacitor may be used if a good PC board layout is used, where frequencies higher than 10 kHz are applied to the reference amplifier.

**$I_O$, $\overline{I_O}$ (Pins 14,15)** The complementary current outputs. Current flow is into the DAC and varies linearily with $I_{ref}$ and the digital input code. $I_{out}$ increases as the digital input increases. Output compliance range is −1.3 V to +2.5 V.

**$V_{EE}$ (Pin 9)** The power supply pin. $V_{EE}$ is nominal −5.2 V, ±5%.

**Gnd (Pin 16)** The ground pin. This line should be as noise-free as possible in order to obtain a noise-free output.

NOTE: $V_{EE}$ = −5.2 V, ±5% Inputs are MECL 10,000 compatible within the temperature and power supply ranges listed. See MECL System Design Handbook for further details. See Fig. 19 in this data sheet.

FIGURE 1 — SETTLING TIME

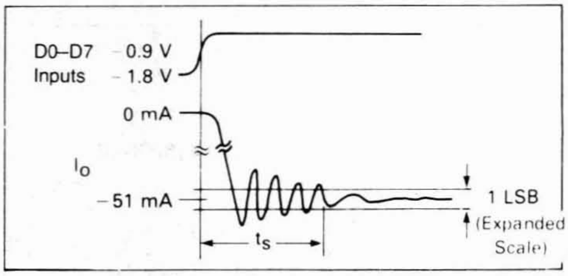
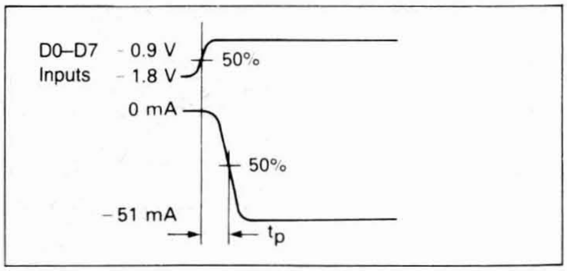


FIGURE 2 — PROPAGATION DELAY



## REFERENCE AMPLIFIER RESPONSE

**Inverting Input ($V_{ref-}$)**
**Test Circuit of Fig. 14**

FIGURE 3 — FREQUENCY RESPONSE

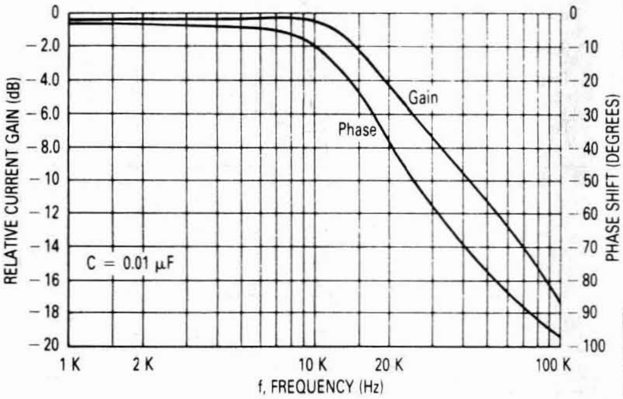


FIGURE 4 — FREQUENCY RESPONSE

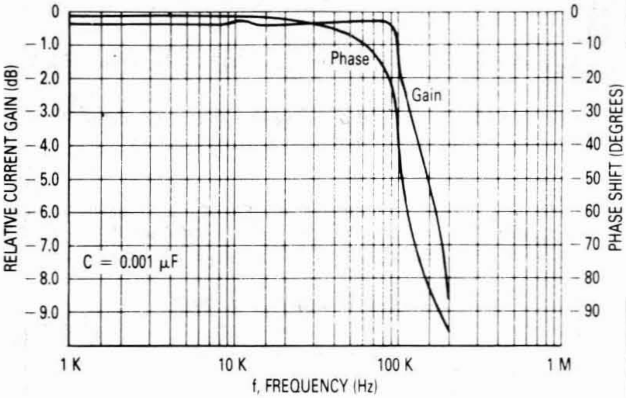
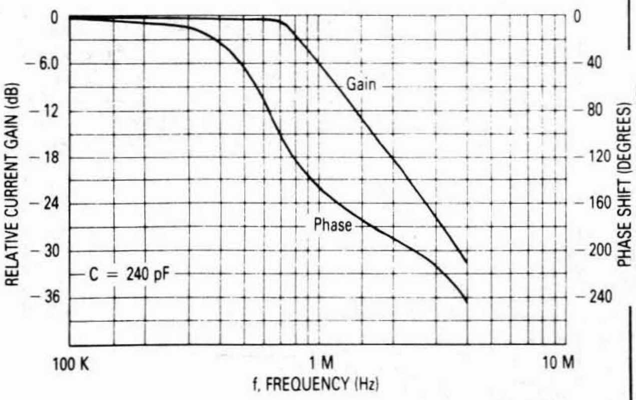


FIGURE 5 — FREQUENCY RESPONSE



**Noninverting Input ($V_{ref+}$)**
**Test Circuit of Fig. 11**

FIGURE 6 — FREQUENCY RESPONSE

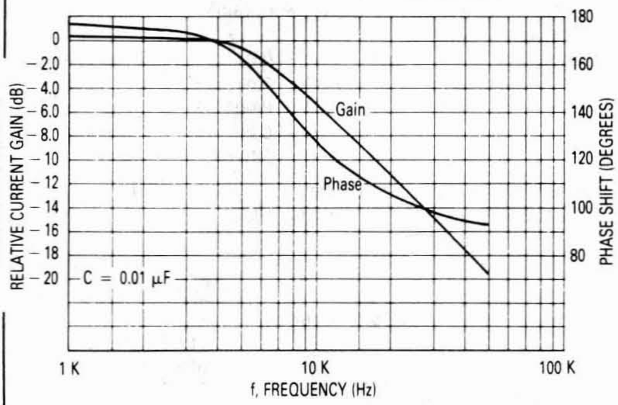


FIGURE 7 — FREQUENCY RESPONSE

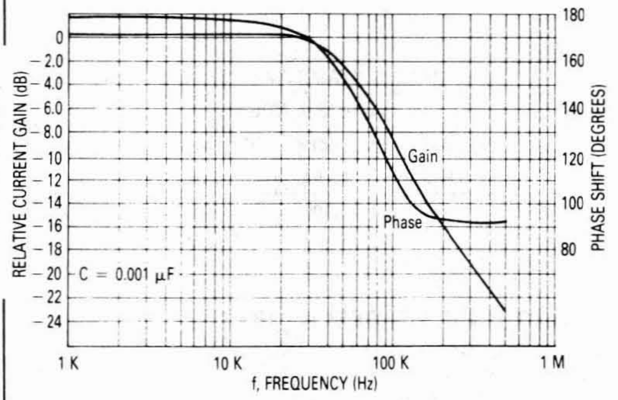
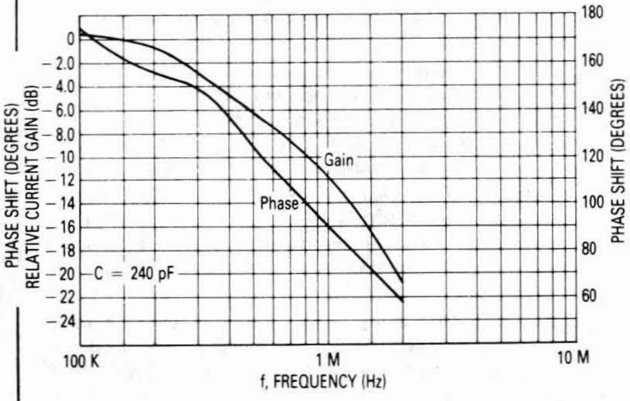
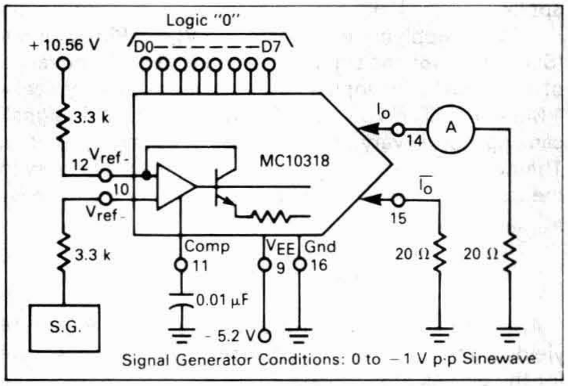


FIGURE 8 — FREQUENCY RESPONSE



## TEST CIRCUITS

FIGURE 9 — FEEDTHROUGH MEASUREMENT


Logic "0"
+10.56 V
D0 — — — — — — D7
3.3 k
12 Vref+
10
Vref-
3.3 k
S.G.
MC10318
Io
14
A
Īo
15
Comp
11
VEE
9
Gnd
16
0.01 µF
-5.2 V
20 Ω
20 Ω

Signal Generator Conditions: 0 to −1 V p-p Sinewave

FIGURE 10 — ZERO/FULL SCALE CURRENT

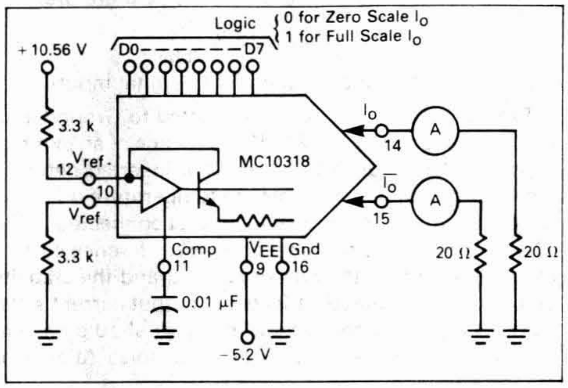
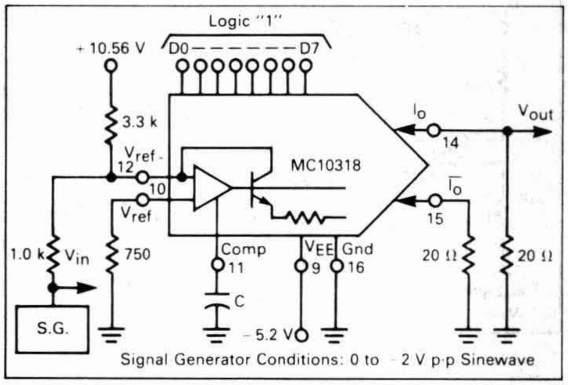

Logic { 0 for Zero Scale Io
1 for Full Scale Io
+10.56 V
D0 — — — — — — D7
3.3 k
12 Vref+
10
Vref-
3.3 k
MC10318
Io
14
A
Īo
15
A
Comp
11
VEE
9
Gnd
16
0.01 µF
-5.2 V
20 Ω
20 Ω

FIGURE 11 — GAIN/PHASE MEASUREMENT


Logic "1"
+10.56 V
D0 — — — — — — D7
3.3 k
Vref+
12
10
Vref-
1.0 k
Vin
750
S.G.
MC10318
Io
14
Vout
Īo
15
Comp
11
C
VEE
9
Gnd
16
-5.2 V
20 Ω
20 Ω

Signal Generator Conditions: 0 to −2 V p-p Sinewave

Reference dB Level: See Text

See Figures 6–8

FIGURE 12 — OUTPUT RESISTANCE

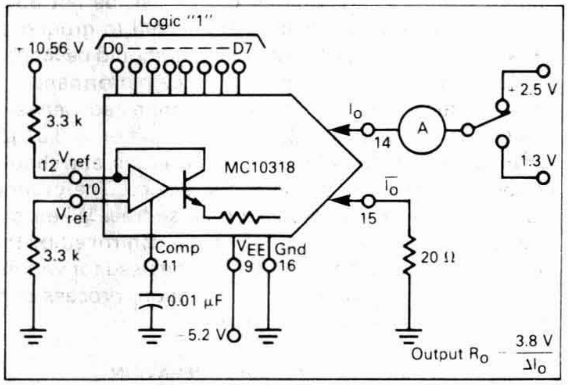
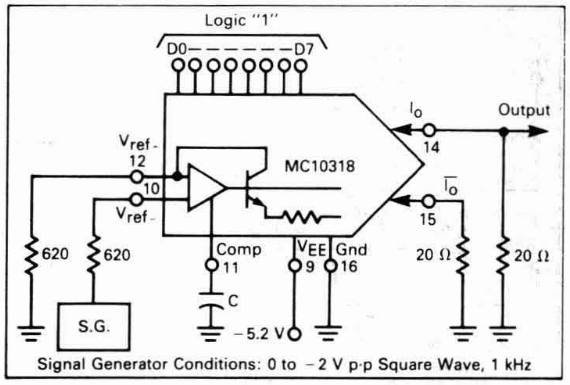
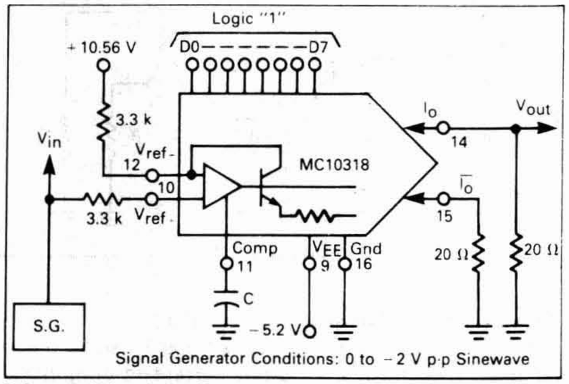

Logic "1"
+10.56 V
D0 — — — — — — D7
3.3 k
12 Vref+
10
Vref-
3.3 k
MC10318
Io
14
A
+2.5 V
1.3 V
Īo
15
Comp
11
0.01 µF
VEE
9
Gnd
16
-5.2 V
20 Ω
Output Ro = 3.8 V / ΔIo

FIGURE 13 — REFERENCE AMPLIFIER SLEW RATE


Logic "1"
D0 — — — — — — D7
Vref+
12
10
Vref-
620
620
S.G.
MC10318
Io
14
Output
Īo
15
Comp
11
C
VEE
9
Gnd
16
-5.2 V
20 Ω
20 Ω

Signal Generator Conditions: 0 to −2 V p-p Square Wave, 1 kHz

FIGURE 14 — GAIN/PHASE MEASUREMENT


Logic "1"
+10.56 V
D0 — — — — — — D7
3.3 k
Vin
Vref+
12
10
3.3 k
Vref-
S.G.
MC10318
Io
14
Vout
Īo
15
Comp
11
C
VEE
9
Gnd
16
-5.2 V
20 Ω
20 Ω

Signal Generator Conditions: 0 to −2 V p-p Sinewave

Reference dB Level: See Text.

See Figures 3–5

## OPERATIONAL INFORMATION

### Typical DAC Operation

The MC10318 is designed to be operated with an $I_{ref}$ (Pin 12) of 3.2 mA, resulting in a full scale output current ($I_O$) of 51 mA when D0 through D7 are at a Logical "1" (−0.9 V). The transfer equation for $I_O$ is therefore:

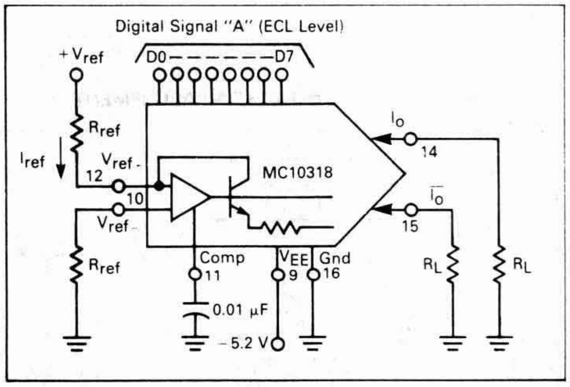
$$I_O = I_{ref} \times 16 \times \frac{A}{256}$$

("A" is the binary value of the digital input).

Typically $V_{ref-}$ (Pin 10) is connected to Ground, and $I_{ref}$ is supplied to $V_{ref+}$ (Pin 12) by means of an external supply $V_r$ (see Figure 15). A resistor inserted between Pin 10 and Ground will minimize temperature drift, and should have a value equivalent to that connected to Pin 12. Any noise or ripple present on the reference current will be present on the output current, and the stability of the reference directly affects the output current's stability. The ground connection for $V_{ref-}$ should be chosen with care so as not to pick up noise (digital or otherwise).

The complementary outputs ($I_O$ and $\overline{I_O}$) are high impedance current sources having a compliance range of 3.8 V (−1.3 to +2.5 V). $I_O$ increases with increasing digital input, while $\overline{I_O}$ decreases. Their sum is a constant equal to 15.94 x $I_{ref}$. Neither output can be left open — an unused output must be connected to ground or a load resistor. Typically both outputs should be loaded similarly for best speed and accuracy performance. A compensation capacitor must be connected between Pin 11 and Ground to stabilize the amplifier. A 0.01 µF ceramic is satisfactory for most applications, and should be located physically close to the device. The ground side of the capacitor should be noise-free. When operated as above, the output(s) will be controlled by the digital inputs, and the MC10318 can be used for various functions such as waveform generation, process control, ADC conversion, and others.

FIGURE 15 — TYPICAL OPERATION


Digital Signal "A" (ECL Level)
+Vref
D0 — — — — — — D7
Rref
Iref
Vref+
12
10
Vref-
MC10318
Io
14
Ī̄o
15
Comp
11
VEE
9
Gnd
16
0.01 µF
−5.2 V
Rref
RL
RL

### Common Mode Range — AC Operation

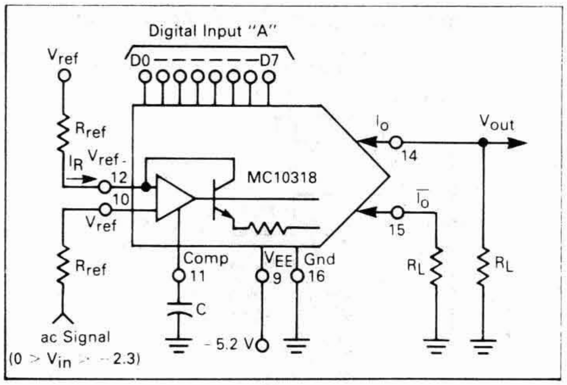
The reference amplifier inputs (Pins 10 and 12) may be used to control the output current in conjunction with the digital inputs for applications such as digitally controlled gain of an ac signal, digitally controlled amplitude modulation, and others. Either the positive or negative input of the reference amplifier may be used, depending on the application. There are, however, differences in the manner in which an ac signal is to be applied.

1) When applying a signal to the $V_{ref-}$ (Pin 10) input (See Figure 16), the signal must be kept within the range of 0 to −2.3 V. The input has a high impedance (typically 1 Megohm). The $V_{ref+}$ pin (Pin 12) will track this signal, causing $I_{ref}$ to vary, in turn causing $I_O$ and $\overline{I_O}$ to vary. The ac component of $I_O$ (and $\overline{I_O}$) will be in phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A \times R_L}{16 \times R_R}$$

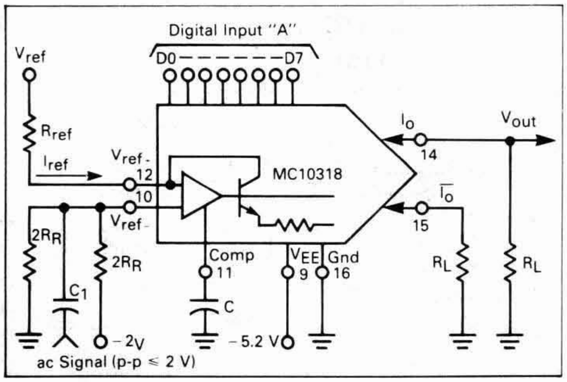
Applying the above to the test circuit of Figure 14 yields a gain of 0.0966, which is the 0 dB reference level for the curves of Figures 3–5.

FIGURE 16 — AC OPERATION, NONINVERTING


Digital Input "A"
Vref
D0 — — — — — — D7
Rref
IR
Vref+
12
10
Vref-
MC10318
Io
Vout
14
Īo
15
Comp
11
VEE
9
Gnd
16
C
−5.2 V
Rref
ac Signal
(0 > Vin > −2.3)
RL
RL

If the peak values of the applied ac signal cannot be kept within the above mentioned voltage range, an alternate circuit is shown in Figure 17.

FIGURE 17 — AC OPERATION, NONINVERTING (ALTERNATE)


Digital Input "A"
Vref
D0 — — — — — — D7
Rref
Iref
Vref+
12
10
Vref-
MC10318
Io
Vout
14
Īo
15
2RR
2RR
C1
−2V
ac Signal (p-p ≤ 2 V)
Comp
11
C
VEE
9
Gnd
16
−5.2 V
RL
RL

The compensation capacitor (Pin 11) of Figures 16 and 17 is to be nominally 0.01 µF for best overall stability. If frequencies higher than 10 kHz are to be applied to the reference input, a smaller value capacitor will be necessary as indicated by Figures 3–5. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

2) When applying a signal to the $V_{ref+}$ (Pin 12) input (see Figure 18), the effect is a direct modulation of the reference current supplied by $V_{ref}$. Pin 12 is a virtual ground, and therefore the current $I_{ref}$ is equal to:

$$I_{ref} = \frac{V_{ref}}{R_{ref}} + \frac{V_i}{R_i}$$

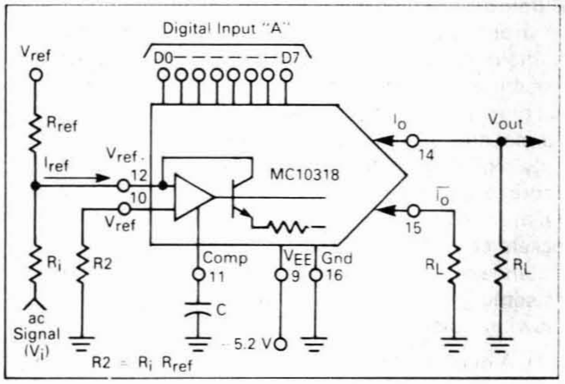
$I_O$ and $\overline{I_O}$ will vary with the reference current, but the ac component will be 180° out of phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{out}}{\Delta V_i} = \frac{-A \times R_L}{16 \times R_i}$$

Applying the above to the test circuit of Figure 11 yields a gain of −0.3188, which is the 0 dB reference level for the curves of Figures 6–8.

The reference current $I_{ref}$ must always flow **into** Pin 12, requiring that the values of $V_{ref}$, $R_{ref}$, $R_i$, and $V_i$ be chosen so as to guarantee this.

FIGURE 18 — AC OPERATION, INVERTING

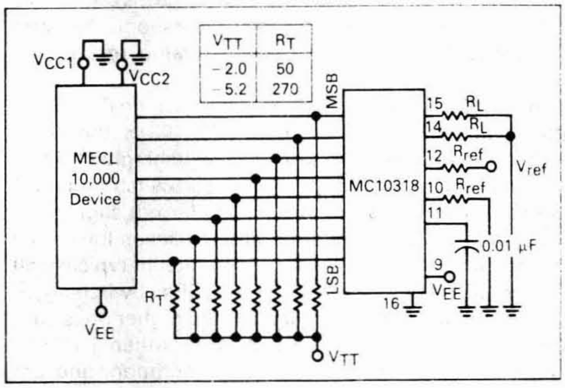

Digital Input "A"
D0 — — — — — — D7
Vref
Rref
Iref
Vref+
12
10
Vref
MC10318
Io
14
Vout
Io
15
Ri
R2
Comp
11
C
VEE
9
Gnd
16
−5.2 V
RL
RL
ac Signal (Vi)
R2 = Ri ∥ Rref

The compensation capacitor (Pin 11) of Figure 18 is to be nominally 0.01 µF for best overall stability. If frequencies higher than 4 kHz are to be applied, a smaller value capacitor will be necessary as indicated by Figures 6–8. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

## DIGITAL INTERFACE

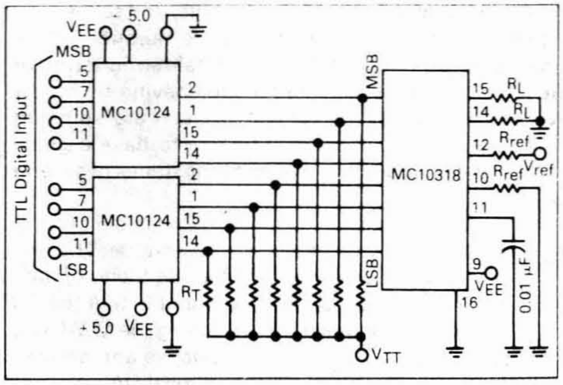
The digital inputs (Pins 1–8) are compatible with MECL 10,000 series devices over the temperature and $V_{EE}$ range listed on page 3. Standard MECL 10,000 design guidelines apply, and should be implemented. Maximum speed response requires careful PC board layout and choice of components. See Motorola's MECL System Design Handbook for a complete explanation of specifications and characteristics. Figure 19 shows a typical ECL interconnection with recommended values for optimum speed performance. Other values of $R_T$ and $V_{TT}$ may be used, but at a slight increase in overall propagation delay. Unused inputs should not be left open, but should be connected to a Logic 0 (−1.8 V), or a Logic 1 (−0.9 V). Resistors $R_T$ should be connected at the receiving end of the interconnection, i.e. physically located adjacent to the MC10318 inputs, for best speed performance.

FIGURE 19 — STANDARD MECL INTERFACE


VCC1
VCC2
VTT
RT
−2.0
50
−5.2
270
MSB
MECL 10,000 Device
MC10318
15
RL
14
RL
12
Rref
Vref
10
Rref
11
0.01 µF
9
VEE
16
LSB
RT
VEE
VTT

Interfacing a TTL system to the MC10318 is easily accomplished by the use of two MC10124 devices (Figure 20).

FIGURE 20 — TTL INTERFACE


VEE
−5.0
MSB
5
7
10
11
MC10124
2
1
15
14
5
7
10
11
MC10124
2
1
15
14
LSB
TTL Digital Input
+5.0
VEE
RT
MSB
LSB
MC10318
15
RL
14
RL
12
Rref
10
Rref
Vref
11
9
VEE
16
0.01 µF
VTT

## OUTPUT CHARACTERISTICS

The MC10318 DAC has been designed specifically for high-speed operation by incorporating ECL structured inputs, bit switching circuits which are small in size and simple in operation, and high-current complementary outputs (which permits current steering rather than on-off switching). In this manner, very short propagation delays and settling times are possible.

### Output Glitch

All DAC's will produce a glitch at the output when various bits are switched in opposite directions, due to differences in transition times of the switching transistors. During the switching period, typically the output current will momentarily seek a value other than the desired final value, and then return to and settle at the final value. This glitch can be several LSBs in magnitude, but of a very short duration (5–6 ns). In some instances, the output current may overshoot, and then undershoot before reaching the final value, resulting in a "glitch doublet."

The glitch is most apparent when switching the higher order bits, and in the case of the MC10318, the maximum glitch generally occurs when switching bit D5 and the lower 5 bits (typically 85 LSB·ns). Switching bit D6 and the lower 6 bits produces a similar but slightly reduced glitch. Switching bit D7 and the seven lower bits (major carry transition) results in a glitch of typically 50 LSB·ns, with an amplitude of 17 LSBs. Switching of lower order bits while maintaining the higher ones constant produces glitches typically of less than 1 LSB in magnitude, and less than 10 ns in duration, and are generally not considered to be of significance.

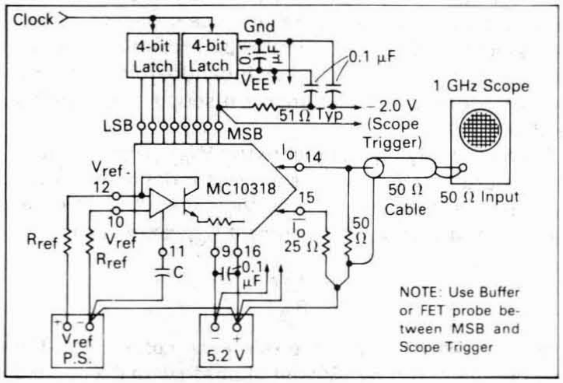
Glitches can be removed from the output by filtering, or by using a sample-and-hold circuit on the output, or by using de-skewing capacitors on the higher order bits. See Fig. 31.

Output glitch is generally specified in terms of glitch energy, which is the area under the curve of the waveform. Most glitches appear as a triangle, and so the area is simply ½ × t × ΔI, where t is the duration of the glitch, and ΔI is the amplitude normalized in terms of LSBs. In the case of a glitch doublet, having both positive and negative amplitude, the areas are summed algebraically. It is possible, therefore to have a glitch with zero energy, although having amplitudes of several LSB's.

In applications where the output glitch is of concern, steps can be taken to minimize its magnitude. The two main factors to consider are: 1) That the 8 bits of data reach the MC10318 simultaneously; and 2) that the PC board layout prevent noise from reaching the MC10318.

It is obvious that if the updated 8 bits are not received by the DAC simultaneously, even an ideal DAC will not produce an ideal waveform. Where simultaneous transmission by the sending device(s) cannot be guaranteed (such as two cascaded counters), latches should be used ahead of the MC10318. The latches should then be clocked after their inputs have settled. Suggested latches are the MC10133/MC10153/MC10168 at the ECL level, and the SN74LS273 at the TTL level.

**FIGURE 21 — PRECISION HIGH-SPEED MEASUREMENTS**



### Nonlinearity

Integral nonlinearity has been specified, rather than differential nonlinearity, as this is a better indicator of the maximum error to be expected. Integral nonlinearity is measured by comparing the **actual** output (at each digital value) with the expected ideal value. The expected values lie along a straight line between zero and the full scale output current. The MC10318 series will not differ from the **ideal** value by more than the specified nonlinearity.

### PC Board Layout

A proper PC board layout is very important in order to obtain the full benefits of the MC10318's high-speed characteristics. Each of the current paths ($I_O$, $\overline{I_O}$, $I_{EE}$, $I_{ref}$, etc.) must be carefully considered to avoid interference, and isolation from other circuits on the board (particularly digital) is essential. By-passing of all supplies is, of course, necessary, and in some cases, by-passing to $V_{EE}$ may be more beneficial than by-passing to Ground. Sockets should be avoided as the extra pin-to-pin capacitance can slow down the ECL edges and/or the output settling time. PC board layout should include the following guidelines:

1) A dedicated ground track from the power supply to Pin 16 (Gnd);
2) A single dedicated ground track from the power supply to the **two** load resistors associated with $I_O$ and $\overline{I_O}$ — this results in a constant dc current in this track;
3) A separate ground for the circuitry associated with $V_{ref+}$, $V_{ref-}$, and Comp (Pins 10–12). Any noise on this ground will feed through the reference amplifier and show up on the output;
4) The compensation capacitor must be physically adjacent to Pin 11;
5) Bypass $V_{EE}$ (Pin 9) with a 0.1 µF to the ground line feeding the load resistors;
6) Provide proper terminations at the inputs — the suggested values for $R_T$ and $V_{TT}$ will provide best speed response;

7) Bypass $V_{TT}$ to $V_{EE}$ **and** to Ground with 0.1 µF capacitors;
8) If the power supplies are not on the same PC board with the MC10318, bypass $V_{EE}$ and $V_{TT}$ to Ground with (minimum) 10 µF and 0.1 µF where the supply voltages enter the PC board;
9) Use of a ground plane is mandatory in all high speed applications;
10) Keep all TTL circuitry tracks separate from the MC10318 by means of ground tracks and/or ground planes.

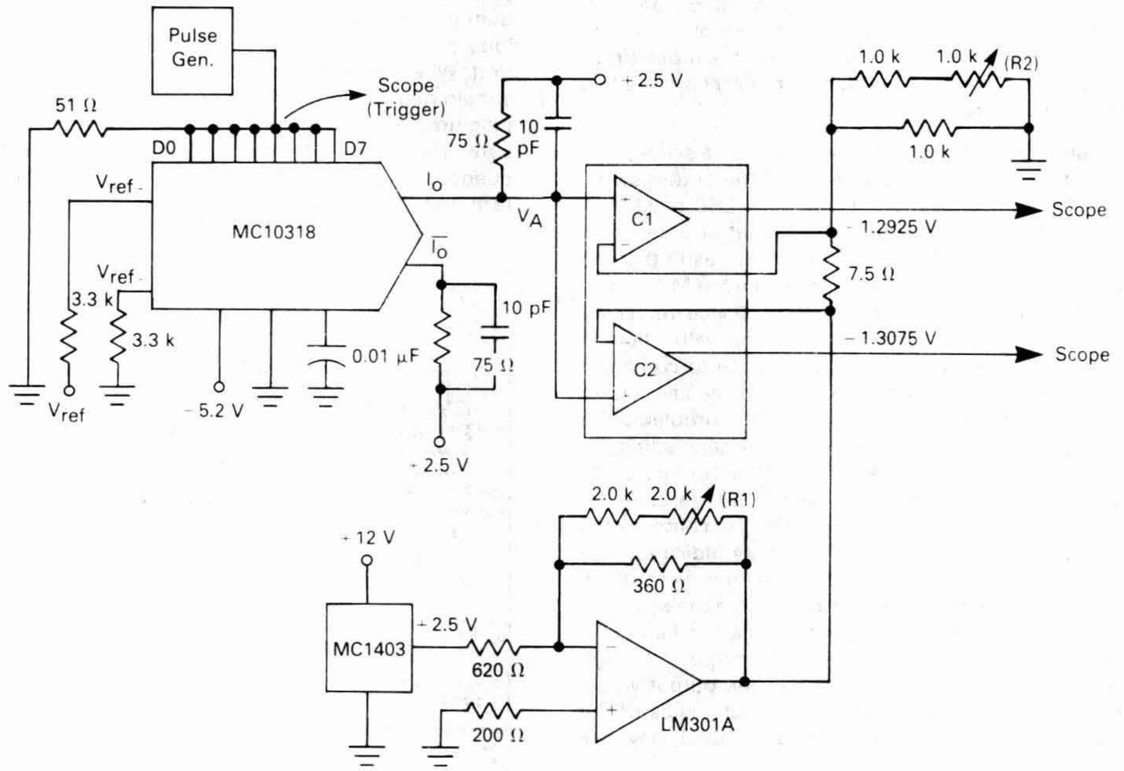
Many of the above points have to do with isolating the device from all other circuitry, since most applications involve using the MC10318 (which is 50% analog) in a (noisy) digital circuit. If the output voltage swing is typically 1 volt, then 1 LSB is approximately 4 mV. Since TTL circuitry can easily generate 50 mV noise on the ground line, the need for isolation is apparent.

The above points are not the only ones to be considered by the designer, as each application will have its own individual additional requirements.

**Propagation Delay**

The propagation delay is measured from the 50% point of the input transition to the 50% point of the output transition. Since the typical propagation delay is on the order of 5 ns, see Figure 21 and the information in Settling Time if this parameter is to be measured. Switching 1 LSB or all of the bits simultaneously produces no significant difference in propagation delay.

FIGURE 22 — SETTLING TIME MEASUREMENT



NOTES:
1) Pulse generator outputs −0.9 V to −1.8 V, $t_r$ and $t_f$ ≈ 2 ns.
2) Adjust $v_{ref}$ for full scale output at $V_A = -1.3000$ V.
3) Adjust R1 for −1.3075 V at input of lower comparator.
4) Adjust R2 for −1.2925 V at input of upper comparator.
5) R1, R2 are 20 turn trimpots.
6) Keep all wiring as short, tidy as possible — isolate all digital and analog supplies, grounds, signal lines, etc.
7) Heavily bypass all supplies at each device, and reference (−) inputs to the comparators.
8) Comparators are high-speed devices, such as AM687ADL.
9) Account for comparator offset when setting reference values.

**Settling Time**

The settling time is defined as the time from the 50% point of the input transition to the point at which the output enters into **and** stays within ± ½LSB (the error band) of the final value. Minimum settling time occurs when the output enters the error band at the maximum slew rate, and then settles out within the band. In actuality, however, the output's slew rate will lessen prior to entering the error band, and then may exit and enter the band once or twice as it settles to its final value. The settling time is determined by the last time the output enters the error band. See Figure 1.

When testing for settling time, the measurement technique used will have an effect on the result. Simply connecting scope probes to an input and output is generally not satisfactory due to the capacitive loading (typically 10–20 pF) of the probes. The rise (fall) time of an ECL input can be significantly increased by such a probe, with the result that the inputs of the MC10318 may be skewed from each other, which, in turn, affects the output. However, probes with low input capacitance, on the order of 2 pF or less (such as FET probes), can be used with very little degradation of the waveforms. The overall propagation delay of the probe (from tip to scope input) must be taken into account, as this can be on the order of 10 ns.

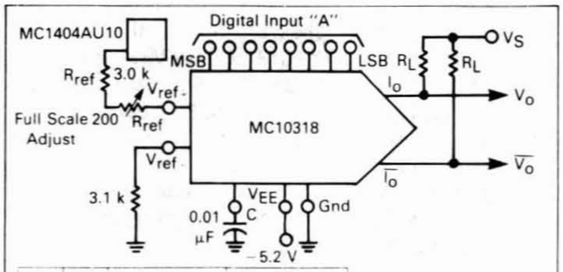
When attempting to view the output on a scope, several factors need to be considered. If the output swing is a full scale transition (e.g., 1.0 V), 1 LSB is 3.9 mV. The scope's amplifier must then be set at a sensitive range (5 mV/cm or 10 mV/cm), with the result that the scope's amplifier will be saturated when the MC10318's output is at the initial value. When the device inputs are switched, the output approaches the final value, but the scope's amplifier will require some time to come out of saturation, and then may overshoot, causing a false indication. In order to overcome this problem, the MC10318 was tested for settling time by connecting the output to a dual high-speed comparator configured as a window detector. The window is 1 LSB wide, centered about the final value. The outputs of the comparators are then monitored on a scope, as they indicate when the MC10318 output is settled within the error band. Propagation delays of the comparators, scope probes, and cable lengths are taken into account. See Figure 22. This method of monitoring the DAC's output, although indirect, does not cause changes to the output waveform because of probe loading, characteristics of the scope, or noise which the probe (and cable) may pick up.

## APPLICATIONS

**Voltage Output**

There are two methods of converting the current output of the MC10318 to voltage outputs, depending on the voltage swing desired. For a limited range (<3.8 V p-p) the circuit of Figure 23 can be used.

**FIGURE 23 — VOLTAGE OUTPUT**

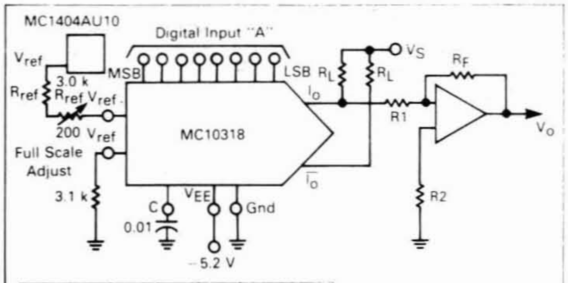


| $V_S$ | $R_L$ | $V_o$ | $\overline{V_o}$ |
|---|---|---|---|
| 0 V | 25.5 | 0 to 1.3 V | 1.3 V to 0 V |
| -2.5 | 49 | -2.5 to 0 V | 0 to -2.5 V |
| -2.5 | 74.5 | -2.5 to 1.3 V | 1.3 to -2.5 V |
| -1.0 | 39 | -1.0 to 1.0 V | 1.0 to -1.0 V |

$$V_O \quad \frac{V_{ref} \cdot A \cdot R_L}{R_{ref} \cdot 16} \cdot V_S$$

Where a larger voltage swing is required, an op amp is required at the output. The choice of op amp will be based on whether accuracy or speed is of primary importance. Where repeatable and stable accuracy is required, the op amp characteristics to consider are open-loop gain, offset voltage, bias current, and temperature drift. Where speed is paramount, a wideband amplifier should be used. Slew rate, propagation delay, and settling time of the op amp are the primary factors to evaluate. The PC board should be designed for high frequency operation, possibly using Microstrip or Stripline techniques. See Figure 24 for a suggested circuit.

**FIGURE 24 — VOLTAGE OUTPUT**



| $R_{ref}$ | $R_L$ | $V_S$ | R1 | $R_F$ | $V_o$ |
|---|---|---|---|---|---|
| 3125 | 20 | 0 | 1.0 k | 5.0 k | 0 to -5 |
| 3125 | 20 | 0 | 1.0 k | 10 k | 0 to -10 |
| 3125 | 40 | -1.02 | 2.0 k | 10 k | 5 to -5 |
| 3125 | 40 | -1.02 | 2.0 k | 20 k | 10 to -10 |

$$V_O \quad \frac{V_{ref}\ A\ R_L}{R_{ref}\ 16}\ \frac{R_F}{(R1 \cdot R_L)}\quad \frac{V_S\ R_F}{(R1 \cdot R_L)}$$

Connecting $I_O$ and $\overline{I_O}$ as shown in the above figures places a constant dc load (51 mA) on the $V_S$ supply, thus facilitating its design. The Gain Adjust resistor should be a 20 turn trimpot, as this will result in one turn equaling approximately 1 LSB of adjustment (for the recommended values in the figure). All of the resistors should have similar temperature coefficients for best temperature stability.

**See Application Note AN848 for further information.**

## WAVEFORM GENERATION

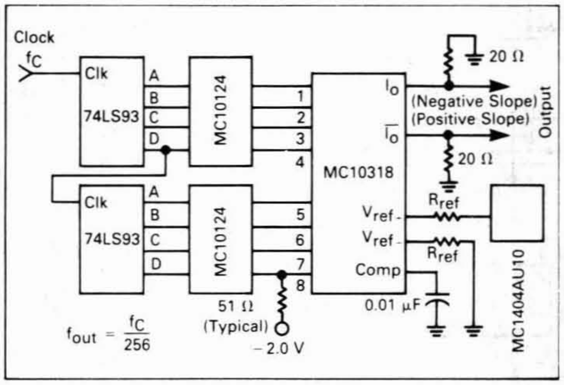

Clock
fC
Clk
74LS93
A
B
C
D
MC10124
1
2
3
4
5
6
7
8
MC10318
Io
Io
20 Ω
(Negative Slope)
(Positive Slope)
Output
Vref-
Vref-
Comp
Rref
Rref
0.01 μF
51 Ω
(Typical)
−2.0 V
MC1404AU10
fout = fC/256

FIGURE 25 — SAWTOOTH GENERATOR

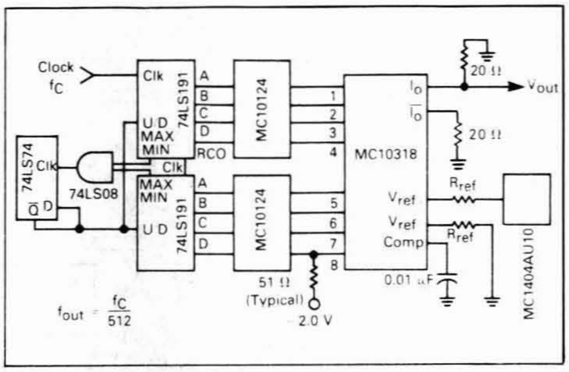
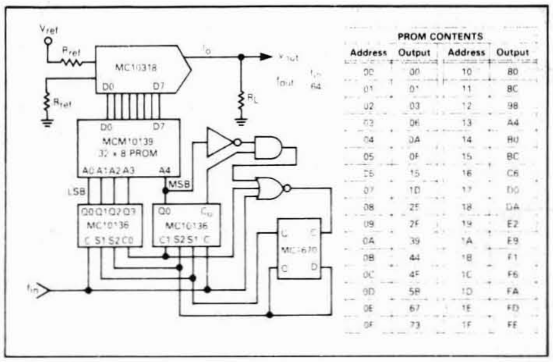

Clock
fC
Clk
74LS191
U/D
MAX
MIN
RCO
74LS74
74LS08
MC10124
MC10318
Vout
20 Ω
Vref
Comp
Rref
0.01 μF
51 Ω
(Typical)
2.0 V
MC1404AU10
fout = fC/512

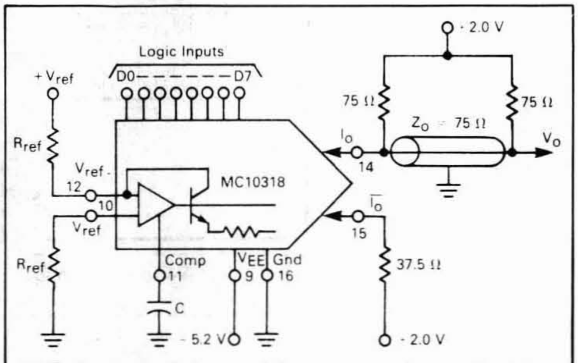
FIGURE 26 — TRIANGLE GENERATOR


Vref
Rref
MC10318
D0
D7
Io
Vout
fout = fin/64
RL
MCM10139
32 × 8 PROM
A0 A1 A2 A3 A4
LSB
MSB
MC10136
MC10136
MC1670
fin

PROM CONTENTS

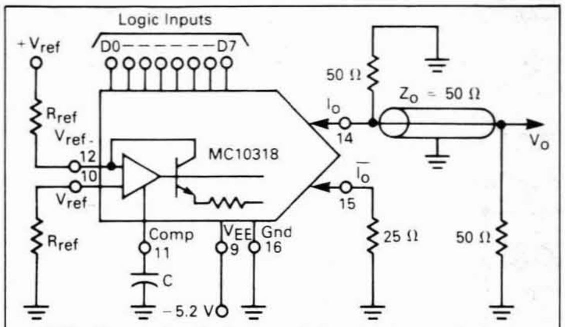
| Address | Output | Address | Output |
|---|---|---|---|
| 00 | 00 | 10 | 80 |
| 01 | 01 | 11 | 8C |
| 02 | 03 | 12 | 98 |
| 03 | 06 | 13 | A4 |
| 04 | 0A | 14 | B0 |
| 05 | 0F | 15 | BC |
| 06 | 15 | 16 | C6 |
| 07 | 1D | 17 | D0 |
| 08 | 25 | 18 | DA |
| 09 | 2F | 19 | E2 |
| 0A | 39 | 1A | E9 |
| 0B | 44 | 1B | F1 |
| 0C | 4F | 1C | F6 |
| 0D | 5B | 1D | FA |
| 0E | 67 | 1E | FD |
| 0F | 73 | 1F | FF |

FIGURE 27 — SINEWAVE GENERATOR


−2.0 V
Logic Inputs
+Vref
D0 — D7
Rref
Vref-
12
10
Vref
MC10318
Io
14
Io
15
75 Ω
75 Ω
Zo = 75 Ω
Vo
37.5 Ω
Comp
11
VEE
9
Gnd
16
C
−5.2 V
−2.0 V

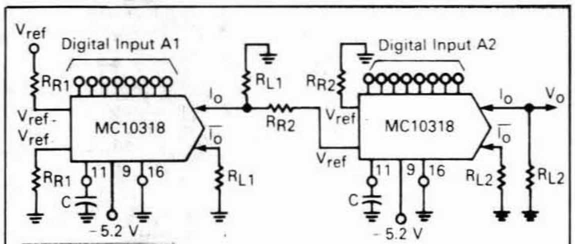
NOTE: Terminating Resistors and $Z_O$ must be matched to within 0.4% to keep initial reflection below 1/2 LSB in magnitude.

FIGURE 28 — OUTPUT CONNECTED TO 75 Ω LINE


Logic Inputs
+Vref
D0 — D7
Rref
Vref-
12
10
Vref
MC10318
Rref
Io
14
Io
15
50 Ω
Zo = 50 Ω
Vo
25 Ω
50 Ω
Comp
11
VEE
9
Gnd
16
C
−5.2 V

NOTE: Terminating Resistors and $Z_O$ must be matched to within 0.4% to keep initial reflection below 1/2 LSB in magnitude.

FIGURE 29 — OUTPUT CONNECTED TO 50 Ω LINE


Vref
Digital Input A1
RR1
Vref-
Vref
MC10318
Io
Io
RL1
RR2
11
9
16
C
−5.2 V
RL1
RR2
Digital Input A2
Vref
Vref
MC10318
Io
Io
Vo
RL2
RL2
−5.2 V

| Suggested Values | |
|---|---|
| $V_{ref}$ | +10 V |
| $R_{R1}$ | 3079* |
| $R_{L1}$ | 20 |
| $R_{R2}$ | 330 |
| $R_{L2}$ | 20 |

$$V_o = \frac{A1 \cdot A2 \cdot V_{ref} \cdot R_{L1} \cdot R_{L2}}{R_{R1} \cdot R_{R2} \cdot 256} = K \cdot A1 \cdot A2$$

(With suggested values, $V_o$ range is 0 to −1.0 V)

* 3.0 k Resistor + 100 Ω Trimpot

FIGURE 30 — DIGITAL MULTIPLICATION

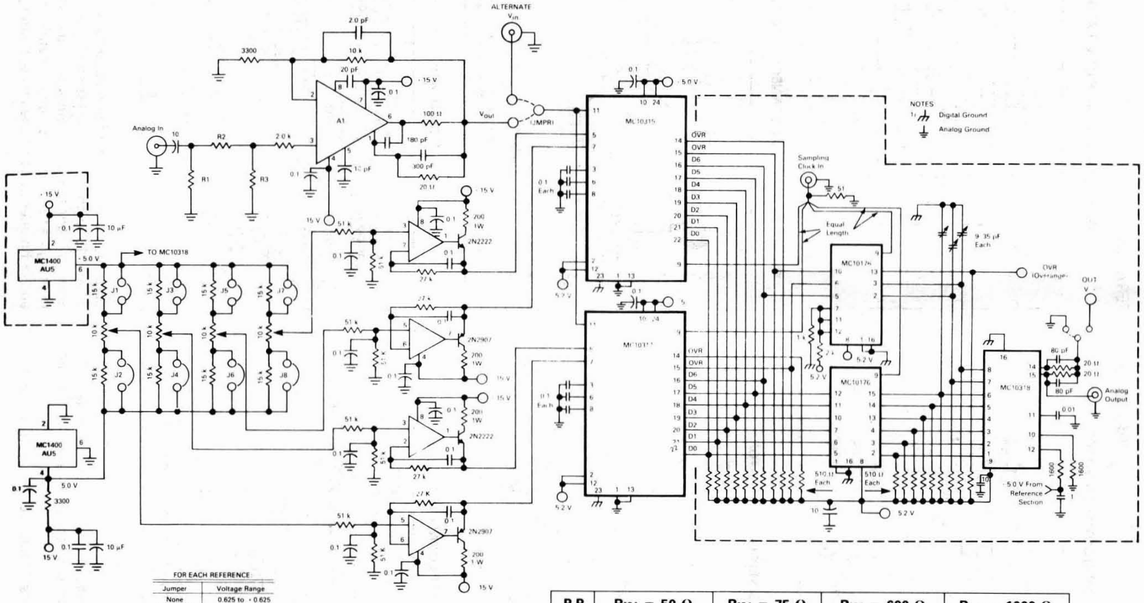
NOTES:

1) When generating waveforms at low frequencies, filtering the output is recommended to smooth out the steps.

2) In many applications, bipolar voltage output may be obtained by monitoring the differential voltage at Pins 14 and 15 (with equal load resistors).

3) When connecting the outputs to transmission lines (See Figures 28 and 29), proper transmission line theory and techniques must be used for optimum performance.

## FIGURE 31 — EVALUATION CIRCUIT BOARD


ALTERNATE
$V_{in}$
2.0 pF
10 k
3300
20 pF
0.1
-15 V
A1
100 Ω
$V_{out}$
JMPR
180 pF
300 pF
20 Ω
Analog In
10
R2
2.0 k
R1
R3
15 V
51 k
200 1W
2N2222
27 k
2N2907
MC1400 AU5
-15 V
10 μF
TO MC10318
-5.0 V
5.0 V
3300
15 V
J1
J2
J3
J4
J5
J6
J7
J8
15 k
10 k
MC10315
MC10317
OVR
D6
D5
D4
D3
D2
D1
D0
0.1 Each
5.2 V
NOTES
Digital Ground
Analog Ground
Sampling Clock In
51
Equal Length
9-35 pF Each
MC10176
OVR (Overrange)
OUT
MC10318
80 pF
20 Ω
Analog Output
510 Ω Each
-5.0 V From Reference Section
1600

FOR EACH REFERENCE

| Jumper | Voltage Range |
|---|---|
| None | 0.625 to 0.625 |
| Odd # Only | 0.5 to 2.5 |
| Even # Only | 2.5 to 0.5 |

— OP AMPS ARE MC34002 BP

| P.P $V_{IN}$ | $R_{IN}$ = 50 Ω R1 | R2 | R3 | $R_{IN}$ = 75 Ω R1 | R2 | R3 | $R_{IN}$ = 600 Ω R1 | R2 | R3 | $R_{IN}$ = 1000 Ω R1 | R2 | R3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 51 | 0 | ∞ | 75 | 0 | ∞ | 1200 | 0 | 1200 | 1000 | 0 | ∞ |
| 2 | 51 | 1300 | 1300 | 100 | 150 | 150 | 1000 | 750 | 750 | 2000 | 1000 | 1000 |
| 4 | 51 | 3000 | 1000 | 91 | 300 | 100 | 1200 | 910 | 300 | 2000 | 1500 | 510 |
| 5 | 51 | 3000 | 750 | 150 | 120 | 30 | 1000 | 1200 | 300 | 3000 | 1200 | 300 |
| 10 | 51 | 2700 | 300 | 100 | 270 | 30 | 750 | 2700 | 300 | 1500 | 2700 | 300 |

## EVALUATION BOARD FOR HIGH SPEED TESTING

**Introduction**

In order to facilitate evaluation of the MC10318 DAC, a PC board layout has been developed providing the appropriate signal levels and timing requirements. The board is designed to simultaneously evaluate the MC10315 and the MC10317 flash ADC's in conjunction with the MC10318 DAC, and the system is capable of passing video speed signals at sampling rates of up to 15 MHz. However, the MC10318 may be evaluated alone by installing only the appropriate components. The board may be purchased from Motorola (blank), or the user may make his own from the artwork shown on Figures 33 and 34.

**Board Specifications**

| | |
|---|---|
| Power supply requirements: | +15 V @ 100 mA. |
| | − 15 V @ 120 mA. |
| | −5.2 V @ 550 mA. |
| | +5.0 V @ 300 mA. |

Sampling clock: $V_{IH} = -0.9$ V, $V_{IL} = -1.8$ V (ECL levels) terminated with 50 ohms, 15 MHz max.
Analog Input level: Selectable, see chart.
Analog Input Impedance: Selectable, see chart.
Output level: 0 to −1.0 V, user alterable.
Digital Input levels: (When ADC converters are not included) $V_{IH} = -0.9$ V, $V_{IL} = -1.8$ V (ECL levels).

**Operation**

The power supplies should be connected as shown in Figure 32. The leads should be short and direct.

The CLK Input (necessary if the ADC converters and or the latches are used) uses a BNC connector, and is terminated with 50 ohms to ground.

The Analog Input level (if the ADC converters are installed) depends on the input resistors selected (see chart). The output of the buffer amplifier should produce a maximum 4 V p-p signal, or an amplitude equal to the references (user adjustable).

The Analog Output is 0 to −1.0 V, corresponding to a digital input (to the MC10318) of FF and 00 respectively. Output impedance is normally 20 ohms, but may be varied by the user (see previous text).

**Options**

**Input Signal** — The p-p voltage level of the analog input signal (when using the ADC converters) is accommodated by selection of the input resistors from the chart (see schematic).

**ALT IN** — The analog signal may be applied directly to the ADC converters (by-passing the on-board amplifier) by applying the input signal to this connector, and relocating the jumper adjacent to the ALT IN connector. The signal source must be capable of driving 2.5 k ohms in parallel with approx. 140 pF.

**V+ OUT** — A pullup voltage (max. +2.5 V) may be applied to this connector in order to increase the output voltage swing. See the APPLICATIONS section of this data sheet. The 20 ohm load resistors may then be changed to other values. The jumper adjacent to the A OUT connector must be relocated.

**Evaluating the MC10318 only** — Only those components within the dotted line on the schematic are required. The digital inputs (ECL level) are to be applied to a connector strip located in pins 15–22 of the MC10317 position. +15 V and −5.2 V supplies are required. The latches transfer the information on the rising edge of the clock.

**Video Testing**

The above described printed circuit board has been tested, with a standard video test signal, for differential phase and differential gain (40 IRE sub-carrier on a 100 IRE ramp, sampled at 14.3 MHz) with results of 1% gain error and 2° phase error. The signal was obtained from a Tektronix 147A video test generator, applied to the ALT IN connector. The output (of the MC10318) was configured into a 75 ohm output impedance, and applied to a vector scope.

Tests conducted with the Evaluation Board in a video system (video camera and a TV monitor) showed no visible degradation of picture quality (at 8 bits resolution). The board provides an easy means of testing picture quality at reduced number of bits, or for conducting any test on a digitized video signal.

FIGURE 32 — COMPONENT LOCATION AND EXTERNAL CONNECTIONS

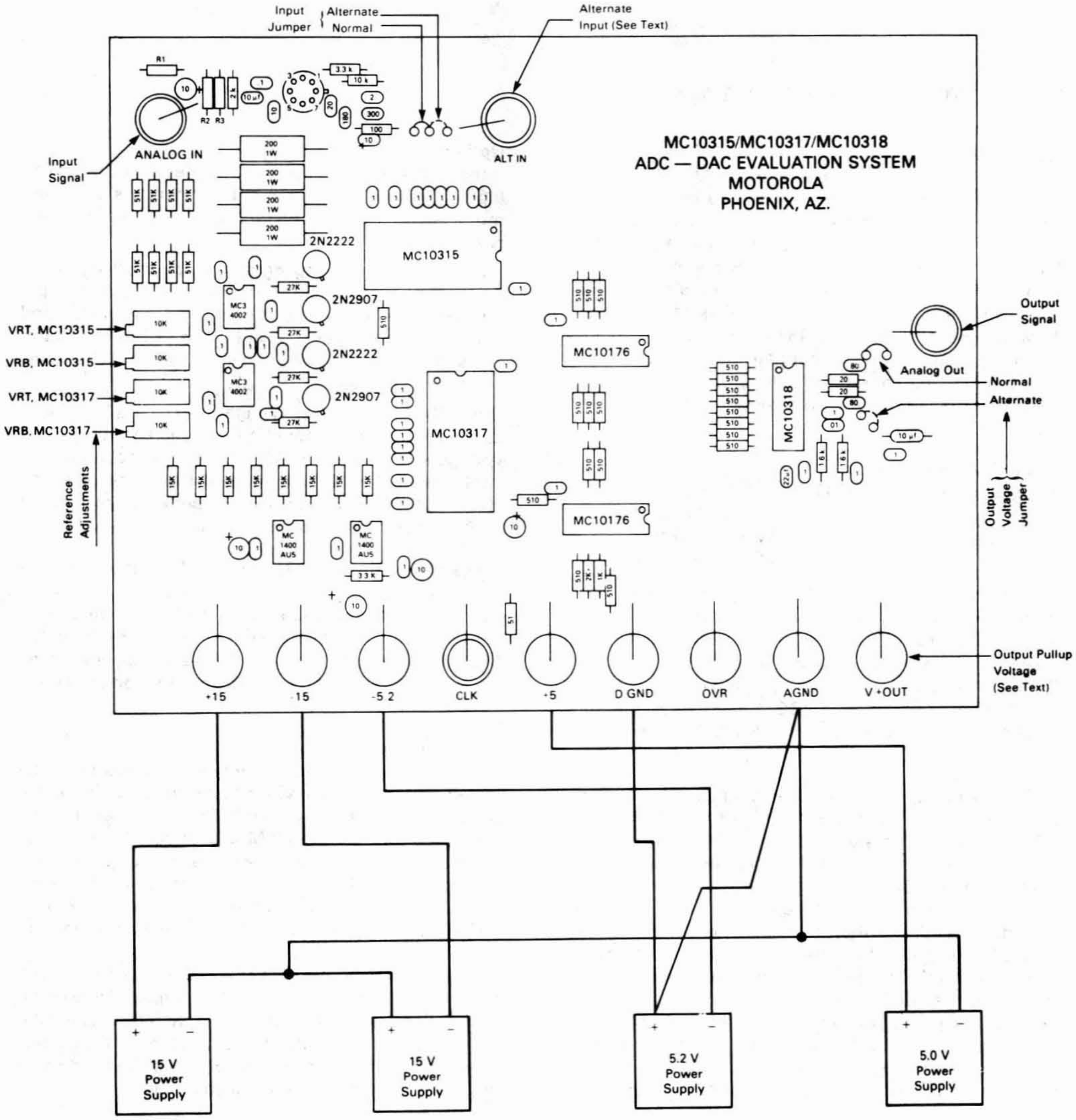

Input Jumper
Alternate
Normal
Alternate Input (See Text)
MC10315/MC10317/MC10318
ADC — DAC EVALUATION SYSTEM
MOTOROLA
PHOENIX, AZ.
ANALOG IN
ALT IN
Input Signal
2N2222
2N2907
MC10315
MC10317
MC10318
MC10176
MC3 4002
MC 1400 AUS
VRT, MC10315
VRB, MC10315
VRT, MC10317
VRB, MC10317
Reference Adjustments
Output Signal
Analog Out
Normal
Alternate
Output Voltage Jumper
Output Pullup Voltage (See Text)
+15
-15
-5.2
CLK
+5
D GND
OVR
AGND
V +OUT
15 V Power Supply
15 V Power Supply
5.2 V Power Supply
5.0 V Power Supply

FIGURE 33 — COMPONENT SIDE ARTWORK (TOP)
(OVERALL SIZE = 6.00″ × 8.00″)

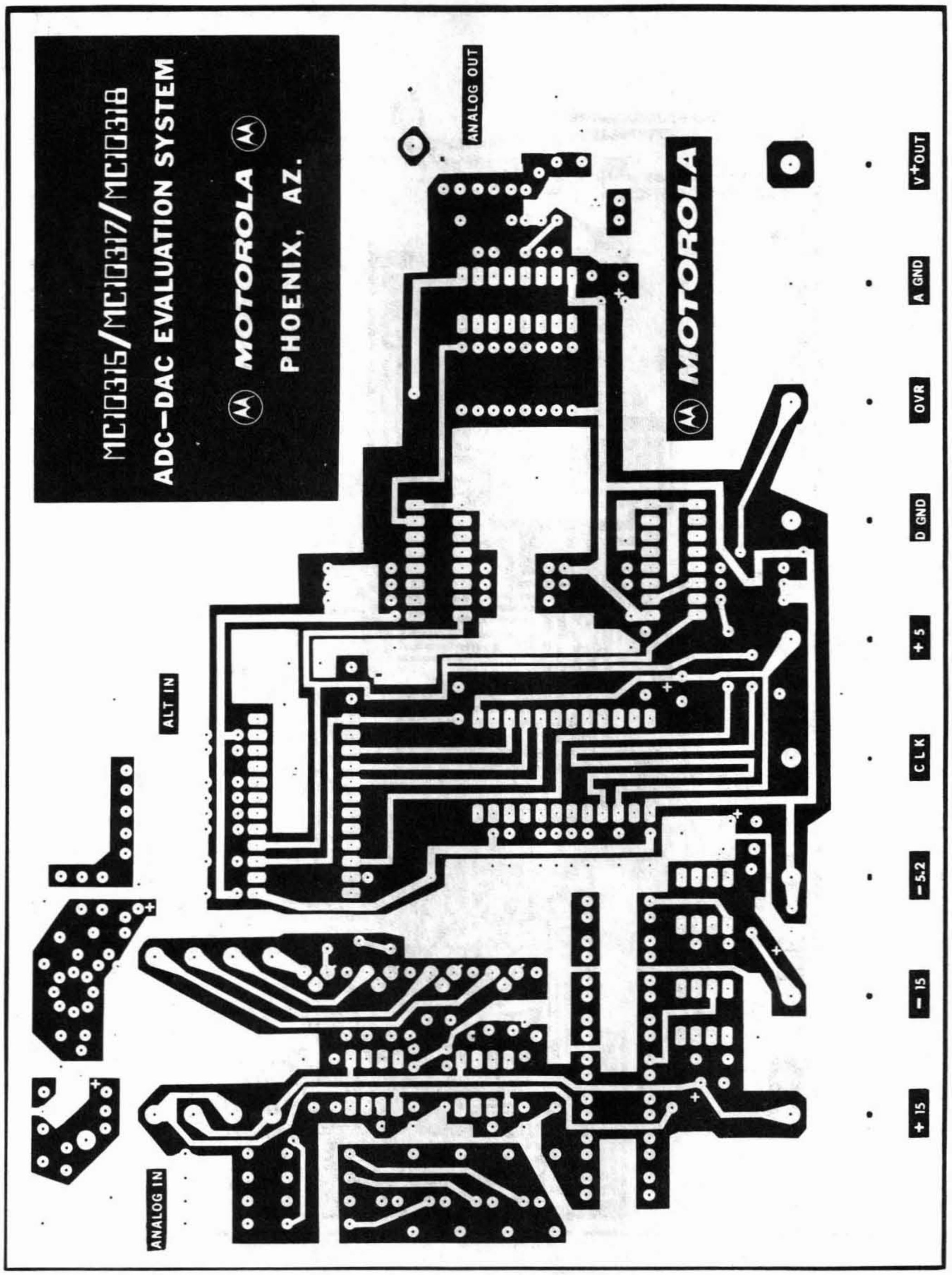

MC10315/MC10317/MC10318
ADC–DAC EVALUATION SYSTEM
MOTOROLA
PHOENIX, AZ.
ANALOG OUT
MOTOROLA
V+OUT
A GND
OVR
D GND
+5
CLK
−5.2
−15
+15
ALT IN
ANALOG IN

FIGURE 34 — SOLDER SIDE ARTWORK (BOTTOM)

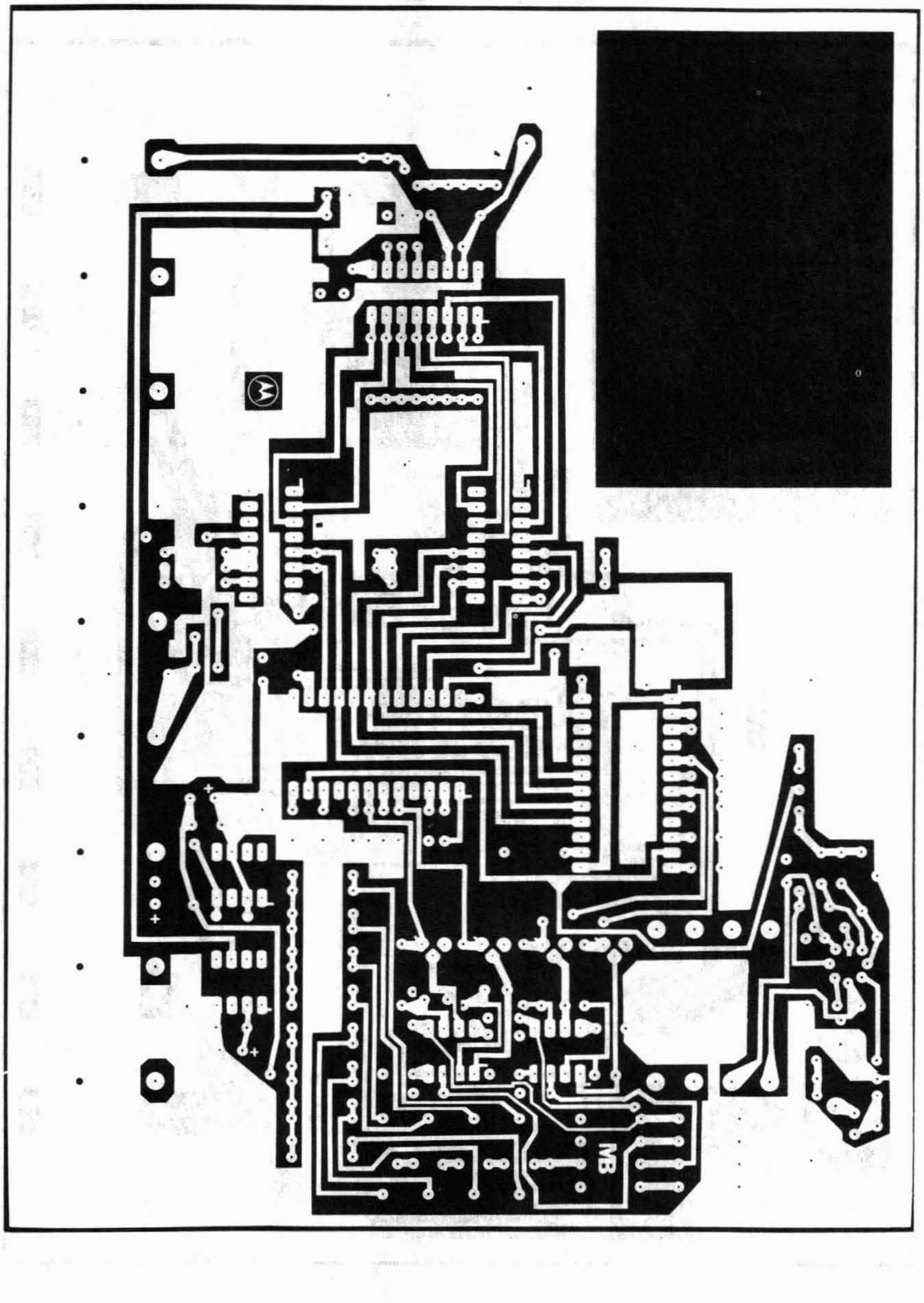
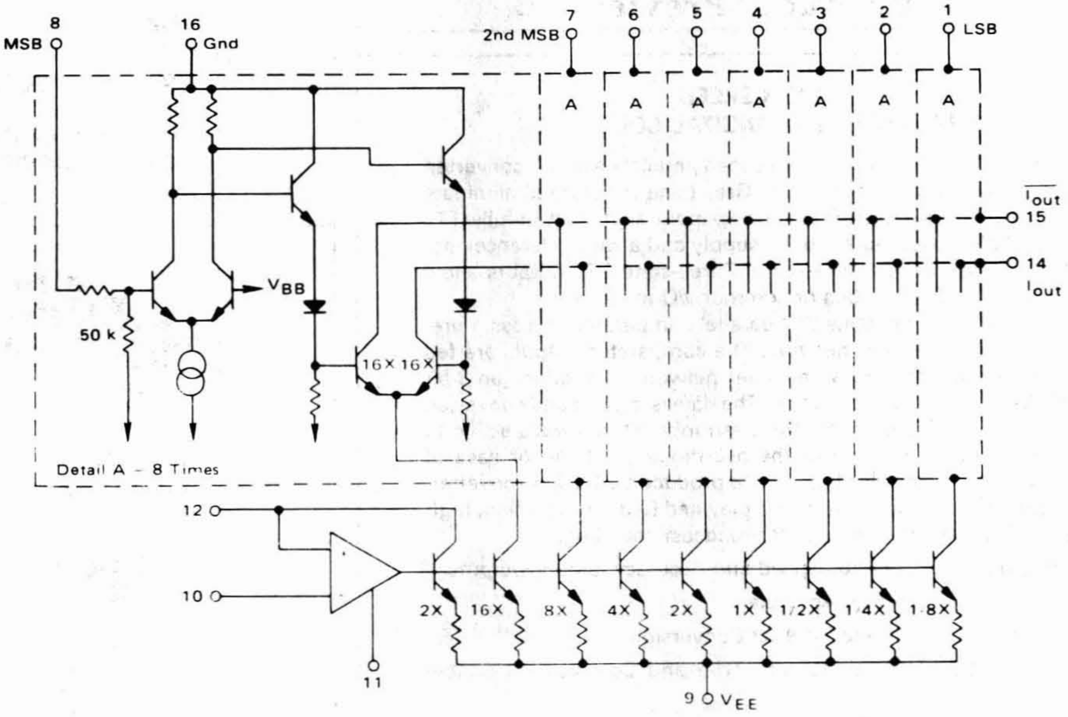


FIGURE 35 — MC10318 EQUIVALENT CIRCUIT


8
MSB
16
Gnd
7
2nd MSB
6
5
4
3
2
1
LSB
A
A
A
A
A
A
A
$\overline{I_{out}}$
15
14
$I_{out}$
$V_{BB}$
50 k
16X 16X
Detail A – 8 Times
12
10
11
2X
16X
8X
4X
2X
1X
1/2X
1/4X
1/8X
9
$V_{EE}$

**MOTOROLA**

# MC10319

## Product Preview

### HIGH SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTER

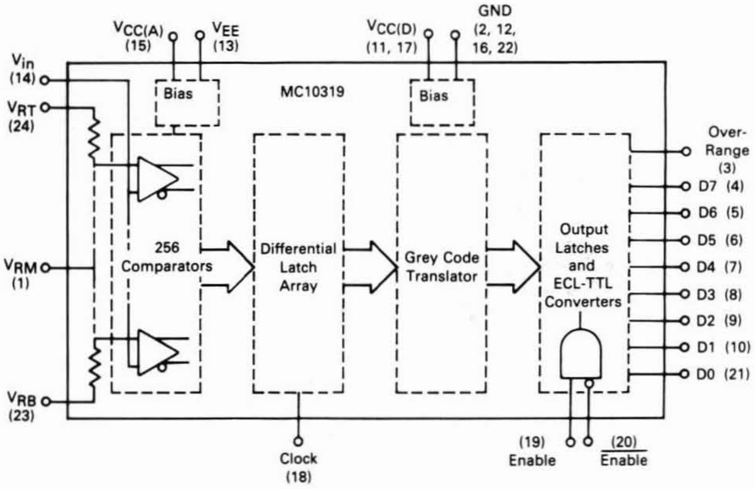
The MC10319 is an 8-bit high speed parallel flash A/D converter. The device employs an internal Grey code structure to eliminate large output errors on fast slewing input signals. It is fully TTL compatible, requiring a +5.0 V supply and a wide tolerance negative supply of −3.0 to −6.0 V. Three-state TTL outputs allow direct drive of a data bus or common I/O memory.

The MC10319 contains 256 parallel comparators across a precision input reference network. The comparator outputs are fed to latches and then to an encoder network, to produce an 8-bit data byte plus an overrange bit. The data is latched and converted to 3-state LS-TTL outputs. The overrange bit is always active to allow for either sensing of the overrange condition or ease of interconnecting a pair of devices to produce a 9-bit A/D converter.

Applications include Video Display and Radar processing, high speed Instrumentation and TV Broadcast encoding.

- Internal Grey Code for Speed and Accuracy, Binary Outputs
- 8-Bit Resolution/9-Bit Accurate
- Easily Interconnected for 9-Bit Conversion
- 3-State LS-TTL Outputs with True and Complement Enable Inputs
- 25 MHz Sampling Rate
- Wide Input Range: 1.0–2.0 Vp-p Between ±2.0 V
- Low Input Capacitance: 50 pF
- Power Dissipation: 600 mW
- No Sample/Hold Required for Video Bandwidth Signals
- Single Clock Cycle Conversion

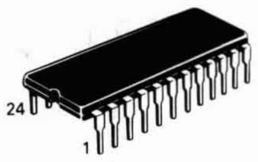
### BLOCK DIAGRAM



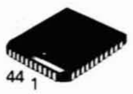
$V_{CC(A)}$ (15)
$V_{EE}$ (13)
$V_{CC(D)}$ (11, 17)
GND (2, 12, 16, 22)
$V_{in}$ (14)
$V_{RT}$ (24)
$V_{RM}$ (1)
$V_{RB}$ (23)
Bias
MC10319
Bias
256 Comparators
Differential Latch Array
Grey Code Translator
Output Latches and ECL-TTL Converters
Over-Range (3)
D7 (4)
D6 (5)
D5 (6)
D4 (7)
D3 (8)
D2 (9)
D1 (10)
D0 (21)
Clock (18)
(19) Enable
(20) $\overline{\text{Enable}}$

### HIGH SPEED 8-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

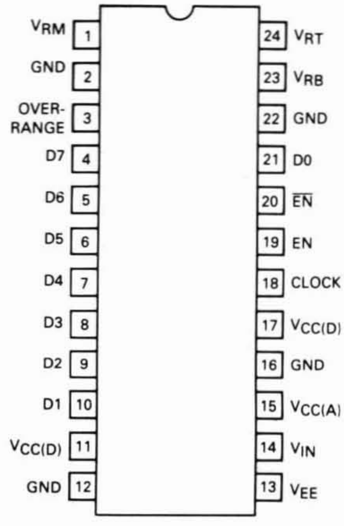


**L SUFFIX**
CERAMIC PACKAGE
CASE 623-05



**FN SUFFIX**
PLASTIC PACKAGE
CASE 777-01
PLCC-44

### PIN DIAGRAM



$V_{RM}$ 1
GND 2
OVER-RANGE 3
D7 4
D6 5
D5 6
D4 7
D3 8
D2 9
D1 10
$V_{CC(D)}$ 11
GND 12
24 $V_{RT}$
23 $V_{RB}$
22 GND
21 D0
20 $\overline{\text{EN}}$
19 EN
18 CLOCK
17 $V_{CC(D)}$
16 GND
15 $V_{CC(A)}$
14 $V_{IN}$
13 $V_{EE}$

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC10319FN | 0° to +70°C | PLCC-44 |
| MC10319L | | Ceramic |

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC(A),(D)}$<br>$V_{EE}$ | +7.0<br>−7.0 | Vdc |
| Positive Supply Voltage Differential | $V_{CC(D)} - V_{CC(A)}$ | 0, −0.3 | V |
| Input Voltage (Digital Inputs) | $V_{I(D)}$ | −0.5 to +7.0 | V |
| Output Voltage (Data Bits in 3-State Mode) | $V_O$ | −0.3 to $V_{CC\ (D)}$ | V |
| Outputs Short Circuit Current (Note 1) | $I_{SC}$ | 225 | mA |
| Input Voltage ($V_{in}$, $V_{RT}$, $V_{RM}$, $V_{RB}$) | $V_{I(A)}$ | ±2.5 | V |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance Junction to Air | $R_{\theta JA}$ | 60 | °C/W |

Note 1. Not more than one output should be shorted at a time. Duration of short should not exceed 1 second.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $V_{EE}$ = −5.2 Vdc, $V_{RT} - V_{RB}$ = 2.0 Vdc, $f_s$ = 22 MHz, $T_A$ = +25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Resolution | N | — | — | 8.0 | Bits |
| Nonlinearity | NL | — | ±0.10 | ±0.19 | % |
| Differential Nonlinearity | DNL | — | — | ±0.10 | % |
| Analog Input Capacitance | $C_{in}$ | — | 50 | — | pF |
| Reference Ladder Resistance (Total Resistance) | $R_{Ref}$ | — | 130 | — | Ω |
| Maximum Sampling Frequency | $f_s$ | — | 25 | — | MHz |
| Sampling Clock Symmetry ($f_s$ = 25 MHz) | | 40 | 50 | 60 | % |
| Digital Input Current $V_{IL}$ = 0.4 V<br>$V_{IH}$ = 2.7 V | $I_{IL}$<br>$I_{IH}$ | —<br>— | —<br>— | −600<br>50 | μA |
| Digital Input Voltage Thresholds Low Logic State<br>High Logic State | $V_{IL}$<br>$V_{IH}$ | 2.0<br>— | —<br>— | —<br>0.8 | V |
| Input Clamp Voltage ($V_{CC}$ = +4.5 V, $I_{IK}$ = −18 mA) | $V_{IK}$ | — | — | −1.5 | V |
| Digital Output Voltage Levels, $V_{CC}$ = +4.5 V<br>Low Logic State ($I_{OL}$ = −8.0 mA)<br>High Logic State ($I_{OH}$ = 400 μA) | <br>$V_{OL}$<br>$V_{OH}$ | <br>—<br>2.4 | <br>—<br>— | <br>0.4<br>— | V |
| Output Current — High Impedance State, $V_{CC}$ = +5.5 V<br>$V_{OL}$ = 0.4 V<br>$V_{OH}$ = 2.4 V | $I_{OZ}$ | <br>—<br>— | <br>—<br>— | <br>−20<br>20 | μA |
| Power Supply Current | $I_{CC}$<br>$I_{EE}$ | —<br>— | 100<br>10 | —<br>— | mA |

**MOTOROLA**

# MC34115

## Specifications and Applications Information

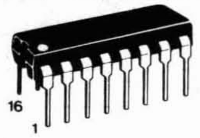
3

## CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

## CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

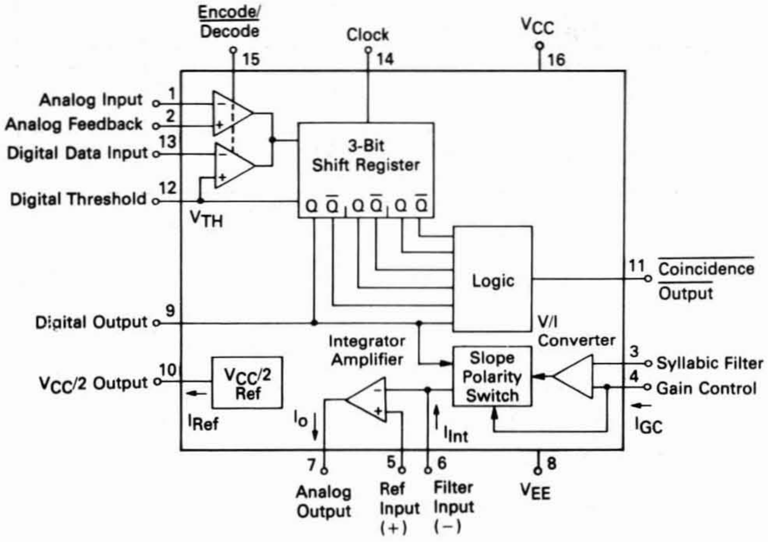
Providing a simplified approach to digital speech encoding/decoding, the MC34115 CVSD is designed for speech synthesis and commercial telephone applications. A single IC provides both encoding and decoding functions.

- Encode and Decode Functions Selectable with a Digital Input
- Utilization of Compatible $I^2L$ — Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- 3-Bit Algorithm

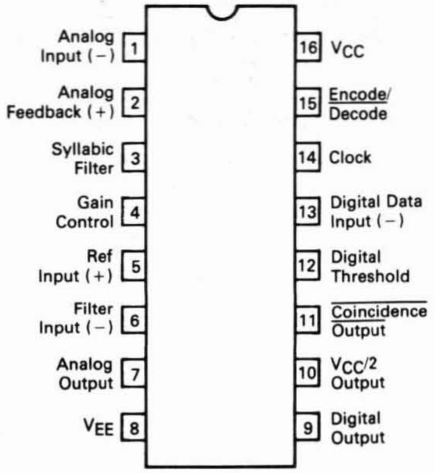


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### CVSD BLOCK DIAGRAM


Encode/ Decode
15
Clock
14
VCC
16
Analog Input 1
Analog Feedback 2
Digital Data Input 13
Digital Threshold 12
VTH
3-Bit Shift Register
Q Q̄ Q Q̄ Q Q̄
Logic
11 Coincidence Output
Digital Output 9
V/I Converter
Integrator Amplifier
Slope Polarity Switch
3 Syllabic Filter
4 Gain Control
VCC/2 Output 10
VCC/2 Ref
IRef
IO
IInt
IGC
7 Analog Output
5 Ref Input (+)
6 Filter Input (−)
8 VEE

### PIN CONNECTIONS


Analog Input (−) 1
Analog Feedback (+) 2
Syllabic Filter 3
Gain Control 4
Ref Input (+) 5
Filter Input (−) 6
Analog Output 7
VEE 8
16 VCC
15 Encode/ Decode
14 Clock
13 Digital Data Input (−)
12 Digital Threshold
11 Coincidence Output
10 VCC/2 Output
9 Digital Output

## MAXIMUM RATINGS

(All voltages referenced to $V_{EE}$, $T_A$ = 25°C unless otherwise noted.) (See Note 2.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | −0.4 to +18 | Vdc |
| Differential Analog Input Voltage | $V_{ID}$ | ±5.0 | Vdc |
| Digital Threshold Voltage | $V_{TH}$ | −0.4 to $V_{CC}$ | Vdc |
| Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$) | $V_{Logic}$ | −0.4 to +18 | Vdc |
| Coincidence Output Voltage | $V_{O(Con)}$ | −0.4 to +18 | Vdc |
| Syllabic Filter Input Voltage | $V_{I(Syl)}$ | −0.4 to $V_{CC}$ | Vdc |
| Gain Control Input Voltage | $V_{I(GC)}$ | −0.4 to $V_{CC}$ | Vdc |
| Reference Input Voltage | $V_{I(Ref)}$ | $V_{CC}/2 - 1.0$ to $V_{CC}$ | Vdc |
| $V_{CC}/2$ Output Current | $I_{Ref}$ | −25 | mA |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Operating Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +125 | °C |

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 12 V, $V_{EE}$ = Gnd, $T_A$ = 0°C to + 70°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage Range (Figure 1) | $V_{CC}$ | 4.75 | 12 | 16.5 | Vdc |
| Power Supply Current (Figure 1) | $I_{CC}$ | | | | mA |
| (Idle Channel) | | | | | |
| $V_{CC}$ = 5.0 V | | — | 4.6 | 7.5 | |
| $V_{CC}$ = 15 V | | — | 7.0 | 12 | |
| Clock Rate | SR | — | 16 k | — | Samples/s |
| Gain Control Current Range (Figure 2) | $I_{GCR}$ | 0.002 | — | 3.0 | mA |
| Analog Comparator Input Range (Pins 1 and 2)<br>4.75 V ≤ $V_{CC}$ ≤ 16.5 V | $V_I$ | 1.3 | — | $V_{CC}$ −1.3 | Vdc |
| Analog Output Range (Pin 7)<br>4.75 V ≤ $V_{CC}$ ≤ 16.5 V, $I_O$ = ±5.0 mA | $V_O$ | 1.3 | — | $V_{CC}$ −1.3 | Vdc |
| Input Bias Currents (Figure 3) | $I_{IB}$ | | | | μA |
| Comparator in Active Region | | | | | |
| Analog Input (I1) | | — | 0.5 | 2.5 | |
| Analog Feedback (I2) | | — | 0.5 | 2.5 | |
| Syllabic Filter Input (I3) | | — | 0.06 | 0.5 | |
| Reference Input (I5) | | — | −0.06 | −0.5 | |
| Input Offset Current | $I_{IO}$ | | | | μA |
| Comparator in Active Region | | | | | |
| Analog Input/Analog Feedback<br>\|I1−I2\| — Figure 3 | | — | 0.15 | 0.8 | |
| Integrator Amplifier<br>\|I5−I6\| — Figure 4 | | — | 0.02 | 0.2 | |
| Input Offset Voltage<br>V/I Converter (Pins 3 and 4) — Figure 5 | $V_{IO}$ | — | 2.0 | 10 | mV |
| Transconductance | gm | | | | mA/mV |
| V/I Converter, 0 to 3.0 mA | | 0.1 | 0.3 | — | |
| Integrator Amplifier, 0 to +5.0 mA Load | | 1.0 | 10 | — | |
| Propagation Delay Times (Note 1) | | | | | μs |
| Clock Trigger to Digital Output | $t_{PLH}$ | — | 1.0 | 3.0 | |
| $C_L$ = 25 pF to Gnd | $t_{PHL}$ | — | 0.8 | 3.0 | |
| Clock Trigger to Coincidence Output | $t_{PLH}$ | — | 1.0 | 3.5 | |
| $C_L$ = 25 pF to Gnd | $t_{PHL}$ | — | 0.8 | 2.5 | |
| $R_L$ = 4.0 kΩ to $V_{CC}$ | | | | | |

NOTES 1. All propagation delay times measured 50% to 50% from the negative going (from $V_{CC}$ to +0.4 V) edge of the clock.
2. Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation.

**ELECTRICAL CHARACTERISTICS (continued)**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Coincidence Output Voltage — Low Logic State<br>$I_{OL(Con)} = 3.0$ mA | $V_{OL(Con)}$ | — | 0.12 | 0.25 | Vdc |
| Coincidence Output Leakage Current — High Logic State<br>$V_{OH} = 15$ V | $I_{OH(Con)}$ | — | 0.01 | 0.5 | μA |
| Applied Digital Threshold Voltage Range (Pin 12) | $V_{TH}$ | +1.2 | — | $V_{CC}$ −2.0 | Vdc |
| Digital Threshold Input Current<br>1.2 V ≤ $V_{th}$ ≤ $V_{CC}$ −2.0 V | $I_{I(th)}$ | | | | μA |
| $V_{IL}$ applied to Pins 13, 14 and 15 | | — | — | 5.0 | |
| $V_{IH}$ applied to Pins 13, 14 and 15 | | — | −10 | −50 | |
| Maximum Integrator Amplifier Output Current | $I_O$ | ±5.0 | — | — | mA |
| $V_{CC}/2$ Generator Maximum Output Current (Source only) | $I_{Ref}$ | +10 | — | — | mA |
| $V_{CC}/2$ Generator Output Impedance<br>0 to +10 mA | $z_{Ref}$ | — | 3.0 | 6.0 | Ω |
| $V_{CC}/2$ Generator Tolerance<br>4.75 V ≤ $V_{CC}$ ≤ 16.5 V | $\epsilon r$ | — | — | ±3.5 | % |
| Logic Input Voltage (Pins 13, 14 and 15) | | | | | Vdc |
| Low Logic State | $V_{IL}$ | Gnd | — | $V_{th}$ −0.4 | |
| High Logic State | $V_{IH}$ | $V_{th}$ +0.4 | — | 16.5 | |
| Dynamic Total Loop Offset Voltage (Note 3) — Figures 3, 4 and 5 | $\Sigma V_{offset}$ | | | | mV |
| $I_{GC} = 33$ μA, $V_{CC} = 12$ V | | | | | |
| $T_A = 25°C$ | | — | ±2.5 | ±7.0 | |
| 0°C ≤ $T_A$ ≤ +70°C | | — | ±3.0 | ±10 | |
| $I_{GC} = 33$ μA, $V_{CC} = 5.0$ V | | | | | |
| $T_A = 25°C$ | | — | ±4.0 | ±8.0 | |
| 0°C ≤ $T_A$ ≤ +70°C | | — | ±4.5 | ±12 | |
| Digital Output Voltage (Pin 9) | | | | | Vdc |
| $I_{OL} = 3.6$ mA | $V_{OL}$ | — | 0.1 | 0.4 | |
| $I_{OH} = -0.35$ mA | $V_{OH}$ | $V_{CC}$ −1.0 | $V_{CC}$ −0.2 | — | |
| Syllabic Filter Applied Voltage (Pin 3) | $V_{I(Syl)}$ | +3.2 | — | $V_{CC}$ | Vdc |
| Integrating Current (Figure 2) | $\lvert I_{Int} \rvert$ | | | | |
| $I_{GC} = 12$ μA | | 8.0 | 10 | 12 | μA |
| $I_{GC} = 1.5$ mA | | 1.4 | 1.5 | 1.6 | mA |
| $I_{GC} = 3.0$ mA | | 2.75 | 3.0 | 3.25 | mA |
| Dynamic Integrating Current Match (Figure 6)<br>$I_{GC} = 1.5$ mA | $V_{O(Ave)}$ | — | ±100 | ±300 | mV |
| Input Current — High Logic State<br>$V_{IH} = 16.5$ V | $I_{IH}$ | | | | μA |
| Digital Data Input | | — | — | +5.0 | |
| Clock Input | | — | — | +5.0 | |
| Encode/$\overline{\text{Decode}}$ Input | | — | — | +5.0 | |
| Input Current — Low Logic State<br>$V_{IL} = 0$ V | $I_{IL}$ | | | | μA |
| Digital Data Input | | — | — | −10 | |
| Clock Input | | — | — | −360 | |
| Encode/$\overline{\text{Decode}}$ Input | | — | — | −36 | |
| Clock Input, $V_{IL} = 0.4$ V | | — | — | −72 | |

NOTE 3. Dynamic total loop offset ($\Sigma V_{offset}$) equals $V_{IO}$ (comparator) (Figure 3) minus $V_{IOX}$ (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. The clock frequency is 16 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size).

## DEFINITIONS AND FUNCTION OF PINS

**Pin 1 — Analog Input**

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between Pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

**Pin 2 — Analog Feedback**

This is the non-inverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be Pin 7 or a low pass filter output connected to Pin 7. In a decode circuit Pin 2 is not used and may be tied to $V_{CC}/2$ on Pin 10, ground or left open.

The analog input comparator has bias currents of 2.5 μA max, thus the driving impedances of Pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

**Pin 3 — Syllabic Filter**

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between Pins 11 and 3. Typical time constant values of 6 ms to 50 ms are used in voice codecs.

**Pin 4 — Gain Control Input**

The syllabic filter voltage appears across $C_S$ of the syllabic filter and is the voltage between $V_{CC}$ and Pin 3. The active voltage to current (V–I) converter drives Pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into Pin 4 ($I_{GC}$) is the syllabic filter voltage divided by the $R_x$ resistance. Figure 7 shows the relationship between $I_{GC}$ (x-axis) and the integrating current, $I_{Int}$ (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The $R_x$ resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

**Pin 5 — Reference Input**

This pin is the non-inverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as Pin 1 and is tied to Pin 10.

**Pin 6 — Filter Input**

This inverting op amp input is used to connect the integrator external components. The integrating current ($I_{Int}$) flows into Pin 6 when the analog input (Pin 1) is high with respect to the analog feedback (Pin 2) in the encode mode or when the digital data input (Pin 13) is high in the decode mode. For the opposite states, $I_{Int}$ flows out of Pin 6. Single integration systems require a capacitor and resistor between Pins 6 and 7. Multipole configurations will have different circuitry. The resistance between Pins 6 and 7 should typically be between 8 kΩ and 13 kΩ to maintain good idle channel characteristics.

**Pin 7 — Analog Output**

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $V_{CC}/2$ to +6 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

**Pin 8 — $V_{EE}$**

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

**Pin 9 — Digital Output**

The digital output provides the results of the delta modulator's conversion. It swings between $V_{CC}$ and $V_{EE}$ and is CMOS or TTL compatible. Pin 9 is inverting with respect to Pin 1 and non-inverting with respect to Pin 2. It is clocked on the falling edge of Pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for $V_{CC} = 12$ V and $C_L = 25$ pF to ground.

**Pin 10 — $V_{CC}/2$ Output**

An internal low impedance mid-supply reference is provided for use of the MC34115 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6 dBmo signal is expected across a 600 ohm input bias resistor, then Pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if Pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from Pin 10 to $V_{EE}$ is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

**Pin 11 — $\overline{\text{Coincidence Output}}$**

The coincidence output will be low whenever the content of the internal 3 bit shift register is all 1s or all 0s. Pin 11 is an open collector of an NPN device and requires a pull-up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of $R_p$ should be much less than $R_S$. In systems requiring different charge and discharge constants, the charging

## DEFINITIONS AND FUNCTION OF PINS (continued)

constant is $R_S C_S$ while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3 mA. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for $R_L = 4\ k\Omega$ to +12 V and $C_L = 25$ pF to ground.

**Pin 12 — Digital Threshold**

This input sets the switching threshold for Pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Typically it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above $V_{EE}$ for TTL interface.

**Pin 13 — Digital Data Input**

In a decode application, the digital data stream is applied to Pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of Pin 15. It is an inverting input with respect to Pin 9. When Pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 μs before and after the clock trigger for proper clocking.

**Pin 14 — Clock Input**

The clock input determines the data rate of the codec circuit. A 16K bit rate requires a 16 kHz clock. The switching threshold of the clock input is set by Pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive-going pulse on the clock input is 300 ns, whereas for a negative-going pulse, it is 900 ns.

**Pin 15 — Encode/$\overline{\text{Decode}}$**

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at Pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through Pin 13 in an encoder.

**Pin 16 — $V_{CC}$**

The power supply range is from 4.75 to 16.5 volts between pin $V_{CC}$ and $V_{EE}$.

FIGURE 1 — POWER SUPPLY CURRENT

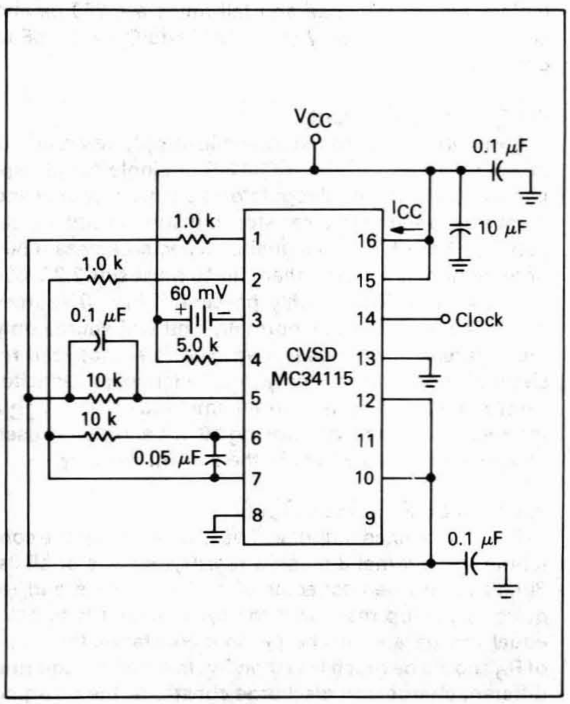
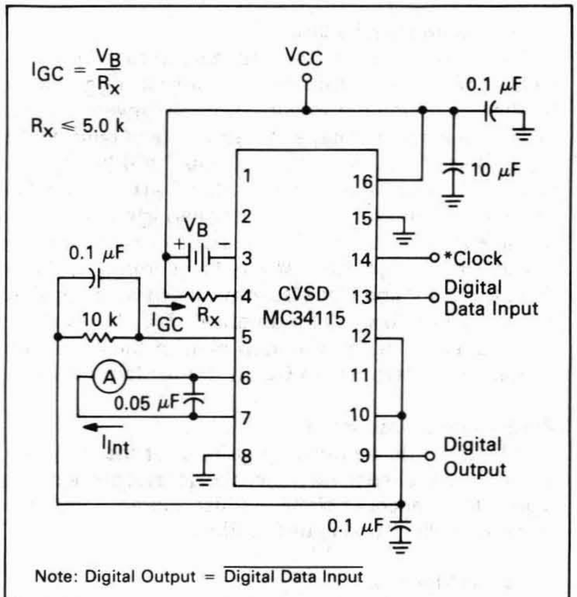


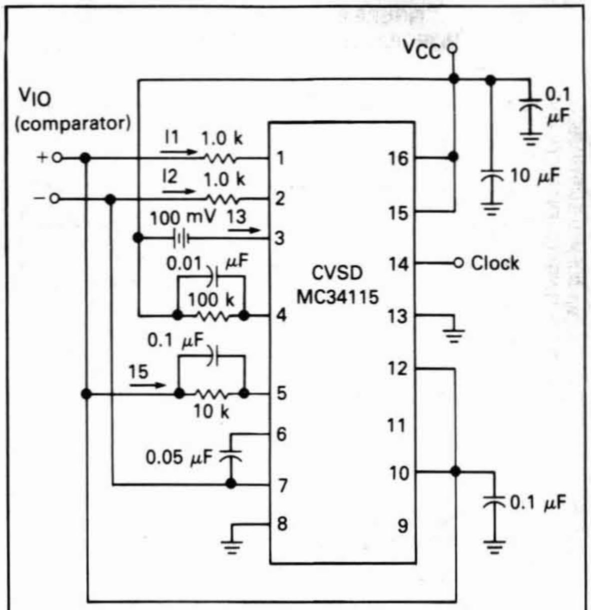
FIGURE 2 — $I_{GCR}$, GAIN CONTROL RANGE and $I_{Int}$ — INTEGRATING CURRENT



Note: Digital Output = $\overline{\text{Digital Data Input}}$

*For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

**FIGURE 3 — INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT**


VCC
VIO
(comparator)
+
−
I1 1.0 k
I2 1.0 k
100 mV I3
0.01 μF
100 k
0.1 μF
I5
10 k
0.05 μF
0.1 μF
10 μF
0.1 μF
CVSD
MC34115
Clock
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

**FIGURE 4 — INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT**

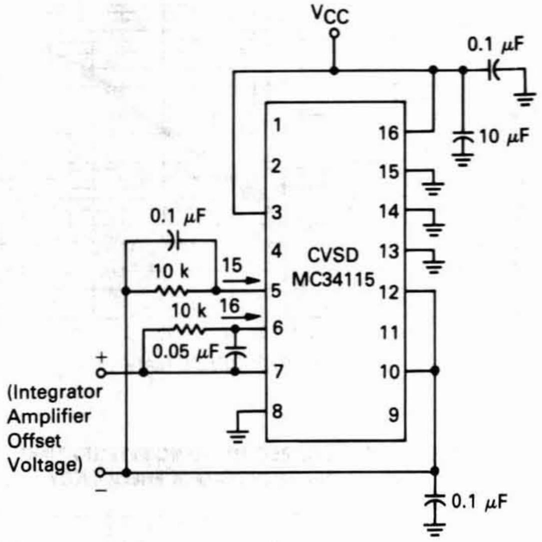
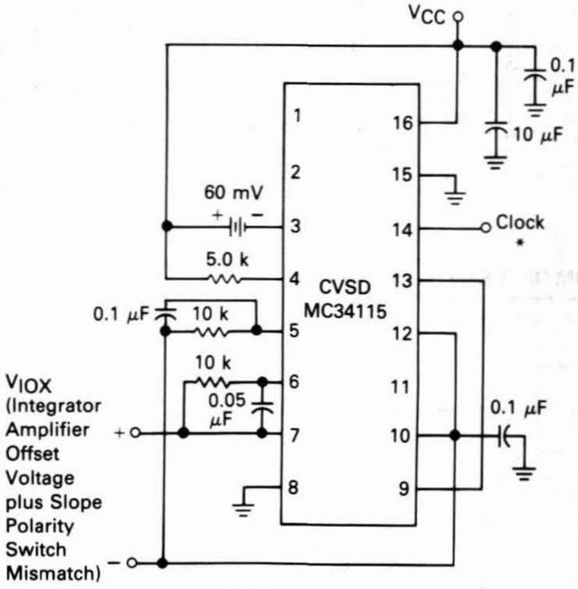

VCC
0.1 μF
10 μF
0.1 μF
10 k
I5
10 k
I6
0.05 μF
+
−
(Integrator Amplifier Offset Voltage)
CVSD
MC34115
0.1 μF
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

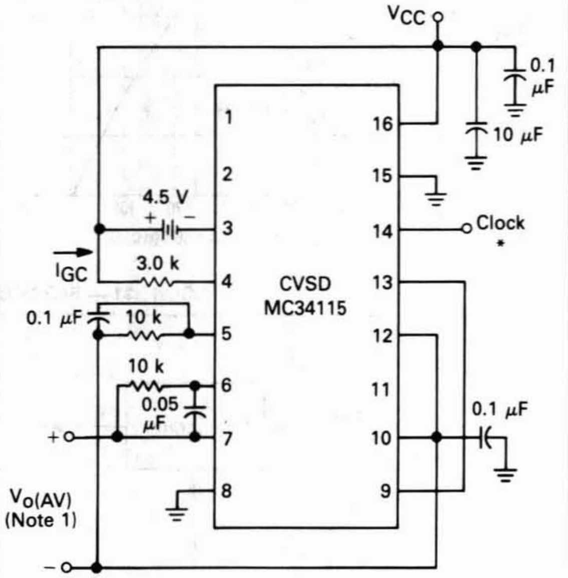
**FIGURE 5 — V/I CONVERTER OFFSET VOLTAGE, $V_{IO}$ and $V_{IOX}$**


VCC
0.1 μF
10 μF
60 mV
5.0 k
0.1 μF
10 k
10 k
0.05 μF
VIOX
(Integrator Amplifier Offset Voltage plus Slope Polarity Switch Mismatch)
+
−
CVSD
MC34115
Clock
*
0.1 μF
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

*Clock Frequency = 16 kHz

Note: $V_{IOX}$ is the average voltage of the triangular waveform observed at the measurement points.

**FIGURE 6 — DYNAMIC INTEGRATING CURRENT MATCH**


VCC
0.1 μF
10 μF
4.5 V
IGC
3.0 k
0.1 μF
10 k
10 k
0.05 μF
+
−
VO(AV)
(Note 1)
CVSD
MC34115
Clock
*
0.1 μF
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

*Clock Frequency = 16 kHz

Notes: 1. $V_{O(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with $I_{GC}$ = 1.5 mA.

2. See Note 3 of the Electrical Characteristics, Page 3.

## TYPICAL PERFORMANCE CURVES

**FIGURE 7 — TYPICAL $I_{Int}$ versus $I_{GC}$ (Mean ± 2σ)**

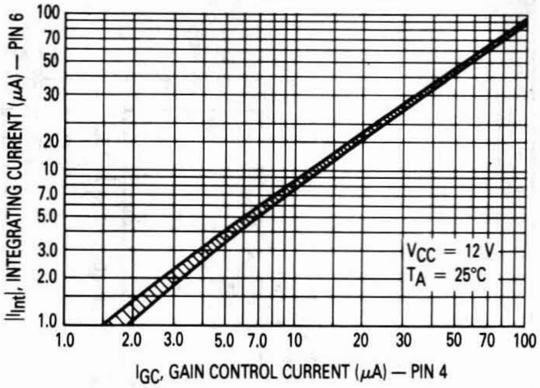


**FIGURE 8 — NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus $V_{CC}$**

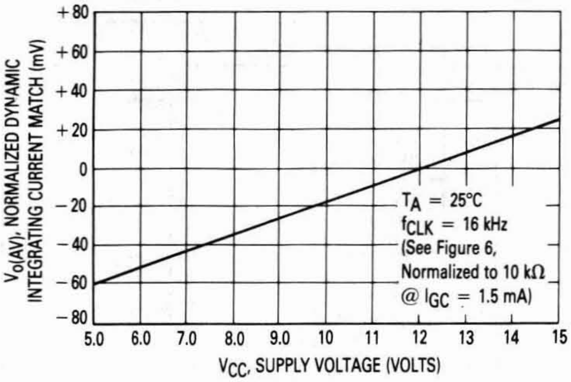


**FIGURE 9 — NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY**

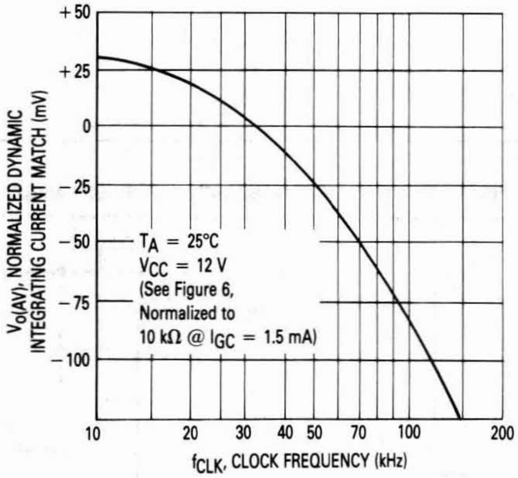


**FIGURE 10 — DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY**

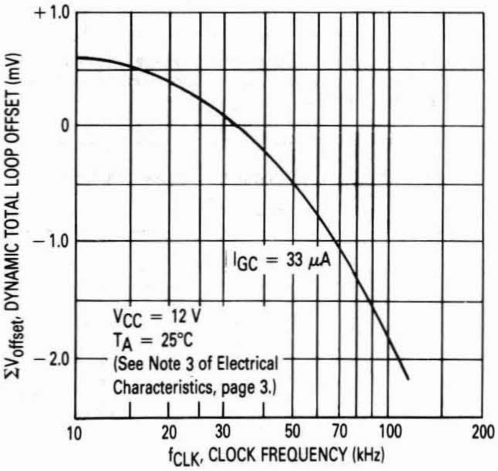


**FIGURE 11 — BLOCK DIAGRAM OF THE CVSD ENCODER**

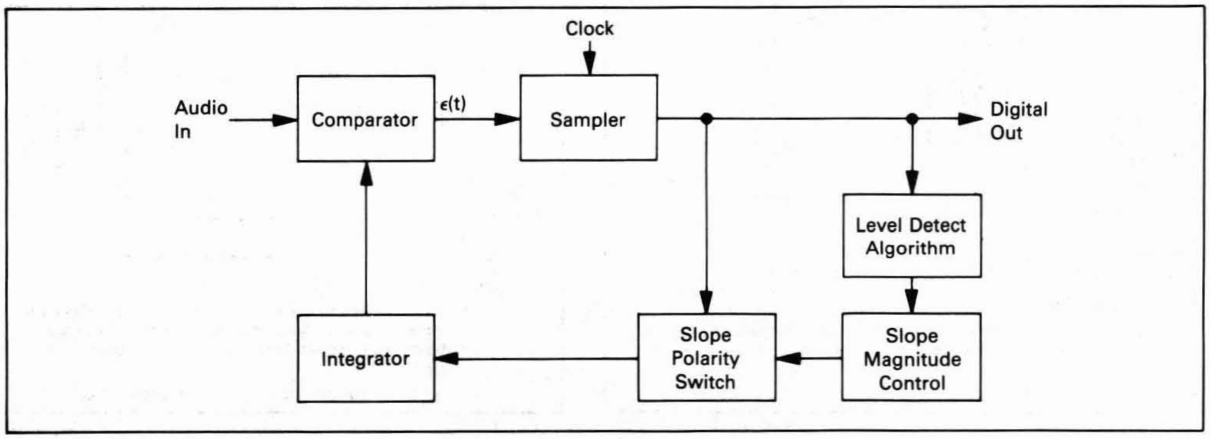

Clock
Audio In
Comparator
ε(t)
Sampler
Digital Out
Level Detect Algorithm
Slope Magnitude Control
Slope Polarity Switch
Integrator

FIGURE 12 — CVSD WAVEFORMS

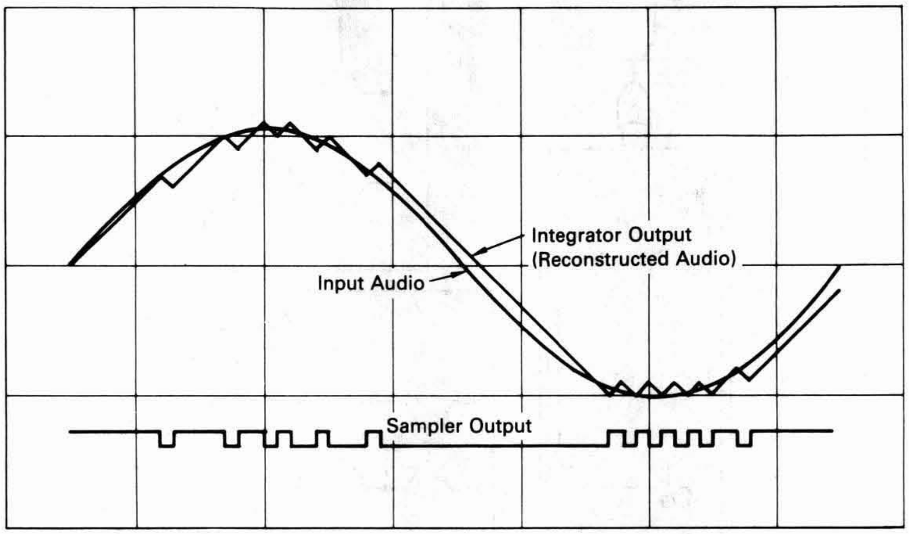
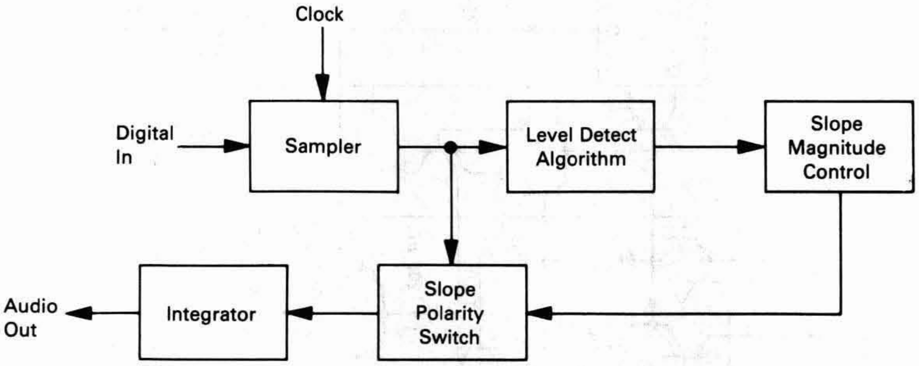
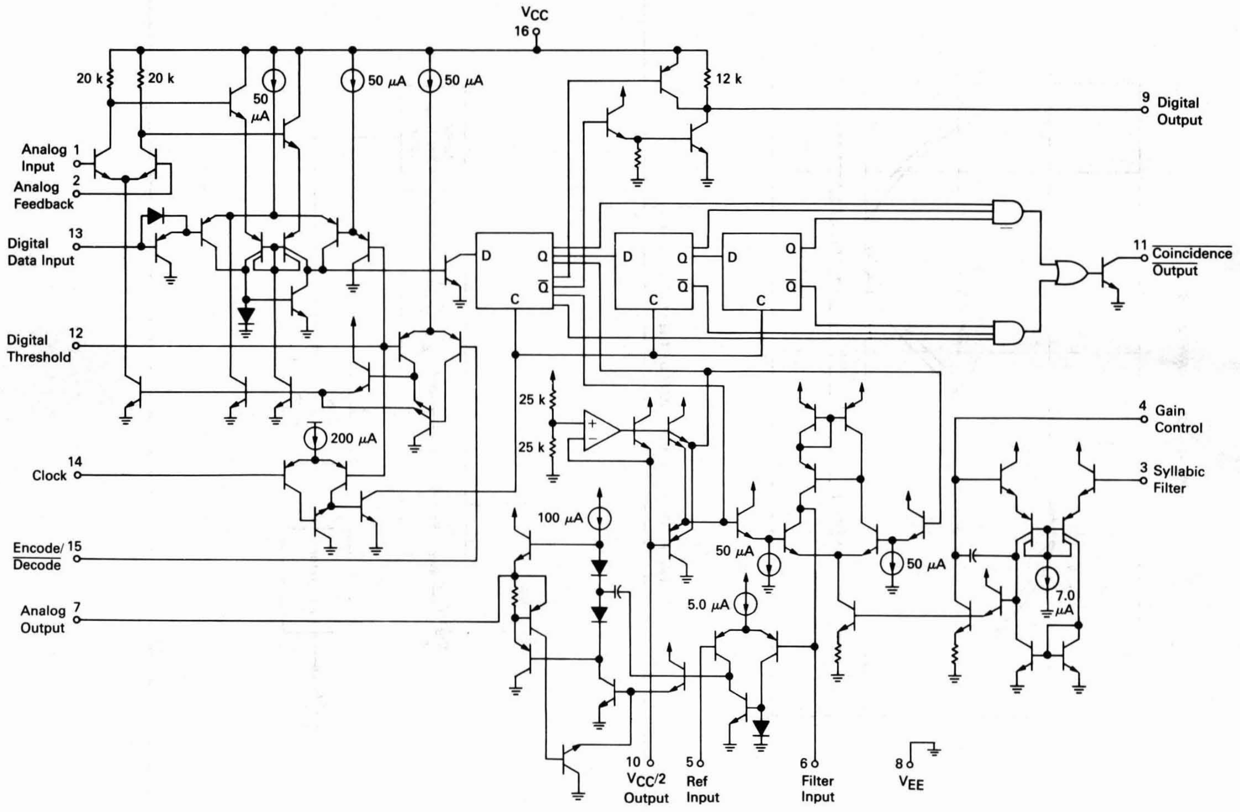


FIGURE 13 — BLOCK DIAGRAM OF THE CVSD DECODER


Clock
Digital In
Sampler
Level Detect Algorithm
Slope Magnitude Control
Audio Out
Integrator
Slope Polarity Switch

## CVSD CIRCUIT SCHEMATIC


VCC
16
20 k
20 k
50 µA
50 µA
50 µA
12 k
9 Digital Output
Analog Input 1
Analog Feedback 2
Digital Data Input 13
D Q Q̄ C
D Q Q̄ C
D Q Q̄ C
11 Coincidence Output
Digital Threshold 12
200 µA
25 k
25 k
4 Gain Control
3 Syllabic Filter
Clock 14
Encode/Decode 15
100 µA
50 µA
50 µA
5.0 µA
7.0 µA
Analog Output 7
10 VCC/2 Output
5 Ref Input
6 Filter Input
8 VEE

## CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

### The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the intregrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

### The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 bits long. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

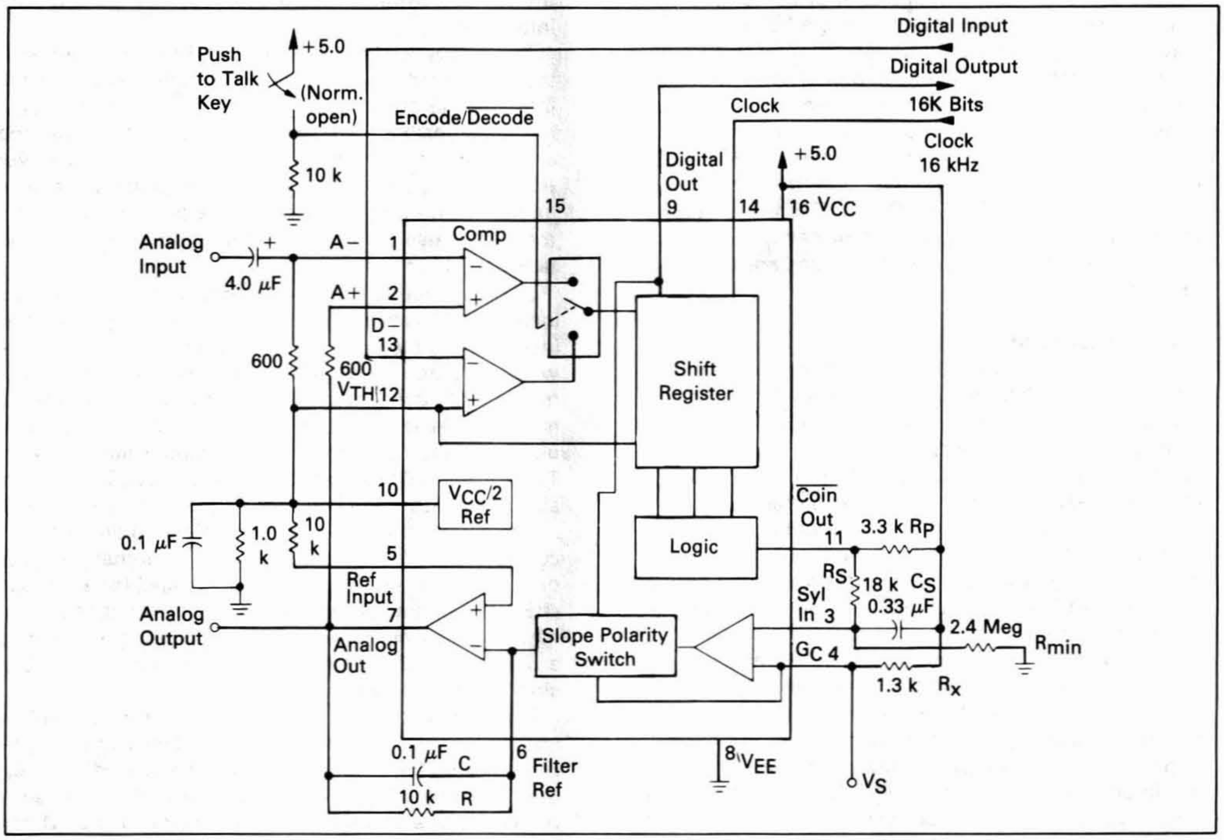
The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communications requirements.

FIGURE 14 — 16 kHz SIMPLEX VOICE CODEC
(Using MC34115, Single Pole Companding and Single Integration)


Push
to Talk
Key
+5.0
(Norm.
open)
Encode/$\overline{\text{Decode}}$
Digital Input
Digital Output
Clock
16K Bits
Clock
16 kHz
10 k
Digital
Out
9
14
15
+5.0
16 $V_{CC}$
Analog
Input
+
4.0 μF
A−
1
A+
2
Comp
D−
13
600
600
$V_{TH}$ 12
Shift
Register
10
$V_{CC}/2$
Ref
0.1 μF
1.0
k
10
k
5
Logic
$\overline{\text{Coin}}$
Out
11
3.3 k $R_P$
$R_S$
18 k
$C_S$
0.33 μF
Syl
In 3
2.4 Meg
$R_{min}$
Analog
Output
Ref
Input
7
Analog
Out
Slope Polarity
Switch
$G_C$ 4
1.3 k
$R_x$
0.1 μF
C
6
Filter
Ref
10 k
R
8 $V_{EE}$
$V_S$

## APPLICATIONS INFORMATION

### CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC34115 is shown in Figure 14. This IC is a general purpose CVSD building block which allow the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC34115. There are six design considerations involved in designing the basic CVSD building block into a specific codec application.

These are listed below:

1. Selection of clock rate
2. Selection of loop gain
3. Selection of minimum step size
4. Design of integration filter transfer function
5. Design of syllabic filter transfer function
6. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 4 and 5 are reduced to their simplest form. They syllabic and integration filters are both single pole networks. The selection of items 1 through 3 govern the codec performance.

## CVSD DESIGN CONSIDERATIONS (continued)

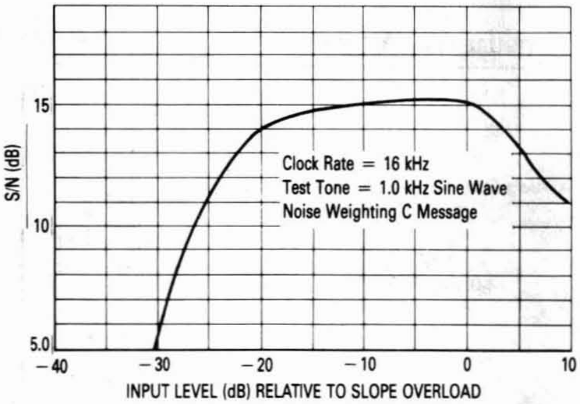
### Layout Considerations

Care should be exercised to isolate all digital signal paths (Pins 9, 11, 13, and 14) from analog signal paths (Pins 1–7 and 10) in order to achieve proper idle channel performance.

### Clock Rate

With minor modifications the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4-wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above.

FIGURE 15 — SIGNAL-TO-NOISE PERFORMANCE OF MC34115 WITH SINGLE INTEGRATION, SINGLE-POLE AND COMPANDING AT 16K BITS — TYPICAL



### Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor $R_X$. $R_X$ must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on Pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R = 10\ k\Omega,\ C = 0.1\ \mu F$$

$$\frac{V_O}{I_i} = \frac{1}{C(S + 1/RC)} \equiv \frac{K}{S + \omega_O}$$

$$\omega_O = 2\pi f$$

$$10^3 = \omega_O = 2\pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single-pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_O}{R} + C\frac{dV_O}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ V}{*2(10\ k\Omega)} + \frac{0.1\ \mu F(1.1)}{0.125\ ms} = 0.935\ mA$$

*The maximum voltage across R when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_x = 0.25(V_{CC})\frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

### Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one-zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC34115 is tested to ensure that a 20 mVp-p mimimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one-zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1-0 pattern.

## CVSD DESIGN CONSIDERATIONS (continued)

To set the idle channel step size, the value of $R_{min}$ must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor ($C_S$) would decay to zero. However, the voltage divider of $R_S$ and $R_{min}$ (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R} + C\frac{dV_o}{dt}$$

For values of $V_o$ near $V_{CC}/2$ the $V_o/R$ term is negligible; thus

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where $\Delta T$ is the clock period and $\Delta V_o$ is the desired peak-to-peak value of the idle output. For a 16K-bit system using the circuit in Figure 14

$$I_i = \frac{0.1\,\mu F\ 20\ mV}{62.5\,\mu s} = 32\,\mu A$$

The voltage on $C_S$ which produces a 32 µA current is determined by the value of $R_x$.

$$I_iR_x = V_{S}min;\ \text{for } 32\,\mu A,\ V_{S}min = 41.6\ mV$$

In Figure 14 $R_S$ is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of $R_S$ and $R_{min}$ must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_{Smin} \quad R_{min} \approx 2.4\ M\Omega$$

Having established these three parameters — clock rate, loop gain and minimum step size — the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

## INCREASING CVSD PERFORMANCE

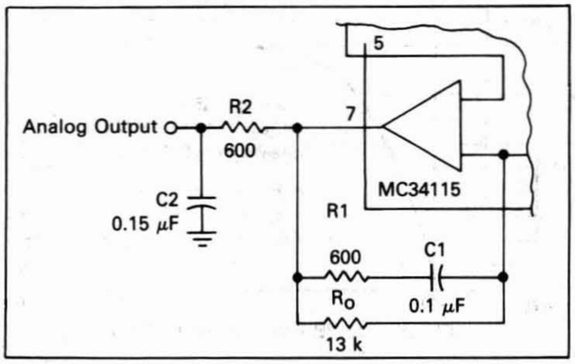
**Integration Filter Design**

The circuit in Figure 14 uses a single-pole integration network formed with a 0.1 µF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1 or 2 dB by using a two-pole integration network. The improved circuit is shown.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low-pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2 kHz and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low-pass filter which breaks at about 2.5 kHz.) The two-pole network in Figure 16 has a transfer function of:

$$\frac{V_o}{I_i} = \frac{R_OR_1\left(S + \frac{1}{R_1C_1}\right)}{R_2C_2(R_O + R_1)\left(S + \frac{1}{(R_O + R_1)C_1}\right)S + \left(\frac{1}{R_2C_2}\right)}$$

FIGURE 16 — IMPROVED FILTER CONFIGURATION



These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on Pin 1.

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network affects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_o}{R_O} + \left(\frac{R_2C_2}{R_O} + \frac{R_1C_1}{R_O} + C_1\right)\frac{\Delta V_o}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_O}\right)\frac{\Delta V_o^2}{\Delta T^2}$$

## INCREASING CVSD PERFORMANCE (continued)

The calculation of desired gain resistor $R_X$ then proceeds exactly as previously described.

**Syllabic Filter Design**

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across $C_S/V_{CC}$.

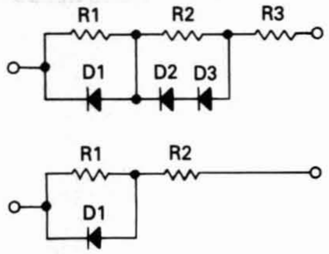
The S/N performance may be improved by modifying the voltage to current transformation produced by $R_X$. If different portions of the total $R_X$ are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to Pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of $R_X$ in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor-diode networks are shown in Figure 17.

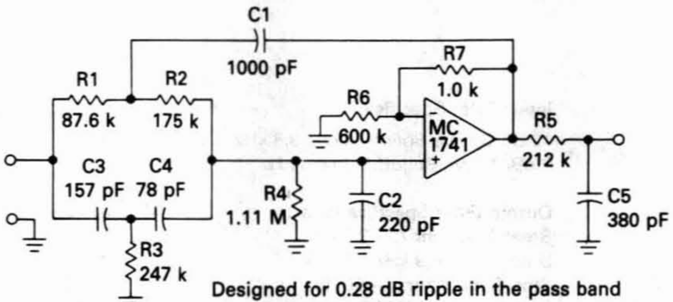
FIGURE 17 — RESISTOR-DIODE NETWORKS



**Output Low Pass Filter**

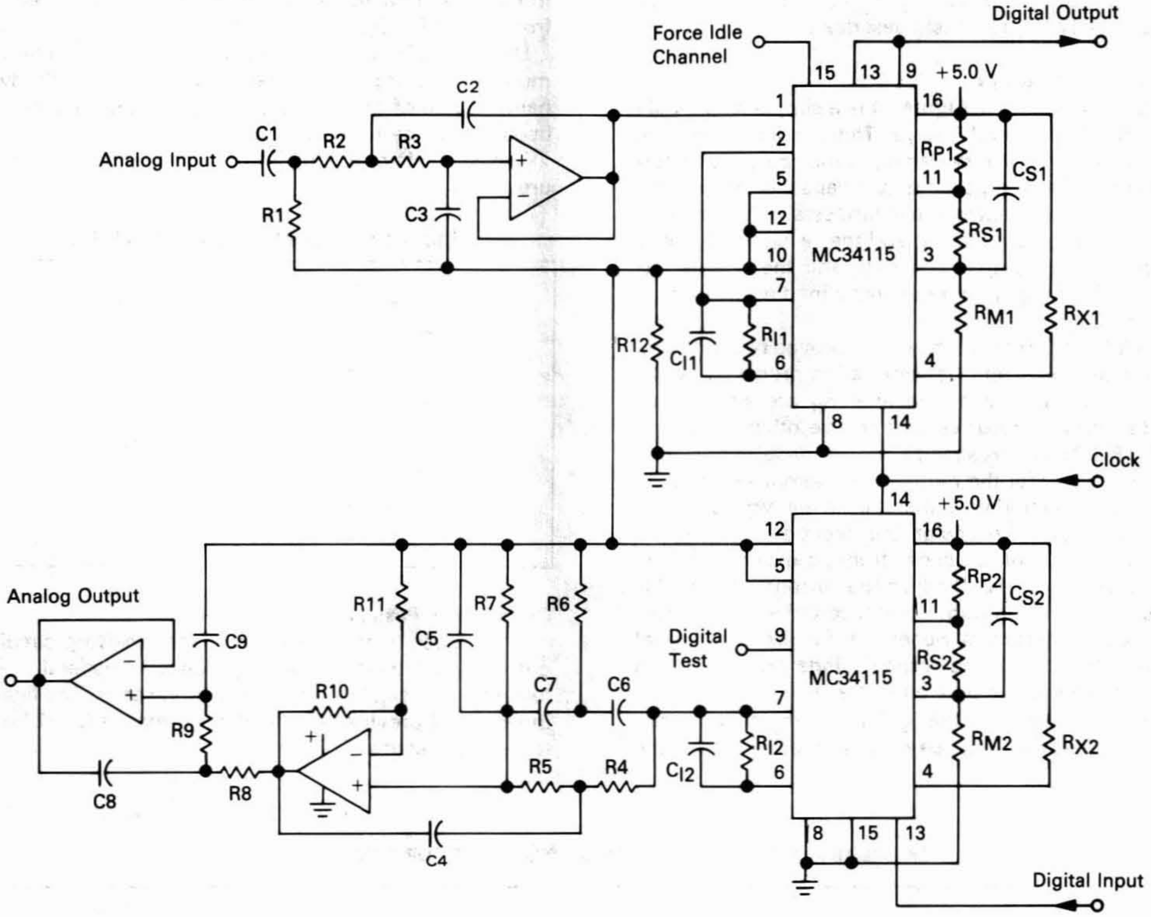
A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 18 provides excellent performance for 12 kHz to 40 kHz systems.

FIGURE 18 — HIGH PERFORMANCE ELLIPTIC FILTER FOR CVSD OUTPUT



Designed for 0.28 dB ripple in the pass band
$\omega_n$ = 3.0 kHz
$\omega_s$ = ≅ 6.0 kHz
AdB at $\omega_s$ and above 29.5 dB

**FIGURE 19 — FULL DUPLEX/16K BIT CVSD VOICE CODEC USING MC34115 AND MC3503/6 OP AMP**


Force Idle
Channel
Digital Output
15
13
9
+5.0 V
C2
1
16
C1
R2
R3
Analog Input
2
$R_{P1}$
$C_{S1}$
5
11
R1
C3
12
$R_{S1}$
10
MC34115
3
7
$R_{M1}$
$R_{X1}$
R12
$C_{I1}$
$R_{I1}$
6
4
8
14
Clock
14
+5.0 V
12
16
5
$R_{P2}$
$C_{S2}$
Analog Output
R11
R7
R6
11
C9
C5
Digital
Test
9
$R_{S2}$
MC34115
3
R10
C7
C6
7
R9
$R_{I2}$
$R_{M2}$
$R_{X2}$
R5
R4
$C_{I2}$
6
4
C8
R8
8
15
13
C4
Digital Input

**Codec Components**

$R_{X1}$, $R_{X2}$ — 3.3 kΩ
$R_{P1}$, $R_{P2}$ — 3.3 kΩ
$R_{S1}$, $R_{S2}$ — 100 kΩ
$R_{I1}$, $R_{I2}$ — 20 kΩ
$R_{12}$ — 1 kΩ
$R_{M1}$, $R_{M2}$ — 10 MΩ
Minimum step size = 20 mV
$C_{S1}$, $C_{S2}$ — 0.05 μF
$C_{I1}$, $C_{I2}$ — 0.05 μF
2 MC34115
1 MC3403 (or MC3406)

Note: All Res. 5%
All Cap. 5%

**Input Filter Specifications**

12 dB/Octave Rolloff above 3.3 kHz
6 dB/Octave Rolloff below 50 Hz

**Output Filter Specifications**

Break Frequency — 3.3 kHz
Stop Band — 9 kHz
Stop Band Atten. — 50 dB
Rolloff — >40 dB/Octave

**Filter Components**

R1 — 965 Ω
R2 — 72 kΩ
R3 — 72 kΩ
R4 — 63.46 kΩ
R5 — 127 kΩ
R6 — 365.5 kΩ
R7 — 1.645 MΩ
R8 — 72 kΩ
R9 — 72 kΩ
R10 — 29.5 kΩ
R11 — 72 kΩ

C1 — 3.3 μF
C2 — 837 pF
C3 — 536 pF
C4 — 1000 pF
C5 — 222 pF
C6 — 77 pF
C7 — 38 pF
C8 — 837 pF
C9 — 536 pF

Note: All Res. 0.1% to 1%.
All Cap. 1.0%

MOTOROLA

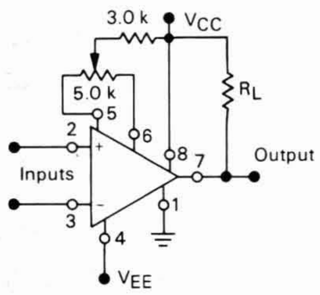
# LM111
# LM211
# LM311

## HIGHLY FLEXIBLE VOLTAGE COMPARATORS

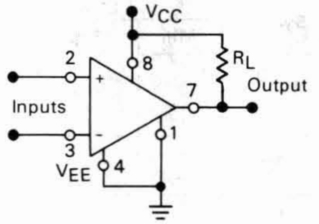
The ability to operate from a single power supply of 5.0 to 30 volts or ±15 volt split supplies, as commonly used with operational amplifiers, makes the LM111/LM211/LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the $V_{CC}$ or the $V_{EE}$ supply. This flexibility makes it possible to drive DTL, RTL, TTL, or MOS logic. The output can also switch voltages to 50 volts at currents to 50 mA. Thus the LM111/LM211/LM311 can be used to drive relays, lamps or solenoids.

### TYPICAL COMPARATOR DESIGN CONFIGURATIONS

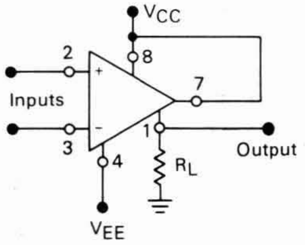
**Split Power-Supply with Offset Balance**


3.0 k
VCC
5.0 k
RL
5
2
6
8
7
Output
Inputs
3
1
4
VEE

**Single Supply**

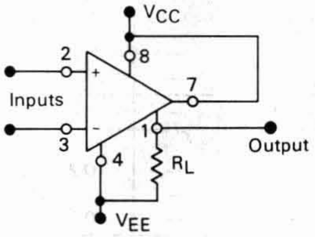

VCC
2
8
RL
7
Output
Inputs
1
3
VEE
4

**Ground-Referred Load**


VCC
2
8
7
Inputs
1
Output
3
4
RL
VEE

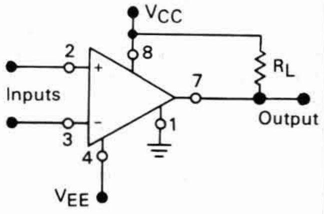
Input polarity is reversed when Gnd pin is used as an output.

**Load Referred to Negative Supply**

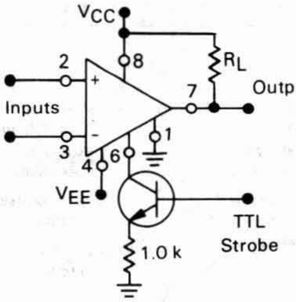

VCC
2
8
7
Inputs
1
Output
3
4
RL
VEE

Input polarity is reversed when Gnd pin is used as an output.

**Load Referred to Positive Supply**


VCC
2
8
RL
7
Inputs
Output
3
1
4
VEE

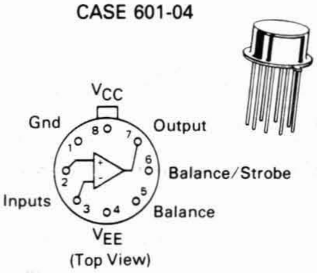
**Strobe Capability**

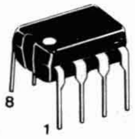

VCC
2
8
RL
7
Output
Inputs
1
3
4
6
VEE
TTL
Strobe
1.0 k

## HIGH PERFORMANCE VOLTAGE COMPARATORS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

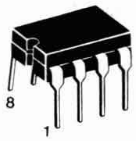
**H SUFFIX**
METAL PACKAGE
CASE 601-04


VCC
Gnd
Output
1
8
7
6
2
Balance/Strobe
Inputs
3
4
5
Balance
VEE
(Top View)

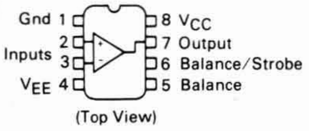


**N SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(LM311 Only)

**J-8 SUFFIX**
CERAMIC PACKAGE
CASE 693-02



**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8
(LM211/LM311 Only)


Gnd 1
8 VCC
Inputs 2
7 Output
3
6 Balance/Strobe
VEE 4
5 Balance
(Top View)

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| LM111H<br>LM111J-8 | −55°C to +125°C | Metal Can<br>Ceramic DIP |
| LM211D<br>LM211H<br>LM211J-8 | −25°C to +85°C | SO-8<br>Metal Can<br>Ceramic DIP |
| LM311D<br>LM311J-8<br>LM311N | 0°C to +70°C | SO-8<br>Ceramic DIP<br>Plastic DIP |

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value |  | Unit |
|---|---|---|---|---|
|  |  | LM111<br>LM211 | LM311 |  |
| Total Supply Voltage | $V_{CC} + \lvert V_{EE} \rvert$ | 36 | 36 | Vdc |
| Output to Negative Supply Voltage | $V_O - V_{EE}$ | 50 | 40 | Vdc |
| Ground to Negative Supply Voltage | $V_{EE}$ | 30 | 30 | Vdc |
| Input Differential Voltage | $V_{ID}$ | ±30 | ±30 | Vdc |
| Input Voltage (Note 2) | $V_{in}$ | ±15 | ±15 | Vdc |
| Voltage at Strobe Pin | — | $V_{CC}$ to $V_{CC}$-5 | $V_{CC}$ to $V_{CC}$-5 | Vdc |
| Power Dissipation and Thermal Characteristics |  |  |  |  |
| Metal Package | $P_D$ | 680 |  | mW |
| Derate above $T_A$ = +25°C | $1//\theta_{JA}$ | 5.5 |  | mW/°C |
| Plastic and Ceramic Dual In-Line Packages | $P_D$ | 625 |  | mW |
| Derate above $T_A$ = +25°C | $1/\theta_{JA}$ | 5.0 |  | mW/°C |
| Operating Ambient Temperature Range | $T_A$ |  |  | °C |
| LM111 |  | -55 to +125 | — |  |
| LM211 |  | -25 to +85 | — |  |
| LM311 |  | — | 0 to +70 |  |
| Operating Junction Temperature | $T_{J(max)}$ | +150 | +150 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 V, $V_{EE}$ = −15 V, $T_A$ = +25°C unless otherwise noted [Note 1].)

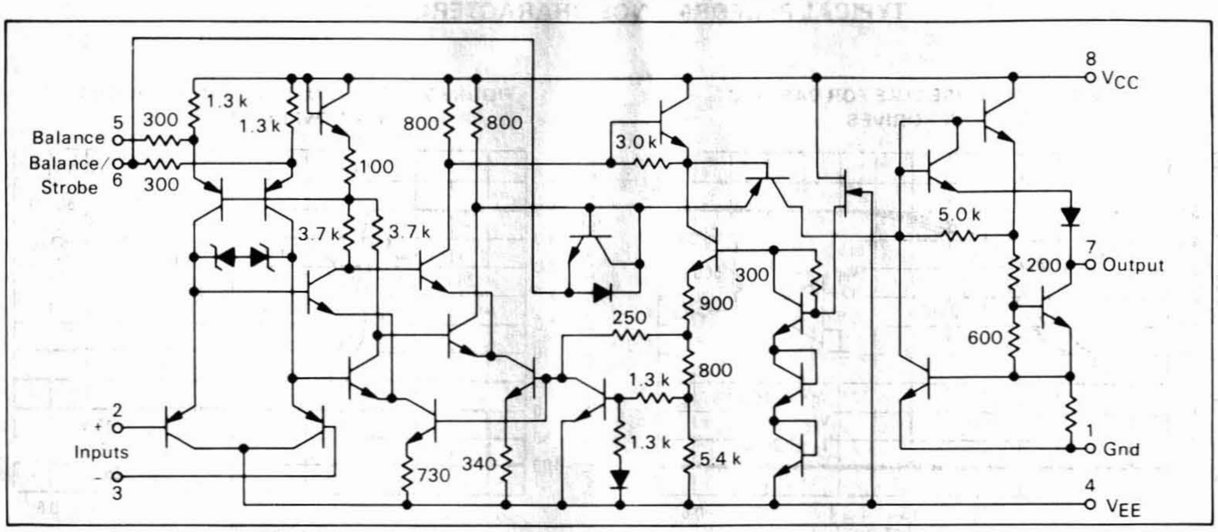
| Characteristic | Symbol | LM111<br>LM211 |  |  | LM311 |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage (Note 3) | $V_{IO}$ |  |  |  |  |  |  | mV |
| $R_S \leq 50$ kΩ, $T_A$ = +25°C |  | — | 0.7 | 3.0 | — | 2.0 | 7.5 |  |
| $R_S \leq 50$ kΩ, $T_{low} \leq T_A \leq T_{high}$* |  | — | — | 4.0 | — | — | 10 |  |
| Input Offset Current (Note 3) $T_A$ = +25°C | $I_{IO}$ | — | 1.7 | 10 | — | 1.7 | 50 | nA |
| $T_{low} \leq T_A \leq T_{high}$* |  | — | — | 20 | — | — | 70 |  |
| Input Bias Current, $T_A$ = +25°C | $I_{IB}$ | — | 45 | 100 | — | 45 | 250 | nA |
| $T_{low} \leq T_A \leq T_{high}$* |  | — | — | 150 | — | — | 300 |  |
| Voltage Gain | $A_V$ | 40 | 200 | — | 40 | 200 | — | V/mV |
| Response Time (Note 4) |  | — | 200 | — | — | 200 | — | ns |
| Saturation Voltage | $V_{OL}$ |  |  |  |  |  |  | V |
| $V_{ID} \leq -5.0$ mV, $I_O$ = 50 mA } $T_A$ = +25°C |  | — | 0.75 | 1.5 | — | — | — |  |
| $V_{ID} \leq -10$ mV, $I_O$ = 50 mA |  | — | — | — | — | 0.75 | 1.5 |  |
| $V_{CC} \geq 4.5$ V, $V_{EE}$ = 0, $T_{low} \leq T_A \leq T_{high}$* |  |  |  |  |  |  |  |  |
| $V_{ID} \leq -6.0$ mV, $I_{sink} \leq 8.0$ mA |  | — | 0.23 | 0.4 | — | — | — |  |
| $V_{ID} \leq -10$ mV, $I_{sink} \leq 8.0$ mA |  | — | — | — | — | 0.23 | 0.4 |  |
| Strobe "On" Current (Note 5) | $I_S$ | — | 3.0 | — | — | 3.0 | — | mA |
| Output Leakage Current |  |  |  |  |  |  |  |  |
| $V_{ID} \geq 5.0$ mV, $V_O$ = 35 V } $T_A$ = +25°C |  | — | 0.2 | 10 | — | — | — | nA |
| $V_{ID} \geq 10$ mV, $V_O$ = 35 V } $I_{strobe}$ = 3.0 mA |  | — | — | — | — | 0.2 | 50 | nA |
| $V_{ID} \geq 5.0$ mV, $V_O$ = 35 V, $T_{low} \leq T_A \leq T_{high}$* |  | — | 0.1 | 0.5 | — | — | — | µA |
| Input Voltage Range ($T_{low} \leq T_A \leq T_{high}$*) | $V_{IR}$ | -14.5 | -14.7 to 13.8 | 13.0 | -14.5 | -14.7 to 13.8 | 13.0 | V |
| Positive Supply Current | $I_{CC}$ | — | +2.4 | +6.0 | — | +2.4 | +7.5 | mA |
| Negative Supply Current | $I_{EE}$ | — | -1.3 | -5.0 | — | -1.3 | -5.0 | mA |

NOTES:

| | |
|---|---|
| * $T_{low}$ = −55°C for LM111 | $T_{high}$ = +125°C for LM111 |
| = −25°C for LM211 | = +85°C for LM211 |
| = 0°C for LM311 | = +70°C for LM311 |

1. Offset voltage, offset current and bias current specifications apply for a supply voltage range from a single 5.0 volt supply up to ± 15 volt supplies.
2. This rating applies for ±15 volt supplies. The positive input voltage limit is 30 volts above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 volts below the positive supply, whichever is less.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.
4. The response time specified is for a 100 mV input step with 5.0 mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3.0 to 5.0 mA.

FIGURE 1 — CIRCUIT SCHEMATIC


8
$V_{CC}$
5
Balance
Balance/
Strobe
6
300
300
1.3 k
1.3 k
800
800
100
3.0 k
3.7 k
3.7 k
5.0 k
7
200
Output
300
900
250
600
800
1.3 k
1.3 k
5.4 k
730
340
2
+
Inputs
−
3
1
Gnd
4
$V_{EE}$

## TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 2 — INPUT BIAS CURRENT versus TEMPERATURE

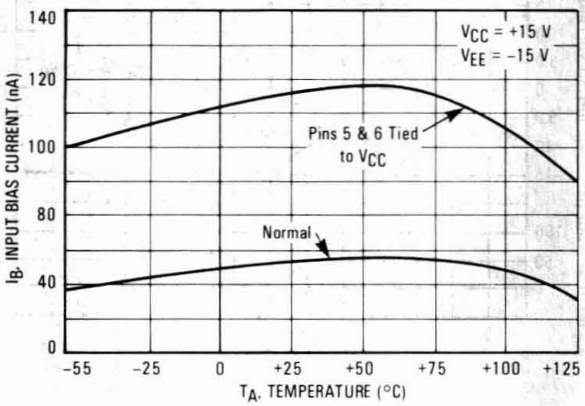


FIGURE 3 — INPUT OFFSET CURRENT versus TEMPERATURE

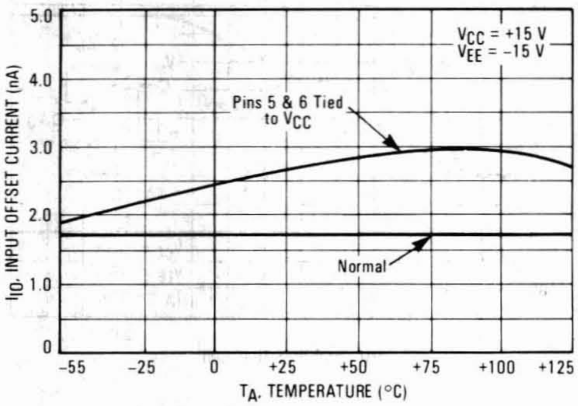


FIGURE 4 — INPUT BIAS CURRENT versus DIFFERENTIAL INPUT VOLTAGE

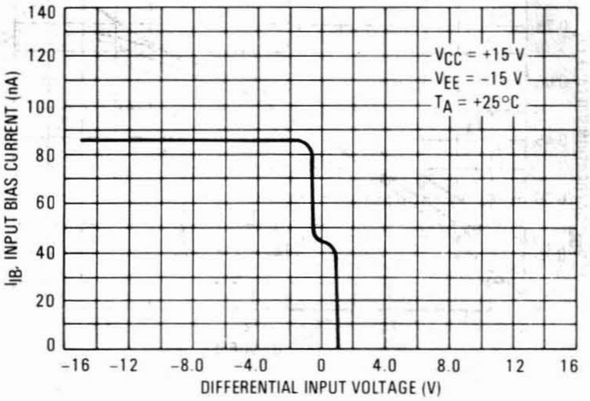
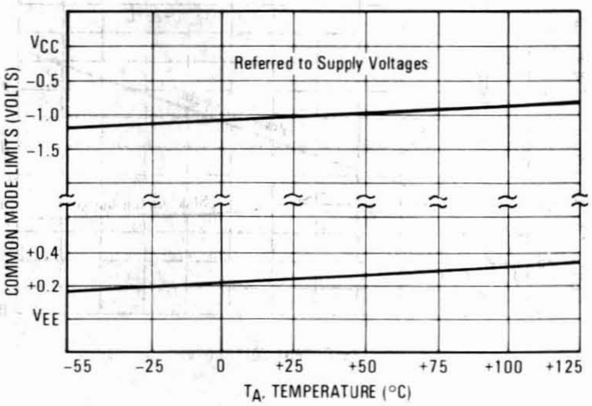


FIGURE 5 — COMMON MODE LIMITS versus TEMPERATURE



## TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 6 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

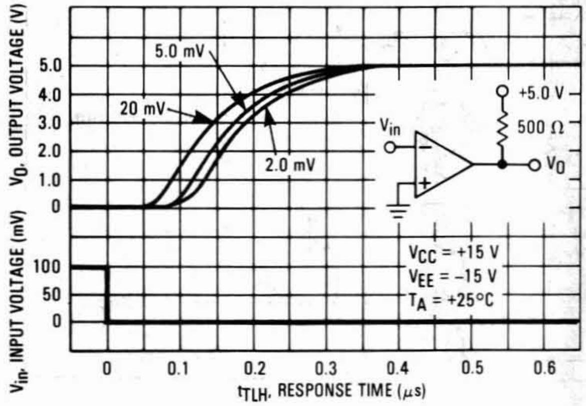


FIGURE 7 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

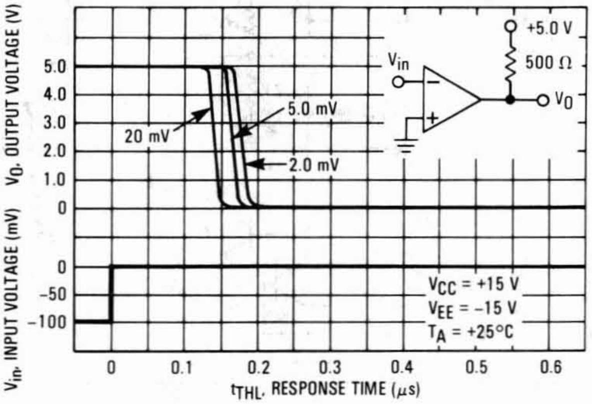


FIGURE 8 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

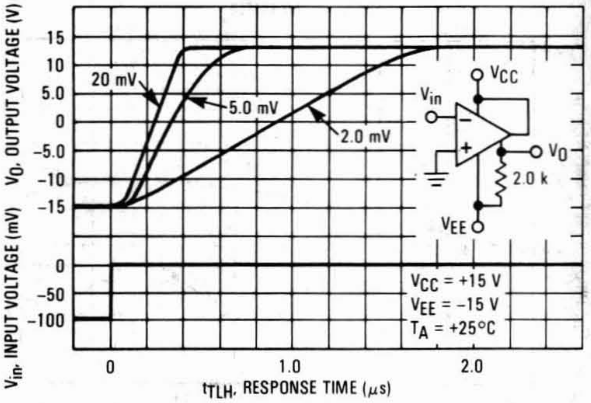


FIGURE 9 — RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

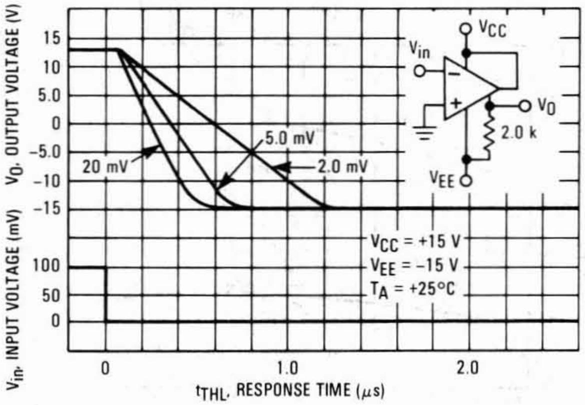


FIGURE 10 — OUTPUT SHORT CIRCUIT CURRENT CHARACTERISTICS AND POWER DISSIPATION

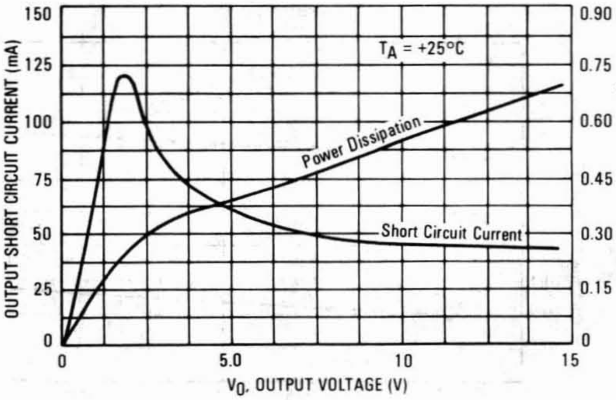
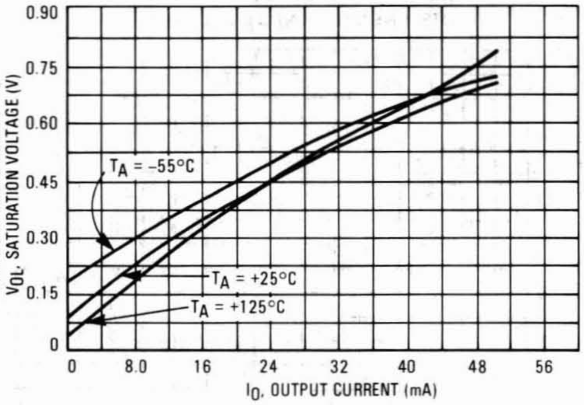


FIGURE 11 — OUTPUT SATURATION VOLTAGE versus OUTPUT CURRENT



## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

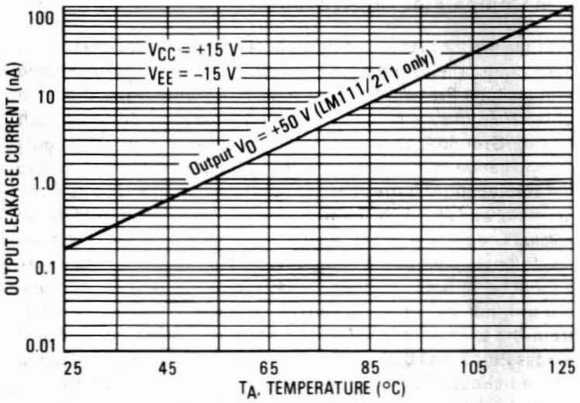


FIGURE 12 — OUTPUT LEAKAGE CURRENT versus TEMPERATURE

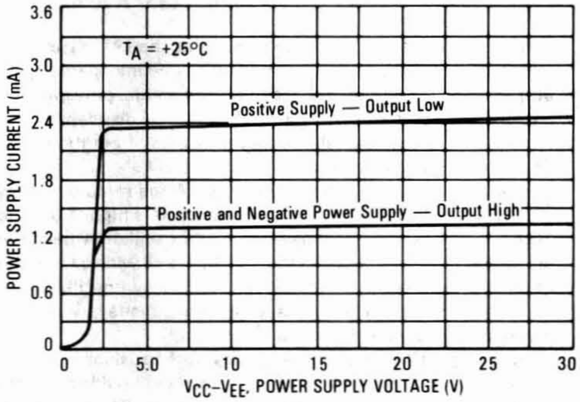


FIGURE 13 — POWER SUPPLY CURRENT versus SUPPLY VOLTAGE

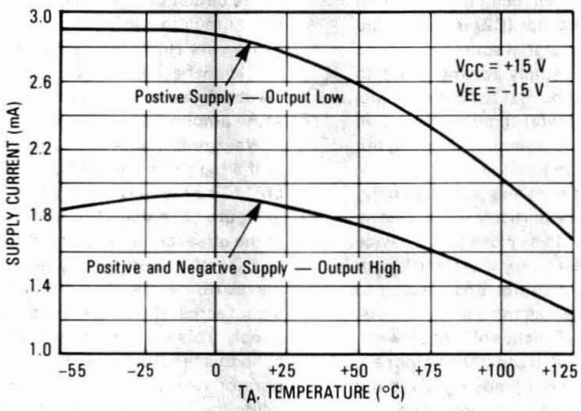


FIGURE 14 — POWER SUPPLY CURRENT versus TEMPERATURE

## APPLICATIONS INFORMATION

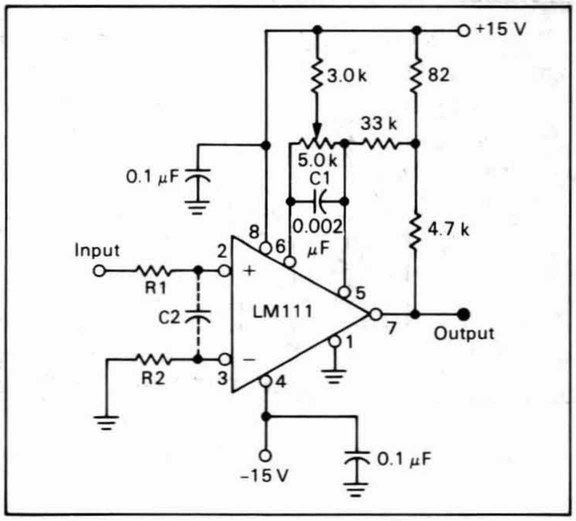

+15 V
3.0 k
82
33 k
5.0 k
C1
0.002 μF
4.7 k
0.1 μF
Input
R1
C2
R2
2
3
8
6
5
7
1
4
LM111
Output
−15 V
0.1 μF

FIGURE 15 — IMPROVED METHOD OF ADDING HYSTERESIS WITHOUT APPLYING POSITIVE FEEDBACK TO THE INPUTS

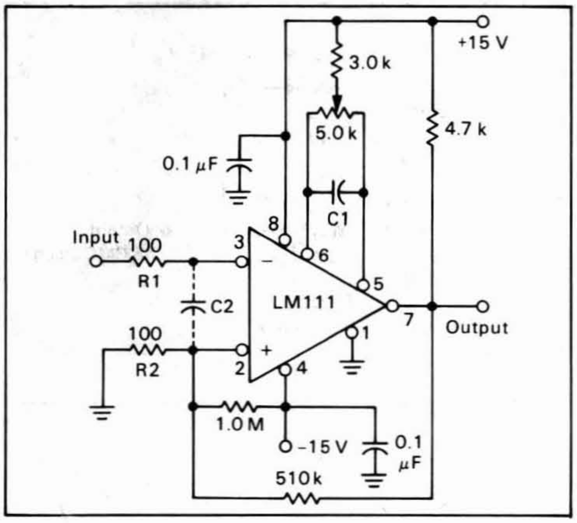

+15 V
3.0 k
5.0 k
4.7 k
0.1 μF
C1
Input
100
R1
C2
100
R2
8
3
6
5
2
4
1
7
LM111
Output
1.0 M
−15 V
0.1 μF
510 k

FIGURE 16 — CONVENTIONAL TECHNIQUE FOR ADDING HYSTERESIS

## APPLICATIONS INFORMATION

### Techniques for Avoiding Oscillations in Comparator Applications

When a high-speed comparator such as the LM111 is used with high-speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1.0 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 15.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μF capacitor (C1) between Pins 5 and 6 will minimize the susceptibility to ac coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 15.

Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor (C2) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R2 of the same value, both for dc and for dynamic (ac) considerations. Carbon, tin-oxide, and metal-film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen. Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any fast high-level signals (such as the output). If Pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located no more than a few inches away from the LM111, and a 0.01 μF capacitor should be installed across Pins 5 and 6. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between Pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111.

A standard procedure is to add hysteresis to a comparator to prevent oscillation, and to avoid excessive noise on the output. In the circuit of Figure 16, the feedback resistor of 510 kΩ from the output to the positive input will cause about 3.0 mV of hysteresis. However, if R2 is larger than 100 Ω, such as 50 kΩ, it would not be practical to simply increase the value of the positive feedback resistor proportionally above 510 kΩ to maintain the same amount of hysteresis.

When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of Figure 15 is ideal. The positive feedback is applied to Pin 5 (one of the offset adjustment pins). This will be sufficient to cause 1.0 to 2.0 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82 Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at Pin 5, so this feedback does not add to the offset voltage of the comparator. As much as 8.0 mV of offset voltage can be trimmed out, using the 5.0 kΩ pot and 3.0 kΩ resistor as shown.

FIGURE 17 — ZERO-CROSSING DETECTOR DRIVING CMOS LOGIC

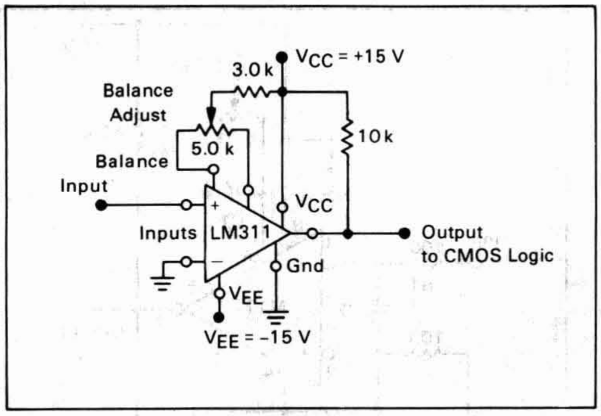
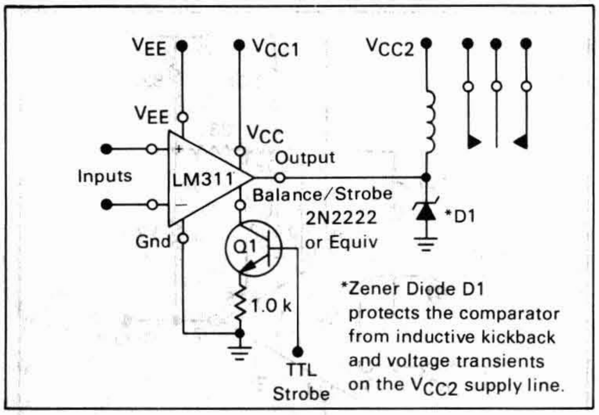


FIGURE 18 — RELAY DRIVER WITH STROBE CAPABILITY



*Zener Diode D1 protects the comparator from inductive kickback and voltage transients on the $V_{CC2}$ supply line.

**MOTOROLA**

# LM139, A
# LM239, A LM2901
# LM339, A MC3302

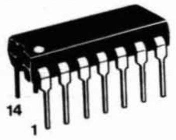
## QUAD SINGLE-SUPPLY COMPARATORS

These comparators are designed for use in level detection, low-level sensing and memory applications in Consumer Automotive and Industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current — 25 nA (Typ)
- Low Input Offset Current — ±5.0 nA (Typ)
- Low Input Offset Voltage — ±1.0 mV (Typ LM139A Series)
- Input Common-Mode Voltage Range to Gnd
- Low Output Saturation Voltage — 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible

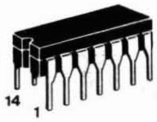
## QUAD COMPARATORS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA

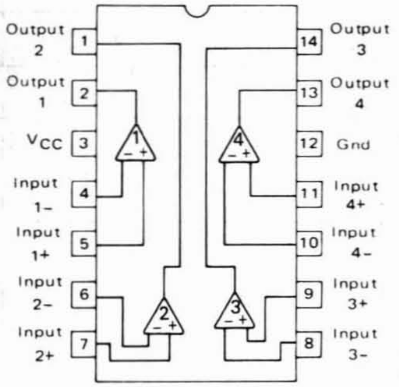


**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14

### MAXIMUM RATINGS

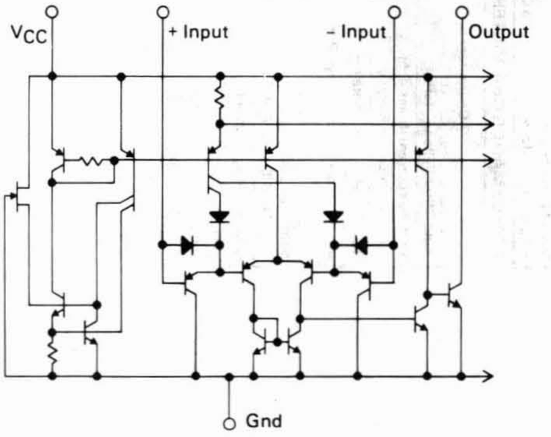
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage LM139, A/LM239, A/<br>LM339A/LM2901<br>MC3302 | $V_{CC}$ | +36 or ±18<br><br>+30 or ±15 | Vdc |
| Input Differential Voltage Range<br>LM139, A/LM239, A/LM339, A/LM2901<br>MC3302 | $V_{IDR}$ | <br>36<br>30 | Vdc |
| Input Common Mode Voltage Range | $V_{ICR}$ | -0.3 to $V_{CC}$ | Vdc |
| Output Short-Circuit to Gnd (Note 1) | $I_{SC}$ | Continuous | |
| Input Current ($V_{in} < -0.3$ Vdc) (Note 2) | $I_{in}$ | 50 | mA |
| Power Dissipation @ $T_A = 25°C$<br>Ceramic Package<br>Derate above 25°C<br>Plastic Package<br>Derate above 25°C | $P_D$ | <br>1.0<br>8.0<br>1.0<br>8.0 | <br>Watts<br>mW/°C<br>Watts<br>mW/°C |
| Operating Ambient Temperature Range<br>LM139, A<br>LM239, A<br>LM2901/MC3302<br>LM339, A | $T_A$ | <br>−55 to +125<br>−25 to +85<br>−40 to +85<br>0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**PIN CONNECTIONS**



(Top View)

FIGURE 1 — CIRCUIT SCHEMATIC (Diagram shown is for 1 comparator)



### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| LM139J, AJ | −55°C to +125°C | Ceramic DIP |
| LM239D<br>LM239J, AJ<br>LM239N, AN | −25°C to +85°C | SO-14<br>Ceramic DIP<br>Plastic DIP |
| LM339D<br>LM339J, AJ<br>LM339N, AN | 0°C to +70°C | SO-14<br>Ceramic DIP<br>Plastic DIP |
| LM2901D<br>LM2901N<br>MC3302L<br>MC3302P | −40°C to +85°C | SO-14<br>Plastic DIP<br>Ceramic DIP<br>Plastic DIP |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | LM139A | | | LM239A/339A | | | LM139 | | | LM239/339 | | | LM2901 | | | MC3302 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage (Note 4) | $V_{IO}$ | — | ±1.0 | ±2.0 | — | ±1.0 | ±2.0 | — | ±2.0 | ±5.0 | — | ±2.0 | ±5.0 | — | ±2.0 | ±7.0 | — | ±3.0 | ±20 | mVdc |
| Input Bias Current (Notes 4, 5) (Output in Linear Range) | $I_{IB}$ | — | 25 | 100 | — | 25 | 250 | — | 25 | 100 | — | 25 | 250 | — | 25 | 250 | — | 25 | 500 | nA |
| Input Offset Current (Note 4) | $I_{IO}$ | — | ±3.0 | ±25 | — | ±5.0 | ±50 | — | ±3.0 | ±25 | — | ±5.0 | ±50 | — | ±5.0 | ±50 | — | ±3.0 | ±100 | nA |
| Input Common-Mode Voltage Range (Note 7) | $V_{ICR}$ | 0 | — | $V_{CC}$ -1.5 | 0 | — | $V_{CC}$ -1.5 | 0 | — | $V_{CC}$ -1.5 | 0 | — | $V_{CC}$ -1.5 | 0 | — | $V_{CC}$ -1.5 | 0 | — | $V_{CC}$ -1.5 | V |
| Supply Current<br>$R_L$ = ∞ (For All Comparators)<br>$R_L$ = ∞, $V_{CC}$ = 30 Vdc | $I_{CC}$ | <br>—<br>— | <br>0.8<br>— | <br>2.0<br>— | <br>—<br>— | <br>0.8<br>— | <br>2.0<br>— | <br>—<br>— | <br>0.8<br>— | <br>2.0<br>— | <br>—<br>— | <br>0.8<br>— | <br>2.0<br>— | <br>—<br>— | <br>0.8<br>1.0 | <br>2.0<br>2.5 | <br>—<br>— | <br>0.8<br>— | <br>2.0<br>— | mA |
| Voltage Gain $R_L \geq 15$ kΩ, $V_{CC}$ = 15 Vdc | $A_V$ | 50 | 200 | — | 50 | 200 | — | — | 200 | — | — | 200 | — | 25 | 100 | — | 2 | 30 | — | V/mV |
| Large Signal Response Time $V_I$ = TTL Logic Swing, $V_{ref}$ = 1.4 Vdc, $V_{RL}$ = 5.0 Vdc, $R_L$ = 5.1 kΩ | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | — | ns |
| Response Time (Note 6) $V_{RL}$ = 5.0 Vdc, $R_L$ = 5.1 kΩ | — | — | 1.3 | — | — | 1.3 | — | — | 1.3 | — | — | 1.3 | — | — | 1.3 | — | — | 1.3 | — | μs |
| Output Sink Current $V_I(-) \geq +1.0$ Vdc, $V_I(+) = 0$, $V_O \leq 1.5$ Vdc | $I_{sink}$ | 6.0 | 16 | — | 6.0 | 16 | — | 6.0 | 16 | — | 6.0 | 16 | — | 6.0 | 16 | — | 6.0 | 16 | — | mA |
| Saturation Voltage $V_I(-) \geq +1.0$ Vdc, $V_I(+) = 0$, $I_{sink} \leq 4.0$ mA | $V_{sat}$ | — | 130 | 400 | — | 130 | 400 | — | 130 | 400 | — | 130 | 400 | — | 130 | 400 | — | 130 | 500 | mV |
| Output Leakage Current $V_I(+) \geq +1.0$ Vdc, $V_I(-) = 0$, $V_O$ = +5.0 Vdc | $I_{OL}$ | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | nA |

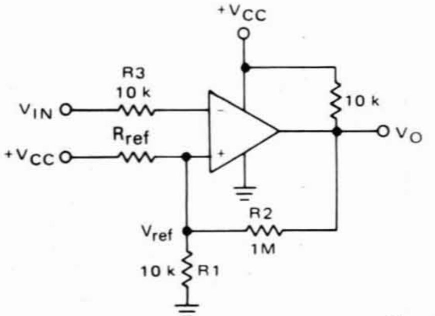
**PERFORMANCE CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $T_A$ = $T_{low}$ to $T_{high}$ [Note 3])

| Characteristic | Symbol | LM139A | | | LM239A/339A | | | LM139 | | | LM239/339 | | | LM2901 | | | MC3302 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage (Note 4) | $V_{IO}$ | — | — | ±4.0 | — | — | ±4.0 | — | — | ±9.0 | — | — | +9.0 | — | — | ±15 | — | — | ±40 | mVdc |
| Input Bias Current (Notes 4, 5) (Output in Linear Range) | $I_{IB}$ | — | — | 300 | — | — | 400 | — | — | 300 | — | — | 400 | — | — | 500 | — | — | 1000 | nA |
| Input Offset Current (Note 4) | $I_{IO}$ | — | — | ±100 | — | — | ±150 | — | — | ±100 | — | — | ±150 | — | — | ±200 | — | — | ±300 | nA |
| Input Common-Mode Voltage Range | $V_{ICR}$ | 0 | — | $V_{CC}$ -2.0 | 0 | — | $V_{CC}$ -2.0 | 0 | — | $V_{CC}$ -2.0 | 0 | — | $V_{CC}$ -2.0 | 0 | — | $V_{CC}$ -2.0 | 0 | — | $V_{CC}$ -2.0 | V |
| Saturation Voltage $V_I(-) \geq +1.0$ Vdc, $V_I(+) = 0$, $I_{sink} \leq 4.0$ mA | $V_{sat}$ | — | — | 700 | — | — | 700 | — | — | 700 | — | — | 700 | — | — | 700 | — | — | 700 | mV |
| Output Leakage Current $V_I(+) \geq +1.0$ Vdc, $V_I(-) = 0$, $V_O$ = 30 Vdc | $I_{OL}$ | — | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | — | 1.0 | μA |
| Differential Input Voltage All $V_I \geq 0$ Vdc (Note 7) | $V_{ID}$ | — | — | $V_{CC}$ | — | — | $V_{CC}$ | — | — | $V_{CC}$ | — | — | $V_{CC}$ | — | — | $V_{CC}$ | — | — | $V_{CC}$ | Vdc |

NOTES:

1. The maximum output current may be as high as 20 mA, independent of the magnitude of $V_{CC}$. Output short circuits to $V_{CC}$ can cause excessive heating and eventual destruction.
2. This magnitude of input current will only occur if the leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector-base junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action which can cause the output voltage of the comparators to go to the $V_{CC}$ voltage level (or ground if overdrive is large) during the time that an input is driven negative. This will not destroy the device when limited to the max rating and normal output states will recover when the inputs become ⩾ ground or negative supply.
3. LM139/139A — $T_{low}$ = -55°C, $T_{high}$ = +125°C  LM339/339A — $T_{low}$ = 0°C, $T_{high}$ = +70°C
3. LM239/239A — $T_{low}$ = -25°C, $T_{high}$ = +85°C  LM2901/MC3302 — $T_{low}$ = -40°C, $T_{high}$ = +85°C
4. At the output switch point, $V_O \simeq 1.4$ Vdc, $R_S \leq 100$ Ω, 5.0 Vdc ⩽ $V_{CC}$ ⩽ 30 Vdc, with the inputs over the full common-mode range (0 Vdc to $V_{CC}$ - 1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.
7. Positive excursions of input voltage may exceed the power supply level. As long as one of the inputs remain within the common-mode range, the comparator will provide the proper output state. With $V_{CC}$ = 5.0 Vdc, $V_I$ should be limited to 25 volts max. Limiting resistors should be used on all inputs that might exceed $V_{CC}$.

**FIGURE 2 — INVERTING COMPARATOR WITH HYSTERESIS**


+VCC
R3
10 k
VIN
Rref
+VCC
10 k
VO
Vref
R2
1M
10 k
R1

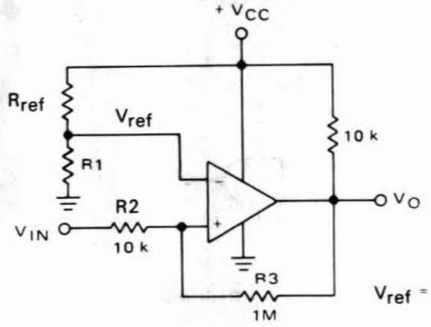
$$V_{ref} \approx \frac{V_{CC}\ R1}{R_{ref} + R1}$$

$$R3 \approx R1\ //\ R_{ref}//R2$$

$$V_H = \frac{R1//\ R_{ref}}{R1//R_{ref} + R2}\ (V_{O\,max} - V_{O\,min})$$

$$R2 >> R_{ref}//R1$$

**FIGURE 3 — NON-INVERTING COMPARATOR WITH HYSTERESIS**


+VCC
Rref
Vref
R1
10 k
VO
R2
VIN
10 k
R3
1M

$$V_{ref} = \frac{V_{CC}\ R1}{R_{ref} + R1}$$

$$R2 \approx R1//R_{ref}$$

Amount of Hysteresis $V_H$

$$V_H = \frac{R2}{R2 + R3}\ (V_{O\,max} - V_{O\,min})$$

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +15 Vdc, $T_A$ = +25°C (each comparator) unless otherwise noted.)

**FIGURE 4 — NORMALIZED INPUT OFFSET VOLTAGE**

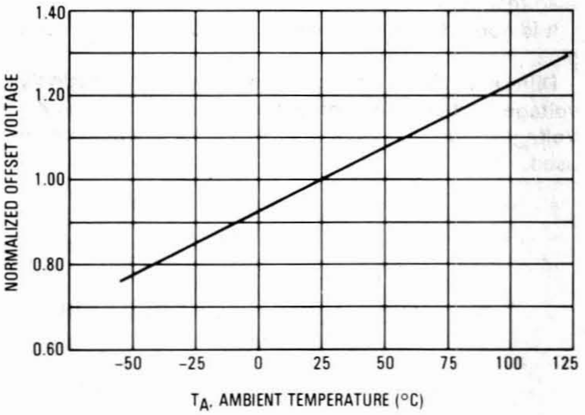


**FIGURE 5 — INPUT BIAS CURRENT**

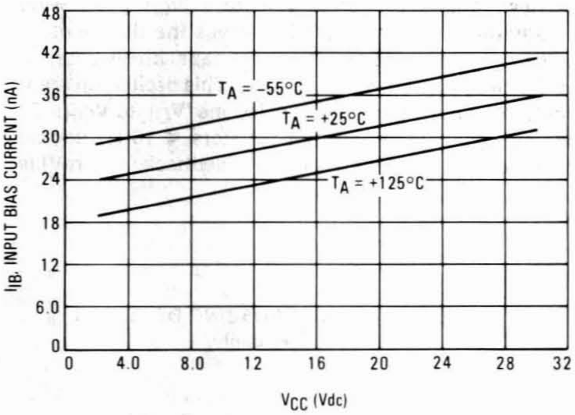


**FIGURE 6 — OUTPUT SINK CURRENT versus OUTPUT SATURATION VOLTAGE**

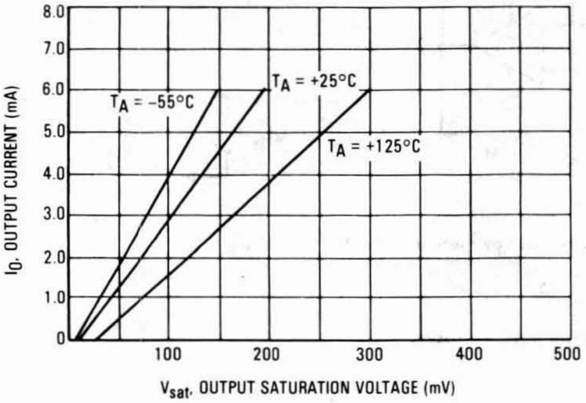
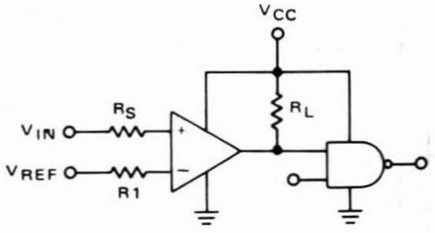


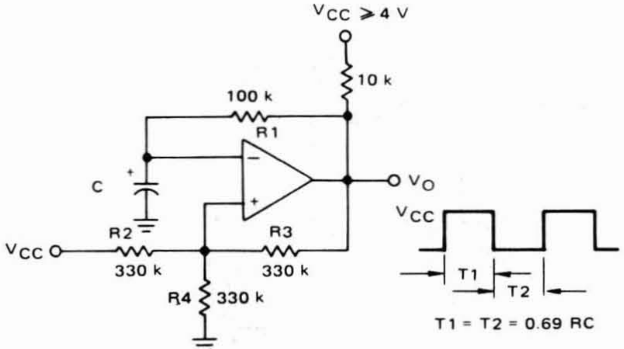
FIGURE 7 — DRIVING LOGIC


V_CC
R_S
R_L
V_IN
V_REF
R1
+
−

$R_S$ = Source Resistance
$R1 \simeq R_S$

| LOGIC | DEVICE | V_CC Volts | R_L kΩ |
|---|---|---|---|
| CMOS | 1/4 MC14001 | +15 | 100 |
| TTL | 1/4 MC7400 | +5 | 10 |

FIGURE 8 — SQUAREWAVE OSCILLATOR


V_CC ≥ 4 V
10 k
100 k
R1
C
+
−
V_O
V_CC
R2
330 k
R3
330 k
R4
330 k
V_CC
T1
T2

$T1 = T2 = 0.69\ RC$

$f \approx \frac{7.2}{C(\mu F)}$

$R2 = R3 = R4$

$R1 \approx R2//R3//R4$

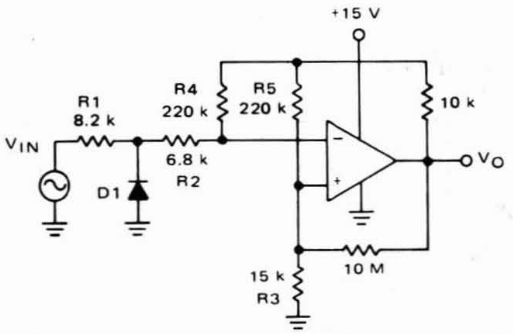
## APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transistions ($V_{OL}$ to $V_{OH}$). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (<10 mV) is also recommended.

It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than −300 mV should not be used.

FIGURE 9 — ZERO CROSSING DETECTOR
(Single Supply)


+15 V
R1
8.2 k
R4
220 k
R5
220 k
10 k
V_IN
6.8 k
R2
D1
−
+
V_O
15 k
R3
10 M

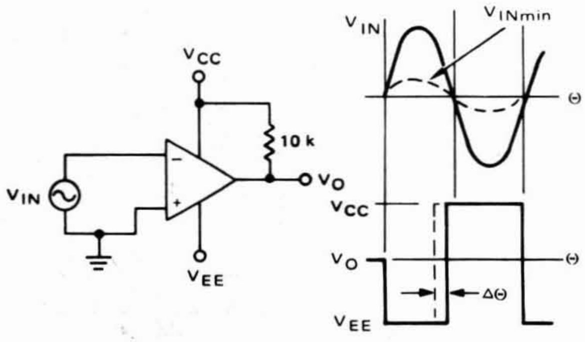
D1 prevents input from going negative by more than 0.6 V.

$R1 + R2 = R3$

$R3 \leq \frac{R5}{10}$ for small error in zero crossing

FIGURE 10 — ZERO CROSSING DETECTOR
(Split Supplies)

$V_{INmin} \approx 0.4$ V peak for 1% phase distortion (ΔΘ).


V_IN
V_INmin
Θ
V_CC
10 k
V_O
V_IN
−
+
V_EE
V_CC
V_O
Θ
ΔΘ
V_EE

**MOTOROLA**

# LM193 LM193A
# LM293 LM293A
# LM393 LM393A
# LM2903

## SINGLE-SUPPLY, LOW-POWER, LOW-OFFSET-VOLTAGE DUAL COMPARATORS

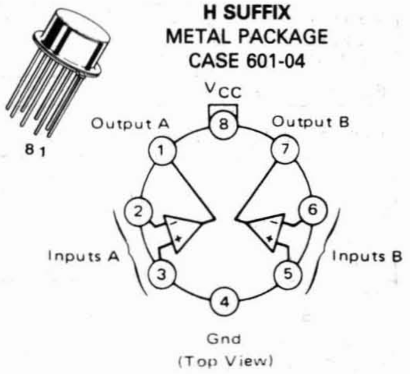
The LM193 series are dual independent precision voltage comparators capable of single-or split-supply operation. These devices are designed to permit a common mode range-to-ground level with single-supply operation. Input offset-voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer automotive, and industrial electronics.

- Wide Single-Supply Range — 2.0 Vdc to 36 Vdc
- Split-Supply Range — ±1.0 Vdc to ±18 Vdc
- Very Low Current Drain Independent of Supply-Voltage — 0.4 mA
- Low Input Bias Current — 25 nA
- Low Input Offset Current — 5.0 nA
- Low Input Offset Voltage — 2.0 mV (max) LM193A/293A/393A
  — 5.0 mV (max) LM193/293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS and CMOS Logic Levels

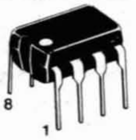
## DUAL COMPARATORS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

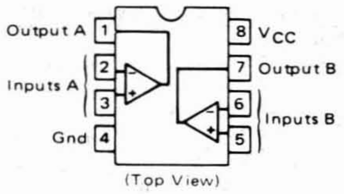
**H SUFFIX**
METAL PACKAGE
CASE 601-04


8 1
VCC
Output A
Output B
8
1
7
2
6
3
5
4
Inputs A
Inputs B
Gnd
(Top View)

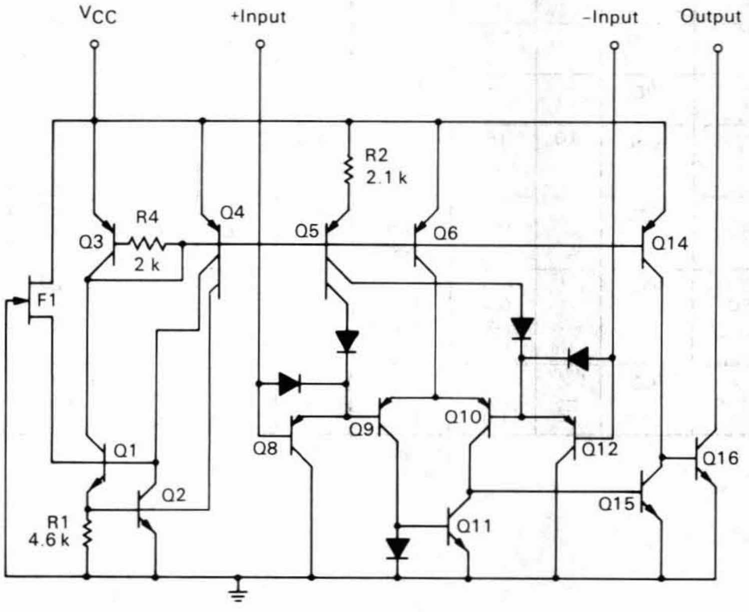
**N SUFFIX**
PLASTIC PACKAGE
CASE 626-04



**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8


Output A
1
Inputs A
2
3
Gnd
4
8
VCC
7
Output B
6
Inputs B
5
(Top View)

### FIGURE 1 — CIRCUIT SCHEMATIC
(Diagram shown is for 1 comparator)


VCC
+Input
-Input
Output
R2
2.1 k
R4
2 k
Q3
Q4
Q5
Q6
Q14
F1
Q1
Q2
R1
4.6 k
Q8
Q9
Q10
Q12
Q16
Q15
Q11

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| LM193AH,H | −55 to +125°C | Metal Can |
| LM293AH,H | 25 to +85°C | Metal Can |
| LM293D | | SO-8 |
| LM393AH,H | 0 to +70°C | Metal Can |
| LM393D | | SO-8 |
| LM393AN,N | | Plastic Mini DIP |
| LM2903D | −40 to +85°C | SO-8 |
| LM2903N | | Plastic Mini DIP |

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +36 or ±18 | Vdc |
| Input Differential Voltage Range | $V_{IDR}$ | 36 | Vdc |
| Input Common Mode Voltage Range | $V_{ICR}$ | -0.3 to +36 | Vdc |
| **Input Current (2)**<br>**($V_{in}$ < −0.3 Vdc)** | $I_{in}$ | 50 | mA |
| **Output Short Circuit-to-Ground**<br>**Output Sink Current (1)** | $I_{SC}$<br>$I_{sink}$ | Continuous<br>20 | mA |
| Power Dissipation @ $T_A$ = 25°C<br>Molded DIP<br>Derate above 25°C<br>Metal Can<br>Derate above 25°C | <br>$P_D$<br>$1/R_{\theta JA}$<br>$P_D$<br>$1/R_{\theta JA}$ | <br>570<br>5.7<br>830<br>6.64 | <br>mW<br>mW/°C<br>mW<br>mW/°C |
| Operating Ambient Temperature Range<br>LM193, 193A<br>LM293, 293A<br>LM393, 393A<br>LM2903 | $T_A$ | <br>-55 to +125<br>-25 to +85<br>0 to +70<br>-40 to +85 | °C |
| Maximum Operating Junction Temperature<br>LM393, 393A, 2903<br>LM193, 193A, 293, 293A | $T_{J(max)}$ | <br>125<br>150 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 Vdc; $^*T_{low} \leqslant T_A \leqslant T_{high}$ unless otherwise stated.)

| | | LM193A | | | LM293A, LM393A | | | |
|---|---|---|---|---|---|---|---|---|
| Characteristic | Symbol | Min | Typ | Max | Min | Typ | Max | Unit |
| **Input Offset Voltage (3)**<br>**$T_A$ = 25°C**<br>**$T_{low} \leqslant T_A \leqslant T_{high}$** | $V_{IO}$ | <br>—<br>— | <br>±1.0<br>— | <br>±2.0<br>4.0 | <br>—<br>— | <br>±1.0<br>— | <br>±2.0<br>4.0 | mV |
| Input Offset Current<br>$T_A$ = 25°C<br>$T_{low} \leqslant T_A \leqslant T_{high}$ | $I_{IO}$ | <br>—<br>— | <br>±3.0<br>— | <br>±25<br>±100 | <br>—<br>— | <br>±5.0<br>— | <br>±50<br>±150 | nA |
| Input Bias Current (4)<br>$T_A$ = 25°C<br>$T_{low} \leqslant T_A \leqslant T_{high}$ | $I_{IB}$ | <br>—<br>— | <br>25<br>— | <br>100<br>300 | <br>—<br>— | <br>25<br>— | <br>250<br>400 | nA |
| Input Common Mode Voltage Range (5)<br>$T_A$ = 25°C<br>$T_{low} \leqslant T_A \leqslant T_{high}$ | $V_{ICR}$ | <br>0<br>0 | <br>—<br>— | <br>$V_{CC}$ -1.5<br>$V_{CC}$ -2.0 | <br>0<br>0 | <br>—<br>— | <br>$V_{CC}$ -1.5<br>$V_{CC}$ -2.0 | Volts |
| Voltage Gain<br>$R_L \geqslant$ 15 kΩ, $V_{CC}$ = 15 Vdc, $T_A$ = 25°C | $A_{VOL}$ | 50 | 200 | — | 50 | 200 | — | V/mV |
| Large Signal Response Time<br>$V_{in}$ = TTL Logic Swing, $V_{ref}$ = 1.4 Vdc<br>$V_{RL}$ = 5.0 Vdc, $R_L$ = 5.1 kΩ, $T_A$ = 25°C | — | — | 300 | — | — | 300 | — | ns |
| Response Time (5)<br>$V_{RL}$ = 5.0 Vdc, $R_L$ = 5.1 kΩ, $T_A$ = 25°C | $t_{TLH}$ | — | 1.3 | — | — | 1.3 | — | μs |
| Input Differential Voltage (7)<br>All $V_{in} \geqslant$ Gnd or V− Supply (if used) | $V_{ID}$ | — | — | $V_{CC}$ | — | — | $V_{CC}$ | V |
| Output Sink Current<br>$V_{in-} \geqslant$ 1.0 Vdc, $V_{in+}$ = 0 Vdc, $V_O \leqslant$ 1.5 Vdc<br>$T_A$ = 25°C | $I_{sink}$ | 6.0 | 16 | — | 6.0 | 16 | — | mA |
| Output Saturation Voltage<br>$V_{in-} \geqslant$ 1.0 Vdc, $V_{in+}$ = 0, $I_{sink} \leqslant$ 4.0 mA, $T_A$ = 25°C<br>$T_{low} \leqslant T_A \leqslant T_{high}$ | $V_{OL}$ | <br>—<br>— | <br>150<br>— | <br>400<br>700 | <br>—<br>— | <br>150<br>— | <br>400<br>700 | mV |
| Output Leakage Current<br>$V_{in-}$ = 0 V, $V_{in+} \geqslant$ 1.0 Vdc, $V_O$ = 5.0 Vdc, $T_A$ = 25°C<br>$V_{in-}$ = 0 V, $V_{in+} \geqslant$ 1.0 Vdc, $V_O$ = 30 Vdc,<br>$T_{low} \leqslant T_A \leqslant T_{high}$ | $I_{OL}$ | <br>—<br>— | <br>0.1<br>— | <br>—<br>1.0 | <br>—<br>— | <br>0.1<br>— | <br>—<br>1.0 | μA |
| Supply Current<br>$R_L$ = ∞ Both Comparators, $T_A$ = 25°C<br>$R_L$ = ∞ Both Comparators, $V_{CC}$ = 30 V | $I_{CC}$ | <br>—<br>— | <br>0.4<br>1.0 | <br>1.0<br>2.5 | <br>—<br>— | <br>0.4<br>1.0 | <br>1.0<br>2.5 | mA |

*LM193/193A — $T_{low}$ = -55°C, $T_{high}$ = +125°C
LM293/293A — $T_{low}$ = -25°C, $T_{high}$ = +85°C
LM393/393A — $T_{low}$ = 0°C, $T_{high}$ = +70°C
LM2903 — $T_{low}$ = -40°C, $T_{high}$ = +85°C

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 Vdc; *$T_{low} \leq T_A \leq T_{high}$ unless otherwise stated.)

| Characteristic | Symbol | LM193 | | | LM293, LM393 | | | LM2903 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage (3) | $V_{IO}$ | | | | | | | | | | mV |
| $T_A$ = 25°C | | — | ±1.0 | ±5.0 | — | ±1.0 | ±5.0 | — | ±2.0 | ±7.0 | |
| $T_{low} \leq T_A \leq T_{high}$ | | — | — | 9.0 | — | — | 9.0 | — | 9.0 | 15 | |
| Input Offset Current | $I_{IO}$ | | | | | | | | | | nA |
| $T_A$ = 25°C | | — | ±3.0 | ±25 | — | ±5.0 | ±50 | — | ±5.0 | ±50 | |
| $T_{low} \leq T_A \leq T_{high}$ | | — | — | ±100 | — | — | ±150 | — | ±50 | ±200 | |
| Input Bias Current (4) | $I_{IB}$ | | | | | | | | | | nA |
| $T_A$ = 25°C | | — | 25 | 100 | — | 25 | 250 | — | 25 | 250 | |
| $T_{low} \leq T_A \leq T_{high}$ | | — | — | 300 | — | — | 400 | — | 200 | 500 | |
| Input Common Mode Voltage Range (4) | $V_{ICR}$ | | | | | | | | | | Volts |
| $T_A$ = 25°C | | 0 | — | $V_{CC}$ -1.5 | 0 | — | $V_{CC}$ -1.5 | 0 | — | $V_{CC}$ -1.5 | |
| $T_{low} \leq T_A \leq T_{high}$ | | 0 | — | $V_{CC}$ -2.0 | 0 | — | $V_{CC}$ -2.0 | 0 | — | $V_{CC}$ -2.0 | |
| Voltage Gain<br>$R_L \geq$ 15 kΩ, $V_{CC}$ = 15 Vdc,<br>$T_A$ = 25°C | $A_{VOL}$ | 50 | 200 | — | 50 | 200 | — | 25 | 200 | — | V/mV |
| Large Signal Response Time<br>$V_{in}$ = TTL Logic Swing,<br>$V_{ref}$ = 1.4 Vdc<br>$V_{RL}$ = 5.0 Vdc, $R_L$ = 5.1 kΩ,<br>$T_A$ = 25°C | — | — | 300 | — | — | 300 | — | — | 300 | — | ns |
| Response Time (6)<br>$V_{RL}$ = 5.0 Vdc, $R_L$ = 5.1 kΩ,<br>$T_A$ = 25°C | $t_{TLH}$ | — | 1.3 | — | — | 1.3 | — | — | 1.5 | — | µs |
| Input Differential Voltage (7)<br>All $V_{in} \geq$ Gnd or V– Supply<br>(if used) | $V_{ID}$ | — | — | $V_{CC}$ | — | — | $V_{CC}$ | — | — | $V_{CC}$ | V |
| Output Sink Current<br>$V_{in-} \geq$ 1.0 Vdc, $V_{in+}$ = 0 Vdc,<br>$V_O \leq$ 1.5 Vdc $T_A$ = 25°C | $I_{sink}$ | 6.0 | 16 | — | 6.0 | 16 | — | 6.0 | 16 | — | mA |
| Output Saturation Voltage | $V_{OL}$ | | | | | | | | | | mV |
| $V_{in-} \geq$ 1.0 Vdc, $V_{in+}$ = 0,<br>$I_{sink} \leq$ 4.0 mA, $T_A$ = 25°C | | — | 150 | 400 | — | 150 | 400 | — | — | 400 | |
| $T_{low} \leq T_A \leq T_{high}$ | | — | — | 700 | — | — | 700 | — | 200 | 700 | |
| Output Leakage Current | $I_{OL}$ | | | | | | | | | | nA |
| $V_{in-}$ = 0 V, $V_{in+} \geq$ 1.0 Vdc,<br>$V_O$ = 5.0 Vdc, $T_A$ = 25°C | | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | |
| $V_{in-}$ = 0 V, $V_{in+} \geq$ 1.0 Vdc,<br>$V_O$ = 30 Vdc,<br>$T_{low} \leq T_A \leq T_{high}$ | | — | — | 1000 | — | — | 1000 | — | — | 1000 | |
| Supply Current | $I_{CC}$ | | | | | | | | | | mA |
| $R_L$ = ∞ Both Comparators,<br>$T_A$ = 25°C | | — | 0.4 | 1.0 | — | 0.4 | 1.0 | — | 0.4 | 1.0 | |
| $R_L$ = ∞ Both Comparators,<br>$V_{CC}$ = 30 V | | — | — | 2.5 | — | — | 2.5 | — | — | 2.5 | |

*LM193/193A — $T_{low}$ = -55°C, $T_{high}$ = +125°C
LM293/293A — $T_{low}$ = -25°C, $T_{high}$ = +85°C
LM393/393A — $T_{low}$ = 0°C, $T_{high}$ = +70°C

**NOTES:**

(1) The max. output current may be as high as 20 mA, independent of the magnitude of $V_{CC}$, output short circuits to $V_{CC}$ can cause excessive heating and eventual destruction.

(2) This magnitude of input current will only occur if the input leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector base junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action on the IC chip. This phenomena can cause the output voltage of the comparators to go to the $V_{CC}$ voltage level (or ground if overdrive is large) during the time the input is driven negative. This will not destroy the device and normal output states will recover when the inputs become > −0.3 V of ground or negative supply.

(3) At output switch point, $V_O \simeq$ 1.4 Vdc, $R_S$ = 0 Ω with $V_{CC}$ from 5.0 Vdc to 30 Vdc, and over the full input common-mode range (0 volts to $V_{CC}$ = −1.5 volts)

(4) Due to the PNP transistor inputs, bias current will flow out of the inputs, this current is essentially constant independent of the output state, therefore, no loading changes will exist on the input lines.

(5) Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is $V_{CC}$ − 1.5 V but either or both inputs can be taken to as high as 30 volts without damage.

(6) Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.

(7) The comparator will exhibit proper output state if one of the inputs become greater than $V_{CC}$, the other input must remain within the common mode range. The low input state must not be less than −0.3 volts of ground of minus supply.

## TYPICAL PERFORMANCE CHARACTERISTICS

### LM193,A/293,A/393,A

FIGURE 2 — INPUT BIAS CURRENT versus POWER SUPPLY VOLTAGE

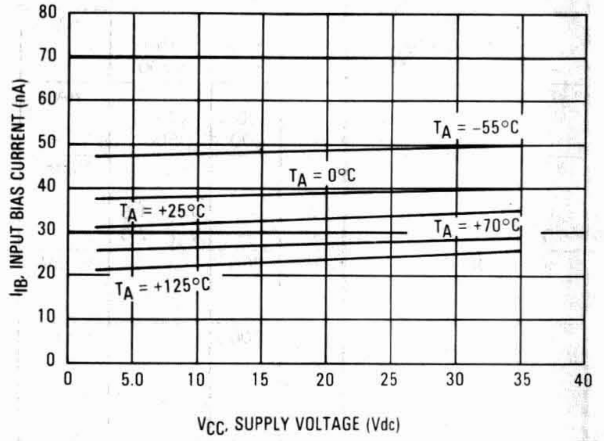


FIGURE 3 — OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

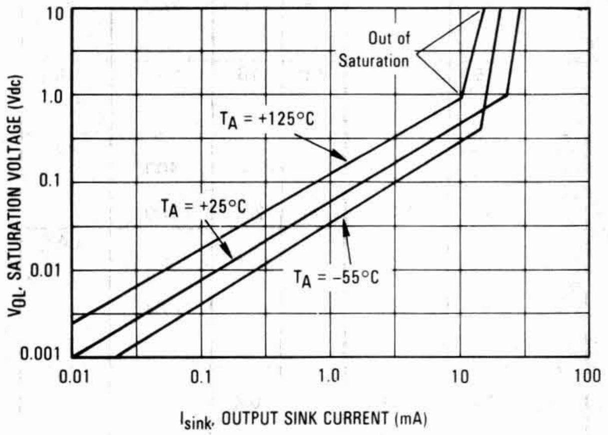
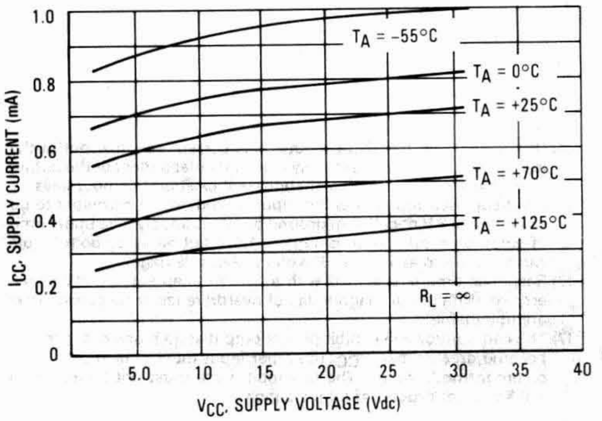


FIGURE 4 — POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE



### LM2903

FIGURE 5 — INPUT BIAS CURRENT versus POWER SUPPLY VOLTAGE

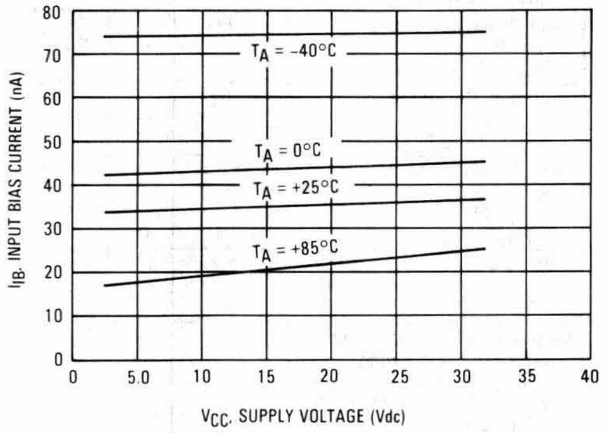


FIGURE 6 — OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

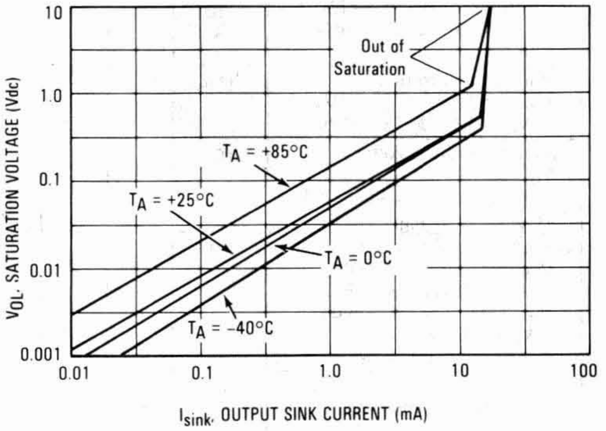
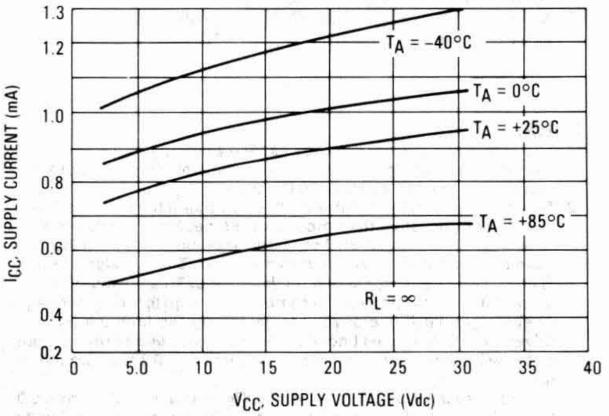


FIGURE 7 — POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE



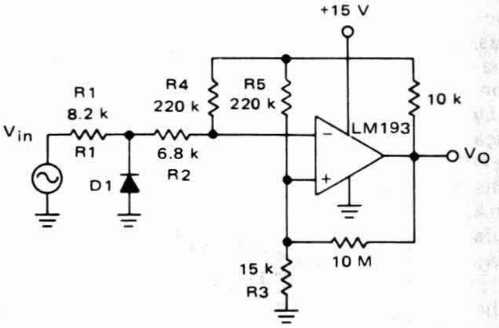
## APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions ($V_{OL}$ to $V_{OH}$). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (< 10 mV) is also recommended.

It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than −0.3 V should not be used.

**FIGURE 8 — ZERO CROSSING DETECTOR**
**(Single Supply)**


+15 V
R1
8.2 k
R4
220 k
R5
220 k
10 k
Vin
R1
6.8 k
R2
D1
LM193
Vo
15 k
R3
10 M

D1 prevents input from going negative by more than 0.6 V.

$R1 + R2 = R3$

$R3 \leqslant \frac{R5}{10}$ for small error in zero crossing

**FIGURE 9 — ZERO CROSSING DETECTOR**
**(Split Supplies)**

$V_{INmin} \approx 0.4$ V peak for 1% phase distortion (ΔΘ).

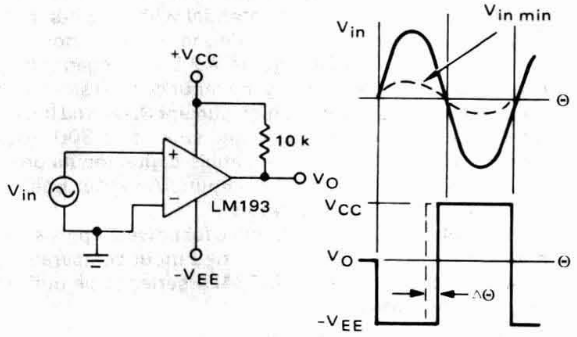

Vin
Vin min
Θ
+VCC
10 k
Vo
Vin
LM193
VCC
Vo
Θ
ΔΘ
-VEE
-VEE

**FIGURE 10 — FREE-RUNNING SQUARE-WAVE OSCILLATOR**

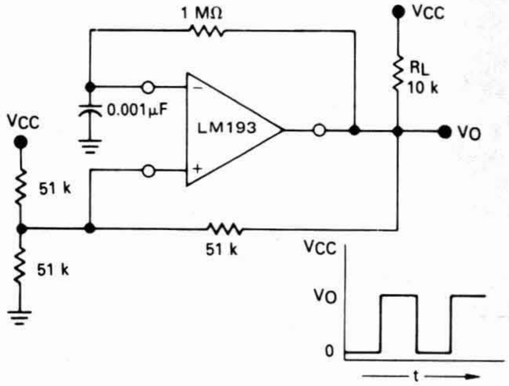
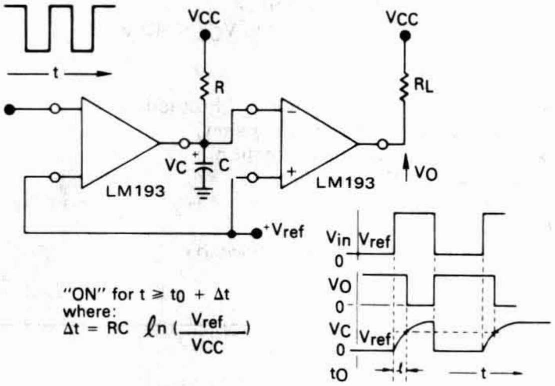
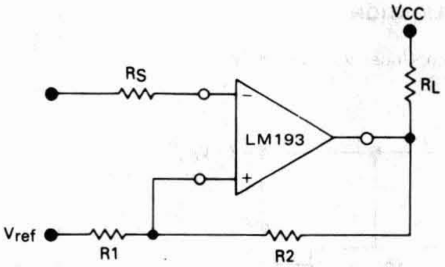

1 MΩ
VCC
RL
10 k
0.001µF
LM193
VO
VCC
51 k
51 k
51 k
VCC
VO
0
t

**FIGURE 11 — TIME DELAY GENERATOR**


t
VCC
VCC
R
RL
VC
C
LM193
LM193
VO
+Vref
Vin
Vref
0
VO
0
VC
Vref
0
tO
t
t

"ON" for t ⩾ $t_0 + \Delta t$
where:
$\Delta t = RC \, \ell n \left(\frac{V_{ref}}{V_{CC}}\right)$

**FIGURE 12 — COMPARATOR WITH HYSTERESIS**


VCC
RS
RL
LM193
Vref
R1
R2

$R_S = R1 \parallel R2$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\,R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_{O\,Low})\,R1}{R1 + R2 + R_L}$$

**Complete data sheet can be found in Chapter 4 on page 4-255.**

# MC3424, MC3424A
# MC3524, MC3524A
# MC3324, MC3324A

## POWER SUPPLY SUPERVISORY CIRCUIT/ DUAL-VOLTAGE COMPARATOR

The MC3424 series is a dual-channel supervisory circuit, consisting of two uncommitted input comparators, a reference, output comparators, with high current Drive and Indicator outputs for each channel. The input comparators feature programmable hysteresis, high common-mode rejection, and wide common-mode range, capable of comparing at ground potential with single-supply operation. Separate Delay pins are provided to increase noise immunity by delaying activation of the outputs. A 2.5 V bandgap voltage reference is pinned-out for referencing the input comparators, or other external functions. Independent high current Drive and Indicator outputs for each channel can source and sink up to 300 mA and 30 mA respectively. CMOS/TTL compatible digital inputs provide Remote Activation of each channel's outputs. An Input Enable pin allows control of the input comparators.

Although this device is intended for power supply supervision, the pinned-out reference, uncommitted input comparators, and many other features, enable the MC3424 series to be utilized for a wide range of applications.

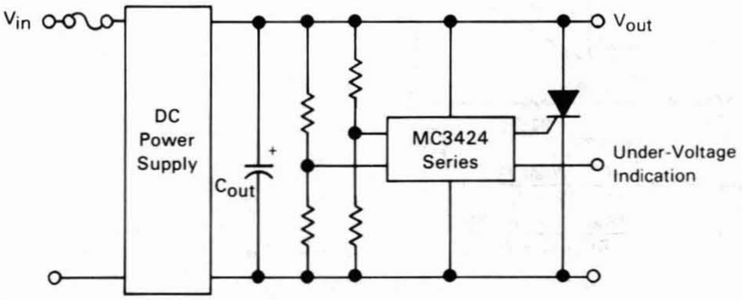
- Pinned-Out 2.5 V Reference
- Wide Common-Mode Range
- Programmable Hysteresis
- Programmable Time Delays
- Two 300 mA Drive Outputs
- Remote Activation Capability
- Wide Supply Range: 4.5 V $\leq V_{CC} \leq$ 40 V

### APPLICATIONS

- Dual Over-Voltage "Crowbar" Protection
- Dual Under-Voltage Supervision
- Over/Under Voltage Protection
- Split-Supply Supervision
- Line-Loss Sensing
- Proportional Controller
- Programmable Frequency Switch
- Battery Charger

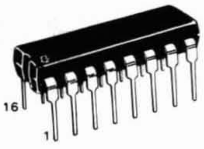
### TYPICAL APPLICATION

Over-Voltage Crowbar Protection, Under-Voltage Indication



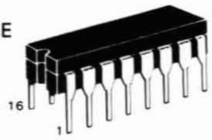
## POWER SUPPLY SUPERVISORY CIRCUIT/DUAL VOLTAGE COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

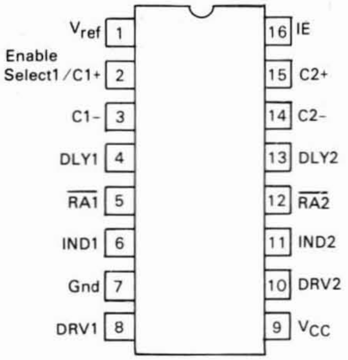


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02



### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

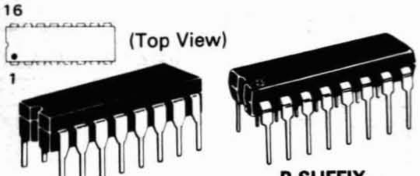
| Device | Temperature Range | Package |
|---|---|---|
| MC3524L, AL | -55 to +125°C | Ceramic DIP |
| MC3324L, AL | -40 to +85°C | Ceramic DIP |
| MC3324P, AP | | Plastic DIP |
| MC3424L, AL | 0 to +70°C | Ceramic DIP |
| MC3424P, AP | | Plastic DIP |

**MOTOROLA**

# MC3430
# thru
# MC3433

## QUAD HIGH-SPEED VOLTAGE COMPARATORS

### SILICON MONOLITHIC INTEGRATED CIRCUITS


16
(Top View)
1

**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

## QUAD DIFFERENTIAL VOLTAGE COMPARATOR/SENSE AMPLIFIERS

The MC3430 thru MC3433 high-speed comparators are ideal for application as sense amplifiers in MOS memory systems. They are specified in a unique way which combines the effects of input offset voltage, input offset current, voltage gain, temperature variations and input common-mode range into a single functional parameter. This parameter, called Input Sensitivity, specifies a minimum differential input voltage which will guarantee a given logic state. Four variations are offered in the comparator series.

The MC3430 and MC3431 versions feature a three-state strobe input common to all four channels which can be used to place the four outputs in a high-impedance state. These two devices use active-pull-up MTTL compatible outputs. The MC3432 and MC3433 are open-collector types which permit the implied AND connection. The MC3430 and MC3432 versions are specified for a ±7.0 mV input sensitivity over the 0 to 70°C temperature range, while the MC3431 and MC3433 are specified for ±12 mV.

- Propagation Delay Time – 40 ns
- Outputs Specified for a Fanout of 10 (MC7400 type loads)
- Specified for all conditions of ±5% Power Supply Variations, Operating Temperature Range, Input Common-Mode Voltage Swing from -3.0 V to 3.0 V, and $R_S \leqslant 200$ ohms.

CONNECTION DIAGRAM

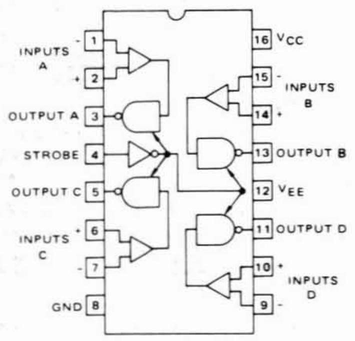
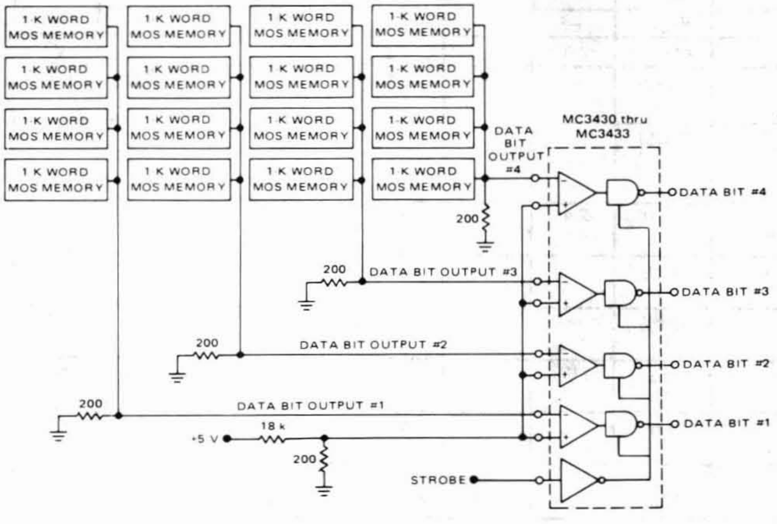

INPUTS A
-
+
1
2
OUTPUT A 3
STROBE 4
OUTPUT C 5
INPUTS C
+
-
6
7
GND 8
16 VCC
15 -
14 +
INPUTS B
13 OUTPUT B
12 VEE
11 OUTPUT D
10 +
9 -
INPUTS D

FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES


1-K WORD MOS MEMORY
DATA BIT OUTPUT #4
MC3430 thru MC3433
DATA BIT #4
200
200
DATA BIT OUTPUT #3
DATA BIT #3
200
DATA BIT OUTPUT #2
DATA BIT #2
200
DATA BIT OUTPUT #1
DATA BIT #1
+5 V
18 k
200
STROBE

Only four devices are required for a 4-k word by 16-bit memory system.

TRUTH TABLE
MC3430 and MC3432

| Input | Strobe | Output | Device |
|---|---|---|---|
| $V_{ID} \geqslant 7.0$ mV<br>$T_A = 0$ to 70°C | L | H | MC3430 |
| | H | Z | |
| | L | Off | MC3432 |
| | H | Off | |
| $-7.0$ mV $\leqslant V_{ID}$<br>$\leqslant 7.0$ mV<br>$T_A = 0$ to 70°C | L | I | MC3430 |
| | H | Z | |
| | L | I | MC3432 |
| | H | Off | |
| $V_{ID} \leqslant -7.0$ mV<br>$T_A = 0$ to 70°C | L | L | MC3430 |
| | H | Z | |
| | L | On | MC3432 |
| | H | Off | |

TRUTH TABLE
MC3431 and MC3433

| Input | Strobe | Output | Device |
|---|---|---|---|
| $V_{ID} \geqslant 12$ mV<br>$T_A = 0$ to 70°C | L | H | MC3431 |
| | H | Z | |
| | L | Off | MC3433 |
| | H | Off | |
| $-12$ mV $\leqslant V_{ID}$<br>$\leqslant +12$ mV<br>$T_A = 0$ to 70°C | L | I | MC3431 |
| | H | Z | |
| | L | I | MC3433 |
| | H | Off | |
| $V_{ID} \leqslant -12$ mV<br>$T_A = 0$ to 70°C | L | L | MC3431 |
| | H | Z | |
| | L | On | MC3433 |
| | H | Off | |

L = Low Logic State
H = High Logic State
Z = Third (High Impedance)
I = Indeterminate State
$R_S < 200\ \Omega$

**MAXIMUM RATINGS** ($T_A$ = 0 to +70°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}, V_{EE}$ | ±7.0 | Vdc |
| Differential Mode Input Signal Voltage Range | $V_{IDR}$ | ±6.0 | Vdc |
| Common-Mode Input Voltage Range | $V_{ICR}$ | ±5.0 | Vdc |
| Strobe Input Voltage | $V_{I(S)}$ | 5.5 | Vdc |
| Output Voltage (MC3432 – 33 versions) | $V_O$ | +7.0 | Vdc |
| Junction Temperature<br>Ceramic Package<br>Plastic Package | $T_J$ | <br>175<br>150 | °C |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**RECOMMENDED OPERATING CONDITIONS** ($T_A$ = 0 to +70°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltages | $V_{CC}$<br>$V_{EE}$ | +4.75<br>-4.75 | +5.0<br>-5.0 | +5.25<br>-5.25 | Vdc |
| Output Load Current | $I_{OL}$ | – | – | 16 | mA |
| Differential-Mode Input Voltage Range | $V_{IDR}$ | -5.0 | – | +5.0 | Vdc |
| Common-Mode Input Voltage Range | $V_{ICR}$ | -3.0 | – | +3.0 | Vdc |
| Input Voltage Range (any input to Ground) | $V_{IR}$ | -5.0 | – | +3.0 | Vdc |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 Vdc, $V_{EE}$ = -5.0 Vdc, $T_A$ = 0°C to +70°C unless otherwise noted.)
Typical Values are Measured at $T_A$ = 25°C

| | | MC3430, MC3431 | | | MC3432, MC3433 | | | |
|---|---|---|---|---|---|---|---|---|
| Characteristic | Symbol | Min | Typ | Max | Min | Typ | Max | Unit |
| Input Sensitivity (See Discussion on Page 3)<br>($R_S \leqslant 200$ Ohms) | $V_{IS}$ | | | | | | | mV |
| (Common Mode Voltage Range = $-3.0\ V \leqslant V_{in} \leqslant 3.0\ V$)<br>$4.75 \leqslant V_{CC} \leqslant 5.25$ V, $-4.75 \geqslant V_{EE} \geqslant -5.25$ V, $T_A = 25°C$, MC3430, MC3432 | | – | – | ±6.0 | – | – | ±6.0 | |
| MC3431, MC3433 | | – | – | ±10 | – | – | ±10 | |
| (Common Mode Voltage Range = $-3.0\ V \leqslant V_{in} \leqslant 3.0\ V$)<br>$4.75 \leqslant V_{CC} \leqslant 5.25$ V, $-4.75 \geqslant V_{EE} \geqslant -5.25$ V, $T_A$ = 0 to 70°C, MC3430, MC3432 | | – | – | ±7.0 | – | – | ±7.0 | |
| MC3431, MC3433 | | – | – | ±12 | – | – | ±12 | |
| Input Offset Voltage<br>($R_S \leqslant 200$ Ohms) | $V_{IO}$ | – | 2.0 | – | – | 2.0 | – | mV |
| Input Bias Current<br>($V_{CC}$ = 5.25 V, $V_{EE}$ = -5.25 V) MC3430, MC3432 | $I_{IB}$ | – | 20 | 40 | – | 20 | 40 | µA |
| MC3431, MC3433 | | – | 20 | 40 | – | 20 | 40 | |
| Input Offset Current | $I_{IO}$ | – | 1.0 | – | – | 1.0 | – | µA |
| Voltage Gain | $A_{vol}$ | – | 1200 | – | – | 1200 | – | V/V |
| Strobe Input Voltage (Low State) | $V_{IL(S)}$ | – | – | 0.8 | – | – | 0.8 | V |
| Strobe Input Voltage (High State) | $V_{IH(S)}$ | 2.0 | – | – | 2.0 | – | – | V |
| Strobe Current (Low State)<br>($V_{CC}$ = 5.25 V, $V_{EE}$ = -5.25 V, $V_{in}$ = 0.4 V) | $I_{IL(S)}$ | – | – | -1.6 | – | – | -1.6 | mA |
| Strobe Current (High State)<br>($V_{CC}$ = 5.25 V, $V_{EE}$ = -5.25 V, $V_{in}$ = 2.4 V) | $I_{IH(S)}$ | – | – | 40 | – | – | 40 | µA |
| ($V_{CC}$ = 5.25 V, $V_{EE}$ = -5.25 V, $V_{in}$ = 5.25 V) | | – | – | 1.0 | – | – | 1.0 | mA |
| Output Voltage (High State)<br>($I_O$ = -400 µA, $V_{CC}$ = 4.75 V, $V_{EE}$ = -4.75 V) | $V_{OH}$ | 2.4 | – | – | – | – | – | V |
| Output Voltage (Low State)<br>($I_O$ = 16 mA, $V_{CC}$ = 4.75 V, $V_{EE}$ = 4.75 V) | $V_{OL}$ | – | – | 0.4 | – | – | 0.4 | V |
| Output Leakage Current<br>($V_{CC}$ = 4.75 V, $V_{EE}$ = -4.75 V, $V_O$ = 5.25 V) | $I_{CEX}$ | – | – | – | – | – | 250 | µA |
| Output Current Short Circuit<br>($V_{CC}$ = 5.25 V, $V_{EE}$ = -5.25 V) | $I_{os}$ | -18 | – | -70 | – | – | – | mA |
| Output Disable Leakage Current<br>($V_{CC}$ = 5.25 V, $V_{EE}$ = -5.25 V) | $I_{off}$ | – | – | 40 | – | – | – | µA |
| High Logic Level Supply Currents<br>($V_{CC}$ = 5.25 V, $V_{EE}$ = -5.25 V) | $I_{CC}$<br>$I_{EE}$ | –<br>– | 45<br>-17 | 60<br>-30 | –<br>– | 45<br>-17 | 60<br>-30 | mA<br>mA |

## A UNIQUE FUNCTIONAL PARAMETER FOR COMPARATORS

A unique approach is used in specifying the MC3430-33 quad comparators. Previously, comparators have been specified as linear devices with common operational amplifier type parameters such as voltage gain ($A_{vol}$), input offset voltage ($V_{IO}$), input offset current ($I_{IO}$) and common-mode rejection ratio (CMRR). This is true despite the fact that most comparators are seldom operated in their linear region because it is difficult to hold a high gain comparator in this narrow region. Comparators are normally used to "detect" when an unknown voltage level exceeds a given reference voltage.

The most desirable comparator parameter is what minimum differential input voltage is required at the comparator's input terminals to guarantee a given output logic state. This new and important parameter has been called input sensitivity ($V_{IS}$) and is analagous to the input threshold voltage specification on a core memory sense amplifier. The input sensitivity specification includes the effects of voltage gain, input offset voltage and input offset current and eliminates the need for specifying these three parameters.

In order to make this parameter as inclusive as possible on the MC3430-33 series quad comparators, the input sensitivity is specified within the following conditions:

Commercial Temperature Range – 0 to 70°C
Power Supply Variations – ±5% (all conditions)
Input Source Resistance – ≤200 Ohms
Common-Mode Voltage Range – -3.0 V to +3.0 V

Note: Typical values have been included on the omitted parameters for applications where the offset voltages are externally nulled.

Voltage gain is defined as the ratio of the resulting $\Delta V_O$ to a change in the $V_{IDR}$ using conditions at which the $V_{IO}$ and $I_{IO}$ are nulled. Thus, for worst case MTTL logic levels, the required output voltage change is 2.0 V ($V_{OH}$min – $V_{OL}$max = 2.4 V – 0.4 V). If 2.0 mV are required at the input terminals to induce this change in logic state, the voltage gain would be 1000 V/V.

Gain however is not the only factor affecting the logic transition. Normally input offset voltages, that are not externally nulled, can add an appreciable error that drastically overshadows the comparator gain. Therefore, the 2.0 mV for example, required to cause the logic transition is often masked. An input offset voltage of up to 7.5 mV might be required to reach the linear region. A further consideration is the input offset current of up to ±10 μA flowing through the matched 200-Ohm source resistors at the input terminals which can create an additional error of ±2.0 mV. In order to determine a worst case input sensitivity, it must be assumed that minimum specified gain and maximum specified offset voltage and current conditions exist. Also it must be assumed that these three factors are cumulative, requiring a worst case input of:

Logic Transition = 2.0 mV
$V_{IO}$ = 7.5 mV
$I_{IO}$ of ±10 μA thru 200-Ohm resistor = 2.0 mV

Therefore, 2 + 7.5 + 2 = 11.5 mV.

The effects of power supply voltage variations, temperature changes and common-mode input voltage conditions have not been considered, as they are not present in the gain and offset specifications on most comparators.

Thus, the input sensitivity specification greatly reduces the effort required in determining the worst case differential voltage required by a given comparator type.

Table I compares the worst case input sensitivity of three popular comparator types at both room temperature and over the specified commercial temperature range (0 to 70°C). This sensitivity was computed from the specified voltage gain, offset voltage and offset current limits.

### TABLE I – WORST CASE COMPARISONS

| | $T_A$ = 25°C | | | | | | $T_A$ = 0 to 70°C | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Type Number | $V_{IO}$ mV Max | $A_{vol}$* V/V Typ | Differential Input Voltage Required for 3.0 V Output Change | $I_{IO}$ $R_S$ = 200 Ω μA Max | Error Voltage Generated Into 200 Ω Source Resistors | Total Sensitivity mV | $V_{IO}$ mV Max | $A_{vol}$* V/V Typ | Differential Input Voltage Required for 3.0 V Output Change | $I_{IO}$ $R_S$ = 200 Ω μA Max | Error Voltage Generated Into 200 Ω Source Resistors | Total Sensitivity mV |
| MC3430, MC3432 | – | – | – | – | – | 6.0 | – | – | – | – | – | 7.0 |
| MC3431, MC3433 | – | – | – | – | – | 10 | – | – | – | – | – | 12 |
| MC1711C | 5.0 | 1500 | 2.0 mV | 15 | 3.0 mV | 10 | 5.0 | 1000 | 3.0 mV | 25 | 5.0 mV | 13 |
| LM311 | 7.5 | 200 k | 0.015 mV | 6.0** | 0.0012 mV | 7.516 | 10 | 100 k | 0.030 mV | 70** | 0.014 mV | 10.04 |

*Typical values given, as minimum gain not always specified.
**$I_{IO}$ measured in nA

FIGURE 2 – GUARANTEED OUTPUT STATE versus DIFFERENTIAL INPUT VOLTAGE

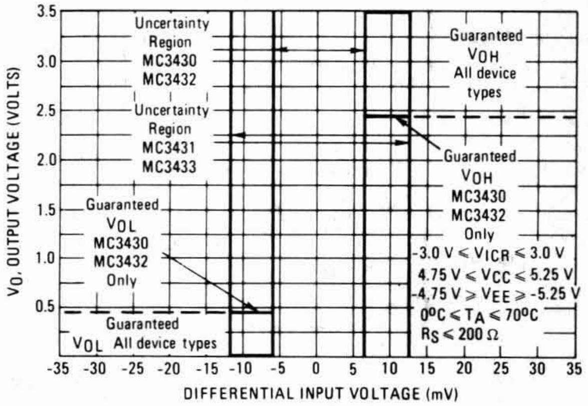
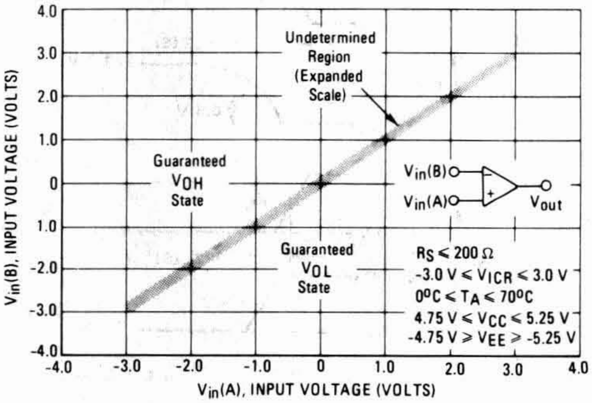


FIGURE 3 – GUARANTEED OUTPUT STATE versus INPUT VOLTAGE

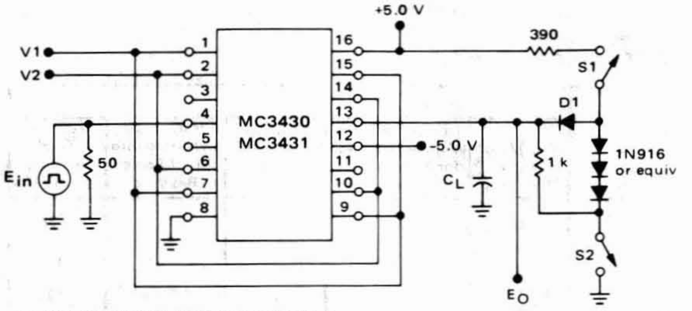


**SWITCHING CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $V_{EE}$ = -5.0 Vdc, $T_A$ = +25°C unless otherwise noted.)

| Characteristic | Symbol | Fig. | MC3430, MC3431 | | | MC3432, MC3433 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| High to Low Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV + $V_{IS}$ | $t_{PHL(D)}$ | 6,8-11 | – | 20 | 45 | – | 27 | 50 | ns |
| Low to High Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV + $V_{IS}$ | $t_{PLH(D)}$ | 6,8-11 | – | 33 | 55 | – | 40 | 65 | ns |
| Open State to High Logic Level Propagation Delay Time (Strobe) | $t_{PZH(S)}$ | 4 | – | – | 35 | – | – | – | ns |
| High Logic Level to Open State Propagation Delay Time (Strobe) | $t_{PHZ(S)}$ | 4 | – | – | 35 | – | – | – | ns |
| Open State to Low Logic Level Propagation Delay Time (Strobe) | $t_{PZL(S)}$ | 4 | – | – | 40 | – | – | – | ns |
| Low Logic Level to Open State Propagation Delay Time (Strobe) | $t_{PLZ(S)}$ | 4 | – | – | 35 | – | – | – | ns |
| High Logic to Low Logic Level Propagation Delay Time (Strobe) | $t_{PHL(S)}$ | 5 | – | – | – | – | – | 40 | ns |
| Low Logic to High Logic Level Propagation Delay Time (Strobe) | $t_{PLH(S)}$ | 5 | – | – | – | – | – | 35 | ns |

## TEST CIRCUITS

FIGURE 4 – STROBE PROPAGATION DELAY TIMES $t_{PLZ(S)}$, $t_{PZL(S)}$, $t_{PHZ(S)}$, and $t_{PZH(S)}$


+5.0 V
V1
V2
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MC3430
MC3431
390
S1
D1
-5.0 V
$C_L$
1 k
1N916
or equiv
S2
$E_O$
$E_{in}$
50

Output of Channel B shown under test, other channels are tested similarly.

| | V1 | V2 | S1 | S2 | $C_L$ |
|---|---|---|---|---|---|
| $t_{PLZ(S)}$ | 100 mV | GND | Closed | Closed | 15 pF |
| $t_{PZL(S)}$ | 100 mV | GND | Closed | Open | 50 pF |
| $t_{PHZ(S)}$ | GND | 100 mV | Closed | Closed | 15 pF |
| $t_{PZH(S)}$ | GND | 100 mV | Open | Closed | 50 pF |

$C_L$ includes jig and probe capacitance.
$E_{in}$ waveform characteristics:
$t_{TLH}$ and $t_{THL}$ ⩽ 10 ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

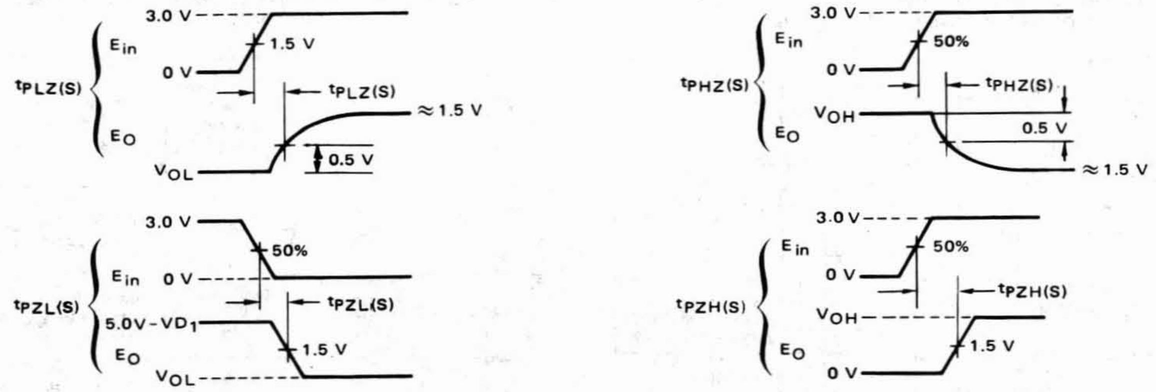
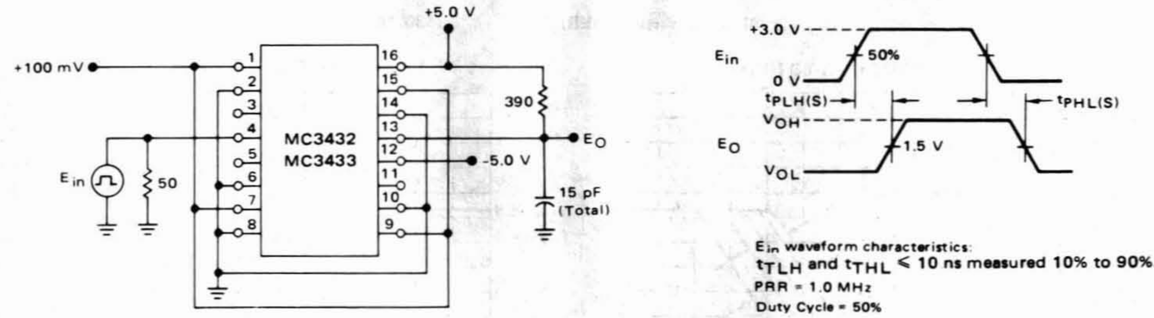

3.0 V
$E_{in}$
1.5 V
0 V
$t_{PLZ(S)}$
$t_{PLZ(S)}$
≈ 1.5 V
$E_O$
0.5 V
$V_{OL}$
3.0 V
$E_{in}$
50%
0 V
$t_{PHZ(S)}$
$t_{PHZ(S)}$
$V_{OH}$
0.5 V
$E_O$
≈ 1.5 V
3.0 V
50%
$E_{in}$
0 V
$t_{PZL(S)}$
$t_{PZL(S)}$
5.0V - $V_{D1}$
$E_O$
1.5 V
$V_{OL}$
3.0 V
$E_{in}$
50%
0 V
$t_{PZH(S)}$
$t_{PZH(S)}$
$V_{OH}$
$E_O$
1.5 V
0 V

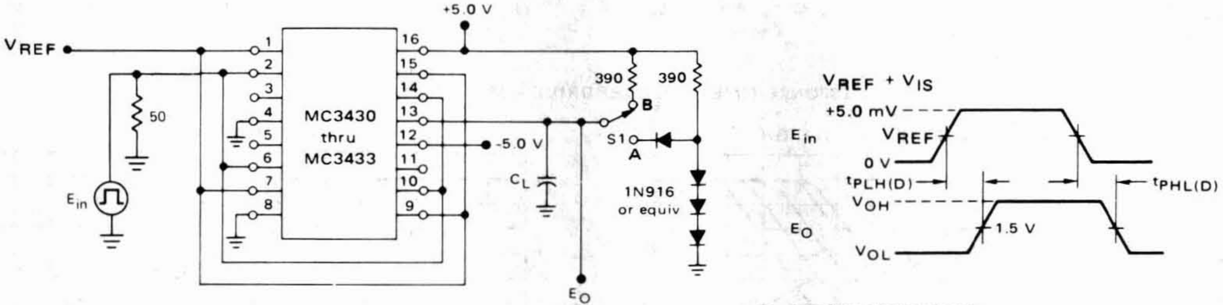
FIGURE 5 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$


+5.0 V
+100 mV
MC3432
MC3433
390
E O
-5.0 V
15 pF (Total)
E in
50
+3.0 V
E in
50%
0 V
tPLH(S)
tPHL(S)
VOH
E O
1.5 V
VOL

$E_{in}$ waveform characteristics:
$t_{TLH}$ and $t_{THL} \leq 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

Output of Channel B shown under test, other channels are tested similarly.

FIGURE 6 – DIFFERENTIAL INPUT PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$


VREF
+5.0 V
50
E in
MC3430
thru
MC3433
390
390
B
S1
A
-5.0 V
CL
1N916
or equiv
E O
VREF + VIS
+5.0 mV
E in
VREF
0 V
tPLH(D)
tPHL(D)
VOH
E O
1.5 V
VOL

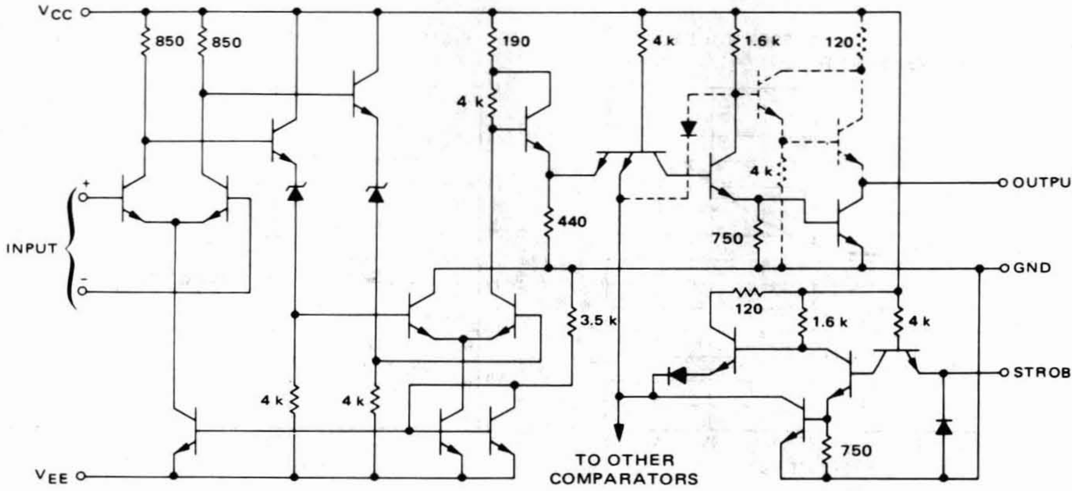
Output of Channel B shown under test, other channels are tested similarly.

$E_{in}$ waveform characteristics:
$t_{TLH}$ and $t_{THL} \leq 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

S1 at "A" for MC3430, MC3431
S1 at "B" for MC3432, MC3433
$C_L$ = 50 pF total for MC3430, MC3431
$C_L$ = 15 pF total for MC3432, MC3433

| Device | $V_{REF}$ mV |
|---|---|
| MC3430 | 11 |
| MC3431 | 15 |
| MC3432 | 11 |
| MC3433 | 15 |

FIGURE 7 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)


VCC
850
850
190
4 k
1.6 k
120
4 k
4 k
+
INPUT
-
440
750
OUTPUT
GND
3.5 k
120
1.6 k
4 k
STROBE
4 k
4 k
750
TO OTHER COMPARATORS
VEE

Dashed components apply to the MC3430 and MC3431 circuits only.

## TYPICAL PERFORMANCE CURVES

### RESPONSE TIME versus OVERDRIVE – MC3430, MC3431

FIGURE 8 – OUTPUT LOW TO HIGH

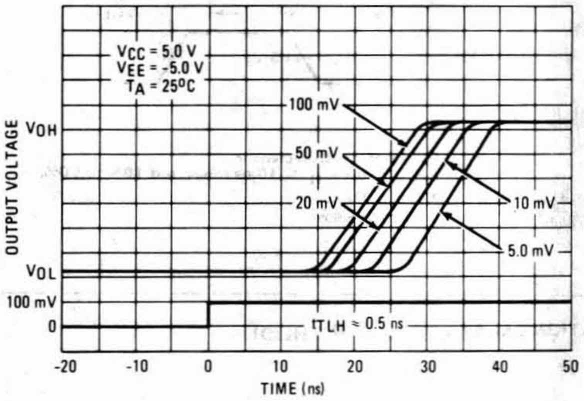
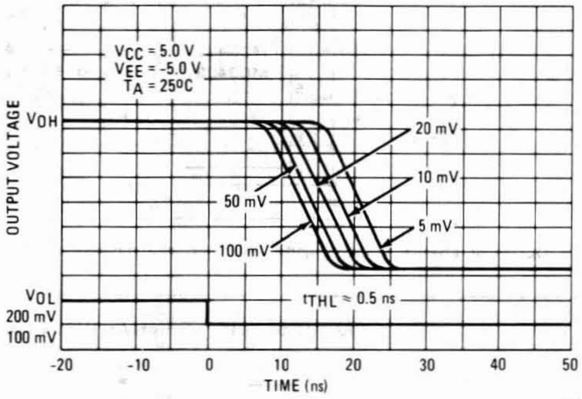


FIGURE 9 – OUTPUT HIGH TO LOW



### RESPONSE TIME versus OVERDRIVE – MC3432, MC3433

FIGURE 10 – OUTPUT LOW TO HIGH

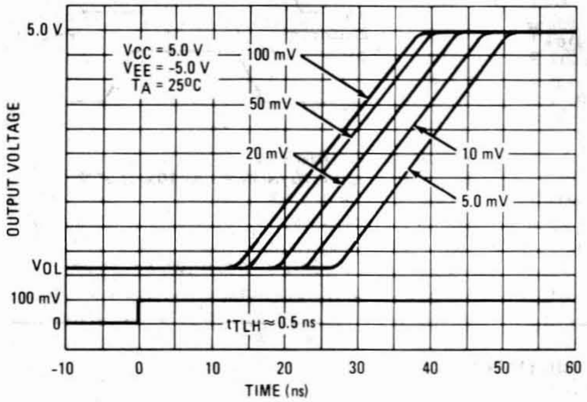


FIGURE 11 – OUTPUT HIGH TO LOW

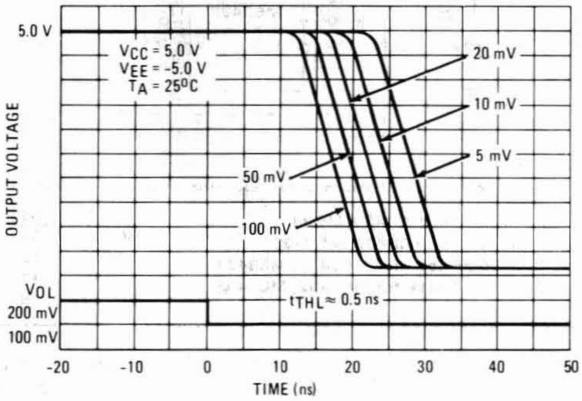


FIGURE 12 – AVERAGE INPUT OFFSET VOLTAGE versus TEMPERATURE

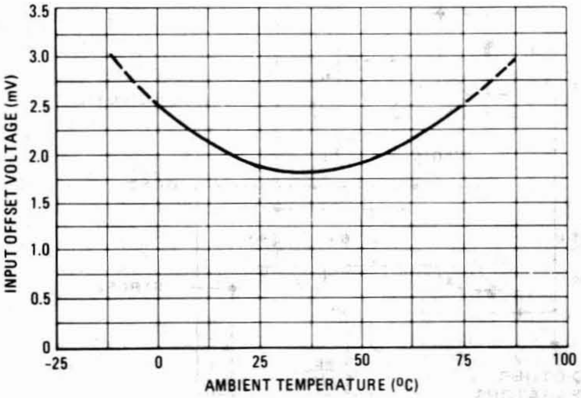
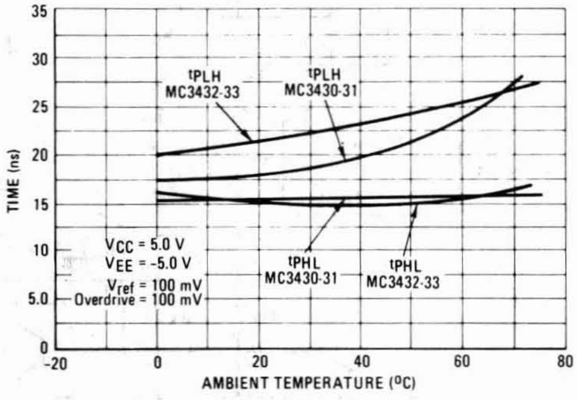


FIGURE 13 – RESPONSE TIME versus TEMPERATURE



## APPLICATIONS INFORMATION

FIGURE 14 – 4-BIT PARALLEL A/D CONVERTER

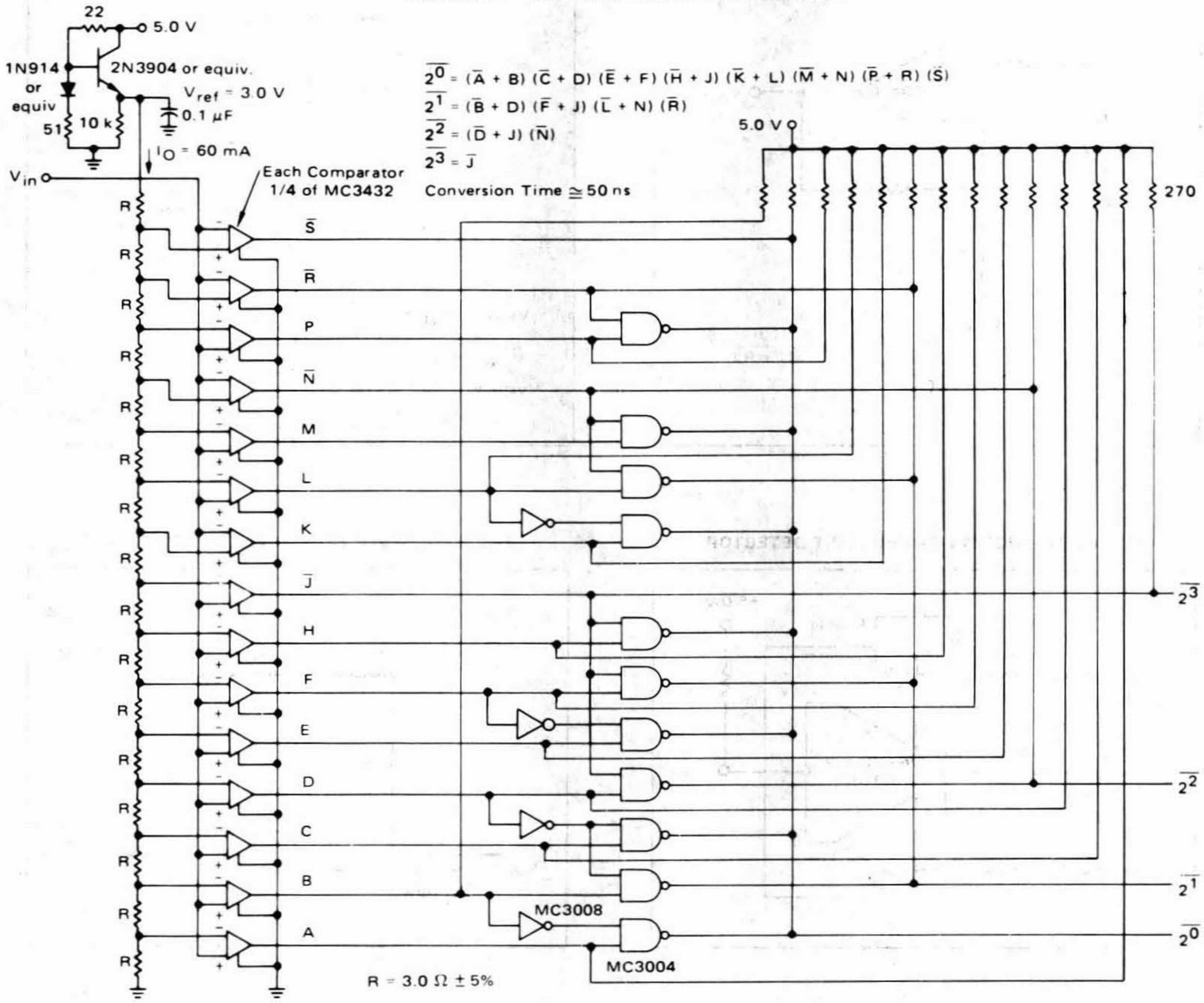
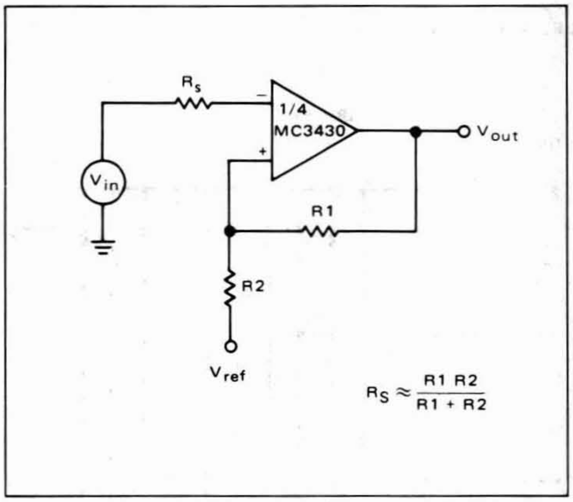
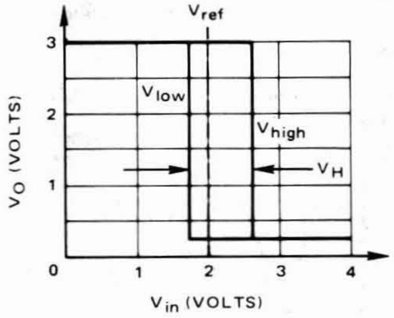

22
5.0 V
1N914 or equiv
2N3904 or equiv.
$V_{ref} = 3.0$ V
0.1 µF
51
10 k
$I_O = 60$ mA
$V_{in}$
Each Comparator 1/4 of MC3432
$\overline{2^0} = (\bar{A} + B)(\bar{C} + D)(\bar{E} + F)(\bar{H} + J)(\bar{K} + L)(\bar{M} + N)(\bar{P} + R)(\bar{S})$
$\overline{2^1} = (\bar{B} + D)(\bar{F} + J)(\bar{L} + N)(\bar{R})$
$\overline{2^2} = (\bar{D} + J)(\bar{N})$
$\overline{2^3} = \bar{J}$
Conversion Time ≅ 50 ns
5.0 V
270
R
$\bar{S}$
$\bar{R}$
P
$\bar{N}$
M
L
K
$\bar{J}$
H
F
E
D
C
B
A
MC3008
MC3004
$\overline{2^3}$
$\overline{2^2}$
$\overline{2^1}$
$\overline{2^0}$
R = 3.0 Ω ± 5%

FIGURE 15 – LEVEL DETECTOR WITH HYSTERESIS


R_s
1/4
MC3430
V_out
V_in
R1
R2
V_ref

$$R_S \approx \frac{R1\,R2}{R1 + R2}$$

FIGURE 16 – TRANSFER CHARACTERISTICS AND EQUATIONS FOR FIGURE 15



$$V_{high} = V_{ref} + \frac{R2\,[V_{O(max)} - V_{REF}]}{R1 + R2}$$

$$V_{low} = V_{ref} + \frac{R2\,[V_{O(min)} - V_{REF}]}{R1 + R2}$$

Hysteresis Loop ($V_h$)

$$V_h = V_{high} - V_{low} = \frac{R2}{R1 + R2}\,[V_{O(max)} - V_{O(min)}]$$

FIGURE 17 – DOUBLE ENDED LIMIT DETECTOR

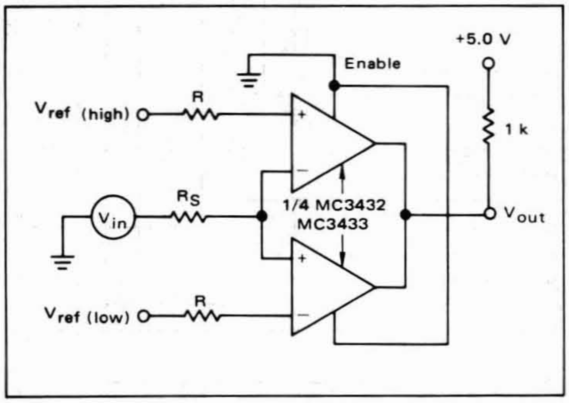
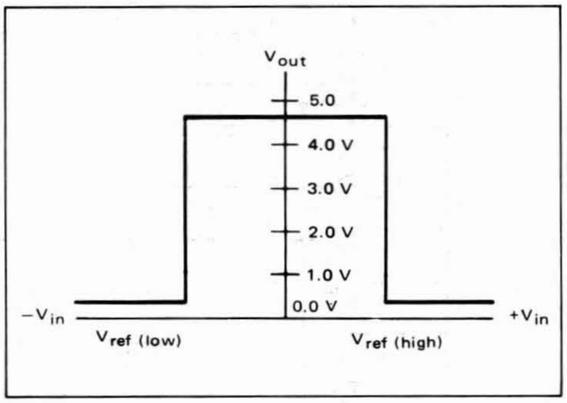

+5.0 V
Enable
V_ref (high)
R
1 k
R_S
V_in
1/4 MC3432
MC3433
V_out
V_ref (low)
R

FIGURE 18 – VOLTAGE TRANSFER FUNCTION



**MOTOROLA**

# MC1455
# MC1555

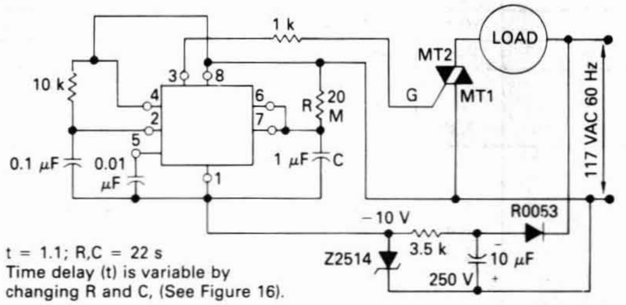
## Specifications and Applications Information

### TIMING CIRCUIT

The MC1555/MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

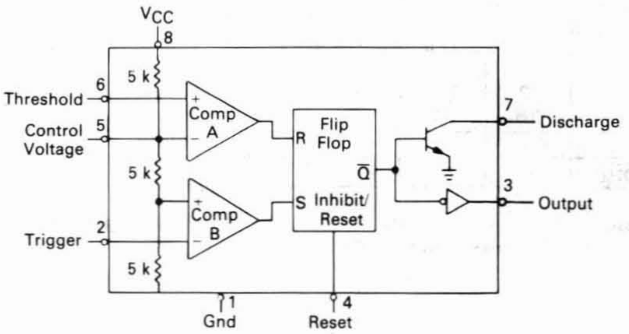
- Direct Replacement for NE555/SE555 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output

FIGURE 1 — 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT


1 k
LOAD
MT2
G
MT1
10 k
3
8
4
2
6
7
R
20 M
5
0.1 μF
0.01 μF
1 μF
C
1
117 VAC 60 Hz
R0053
−10 V
3.5 k
Z2514
10 μF
250 V

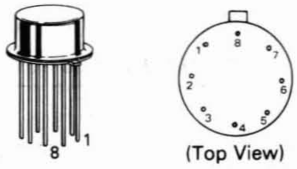
t = 1.1; R,C = 22 s
Time delay (t) is variable by changing R and C, (See Figure 16).

FIGURE 2 — BLOCK DIAGRAM


VCC
8
6
Threshold
5
Control Voltage
2
Trigger
5 k
5 k
5 k
Comp A
Comp B
Flip Flop
R
S
Q̄
Inhibit/ Reset
7
Discharge
3
Output
1
Gnd
4
Reset

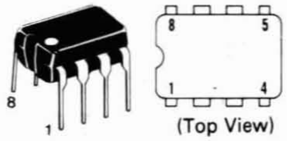
### TIMING CIRCUIT

**SILICON MONOLITHIC INTEGRATED CIRCUIT**


8
1
1
2
3
4
5
6
7
8
(Top View)

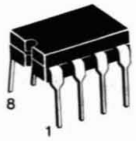
**G SUFFIX**
METAL PACKAGE
CASE 601-04

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. $V_{CC}$


8
1
8
5
1
4
(Top View)

**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(MC1455P1 only)

**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02



**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8

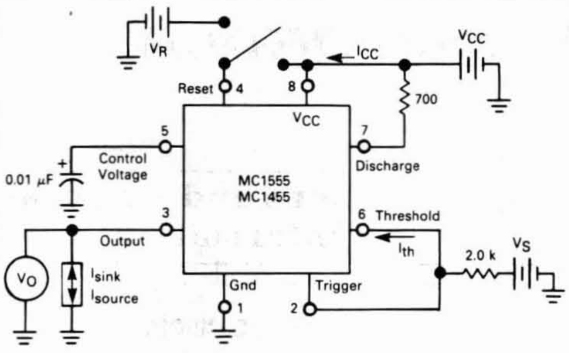
**ORDERING INFORMATION**

| Device | Alternate | Temperature Range | Package |
|---|---|---|---|
| MC1455G | — | 0°C to +70°C | Metal Can |
| MC1455P1 | NE555V | 0°C to +70°C | Plastic DIP |
| MC1455D | — | 0°C to +70°C | SO-8 |
| MC1455U | — | 0°C to +70°C | Ceramic DIP |
| MC1455BP1 | — | −40°C to +85°C | Plastic DIP |
| MC1555G | — | −55°C to +125°C | Metal Can |
| MC1555U | SE555 | −55°C to +125°C | Ceramic DIP |

## MAXIMUM RATINGS ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +18 | Vdc |
| Discharge Current (Pin 7) | $I_7$ | 200 | mA |
| Power Dissipation (Package Limitation) | $P_D$ | | |
| Metal Can | | 680 | mW |
| Derate above $T_A$ = +25°C | | 4.6 | mW/°C |
| Plastic Dual In-Line Package | | 625 | mW |
| Derate above $T_A$ = +25°C | | 5.0 | mW/°C |
| Operating Temperature Range (Ambient) | $T_A$ | | °C |
| MC1555 | | −55 to +125 | |
| MC1455B | | −40 to +85 | |
| MC1455 | | 0 to +70 | |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

### FIGURE 3 — GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters: (to set output and measure parameters)

a) When $V_S \geqslant 2/3\ V_{CC}$, $V_O$ is low.

b) When $V_S \leqslant 1/3\ V_{CC}$, $V_O$ is high.

c) When $V_O$ is low, pin 7 sinks current. To test for Reset, set $V_O$, high, apply Reset voltage, and test for current flowing into pin 7. When Reset is not in use, it should be tied to $V_{CC}$.

## ELECTRICAL CHARACTERISTICS ($T_A$ = +25°C, $V_{CC}$ = +5.0 V to +15 V unless otherwise noted.)

| Characteristics | Symbol | MC1555 | | | MC1455 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supply Voltage | $V_{CC}$ | 4.5 | – | 18 | 4.5 | – | 16 | V |
| Supply Current | $I_{CC}$ | | | | | | | mA |
| $V_{CC}$ = 5.0 V, $R_L = \infty$ | | – | 3.0 | 5.0 | – | 3.0 | 6.0 | |
| $V_{CC}$ = 15 V, $R_L = \infty$ | | – | 10 | 12 | – | 10 | 15 | |
| Low State, (Note 1) | | | | | | | | |
| Timing Error (Note 2) | | | | | | | | |
| R = 1.0 kΩ to 100 kΩ | | | | | | | | |
| Initial Accuracy C = 0.1 µF | | – | 0.5 | 2.0 | – | 1.0 | – | % |
| Drift with Temperature | | – | 30 | 100 | – | 50 | – | PPM/°C |
| Drift with Supply Voltage | | – | 0.05 | 0.20 | – | 0.10 | – | %/Volt |
| Threshold Voltage | $V_{th}$ | – | 2/3 | – | – | 2/3 | – | $xV_{CC}$ |
| Trigger Voltage | $V_T$ | | | | | | | V |
| $V_{CC}$ = 15 V | | 4.8 | 5.0 | 5.2 | – | 5.0 | – | |
| $V_{CC}$ = 5.0 V | | 1.45 | 1.67 | 1.9 | – | 1.67 | – | |
| Trigger Current | $I_T$ | – | 0.5 | – | – | 0.5 | – | µA |
| Reset Voltage | $V_R$ | 0.4 | 0.7 | 1.0 | 0.4 | 0.7 | 1.0 | V |
| Reset Current | $I_R$ | – | 0.1 | – | – | 0.1 | – | mA |
| Threshold Current (Note 3) | $I_{th}$ | – | 0.1 | 0.25 | – | 0.1 | 0.25 | µA |
| Discharge Leakage Current (Pin 7) | $I_{dis}$ | – | – | 100 | – | – | 100 | nA |
| Control Voltage Level | $V_{CL}$ | | | | | | | V |
| $V_{CC}$ = 15 V | | 9.6 | 10 | 10.4 | 9.0 | 10 | 11 | |
| $V_{CC}$ = 5.0 V | | 2.9 | 3.33 | 3.8 | 2.6 | 3.33 | 4.0 | |
| Output Voltage Low | $V_{OL}$ | | | | | | | |
| ($V_{CC}$ = 15 V) | | | | | | | | V |
| $I_{sink}$ = 10 mA | | – | 0.1 | 0.15 | – | 0.1 | 0.25 | |
| $I_{sink}$ = 50 mA | | – | 0.4 | 0.5 | – | 0.4 | 0.75 | |
| $I_{sink}$ = 100 mA | | – | 2.0 | 2.2 | – | 2.0 | 2.5 | |
| $I_{sink}$ = 200 mA | | – | 2.5 | – | – | 2.5 | – | |
| ($V_{CC}$ = 5.0 V) | | | | | | | | |
| $I_{sink}$ = 8.0 mA | | – | 0.1 | 0.25 | – | – | – | |
| $I_{sink}$ = 5.0 mA | | – | – | – | – | 0.25 | 0.35 | |
| Output Voltage High | $V_{OH}$ | | | | | | | V |
| ($I_{source}$ = 200 mA) | | | | | | | | |
| $V_{CC}$ = 15 V | | – | 12.5 | – | – | 12.5 | – | |
| ($I_{source}$ = 100 mA) | | | | | | | | |
| $V_{CC}$ = 15 V | | 13 | 13.3 | – | 12.75 | 13.3 | – | |
| $V_{CC}$ = 5.0 V | | 3.0 | 3.3 | – | 2.75 | 3.3 | – | |
| Rise Time of Output | $t_{OLH}$ | – | 100 | – | – | 100 | – | ns |
| Fall Time of Output | $t_{OHL}$ | – | 100 | – | – | 100 | – | ns |

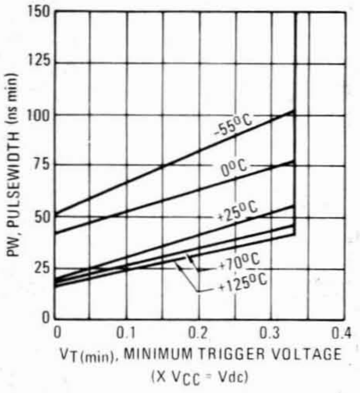
NOTES:

1. Supply current when output is high is typically 1.0 mA less.
2. Tested at $V_{CC}$ = 5.0 V and $V_{CC}$ = 15 V. Monostable mode
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

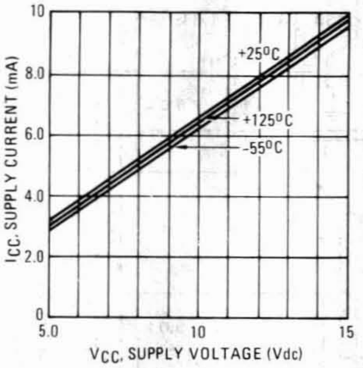
## TYPICAL CHARACTERISTICS

($T_A$ = +25°C unless otherwise noted.)

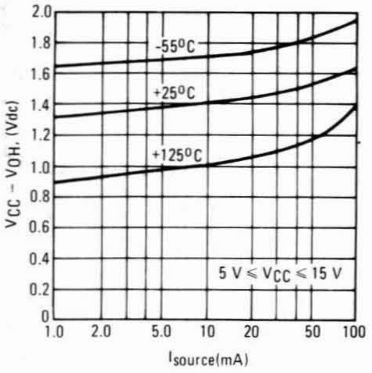
### FIGURE 4 — TRIGGER PULSE WIDTH



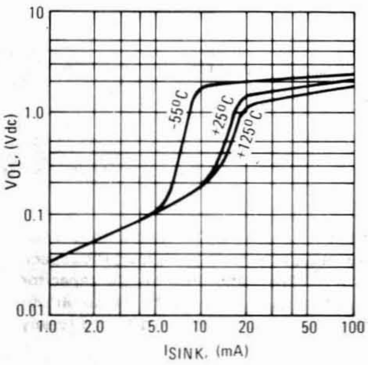
### FIGURE 5 — SUPPLY CURRENT



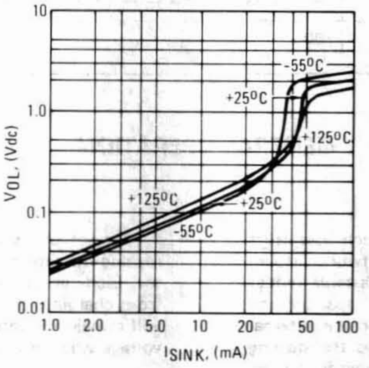
### FIGURE 6 — HIGH OUTPUT VOLTAGE



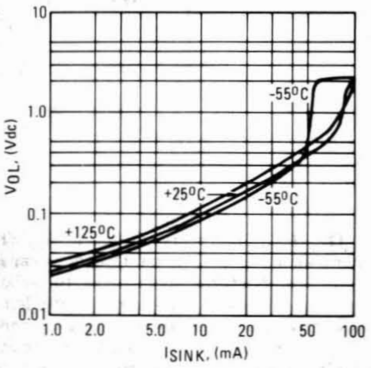
### FIGURE 7 — LOW OUTPUT VOLTAGE @ $V_{CC}$ = 5.0 Vdc



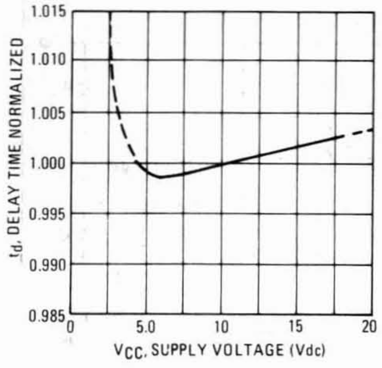
### FIGURE 8 — LOW OUTPUT VOLTAGE @ $V_{CC}$ = 10 Vdc



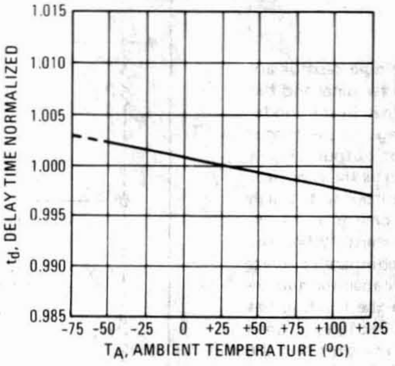
### FIGURE 9 — LOW OUTPUT VOLTAGE @ $V_{CC}$ = 15 Vdc



### FIGURE 10 — DELAY TIME versus SUPPLY VOLTAGE



### FIGURE 11 — DELAY TIME versus TEMPERATURE



### FIGURE 12 — PROPAGATION DELAY versus TRIGGER VOLTAGE

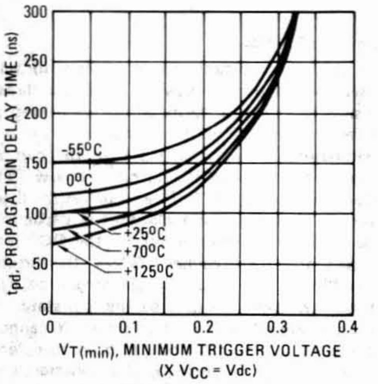
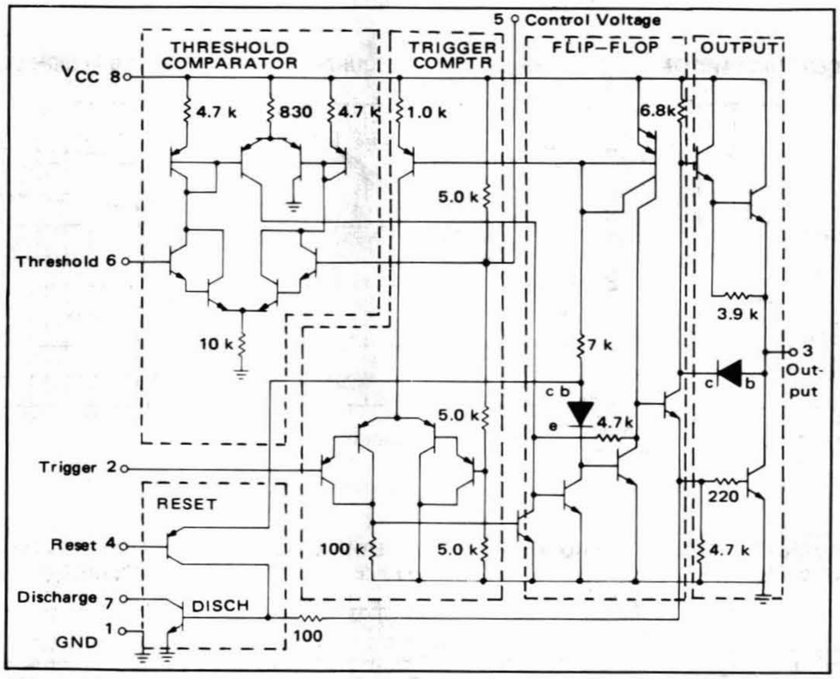


FIGURE 13 — REPRESENTATIVE CIRCUIT SCHEMATIC


5 Control Voltage
THRESHOLD COMPARATOR
TRIGGER COMPTR
FLIP–FLOP
OUTPUT
$V_{CC}$ 8
4.7 k
830
4.7 k
1.0 k
6.8k
5.0 k
Threshold 6
3.9 k
10 k
7 k
3 Output
c b
e
4.7k
c
b
5.0 k
Trigger 2
RESET
220
Reset 4
100 k
5.0 k
4.7 k
Discharge 7
DISCH
GND 1
100

## GENERAL OPERATION

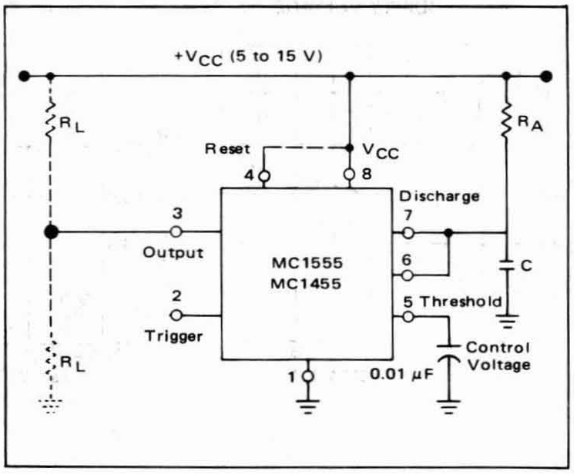
The MC1555 is a monolithic timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

**Monostable Mode**

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 $V_{CC}$ the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 $V_{CC}$ the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

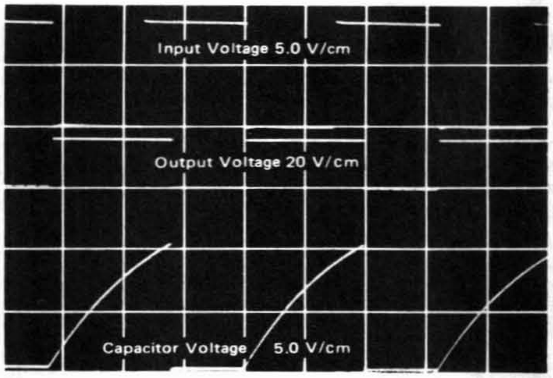
A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

FIGURE 14 — MONOSTABLE CIRCUIT


+$V_{CC}$ (5 to 15 V)
$R_L$
$R_A$
Reset
$V_{CC}$
4
8
Discharge
7
3
Output
MC1555
MC1455
6
C
2
5 Threshold
Trigger
Control Voltage
$R_L$
1
0.01 µF

## GENERAL OPERATION (continued)

**FIGURE 15 — MONOSTABLE WAVEFORMS**



t = 50 µs/cm
($R_A$ = 10 kΩ, C = 0.01 µF, $R_L$ = 1.0 kΩ, $V_{CC}$ = 15 V)

**FIGURE 16 — TIME DELAY**

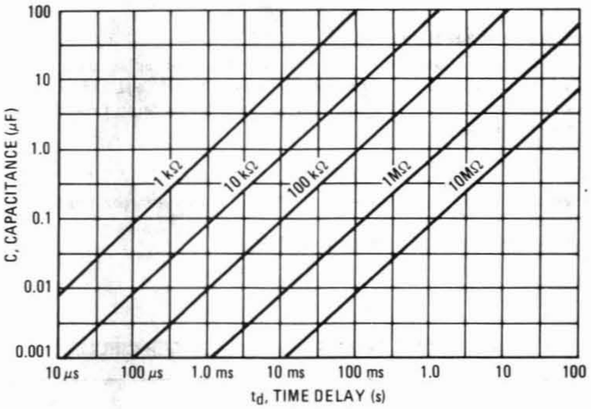


**FIGURE 17 — ASTABLE CIRCUIT**

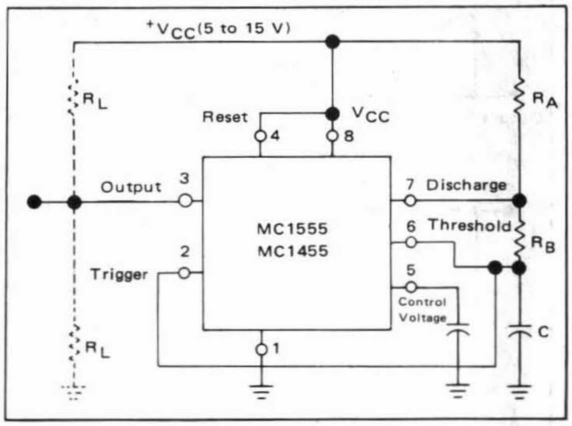
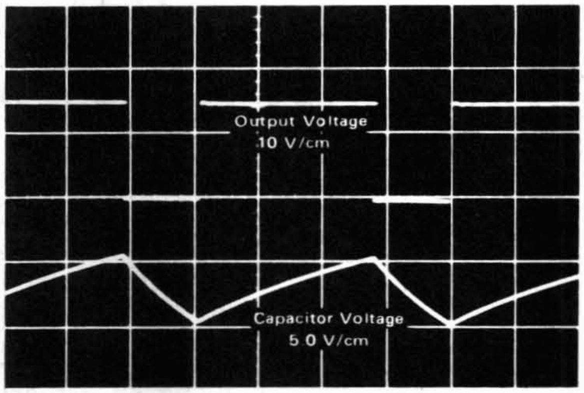


**FIGURE 18 — ASTABLE WAVEFORMS**



t = 20 µs/cm

($R_A$ = 5.1 kΩ, C = 0.01 µF, $R_L$ = 1.0 kΩ;
$R_B$ = 3.9 kΩ, $V_{CC}$ = 15 V)

### Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 $V_{CC}$ and 2/3 $V_{CC}$. See Figure 17.

The external capacitor charges to 2/3 $V_{CC}$ through $R_A$ and $R_B$ and discharges to 1/3 $V_{CC}$ through $R_B$. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695\,(R_A+R_B)\,C$

The discharge time (output low) by: $t_2 = 0.695\,(R_B)\,C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695\,(R_A+2R_B)\,C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B)\,C}$

and may be easily found as shown in Figure 19.

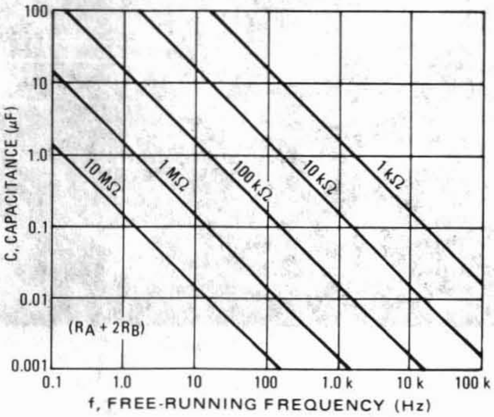
The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle $R_A$ must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of $R_A$ is given by:

$$R_A \geqslant \frac{V_{CC}\ (\text{Vdc})}{I_7\ (\text{A})} \geqslant \frac{V_{CC}\ (\text{Vdc})}{0.2}$$

**FIGURE 19 — FREE-RUNNING FREQUENCY**



## APPLICATIONS INFORMATION

**Linear Voltage Ramp**

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from 0 to 2/3 $V_{CC}$. The linear ramp time is given by $t = \frac{2}{3}\frac{V_{CC}}{I}$

where $I = \frac{V_{CC} - V_B - V_{BE}}{R_E}$. If $V_B$ is much larger than $V_{BE}$, then t can be made independent of $V_{CC}$.

**Missing Pulse Detector**

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.

FIGURE 20 — LINEAR VOLTAGE SWEEP CIRCUIT

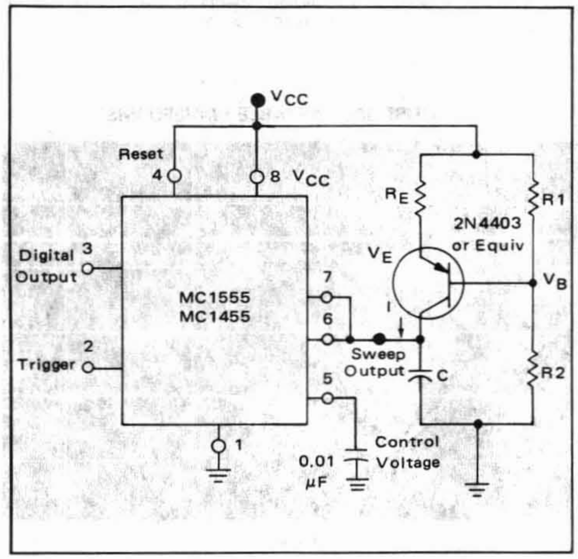

VCC
Reset
4
8 VCC
RE
R1
2N4403
or Equiv
Digital Output
3
VE
VB
MC1555
MC1455
7
6
I
Sweep Output
C
2
Trigger
5
R2
1
Control Voltage
0.01 µF

FIGURE 22

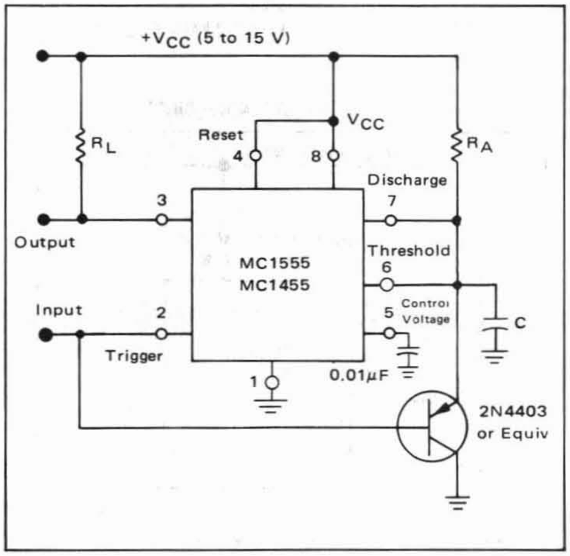

+VCC (5 to 15 V)
RL
Reset
4
8
VCC
RA
Discharge
7
3
Output
Threshold
6
MC1555
MC1455
Input
2
5
Control Voltage
C
Trigger
1
0.01µF
2N4403
or Equiv

FIGURE 21 — LINEAR VOLTAGE RAMP WAVEFORMS
($R_E$ = 10 kΩ, R2 = 100 kΩ, R1 = 39 kΩ, C = 0.01 µF, $V_{CC}$ = 15 V)

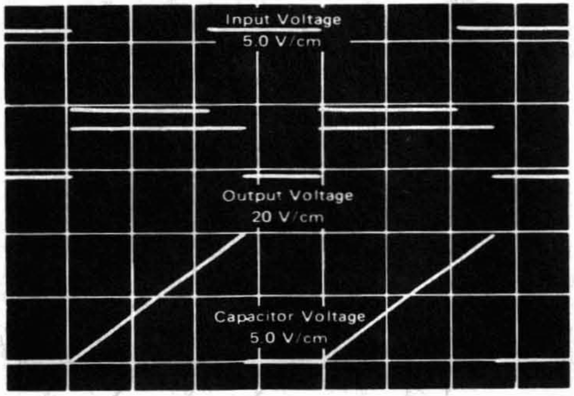
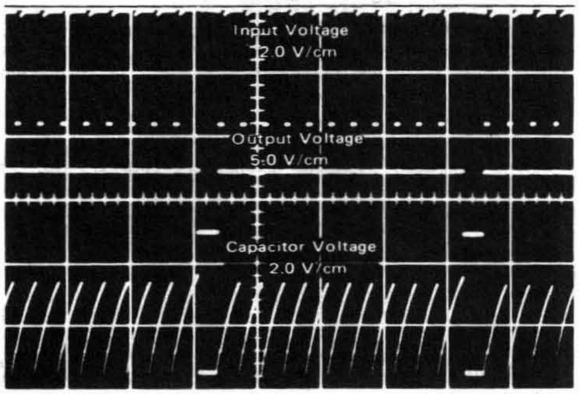


FIGURE 23 — MISSING PULSE DETECTOR WAVEFORMS
($R_A$ = 2.0 kΩ, $R_L$ = 1.0 kΩ, C = 0.1 µF, $V_{CC}$ = 15 V)



## APPLICATIONS INFORMATION (continued)

**Pulse Width Modulation**

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

**FIGURE 24**

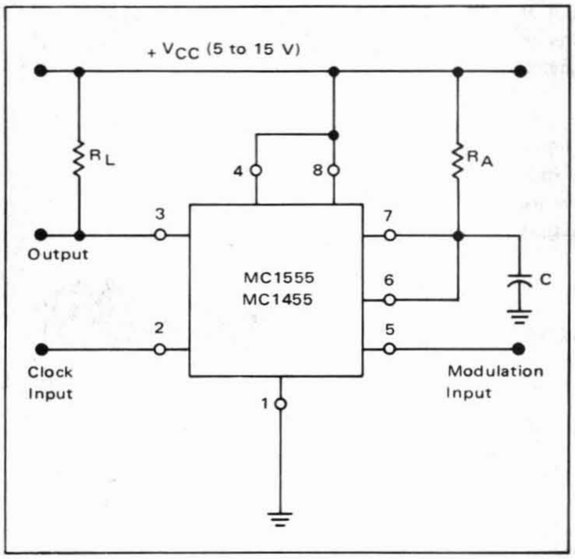
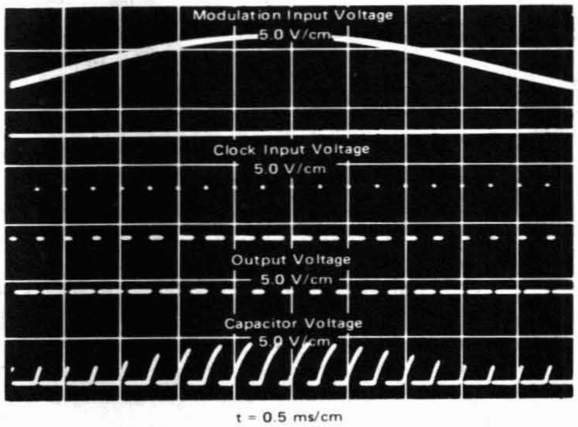

+ $V_{CC}$ (5 to 15 V)
$R_L$
$R_A$
4
8
3
7
Output
MC1555
MC1455
6
C
2
5
Clock Input
Modulation Input
1

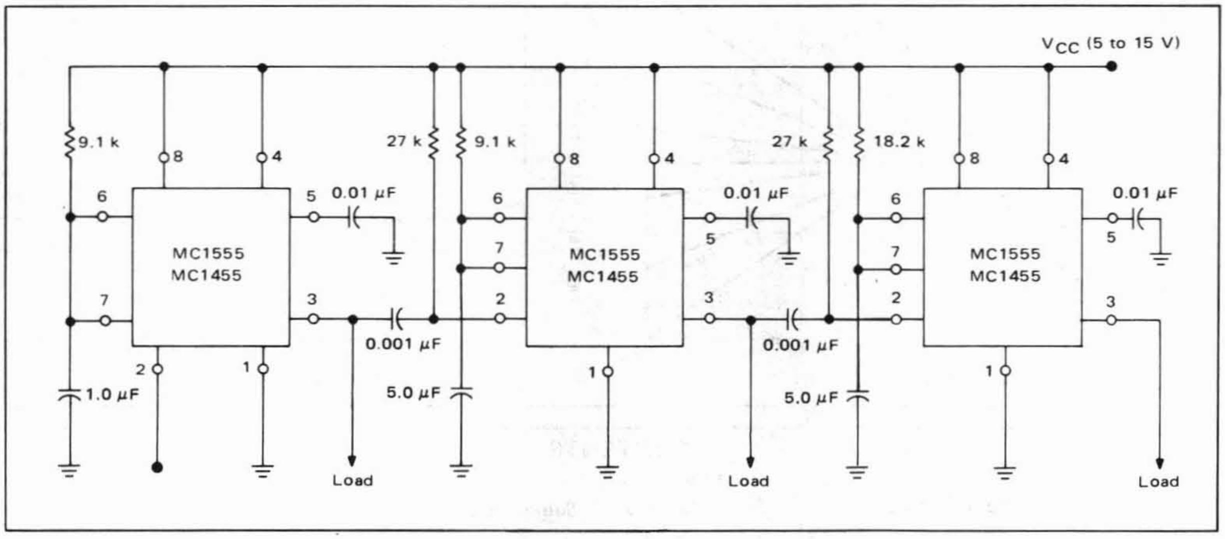
**FIGURE 25 — PULSE WIDTH MODULATION WAVEFORMS ($R_A$ = 10 kΩ, C = 0.02 µF, $V_{CC}$ = 15 V)**



**Test Sequences**

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

**FIGURE 26**


$V_{CC}$ (5 to 15 V)
9.1 k
8
4
6
5
0.01 µF
MC1555
MC1455
7
3
2
1
1.0 µF
0.001 µF
Load
27 k
9.1 k
5.0 µF
8
4
6
7
0.01 µF
5
MC1555
MC1455
2
3
1
0.001 µF
Load
27 k
18.2 k
5.0 µF
8
4
6
7
2
0.01 µF
5
MC1555
MC1455
3
1
Load

MOTOROLA

# MC1494L
# MC1594L

## Specifications and Applications Information

## LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

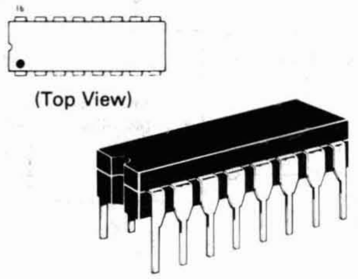
**SILICON MONOLITHIC EPITAXIAL PASSIVATED**

### MONOLITHIC FOUR-QUADRANT MULTIPLIER

. . . designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

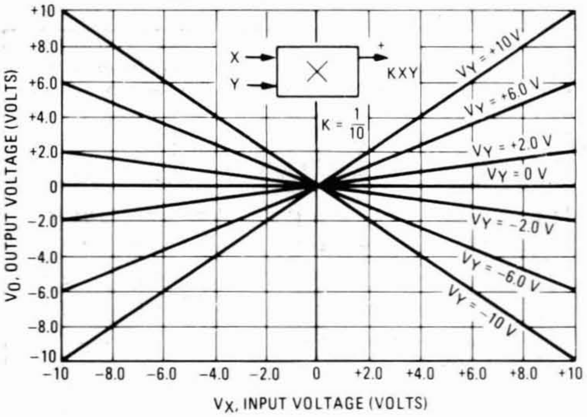
The MC1594/1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

- Operates With ± 15 V Supplies
- Excellent Linearity – Maximum Error (X or Y): ± 0.5% (MC1594)
  ± 1.0% (MC1494)
- Wide Input Voltage Range – ± 10 volts
- Adjustable Scale Factor, K (0.1 nominal)
- Single-Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small-Signal) – 1.0 MHz
- Power Supply Sensitivity – 30 mV/V typical

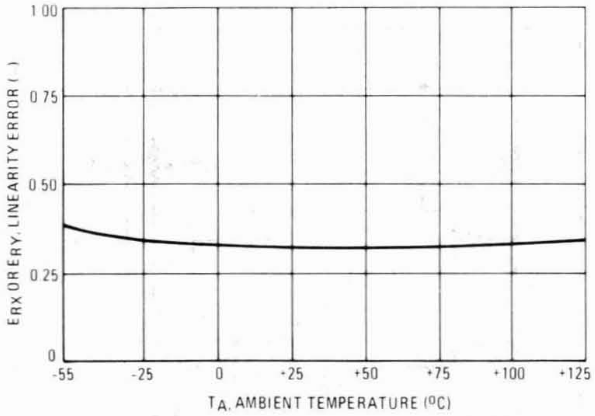


CERAMIC PACKAGE
CASE 620-02

FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC



TYPICAL LINEARITY ERROR versus TEMPERATURE



### CONTENTS

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| **Electrical Characteristics** | 2 | DC Applications | 9 |
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| Circuit Description | 5 | General Information Index | 14 |
| **Circuit Schematic** | 5 | | |
| DC Operation | 6 | | |

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V^+$ | +18 | Vdc |
| | $V^-$ | -18 | |
| Differential Input Signal | $V_9 - V_6$ | $\pm\|6 + I_1 R_Y\| < 30$ | Vdc |
| | $V_{10} - V_{13}$ | $\pm\|6 + I_1 R_X\| < 30$ | |
| Common-Mode Input Voltage | | | Vdc |
| $V_{CMY} = V_9 = V_6$ | $V_{CMY}$ | ±11.5 | |
| $V_{CMX} = V_{10} = V_{13}$ | $V_{CMX}$ | ±11.5 | |
| Power Dissipation (Package Limitation) | | | |
| $T_A$ = +25°C | $P_D$ | 750 | mW |
| Derate above $T_A$ = +25°C | $1/\theta_{JA}$ | 5.0 | mW/°C |
| Operating Temperature Range | $T_A$ | | °C |
| MC1594 | | -55 to +125 | |
| MC1494 | | 0 to + 70 | |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V^+$ = +15 V, $V^-$ = -15 V, $T_A$ = +25°C, R1 = 16 kΩ, $R_X$ = 30 kΩ, $R_Y$ = 62 kΩ, $R_L$ = 47 kΩ, unless otherwise noted)

| Characteristic | Fig. | Symbol | MC1594 | | | MC1494 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Linearity | 1 | $E_{RX}$ or $E_{RY}$ | | | | | | | % |
| Output error in Percent of full scale | | | | | | | | | |
| $-10\text{ V} < V_x < +10\text{ V}$ ($V_y = \pm 10$ V) | | | | | | | | | |
| $-10\text{ V} < V_y < +10\text{ V}$ ($V_x = \pm 10$ V) | | | | | | | | | |
| $T_A$ = +25°C | | | – | ± 0.3 | ± 0.5 | – | ± 0.5 | ± 1.0 | |
| $T_A = T_{high}$ ① | | | – | – | ± 0.8 | – | – | ± 1.3 | |
| $T_A = T_{low}$ ② | | | – | – | ± 0.8 | – | – | ± 1.3 | |
| Input | 2,3,4 | | | | | | | | |
| Voltage Range ($V_X = V_Y = V_{in}$) | | $V_{in}$ | ±10 | – | – | ±10 | – | – | $V_{pk}$ |
| Resistance (X or Y Input) | | $R_{in}$ | – | 300 | – | – | 300 | – | MΩ |
| Offset Voltage (X Input) (Note 1) | | $\|V_{iox}\|$ | – | 0.1 | 1.6 | – | 0.2 | 2.5 | V |
| (Y Input) (Note 1) | | $\|V_{ioy}\|$ | – | 0.4 | 1.6 | – | 0.8 | 2.5 | |
| Bias Current (X or Y Input) | | $I_b$ | – | 0.5 | 1.5 | – | 1.0 | 2.5 | µA |
| Offset Current (X or Y Input) | | $\|I_{io}\|$ | – | 28 | 150 | – | 50 | 400 | nA |
| Output | 3,4 | | | | | | | | |
| Voltage Swing Capability | | $V_o$ | ±10 | – | – | ±10 | – | – | $V_{pk}$ |
| Impedance | | $R_o$ | – | 850 | – | – | 850 | – | kΩ |
| Offset Voltage (Note 1) | | $\|V_{oo}\|$ | – | 0.8 | 1.6 | – | 1.2 | 2.5 | V |
| Offset Current (Note 1) | | $\|I_{oo}\|$ | – | 17 | 34 | – | 25 | 52 | µA |
| Temperature Stability (Drift) | | | | | | | | | |
| $T_A = T_{high}$ to $T_{low}$ | | | | | | | | | |
| Output Offset (X = 0, Y = 0) Voltage | | $\|TCV_{oo}\|$ | – | 1.3 | – | – | 1.3 | – | mV/°C |
| Current | | $\|TCI_{oo}\|$ | – | 27 | – | – | 27 | – | nA/°C |
| X Input Offset (Y = 0) | | $\|TCV_{iox}\|$ | – | 0.3 | – | – | 0.3 | – | mV/°C |
| Y Input Offset (X = 0) | | $\|TCV_{ioy}\|$ | – | 1.5 | – | – | 1.5 | – | |
| Scale Factor | | $\|TCK\|$ | – | 0.07 | – | – | 0.07 | – | %/°C |
| Total dc Accuracy Drift (X = 10, Y = 10) | | $\|TCE\|$ | – | 0.09 | – | – | 0.09 | – | |
| Dynamic Response | 5 | | | | | | | | |
| Small Signal (3 dB) X | | $BW_{3\,dB(X)}$ | – | 0.8 | – | – | 0.8 | – | MHz |
| Y | | $BW_{3\,dB(Y)}$ | – | 1.0 | – | – | 1.0 | – | |
| Power Bandwidth (47 k) | | $P_{BW}$ | – | 440 | – | – | 440 | – | kHz |
| 3° Relative Phase Shift | | $f_\phi$ | – | 240 | – | – | 240 | – | |
| 1% Absolute Error | | $f_\theta$ | – | 30 | – | – | 30 | – | |
| Common Mode | 6 | | | | | | | | |
| Input Swing (X or Y) | | CMV | ±10.5 | – | – | ±10.5 | – | – | $V_{pk}$ |
| Gain (X or Y) | | $A_{CM}$ | – | -65 | – | – | -65 | – | dB |
| Power Supply | 7 | | | | | | | | |
| Current | | $I_d^+$ | – | 6.0 | 9.0 | – | 6.0 | 12 | mAdc |
| | | $I_d^-$ | – | 6.5 | 9.0 | – | 6.5 | 12 | |
| Quiescent Power Dissipation | | $P_d$ | – | 185 | 260 | – | 185 | 350 | mW |
| Sensitivity | | $S^+$ | – | 13 | 50 | – | 13 | 100 | mV/V |
| | | $S^-$ | – | 30 | 100 | – | 30 | 200 | |
| Regulated Offset Adjust Voltages | 7 | | | | | | | | |
| Positive | | $V_R^+$ | +3.5 | +4.3 | +5.0 | +3.5 | +4.3 | +5.0 | Vdc |
| Negative | | $V_R^-$ | -3.5 | -4.3 | -5.0 | -3.5 | -4.3 | -5.0 | |
| Temperature Coefficient ($V_R^+$ or $V_R^-$) | | $TCV_R$ | – | 0.03 | – | – | 0.03 | – | mV/°C |
| Power Supply Sensitivity ($V_R^+$ or $V_R^-$) | | $S_R^+, S_R^-$ | – | 0.6 | – | – | 0.6 | – | mV/V |

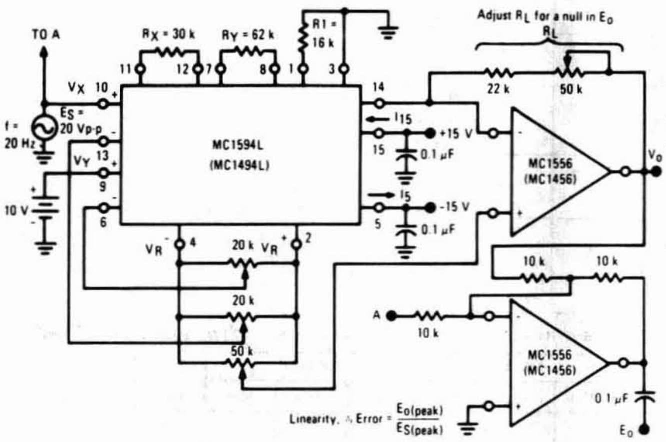
Note 1: Offsets can be adjusted to zero with external potentiometers.

① $T_{high}$ = +125°C for MC1594
+ 70°C for MC1494

② $T_{low}$ = - 55°C for MC1594
0°C for MC1494

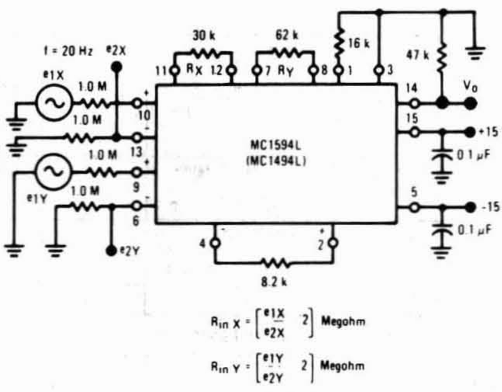
## TEST CIRCUITS

### FIGURE 1 – LINEARITY


TO A
RX = 30 k
RY = 62 k
R1 = 16 k
Adjust RL for a null in Eo
RL
22 k
50 k
VX
ES = 20 Vp-p
f = 20 Hz
VY
10 V
MC1594L
(MC1494L)
I15
+15 V
0.1 μF
I5
-15 V
MC1556
(MC1456)
Vo
VR-
VR+
20 k
50 k
10 k
A
Eo

$$\text{Linearity, \% Error} = \frac{E_{o(peak)}}{E_{S(peak)}}$$

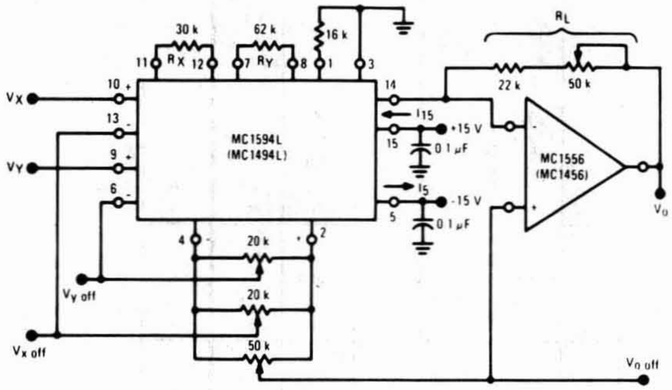
### FIGURE 2 – INPUT RESISTANCE


f = 20 Hz
e2X
e1X
1.0 M
e1Y
e2Y
30 k
62 k
16 k
47 k
RX
RY
Vo
MC1594L
(MC1494L)
+15 V
0.1 μF
-15 V
8.2 k

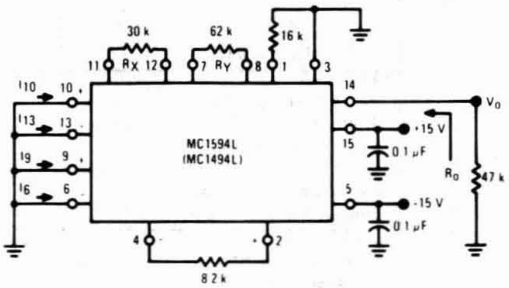
$$R_{in}\,X = \left[\frac{e1X}{e2X}\quad 2\right]\ \text{Megohm}$$

$$R_{in}\,Y = \left[\frac{e1Y}{e2Y}\quad 2\right]\ \text{Megohm}$$

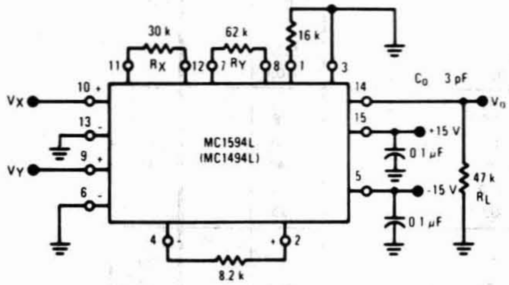
### FIGURE 3 – OFFSET VOLTAGES, GAIN


30 k
62 k
16 k
RX
RY
RL
22 k
50 k
VX
VY
MC1594L
(MC1494L)
I15
+15 V
0.1 μF
I5
-15 V
MC1556
(MC1456)
Vo
20 k
50 k
Vy off
Vx off
Vo off

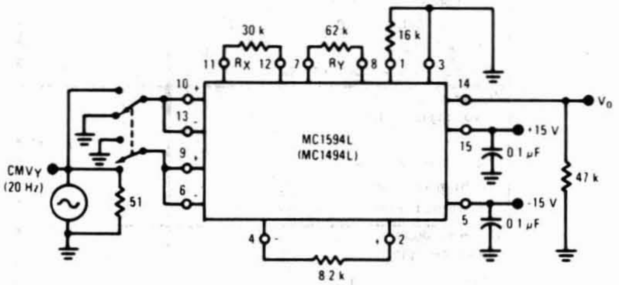
### FIGURE 4 – INPUT BIAS CURRENT/INPUT OFFSET CURRENT, OUTPUT RESISTANCE


30 k
62 k
16 k
RX
RY
I10
I13
I9
I6
MC1594L
(MC1494L)
Vo
+15 V
0.1 μF
-15 V
Ro
47 k
8.2 k

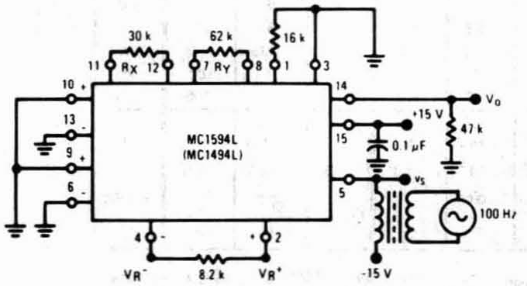
### FIGURE 5 – FREQUENCY RESPONSE


30 k
62 k
16 k
RX
RY
Co 3 pF
VX
VY
MC1594L
(MC1494L)
Vo
+15 V
0.1 μF
-15 V
47 k
RL
8.2 k

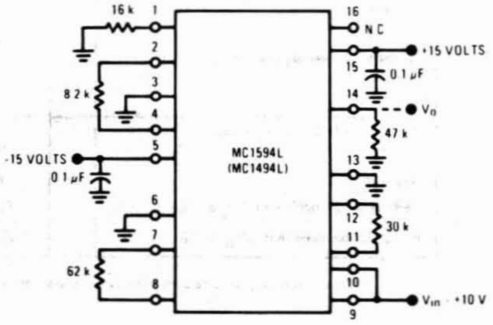
### FIGURE 6 – COMMON MODE


30 k
62 k
16 k
RX
RY
CMVY
(20 Hz)
51
MC1594L
(MC1494L)
Vo
+15 V
0.1 μF
-15 V
47 k
8.2 k

### FIGURE 7 – POWER-SUPPLY SENSITIVITY


30 k
62 k
16 k
RX
RY
MC1594L
(MC1494L)
Vo
+15 V
47 k
0.1 μF
vs
100 Hz
-15 V
VR-
8.2 k
VR+

### FIGURE 8 – BURN-IN


16 k
N.C.
+15 VOLTS
0.1 μF
Vo
8.2 k
47 k
-15 VOLTS
0.1 μF
MC1594L
(MC1494L)
30 k
62 k
Vin = +10 V

## TYPICAL CHARACTERISTICS

(Unless otherwise noted, $V^+ = +15$ V, $V^- = -15$ V, R1 = 16 kΩ, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, $R_L = 47$ kΩ, $T_A = +25°C$)

FIGURE 9 – FREQUENCY RESPONSE OF Y INPUT versus LOAD RESISTANCE

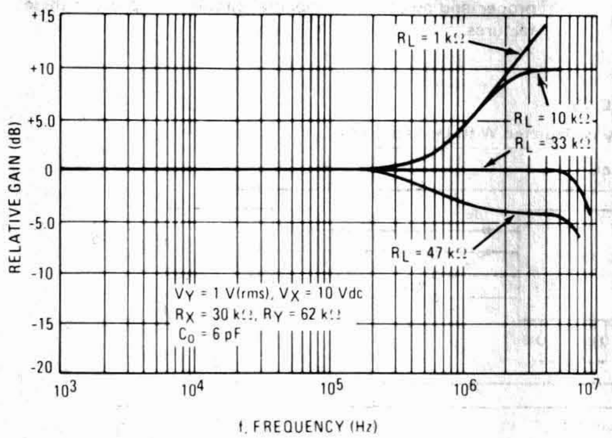


FIGURE 10 – FREQUENCY RESPONSE OF X INPUT versus LOAD RESISTANCE

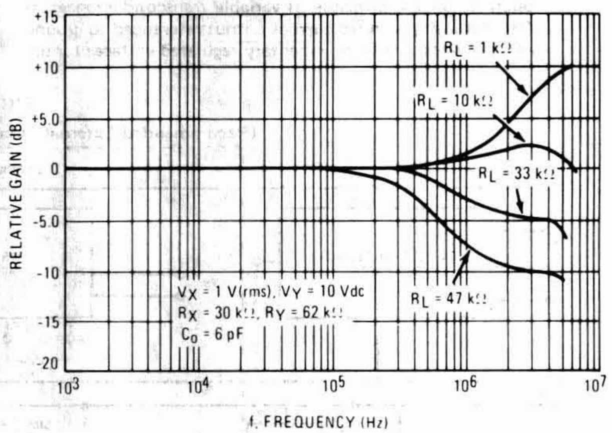


FIGURE 11 – LARGE SIGNAL VOLTAGE versus FREQUENCY

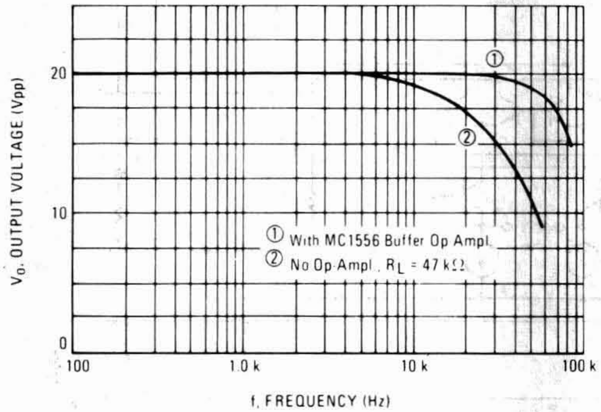


FIGURE 12 – LINEARITY versus $R_X$ OR $R_Y$ WITH K = 1/10

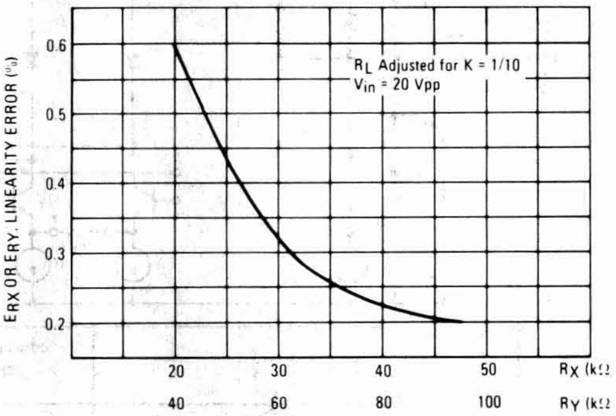


FIGURE 13 – LINEARITY versus $R_X$ OR $R_Y$ WITH K = 1

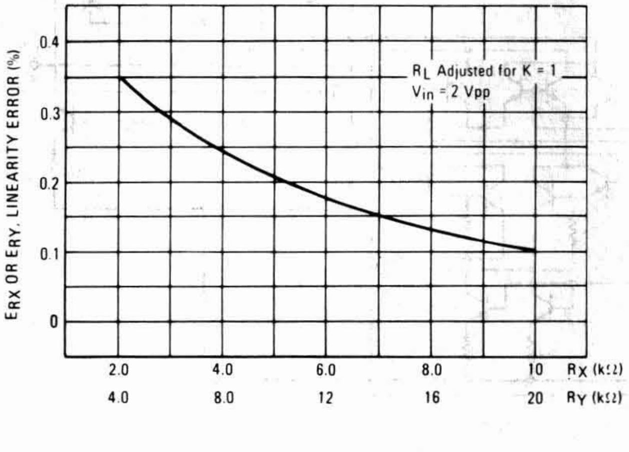
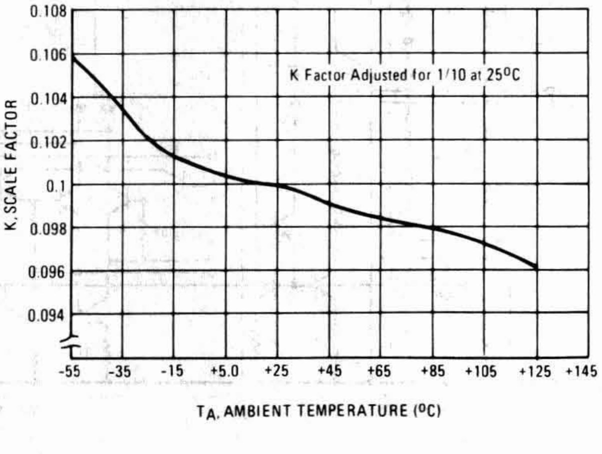


FIGURE 14 – SCALE FACTOR (K) versus TEMPERATURE



## GENERAL INFORMATION

### 1. CIRCUIT DESCRIPTION

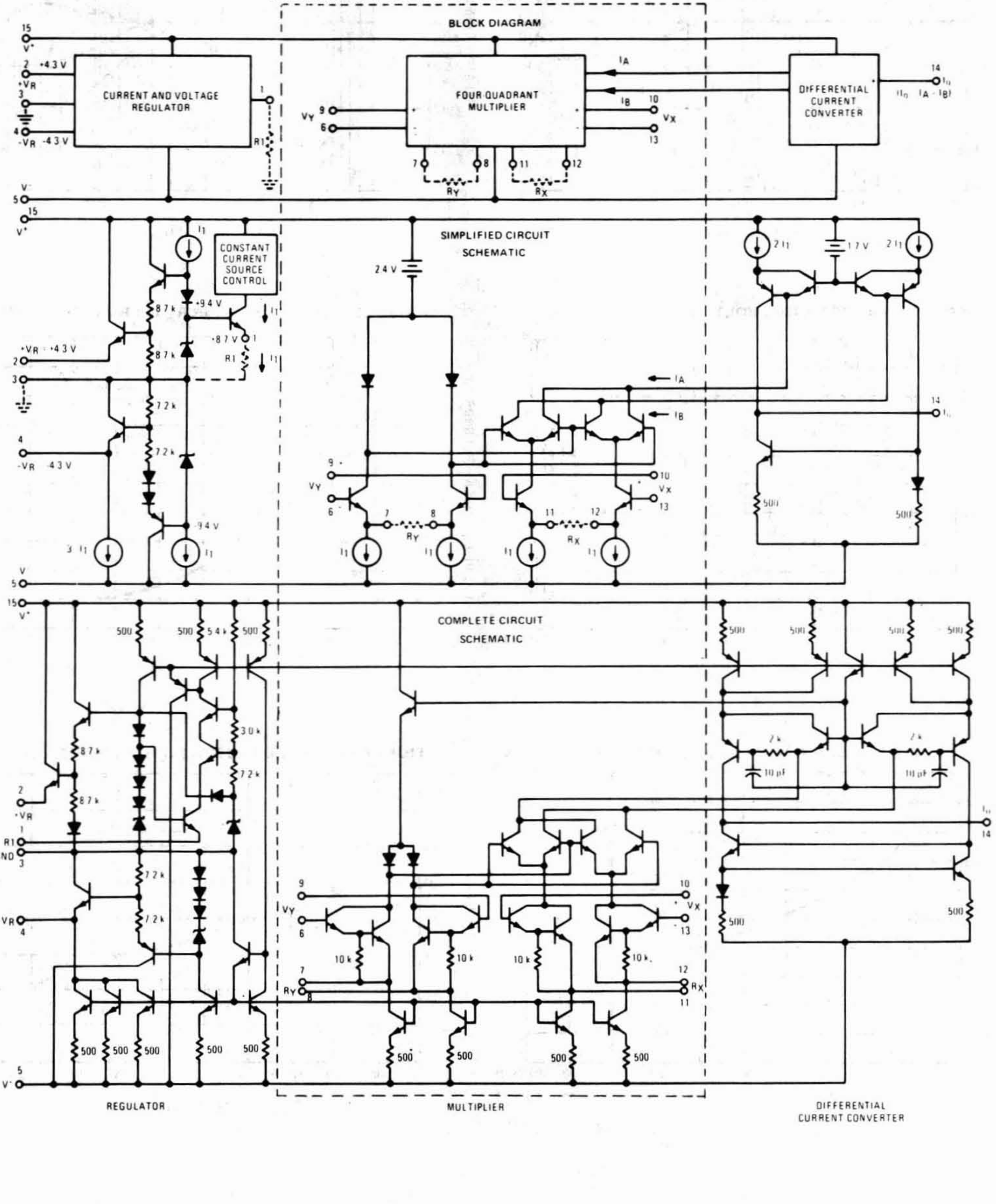
### 1.1 Introduction

The MC1594 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a single-ended current output referenced to ground and provides two complementary regulated voltages for use with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltage.

As shown in Figure 15, the MC1594 consists of a multiplier proper and associated peripheral circuitry to provide these features.

**FIGURE 15**

**(Recommended External Circuitry is Depicted With Dotted Lines)**


BLOCK DIAGRAM
CURRENT AND VOLTAGE REGULATOR
FOUR QUADRANT MULTIPLIER
DIFFERENTIAL CURRENT CONVERTER
15 V+
2 +4.3 V +VR
3
4 -VR -4.3 V
V- 5
1
R1
VY 9 6
7 8 RY
11 12 RX
IA
IB
10 VX 13
14 Io
Io = IA - IB
SIMPLIFIED CIRCUIT SCHEMATIC
CONSTANT CURRENT SOURCE CONTROL
I1
+9.4 V
+8.7 V
8.7 k
7.2 k
-9.4 V
3 I1
2.4 V
2 I1
1.7 V
500
COMPLETE CIRCUIT SCHEMATIC
5.4 k
3.0 k
2 k
10 pF
10 k
R1
GND
REGULATOR
MULTIPLIER
DIFFERENTIAL CURRENT CONVERTER

**1.2 Regulator (Figure 15)**

The regulator biases the entire MC1594 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at pin 2 is approximately +4.3 V while the regulated voltage at pin 4 is approximately -4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0$ mA (equivalent load of 8.6 kΩ). As will be shown later, there will normally be two 20 k-ohm potentiometers and one 50 k-ohm potentiometer connected between pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1594. Note that all current sources are related to current $I_1$ which is determined by R1. For best temperature performance, R1 should be 16 kΩ so that $I_1 \approx 0.5$ mA for all applications.

**1.3 Multiplier (Figure 15)**

The multiplier section of the MC1594 (center section of Figure 15) is nearly identical to the MC1595 and is discussed in detail in Application Note AN-489, "Analysis and Basic Operation of the MC1595". The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I \approx \frac{2V_X V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages.

**1.4 Differential Current Converter (Figure 15)**

This portion of the circuitry converts the differential output current ($I_A - I_B$) of the multiplier to a single-ended output current ($I_o$):

$$I_o = I_A - I_B$$

or

$$I_o = \frac{2V_X V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor $R_L$ from the output (pin 14) to ground (Figure 17) or by using an op-ampl. as a current-to-voltage converter (Figure 16). The result in both circuits is that the output voltage is given by:

$$V_o = \frac{2R_L V_X V_Y}{R_X R_Y I_1} = KV_X V_Y$$

$$\text{where K (scale factor)} = \frac{2R_L}{R_X R_Y I_1}$$

## 2. DC OPERATION

**2.1 Selection of External Components**

For low frequency operation the circuit of Figure 16 is recommended. For this circuit, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, R1 = 16 kΩ and hence $I_1 \approx 0.5$ mA. Therefore, to set the scale factor, K, equal to 1/10, the value of $R_L$ can be calculated to be:

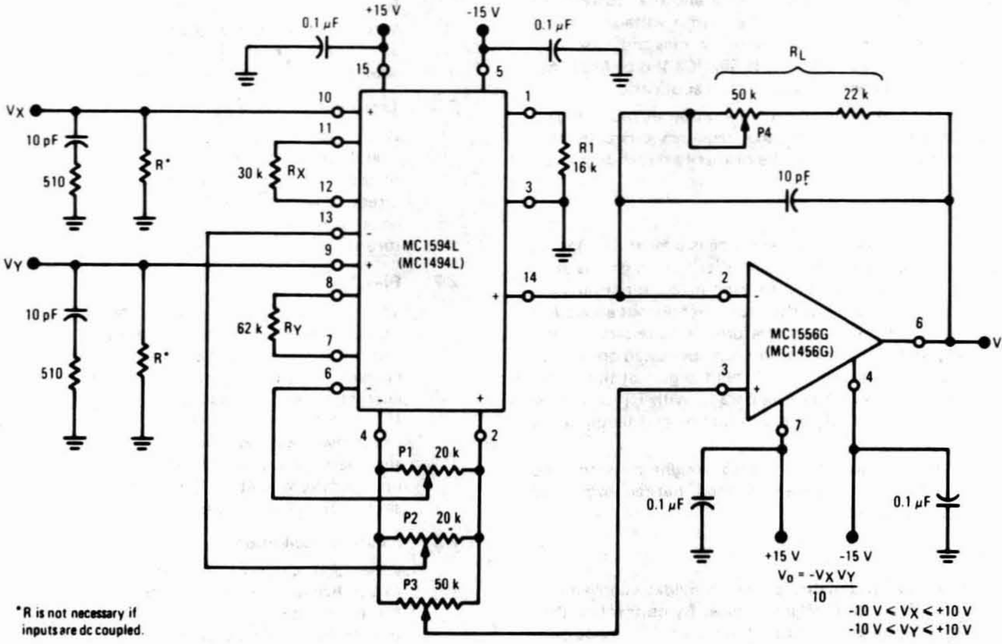
$$K = \frac{1}{10} = \frac{2R_L}{R_X R_Y I_1}$$

$$\text{or} \quad R_L = \frac{R_X R_Y I_1}{(2)(10)} = \frac{(30\text{ k})(62\text{ k})(0.5\text{ mA})}{20}$$

$$R_L = 46.5\text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making $R_L$ a fixed 47 kΩ resistor. However, if it is desired

FIGURE 16 – TYPICAL MULTIPLIER CONNECTION



**that the scale factor be exact, $R_L$ can be comprised of a fixed resistor and a potentiometer as shown in Figure 16. It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the $V_X$ and $V_Y$ input voltages are expected to be large, say ±10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set K = 1/2 or K = 1 or even K = 100. This can be accomplished by adjusting $R_X$, $R_Y$ and $R_L$ appropriately.**

The selection of $R_L$ is arbitrary and can be chosen after resistors $R_X$ and $R_Y$ are found. Note in Figure 16 that $R_Y$ is 62 kΩ while $R_X$ is 30 kΩ. The reason for this is that the "Y" side of the multiplier exhibits a second order non-linearity whereas the "X" side exhibits a simple non-linearity. By making the $R_Y$ resistor approximately twice the value of the $R_X$ resistor, the linearity on both the "X" and "Y" sides are made equal. The selection of the $R_X$ and $R_Y$ resistor values is dependent upon the expected amplitude of $V_X$ and $V_Y$ inputs. To maintain a specified linearity, resistors $R_X$ and $R_Y$ should be selected according to the following equations:

$R_X \geq 3\, V_X$ (max) in kΩ when $V_X$ is in volts

$R_Y \geq 6\, V_Y$ (max) in kΩ when $V_Y$ is in volts

For example, if the maximum input on the "X" side is ±1 volt, resistor $R_X$ can be selected to be 3 kΩ. If the maximum input on the "Y" side is also ±1 volt, then resistor $R_Y$ can be selected to be 6 kΩ (6.2 kΩ nominal value). If a scale factor of K = 10 is desired, the load resistor is found to be 47 kΩ. In this example, the multiplier provides a gain of 20 dB.

### 2.2 Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate current-to-voltage converter. The output current of the multiplier flows through the feedback resistor $R_L$ to provide a low impedance output voltage from the op-ampl. Since the offset current and bias currents of the op-ampl. will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1556/MC1456 or MC1741/MC1741C are excellent choices for this application.

Since the MC1594 is capable of operation at much higher frequencies than the op-ampl., the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the op-ampl.

### 2.3 Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op-ampls.) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with $R_L$ should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op-ampl. might be employed using slightly heavier compensation than that recommended for unity-gain operation.

### 2.4 Offset Adjustment

**The non-inverting input of the op-ampl. provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output offset voltage can be adjusted to zero (see offset and scale factor adjustment procedure).**

**The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).**

### 2.5 Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 16 is:

A. X Input Offset
  - (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 9)
  - (b) connect "X" input (pin 10) to ground
  - (c) adjust X-offset potentiometer, P2 for an ac null at the output

B. Y Input Offset
  - (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 10)
  - (b) connect "Y" input (pin 9) to ground
  - (c) adjust Y-offset potentiometer, P1 for an ac null at the output

C. Output Offset
  - (a) connect both "X" and "Y" inputs to ground
  - (b) adjust output offset potentiometer, P3, until the output voltage $V_O$, is zero volts dc

D. Scale Factor
  - (a) apply +10 Vdc to both the "X" and "Y" inputs
  - (b) adjust P4 to achieve −10.00 V at the output
  - (c) apply −10 Vdc to both "X" and "Y" inputs and check for $V_O = -10.00$ V

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1594 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinite" resolution type rather than wirewound. Fine adjustments in balanced-modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

### 2.6 Temperature Stability

While the MC1594 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Previous discussion shows the direct dependence on $R_X$, $R_Y$, and $R_L$ and indirect dependence on R1 (through $I_1$). Any circuit subjected to temperature variations should be evaluated with these effects in mind.

### 2.7 Bias Currents

The MC1594 multiplier, like most linear IC's, requires a dc bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs $V_X$ and $V_Y$ are able to supply the small bias current (≈ 0.5 μA) resistors, R (Figure 16) can be omitted. If the MC1594 is used in an ac mode of operation and capacitive coupling is used the value of resistor R can be any reasonable value up to 100 kΩ. For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

### 2.8 Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network is to reduce the "Q" of the source-tuned circuits which cause the oscillation.

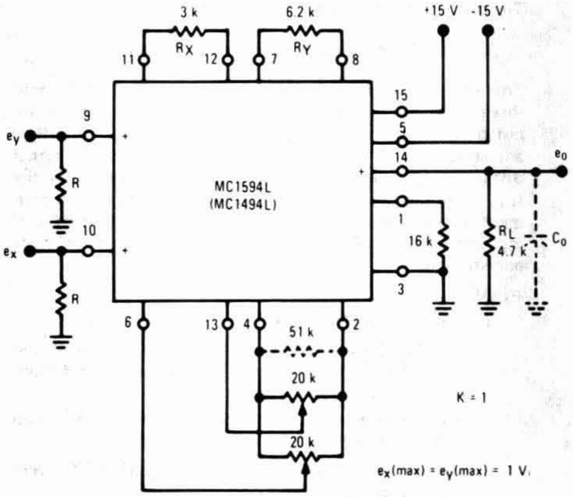
Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

## 3. AC OPERATION

### 3.1 General

For ac operation, such as balanced modulation, frequency doubler, AGC, etc., the op-ampl. will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be ac-coupled and the dc voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 17 shows a typical ac multiplier circuit with a scale factor K≈1. Again, resistor $R_X$ and $R_Y$ are chosen as outlined in the previous section, with $R_L$ chosen to provide the required scale factor.

FIGURE 17 – WIDEBAND MULTIPLIER



The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1594 is typically 17 μA and 35 μA maximum. Thus, the maximum output offset would be about 160 mV.

### 3.2 Bandwidth

The bandwidth of the MC1594 is primarily determined by two factors. First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance ($C_0$) of 10 pF, the 3 dB bandwidth would be approximately 3.4 MHz. If the load resistor were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors $R_X$ and $R_Y$ and the transistors associated with them. The effect of these transmission "zeros" is seen in Figures 9 and 10. The reason for this increase in gain is due to the bypassing of $R_X$ and $R_Y$ at high frequencies. Since the $R_Y$ resistor is approximately twice the value of the $R_X$ resistor, the zero associated with the "Y" input will occur at approximately one octave below the zero associated with the "X" input. For $R_X$ = 30 kΩ and $R_Y$ = 62 kΩ, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7 MHz respectively.

It should be noted that the MC1594 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a dc voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an ac voltage on both the "X" and "Y" side, such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for ac applications; (1) the value of resistors $R_X$, $R_Y$ and $R_L$ should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor $R_L$ such that the dominant pole ($R_L$, $C_0$) cancels the input zero ($R_X$, 3.5 pF or $R_Y$, 3.5 pF) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10. Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the ac signal.

For ac applications requiring bandwidths greater than those specified for the MC1594, two other devices are recommended. For modulator-demodulator applications, the MC1596 may be used up to 100 MHz. For wideband multiplier applications, the MC1595 (using small collector loads and ac coupling) can be used.

### 3.3 Slew-Rate

The MC1594 multiplier is not slew-rate limited in the ordinary sense that an op-ampl. is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitations. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew-Rate} \quad \frac{\Delta V_o}{\Delta T} = \frac{I_o}{C}$$

Thus, if $C_o$ is 10 pF, the maximum slew-rate would be:

$$\frac{\Delta V_o}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50\ \text{V}/\mu\text{s}$$

This can be improved if necessary by addition of an emitter-follower or other type of buffer.

### 3.4 Phase-Vector Error

All multipliers are subject to an error which is known as the phase-vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase-vector error is best explained by an example. If the "X" input is described in vector notation as

$$X = A \measuredangle 0^{\circ}$$

and the "Y" input is described as

$$Y = B \measuredangle 0^{\circ}$$

then the output product would be expected to be

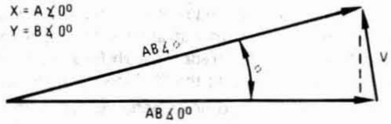
$$V_o = AB \measuredangle 0^{\circ} \text{ (see Figure 18)}$$

However, due to a relative phase shift between the "X" and "Y" channels, the output product will be given by

$$V_o = AB \measuredangle \phi$$

Notice that the magnitude is correct but the phase angle of the product is in error. The vector, V, associated with this error is the "phase-vector error". The startling fact about the phase-vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.57° will result in a 1% phase-vector error. For most applications, this error is meaningless. If phase of the output product is not important, then neither is the phase-vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase-vector error will represent a 1% amplitude error at the phase angle of interest.

FIGURE 18 – PHASE-VECTOR ERROR



### 3.5 Circuit Layout

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across $R_X$ and $R_Y$ should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

## 4. DC APPLICATIONS

### 4.1 Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:

$$V_o = KV^2$$

where K is the scale factor (see Figure 19).

However, a more careful look at the multiplier's defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:

$$V_o = K(V_x + V_{iox} - V_{x\,off})\,(V_y + V_{ioy} - V_{y\,off}) + V_{oo}$$

(See "Definitions" for an explanation of terms).

With $V_x = V_y = V$ (squaring) and defining

$$\epsilon_x = V_{iox} - V_{x\,off}$$

$$\epsilon_y = V_{ioy} - V_{y\,off}$$

The output voltage equation becomes

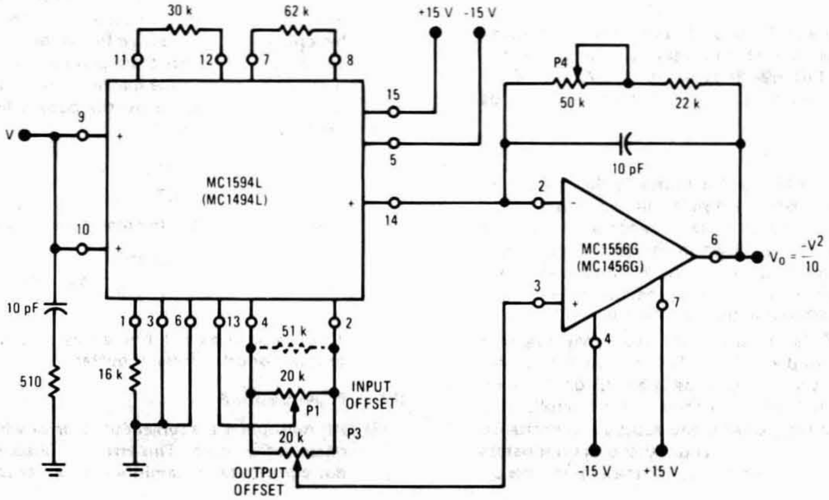
$$V_o = K\,V_x^2 + KV_x\,(\epsilon_x + \epsilon_y) + K\epsilon_x\epsilon_y + V_{oo}$$

This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, $\epsilon_x$ is determined by the internal offset, $V_{iox}$, but $\epsilon_y$ is adjustable to the extent that the $(\epsilon_x + \epsilon_y)$ term can be zeroed. Then the output offset adjustment is used to adjust the $V_{oo}$ term and thus zero the remaining error terms. An ac procedure for nulling with three adjustments is:

A. AC Procedure:

1. Connect oscillator (1 kHz, 15 Vpp) to input
2. Monitor output at 2 kHz with tuned voltmeter and adjust P4 for desired gain (Be sure to peak response of voltmeter)
3. Tune voltmeter to 1 kHz and adjust P1 for a minimum output voltage
4. Ground input and adjust P3 (output offset) for zero volts dc out
5. Repeat steps 1 through 4 as necessary.

FIGURE 19 – MC1594 SQUARING CIRCUIT



B. DC Procedure:

1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_o = 0.0$ Vdc
2. Set $V_X = V_Y = 1.0$ V and adjust P1 (Y input offset potentiometer) such that the output voltage is -0.100 volts
3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is -10.00 volts
4. Set $V_X = V_Y = -10$ Vdc and check that $V_O = -10$V Repeat steps 1 through 4 as necessary.

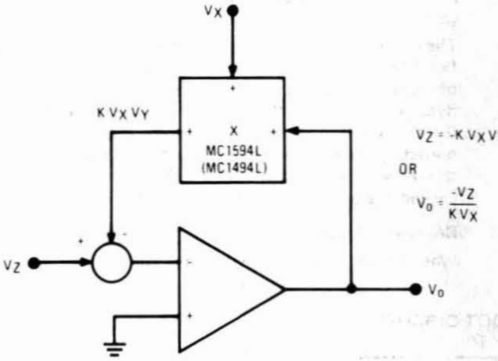
### 4.2 Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21.

The characteristic "failure" mode of the divide circuit is latch-up. One way it can occur is if $V_X$ is allowed to go negative or, in some cases, if $V_X$ approaches zero.

Figure 20 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is non-inverting. Its output is fed to the inverting input of the op-ampl. Thus, operation is in the negative feedback mode and the circuit is dc stable.

FIGURE 20 – BASIC DIVIDE CIRCUIT USING MULTIPLIER



Should $V_X$ change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from $V_X$ being near zero is a result of the transfer through the multiplier being near zero. The op-ampl. is then operating with a very high closed loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op-ampl. exceeding the rated common-mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op-ampl. to approximately ± 10.7 volts. Five-percent tolerance, 10-volt zeners are used to assure adequate output swing but still limit the output voltage of the op-ampl. from exceeding the common-mode input range of the MC1594.

Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P3) until the output voltage ($V_o$) remains at some (not necessarily zero) constant value as $V_X$ is varied between +1.0 volt and +10 volts.
2. Maintain $V_Z$ at 0 volts, set $V_X$ at +10 volts and adjust the Y input offset potentiometer (P1) until $V_o = 0$ volts.
3. With $V_X = V_Z$, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily - 10 volts) constant value as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
4. Maintain $V_X = V_Z$ and adjust the scale factor potentiometer ($R_L$) until the average value of $V_o$ is - 10 volts as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denomi-

FIGURE 21 – PRACTICAL DIVIDE CIRCUIT

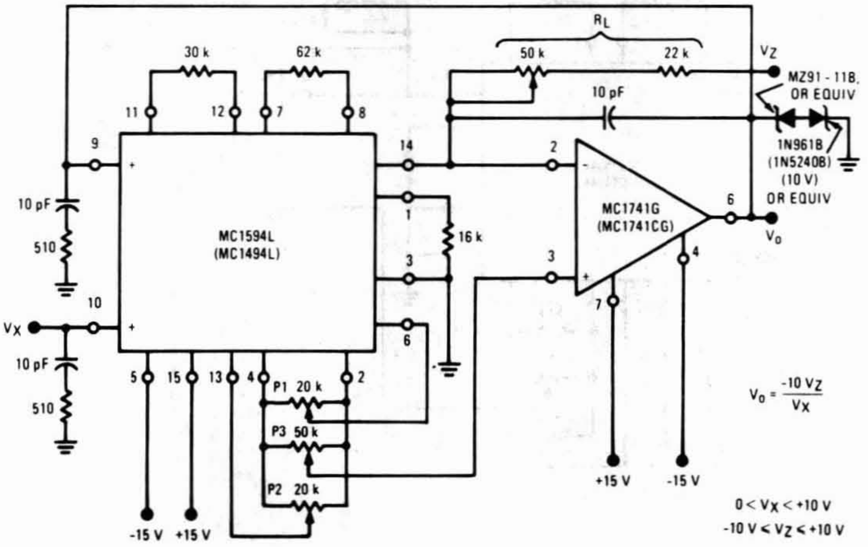
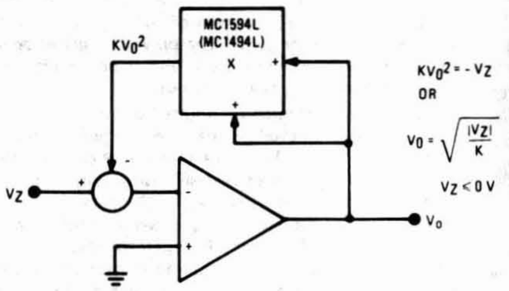


FIGURE 22 – BASIC SQUARE ROOT CIRCUIT



nator voltage. As a result, if $V_X$ is set to 10 volts and 0.5% accuracy is available, then 5% accuracy can be expected when $V_X$ is only 1 volt.

In accordance with an earlier statement, $V_X$ may have only one polarity, positive, while $V_Z$ may be either polarity.

### 4.3 Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up.

This circuit too, may be adjusted in the closed-loop mode:

1. Set $V_Z$ = -0.01 Vdc and adjust P3 (output offset) for $V_O$ = 0.316 Vdc.
2. Set $V_Z$ to -0.9 Vdc and adjust P2 ("X" adjust) for $V_O$ = +3 Vdc.
3. Set $V_Z$ to -10 Vdc and adjust P4 (gain adjust) for $V_O$ = +10 Vdc.

Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

Note: Operation near zero volts input may prove very inaccurate, hence, it may not be possible to adjust $V_O$ to 0 but rather only to within 100 to 400 mV of zero.

## 5. AC APPLICATIONS

### 5.1 Wideband Amplifier With Linear AGC

If one input to the MC1594 is a dc voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the dc voltage. Hence, the multiplier can function as a dc coupled, wideband amplifier with linear AGC control.

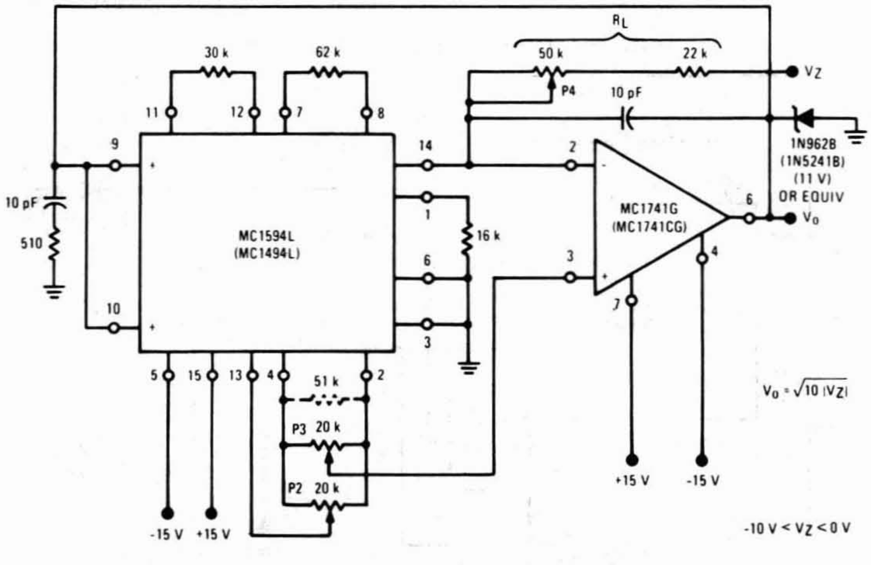
In addition to the advantage of Linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with zero volts dc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using cermet multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output-voltage-swing capability and output impedance are unchanged with variations in AGC voltage.

The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier can handle 1 V(rms) and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter-follower buffer has been added to extend the bandwidth in excess of 1 MHz.

### 5.2 Balanced Modulator

When two-time variant signals are used as inputs, the result-

FIGURE 23 – SQUARE ROOT CIRCUIT



ing output is suppressed-carrier double-sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

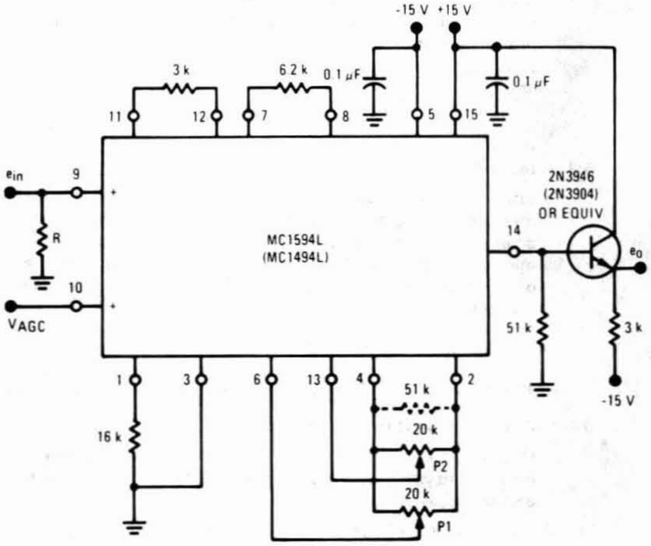
$$V_o = K(e_1 \cos\omega_m t)(e_2 \cos\omega_c t)$$

where $\omega_m$ is the modulation frequency and $\omega_c$ is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_o = \frac{Ke_1e_2}{2}\,[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

Unlike many modulation schemes, which are non-linear in nature, the modulation which takes place when using the MC1594 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 25 shows the MC1594 configuration to perform this function.

FIGURE 24 – WIDEBAND AMPLIFIER WITH LINEAR AGC

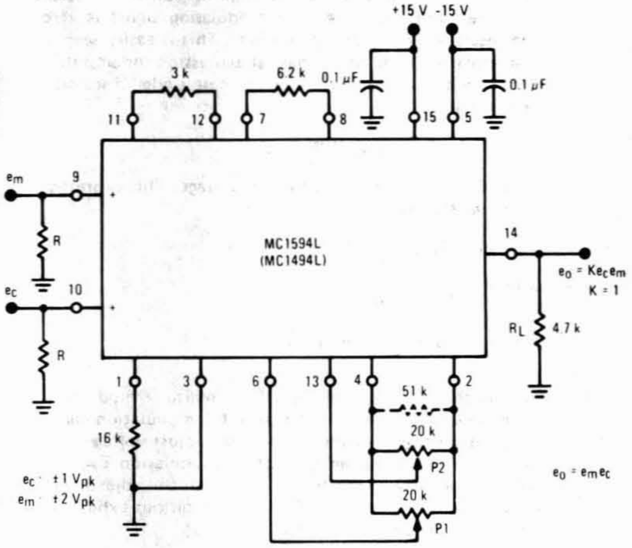


Notice that the resistor values for $R_X$, $R_Y$, and $R_L$ have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1594 and then lowering $R_X$ and $R_Y$ to achieve a gain of 1. The $e_c$ can be as large as 1 volt peak and $e_m$ as high as 2 volts peak. No output offset adjust is employed since we are interested only in the ac output components.

The input R's are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 k ohm output impedance and capacitive loading. Assuming a 6 pF load, the small-signal bandwidth is 5.5 MHz.

The circuit of Figure 25 will provide a typical carrier rejection of ≥70 dB from 10 kHz to 1.5 MHz.

FIGURE 25 – BALANCED MODULATOR



The adjustment procedure for this circuit is quite simple.

(1) Place the carrier signal at pin 10. With no signal applied to pin 9, adjust potentiometer P1 such that an ac null is obtained at the output.

(2) Place a modulation signal at pin 9. With no signal applied to pin 10, adjust potentiometer P2 such that an ac null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

### 5.3 Frequency Doubler

If for Figure 25 both inputs are identical;

$$e_m = e_c = E\cos\omega t$$

Then the output is given by

$$e_o = e_me_c = E^2\cos^2\omega t$$

which reduces to

$$e_o = \frac{E^2}{2}\,(1 + \cos 2\omega t)$$

This equation states that the output will consist of a dc term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires no filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2 MHz.

### 5.4 Amplitude Modulator

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the modulation input. This procedure places a dc offset on the modulation input of the multiplier such that the carrier still passes thru the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with K = 1,

$$e_o = (E + E_m \cos\omega_m t)\ (E_c \cos\omega_c t)$$

where E is the dc input offset adjust voltage. This expression can be written as:

$$e_o = E_o\ [1 + M \cos\omega_c t]\ \cos\omega_c t$$

where $E_o = EE_c$

and $M = \dfrac{E_m}{E}$ = modulation index

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation, $E_m$. This is done by observing the output waveform and adjusting the input offset potentiometer, P1, until the output exhibits the familiar amplitude modulation waveform.

### 5.5 Phase Detector

If the circuit of Figure 25 has as its inputs two signals of identical frequency but having a relative phase shift the output will be a dc signal which is directly proportional to the cosine of phase difference as well as the double frequency term.

$$e_c = E_c \cos\omega_c t$$

$$e_m = E_m \cos(\omega_c t + \phi)$$

$$e_o = e_c e_m = E_c E_m \cos\omega_c t \cos(\omega_c t + \phi)$$

or

$$e_o = \frac{E_c E_m}{2}\ [\cos\phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of $R_L$ to an offset adjustment potentiometer will result in a dc output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

## 6. DEFINITIONS OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of this mystery, the following definitions and examples are presented.

### 6.1 Multiplier Transfer Function

The output of the multiplier may be expressed by this equation:

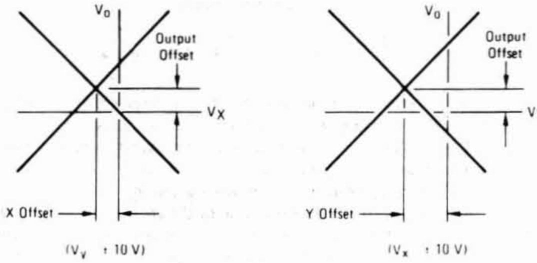
$$V_o = K(V_x \pm V_{iox} - V_{x\,off})\ (V_y \pm V_{ioy} - V_{y\,off}) \pm V_{oo} \quad (1)$$

where K = scale factor (see 6.5)

$V_x$ = "x" input voltage
$V_y$ = "y" input voltage
$V_{iox}$ = "x" input offset voltage
$V_{ioy}$ = "y" input offset voltage
$V_{x\,off}$ = "x" input offset adjust voltage
$V_{y\,off}$ = "y" input offset adjust voltage
$V_{oo}$ = output offset voltage

The voltage transfer characteristic below indicates "X", "Y" and output offset voltages.

FIGURE 26



### 6.2 Linearity

Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full-scale output and is measured for $V_x$ and $V_y$ separately either using an "X-Y" plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_o = \frac{V_x V_y}{10} \pm (0.0035)\ (10 \text{ volts})$$

### 6.3 Input Offset Voltage

The input offset voltage is defined from Equation (1). It is measured for $V_x$ and $V_y$ separately and is defined to be that dc input offset adjust voltage ("x" or "y") that will result in minimum ac output when ac (5 Vpp, 1 kHz) is applied to the other input ("y" or "x" respectively). From Equation (1) we have:

$$V_{o(ac)} = K\ (0 \pm V_{iox} - V_{x\,off})\ (\sin\omega t)$$

adjust $V_{x\,off}$ so that $(\pm V_{iox} - V_{x\,off}) = 0$.

### 6.4 Output Offset Current and Voltage

Output offset current ($I_{oo}$) is the dc current flowing in the output lead when $V_x = V_y = 0$ and "X" and "Y" offset voltages are adjusted to zero.

Output offset voltage ($V_{oo}$) is:

$$V_{oo} = I_{oo}\, R_L$$

where $R_L$ is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting "X" and "Y" offset voltages to zero. Thus it includes input offset terms, an output offset term and a scale factor term.

### 6.5 Scale Factor

Scale factor is the K term in Equation (1). It determines the "gain" of the multiplier and is expressed approximately by the following equation.

$$K = \frac{2R_L}{R_x R_y I_1} \quad \text{where } R_x \text{ and } R_y \gg \frac{kT}{qI_1}$$

and $I_1$ is the current out of pin 1.

### 6.6 Total DC Accuracy

The total dc accuracy of a multiplier is defined as error in multiplier output with dc (±10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1594 because error terms can be nulled by the user.

### 6.7 Temperature Stability (Drift)

Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by re-adjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by:

$$\Delta V_O = \pm[K \pm K\ (TCK)\ (\Delta T)\ ]\ [\ (TCV_{iox})\ (\Delta T)\ ]\ [\ (TCV_{ioy})\ (\Delta T)\ ] \pm (TCV_{oo})\ (\Delta T)$$

### 6.8 Total DC Accuracy Drift

This is the temperature drift in output voltage with 10 volts applied to each input. The output is adjusted to 10 volts at $T_A = +25^{\circ}C$. Assuming initial offset voltages have been adjusted to zero at $T_A = +25^{\circ}C$, then:

$$V_O = [K \pm K\ (TCK)\ (\Delta T)\ ]\ [10 \pm (TCV_{iox})\ (\Delta T)\ ]\ [10 \pm (TCV_{ioy})\ (\Delta T)\ ] \pm (TCV_{oo})\ (\Delta T)$$

### 6.9 Power Supply Rejection

Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1-volt, 100-Hz signal on each supply (±15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

### 6.10 Output Voltage Swing

Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load (note-output offset is adjusted to zero).

If an op-ampl. is used, the multiplier output becomes a virtual ground – the swing is then determined by the scale factor and the op-ampl. selected.

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## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC1495L | 0°C to +70°C | Ceramic DIP |
| MC1595L | −55°C to +125°C | Ceramic DIP |

# MC1495L
# MC1595L

## Specifications and Applications Information

### WIDEBAND MONOLITHIC FOUR-QUADRANT MULTIPLIER

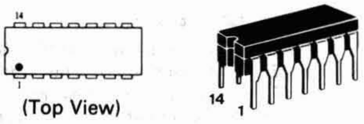
. . . designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier.

- Wide Bandwidth
- Excellent Linearity – 1% max Error on X-Input, 2% max Error on Y-Input – MC1595L
- Excellent Linearity – 2% max Error on X-Input, 4% max Error on Y-Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts
- ± 15 Volt Operation

### LINEAR FOUR-QUADRANT MULTIPLIER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



CERAMIC PACKAGE
CASE 632-02
MO-001AA

FIGURE 1 – FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC

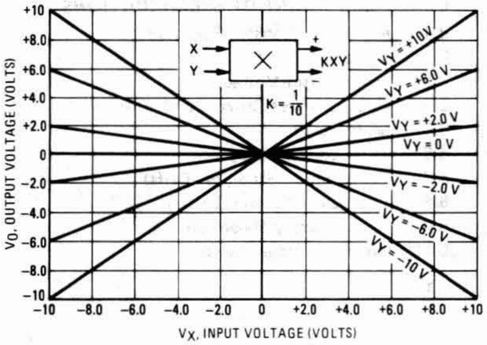


FIGURE 2 – TRANSCONDUCTANCE BANDWIDTH

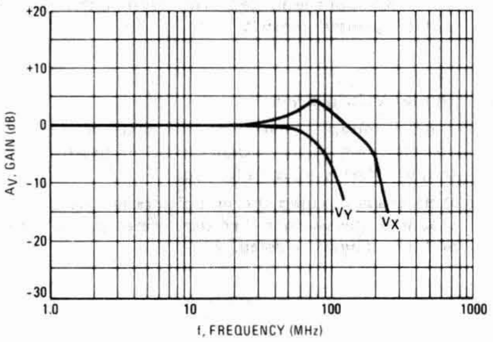
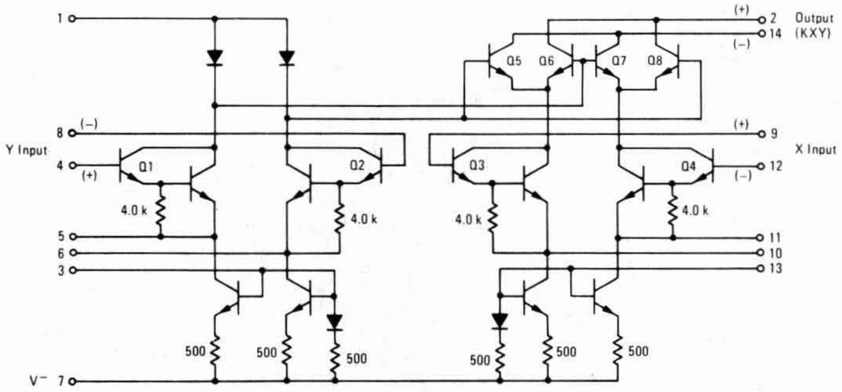


FIGURE 3 – CIRCUIT SCHEMATIC



## ELECTRICAL CHARACTERISTICS ($V^+$ = +32V, $V^-$ = −15 V, $T_A$ = +25°C, $I_3 = I_{13}$ = 1 mA, $R_X = R_Y$ = 15 kΩ, $R_L$ = 11 kΩ unless otherwise noted)

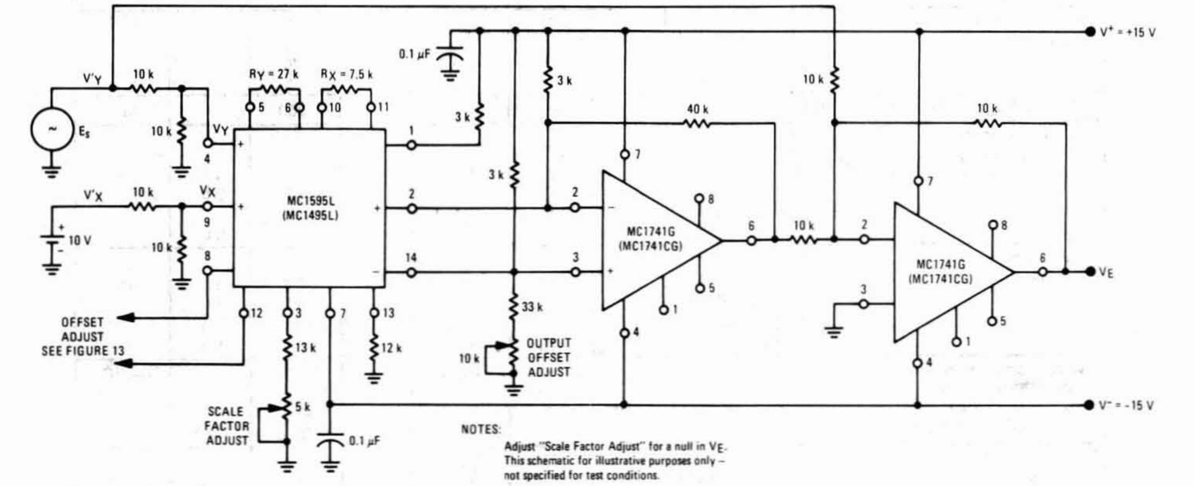
| Characteristic | | Figure | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Linearity: | | | | | | | |
| Output Error in Percent of Full Scale: | | 5 | | | | | % |
| $T_A$ = +25°C | | | | | | | |
| $-10 < V_X < +10$ ($V_Y = \pm10$ V) | MC1495 | | $E_{RX}$ | – | ± 1.0 | ± 2.0 | |
| | MC1595 | | | – | ± 0.5 | ± 1.0 | |
| $-10 < V_Y < +10$ ($V_X = \pm10$ V) | MC1495 | | $E_{RY}$ | – | ± 2.0 | ± 4.0 | |
| | MC1595 | | | – | ± 1.0 | ± 2.0 | |
| $T_A$ = 0 to +70°C | MC1495 | | | | | | |
| $-10 < V_X < +10$ ($V_Y = \pm10$ V) | | | $E_{RX}$ | – | ± 1.5 | – | |
| $-10 < V_Y < +10$ ($V_X = \pm10$ V) | | | $E_{RY}$ | – | ± 3.0 | – | |
| $T_A$ = −55°C to +125°C | MC1595 | | | | | | |
| $-10 < V_X < +10$ ($V_Y = \pm10$ V) | | | $E_{RX}$ | – | ± 0.75 | – | |
| $-10 < V_Y < +10$ ($V_X = \pm10$ V) | | | $E_{RY}$ | – | ± 1.50 | – | |
| Squaring Mode Error:<br>Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment | | 5 | $E_{SQ}$ | | | | % |
| $T_A$ = +25°C | MC1495 | | | – | ± 0.75 | – | |
| | MC1595 | | | – | ± 0.5 | – | |
| $T_A$ = 0 to +70°C | MC1495 | | | – | ± 1.0 | – | |
| $T_A$ = −55°C to +125°C | MC1595 | | | – | ± 0.75 | – | |
| Scale Factor (Adjustable)<br>$(K = \frac{2R_L}{I_3 R_X R_Y})$ | | – | K | – | 0.1 | – | – |
| Input Resistance (f = 20 Hz) | MC1495 | 7 | $R_{INX}$ | – | 20 | – | MΩ |
| | MC1595 | | | – | 35 | – | |
| | MC1495 | | $R_{INY}$ | – | 20 | – | |
| | MC1595 | | | – | 35 | – | |
| Differential Output Resistance (f = 20 Hz) | | 8 | $R_o$ | – | 300 | – | kΩ |
| Input Bias Current<br>$I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$ | MC1495 | 6 | $I_{bx}$ | – | 2.0 | 12 | µA |
| | MC1595 | | | – | 2.0 | 8.0 | |
| | MC1495 | | $I_{by}$ | – | 2.0 | 12 | |
| | MC1595 | | | – | 2.0 | 8.0 | |
| Input Offset Current<br>$\lvert I_9 - I_{12} \rvert$ | MC1495 | 6 | $\lvert I_{iox} \rvert$ | – | 0.4 | 2.0 | µA |
| | MC1595 | | | – | 0.2 | 1.0 | |
| $\lvert I_4 - I_8 \rvert$ | MC1495 | | $\lvert I_{ioy} \rvert$ | – | 0.4 | 2.0 | |
| | MC1595 | | | – | 0.2 | 1.0 | |
| Average Temperature Coefficient of Input Offset Current | | 6 | $\lvert TC_{Iio} \rvert$ | | | | nA/°C |
| ($T_A$ = 0 to +70°C) | MC1495 | | | – | 2.5 | – | |
| ($T_A$ = −55°C to +125°C) | MC1595 | | | – | 2.5 | – | |
| Output Offset Current<br>$\lvert I_{14} - I_2 \rvert$ | MC1495 | 6 | $\lvert I_{oo} \rvert$ | – | 20 | 100 | µA |
| | MC1595 | | | – | 10 | 50 | |
| Average Temperature Coefficient of Output Offset Current | | 6 | $\lvert TC_{Ioo} \rvert$ | | | | nA/°C |
| ($T_A$ = 0 to +70°C) | MC1495 | | | – | 20 | – | |
| ($T_A$ = −55°C to +125°C) | MC1595 | | | – | 20 | – | |
| Frequency Response | | | | | | | |
| 3.0 dB Bandwidth, $R_L$ = 11 kΩ | | 9,10 | $BW_{3dB}$ | – | 3.0 | – | MHz |
| 3.0 dB Bandwidth, $R_L$ = 50 Ω (Transconductance Bandwidth) | | | $T_{BW3\ dB}$ | – | 80 | – | MHz |
| 3° Relative Phase Shift Between $V_X$ and $V_Y$ | | | $f_\phi$ | – | 750 | – | kHz |
| 1% Absolute Error Due to Input-Output Phase Shift | | | $f_\theta$ | – | 30 | – | kHz |
| Common Mode Input Swing (Either Input) | MC1495 | 11 | CMV | ±10.5 | ±12 | – | Vdc |
| | MC1595 | | | ±11.5 | ±13 | – | |
| Common Mode Gain (Either Input) | MC1495 | 11 | $A_{CM}$ | −40 | −50 | – | dB |
| | MC1595 | | | −50 | −60 | – | |
| Common Mode Quiescent Output Voltage | | 12 | $V_{o1}$ | – | 21 | – | Vdc |
| | | | $V_{o2}$ | – | 21 | – | |
| Differential Output Voltage Swing Capability | | 9 | $V_o$ | – | ±14 | – | $V_{peak}$ |
| Power Supply Sensitivity | | 12 | $S^+$ | – | 5.0 | – | mV/V |
| | | | $S^-$ | – | 10 | – | |
| Power Supply Current | | 12 | $I_7$ | – | 6.0 | 7.0 | mA |
| DC Power Dissipation | | 12 | $P_D$ | – | 135 | 170 | mW |

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Applied Voltage<br>($V_2-V_1$, $V_{14}-V_1$, $V_1-V_9$, $V_1-V_{12}$, $V_1-V_4$, $V_1-V_8$, $V_{12}-V_7$, $V_9-V_7$, $V_8-V_7$, $V_4-V_7$) | $\Delta V$ | 30 | Vdc |
| Differential Input Signal | $V_{12}-V_9$<br>$V_4-V_8$ | $\pm(6+I_{13}R_X)$<br>$\pm(6+I_3R_Y)$ | Vdc<br>Vdc |
| Maximum Bias Current | $I_3$<br>$I_{13}$ | 10<br>10 | mA |
| Power Dissipation (Package Limitation)<br>Ceramic Package<br>Derate above $T_A$ = +25°C | $P_D$ | <br>750<br>5.0 | <br>mW<br>mW/°C |
| Operating Temperature Range<br>MC1495<br>MC1595 | $T_A$ | <br>0 to +70<br>-55 to +125 | °C<br>°C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

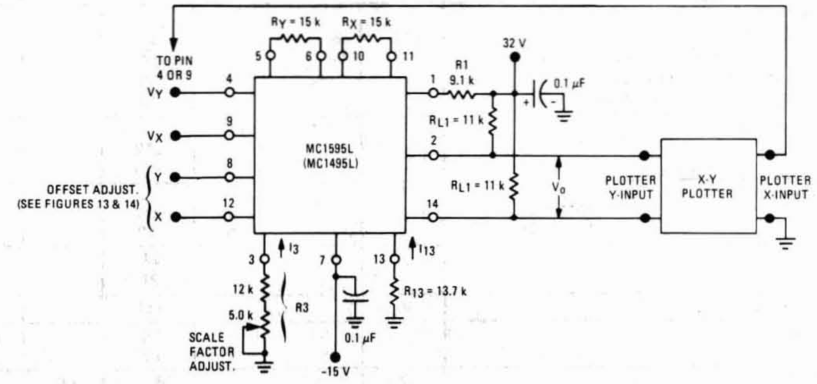
## TEST CIRCUITS

### FIGURE 4 – LINEARITY (USING NULL TECHNIQUE)


V'Y
10 k
10 k
E_s
VY
4
RY = 27 k
RX = 7.5 k
5
6
10
11
1
3 k
3 k
3 k
0.1 µF
V+ = +15 V
10 k
40 k
10 k
7
V'X
10 k
VX
10 V
10 k
9
8
MC1595L
(MC1495L)
2
14
3
MC1741G
(MC1741CG)
8
6
5
1
4
10 k
2
7
8
MC1741G
(MC1741CG)
6
VE
3
5
1
4
12
3
7
13
13 k
12 k
33 k
10 k
OUTPUT OFFSET ADJUST
OFFSET ADJUST SEE FIGURE 13
SCALE FACTOR ADJUST
5 k
0.1 µF
V– = -15 V

NOTES:
Adjust "Scale Factor Adjust" for a null in $V_E$.
This schematic for illustrative purposes only – not specified for test conditions.

### FIGURE 5 – LINEARITY (USING X-Y PLOTTER TECHNIQUE)


RY = 15 k
RX = 15 k
TO PIN 4 OR 9
5
6
10
11
4
VY
9
VX
8
12
Y
X
OFFSET ADJUST. (SEE FIGURES 13 & 14)
MC1595L
(MC1495L)
32 V
R1
9.1 k
1
0.1 µF
RL1 = 11 k
2
RL1 = 11 k
Vo
14
PLOTTER Y-INPUT
X-Y PLOTTER
PLOTTER X-INPUT
3
I3
7
13
I13
12 k
5.0 k
R3
R13 = 13.7 k
0.1 µF
SCALE FACTOR ADJUST.
-15 V

## TEST CIRCUITS (continued)

**FIGURE 6 – INPUT AND OUTPUT CURRENT**

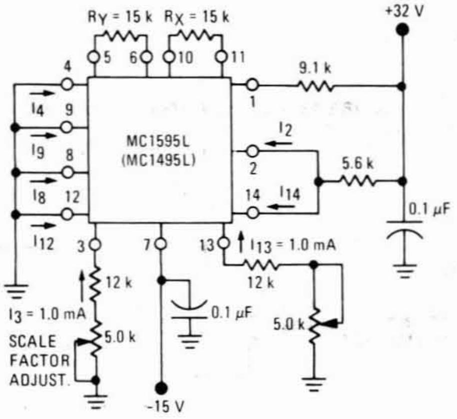

RY = 15 k
RX = 15 k
+32 V
MC1595L
(MC1495L)
9.1 k
5.6 k
0.1 µF
I4
I9
I8
I12
I2
I14
I13 = 1.0 mA
12 k
I3 = 1.0 mA
0.1 µF
5.0 k
SCALE
FACTOR
ADJUST.
-15 V

**FIGURE 7 – INPUT RESISTANCE**

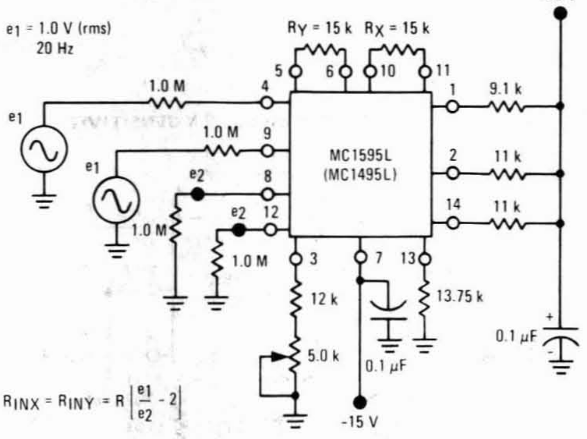

e1 = 1.0 V (rms)
20 Hz
RY = 15 k
RX = 15 k
+32 V
1.0 M
1.0 M
e1
e2
1.0 M
1.0 M
MC1595L
(MC1495L)
9.1 k
11 k
11 k
12 k
13.75 k
5.0 k
0.1 µF
0.1 µF
-15 V
RINX = RINY = R |e1/e2 - 2|

**FIGURE 8 – OUTPUT RESISTANCE**

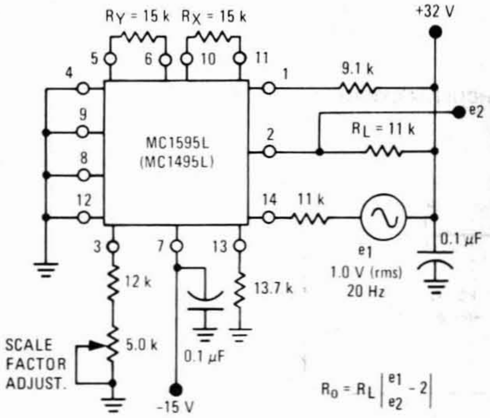

RY = 15 k
RX = 15 k
+32 V
MC1595L
(MC1495L)
9.1 k
RL = 11 k
e2
11 k
e1
1.0 V (rms)
20 Hz
0.1 µF
12 k
13.7 k
0.1 µF
5.0 k
SCALE
FACTOR
ADJUST.
-15 V
Ro = RL |e1/e2 - 2|

**FIGURE 9 – BANDWIDTH ($R_L$ = 11 kΩ)**

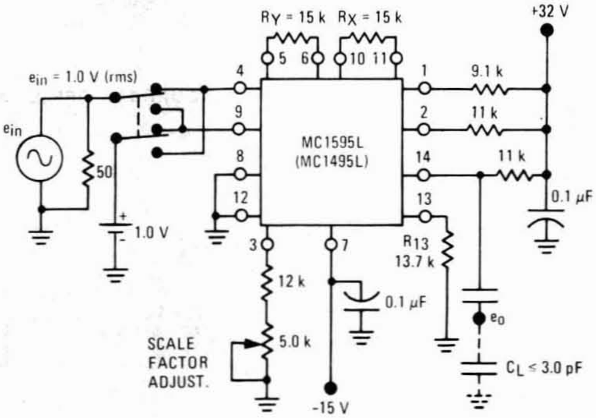

RY = 15 k
RX = 15 k
+32 V
ein = 1.0 V (rms)
ein
50
1.0 V
MC1595L
(MC1495L)
9.1 k
11 k
11 k
0.1 µF
R13
13.7 k
12 k
0.1 µF
eo
CL ≤ 3.0 pF
5.0 k
SCALE
FACTOR
ADJUST.
-15 V

**FIGURE 10 – BANDWIDTH ($R_L$ = 50 Ω)**

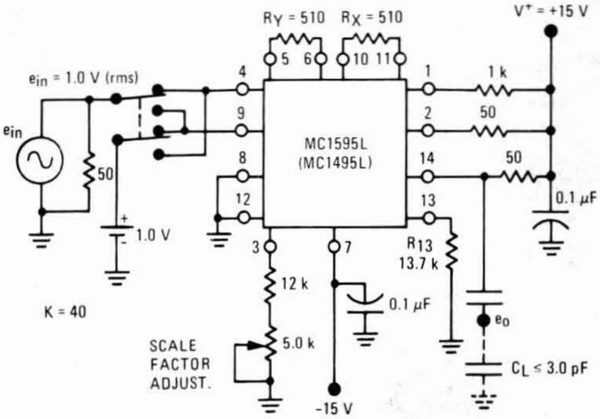
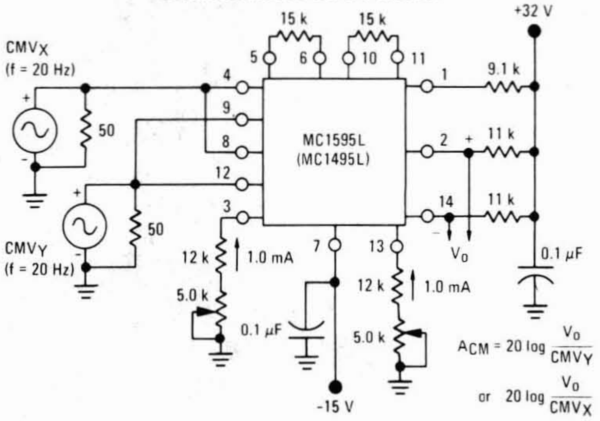
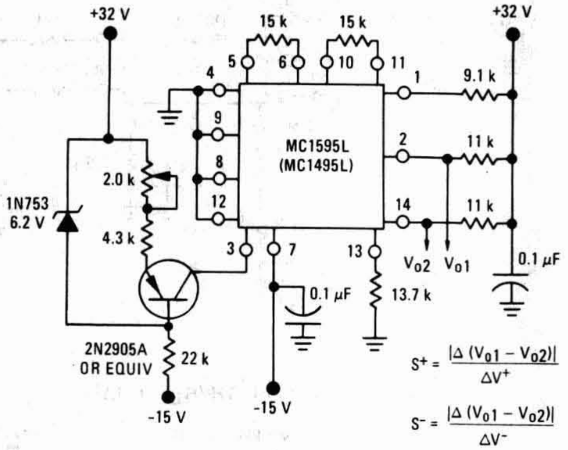

RY = 510
RX = 510
V+ = +15 V
ein = 1.0 V (rms)
ein
50
1.0 V
MC1595L
(MC1495L)
1 k
50
50
0.1 µF
R13
13.7 k
12 k
0.1 µF
eo
CL ≤ 3.0 pF
K = 40
5.0 k
SCALE
FACTOR
ADJUST.
-15 V

**FIGURE 11 – COMMON-MODE GAIN and COMMON-MODE INPUT SWING**


15 k
15 k
+32 V
CMVX
(f = 20 Hz)
50
CMVY
(f = 20 Hz)
50
MC1595L
(MC1495L)
9.1 k
11 k
11 k
Vo
0.1 µF
12 k
1.0 mA
12 k
1.0 mA
5.0 k
5.0 k
0.1 µF
-15 V
ACM = 20 log Vo/CMVY
or 20 log Vo/CMVX

## TEST CIRCUITS (continued)

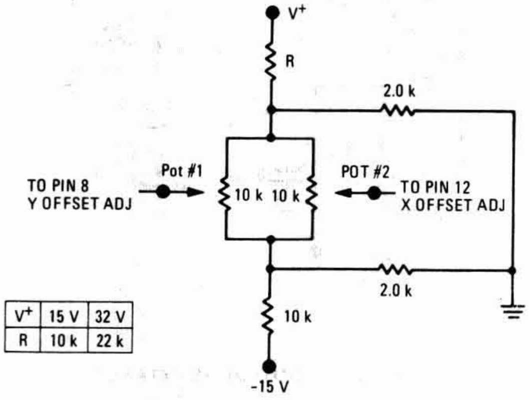
### FIGURE 12 – POWER SUPPLY SENSITIVITY


+32 V
15 k
15 k
+32 V
5
6
10
11
4
1
9.1 k
9
MC1595L
(MC1495L)
2
11 k
2.0 k
8
12
14
11 k
1N753
6.2 V
4.3 k
3
7
13
V_o2
V_o1
0.1 µF
0.1 µF
13.7 k
2N2905A
OR EQUIV
22 k
-15 V
-15 V

$$S^+ = \frac{|\Delta(V_{o1} - V_{o2})|}{\Delta V^+}$$

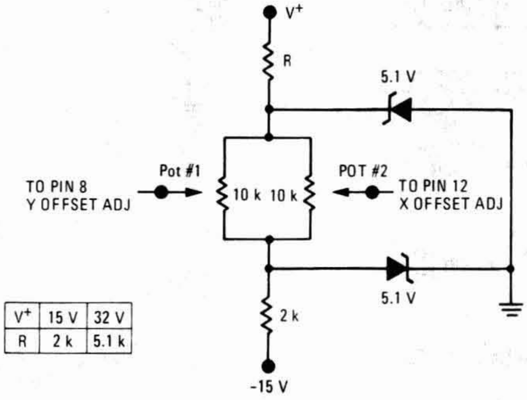
$$S^- = \frac{|\Delta(V_{o1} - V_{o2})|}{\Delta V^-}$$

### FIGURE 13 – OFFSET ADJUST CIRCUIT


V+
R
2.0 k
Pot #1
POT #2
TO PIN 8
Y OFFSET ADJ
10 k
10 k
TO PIN 12
X OFFSET ADJ
2.0 k
10 k
-15 V

| V+ | 15 V | 32 V |
|---|---|---|
| R | 10 k | 22 k |

### FIGURE 14 – OFFSET ADJUST CIRCUIT (ALTERNATE)


V+
R
5.1 V
Pot #1
POT #2
TO PIN 8
Y OFFSET ADJ
10 k
10 k
TO PIN 12
X OFFSET ADJ
5.1 V
2 k
-15 V

| V+ | 15 V | 32 V |
|---|---|---|
| R | 2 k | 5.1 k |

## TYPICAL CHARACTERISTICS

FIGURE 15 – LINEARITY versus TEMPERATURE

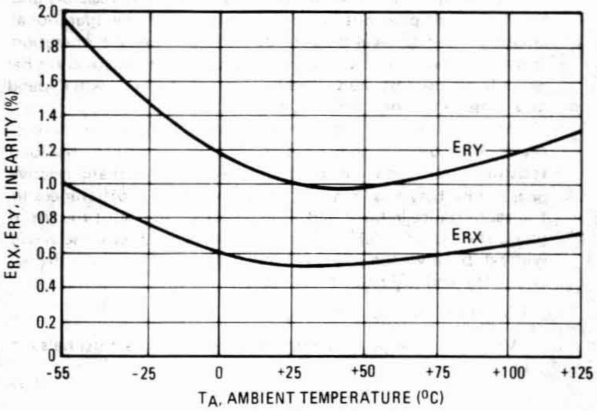


FIGURE 16 – SCALE FACTOR versus TEMPERATURE

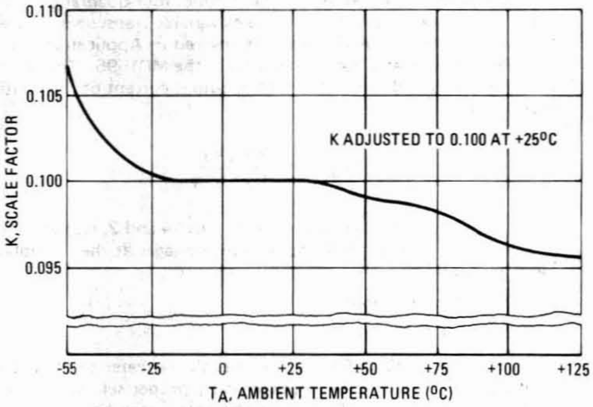


FIGURE 17 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

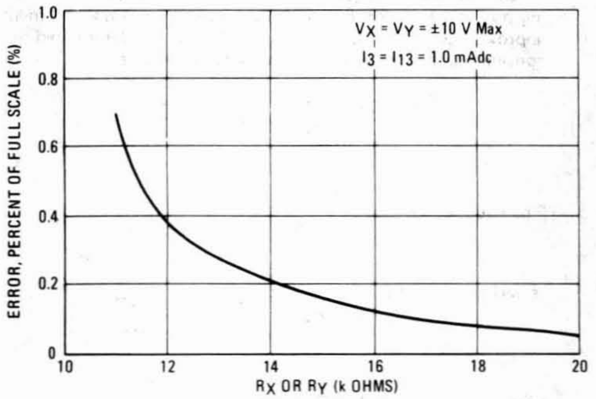


FIGURE 18 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

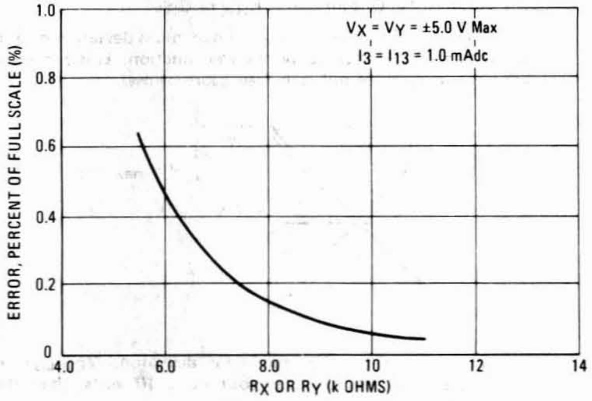
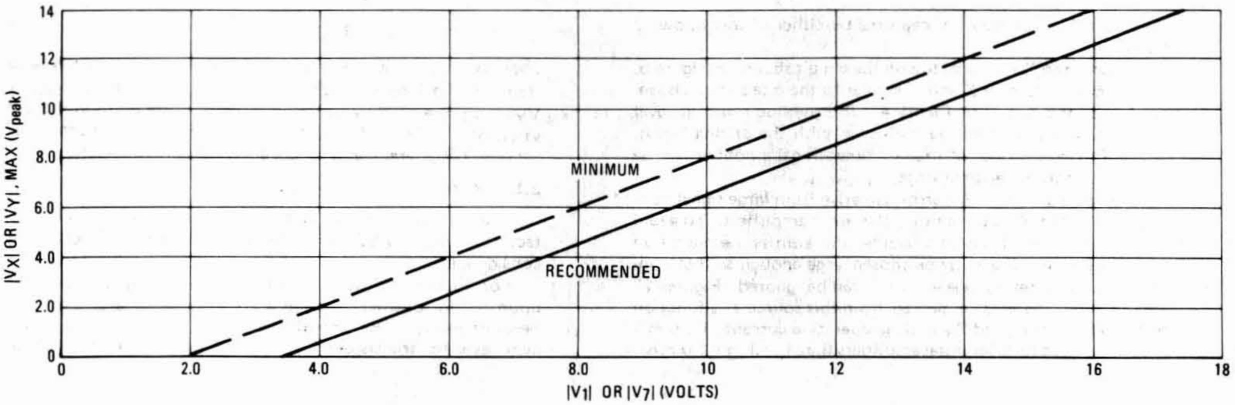


FIGURE 19 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7



## OPERATION AND APPLICATIONS INFORMATION

### 1. Theory of Operation

The MC1595 (MC1495) is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. The detailed theory of operation is covered in Application Note AN-489, Analysis and Basic Operation of the MC1595. The result of this analysis is that the differential output current of the multiplier is given by

$$I_A - I_B = \Delta I = \frac{2V_X V_Y}{R_X R_Y I_3}$$

where $I_A$ and $I_B$ are the currents into pins 14 and 2, respectively, and $V_X$ and $V_Y$ are the X and Y input voltages at the multiplier input terminals.

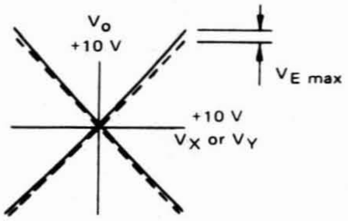
### 2. Design Considerations

#### 2.1 General

The MC1595 (MC1495) permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

#### 2.1.1 Linearity, Output Error, $E_{RX}$ or $E_{RY}$

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_{E(max)}$, is ±100 mV and the full scale output is 10 volts, then the percentage error is

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%.$$

Linearity error may be measured by either of the following methods:

1. Using an X – Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input. The peak output of the null operational amplifier will be equal to the error voltage, $V_{E(max)}$.

One source of linearity error can arise from large signal nonlinearity in the X and Y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors $R_X$ and $R_Y$ must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of $R_X$ and $R_Y$ with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

#### 2.1.2 3 dB-Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between $V_X$ and $V_Y$ results in a vector error of 5%.

#### 2.1.3 Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ maximum input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$

$$V_{Y(max)} < I_3 R_Y.$$

Exceeding this value will drive one side of the input amplifier to "cutoff" and cause non-linear operation.

Currents $I_3$ and $I_{13}$ are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then $R_X$ and $R_Y$ can be determined by considering the input signal handling requirements.

For $V_{X(max)} = V_{Y(max)} = 10$ volts;

$$R_X = R_Y > \frac{10\text{ V}}{1.0\text{ mA}} = 10\text{ k}\Omega.$$

The equation $I_A - I_B = \dfrac{2V_X V_Y}{R_X R_Y I_3}$

is derived from $I_A - I_B = \dfrac{2V_X V_Y}{(R_X + \frac{2kT}{qI_{13}})(R_Y + \frac{2kT}{qI_3})I_3}$

with the assumption $R_X \gg \dfrac{2kT}{qI_{13}}$ and $R_Y \gg \dfrac{2kT}{qI_3}$.

At $T_A = +25°C$ and $I_{13} = I_3 = 1$ mA,

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\ \Omega.$$

Therefore, with $R_X = R_Y = 10$ kΩ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to $V_1$ and $V_7$. Exceeding these limits will cause saturation or "cutoff" of the input transistors. See Step 4 of Section 3 (General Design Procedure) for further details.

#### 2.1.4 Maximum Output Voltage Swing

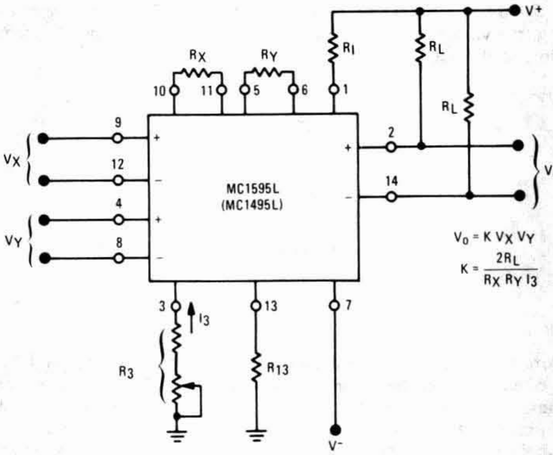
The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon $V^+$ for positive swing and upon the voltage at pin 1 for negative swing. The potential at pin 1 determines the quiescent level for transistors $Q_5$, $Q_6$, $Q_7$, and $Q_8$. This potential

## OPERATION AND APPLICATIONS INFORMATION (continued)

should be related so that negative swing at pins 2 or 14 does not saturate those transistors. See Section 3 for further information regarding selection of these potentials.

**FIGURE 20 – BASIC MULTIPLIER**



V+
RX
RY
RI
RL
RL
10
11
5
6
1
9
12
4
8
2
14
VX
VY
Vo
MC1595L
(MC1495L)
$V_o = K\,V_X\,V_Y$
$K = \frac{2R_L}{R_X\,R_Y\,I_3}$
3
13
7
I3
R3
R13
V-

If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

### 3. General Design Procedure

Selection of component values is best demonstrated by the following example: assume resistive dividers are used at the X and Y inputs to limit the maximum multiplier input to ±5.0 volts ($V_X = V_{Y\,[max]}$) for a ±10-volt input ($V_X' = V_Y'{}_{[max]}$). (See Figure 21). If an overall scale factor of 1/10 is desired, then

$$V_o = \frac{V_X'\,V_Y'}{10} = \frac{(2V_X)\,(2V_Y)}{10} = 4/10\ V_X V_Y\,.$$

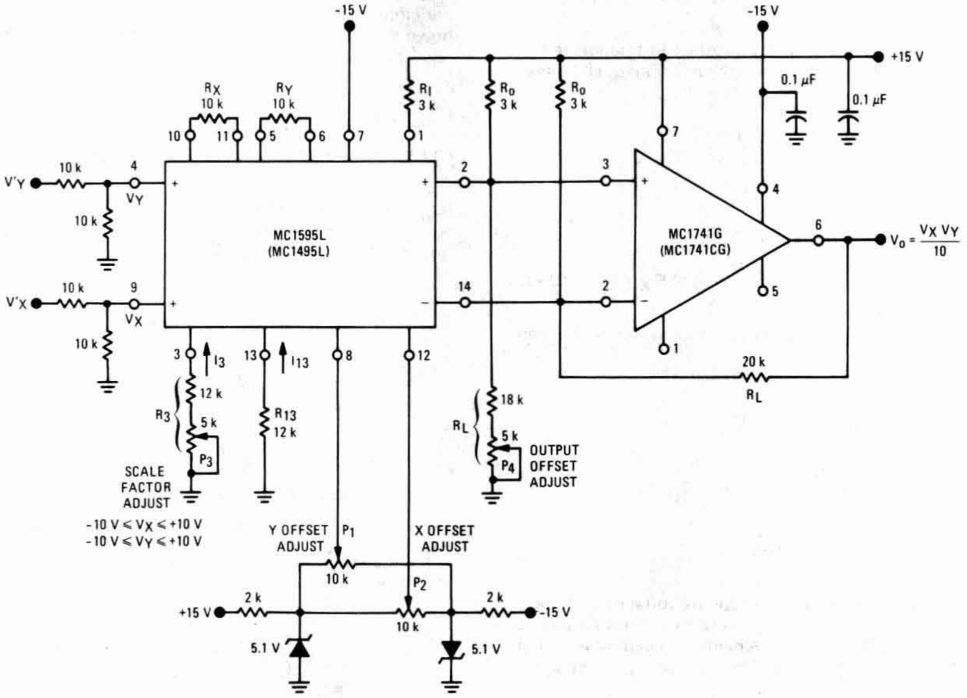
Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The first step is to select current $I_3$ and current $I_{13}$. There are no restrictions on the selection of either of these currents except the power dissipation of the device. $I_3$ and $I_{13}$ will normally be one or two milliamperes. Further, $I_3$ does not have to be equal to $I_{13}$, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1\text{ mA}.$$

To set currents $I_3$ and $I_{13}$ to the desired value, it is only necessary to connect a resistor between pin 13 and ground, and between pin 3 and ground. From the schematic shown in Figure 3,

**FIGURE 21 – MULTIPLIER WITH OP-AMPL. LEVEL SHIFT**



-15 V
-15 V
+15 V
RX
10 k
RY
10 k
RI
3 k
Ro
3 k
Ro
3 k
0.1 μF
0.1 μF
10
11
5
6
7
1
7
V'Y
10 k
4
VY
10 k
2
3
4
MC1595L
(MC1495L)
MC1741G
(MC1741CG)
6
$V_o = \frac{V_X\,V_Y}{10}$
V'X
10 k
9
VX
10 k
14
2
5
3
I3
13
I13
8
12
1
20 k
RL
12 k
R3
5 k
P3
R13
12 k
RL
18 k
5 k
P4
OUTPUT
OFFSET
ADJUST
SCALE
FACTOR
ADJUST
-10 V ≤ VX ≤ +10 V
-10 V ≤ VY ≤ +10 V
Y OFFSET
ADJUST
P1
X OFFSET
ADJUST
10 k
P2
+15 V
2 k
2 k
-15 V
10 k
5.1 V
5.1 V

## OPERATION AND APPLICATIONS INFORMATION (continued)

it can be seen that the resistor values necessary are given by:

$$R_{13} + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_{13}}$$

$$R_3 + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_3}$$

Let $V^- = -15\ V$

Then $R_{13} + 500 = \frac{14.3\ V}{1\ mA}$ or $R_{13} = 13.8\ k\Omega$

Let $R_{13} = 12\ k\Omega$

Similarly, $R_3 = 13.8\ k\Omega$

Let $R_3 = 15\ k\Omega$

However, for applications which require an accurate scale factor, the adjustment of $R_3$ and consequently, $I_3$, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor $R_3$ is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.), pins 3 and 13 can be connected together and a single resistor from pin 3 to ground can be used. In this case, the single resistor would have a value of one-half the above calculated value for $R_{13}$.

Step 2. The next step is to select $R_X$ and $R_Y$. To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13} \qquad \frac{V_Y}{R_Y} < I_3.$$

A good rule of thumb is to make $I_3R_Y \geqslant 1.5\ V_{Y(max)}$ and $I_{13}\,R_X \geqslant 1.5\ V_{X(max)}$.

The larger the $I_3R_Y$ and $I_{13}R_X$ product in relation to $V_Y$ and $V_X$ respectively, the more accurate the multiplier will be (see Figures 17 and 18).

Let $R_X = R_Y = 10\ k\Omega$

Then $I_3R_Y = 10\ V$

$I_{13}R_X = 10\ V$

since $V_{X(max)} = V_{Y(max)} = 5.0$ volts the value of $R_X = R_Y = 10\ k\Omega$ is sufficient.

Step 3. Now that $R_X$, $R_Y$ and $I_3$ have been chosen, $R_L$ can be determined:

$$K = \frac{2R_L}{R_XR_YI_3} = \frac{4}{10}$$

$$\text{or} \quad \frac{(2)\ (R_L)}{(10\ k)\ (10\ k)\ (1\ mA)} = \frac{4}{10}$$

Thus $R_L = 20\ k\Omega$.

Step 4. To determine what power-supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors $Q_1$, $Q_2$, $Q_3$ and $Q_4$ in an active region when the maximum input voltages are applied ($V_X' = V_Y' = 10$ V or $V_X = 5.0$ V, $V_Y = 5.0$ V), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors $Q_3$ and $Q_4$ are at a potential which is two diode-drops below the voltage at pin 1. Thus, the voltage at pin 1 should be about two volts higher than the maximum input voltage. Therefore, to handle +5.0 volts at the inputs, the voltage at pin 1 must be at least +7.0 volts. Let $V_1 = 9.0$ Vdc.

Since the current following into pin 1 is always equal to $2I_3$, the voltage at pin 1 can be set by placing a resistor, $R_1$ from pin 1 to the positive supply:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

Let $V^+ = +15\ V$

Then $R_1 = \frac{15\ V - 9\ V}{(2)\ (1\ mA)}$

$R_1 = 3\ k\Omega$.

Note that the voltage at the base of transistors $Q_5$, $Q_6$, $Q_7$ and $Q_8$ is one diode-drop below the voltage at pin 1. Thus, in order that these transistors stay active, the voltage at pins 2 and 14 should be approximately halfway between the voltage at pin 1 and the positive-supply voltage. For this example, the voltage at pins 2 and 14 should be approximately 11 volts.

Step 5. Level Shifting

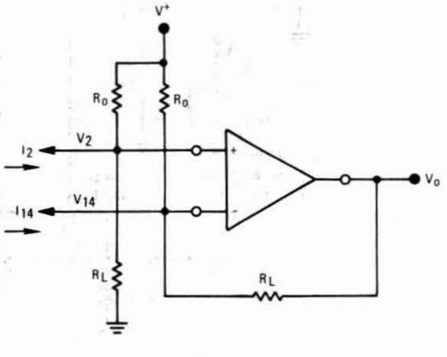
For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_o = (I_2 - I_{14})\,R_L$$

And since $I_A - I_B = I_2 - I_{14} = \frac{2I_XI_Y}{I_3} = \frac{2\,V_XV_Y}{I_3R_XR_Y}$

Then $V_o = \frac{2R_LV_X'V_Y'}{4R_XR_XI_3}$ where $V_X'V_Y'$ is the voltage at the input to the voltage dividers.

FIGURE 22 – LEVEL SHIFT CIRCUIT



## OPERATION AND APPLICATIONS INFORMATION (continued)

The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common-mode input voltage range as well as a high common-mode rejection ratio. The MC1556, and MC1741 operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents $I_2$ and $I_{14}$ will be equal to $I_{13}$. In Step 3, $R_L$ was found to be 20 kΩ and in Step 4, $V_2$ and $V_{14}$ were found to be approximately 11 volts. From this information, $R_o$ can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V_2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_o}$$

And for this example, $\frac{11\text{ V}}{20\text{ k}\Omega} + 1\text{ mA} = \frac{15\text{ V} - 11\text{ V}}{R_o}$

Solving for $R_o$, $R_o = 2.6\text{ k}\Omega$

Thus, select $R_o = 3.0\text{ k}\Omega$

For $R_o = 3.0\text{ k}\Omega$, the voltage at pins 2 and 14 is calculated to be

$$V_2 = V_{14} = 10.4\text{ volts.}$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are possible as shown in Figure 23 where $R_Y$ has been increased substantially to improve the Y linearity, and $R_X$ decreased somewhat so as not to materially affect the X linearity, this avoids increasing $R_L$ significantly in order to maintain a K of 0.1.

The versatility of the MC1595 (MC1495) allows the user to to optimize its performance for various input and output signal levels.

### 4. Offset and Scale Factor Adjustment

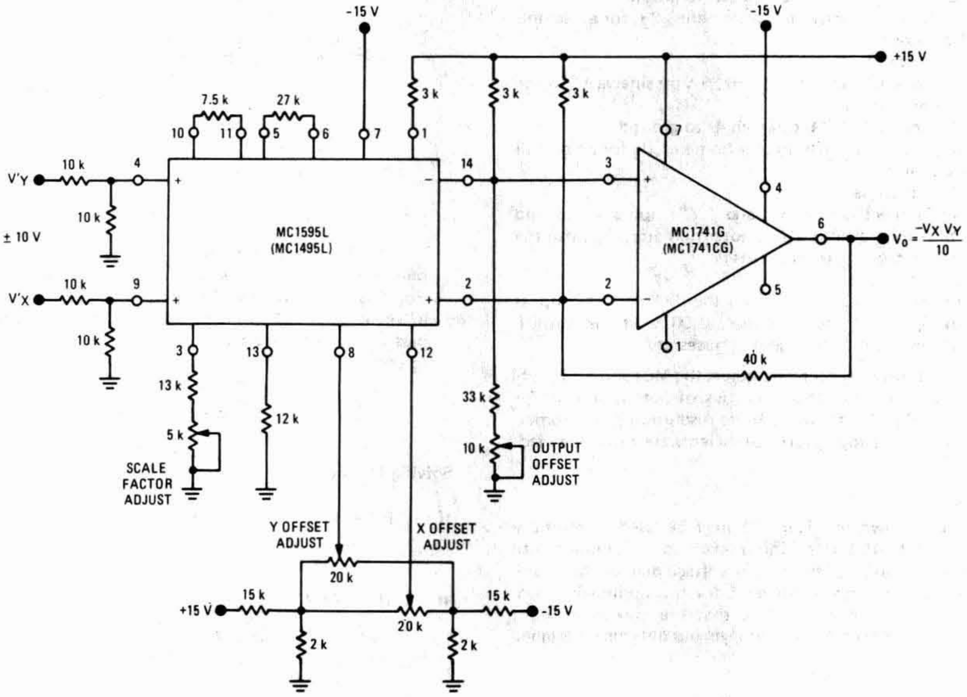
#### 4.1 Offset Voltages

Within the monolithic multiplier (Figure 3) transistor base-emitter junctions are typically matched within 1 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X-input offset voltage, Y-input offset voltage, and output-offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function:

$$V_o = K(V_X \pm V_{IOX} \pm V_{X\,off})(V_Y \pm V_{IOY} \pm V_{Y\,off}) \pm V_{oo} \qquad (1)$$

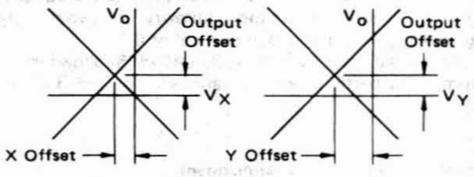
Where K = scale factor
$V_X$ = X input voltage
$V_Y$ = Y input voltage
$V_{IOX}$ = X input offset voltage
$V_{IOY}$ = Y input offset voltage
$V_{X\,off}$ = X input offset adjust voltage
$V_{Y\,off}$ = Y input offset adjust voltage
$V_{oo}$ = output offset voltage.

FIGURE 23 – MULTIPLIER WITH IMPROVED LINEARITY



## OPERATION AND APPLICATIONS INFORMATION (continued)

X, Y and Output Offset Voltages



For most dc applications, all three offset adjust potentiometers ($P_1$, $P_2$, $P_4$) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (See Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

### 4.2 Scale Factor

The scale factor, K, is set by $P_3$(Figure 21). $P_3$ varies $I_3$ which inversely controls the scale factor K. It should be noted that current $I_3$ is one-half the current through $R_1$. $R_1$ sets the bias level for $Q_5$, $Q_6$, $Q_7$, and $Q_8$ (See Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting $P_3$ over wide voltage ranges (see Section 3, General Design Procedure).

### 4.3 Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation. (See Figure 21)

1. X Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 4)
   (b) Connect "X" input (pin 9) to ground
   (c) Adjust X offset potentiometer, $P_2$, for an ac null at the output
2. Y Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 9)
   (b) Connect "Y" input (pin 4) to ground
   (c) Adjust "Y" offset potentiometer, $P_1$, for an ac null at the output
3. Output Offset
   (a) Connect both "X" and "Y" inputs to ground
   (b) Adjust output offset potentiometer, $P_4$, until the output voltage $V_o$ is zero volts dc
4. Scale Factor
   (a) Apply +10 Vdc to both the "X" and "Y" inputs
   (b) Adjust $P_3$ to achieve + 10.00 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1595 (MC1495) depends upon the characteristics of potentiometers $P_1$ through $P_4$. Multi-turn, infinite resolution potentiometers with low-temperature coefficients are recommended.

## 5. DC Applications

### 5.1 Multiply

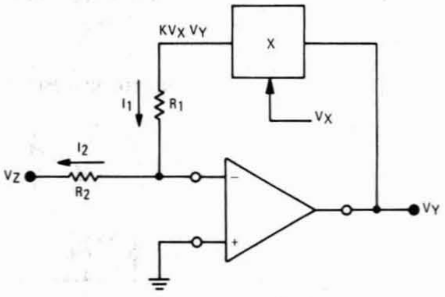
The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large – however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

### 5.2 Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is $V_o = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

1. AC Procedure:
   (a) Connect oscillator (1 kHz, 15 Vpp) to input
   (b) Monitor output at 2 kHz with tuned voltmeter and adjust $P_3$ for desired gain (be sure to peak response of the voltmeter)
   (c) Tune voltmeter to 1 kHz and adjust $P_1$ for a minimum output voltage
   (d) Ground input and adjust $P_4$ (output offset) for zero volts dc output
   (e) Repeat steps a through d as necessary.
2. DC Procedure:
   (a) Set $V_X = V_Y = 0$ V and adjust $P_4$ (output offset potentiometer) such that $V_o = 0.0$ Vdc
   (b) Set $V_X = V_Y = 1.0$ V and adjust $P_1$ (Y input offset potentiometer) such that the output voltage is +0.100 volts
   (c) Set $V_X = V_Y = 10$ Vdc and adjust $P_3$ such that the output voltage is +10.00 volts
   (d) Set $V_X = V_Y = -10$ Vdc. Repeat steps a through d as necessary.

FIGURE 24 – BASIC DIVIDE CIRCUIT



### 5.3 Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a "virtual ground" at the inverting (–) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2} \quad (1)$$

Solving for $V_Y$,

$$V_Y = \frac{-R1}{R2\,K}\,\frac{V_Z}{V_X}. \quad (2)$$

If R1 = R2

$$V_Y = \frac{-V_Z}{KV_X} \quad (3)$$

If R1 = KR2

$$V_Y = \frac{-V_Z}{V_X}. \quad (4)$$

## OPERATION AND APPLICATIONS INFORMATION (continued)

Hence, the output voltage is the ratio of $V_Z$ to $V_X$ and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be

$$V_Y = -\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X} + \frac{\Delta E}{KV_X}, \tag{5}$$

where $\Delta E$ is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of $V_Y$. For example, assume that $R1 = R2$, and $K = 1/10$. For these conditions the output of the divide circuit is given by:

$$V_Y = \frac{-10\,V_Z}{V_X} + \frac{10\,\Delta E}{V_X}. \tag{6}$$

From equation 6, it is seen that only when $V_X = 10$ V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when $V_X$ is small, (0.1 volt) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

In terms of percentage error,

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\%$$

or from equation (5),

$$\text{P.E.}_D = \frac{\dfrac{\Delta E}{KV_X}}{\left[\dfrac{R1}{R2\,K}\right]\dfrac{V_Z}{V_X}} = \left[\frac{R2}{R1}\right]\frac{\Delta E}{V_Z}. \tag{7}$$

From equation 7, the percentage error is inversely related to voltage $V_Z$ (i.e., for increasing values of $V_Z$, the percentage error decreases).

A circuit that performs the divide function is shown in Figure 25.

Two things should be emphasized concerning Figure 25.

1. The input voltage ($V'_X$) must be greater than zero and must be positive. This insures that the current out of pin 2 of the multiplier will always be in a direction compatible with the polarity of $V_Z$.
2. Pins 2 and 14 of the multiplier have been interchanged in respect to the operational amplifiers input terminals. In this instance, Figure 25 differs from the circuit connection shown in Figure 21; necessitated to insure negative feedback around the loop.

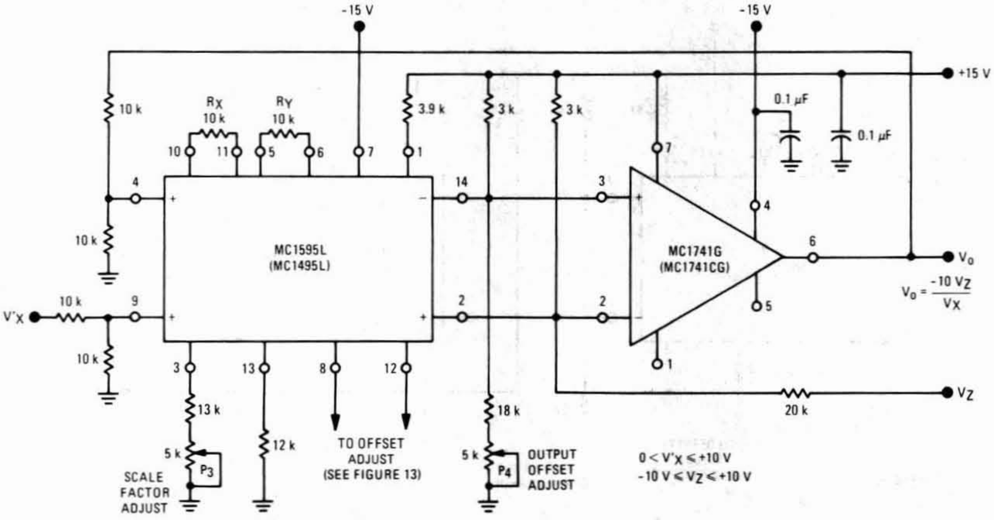
A Suggested Adjustment Procedure for the Divide Circuit

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer ($P_4$) until the output voltage ($V_o$) remains at some (not necessarily zero) constant value as $V_X'$ is varied between +1.0 volt and +10 volts.
2. Keep $V_Z$ at 0 volts, set $V_X'$ at +10 volts and adjust the Y input offset potentiometer ($P_1$) until $V_o = 0$ volts.
3. Let $V_X' = V_Z$ and adjust the X input offset potentiometer ($P_2$) until the output voltage remains at some (not necessarily − 10 volts) constant value as $V_Z = V_X'$ is varied between +1.0 and +10 volts.
4. Keep $V_X' = V_Z$ and adjust the scale factor potentiometer ($P_3$) until the average value of $V_o$ is − 10 volts as $V_Z = V_X'$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

### 5.4 Square Root

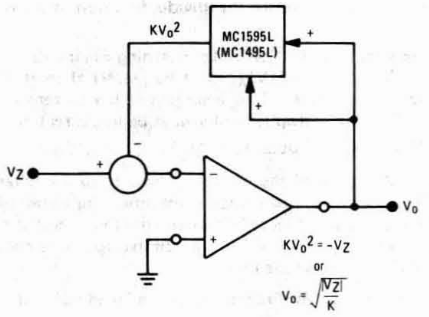
A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function

FIGURE 25 – DIVIDE CIRCUIT



## OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 26 – BASIC SQUARE ROOT CIRCUIT


$KV_0^2$
MC1595L
(MC1495L)
+
+
–
+
$V_Z$
–
+
$V_0$
$KV_0{}^2 = -V_Z$
or
$V_0 = \sqrt{\frac{|V_Z|}{K}}$

as indicated in Figure 26. This circuit may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch-up.

This circuit also may be adjusted in the closed-loop mode as follows:

1. Set $V_Z$ to –0.01 volts and adjust $P_4$ (output offset) for $V_o$ = +0.316 volts, being careful to approach the output from the positive side to preclude the effect of the output diode clamping.
2. Set $V_Z$ to –0.9 volts and adjust $P_2$ (X adjust) for $V_o$ = +3.0 volts.
3. Set $V_Z$ to –10 volts and adjust $P_3$ (scale factor adjust) for $V_o$ = +10 volts.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

### 6. AC Applications

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize dc multiplication operation, can hinder ac applications.

6.1 Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a dc term, which can be removed with ac coupling.

$$e_0 = KE^2 \cos^2 \omega t$$

$$e_0 = \frac{KE^2}{2} (1 + \cos 2\omega t).$$

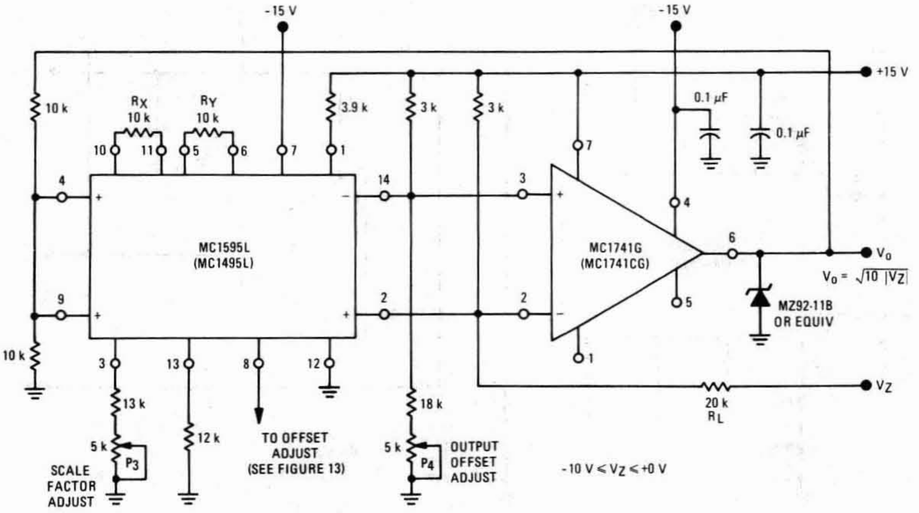
A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level-shift amplifier. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ± 15-volt supplies are used. An input dynamic range of 5.0 volts peak-to-peak is allowed. The circuit generates wave-forms that are double frequency; less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

A slightly modified version of the MC1595 (MC1495) – the MC1596 (MC1496) – has been successfully used as a doubler to obtain 400 MHz. (See Figure 28.)

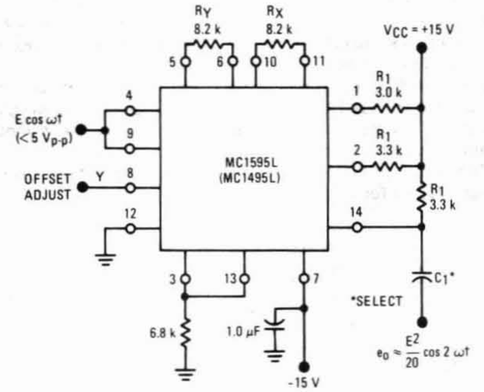
6.2 Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

FIGURE 27 – SQUARE ROOT CIRCUIT


-15 V
-15 V
+15 V
10 k
$R_X$
10 k
$R_Y$
10 k
3.9 k
3 k
3 k
0.1 µF
0.1 µF
10
11
5
6
7
1
7
4
14
3
4
MC1595L
(MC1495L)
MC1741G
(MC1741CG)
6
$V_o$
$V_o = \sqrt{10\ |V_Z|}$
9
2
2
5
MZ92-11B
OR EQUIV
10 k
3
13
8
12
1
$V_Z$
13 k
18 k
20 k
$R_L$
5 k
$P_3$
12 k
TO OFFSET
ADJUST
(SEE FIGURE 13)
5 k
$P_4$
OUTPUT
OFFSET
ADJUST
SCALE
FACTOR
ADJUST
$-10\ V \leqslant V_Z \leqslant +0\ V$

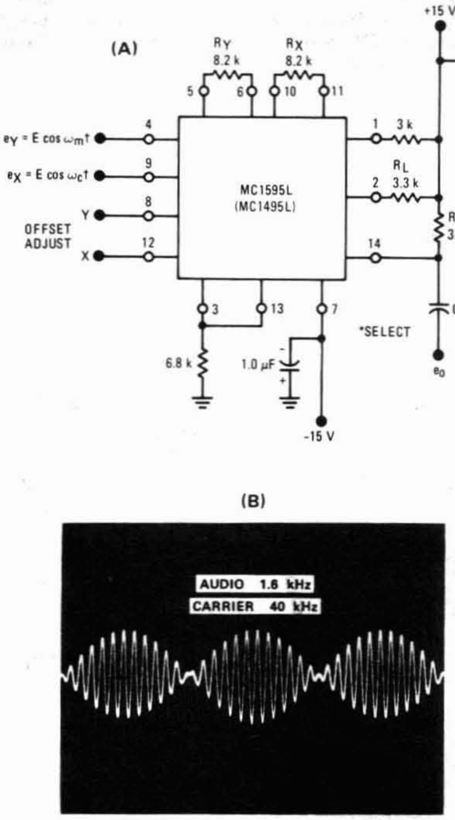
## OPERATION AND APPLICATIONS INFORMATION (continued)

### FIGURE 28 – FREQUENCY DOUBLER



When two equal cosine waves are applied to X and Y, the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal, output was 20 kHz.

### FIGURE 29 – BALANCED MODULATOR



The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)(E_c \cos \omega_c t) =$$

$$\frac{KE_cE_m}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where $\omega_c$ is the carrier frequency, $\omega_m$ is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier; a higher operating frequency results.

A problem common to communications is to extract the intelligence from single-sideband received signal. The ssb signal is of the form

$$e_{ssb} = A \cos(\omega_c + \omega_m)t$$

and if multiplied by the appropriate carrier waveform, $\cos \omega_c t$,

$$e_{ssb}e_{carrier} = \frac{AK}{2}[\cos(2\omega_c + \omega_m)t + \cos(\omega_c)t].$$

If the frequency of the band-limited carrier signal, $\omega_c$, is ascertained in advance the designer can insert a low-pass filter and obtain the (AK/2) ($\cos \omega_c t$) term with ease. He also can use an operational amplifier for a combination level shift-active filter, as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low-pass filter.

### 6.3 Amplitude Modulation

The multiplier performs amplitude modulation, similar to balanced modulation, when a dc term is added to the modulating signal with the Y offset adjust potentiometer. (See Figure 30.)

Here, the identity is

$$E_m(1 + m \cos \omega_m t)E_c \cos \omega_c t = KE_mE_c \cos \omega_c t +$$

$$\frac{KE_mE_cm}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

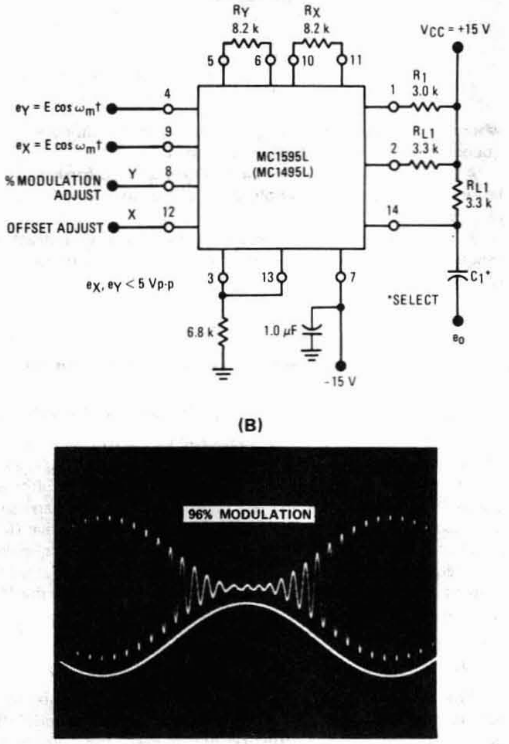
where m indicates the degree of modulation. Since m is adjustable, via potentiometer $P_1$, 100% modulation is possible. Without extensive tweaking, 96% modulation may be obtained where $\omega_c$ and $\omega_m$ are the same as in the balanced-modulator example.

### 6.4 Linear Gain Control

To obtain linear gain control, the designer can feed to one of the two MC1595 (MC1495) inputs a signal that will vary the unit's gain. The following example demonstrates the feasibility of this application. Suppose a 200 kHz sine wave, 1.0 volt peak-to-peak, is the signal to which a gain control will be added. The dynamic range of the control voltage $V_C$ is 0 to +1.0 volt. These must be ascertained and the proper values of $R_X$ and $R_Y$ can be selected for optimum performance. For the 200-kHz operating frequency, load resistors of 100 ohms were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency. (See Figure 31.)

## OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 30 – AMPLITUDE MODULATION


RY
8.2 k
RX
8.2 k
VCC = +15 V
5
6
10
11
R1
3.0 k
1
eY = E cos ωmt
4
eX = E cos ωmt
9
RL1
3.3 k
2
MC1595L
(MC1495L)
% MODULATION ADJUST
Y
8
RL1
3.3 k
X
12
14
OFFSET ADJUST
eX, eY < 5 Vp-p
3
13
7
C1*
*SELECT
6.8 k
1.0 μF
eo
-15 V
96% MODULATION

(B)

The signal is applied to the unit's Y input. Since the total input range is limited to 1.0 volt p-p, a 2.0-volt swing, a current source of 2.0 mA and an $R_Y$ value of 1.0 kilohm is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X input varies between 0 and +1.0 volt, the current source selected was 1.0 mA and the $R_X$ value chosen was 2.0 kilohms. This also insures linear operation over the X input dynamic range.

Choosing $R_L = 100$ assures wide-bandwidth operation. Hence, the scale factor for this configuration is

$$K = \frac{R_L}{R_X R_Y I_3}$$

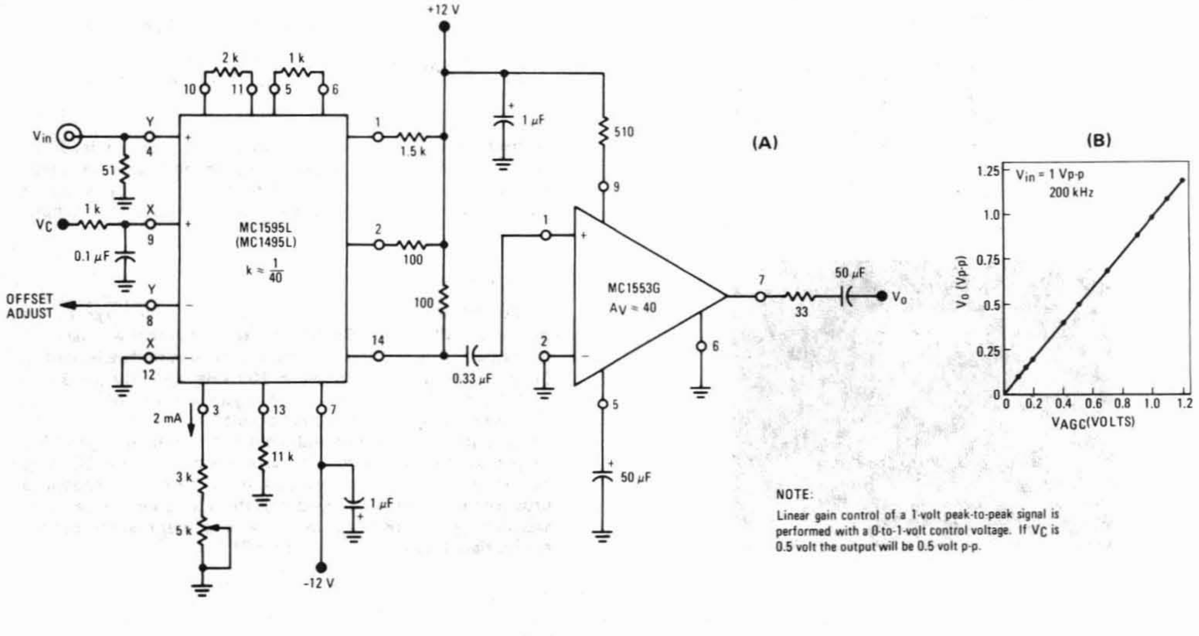
$$= \frac{100}{(2\text{ k})(1\text{ k})(2 \times 10^{+3})} \; V^{-1}$$

$$= \frac{1}{40} \; V^{-1}.$$

The 2 in the numerator of the equation is missing in this scale-factor expression because the output is single-ended and ac coupled.

To recover the gain, an MC1552 video amplifier with a gain of 40 is used. An operational amplifier also could have been used with frequency compensation to allow a gain of 40 at 200 kHz. The MC1539 operational amplifier can be tailored for this use; and the MC1520 operational amplifier does it directly.

FIGURE 31 – LINEAR GAIN CONTROL


+12 V
2 k
1 k
10
11
5
6
Vin
Y
4
+
1
1.5 k
1 μF
510
51
1 k
X
VC
9
0.1 μF
MC1595L
(MC1495L)
k ≈ 1/40
2
100
9
1
+
OFFSET ADJUST
Y
8
100
MC1553G
AV ≈ 40
7
50 μF
33
Vo
X
12
14
0.33 μF
2
6
2 mA
3
13
7
5
11 k
3 k
5 k
1 μF
50 μF
-12 V
1.25
Vin = 1 Vp-p
200 kHz
1.0
0.75
Vo (Vp-p)
0.5
0.25
0
0
0.2
0.4
0.6
0.8
1.0
1.2
VAGC(VOLTS)

(A)

(B)

NOTE:
Linear gain control of a 1-volt peak-to-peak signal is performed with a 0-to-1-volt control voltage. If $V_C$ is 0.5 volt the output will be 0.5 volt p-p.

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1496D | 0°C to +70°C | SO-14 |
| MC1496G | 0°C to +70°C | Metal Can |
| MC1496L | 0°C to +70°C | Ceramic DIP |
| MC1496P | 0°C to +70°C | Plastic DIP |
| MC1596G | −55°C to +125°C | Metal Can |
| MC1596L | −55°C to +125°C | Ceramic DIP |

# MC1496
# MC1596

## Specifications and Applications Information

## BALANCED MODULATOR — DEMODULATOR

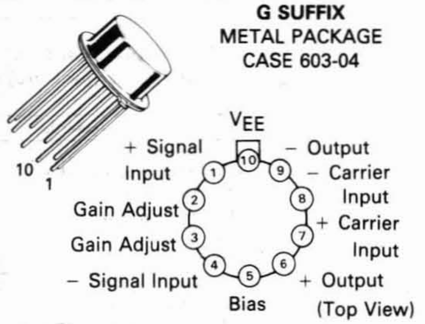
**SILICON MONOLITHIC INTEGRATED CIRCUIT**

## BALANCED MODULATOR – DEMODULATOR

. . . designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN-531 for additional design information.

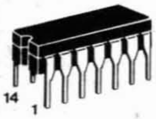
- Excellent Carrier Suppression – 65 dB typ @ 0.5 MHz
  – 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common-Mode Rejection – 85 dB typ

**G SUFFIX**
METAL PACKAGE
CASE 603-04



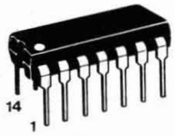
10
1
VEE
+ Signal Input
Gain Adjust
Gain Adjust
− Signal Input
Bias
+ Output
+ Carrier Input
− Carrier Input
− Output
1
2
3
4
5
6
7
8
9
10
(Top View)

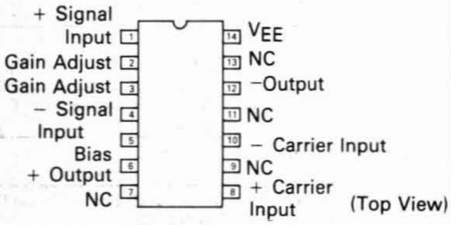
**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02



**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14

**P SUFFIX**
PLASTIC
PACKAGE
CASE 646-05





+ Signal Input
Gain Adjust
Gain Adjust
− Signal Input
Bias
+ Output
NC
1
2
3
4
5
6
7
14
13
12
11
10
9
8
VEE
NC
−Output
NC
− Carrier Input
NC
+ Carrier Input
(Top View)

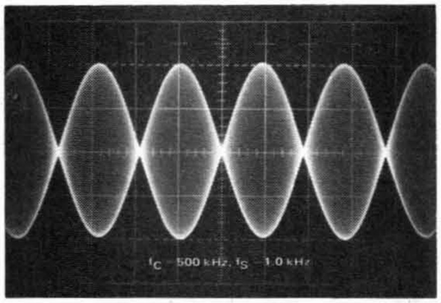


FIGURE 1 – SUPPRESSED-CARRIER OUTPUT WAVEFORM

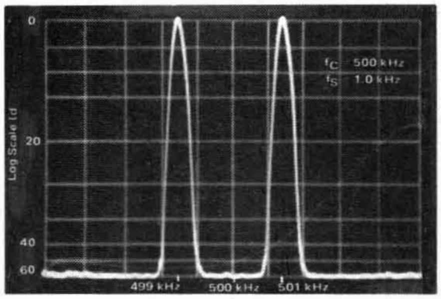


FIGURE 2 – SUPPRESSED-CARRIER SPECTRUM

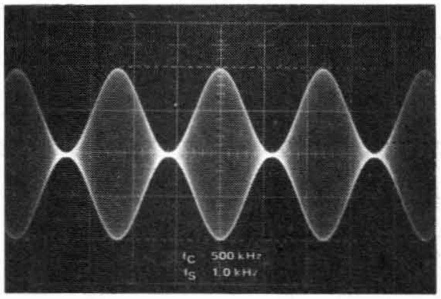
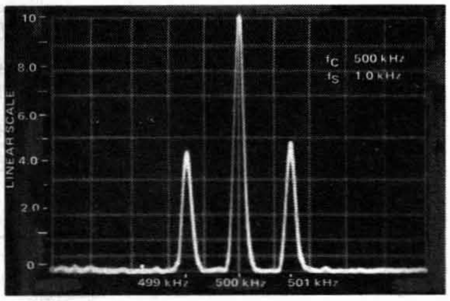


FIGURE 3 – AMPLITUDE-MODULATION OUTPUT WAVEFORM

FIGURE 4 – AMPLITUDE-MODULATION SPECTRUM



**MAXIMUM RATINGS*** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Applied Voltage<br>($V_6 - V_7$, $V_8 - V_1$, $V_9 - V_7$, $V_9 - V_8$, $V_7 - V_4$, $V_7 - V_1$, $V_8 - V_4$, $V_6 - V_8$, $V_2 - V_5$, $V_3 - V_5$) | $\Delta V$ | 30 | Vdc |
| Differential Input Signal | $V_7 - V_8$<br>$V_4 - V_1$ | +5.0<br>$\pm(5 + I_5 R_e)$ | Vdc |
| Maximum Bias Current | $I_5$ | 10 | mA |
| Thermal Resistance, Junction to Air | $R_{\theta JA}$ | | °C/W |
| Ceramic Dual In-Line Package | | 180 | |
| Plastic Dual In-Line Package | | 100 | |
| Metal Package | | 200 | |
| Operating Temperature Range | $T_A$ | | °C |
| MC1496 | | 0 to +70 | |
| MC1596 | | -55 to +125 | |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS*** ($V_{CC}$ = +12 Vdc, $V_{EE}$ = -8.0 Vdc, $I_5$ = 1.0 mAdc, $R_L$ = 3.9 kΩ, $R_e$ = 1.0 kΩ, $T_A$ = +25°C unless otherwise noted) (All input and output characteristics are single-ended unless otherwise noted.)

| | | | | MC1596 | | | MC1496 | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Characteristic** | **Fig** | **Note** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Carrier Feedthrough | 5 | 1 | $V_{CFT}$ | | | | | | | μV(rms) |
| $V_C$ = 60 mV(rms) sine wave and $f_C$ = 1.0 kHz | | | | – | 40 | – | – | 40 | – | |
| offset adjusted to zero $f_C$ = 10 MHz | | | | – | 140 | – | – | 140 | – | |
| $V_C$ = 300 mVp-p square wave: | | | | | | | | | | mV(rms) |
| offset adjusted to zero $f_C$ = 1.0 kHz | | | | – | 0.04 | 0.2 | – | 0.04 | 0.4 | |
| offset not adjusted $f_C$ = 1.0 kHz | | | | – | 20 | 100 | – | 20 | 200 | |
| Carrier Suppression | 5 | 2 | $V_{CS}$ | | | | | | | dB |
| $f_S$ = 10 kHz, 300 mV(rms) | | | | | | | | | | |
| $f_C$ = 500 kHz, 60 mV(rms) sine wave | | | | 50 | 65 | – | 40 | 65 | – | |
| $f_C$ = 10 MHz, 60 mV(rms) sine wave | | | | – | 50 | – | – | 50 | – | k |
| Transadmittance Bandwidth (Magnitude) ($R_L$ = 50 ohms) | 8 | 8 | $BW_{3dB}$ | | | | | | | MHz |
| Carrier Input Port, $V_C$ = 60 mV(rms) sine wave $f_S$ = 1.0 kHz, 300 mV(rms) sine wave | | | | – | 300 | – | – | 300 | – | |
| Signal Input Port, $V_S$ = 300 mV(rms) sine wave $\lvert V_C \rvert$ = 0.5 Vdc | | | | – | 80 | – | – | 80 | – | |
| Signal Gain $V_S$ = 100 mV(rms), f = 1.0 kHz; $\lvert V_C \rvert$ = 0.5 Vdc | 10 | 3 | $A_{VS}$ | 2.5 | 3.5 | – | 2.5 | 3.5 | – | V/V |
| Single-Ended Input Impedance, Signal Port, f = 5.0 MHz | 6 | – | | | | | | | | |
| Parallel Input Resistance | | | $r_{ip}$ | – | 200 | – | – | 200 | – | kΩ |
| Parallel Input Capacitance | | | $c_{ip}$ | – | 2.0 | – | – | 2.0 | – | pF |
| Single-Ended Output Impedance, f = 10 MHz | 6 | – | | | | | | | | |
| Parallel Output Resistance | | | $r_{op}$ | – | 40 | – | – | 40 | – | kΩ |
| Parallel Output Capacitance | | | $c_{op}$ | – | 5.0 | – | – | 5.0 | – | pF |
| Input Bias Current | 7 | – | | | | | | | | μA |
| $I_{bS} = \frac{I_1 + I_4}{2}$; $I_{bC} = \frac{I_7 + I_8}{2}$ | | | $I_{bS}$<br>$I_{bC}$ | –<br>– | 12<br>12 | 25<br>25 | –<br>– | 12<br>12 | 30<br>30 | |
| Input Offset Current | 7 | – | | | | | | | | μA |
| $I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$ | | | $\lvert I_{ioS} \rvert$<br>$\lvert I_{ioC} \rvert$ | –<br>– | 0.7<br>0.7 | 5.0<br>5.0 | –<br>– | 0.7<br>0.7 | 7.0<br>7.0 | |
| Average Temperature Coefficient of Input Offset Current ($T_A$ = -55°C to +125°C) | 7 | – | $\lvert TC_{Iio} \rvert$ | – | 2.0 | – | – | 2.0 | – | nA/°C |
| Output Offset Current ($I_6 - I_9$) | 7 | – | $\lvert I_{oo} \rvert$ | – | 14 | 50 | – | 14 | 80 | μA |
| Average Temperature Coefficient of Output Offset Current ($T_A$ = -55°C to +125°C) | 7 | – | $\lvert TC_{Ioo} \rvert$ | – | 90 | – | – | 90 | – | nA/°C |
| Common-Mode Input Swing, Signal Port, $f_S$ = 1.0 kHz | 9 | 4 | CMV | – | 5.0 | – | – | 5.0 | – | Vp-p |
| Common-Mode Gain, Signal Port, $f_S$ = 1.0 kHz, $\lvert V_C \rvert$ = 0.5 Vdc | 9 | – | ACM | – | -85 | – | – | -85 | – | dB |
| Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9) | 10 | – | $V_o$ | – | 8.0 | – | – | 8.0 | – | Vdc |
| Differential Output Voltage Swing Capability | 10 | – | $V_{out}$ | – | 8.0 | – | – | 8.0 | – | Vp-p |
| Power Supply Current | 7 | 6 | | | | | | | | mAdc |
| $I_6 + I_9$ | | | $I_{CC}$ | – | 2.0 | 3.0 | – | 2.0 | 4.0 | |
| $I_{10}$ | | | $I_{EE}$ | – | 3.0 | 4.0 | – | 3.0 | 5.0 | |
| DC Power Dissipation | 7 | 5 | $P_D$ | – | 33 | – | – | 33 | – | mW |

*** Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.**

## GENERAL OPERATING INFORMATION *

**Note 1 – Carrier Feedthrough**

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer ($R_1$ of Figure 5).

**Note 2 – Carrier Suppression**

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, $V_S$. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Note 3 and Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

**Note 3 – Signal Gain and Maximum Input Level**

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \quad \text{where } r_e = \frac{26\text{ mV}}{I_5\text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" ($V_C$ = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by $R_E$ and the bias current $I_5$

$$V_S \leq I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, $V_S$ corresponds to a maximum value of 1 volt peak.

**Note 4 – Common-Mode Swing**

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

**Note 5 – Power Dissipation**

Power dissipation, $P_D$, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_9 = V_6$, $I_5 = I_6 = I_9$ and ignoring base current, $P_D = 2\,I_5\,(V_6 - V_{10}) + I_5\,(V_5 - V_{10})$ where subscripts refer to pin numbers.

**Note 6 – Design Equations**

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions. See Note 3 for $R_e$ equation.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_9$$

$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V^- - \phi}{I_5} - 500\ \Omega \quad \text{where: } R_5 \text{ is the resistor between pin 5 and ground}$$

$$\phi = 0.75\text{ V at } T_A = +25^{\circ}\text{C}$$

The MC1596 has been characterized for the condition $I_5$ = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L$$

**Note 7 – Biasing**

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30\text{ Vdc} \geq [(V_6, V_9) - (V_7, V_8)] \geq 2\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_7, V_8) - (V_1, V_4)] \geq 2.7\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7\text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_9, \quad V_7 = V_8, \quad V_1 = V_4$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

**Note 8 – Transadmittance Bandwidth**

Carrier transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$y_{21C} = \frac{i_o\text{ (each sideband)}}{v_s\text{ (signal)}}\bigg|\ V_o = 0$$

Signal transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$y_{21S} = \frac{i_o\text{ (signal)}}{v_s\text{ (signal)}}\bigg|\ V_c = 0.5\text{ Vdc},\ V_o = 0$$

---

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

**Note 9 – Coupling and Bypass Capacitors $C_1$ and $C_2$**

Capacitors $C_1$ and $C_2$ (Figure 5) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

**Note 10 – Output Signal, $V_o$**

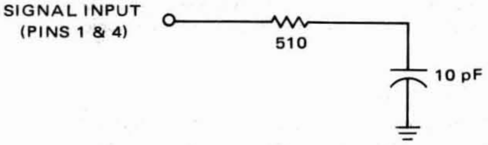
The output signal is taken from pins 6 and 9, either balanced or single-ended. Figure 12 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

**Note 11 – Negative Supply, $V_{EE}$**

$V_{EE}$ should be dc only. The insertion of an RF choke in series with $V_{EE}$ can enhance the stability of the internal current sources.

**Note 12 – Signal Port Stability**

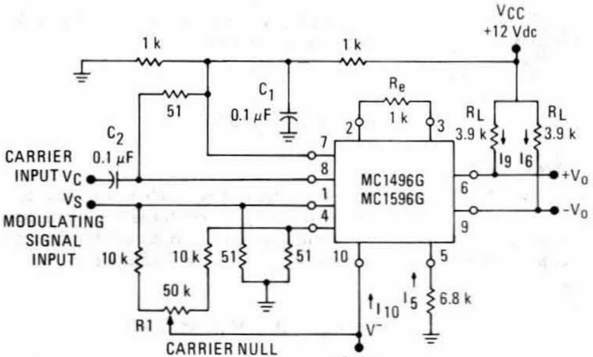
Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.


SIGNAL INPUT
(PINS 1 & 4)
510
10 pF

An alternate method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 1 and 4. In this case input current drift may cause serious degradation of carrier suppression.

## TEST CIRCUITS

FIGURE 5 – CARRIER REJECTION AND SUPPRESSION


VCC
+12 Vdc
1 k
1 k
51
C1
0.1 µF
Re
1 k
RL
3.9 k
RL
3.9 k
I9
I6
C2
CARRIER INPUT VC
0.1 µF
VS
MODULATING SIGNAL INPUT
10 k
10 k
51
51
50 k
R1
CARRIER NULL
MC1496G
MC1596G
2
3
7
8
1
4
6
9
10
5
+Vo
-Vo
I10
I5
6.8 k
V⁻
-8 Vdc
VEE

NOTE: Shielding of input and output leads may be needed to properly perform these tests.

FIGURE 6 – INPUT-OUTPUT IMPEDANCE

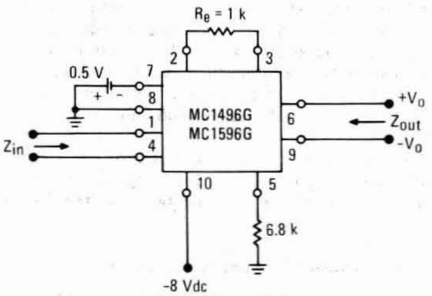

Re = 1 k
2
3
0.5 V
7
8
1
4
Zin
MC1496G
MC1596G
6
9
+Vo
Zout
-Vo
10
5
6.8 k
-8 Vdc

FIGURE 7 – BIAS AND OFFSET CURRENTS

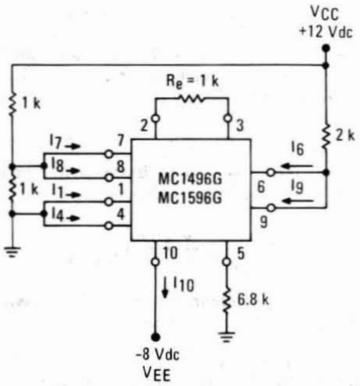
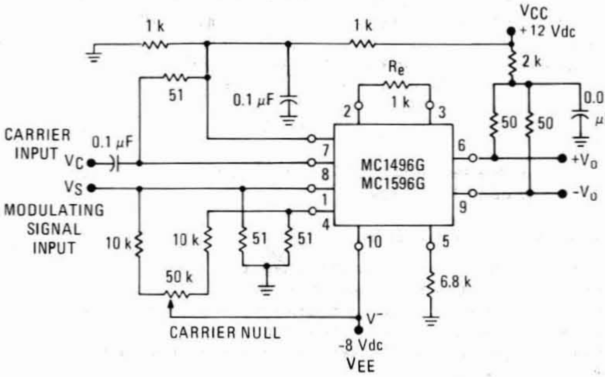

VCC
+12 Vdc
1 k
1 k
Re = 1 k
2
3
I7
I8
I1
I4
7
8
1
4
MC1496G
MC1596G
I6
I9
6
9
2 k
10
5
I10
6.8 k
-8 Vdc
VEE

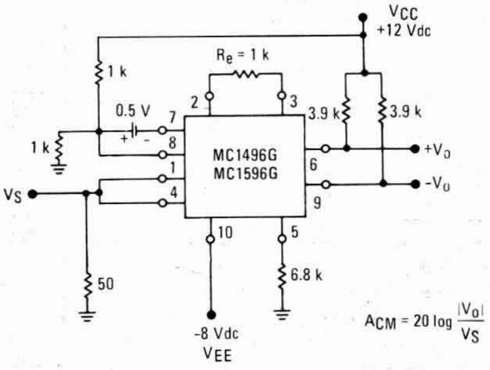
FIGURE 8 – TRANSCONDUCTANCE BANDWIDTH


VCC
+12 Vdc
1 k
1 k
2 k
51
0.1 µF
Re
1 k
50
50
0.01 µF
CARRIER INPUT VC
0.1 µF
VS
MODULATING SIGNAL INPUT
10 k
10 k
51
51
50 k
CARRIER NULL
MC1496G
MC1596G
2
3
7
8
1
4
6
9
10
5
+Vo
-Vo
6.8 k
V⁻
-8 Vdc
VEE

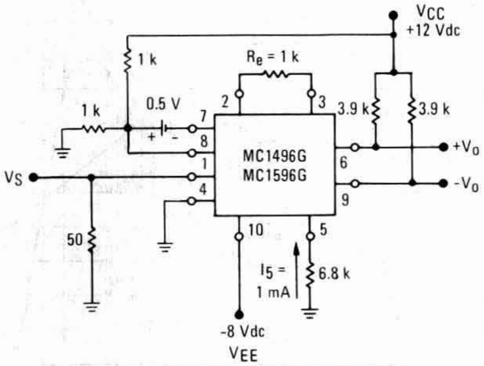
NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

## TEST CIRCUITS (continued)

### FIGURE 9 – COMMON-MODE GAIN


VCC
+12 Vdc
Re = 1 k
1 k
0.5 V
2
3
7
8
1
4
1 k
3.9 k
3.9 k
MC1496G
MC1596G
6
9
10
5
+Vo
-Vo
VS
50
6.8 k
-8 Vdc
VEE
ACM = 20 log |Vo| / VS

### FIGURE 10 – SIGNAL GAIN AND OUTPUT SWING

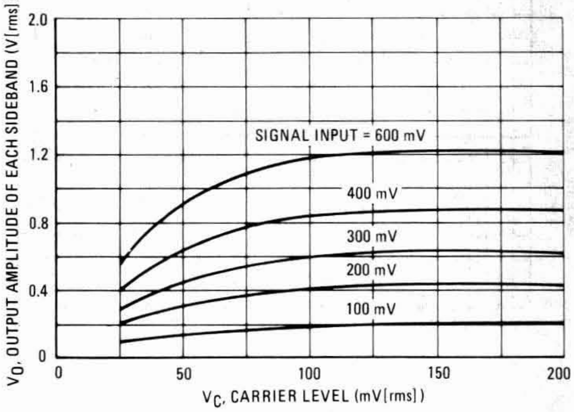

VCC
+12 Vdc
1 k
Re = 1 k
1 k
0.5 V
2
3
7
8
1
4
3.9 k
3.9 k
MC1496G
MC1596G
6
9
+Vo
-Vo
VS
50
10
5
I5 = 1 mA
6.8 k
-8 Vdc
VEE

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

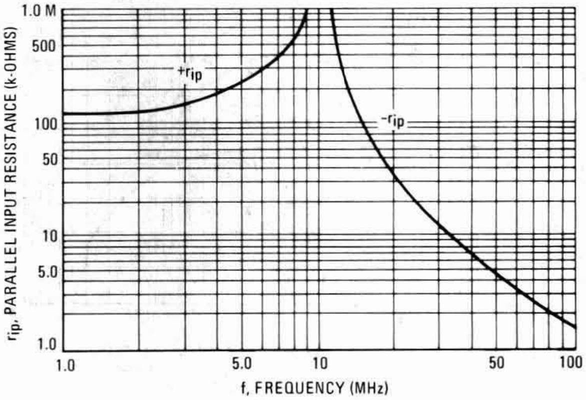
## TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, $f_C$ = 500 kHz (sine wave), $V_C$ = 60 mV(rms), $f_S$ = 1 kHz, $V_S$ = 300 mV(rms), $T_A$ = +25°C unless otherwise noted.

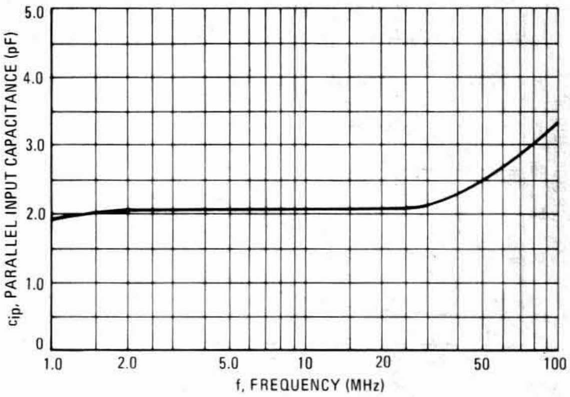
### FIGURE 11 – SIDEBAND OUTPUT versus CARRIER LEVELS



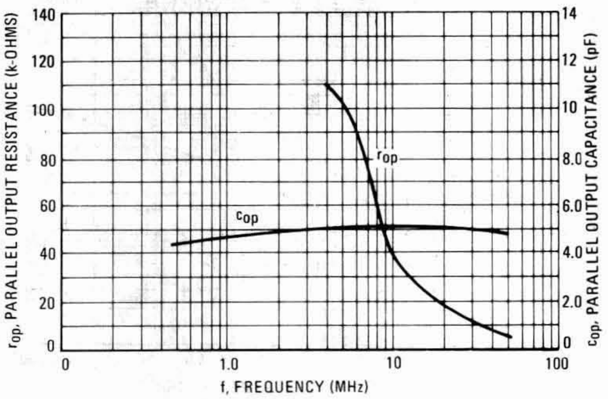
### FIGURE 12 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY



### FIGURE 13 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY



### FIGURE 14 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



## TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, $f_C$ = 500 kHz (sine wave), $V_C$ = 60 mV(rms), $f_S$ = 1 kHz, $V_S$ = 300 mV(rms), $T_A$ = +25°C unless otherwise noted.

FIGURE 15 – SIDEBAND AND SIGNAL PORT TRANSADMITTANCES versus FREQUENCY

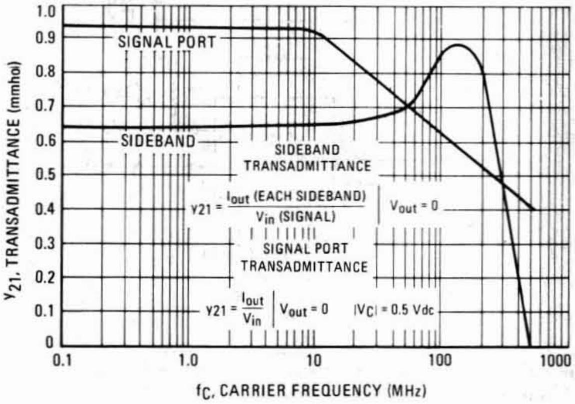


FIGURE 16 – CARRIER SUPPRESSION versus TEMPERATURE

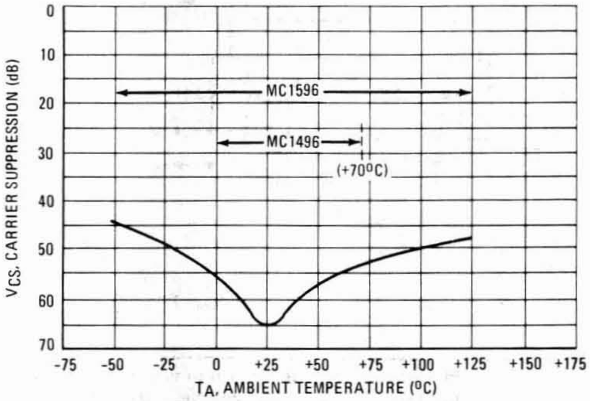


FIGURE 17 – SIGNAL-PORT FREQUENCY RESPONSE

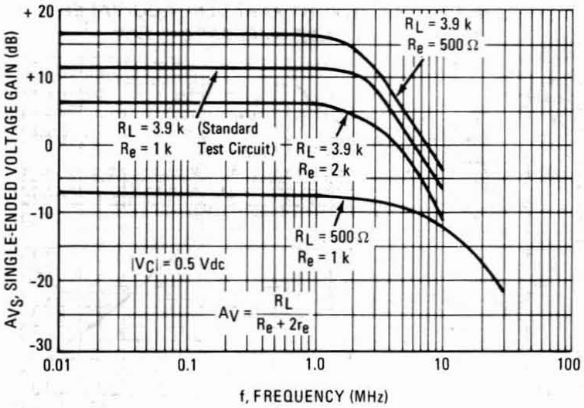


FIGURE 18 – CARRIER SUPPRESSION versus FREQUENCY

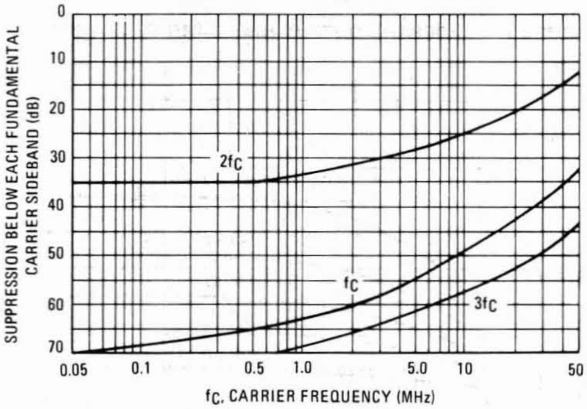


FIGURE 19 – CARRIER FEEDTHROUGH versus FREQUENCY

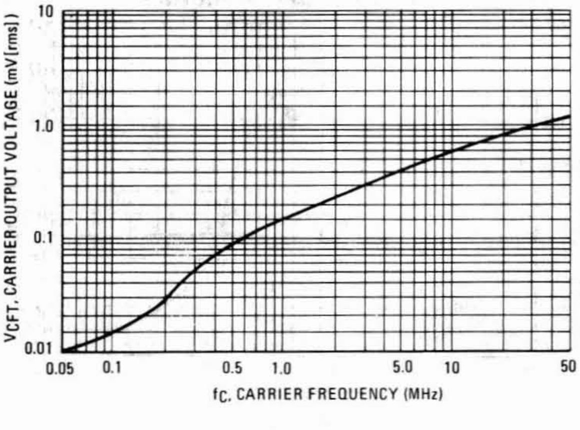
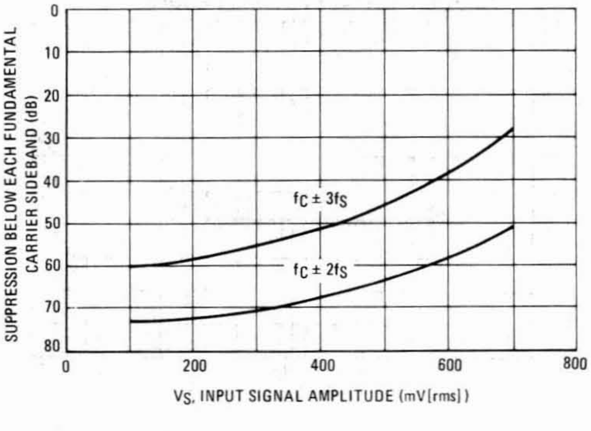


FIGURE 20 – SIDEBAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



## TYPICAL CHARACTERISTICS (continued)

FIGURE 21 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

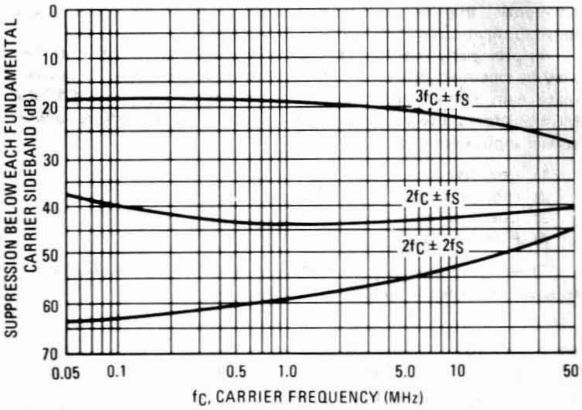
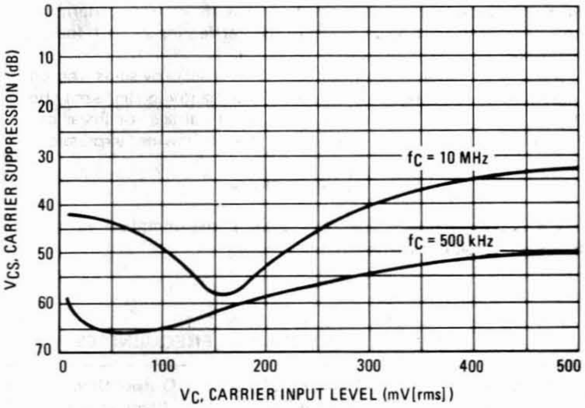


FIGURE 22 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



## OPERATIONS INFORMATION

The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

### Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

FIGURE 23 – CIRCUIT SCHEMATIC

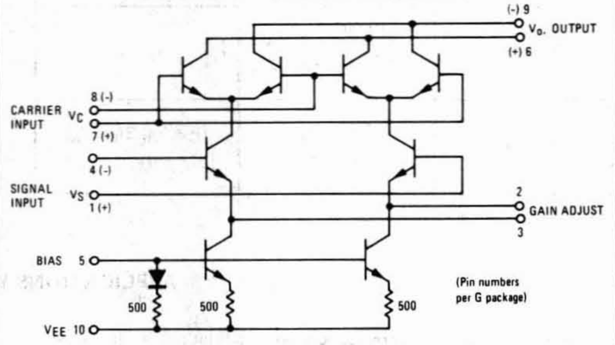
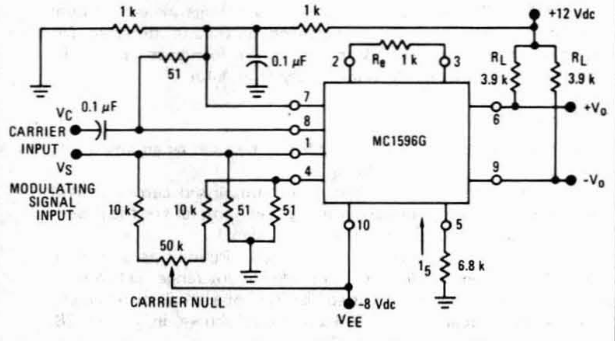

(-) 9
Vo, OUTPUT
(+) 6
CARRIER INPUT
VC
8 (-)
7 (+)
SIGNAL INPUT
VS
4 (-)
1 (+)
2
GAIN ADJUST
3
BIAS 5
500
500
500
VEE 10
(Pin numbers per G package)

FIGURE 24 – TYPICAL MODULATOR CIRCUIT


1 k
1 k
+12 Vdc
51
0.1 µF
2
Re 1 k
3
RL 3.9 k
RL 3.9 k
VC 0.1 µF
CARRIER INPUT
7
8
1
MC1596G
6
+Vo
VS
MODULATING SIGNAL INPUT
4
9
-Vo
10 k
10 k
51
51
50 k
10
5
I5
6.8 k
CARRIER NULL
-8 Vdc
VEE

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

## OPERATIONS INFORMATION (continued)

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I_5)(R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of $R_E$ for a given input voltage amplitude.

### FIGURE 25 – TABLE 1
### VOLTAGE GAIN AND OUTPUT FREQUENCIES

| Carrier Input Signal ($V_C$) | Approximate Voltage Gain | Output Signal Frequency(s) |
|---|---|---|
| Low-level dc | $\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$ | $f_M$ |
| High-level dc | $\frac{R_L}{R_E + 2r_e}$ | $f_M$ |
| Low-level ac | $\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$ | $f_C \pm f_M$ |
| High-level ac | $\frac{0.637 R_L}{R_E + 2r_e}$ | $f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . . |

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level dc
2) High-level dc
3) Low-level ac
4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

NOTES:

1. Low-level Modulating Signal, $V_M$, assumed in all cases. $V_C$ is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. $R_L$ = Load resistance.
5. $R_E$ = Emitter resistance between pins 2 and 3.
6. $r_e$ = Transistor dynamic emitter resistance, at +25°C;

$$r_e \approx \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26 \text{ mV at room temperature}$$

## APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

### AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

### Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on pins 7 and 8 should be increased to 1.0 μF. Also, the output filter at pin 9 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

## APPLICATIONS INFORMATION (continued)

**Doubly Balanced Mixer**

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

**Frequency Doubler**

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

**Phase Detection and FM Detection**

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

## TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR (+12 Vdc SINGLE SUPPLY)

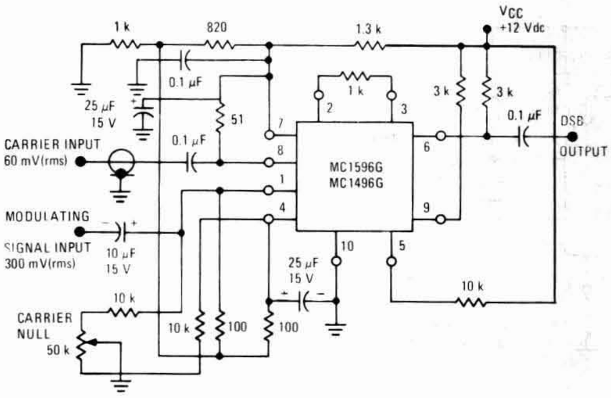

VCC
+12 Vdc
1 k
820
1.3 k
0.1 µF
25 µF
15 V
51
0.1 µF
1 k
3 k
3 k
0.1 µF
DSB
OUTPUT
CARRIER INPUT
60 mV(rms)
MC1596G
MC1496G
MODULATING
SIGNAL INPUT
300 mV(rms)
10 µF
15 V
25 µF
15 V
10 k
CARRIER
NULL
50 k
10 k
100
100
10 k

FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

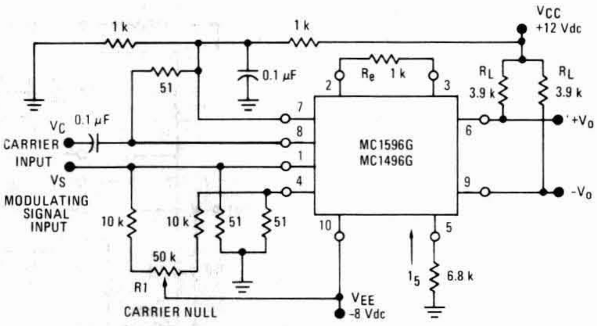

VCC
+12 Vdc
1 k
1 k
51
0.1 µF
Re 1 k
RL
3.9 k
RL
3.9 k
VC 0.1 µF
CARRIER
INPUT
VS
MODULATING
SIGNAL
INPUT
MC1596G
MC1496G
+Vo
-Vo
10 k
10 k
51
51
50 k
R1
CARRIER NULL
VEE
-8 Vdc
I5
6.8 k

FIGURE 28 – AM MODULATOR CIRCUIT

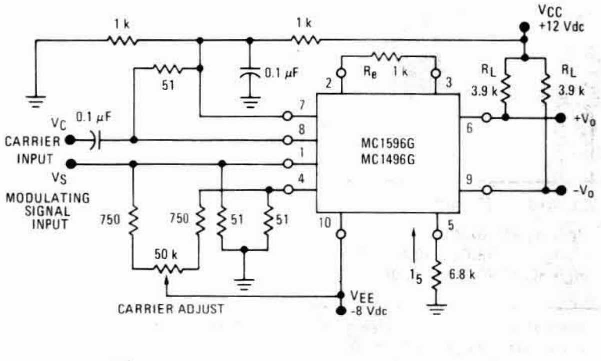
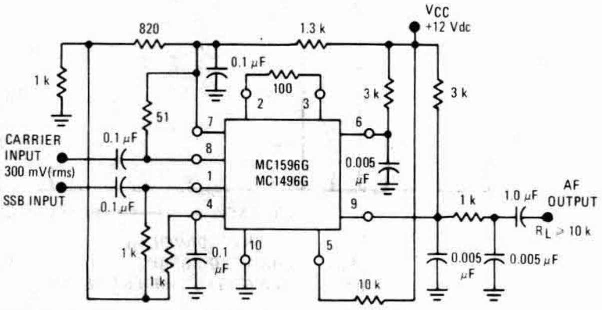
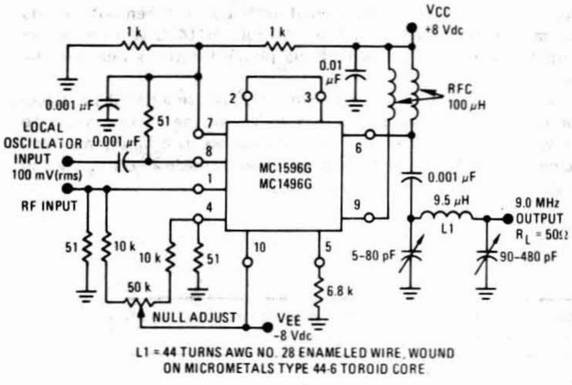

VCC
+12 Vdc
1 k
1 k
51
0.1 µF
Re 1 k
RL
3.9 k
RL
3.9 k
VC 0.1 µF
CARRIER
INPUT
VS
MODULATING
SIGNAL
INPUT
MC1596G
MC1496G
+Vo
-Vo
750
750
51
51
50 k
CARRIER ADJUST
VEE
-8 Vdc
I5
6.8 k

FIGURE 29 – PRODUCT DETECTOR (+12 Vdc SINGLE SUPPLY)


VCC
+12 Vdc
820
1.3 k
1 k
0.1 µF
100
3 k
3 k
51
CARRIER
INPUT
300 mV(rms)
SSB INPUT
0.1 µF
0.1 µF
MC1596G
MC1496G
0.005 µF
1 k
1.0 µF
AF
OUTPUT
RL ≥ 10 k
1 k
0.1 µF
1 k
0.005 µF
0.005 µF
10 k

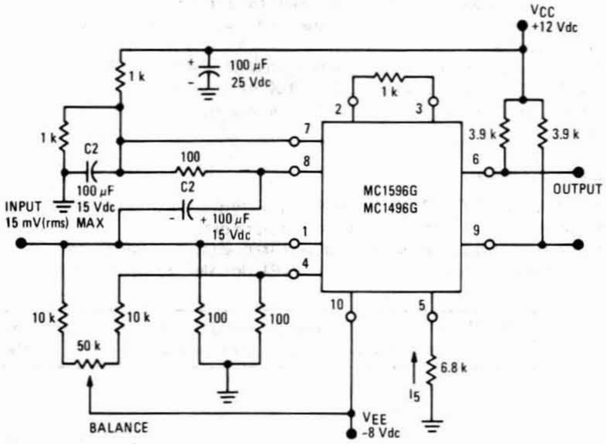
## TYPICAL APPLICATIONS (continued)

### FIGURE 30 – DOUBLY BALANCED MIXER (BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)

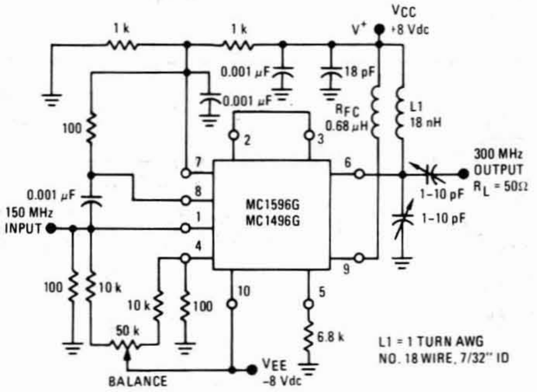

VCC
+8 Vdc
1 k
1 k
0.01 µF
RFC
100 µH
0.001 µF
51
LOCAL OSCILLATOR INPUT
100 mV(rms)
0.001 µF
RF INPUT
MC1596G
MC1496G
0.001 µF
9.5 µH
L1
9.0 MHz OUTPUT
RL = 50Ω
5–80 pF
90–480 pF
51
10 k
10 k
51
50 k
6.8 k
NULL ADJUST
VEE
-8 Vdc

L1 = 44 TURNS AWG NO. 28 ENAMELED WIRE, WOUND ON MICROMETALS TYPE 44-6 TOROID CORE

### FIGURE 31 – LOW-FREQUENCY DOUBLER

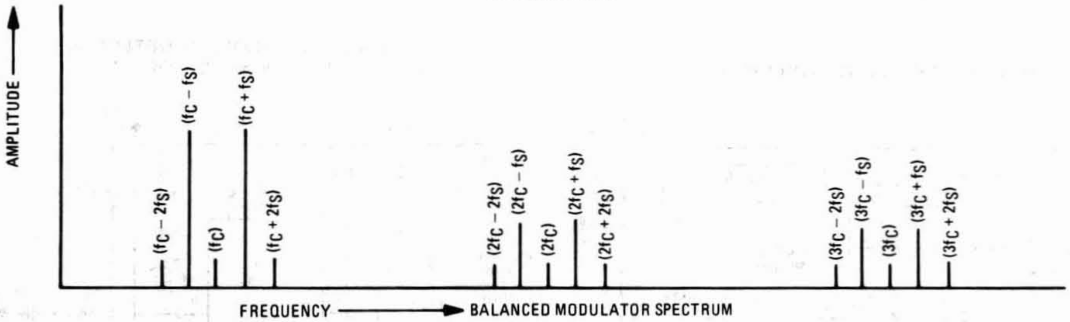

VCC
+12 Vdc
1 k
100 µF
25 Vdc
1 k
1 k
C2
100
100 µF
15 Vdc
C2
100 µF
15 Vdc
INPUT
15 mV(rms) MAX
3.9 k
3.9 k
OUTPUT
MC1596G
MC1496G
10 k
10 k
100
100
50 k
6.8 k
I5
BALANCE
VEE
-8 Vdc

### FIGURE 32 – 150 to 300 MHz DOUBLER


VCC
V+
+8 Vdc
1 k
1 k
0.001 µF
18 pF
0.001 µF
RFC
0.68 µH
L1
18 nH
100
300 MHz OUTPUT
RL = 50Ω
1–10 pF
1–10 pF
0.001 µF
150 MHz INPUT
MC1596G
MC1496G
100
10 k
10 k
100
50 k
6.8 k
BALANCE
VEE
-8 Vdc

L1 = 1 TURN AWG NO. 18 WIRE, 7/32" ID

### DEFINITIONS



BALANCED MODULATOR SPECTRUM

| | | | |
|---|---|---|---|
| $f_C$ | CARRIER FUNDAMENTAL | $f_C \pm nf_S$ | FUNDAMENTAL CARRIER SIDEBAND HARMONICS |
| $f_S$ | MODULATING SIGNAL | $nf_C$ | CARRIER HARMONICS |
| $f_C \pm f_S$ | FUNDAMENTAL CARRIER SIDEBANDS | $nf_C \pm nf_S$ | CARRIER HARMONIC SIDEBANDS |

NOTE: Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

**MOTOROLA**

# MC3373

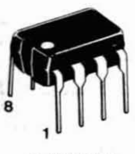
## REMOTE CONTROL WIDEBAND AMPLIFIER WITH DETECTOR

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

## REMOTE CONTROL AMPLIFIER-DETECTOR

The MC3373 is intended for application in infrared remote controls. It provides the high gain and pulse shaping needed to couple the signal from an IR receiver diode to the tuning control system logic.

- High Gain Pre-Amp
- Envelope Detector for PCM Demodulation
- Simple Interface to Microcomputer Remote Control Decoder
- May Be Used with Tuned Circuit for Narrow Bandwidth, Lower Noise Operation
- Small Package Size
- Minimum External Components
- Wide Operating Supply Voltage Range
- Low Current Drain
- Improved retrofit for NEC part no. μPC1373



**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

**Pin Connections**

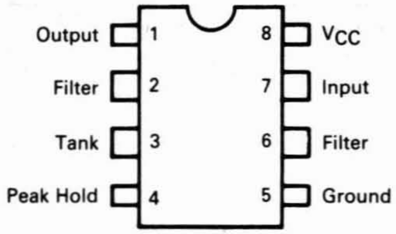
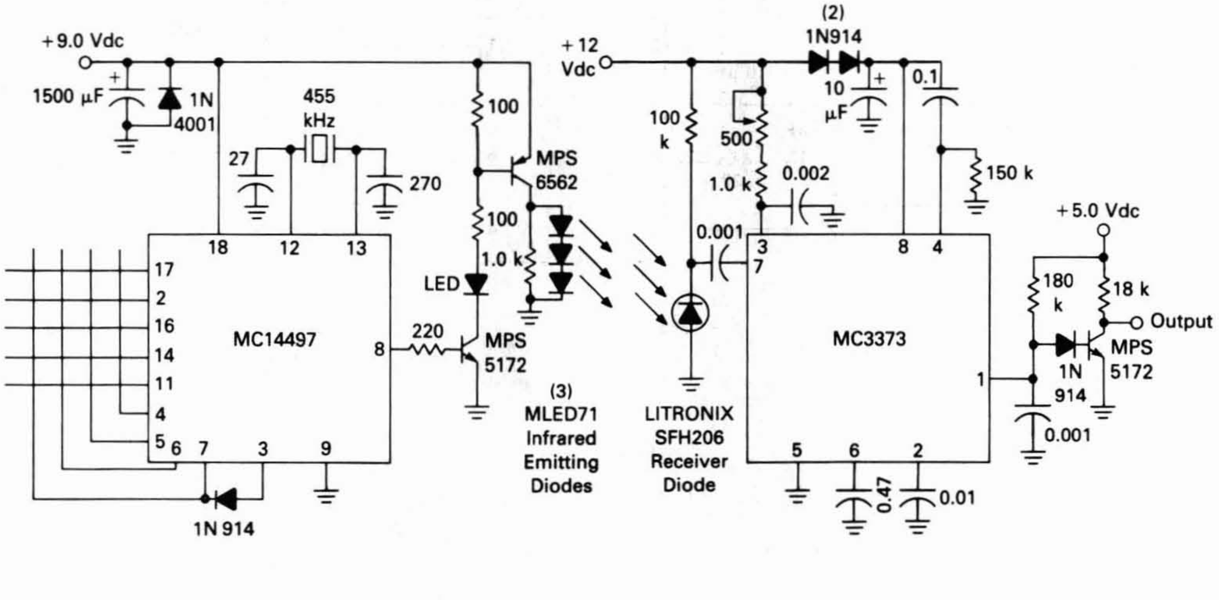

Output 1
Filter 2
Tank 3
Peak Hold 4
8 VCC
7 Input
6 Filter
5 Ground

**FIGURE 1 — REMOTE CONTROL APPLICATION**


+9.0 Vdc
1500 μF
1N 4001
455 kHz
27
270
100
MPS 6562
100
1.0 k
LED
18
12
13
17
2
16
14
11
4
5
6
7
3
9
MC14497
8
220
MPS 5172
1N 914
(3) MLED71 Infrared Emitting Diodes
+12 Vdc
100 k
500
1.0 k
0.002
0.001
(2) 1N914
10 μF
0.1
150 k
LITRONIX SFH206 Receiver Diode
3
7
8
4
MC3373
1
5
6
2
0.47
0.01
+5.0 Vdc
180 k
18 k
Output
1N 914
MPS 5172
0.001

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 15 | Vdc |
| Operating Temperature Range | $T_A$ | 0 to 75 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +125 | °C |
| Junction Temperature | $T_J$ | 150 | °C |
| Power Dissipation, Package Rating<br>Derate above 25°C | $P_D$<br>$1/\theta_{JA}$ | 1.25<br>10 | Watts<br>mW/°C |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage (25°C) | $V_{CC}$ | 4.75 | — | 15 | Vdc |
| Power Supply Voltage (0°C) | $V_{CC}$ | 5.0 | — | 15 | Vdc |
| Input Frequency | $f_{in}$ | 30 | 40 | 80 | kHz |

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C, $V_{CC}$ = 5.0 V, $f_{in}$ = 40 kHz, Test circuit of Figure 2)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Current | $I_{CC}$ | 1.5 | 2.5 | 3.5 | mAdc |
| Input Terminal Voltage | V(Pin 7) | 2.4 | 2.8 | 3.0 | Vdc |
| Input Voltage Threshold | $V_{in}$ | — | 50 | 100 | $\mu V_{P-P}$ |
| Input Amplifier Voltage Gain (V[Pin 3] = 500 $mV_{P-P}$) | $A_V$ | — | 60 | — | dB |
| Input Impedance | $r_{in}$ | 40 | 60 | 80 | kΩ |
| Output Voltage, $V_{in}$ = 1.0 $mV_{P-P}$ | $V_{OL}$ | — | — | 0.5 | V |
| Output Leakage, $V_{CC}$ = $V_{OH}$ = 15 Vdc | $I_{OH}$ | — | — | 2.0 | μA |
| Output Voltage, Input Open | $V_{OH}$ | — | — | 5.0 | Vdc |

FIGURE 2 — TEST CIRCUIT

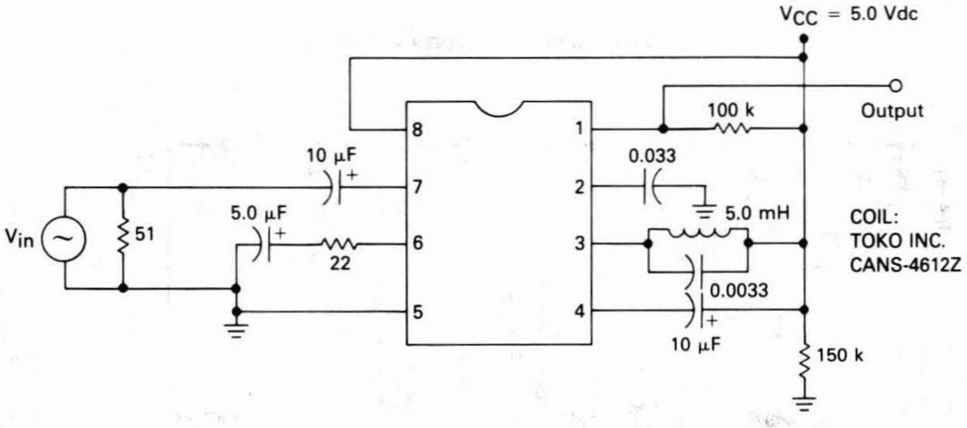


FIGURE 3 — BLOCK DIAGRAM

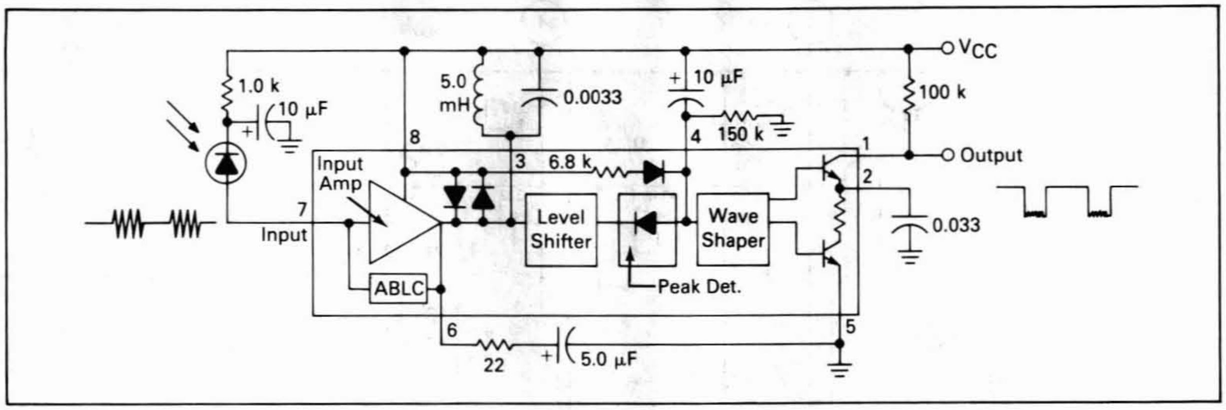

VCC
1.0 k
10 µF
5.0 mH
0.0033
10 µF
150 k
100 k
8
3
6.8 k
4
1
Output
2
0.033
Input Amp
7
Input
Level Shifter
Peak Det.
Wave Shaper
ABLC
6
22
5.0 µF
5

FIGURE 4 — INPUT AMPLIFIER GAIN

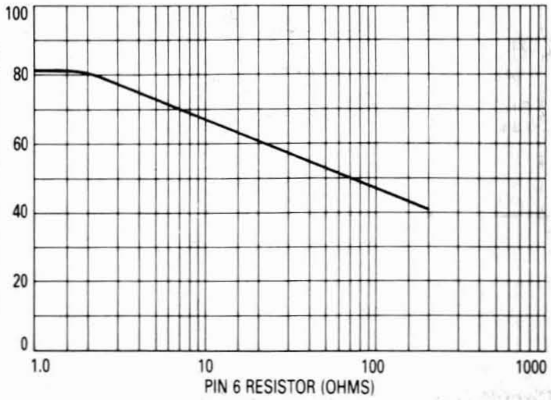


FIGURE 5 — DETECTOR THRESHOLD

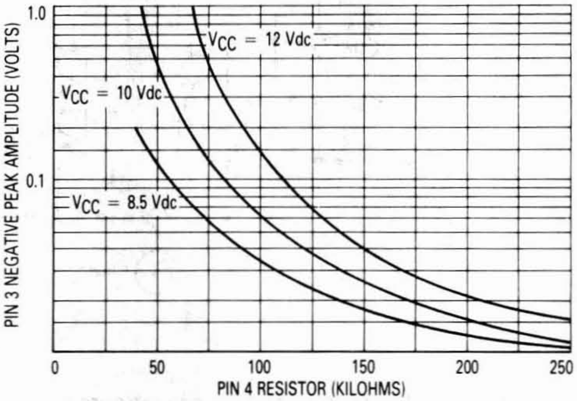
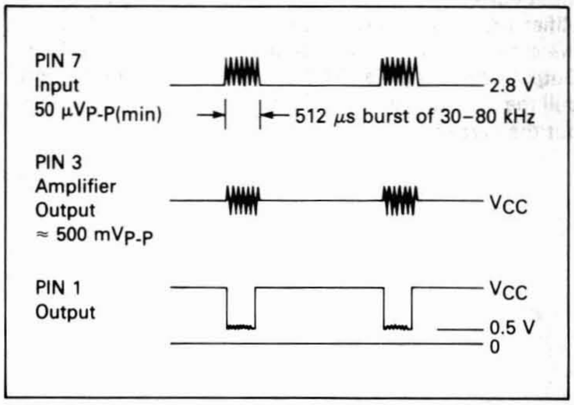


FIGURE 6 — TYPICAL SIGNAL WAVEFORMS

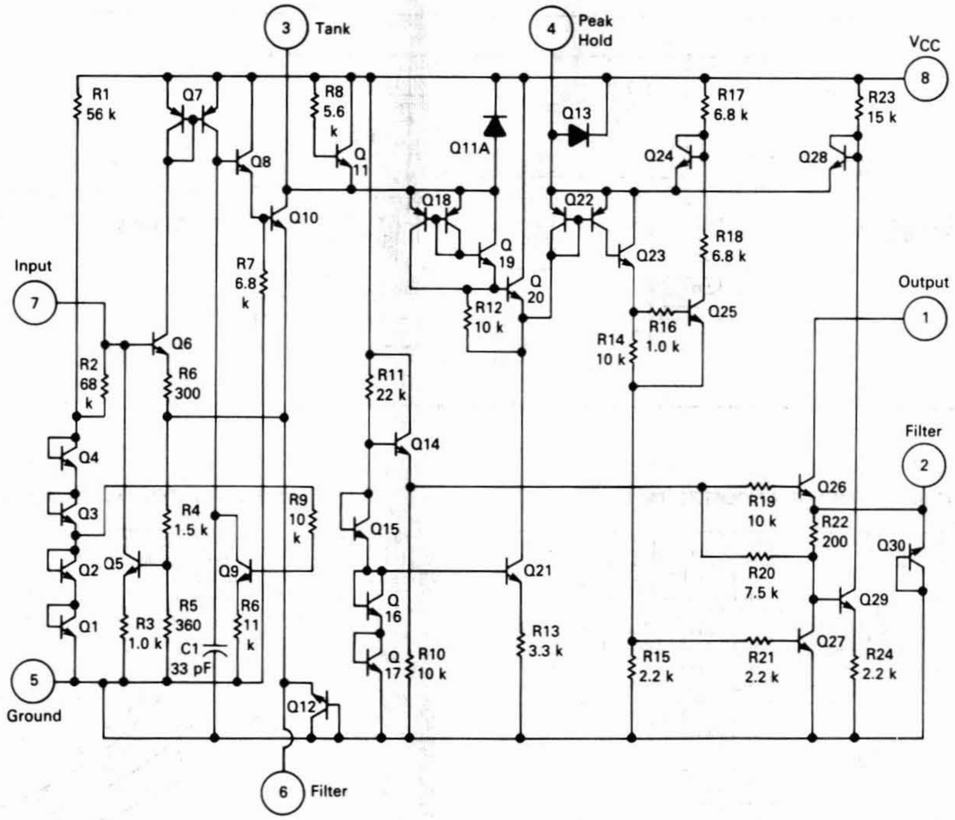

PIN 7
Input
50 µVP-P(min)
2.8 V
512 µs burst of 30–80 kHz
PIN 3
Amplifier
Output
≈ 500 mVP-P
VCC
PIN 1
Output
VCC
0.5 V
0

## APPLICATIONS INFORMATION

The MC3373 is designed to amplify and detect the signal from an infrared receiver diode in a remote control system. The signal is generally in the form of ultrasonic bursts, ranging in amplitude from 50 $\mu V_{P\text{-}P}$ to several hundred millivolts. The receiver diode may be directly connected to the MC3373 to save parts; the input is internally compensated by an ABLC (automatic bias level control). However, it is advantageous to ac couple the input, as shown in Figure 1, in order to provide attenuation of the power line frequency IR inputs, which are plentiful in most cases.

The input amplifier gain is approximately equal to the load impedance at Pin 3, divided by the resistor from Pin 6 to ground. Again, the low frequency gain can be reduced by using a small coupling capacitor in series with the Pin 6 resistor.

FIGURE 7 — INTERNAL SCHEMATIC


3 Tank
4 Peak Hold
VCC
8
R1 56 k
Q7
R8 5.6 k
Q11
Q8
Q11A
Q13
R17 6.8 k
R23 15 k
Q24
Q28
Q10
Q18
Q19
Q22
Q23
R18 6.8 k
Input
7
R7 6.8 k
Q20
R12 10 k
Output
1
Q25
R16 1.0 k
R14 10 k
Q6
R2 68 k
R6 300
R11 22 k
Q14
Filter
2
Q4
Q3
R4 1.5 k
R9 10 k
Q15
R19 10 k
Q26
R22 200
Q30
Q2
Q5
Q9
Q21
R20 7.5 k
Q29
Q1
R3 1.0 k
R5 360
R6 11 k
C1 33 pF
Q16
Q17
R10 10 k
R13 3.3 k
R15 2.2 k
R21 2.2 k
Q27
R24 2.2 k
5
Ground
Q12
6 Filter

The load may be resistive, as shown in the application circuit, or tuned, as in the test circuit. The amplifier output is limited by back-to-back clamping diodes, level shifted, buffered and fed to a negative peak detector. The detector threshold is set by the external resistor on Pin 4, and an internal 6.8 kΩ resistor and diode to $V_{CC}$. The capacitor from $V_{CC}$ to Pin 4 quickly charges during the negative peaks and then settles toward the set-up voltage between signal bursts at a rate roughly determined by the value of the capacitor and the 6.8 k resistor. The external capacitor at Pin 2 filters the ultrasonic carrier from the pulses.

## Circuit Description (Refer to Figure 7)

Q1–Q4 set the bias on the amplifier input at approximately 2.8 V. Q6–Q10 form the input amplifier, which has a gain of about 80 dB when R(Pin 6) = 0. Q5 sinks input current from the photo diode and keeps the amplifier properly biased. Q18–Q20 level shift and buffer the signal to the negative peak detector, Q22 and Q23. Output devices Q26 and Q27 conduct during peaks and pull the output, Pin 1, low. The capacitor on Pin 2 filters out the carrier.

**ORDERING INFORMATION**

| Device | Alternate | Temperature Range | Package |
|---|---|---|---|
| MC3456D | — | 0°C to +70°C | SO-14 |
| MC3456L | — | 0°C to +70°C | Ceramic DIP |
| MC3456P | NE556A | 0°C to +70°C | Plastic DIP |
| MC3556L | — | −55°C to +125°C | Ceramic DIP |

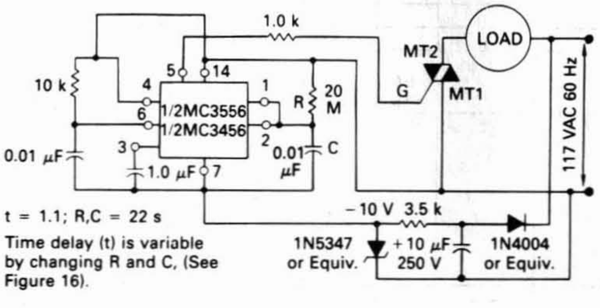
# Specifications and Applications Information

## DUAL TIMING CIRCUIT

The MC3556/MC3456 dual timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor per timer. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor per timer. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE556/SE556 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output
- Dual Version of the Popular MC1555/MC1455 Timer

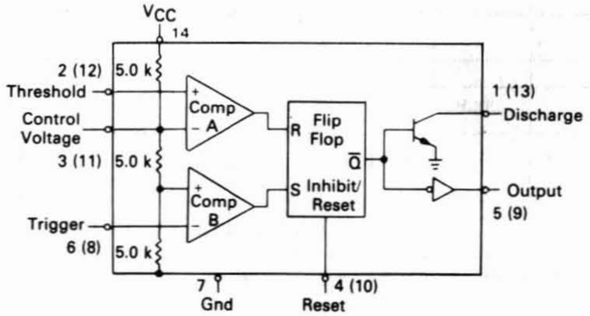
FIGURE 1 — 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT


1.0 k
LOAD
MT2
MT1
G
10 k
4
5
14
1
6
1/2MC3556
1/2MC3456
R
20 M
2
3
0.01 μF
0.01 μF
C
1.0 μF
7
117 VAC 60 Hz
−10 V
3.5 k
1N5347 or Equiv.
+10 μF 250 V
1N4004 or Equiv.

t = 1.1; R,C = 22 s

Time delay (t) is variable by changing R and C, (See Figure 16).

FIGURE 2 — BLOCK DIAGRAM (1/2 SHOWN)

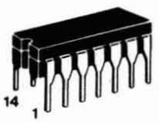

VCC
14
2 (12)
Threshold
5.0 k
Control Voltage
3 (11)
5.0 k
Trigger
6 (8)
5.0 k
Comp A
Comp B
R
S
Flip Flop
Q̄
Inhibit/Reset
1 (13)
Discharge
Output
5 (9)
7
Gnd
4 (10)
Reset

# MC3456
# MC3556

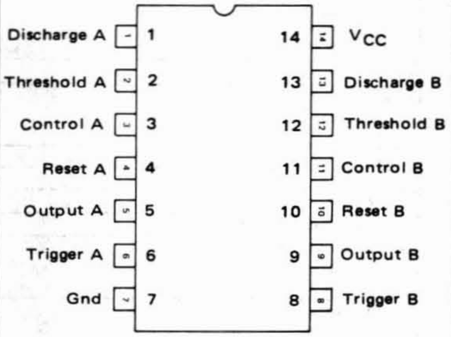
## DUAL TIMING CIRCUIT

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA

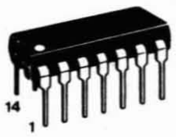


**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14


Discharge A 1
Threshold A 2
Control A 3
Reset A 4
Output A 5
Trigger A 6
Gnd 7
14 VCC
13 Discharge B
12 Threshold B
11 Control B
10 Reset B
9 Output B
8 Trigger B

(Top View)

**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05
(MC3456 only)



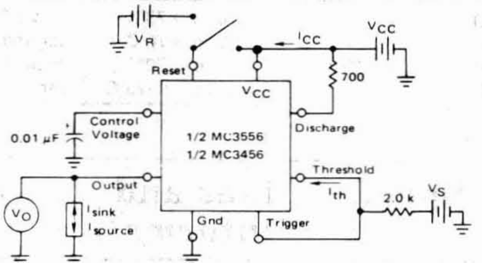
**TYPICAL APPLICATIONS**

- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

## MAXIMUM RATINGS ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +18 | Vdc |
| Discharge Current | $I_{dis}$ | 200 | mA |
| Power Dissipation (Package Limitation) | $P_D$ | | |
| Ceramic Dual-In-Line Package | | 1000 | mW |
| Derate above $T_A$ = +25°C | | 6.6 | mW/°C |
| Plastic Dual In-Line Package | | 625 | mW |
| Derate above $T_A$ = +25°C | | 5.0 | mW/°C |
| Operating Ambient Temperature Range | $T_A$ | | °C |
| MC3556 | | -55 to +125 | |
| MC3456 | | 0 to +70 | |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

### FIGURE 3 – GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters:
(to set output and measure parameters)

a. When $V_S \geq 2/3\ V_{CC}$, $V_O$ is low.
b. When $V_S \leq 1/3\ V_{CC}$, $V_O$ is high.
c. When $V_O$ is low, pin 7 sinks current. To test for Reset, set $V_O$ high, apply Reset voltage, and test for current flowing into discharge pin. When Reset is not in use, it should be tied to $V_{CC}$.

## ELECTRICAL CHARACTERISTICS ($T_A$ = +25°C, $V_{CC}$ = +5.0 V to +15 V unless otherwise noted.)

| Characteristics | Symbol | MC3556 | | | MC3456 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supply Voltage | $V_{CC}$ | 4.5 | – | 18 | 4.5 | – | 16 | V |
| Supply Current (Per timer, double for both halfs) | $I_{CC}$ | | | | | | | mA |
| $V_{CC}$ = 5.0 V, $R_L = \infty$ | | – | 3.0 | 5.0 | – | 3.0 | 6.0 | |
| $V_{CC}$ = 15 V, $R_L = \infty$ | | – | 10 | 12 | – | 10 | 15 | |
| Low State, (Note 1) | | | | | | | | |
| Timing Error (Note 2) | | | | | | | | |
| Monostable Mode | | | | | | | | |
| $R_A$ = 2.0 kΩ to 100 kΩ | | | | | | | | |
| Initial Accuracy C = 0.1 µF | | – | 0.5 | 1.5 | – | 0.75 | – | % |
| Drift with Temperature | | – | 30 | 100 | – | 50 | – | PPM/°C |
| Drift with Supply Voltage | | – | 0.15 | 0.2 | – | 0.1 | – | %/Volt |
| Astable Mode | | | | | | | | |
| $R_A = R_B$ = 2.0 kΩ to 100 kΩ | | | | | | | | |
| C = 0.01 µF | | | | | | | | |
| Initial Accuracy | | – | 1.5 | – | – | 2.25 | – | % |
| Drift with Temperature | | – | 90 | – | – | 150 | – | PPM/°C |
| Drift with Supply Voltage | | – | 0.15 | – | – | 0.3 | – | %/Volt |
| Threshold Voltage | $V_{th}$ | – | 2/3 | – | – | 2/3 | – | $xV_{CC}$ |
| Trigger Voltage | $V_T$ | | | | | | | V |
| $V_{CC}$ = 15 V | | 4.8 | 5.0 | 5.2 | – | 5.0 | – | |
| $V_{CC}$ = 5.0 V | | 1.45 | 1.67 | 1.9 | – | 1.67 | – | |
| Trigger Current | $I_T$ | – | 0.5 | – | – | 0.5 | – | µA |
| Reset Voltage | $V_R$ | 0.4 | 0.7 | 1.0 | 0.4 | 0.7 | 1.0 | V |
| Reset Current | $I_R$ | – | 0.1 | – | – | 0.1 | – | mA |
| Threshold Current (Note 3) | $I_{th}$ | – | 0.03 | 0.1 | – | 0.03 | 0.1 | µA |
| Control Voltage Level | $V_{CL}$ | | | | | | | V |
| $V_{CC}$ = 15 V | | 9.6 | 10 | 10.4 | 9.0 | 10 | 11 | |
| $V_{CC}$ = 5.0 V | | 2.9 | 3.33 | 3.8 | 2.6 | 3.33 | 4.0 | |
| Output Voltage Low | $V_{OL}$ | | | | | | | |
| ($V_{CC}$ = 15 V) | | | | | | | | V |
| $I_{sink}$ = 10 mA | | – | 0.1 | 0.15 | – | 0.1 | 0.25 | |
| $I_{sink}$ = 50 mA | | – | 0.4 | 0.5 | – | 0.4 | 0.75 | |
| $I_{sink}$ = 100 mA | | – | 2.0 | 2.25 | – | 2.0 | 2.75 | |
| $I_{sink}$ = 200 mA | | – | 2.5 | – | – | 2.5 | – | |
| ($V_{CC}$ = 5.0 V) | | | | | | | | |
| $I_{sink}$ = 8.0 mA | | – | 0.1 | 0.25 | – | – | – | |
| $I_{sink}$ = 5.0 mA | | – | – | – | – | 0.25 | 0.35 | |
| Output Voltage High | $V_{OH}$ | | | | | | | V |
| ($I_{source}$ = 200 mA) | | | | | | | | |
| $V_{CC}$ = 15 V | | – | 12.5 | – | – | 12.5 | – | |
| ($I_{source}$ = 100 mA) | | | | | | | | |
| $V_{CC}$ = 15 V | | 13 | 13.3 | – | 12.75 | 13.3 | – | |
| $V_{CC}$ = 5.0 V | | 3.0 | 3.3 | – | 2.75 | 3.3 | – | |
| Toggle Rate (Figures 17, 19) | | | | | | | | |
| $R_A$ = 3.3 kΩ, $R_B$ = 6.8 kΩ, C = 0.003 µF | – | – | 100 | -- | – | 100 | – | kHz |
| Discharge Leakage Current | $I_{dis}$ | – | 20 | 100 | – | 20 | 100 | nA |
| Rise Time of Output | $t_{OLH}$ | – | 100 | – | – | 100 | – | ns |
| Fall Time of Output | $t_{OHL}$ | – | 100 | – | – | 100 | – | ns |
| Matching Characteristics Between Sections | | | | | | | | |
| (Monostable) | | | | | | | | |
| Initial Timing Accuracy | | – | 0.5 | 1.0 | – | 1.0 | 2.0 | % |
| Timing Drift with Temperature | | – | ±10 | – | – | ±10 | – | ppm/°C |
| Drift with Supply Voltage | | – | 0.1 | 0.2 | – | 0.2 | 0.5 | %/V |

NOTES:
1. Supply current when output is high is typically 2.0 mA less.
2. Tested at $V_{CC}$ = 5.0 V and $V_{CC}$ = 15 V.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

## TYPICAL CHARACTERISTICS

($T_A$ = +25°C unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

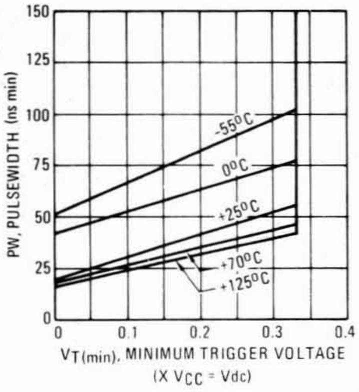


FIGURE 5 – SUPPLY CURRENT

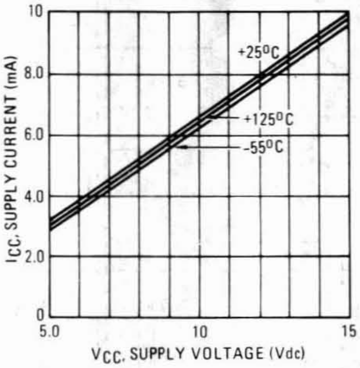


FIGURE 6 – HIGH OUTPUT VOLTAGE

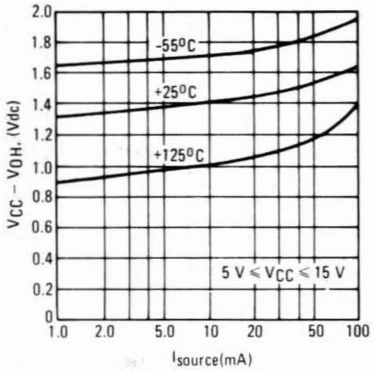


FIGURE 7 – LOW OUTPUT VOLTAGE @ $V_{CC}$ = 5.0 Vdc

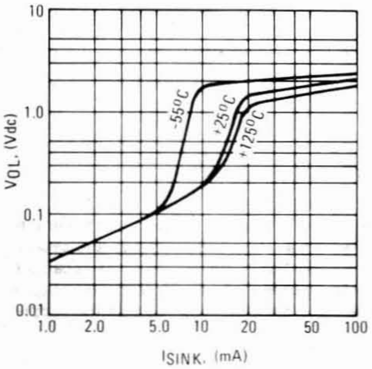


FIGURE 8 – LOW OUTPUT VOLTAGE @ $V_{CC}$ = 10 Vdc

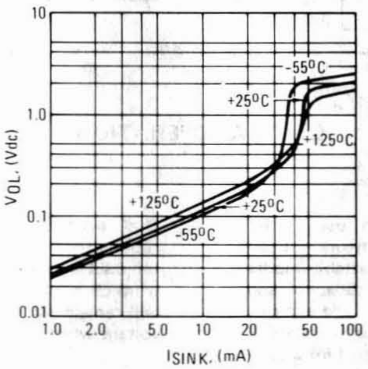


FIGURE 9 – LOW OUTPUT VOLTAGE @ $V_{CC}$ = 15 Vdc

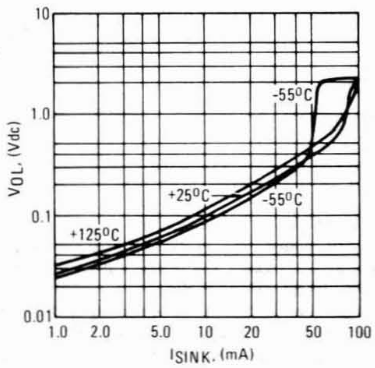


FIGURE 10 – DELAY TIME versus SUPPLY VOLTAGE

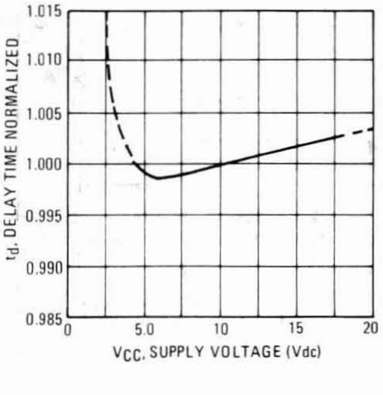


FIGURE 11 – DELAY TIME versus TEMPERATURE

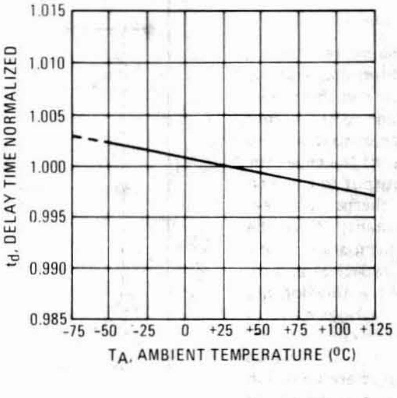


FIGURE 12 – PROPAGATION DELAY versus TRIGGER VOLTAGE

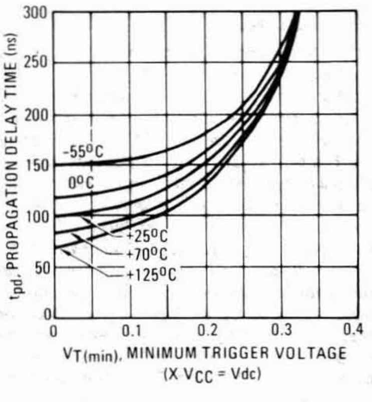
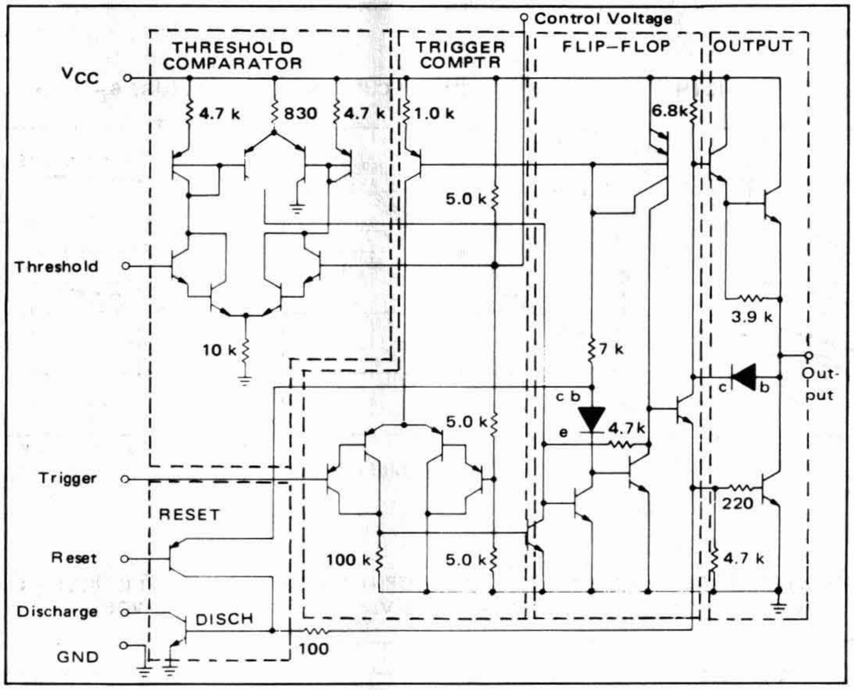


FIGURE 13 – 1/2 REPRESENTATIVE CIRCUIT SCHEMATIC


Control Voltage
THRESHOLD COMPARATOR
TRIGGER COMPTR
FLIP–FLOP
OUTPUT
$V_{CC}$
4.7 k
830
4.7 k
1.0 k
6.8k
5.0 k
Threshold
3.9 k
10 k
7 k
Out-put
c b
c
b
e
4.7k
5.0 k
Trigger
RESET
220
Reset
100 k
5.0 k
4.7 k
Discharge
DISCH
GND
100

## GENERAL OPERATION

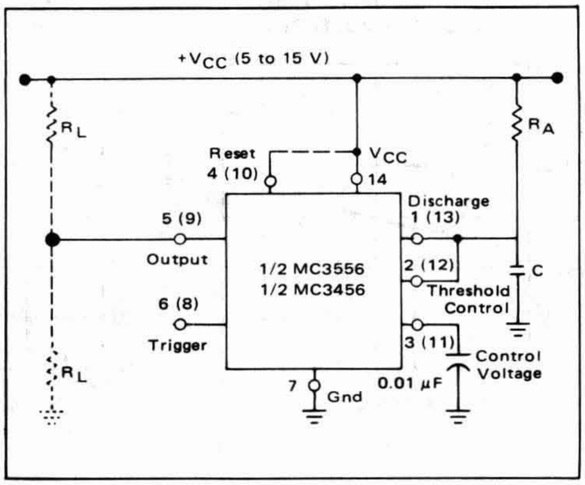
The MC3556 is a dual timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

**Monostable Mode**

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 $V_{CC}$ the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 $V_{CC}$ the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

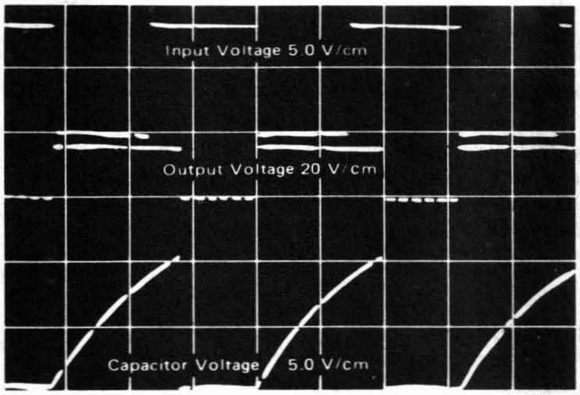
A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

FIGURE 14 – MONOSTABLE CIRCUIT


+$V_{CC}$ (5 to 15 V)
$R_L$
$R_A$
Reset
4 (10)
$V_{CC}$
14
Discharge
1 (13)
5 (9)
Output
1/2 MC3556
1/2 MC3456
2 (12)
C
Threshold
6 (8)
Control
Trigger
3 (11)
Control Voltage
$R_L$
7
Gnd
0.01 μF

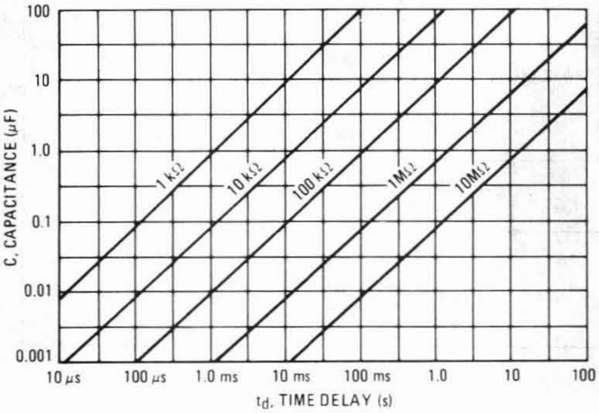
## GENERAL OPERATION (continued)

FIGURE 15 – MONOSTABLE WAVEFORMS



t = 50 μs/cm
($R_A$ = 10 kΩ, C = 0.01 μF, $R_L$ = 1.0 kΩ, $V_{CC}$ = 15 V)

FIGURE 16 – TIME DELAY



**Astable Mode**

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 $V_{CC}$ and 2/3 $V_{CC}$. See Figure 17.

The external capacitor charges to 2/3 $V_{CC}$ through $R_A$ and $R_B$ and discharges to 1/3 $V_{CC}$ through $R_B$. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695\,(R_A+R_B)\,C$

The discharge time (output low) by: $t_2 = 0.695\,(R_B)\,C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695\,(R_A+2R_B)\,C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B)\,C}$

and may be easily found as shown in Figure 19.

The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle $R_A$ must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of $R_A$ is given by:

$$R_A \geqslant \frac{V_{CC}\ (\text{Vdc})}{I_7\ (\text{A})} \geqslant \frac{V_{CC}\ (\text{Vdc})}{0.2}$$

FIGURE 17 – ASTABLE CIRCUIT

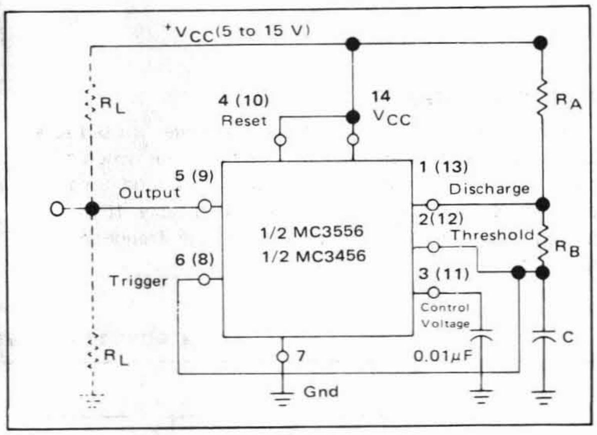
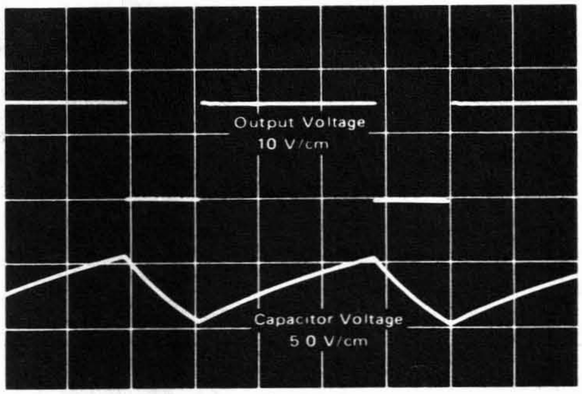
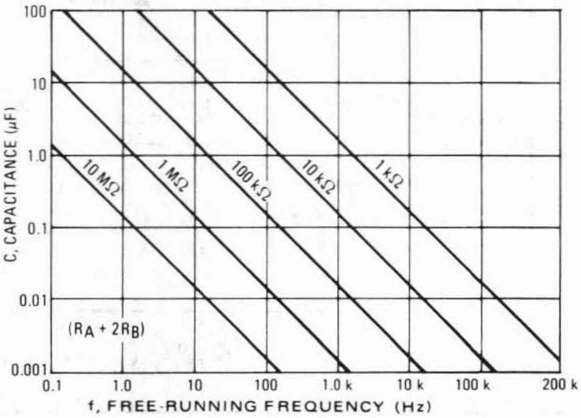


FIGURE 18 – ASTABLE WAVEFORMS



t = 20 μs/cm
($R_A$ = 5.1 kΩ, C = 0.01 μF, $R_L$ = 1.0 kΩ;
$R_B$ = 3.9 kΩ, $V_{CC}$ = 15 V)

FIGURE 19 – FREE-RUNNING FREQUENCY



## APPLICATIONS INFORMATION

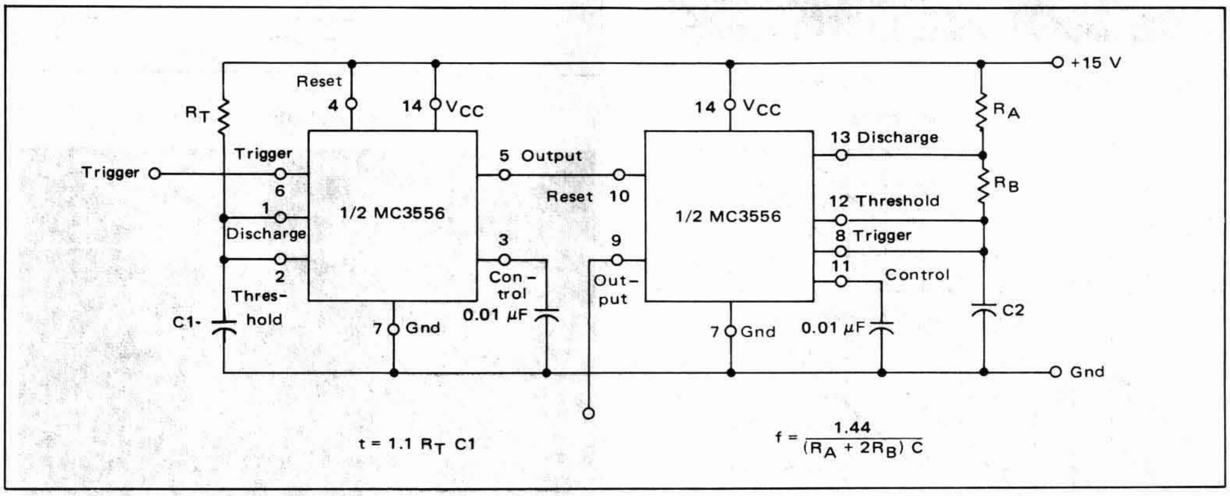
### TONE BURST GENERATOR

For a tone burst generator the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at Pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.

### DUAL ASTABLE MULTIVIBRATOR

This dual astable multivibrator provides versatility not available with single timer circuits. The duty cycle can be adjusted from 5% to 95%. The two outputs provide two phase clock signals often required in digital systems. It can also be inhibited by use of either reset terminal.

FIGURE 20 – TONE BURST GENERATOR

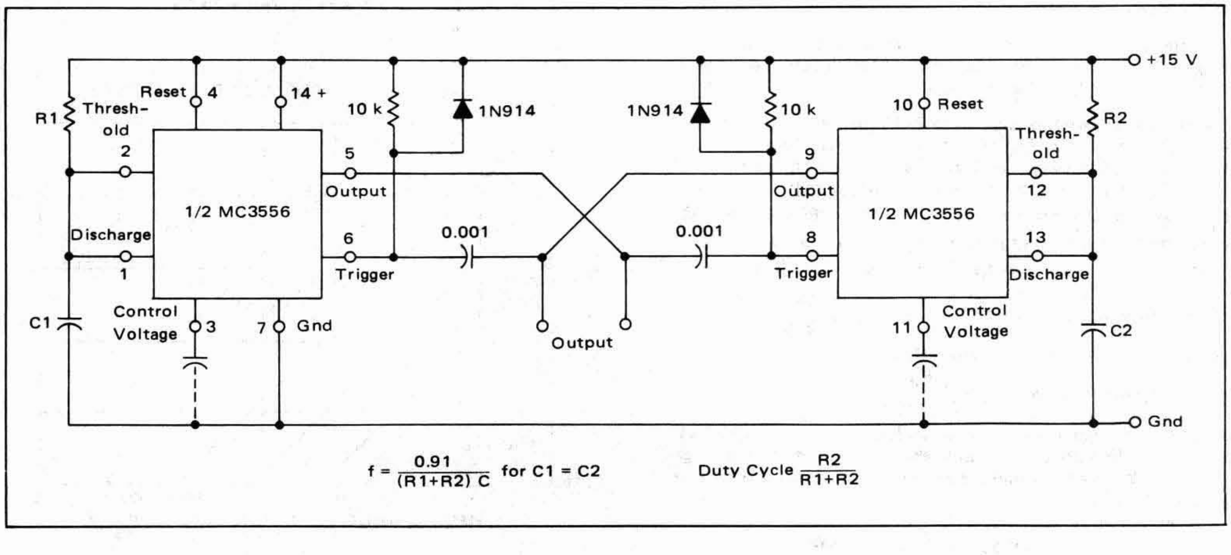


+15 V
Reset
4
14
VCC
$R_T$
Trigger
Trigger
6
1
Discharge
2
Thres-
hold
C1
1/2 MC3556
5 Output
3
Con-
trol
0.01 µF
7 Gnd
Reset 10
9
Out-
put
14 VCC
1/2 MC3556
13 Discharge
12 Threshold
8 Trigger
11
Control
0.01 µF
7 Gnd
$R_A$
$R_B$
C2
Gnd

$t = 1.1\ R_T\ C1$

$f = \frac{1.44}{(R_A + 2R_B)\ C}$

FIGURE 21 – DUAL ASTABLE MULTIVIBRATOR



+15 V
R1
Reset
4
14 +
Thresh-
old
2
Discharge
1
C1
Control
Voltage
3
7
Gnd
1/2 MC3556
10 k
1N914
5
Output
6
Trigger
0.001
Output
1N914
10 k
9
Output
8
Trigger
0.001
10 Reset
1/2 MC3556
Thresh-
old
12
13
Discharge
Control
Voltage
11
R2
C2
Gnd

$f = \frac{0.91}{(R1+R2)\ C}$ for C1 = C2

Duty Cycle $\frac{R2}{R1+R2}$

## APPLICATIONS INFORMATION (continued)

**Pulse Width Modulation**

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 3. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 22

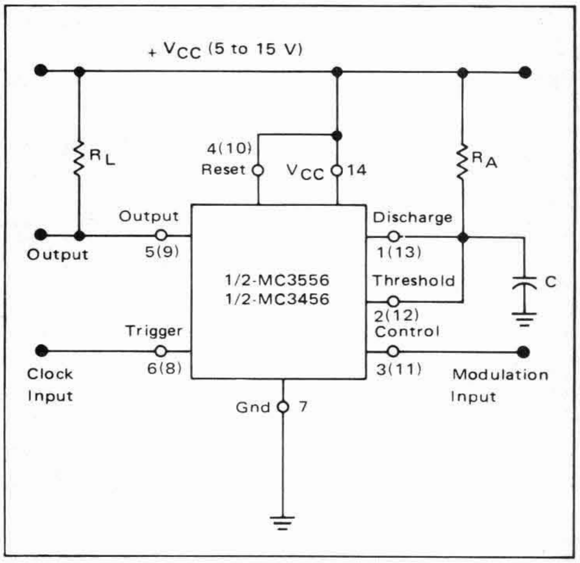
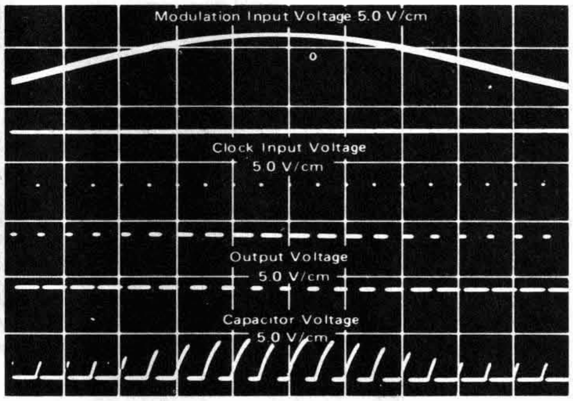

+ $V_{CC}$ (5 to 15 V)
$R_L$
4(10)
Reset
$V_{CC}$ 14
$R_A$
Output
Output
5(9)
Discharge
1(13)
1/2-MC3556
1/2-MC3456
Threshold
2(12)
Control
C
Trigger
6(8)
Clock
Input
3(11)
Modulation
Input
Gnd 7

FIGURE 23 – PULSE WIDTH MODULATION WAVEFORMS
($R_A$ = 10 kΩ, C = 0.02 μF, $V_{CC}$ = 15 V)

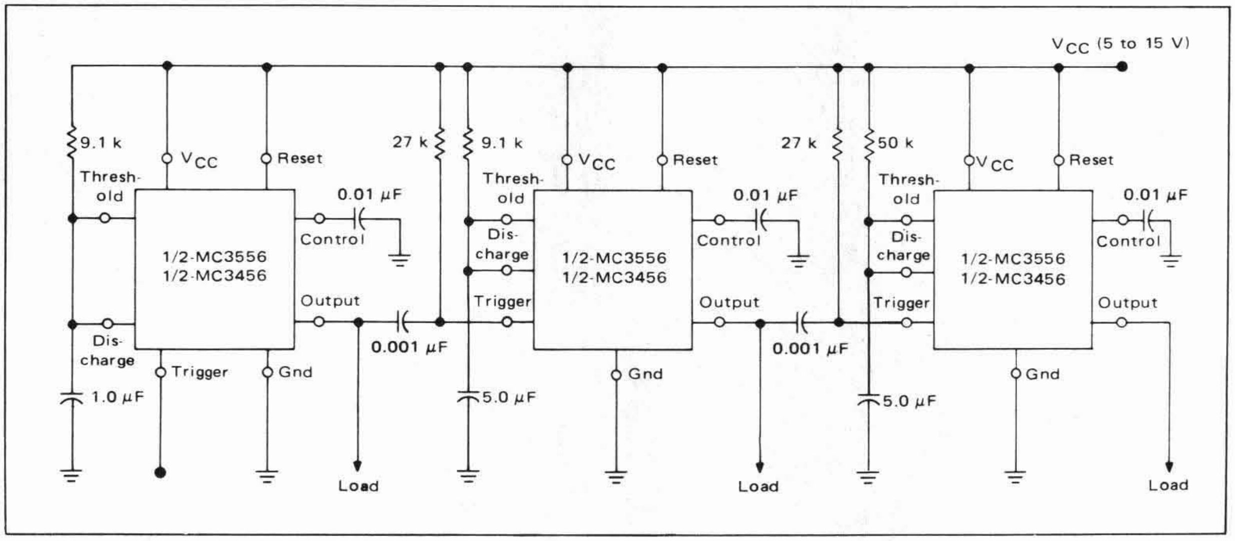


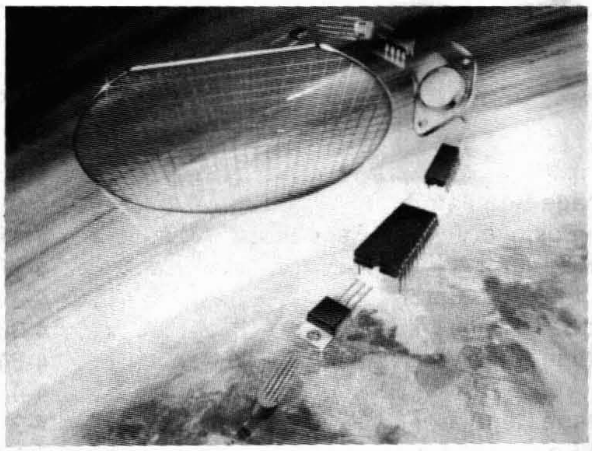
t = 0.5 ms/cm

**Test Sequences**

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 24 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 24


$V_{CC}$ (5 to 15 V)
9.1 k
$V_{CC}$
Reset
Thresh-old
0.01 μF
Control
1/2-MC3556
1/2-MC3456
Output
Dis-charge
Trigger
Gnd
1.0 μF
0.001 μF
Load
27 k
9.1 k
$V_{CC}$
Reset
Thresh-old
0.01 μF
Dis-charge
Control
1/2-MC3556
1/2-MC3456
Trigger
Output
Gnd
5.0 μF
0.001 μF
Load
27 k
50 k
$V_{CC}$
Reset
Thresh-old
0.01 μF
Dis-charge
Control
1/2-MC3556
1/2-MC3456
Trigger
Output
Gnd
5.0 μF
Load



# Power Supply Circuits

Voltage/Switching Regulators

Voltage References

Supervisory Circuits

Power Controllers

# POWER SUPPLY CIRCUITS

## Voltage/Switching Regulators

| Device | Function | Page |
|---|---|---|
| LM109 | Positive Voltage Regulator | 4-4 |
| LM117 | 3-Terminal Adjustable Positive Voltage Regulator | 4-9 |
| LM117L | Low-Current 3-Terminal Adjustable Positive Voltage Regulator | 4-17 |
| LM123,A | 3-Ampere, 5 Volt Positive Voltage Regulator | 4-25 |
| LM137 | 3-Terminal Adjustable Negative Voltage Regulator | 4-31 |
| LM140,A | Three-Terminal Positive Fixed Voltage Regulators | 4-38 |
| LM150 | 3-Terminal Adjustable Positive Voltage Regulator | 4-54 |
| LM209 | Positive Voltage Regulator | 4-4 |
| LM217 | 3-Terminal Adjustable Positive Voltage Regulator | 4-9 |
| LM217L | Low-Current 3-Terminal Adjustable Positive Voltage Regulator | 4-17 |
| LM223,A | 3-Ampere, 5 Volt Positive Voltage Regulator | 4-25 |
| LM237 | 3-Terminal Adjustable Negative Voltage Regulator | 4-31 |
| LM250 | 3-Terminal Adjustable Positive Voltage Regulator | 4-54 |
| LM309 | Positive Voltage Regulator | 4-4 |
| LM317 | 3-Terminal Adjustable Positive Voltage Regulator | 4-9 |
| LM317L | Low-Current 3-Terminal Adjustable Positive Voltage Regulator | 4-17 |
| LM317M | Medium-Current 3-Terminal Adjustable Positive Voltage Regulator | 4-62 |
| LM323,A | 3-Ampere, 5 Volt Positive Voltage Regulator | 4-25 |
| LM337 | 3-Terminal Adjustable Negative Voltage Regulator | 4-31 |
| LM337M | Medium-Current 3-Terminal Adjustable Negative Voltage Regulator | 4-70 |
| LM340,A | Three-Terminal Positive Fixed Voltage Regulators | 4-38 |
| LM350 | 3-Terminal Adjustable Positive Voltage Regulator | 4-54 |
| MC1466L | Voltage and Current Regulator | 4-77 |
| MC1468 | Dual ± 15-Volt Tracking Regulator | 4-87 |
| MC1566L | Voltage and Current Regulator | 4-77 |
| MC1568 | Dual ± 15-Volt Regulator | 4-87 |
| MC1723,C | Adjustable Positive or Negative Voltage Regulator | 4-93 |
| MC3324,A | Power Supply Supervisory Circuit/Dual-Voltage Comparator | |
| MC3420 | Switchmode Regulator Control Circuit | 4-99 |
| MC3520 | Switchmode Regulator Control Circuit | 4-99 |
| MC7800 Series | 3-Terminal Positive Voltage Regulators | 4-118 |
| MC78L00C,AC Series | Positive Voltage Regulators | 4-130 |
| MC78M00BC Series | Positive Voltage Regulator | 4-136 |
| MC78T00 Series | Three-Ampere Positive Voltage Regulators | 4-144 |
| MC7900C Series | Three-Terminal Negative Fixed Voltage Regulators | 4-157 |
| MC79L00C,AC Series | Three-Terminal Negative Fixed Voltage Regulators | 4-166 |
| MC79M00 Series | Three-Terminal Negative Fixed Voltage Regulators | 4-171 |
| MC33063 | DC to DC Converter Control Circuits | 4-187 |
| MC34060 | Switchmode Pulse Width Modulation Control Circuits | 4-174 |
| MC34060A | Switchmode Pulse Width Modulation Control Circuits | 4-186 |
| MC34063 | DC to DC Converter Control Circuits | 4-187 |
| MC35060 | Switchmode Pulse Width Modulation Control Circuits | 4-174 |
| MC35063 | DC to DC Converter Control Circuits | 4-187 |
| SG1525A | Pulse Width Modulator Control Circuits | 4-193 |
| SG1526 | Pulse Width Modulation Control Circuits | 4-193 |
| SG1527A | Pulse Width Modulator Control Circuits | 4-193 |
| SG2525A | Pulse Width Modulator Control Circuits | 4-193 |
| SG2526 | Pulse Width Modulation Control Circuits | 4-193 |
| SG2527A | Pulse Width Modulator Control Circuits | 4-193 |
| SG3525A | Pulse Width Modulator Control Circuits | 4-193 |

## Voltage/Switching Regulators (con't)

| Device | Function | Page |
|---|---|---|
| SG3526 | Pulse Width Modulation Control Circuits | 4-193 |
| SG3527A | Pulse Width Modulator Control Circuits | 4-193 |
| TDA4600 | Flyback Converter Regulator Control Circuit | 4-201 |
| TL494 | Switchmode Pulse Width Modulation Control Circuits | 4-207 |
| TL495 | Switchmode Pulse Width Modulation Control Circuits | 4-207 |
| TL780 | Three-Terminal Positive Voltage Regulators | 4-218 |
| μA78S40 | Universal Switching Regulator Subsystem | 4-224 |

## Voltage References

| Device | Function | Page |
|---|---|---|
| LM285 | Micropower Voltage Reference Diodes | 4-237 |
| LM385 | Micropower Voltage Reference Diode | 4-237 |
| MC1400 | Precision Voltage References | 4-241 |
| MC1403,A | Precision Low-Voltage Reference | 4-246 |
| MC1404,A | Precision Low-Drift Voltage Reference | 4-250 |
| MC1500 | Precision Voltage References | 4-241 |
| MC1503,A | Precision Low-Voltage Reference | 4-246 |
| MC1504 | Precision Low-Drift Voltage Reference | 4-250 |
| TL431,A | Programmable Precision References | 4-255 |

## Supervisory Circuits

| Device | Function | Page |
|---|---|---|
| MC3324,A | Power Supply Supervisory Circuit/Dual-Voltage Comparator | 4-270 |
| MC3423 | Overvoltage Sensing Circuit | 4-263 |
| MC3424,A | Power Supply Supervisory Circuit/Dual-Voltage Comparator | 4-270 |
| MC3425,A | Power Supply Supervisory/Over-Under-Voltage Protection Circuit | 4-286 |
| MC3523 | Overvoltage Sensing Circuit | 4-263 |
| MC3524,A | Power Supply Supervisory Circuit/Dual-Voltage comparator | 4-270 |
| MC33031T | Series Switch Transient Protection Circuit | 4-294 |
| MC34061,A | Three-Terminal Programmable Overvoltage Sensing Circuit | 4-297 |
| MC34062 | Pin-Programmable Overvoltage Sensing Circuit | 4-304 |
| MC35062 | Pin-Programmable Overvoltage Sensing Circuit | 4-304 |

## Power Controllers

| Device | Function | Page |
|---|---|---|
| CA3059 | Zero Voltage Switch | 4-315 |
| CA3079 | Zero Voltage Switch | 4-315 |
| MC3344 | Programmable Frequency Switch | 4-320 |
| MC3479P | Stepper Motor Driver | 4-325 |
| MC3484V2,V4 | Integrated Solenoid Driver | 4-333 |
| MC33030 | DC Servo Motor Controller/Driver | 4-339 |
| MC33038 | High-Side Driver Switch | 4-352 |
| SAA1042,A | Stepper Motor Driver | 4-355 |
| TCA5600 | Universal Microprocessor Power Supply Controller | 4-360 |
| TCF5600 | Universal Microprocessor Power Supply Controller | 4-360 |
| TDA1085A | Universal Motor Speed Controller | 4-371 |
| TDA1085C | Universal Motor Speed Controller | 4-378 |
| TDA1185A | Triac Phase Angle Controller | 4-388 |
| TDA1285A | Universal Motor Speed Controller | 4-395 |
| UAA1016B | Zero Voltage Controller | 4-402 |

**MOTOROLA**

# LM109
# LM209
# LM309

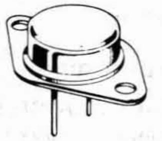
## MONOLITHIC POSITIVE THREE - TERMINAL FIXED VOLTAGE REGULATOR

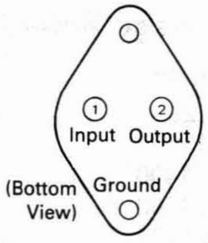
A versatile positive fixed +5.0-volt regulator designed for easy application as on on-card, local voltage regulator for digital logic systems. Current limiting and thermal shutdown are provided to make the units extremely rugged.

In most applications only one external component, a capacitor, is required in conjunction with the LM109 Series devices. Even this component may be omitted if the power-supply filter is not located an appreciable distance from the regulator.

- High Maximum Output Current – Over 1.0 Ampere in TO-3 type Package – Over 200 mA in TO-39 type Package.
- Minimum External Components Required
- Internal Short-Circuit Protection
- Internal Thermal Overload Protection
- Excellent Line and Load Transient Rejection
- Designed for Use with Popular MDTL and MTTL Logic

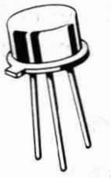
## POSITIVE VOLTAGE REGULATOR

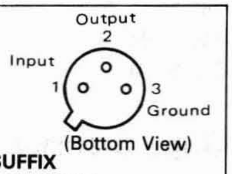




①
②
Input
Output
(Bottom View)
Ground

**K SUFFIX**
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)





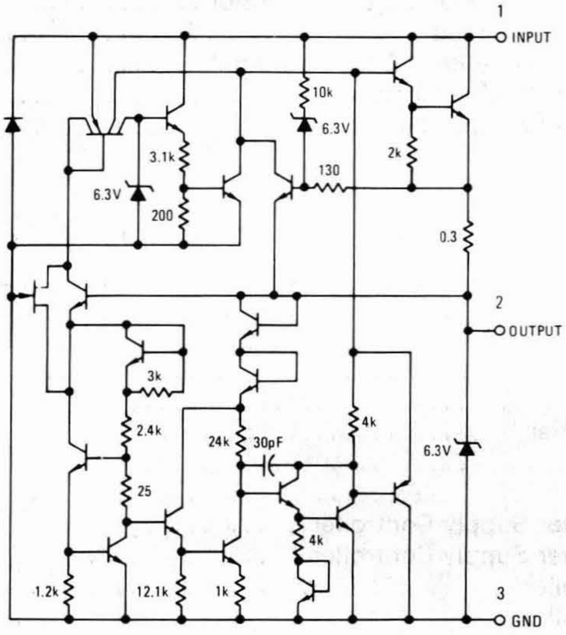
Output
2
Input
1
3
Ground
(Bottom View)

**H SUFFIX**
METAL PACKAGE
CASE 79-02
TO-205AD
(TO 39)

ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| LM109H | $T_J$ = −55°C to +150°C | Metal Can |
| LM109K | $T_J$ = −55°C to +150°C | Metal Power |
| LM209H | $T_J$ = −55°C to +150°C | Metal Can |
| LM209K | $T_J$ = −55°C to +150°C | Metal Power |
| LM309H | $T_J$ = 0°C to +125°C | Metal Can |
| LM309K | $T_J$ = 0°C to +125°C | Metal Power |

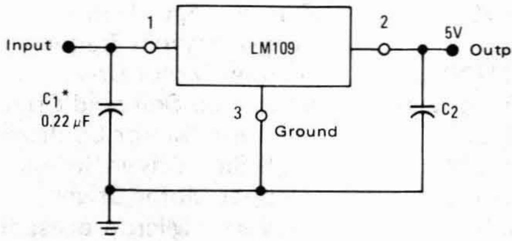
### CIRCUIT SCHEMATIC



1
INPUT
10k
6.3V
2k
3.1k
130
6.3V
200
0.3
2
OUTPUT
3k
2.4k
4k
24k
30pF
6.3V
25
4k
1.2k
12.1k
1k
3
GND

### TYPICAL APPLICATION

FIXED 5.0 V REGULATOR



1
2
Input
LM109
5V
Output
C1*
0.22 μF
3
Ground
C2

*Required if regulator is located an appreciable distance from power supply filter.
Although no output capacitor is needed for stability, it does improve transient response.

# LM109, LM209, LM309

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage | $V_{in}$ | 35 | Vdc |
| Power Dissipation | $P_D$ | Internally Limited | |
| Junction Temperature Range | $T_J$ | | °C |
| LM109 | | -55 to +150 | |
| LM209 | | -55 to +150 | |
| LM309 | | 0 to +125 | |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Lead Temperature<br>(soldering, t = 60 s) | $T_S$ | 300 | °C |

## ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | LM109/LM209 ① | | | LM309 ② | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 4.7 | 5.05 | 5.3 | 4.8 | 5.05 | 5.2 | Vdc |
| Input Regulation ($T_J$ = +25°C)<br>$7.0 \leqslant V_{in} \leqslant 25$ V | $Reg_{line}$ | – | 4.0 | 50 | – | 4.0 | 50 | mV |
| Load Regulation ($T_J$ = +25°C) | $Reg_{load}$ | | | | | | | mV |
| Case 11-01 **(type TO-3)** $5.0\text{ mA} \leqslant I_O \leqslant 1.5$A | | – | 50 | 100 | – | 50 | 100 | |
| Case 79-02 **(TO-39)** $5.0\text{ mA} \leqslant I_O \leqslant 0.5$A | | – | 20 | 50 | – | 20 | 50 | |
| Output Voltage Range<br>$7.0\text{ V} \leqslant V_{in} \leqslant 25$ V<br>$5.0\text{ mA} \leqslant I_O \leqslant I_{max}, P \leqslant P_{max}$ | $V_O$ | 4.6 | – | 5.4 | 4.75 | – | 5.25 | Vdc |
| Quiescent Current ($7.0\text{ V} \leqslant V_{in} \leqslant 25$ V) | $I_B$ | – | 5.2 | 10 | – | 5.2 | 10 | mAdc |
| Quiescent Current Change ($7.0\text{ V} \leqslant V_{in} \leqslant 25$ V) | $\Delta I_B$ | | – | 0.5 | – | – | 0.5 | |
| $5.0\text{ mA} \leqslant I_O \leqslant I_{max}$ | | – | – | 0.8 | – | – | 0.8 | |
| Output Noise Voltage ($T_A$ = +25°C)<br>$10\text{ Hz} \leqslant f \leqslant 100$ kHz | $V_N$ | – | 40 | – | – | 40 | – | µV |
| Long Term Stability | S | – | – | 10 | – | – | 20 | mV |
| Thermal Resistance, Junction to Case ③ | $\theta JC$ | | | | | | | °C/W |
| Case 1 (type TO-3) | | – | 3.0 | – | – | 3.0 | – | |
| Case 79-02 (TO-39) | | – | 15 | – | – | 15 | – | |

NOTES:

① Unless otherwise specified, these specifications apply for $-55°C \leqslant T_J \leqslant +150°$ ($-25°C \leqslant T_J \leqslant +150°C$ for the LM209). For Case 79-02 (TO-39) $V_{in}$ = 10 V, $I_O$ = 0.1 A, $I_{max}$ = 0.2 A and $P_{max}$ = 2.0 W. For Case 1 **(type TO-3)** $V_{in}$ = 10 V, $I_O$ = 0.5 A, $I_{max}$ = 1.0 A and $P_{max}$ = 20 W.

② Unless otherwise specified, these specifications apply for $0°C \leqslant T_J \leqslant +125°C$, $V_{in}$ = 10V. For Case 79 02 (TO-39) $I_O$ = 0.1A, $I_{max}$ = 0.2A and, $P_{max}$ = 2.0 W. For Case 1. (type TO-3) $I_O$ = 0.5 A., $I_{max}$ = 1.0 A and $P_{max}$ = 20 W.

③ Without a heat sink, the thermal resistance of the Case 79-02 **(TO-39)** package is about 150°C/W, while that of the Case 1 (type TO-3) package is aoproximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the heat sink.

## TYPICAL CHARACTERISTICS

**($V_{in}$ = 10 V, $T_A$ = +25°C unless otherwise noted.)**

**FIGURE 1 – MAXIMUM AVERAGE POWER DISSIPATION (LM109K, LM209K)**

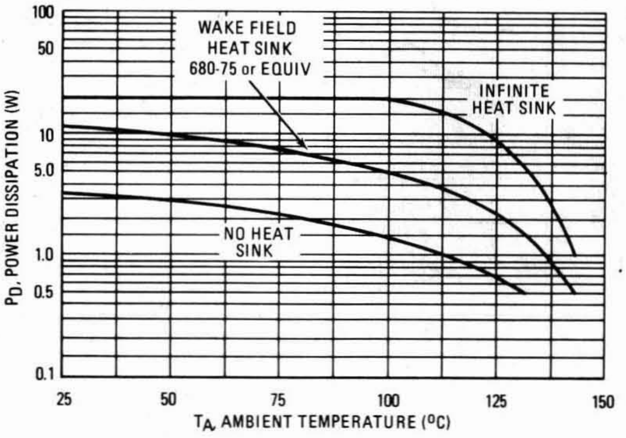
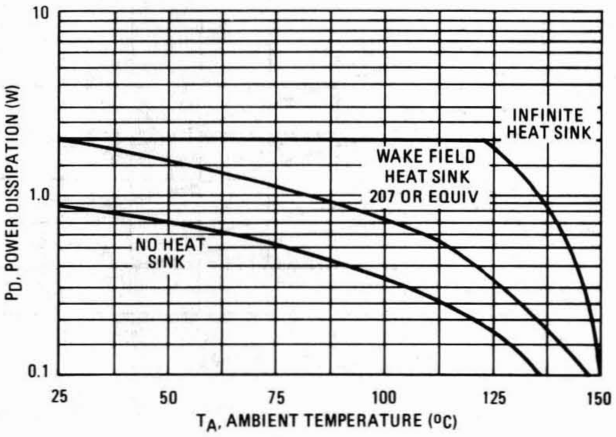


**FIGURE 2 – MAXIMUM AVERAGE POWER DISSIPATION (LM109H, LM209H)**



## TYPICAL CHARACTERISTICS (continued)

($V_{in}$ = 10 V, $T_A$ = +25°C unless otherwise noted.)

FIGURE 3 – MAXIMUM AVERAGE POWER DISSIPATION (LM309K)

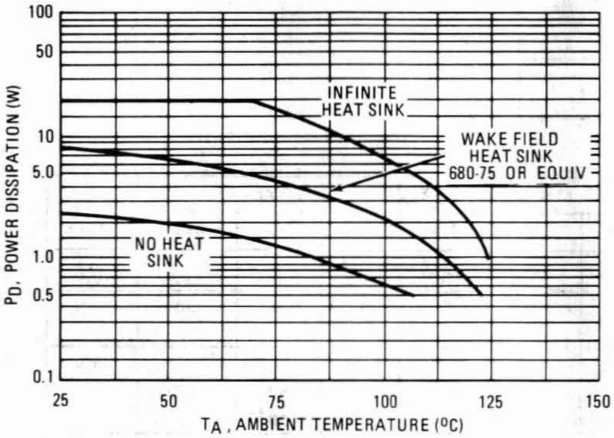


FIGURE 4 – MAXIMUM AVERAGE POWER DISSIPATION (LM309H)

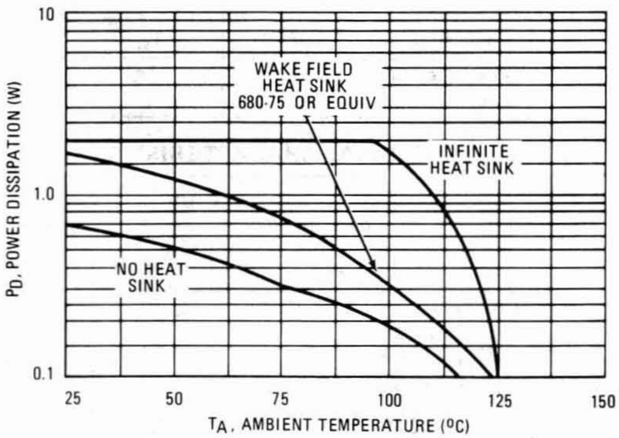


FIGURE 5 - OUTPUT IMPEDANCE versus FREQUENCY

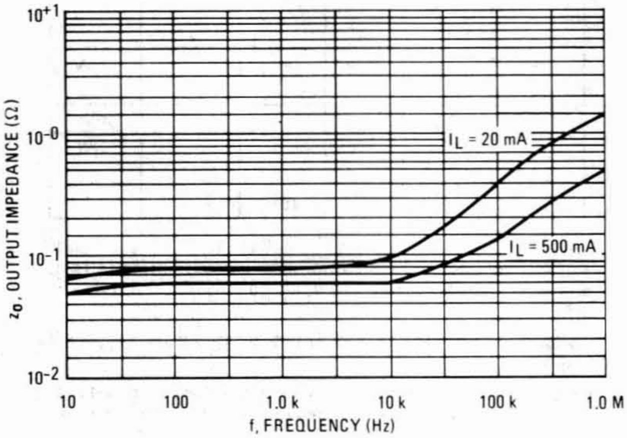


FIGURE 6 – PEAK OUTPUT CURRENT (K PACKAGE)

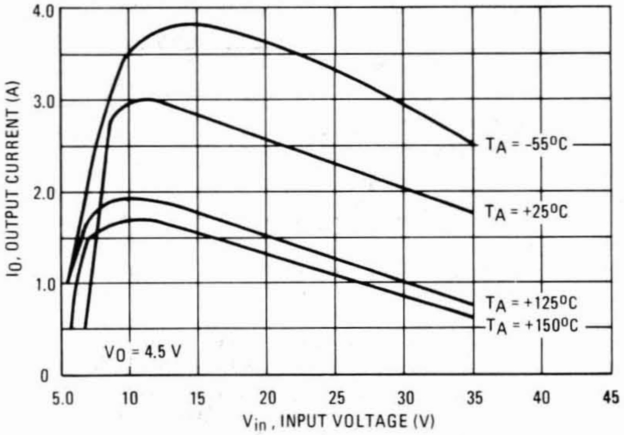


FIGURE 7 – PEAK OUTPUT CURRENT (H PACKAGE)

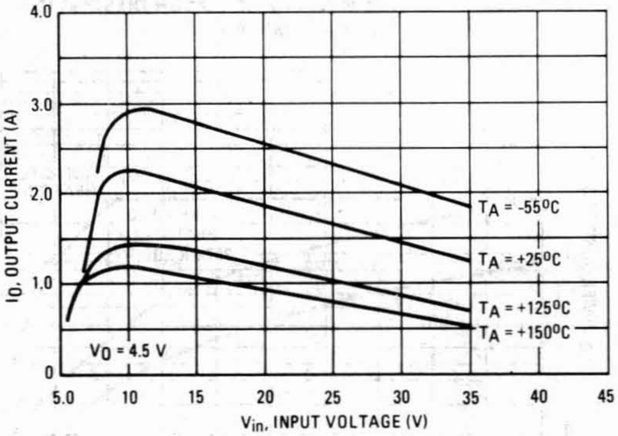
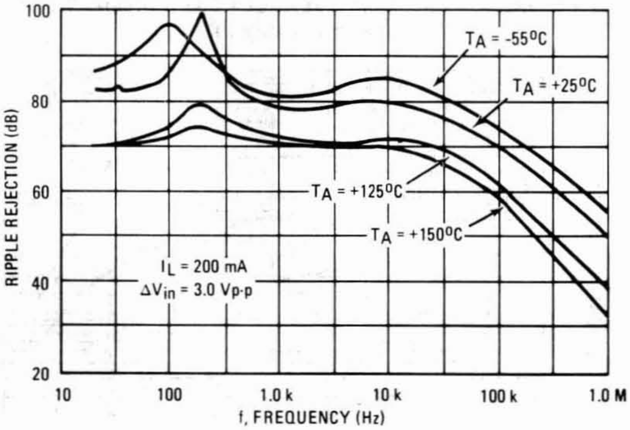


FIGURE 8 – RIPPLE REJECTION



## TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DROPOUT VOLTAGE

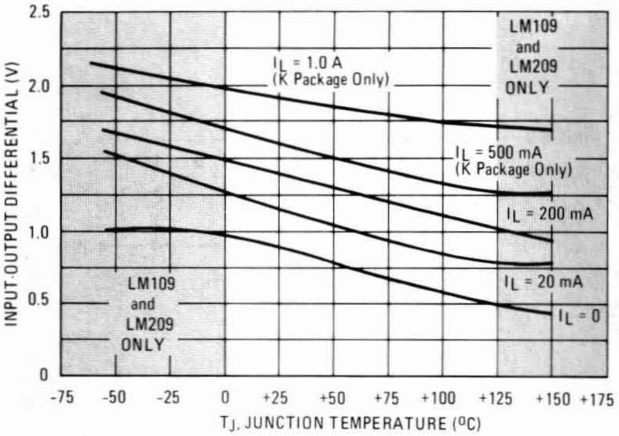


FIGURE 10 – DROPOUT CHARACTERISTIC (K PACKAGE)

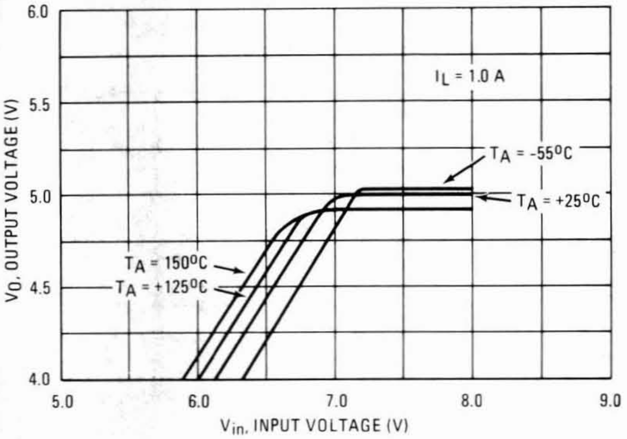


FIGURE 11 – OUTPUT VOLTAGE

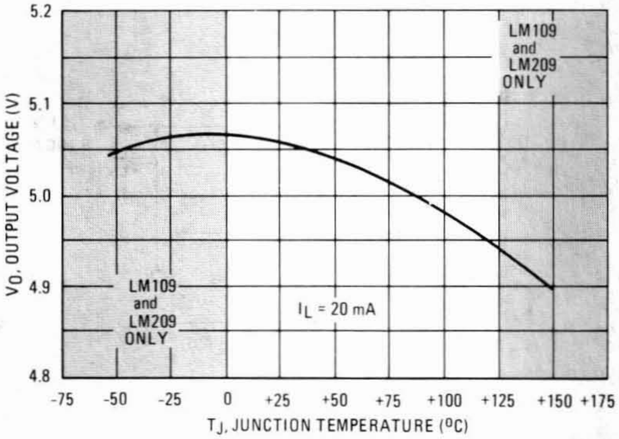


FIGURE 12 – OUTPUT NOISE VOLTAGE

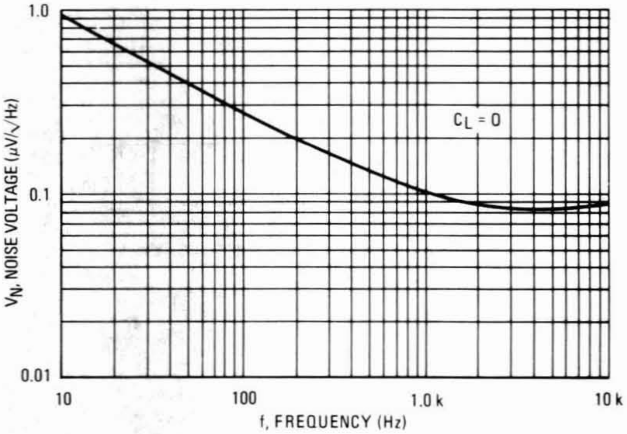


FIGURE 13 – QUIESCENT CURRENT

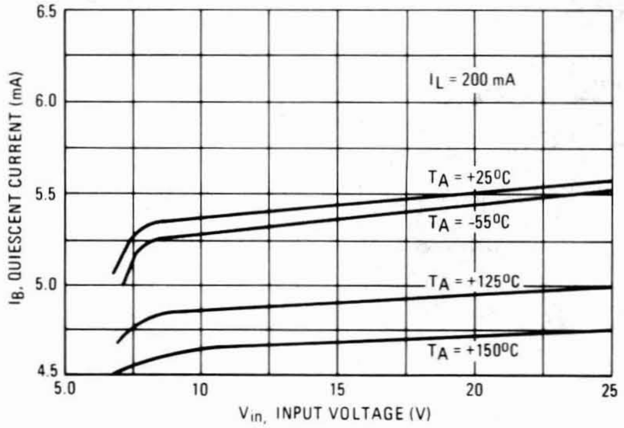
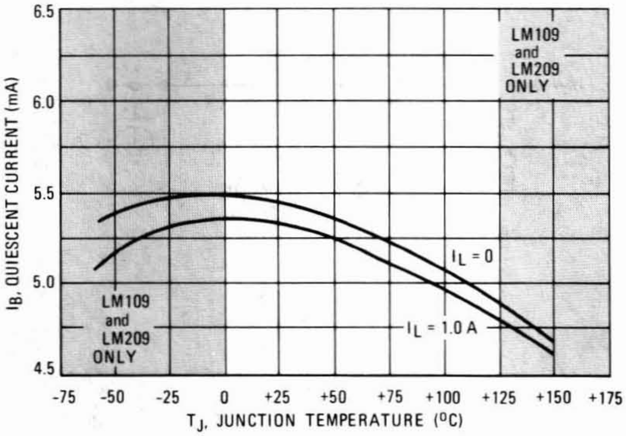


FIGURE 14 – QUIESCENT CURRENT



## TYPICAL APPLICATIONS

**FIGURE 15 – ADJUSTABLE OUTPUT REGULATOR**

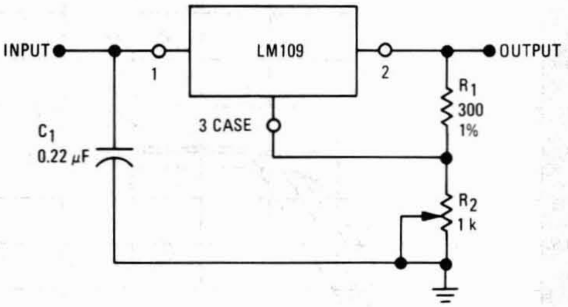
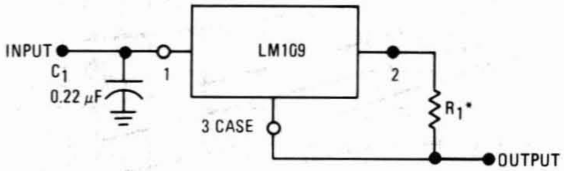

INPUT
LM109
1
2
OUTPUT
3 CASE
$C_1$
0.22 μF
$R_1$
300
1%
$R_2$
1 k

**FIGURE 16 – CURRENT REGULATOR**


INPUT
$C_1$
0.22 μF
1
LM109
2
3 CASE
$R_1$*
OUTPUT

*DETERMINES OUTPUT CURRENT.

**FIGURE 17 – 5.0-VOLT, 3.0-AMPERE REGULATOR**
**(with plastic boost transistor)**

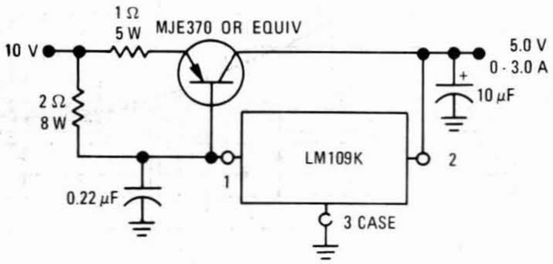

1 Ω
5 W
MJE370 OR EQUIV
10 V
5.0 V
0 - 3.0 A
10 μF
2 Ω
8 W
LM109K
1
2
0.22 μF
3 CASE

**FIGURE 18 – 5.0 VOLT, 4.0-AMPERE TRANSISTOR**
**(with plastic Darlington boost transistor)**

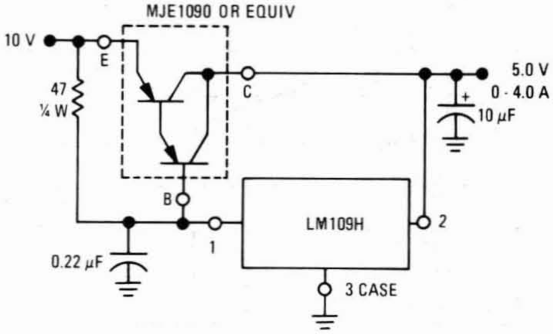

MJE1090 OR EQUIV
10 V
E
47
¼ W
C
5.0 V
0 - 4.0 A
10 μF
B
LM109H
1
2
0.22 μF
3 CASE

**FIGURE 19 – 5.0-VOLT, 10-AMPERE REGULATOR**

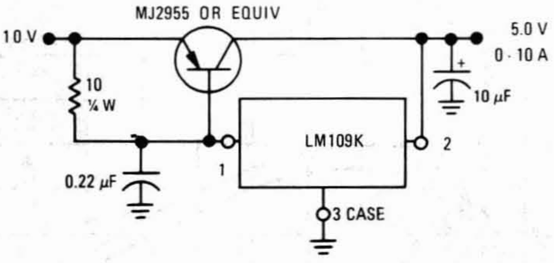
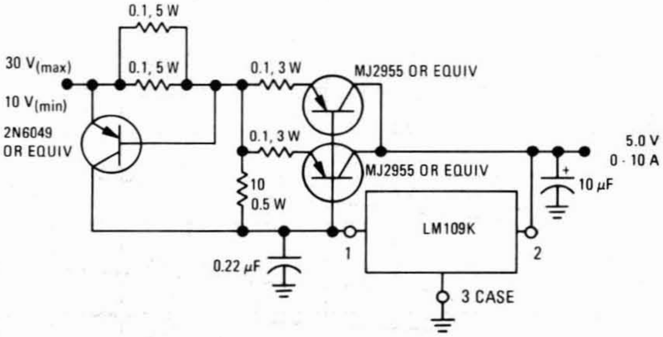

MJ2955 OR EQUIV
10 V
5.0 V
0 - 10 A
10 μF
10
¼ W
LM109K
1
2
0.22 μF
3 CASE

**FIGURE 20 – 5.0-VOLT, 10-AMPERE REGULATOR**
**(with Short-Circuit Current Limiting for**
**Safe-Area Protection of pass transistors)**


0.1, 5 W
30 V(max)
0.1, 5 W
0.1, 3 W
MJ2955 OR EQUIV
10 V(min)
2N6049
OR EQUIV
0.1, 3 W
5.0 V
0 - 10 A
10
0.5 W
MJ2955 OR EQUIV
10 μF
LM109K
1
2
0.22 μF
3 CASE

**MOTOROLA**

# LM117
# LM217
# LM317

## Specifications and Applications Information

**3-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR**

SILICON MONOLITHIC INTEGRATED CIRCUIT

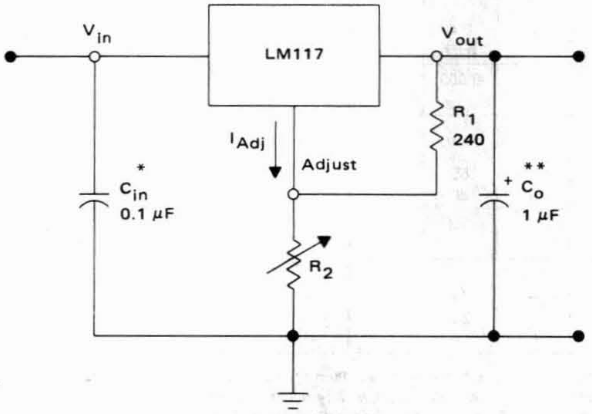
### 3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

The LM117/217/317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117 series serve a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in TO-3 and TO-220 Packages
- Output Current in Excess of 0.5 Ampere in TO-39 Package
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

### STANDARD APPLICATION



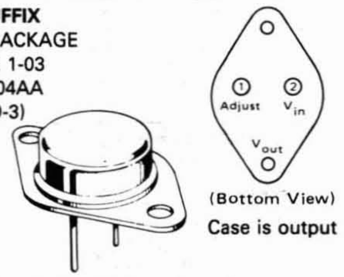
* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_o$ is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

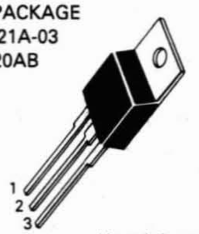
Since $I_{Adj}$ is controlled to less than 100 μA, the error associated with this term is negligible in most applications

**K SUFFIX**
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)



Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

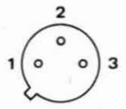
**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220AB



Pin 1 Adjust
Pin 2 $V_{out}$
Pin 3 $V_{in}$

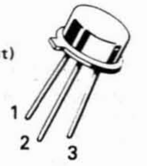
Heatsink surface connected to Pin 2

**H SUFFIX**
METAL PACKAGE
CASE 79-02
TO-205AD
(TO-39)



(Bottom View)

(Case is output)



Pin 1 $V_{in}$
Pin 2 Adjust
Pin 3 $V_{out}$

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| LM117H | $T_J$ = -55°C to +150°C | Metal Can |
| LM117K | $T_J$ = -55°C to +150°C | Metal Power |
| LM217H | $T_J$ = -25°C to +150°C | Metal Can |
| LM217K | $T_J$ = -25°C to +150°C | Metal Power |
| LM317H | $T_J$ = 0°C to +125°C | Metal Can |
| LM317K | $T_J$ = 0°C to +125°C | Metal Power |
| LM317T | $T_J$ = 0°C to +125°C | Plastic Power |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input-Output Voltage Differential | $V_I$-$V_O$ | 40 | Vdc |
| Power Dissipation | $P_D$ | Internally Limited | |
| Operating Junction Temperature Range<br>LM117<br>LM217<br>LM317 | $T_J$ | <br>-55 to +150<br>-25 to +150<br>0 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

## ELECTRICAL CHARACTERISTICS

($V_I$-$V_O$ = 5.0 V; $I_O$ = 0.5 A for K and T packages; $I_O$ = 0.1 A for H package; $T_J$ = $T_{low}$ to $T_{high}$ [see Note 1]; $I_{max}$ and $P_{max}$ per Note 2; unless otherwise specified.)

| Characteristic | Figure | Symbol | LM117/217 | | | LM317 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation (Note 3)<br>$T_A$ = 25°C, 3.0 V ≤ $V_I$-$V_O$ ≤ 40 V | 1 | $Reg_{line}$ | — | 0.01 | 0.02 | — | 0.01 | 0.04 | %/V |
| Load Regulation (Note 3)<br>$T_A$ = 25°C, 10 mA ≤ $I_O$ ≤ $I_{max}$<br>$V_O$ ≤ 5.0 V<br>$V_O$ ≥ 5.0 V | 2 | $Reg_{load}$ | <br><br>—<br>— | <br><br>5.0<br>0.1 | <br><br>15<br>0.3 | <br><br>—<br>— | <br><br>5.0<br>0.1 | <br><br>25<br>0.5 | <br><br>mV<br>% $V_O$ |
| Thermal Regulation ($T_A$ = +25°C)<br>20 ms Pulse | | — | — | 0.02 | 0.07 | — | 0.03 | 0.07 | %/W |
| Adjustment Pin Current | 3 | $I_{Adj}$ | — | 50 | 100 | — | 50 | 100 | μA |
| Adjustment Pin Current Change<br>2.5 V ≤ $V_I$-$V_O$ ≤ 40 V<br>10 mA ≤ $I_L$ ≤ $I_{max}$, $P_D$ ≤ $P_{max}$ | 1,2 | $\Delta I_{Adj}$ | — | 0.2 | 5.0 | — | 0.2 | 5.0 | μA |
| Reference Voltage (Note 4)<br>3.0 V ≤ $V_I$-$V_O$ ≤ 40 V<br>10 mA ≤ $I_O$ ≤ $I_{max}$, $P_D$ ≤ $P_{max}$ | 3 | $V_{ref}$ | 1.20 | 1.25 | 1.30 | 1.20 | 1.25 | 1.30 | V |
| Line Regulation (Note 3)<br>3.0 V ≤ $V_I$-$V_O$ ≤ 40 V | 1 | $Reg_{line}$ | — | 0.02 | 0.05 | — | 0.02 | 0.07 | %/V |
| Load Regulation (Note 3)<br>10 mA ≤ $I_O$ ≤ $I_{max}$<br>$V_O$ ≤ 5.0 V<br>$V_O$ ≥ 5.0 V | 2 | $Reg_{load}$ | <br><br>—<br>— | <br><br>20<br>0.3 | <br><br>50<br>1.0 | <br><br>—<br>— | <br><br>20<br>0.3 | <br><br>70<br>1.5 | <br><br>mV<br>% $V_O$ |
| Temperature Stability ($T_{low}$ ≤ $T_J$ ≤ $T_{high}$) | 3 | $T_S$ | — | 0.7 | — | — | 0.7 | — | % $V_O$ |
| Minimum Load Current to Maintain Regulation ($V_I$-$V_O$ = 40 V) | 3 | $I_{Lmin}$ | — | 3.5 | 5.0 | — | 3.5 | 10 | mA |
| Maximum Output Current<br>$V_I$-$V_O$ ≤ 15 V, $P_D$ ≤ $P_{max}$<br>K and T Packages<br>H Package<br>$V_I$-$V_O$ = 40 V, $P_D$ ≤ $P_{max}$, $T_A$ = 25°C<br>K and T Packages<br>H Package | 3 | $I_{max}$ | <br><br>1.5<br>0.5<br><br>0.25<br>— | <br><br>2.2<br>0.8<br><br>0.4<br>0.07 | <br><br>—<br>—<br><br>—<br>— | <br><br>1.5<br>0.5<br><br>0.15<br>— | <br><br>2.2<br>0.8<br><br>0.4<br>0.07 | <br><br>—<br>—<br><br>—<br>— | A |
| RMS Noise, % of $V_O$<br>$T_A$ = 25°C, 10 Hz ≤ f ≤ 10 kHz | — | N | — | 0.003 | — | — | 0.003 | — | % $V_O$ |
| Ripple Rejection, $V_O$ = 10 V, f = 120 Hz (Note 5)<br>Without $C_{Adj}$<br>$C_{Adj}$ = 10 μF | 4 | RR | <br>—<br>66 | <br>65<br>80 | <br>—<br>— | <br>—<br>66 | <br>65<br>80 | <br>—<br>— | dB |
| Long-Term Stability, $T_J$ = $T_{high}$ (Note 6)<br>$T_A$ = 25°C for Endpoint Measurements | 3 | S | — | 0.3 | 1.0 | — | 0.3 | 1.0 | %/1.0 k Hrs. |
| Thermal Resistance Junction to Case<br>H Package (TO-39)<br>K Package (TO-3)<br>T Package (TO-220) | — | $R_{\theta JC}$ | <br>—<br>—<br>— | <br>12<br>2.3<br>— | <br>15<br>3.0<br>— | <br>—<br>—<br>— | <br>12<br>2.3<br>5.0 | <br>15<br>3.0<br>— | °C/W |

NOTES:
(1) $T_{low}$ = −55°C for LM117 $T_{high}$ = +150°C for LM117
= −25°C for LM217 = +150°C for LM217
= 0°C for LM317 = +125°C for LM317
(2) $I_{max}$ = 1.5 A for K (TO-3) and T (TO-220) Packages
= 0.5 A for H (TO-39) Package
$P_{max}$ = 20 W for K (TO-3) Package
= 20 W for T (TO-220) Package
= 2.0 W for H (TO-39) Package
(3) Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
(4) Selected devices with tightened tolerance reference voltage available.
(5) $C_{ADJ}$, when used, is connected between the adjustment pin and ground.
(6) Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

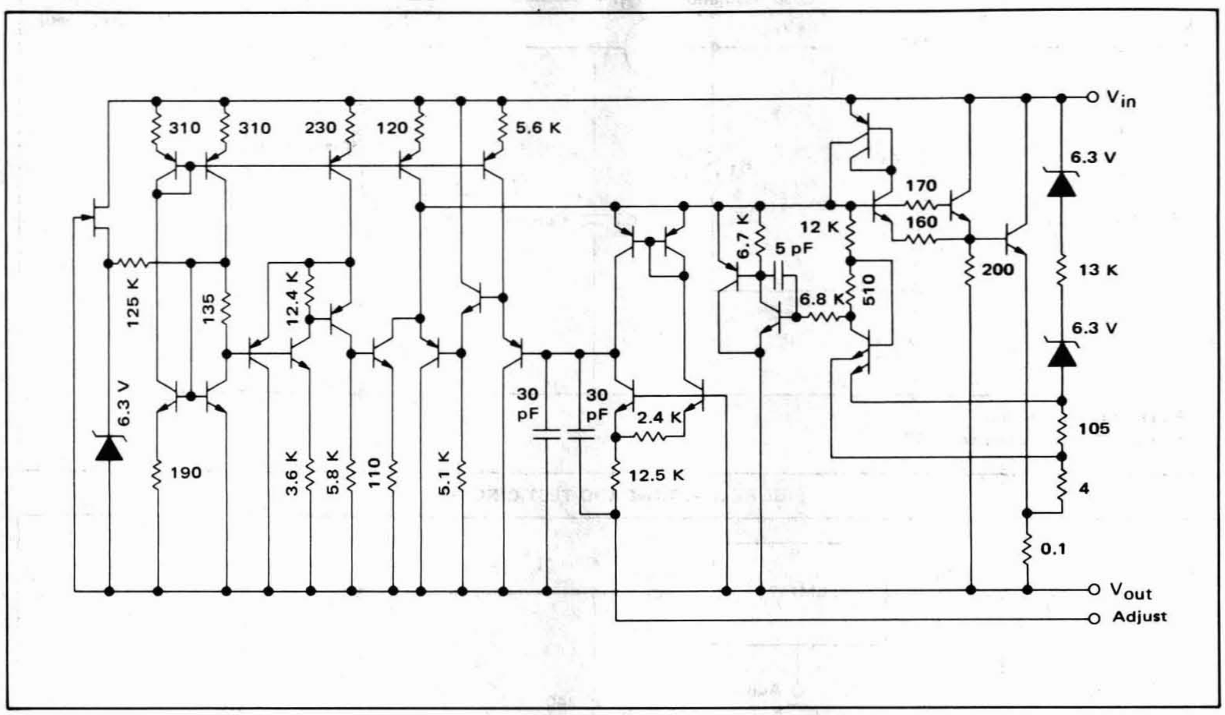
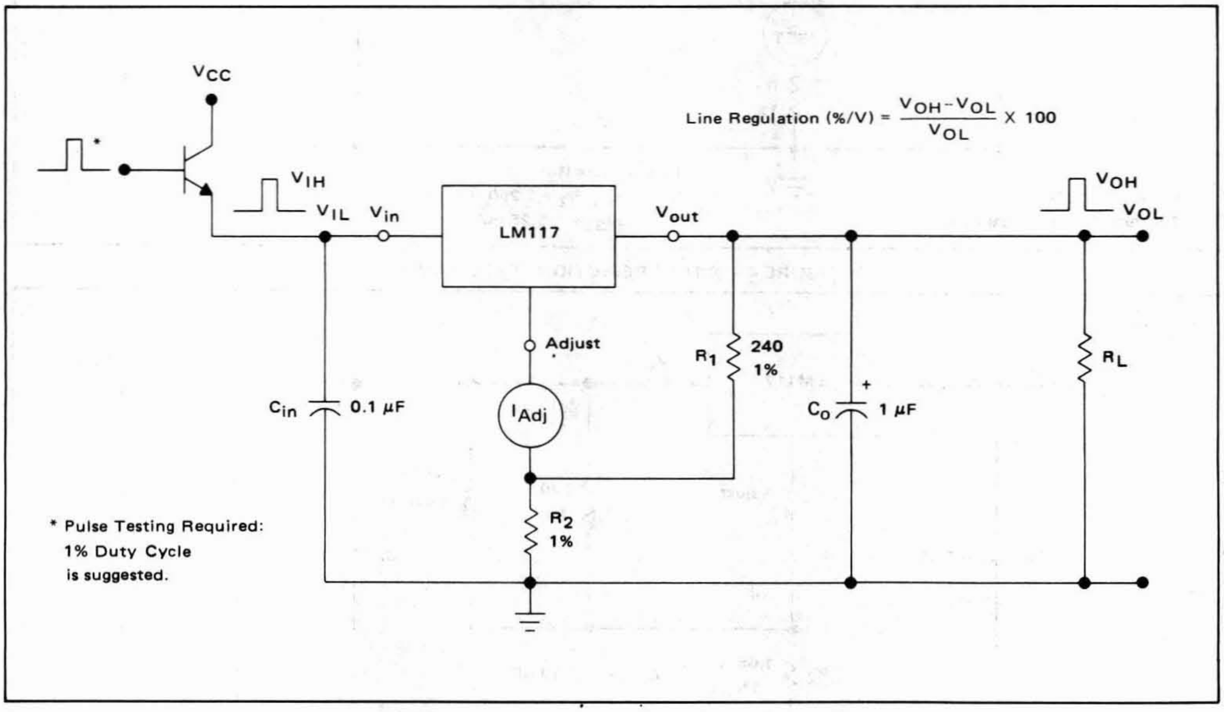
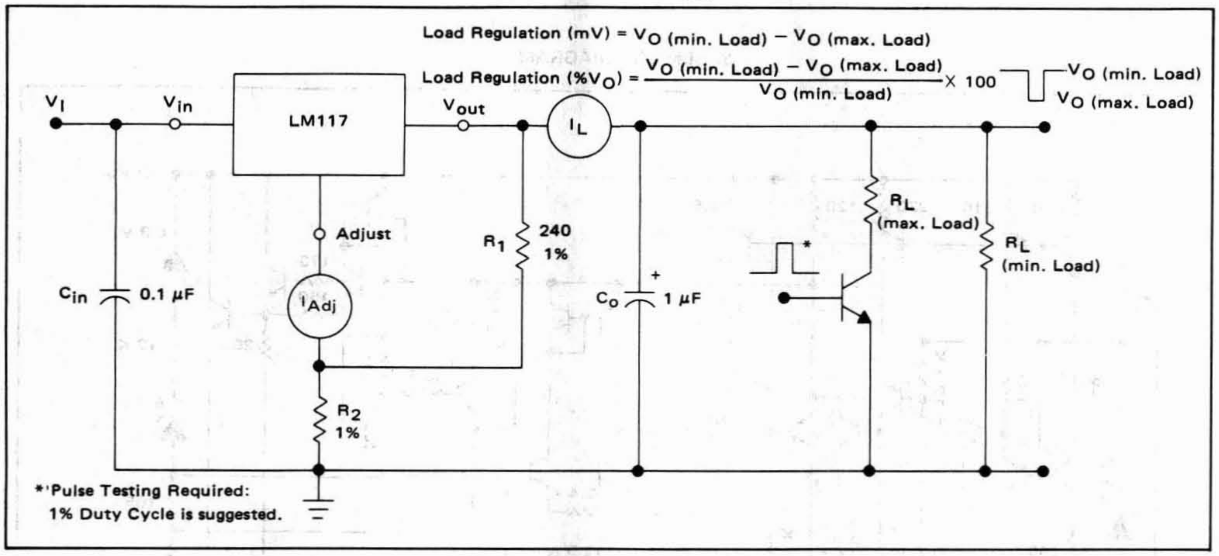

310
310
230
120
5.6 K
$V_{in}$
6.3 V
170
160
12 K
6.7 K
5 pF
200
13 K
125 K
135
12.4 K
6.8 K
510
6.3 V
6.3 V
30 pF
30 pF
2.4 K
105
190
3.6 K
5.8 K
110
5.1 K
12.5 K
4
0.1
$V_{out}$
Adjust

FIGURE 1 – LINE REGULATION AND $\Delta I_{Adj}$/LINE TEST CIRCUIT


$V_{CC}$
*
Line Regulation (%/V) = $\frac{V_{OH} - V_{OL}}{V_{OL}}$ X 100
$V_{IH}$
$V_{IL}$
$V_{in}$
LM117
$V_{out}$
$V_{OH}$
$V_{OL}$
Adjust
$R_1$
240
1%
$R_L$
$C_{in}$
0.1 µF
$I_{Adj}$
$C_o$
+
1 µF
$R_2$
1%

* Pulse Testing Required:
1% Duty Cycle
is suggested.

FIGURE 2 – LOAD REGULATION AND $\Delta I_{Adj}$/LOAD TEST CIRCUIT

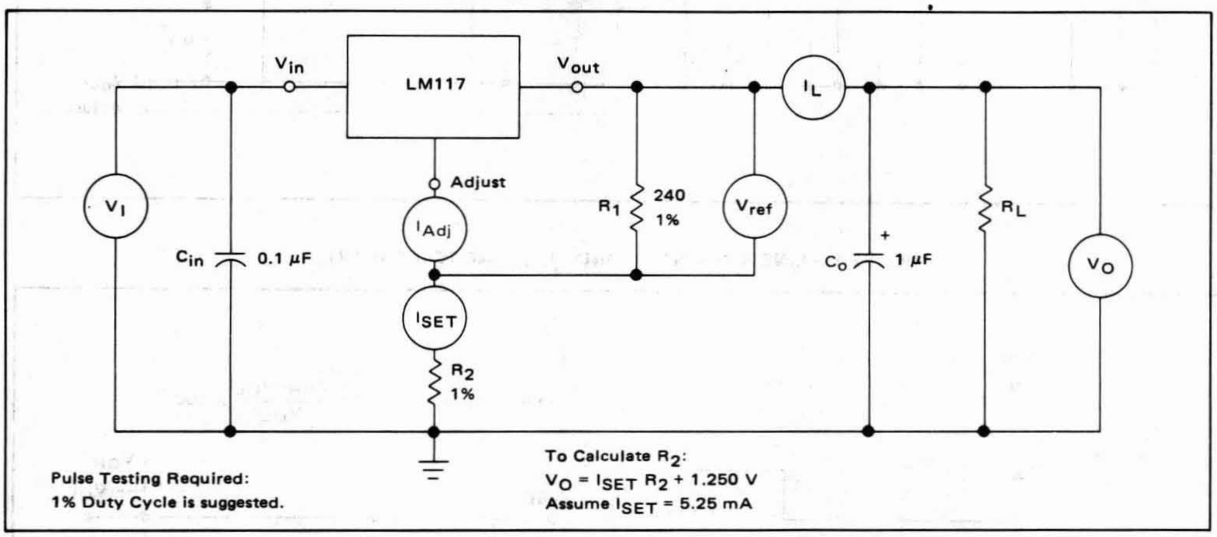

$V_I$
$V_{in}$
LM117
$V_{out}$
$I_L$
Adjust
$R_1$
240
1%
$C_{in}$
0.1 µF
$I_{Adj}$
$R_2$
1%
$C_O$
1 µF
+
*
$R_L$ (max. Load)
$R_L$ (min. Load)
$V_O$ (min. Load)
$V_O$ (max. Load)

Load Regulation (mV) = $V_O$ (min. Load) – $V_O$ (max. Load)

$$\text{Load Regulation } (\%V_O) = \frac{V_O\text{ (min. Load)} - V_O\text{ (max. Load)}}{V_O\text{ (min. Load)}} \times 100$$

*Pulse Testing Required:
1% Duty Cycle is suggested.

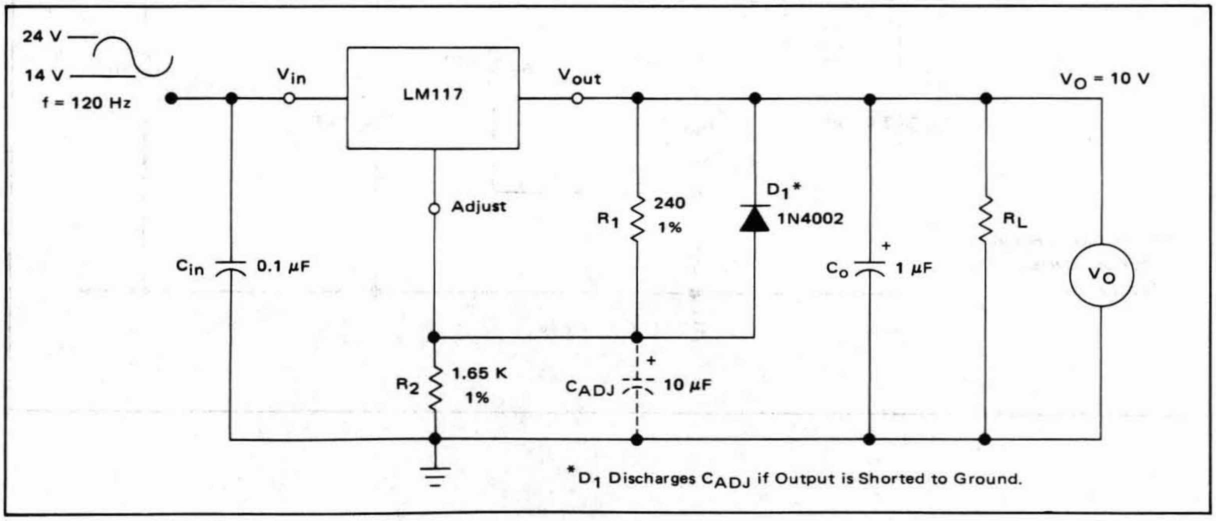
FIGURE 3 – STANDARD TEST CIRCUIT


$V_{in}$
LM117
$V_{out}$
$I_L$
$V_I$
Adjust
$I_{Adj}$
$R_1$
240
1%
$V_{ref}$
$C_{in}$
0.1 µF
$C_O$
1 µF
+
$R_L$
$V_O$
$I_{SET}$
$R_2$
1%

Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate $R_2$:
$V_O = I_{SET} R_2 + 1.250$ V
Assume $I_{SET}$ = 5.25 mA

FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT


24 V
14 V
f = 120 Hz
$V_{in}$
LM117
$V_{out}$
$V_O$ = 10 V
Adjust
$R_1$
240
1%
$D_1$*
1N4002
$R_L$
$C_{in}$
0.1 µF
$C_O$
1 µF
+
$V_O$
$R_2$
1.65 K
1%
$C_{ADJ}$
10 µF
+

*$D_1$ Discharges $C_{ADJ}$ if Output is Shorted to Ground.

FIGURE 5 – LOAD REGULATION

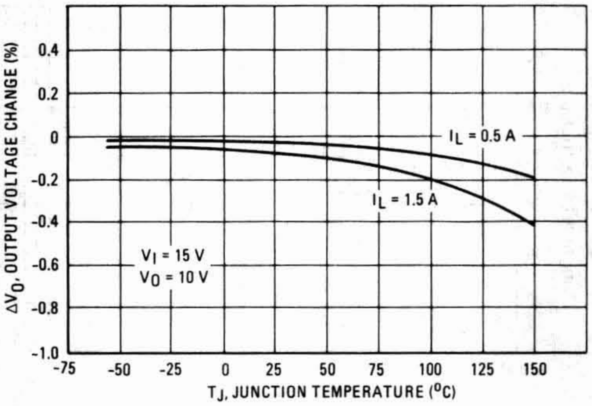


FIGURE 6 – CURRENT LIMIT

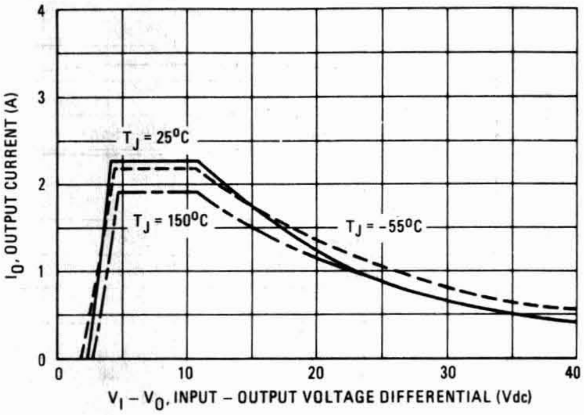


FIGURE 7 – ADJUSTMENT PIN CURRENT

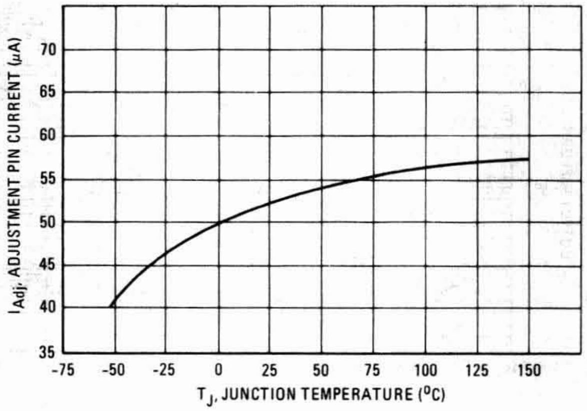


FIGURE 8 – DROPOUT VOLTAGE

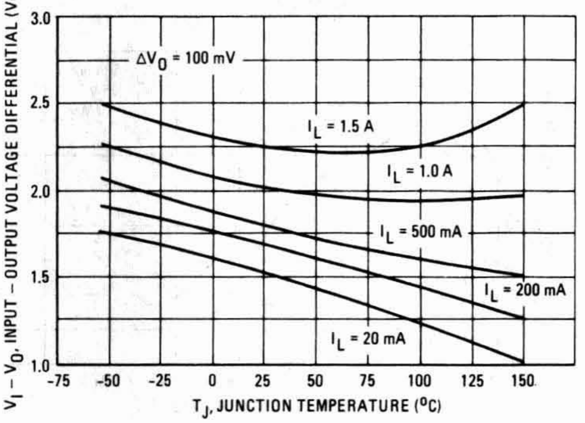


FIGURE 9 – TEMPERATURE STABILITY

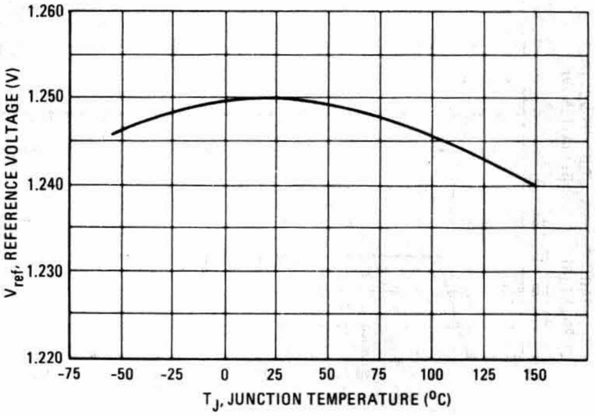


FIGURE 10 – MINIMUM OPERATING CURRENT

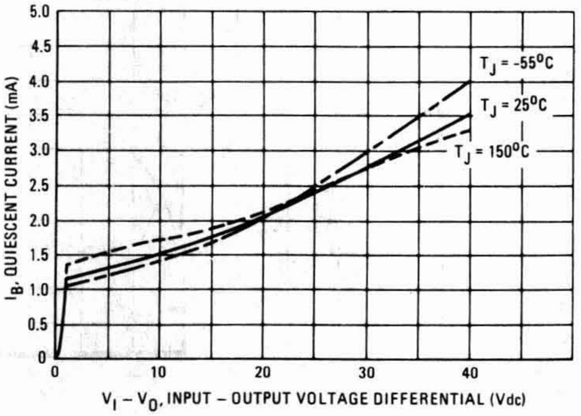


**FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE**

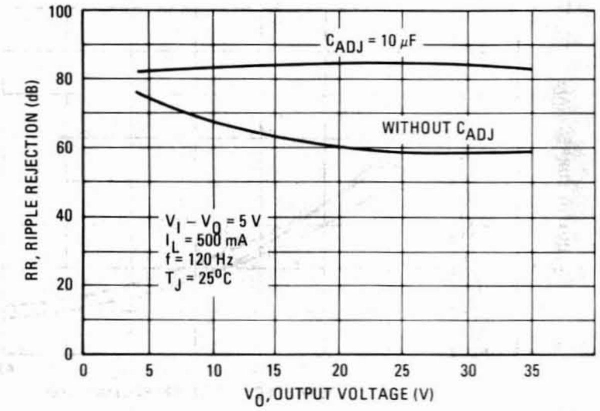


**FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT**

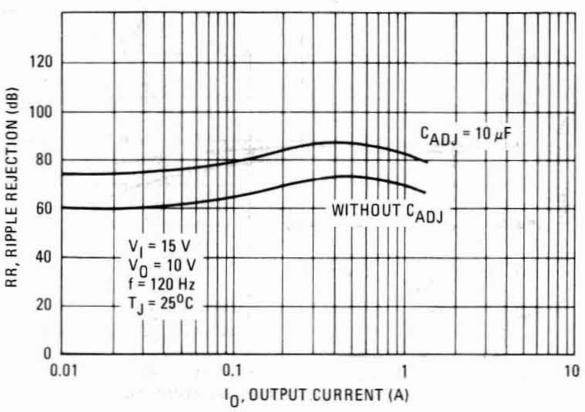


**FIGURE 13 — RIPPLE REJECTION versus FREQUENCY**

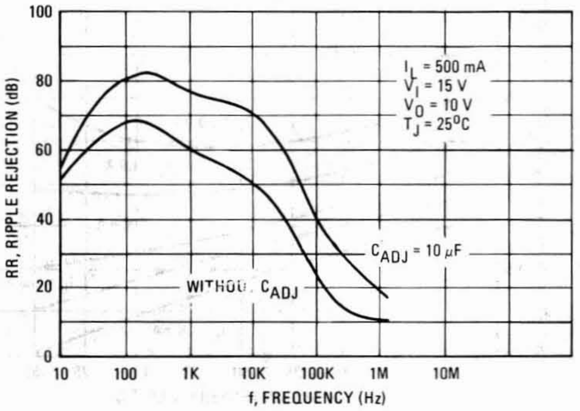


**FIGURE 14 — OUTPUT IMPEDANCE**

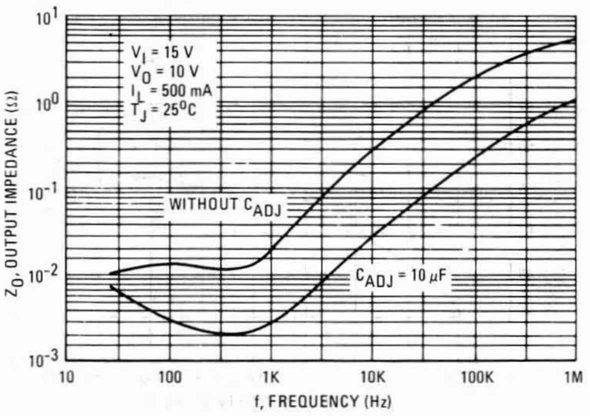


**FIGURE 15 — LINE TRANSIENT RESPONSE**

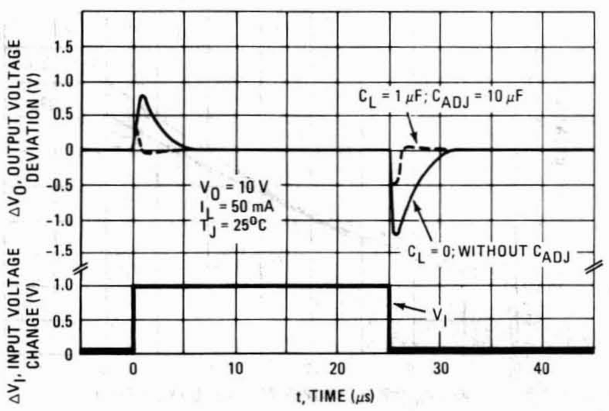
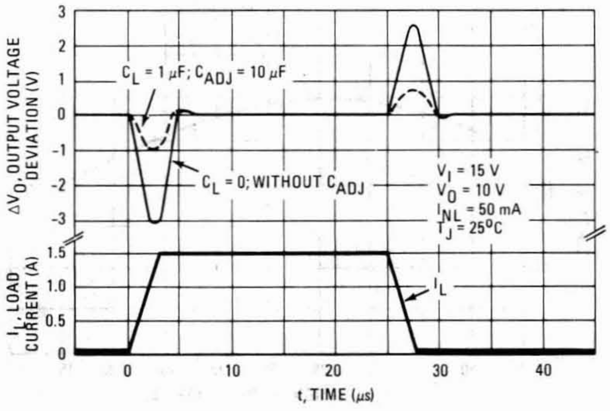


**FIGURE 16 — LOAD TRANSIENT RESPONSE**



## APPLICATIONS INFORMATION

### BASIC CIRCUIT OPERATION

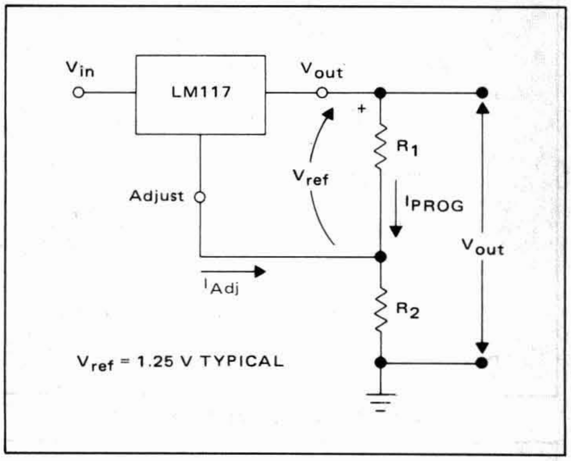
The LM117 is a 3-terminal floating regulator. In operation, the LM117 develops and maintains a nominal 1.25 volt reference ($V_{ref}$) between its output and adjustment terminals. This reference voltage is converted to a programming current ($I_{PROG}$) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\,(1 + \frac{R2}{R1}) + I_{Adj}\,R2$$

Since the current from the adjustment terminal ($I_{Adj}$) represents an error term in the equation, the LM117 was designed to control $I_{Adj}$ to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



### LOAD REGULATION

The LM117 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

### EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor ($C_{in}$) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor ($C_{ADJ}$) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance ($C_o$) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

### PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM117 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_o > 25$ μF, $C_{ADJ} > 10$ μF). Diode $D_1$ prevents $C_o$ from discharging thru the I.C. during an input short circuit. Diode $D_2$ protects against capacitor $C_{ADJ}$ discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents $C_{ADJ}$ from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

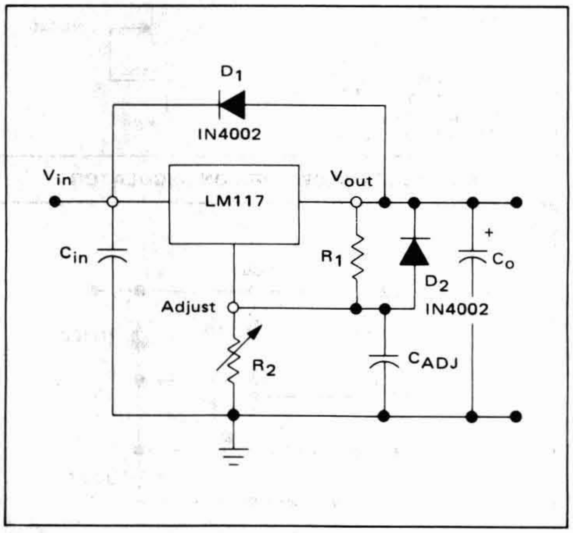
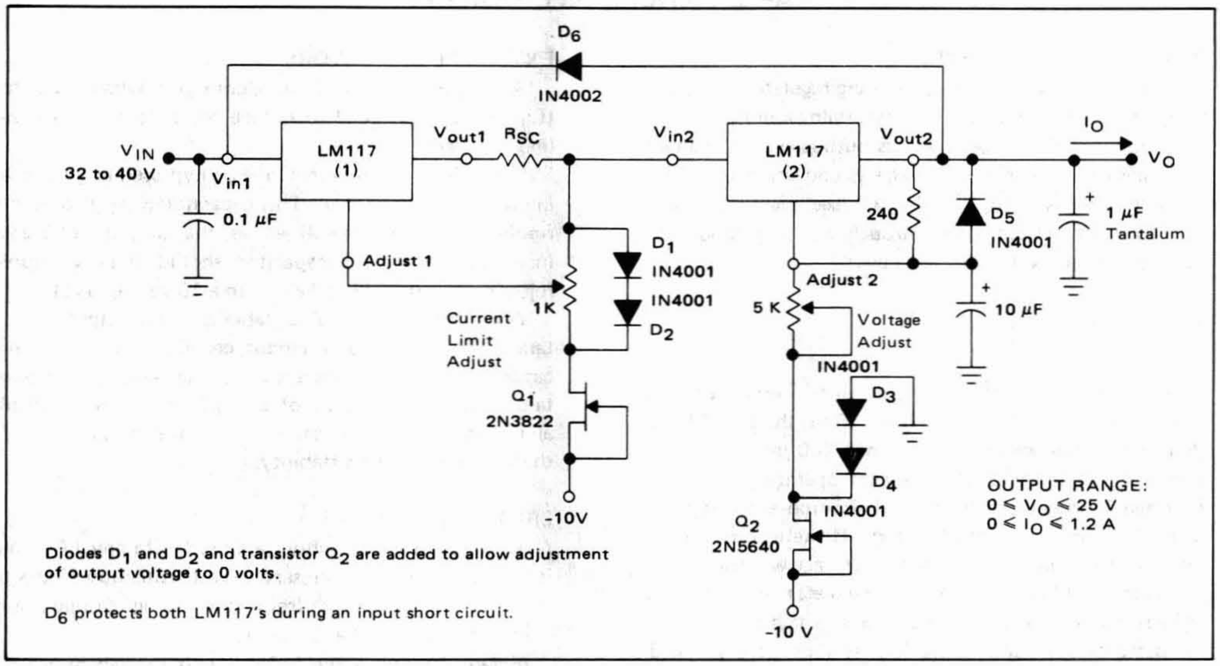


FIGURE 19 – "LABORATORY" POWER SUPPLY WITH ADJUSTABLE CURRENT LIMIT AND OUTPUT VOLTAGE

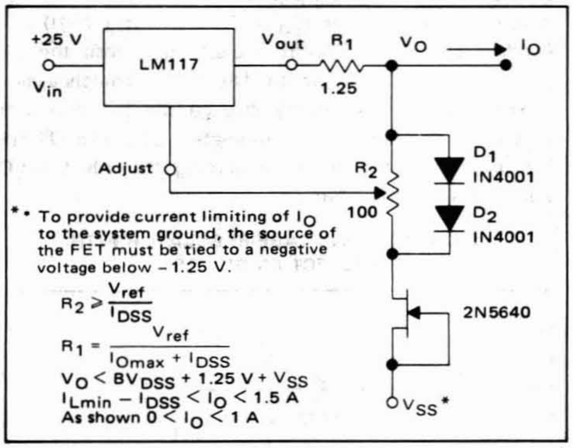

D6
1N4002
VIN
32 to 40 V
Vin1
0.1 µF
LM117
(1)
Adjust 1
Vout1
RSC
D1
1N4001
1N4001
D2
1K
Current
Limit
Adjust
Q1
2N3822
-10V
Vin2
LM117
(2)
Vout2
240
Adjust 2
5 K
Voltage
Adjust
1N4001
D3
D4
1N4001
Q2
2N5640
-10 V
D5
1N4001
10 µF
IO
VO
1 µF
Tantalum

OUTPUT RANGE:
$0 \leq V_O \leq 25$ V
$0 \leq I_O \leq 1.2$ A

Diodes $D_1$ and $D_2$ and transistor $Q_2$ are added to allow adjustment of output voltage to 0 volts.

$D_6$ protects both LM117's during an input short circuit.

FIGURE 20 – ADJUSTABLE CURRENT LIMITER


+25 V
Vin
LM117
Vout
R1
1.25
VO
IO
Adjust
R2
100
D1
IN4001
D2
IN4001
2N5640
VSS*

* To provide current limiting of $I_O$ to the system ground, the source of the FET must be tied to a negative voltage below −1.25 V.

$R_2 \geq \frac{V_{ref}}{I_{DSS}}$

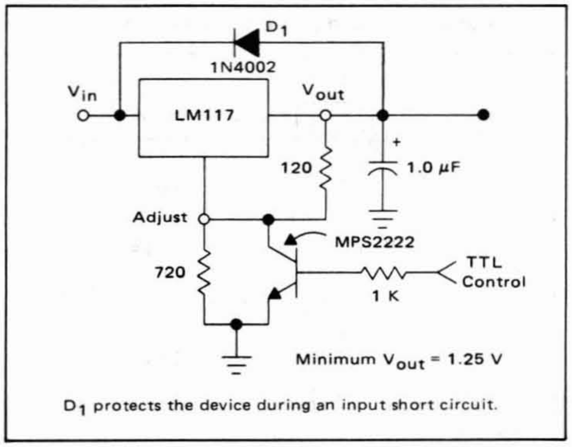
$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$

$V_O < BV_{DSS} + 1.25\text{ V} + V_{SS}$

$I_{Lmin} - I_{DSS} < I_O < 1.5\text{ A}$

As shown $0 < I_O < 1$ A

FIGURE 21 – 5 V ELECTRONIC SHUT DOWN REGULATOR


D1
1N4002
Vin
LM117
Vout
120
1.0 µF
Adjust
720
MPS2222
1 K
TTL
Control

Minimum $V_{out} = 1.25$ V

$D_1$ protects the device during an input short circuit.

FIGURE 22 – SLOW TURN-ON REGULATOR

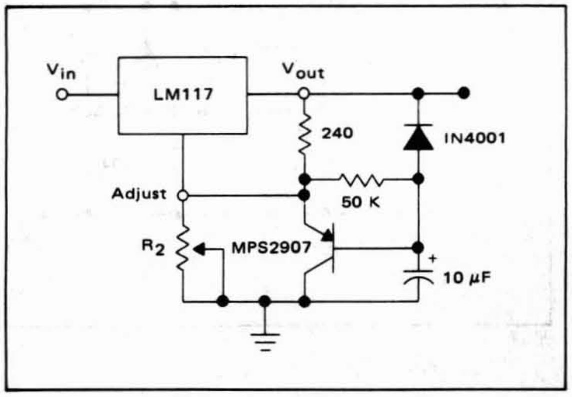
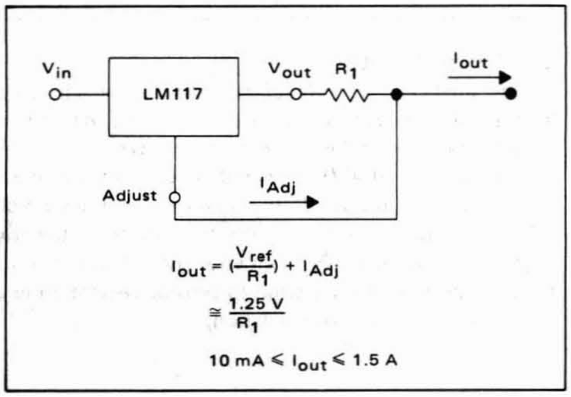

Vin
LM117
Vout
240
IN4001
Adjust
50 K
R2
MPS2907
10 µF

FIGURE 23 – CURRENT REGULATOR


Vin
LM117
Vout
R1
Iout
Adjust
IAdj

$I_{out} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj}$

$\cong \frac{1.25\text{ V}}{R_1}$

$10\text{ mA} \leq I_{out} \leq 1.5\text{ A}$

**MOTOROLA**

# LM117L
# LM217L
# LM317L

## Specifications and Applications Information

### LOW-CURRENT 3-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

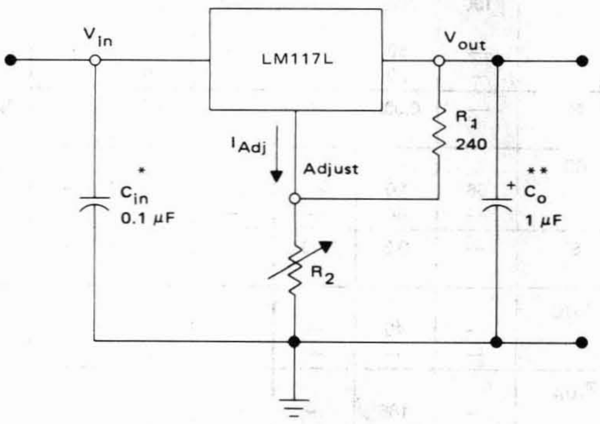
### 3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

The LM117L/217L/317L are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117L series serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117L series can be used as a precision current regulator.

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



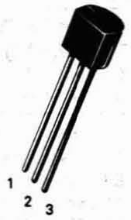
* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_o$ is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2$$

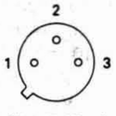
Since $I_{Adj}$ is controlled to less than 100 µA, the error associated with this term is negligible in most applications

**Z SUFFIX**
CASE 29-02
TO-226AA
(TO-92)
PLASTIC PACKAGE
(LM317 only)

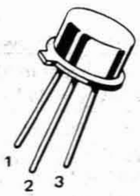


Pin 1 Adjust
Pin 2 $V_{out}$
Pin 3 $V_{in}$

**H SUFFIX**
METAL PACKAGE
CASE 79-02
TO-205AD
(TO-39)

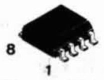


(Bottom View)



(Case is output)

Pin 1 $V_{in}$
Pin 2 Adjust
Pin 3 $V_{out}$



**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SOP-8*
(LM317L Only)

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

***Surface Mount pin-out is different than standard package pin-out for this device. Please refer to Chapter 13 for details.**

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| LM117LH | $T_J$ = −55°C to +150°C | Metal Can |
| LM217LH | $T_J$ = −25°C to +150°C | Metal Can |
| LM317LD | $T_J$ = 0°C to +125°C | SOP-8 |
| LM317LH | | Metal Can |
| LM317LZ | | Plastic |

# LM117L, LM217L, LM317L

## MAXIMUM RATINGS

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Input-Output Voltage Differential | | $V_I$-$V_O$ | 40 | Vdc |
| Power Dissipation | | $P_D$ | Internally Limited | |
| Operating Junction Temperature Range | LM117L<br>LM217L<br>LM317L | $T_J$ | -55 to +150<br>-25 to +150<br>0 to +125 | °C |
| Storage Temperature Range | | $T_{stg}$ | -65 to +150 | °C |

## ELECTRICAL CHARACTERISTICS

($V_I - V_O = 5.0$ V; $I_O = 40$ mA; $T_J = T_{low}$ to $T_{high}$ [see Note 1]; $I_{max}$ and $P_{max}$ per Note 2; unless otherwise specified.)

| Characteristic | Figure | Symbol | LM117L/217L | | | LM317L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation (Note 3)<br>$T_A = 25°C$, $3.0\ V \leq V_I - V_O \leq 40\ V$ | 1 | $Reg_{line}$ | — | 0.01 | 0.02 | — | 0.01 | 0.04 | %/V |
| Load Regulation (Note 3), $T_A = 25°C$<br>$5.0\ mA \leq I_O \leq I_{max}$ — LM117L/217L<br>$10\ mA \leq I_O \leq I_{max}$ — LM317L<br>$V_O \leq 5.0$ V<br>$V_O \geq 5.0$ V | 2 | $Reg_{load}$ | —<br>— | 5.0<br>0.1 | 15<br>0.3 | —<br>— | 5.0<br>0.1 | 25<br>0.5 | mV<br>% $V_O$ |
| Adjustment Pin Current | 3 | $I_{Adj}$ | — | 50 | 100 | — | 50 | 100 | μA |
| Adjustment Pin Current Change<br>$2.5\ V \leq V_I - V_O \leq 40\ V$, $P_D \leq P_{max}$<br>$5.0\ mA \leq I_O \leq I_{max}$ — LM117L/217L<br>$10\ mA \leq I_O \leq I_{max}$ — LM317L | 1,2 | $\Delta I_{Adj}$ | — | 0.2 | 5.0 | — | 0.2 | 5.0 | μA |
| Reference Voltage (Note 4)<br>$3.0\ V \leq V_I - V_O \leq 40\ V$, $P_D \leq P_{max}$<br>$5.0\ mA \leq I_O \leq I_{max}$ — LM117L/217L<br>$10\ mA \leq I_O \leq I_{max}$ — LM317L | 3 | $V_{ref}$ | 1.20 | 1.25 | 1.30 | 1.20 | 1.25 | 1.30 | V |
| Line Regulation (Note 3)<br>$3.0\ V \leq V_I - V_O \leq 40\ V$ | 1 | $Reg_{line}$ | — | 0.02 | 0.05 | — | 0.02 | 0.07 | %/V |
| Load Regulation (Note 3)<br>$5.0\ mA \leq I_O \leq I_{max}$ — LM117L/217L<br>$10\ mA \leq I_O \leq I_{max}$ — LM317L<br>$V_O \leq 5.0$ V<br>$V_O \geq 5.0$ V | 2 | $Reg_{load}$ | —<br>— | 20<br>0.3 | 50<br>1.0 | —<br>— | 20<br>0.3 | 70<br>1.5 | mV<br>% $V_O$ |
| Temperature Stability ($T_{low} \leq T_J \leq T_{high}$) | 3 | $T_S$ | — | 0.7 | — | — | 0.7 | — | % $V_O$ |
| Minimum Load Current to Maintain Regulation ($V_I - V_O = 40$ V) | 3 | $I_{Lmin}$ | — | 3.5 | 5.0 | — | 3.5 | 10 | mA |
| Maximum Output Current<br>$V_I - V_O \leq 20$ V, $P_D \leq P_{max}$, H Package<br>$V_I - V_O \leq 6.25$ V, $P_D \leq P_{max}$, Z Package<br>$V_I - V_O = 40$ V, $P_D \leq P_{max}$, $T_A = 25°C$<br>H Package<br>Z Package | 3 | $I_{max}$ | 100<br>100<br>—<br>— | 200<br>200<br>50<br>20 | —<br>—<br>—<br>— | 100<br>1005<br>—<br>— | 200<br>200<br>50<br>20 | —<br>—<br>—<br>— | A |
| RMS Noise, % of $V_O$<br>$T_A = 25°C$, $10\ Hz \leq f \leq 10\ kHz$ | — | N | — | 0.003 | — | — | 0.003 | — | % $V_O$ |
| Ripple Rejection (Note 5)<br>$V_O = 1.25$ V, f = 120 Hz<br>$C_{ADJ} = 10\ \mu F$ $V_O = 10.0$ V | 4 | RR | 66<br>— | 80<br>80 | —<br>— | 60<br>— | 80<br>80 | —<br>— | dB |
| Long Term Stability, $T_J = T_{high}$ (Note 6)<br>$T_A = 25°C$ for Endpoint Measurements | 3 | S | — | 0.3 | 1.0 | — | 0.3 | 1.0 | %/1.0 k Hrs. |
| Thermal Resistance Junction to Case<br>H Package (TO-39)<br>Z Package (TO-92) | — | $R_{\theta JC}$ | —<br>— | 40<br>— | —<br>— | —<br>— | 40<br>83 | —<br>— | °C/W |
| Thermal Resistance Junction to Air<br>H Package (TO-39)<br>Z Package (TO-92) | — | $R_{\theta JA}$ | —<br>— | 185<br>— | —<br>— | —<br>— | 185<br>160 | —<br>— | °C/W |

NOTES:

(1) $T_{low}$ = −55°C for LM117L $\quad T_{high}$ = +150°C for LM117L
−25°C for LM217L $\quad$ = +150°C for LM217L
0°C for LM317L $\quad$ = +125°C for LM317L

(2) $I_{max}$ = 100 mA
$P_{max}$ = 2 W for H (TO-39) Package
= 625 mW for Z (TO-92) Package

(3) Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) $C_{ADJ}$, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

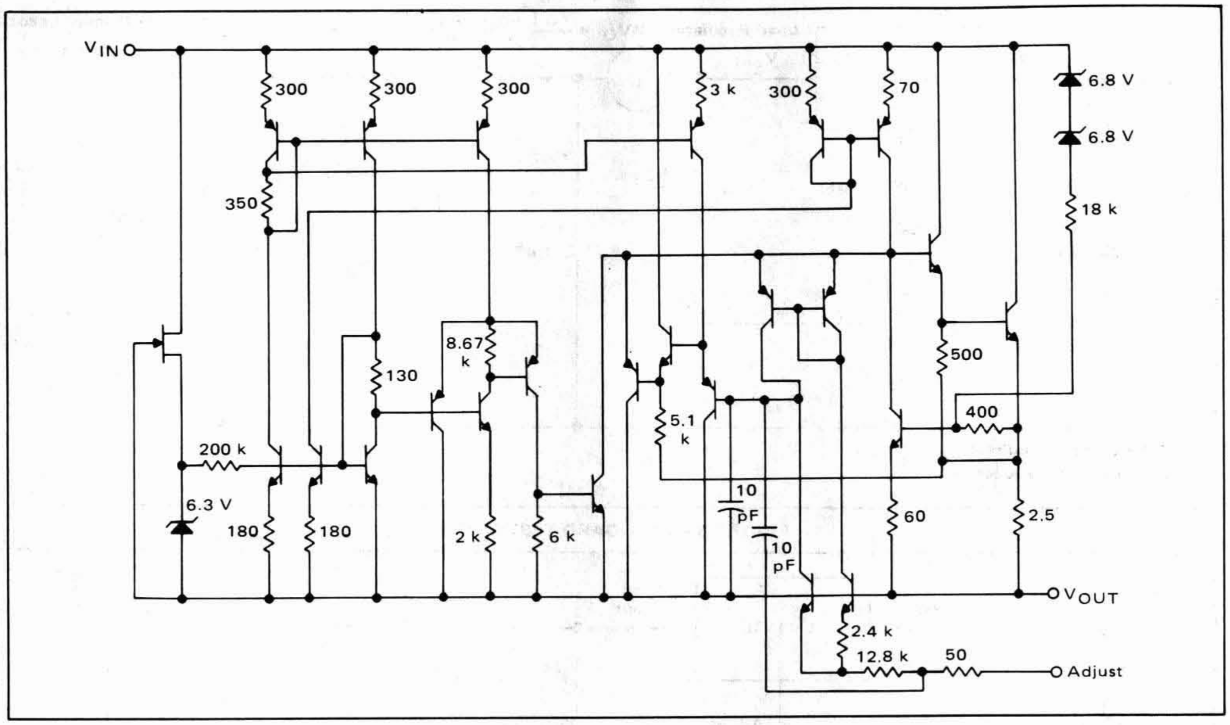
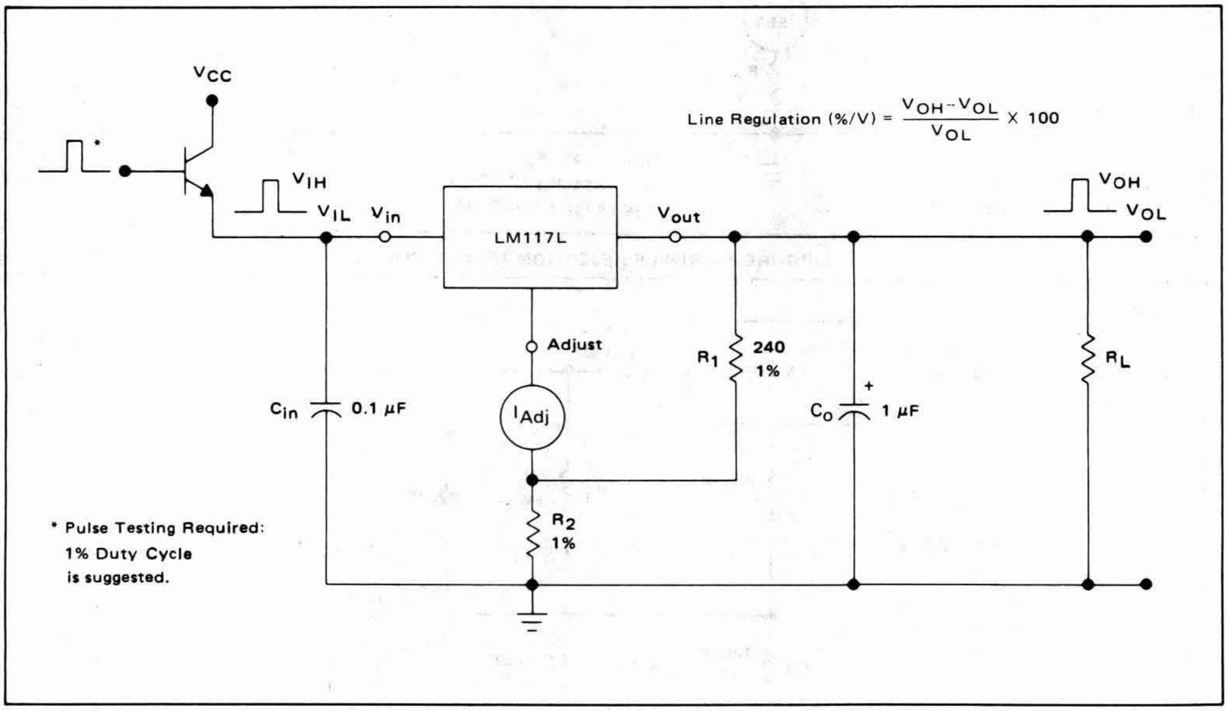

VIN
300
300
300
3 k
300
70
6.8 V
6.8 V
350
18 k
8.67 k
130
500
400
5.1 k
200 k
6.3 V
180
180
2 k
6 k
10 pF
10 pF
60
2.5
VOUT
2.4 k
12.8 k
50
Adjust

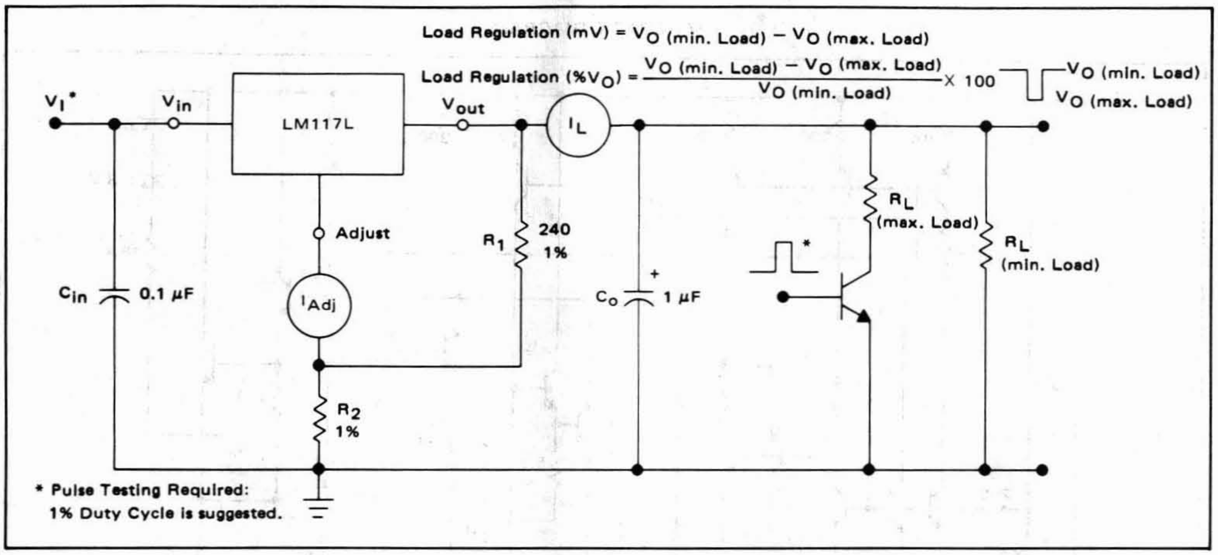
FIGURE 1 – LINE REGULATION AND $\Delta I_{Adj}$/LINE TEST CIRCUIT


VCC
*
VIH
VIL
Vin
LM117L
Vout
VOH
VOL
Adjust
IAdj
R1
240
1%
Cin
0.1 µF
Co
+
1 µF
RL
R2
1%

$$\text{Line Regulation (\%/V)} = \frac{V_{OH} - V_{OL}}{V_{OL}} \times 100$$

* Pulse Testing Required:
1% Duty Cycle
is suggested.

FIGURE 2 – LOAD REGULATION AND $\Delta I_{Adj}$/LOAD TEST CIRCUIT

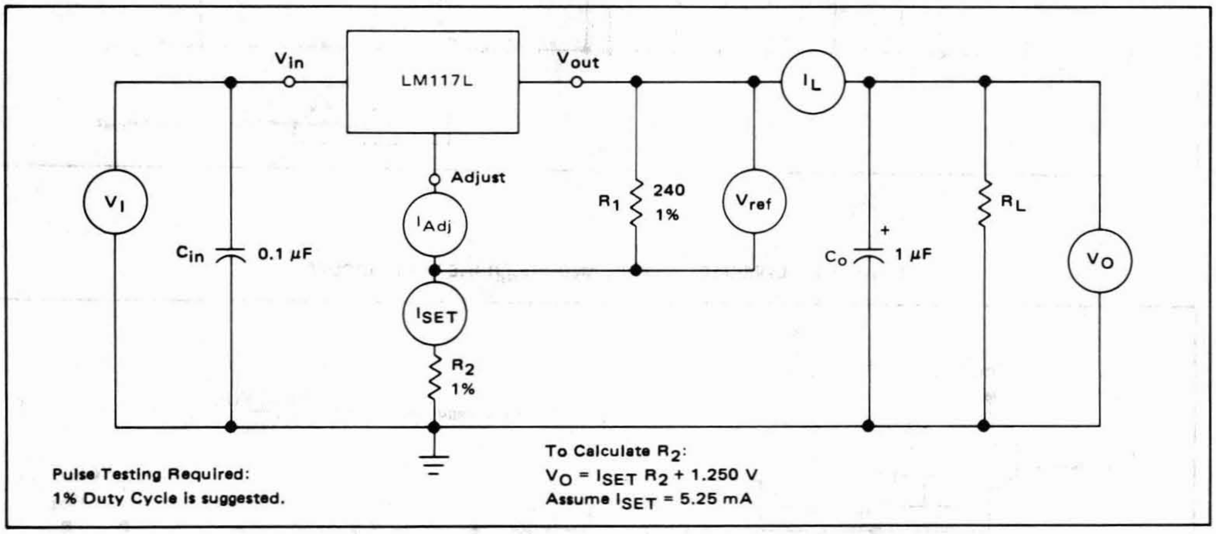

$V_I$*
$V_{in}$
LM117L
$V_{out}$
$I_L$
Adjust
$R_1$
240
1%
$C_{in}$
0.1 µF
$I_{Adj}$
$C_O$
+
1 µF
*
$R_L$
(max. Load)
$R_L$
(min. Load)
$R_2$
1%
$V_O$ (min. Load)
$V_O$ (max. Load)

Load Regulation (mV) = $V_O$ (min. Load) − $V_O$ (max. Load)

$$\text{Load Regulation } (\%V_O) = \frac{V_O \text{ (min. Load)} - V_O \text{ (max. Load)}}{V_O \text{ (min. Load)}} \times 100$$

* Pulse Testing Required:
1% Duty Cycle is suggested.

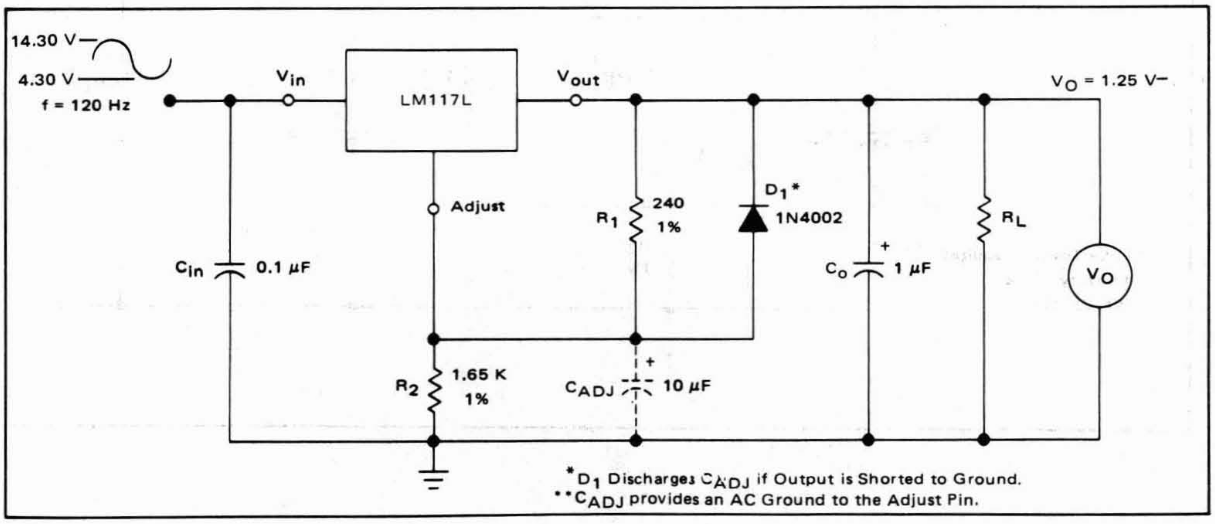
FIGURE 3 – STANDARD TEST CIRCUIT


$V_{in}$
LM117L
$V_{out}$
$I_L$
$V_I$
Adjust
$R_1$
240
1%
$V_{ref}$
$R_L$
$C_{in}$
0.1 µF
$I_{Adj}$
$C_O$
+
1 µF
$V_O$
$I_{SET}$
$R_2$
1%

Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate $R_2$:
$V_O = I_{SET} R_2 + 1.250$ V
Assume $I_{SET}$ = 5.25 mA

FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT


14.30 V
4.30 V
f = 120 Hz
$V_{in}$
LM117L
$V_{out}$
$V_O$ = 1.25 V
Adjust
$R_1$
240
1%
$D_1$*
1N4002
$R_L$
$C_{in}$
0.1 µF
$C_O$
+
1 µF
$V_O$
$R_2$
1.65 K
1%
$C_{ADJ}$
+
10 µF

*$D_1$ Discharges $C_{ADJ}$ if Output is Shorted to Ground.
**$C_{ADJ}$ provides an AC Ground to the Adjust Pin.

**FIGURE 5 — LOAD REGULATION**

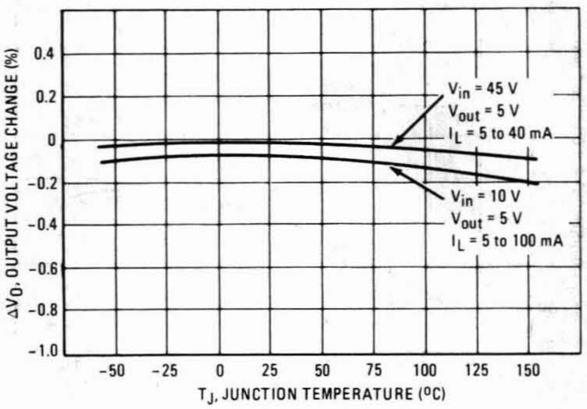


**FIGURE 6 — RIPPLE REJECTION**

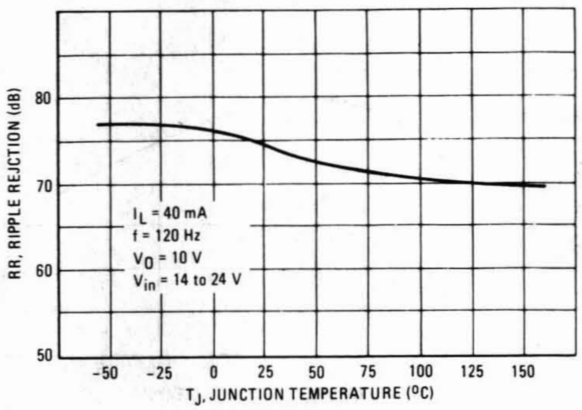


**FIGURE 7 — CURRENT LIMIT**

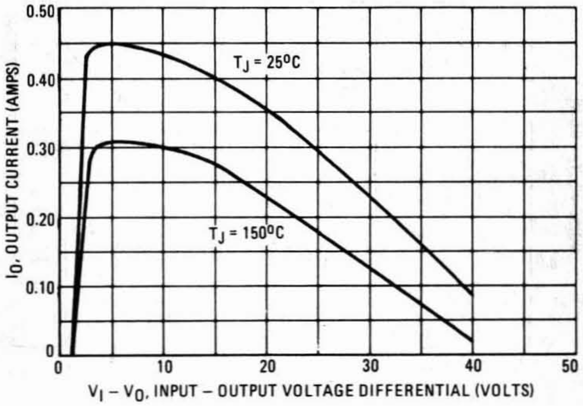


**FIGURE 8 — DROPOUT VOLTAGE**

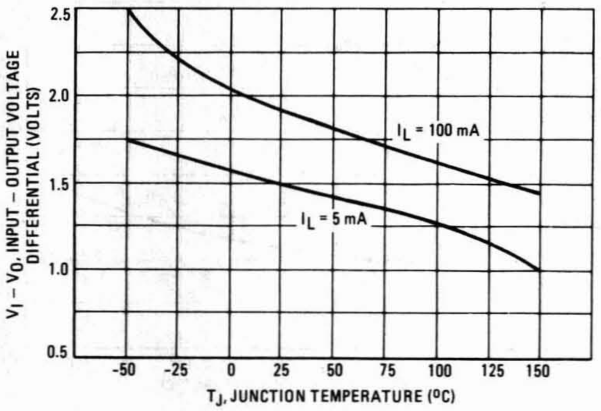


**FIGURE 9 — MINIMUM OPERATING CURRENT**

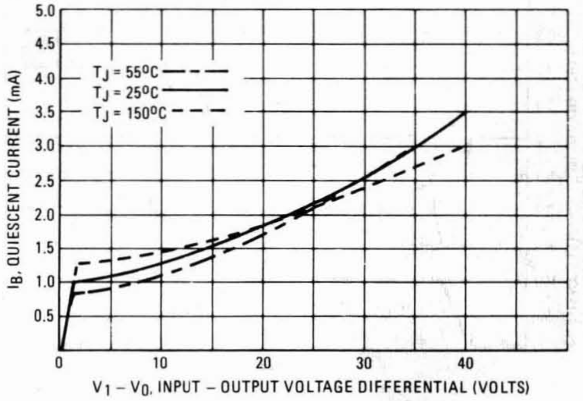


**FIGURE 10 — RIPPLE REJECTION versus FREQUENCY**

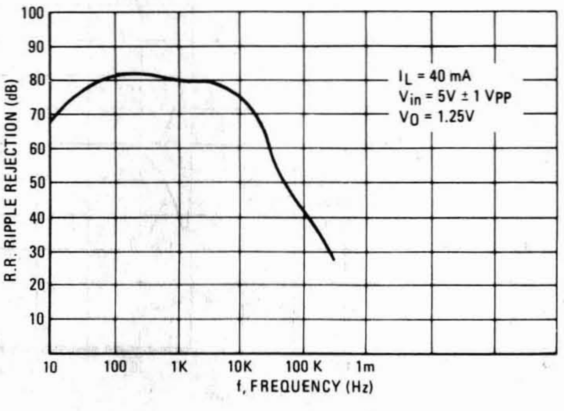


FIGURE 11 — TEMPERATURE STABILITY

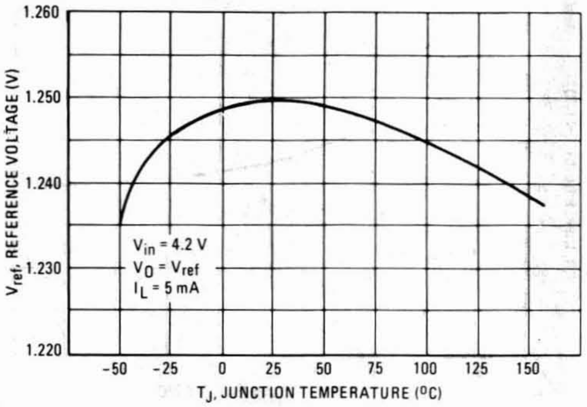


FIGURE 12 — ADJUSTMENT PIN CURRENT

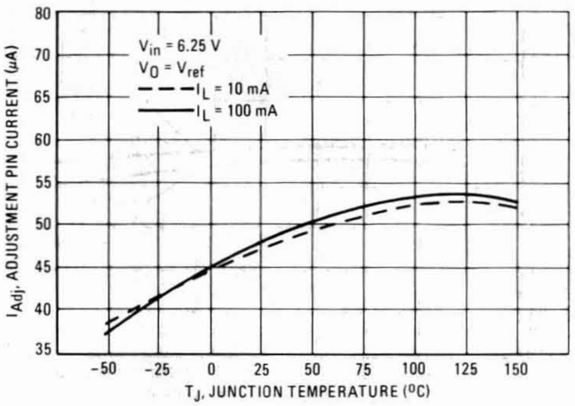


FIGURE 13 — LINE REGULATION

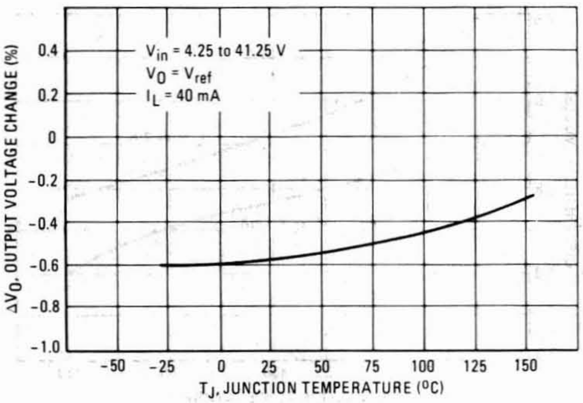


FIGURE 14 — OUTPUT NOISE

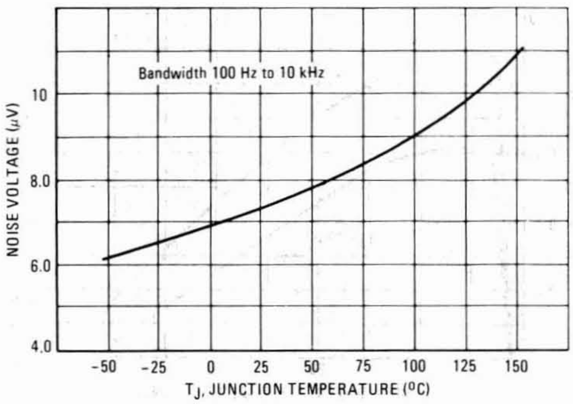


FIGURE 15 — LINE TRANSIENT RESPONSE

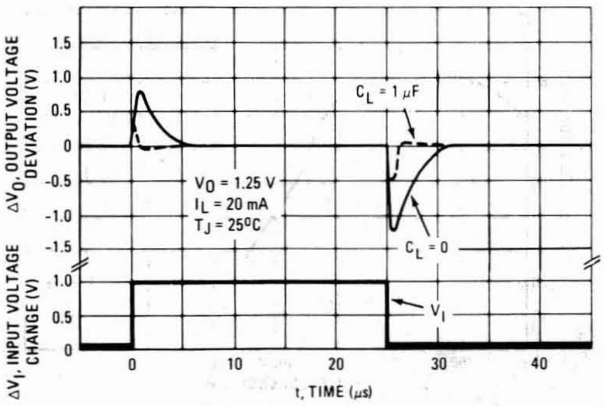
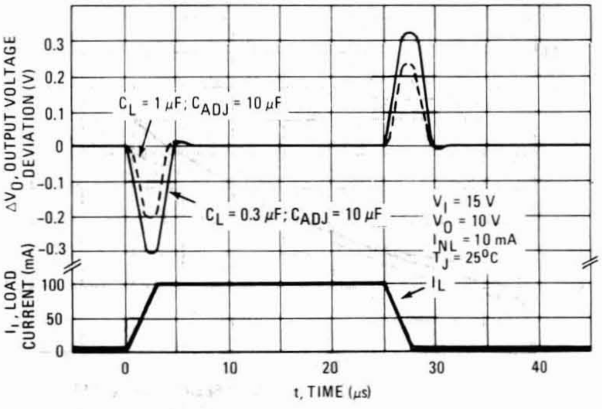


FIGURE 16 — LOAD TRANSIENT RESPONSE



## APPLICATIONS INFORMATION

### BASIC CIRCUIT OPERATION

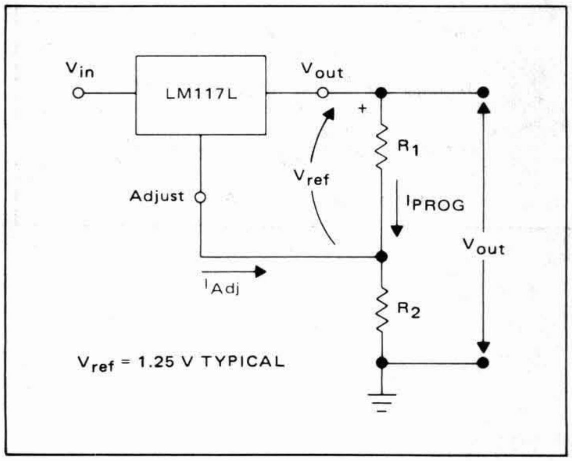
The LM117L is a 3-terminal floating regulator. In operation, the LM117L develops and maintains a nominal 1.25 volt reference ($V_{ref}$) between its output and adjustment terminals. This reference voltage is converted to a programming current ($I_{PROG}$) by R1 (see Figure 13), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\,(1 + \frac{R2}{R1}) + I_{Adj}\,R2$$

Since the current from the adjustment terminal ($I_{Adj}$) represents an error term in the equation, the LM117L was designed to control $I_{Adj}$ to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



### LOAD REGULATION

The LM117L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

### EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor ($C_{in}$) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor ($C_{ADJ}$) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance ($C_o$) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

### PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 14 shows the LM117L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_o > 10$ μF, $C_{ADJ} > 5$ μF). Diode $D_1$ prevents $C_o$ from discharging thru the I.C. during an input short circuit. Diode $D_2$ protects against capacitor $C_{ADJ}$ discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents $C_{ADJ}$ from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

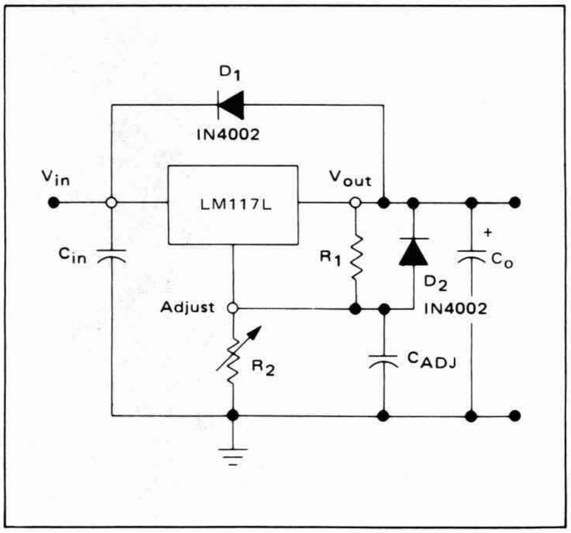
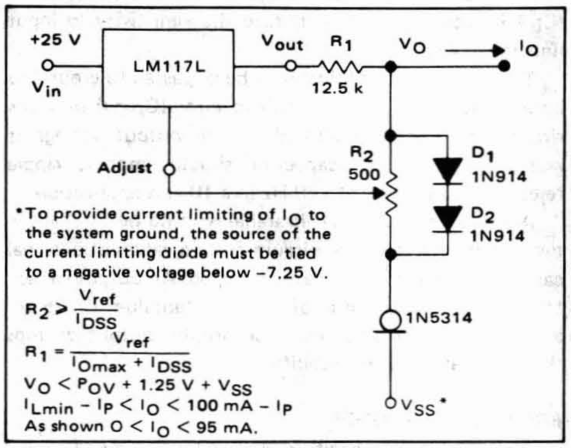


FIGURE 19 – ADJUSTABLE CURRENT LIMITER


+25 V
$V_{in}$
LM117L
$V_{out}$
$R_1$
12.5 k
$V_O$
$I_O$
Adjust
$R_2$
500
$D_1$
1N914
$D_2$
1N914
1N5314
$V_{SS}$*

*To provide current limiting of $I_O$ to the system ground, the source of the current limiting diode must be tied to a negative voltage below −7.25 V.

$R_2 \geq \frac{V_{ref}}{I_{DSS}}$

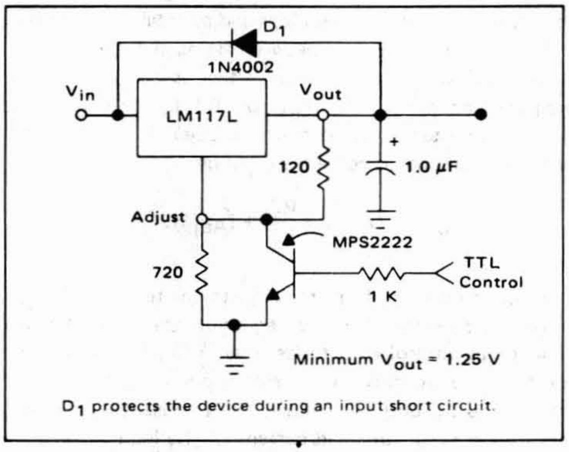
$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$

$V_O < P_{OV} + 1.25\ V + V_{SS}$

$I_{Lmin} - I_P < I_O < 100\ mA - I_P$

As shown $0 < I_O < 95\ mA$.

FIGURE 20 – 5 V ELECTRONIC SHUTDOWN REGULATOR


$D_1$
1N4002
$V_{in}$
LM117L
$V_{out}$
120
+
1.0 μF
Adjust
MPS2222
720
TTL
Control
1 K

Minimum $V_{out}$ = 1.25 V

$D_1$ protects the device during an input short circuit.

FIGURE 21 – SLOW TURN-ON REGULATOR

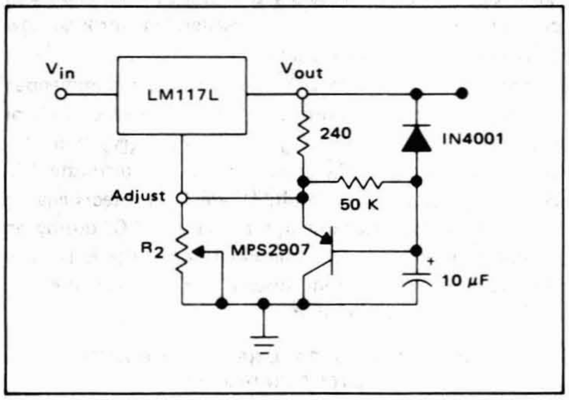
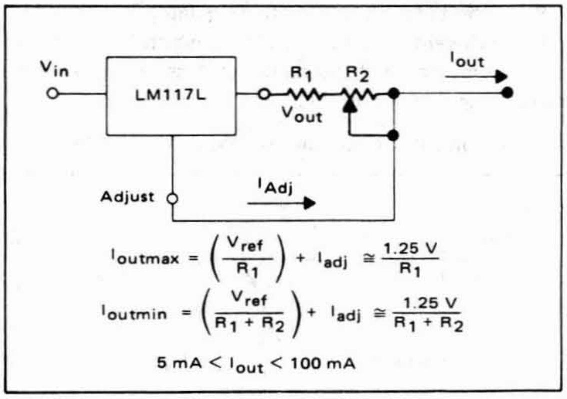

$V_{in}$
LM117L
$V_{out}$
240
IN4001
Adjust
50 K
$R_2$
MPS2907
+
10 μF

FIGURE 22 – CURRENT REGULATOR


$V_{in}$
LM117L
$R_1$
$R_2$
$V_{out}$
$I_{out}$
Adjust
$I_{Adj}$

$$I_{outmax} = \left(\frac{V_{ref}}{R_1}\right) + I_{adj} \cong \frac{1.25\ V}{R_1}$$

$$I_{outmin} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{adj} \cong \frac{1.25\ V}{R_1 + R_2}$$

$5\ mA < I_{out} < 100\ mA$

**MOTOROLA**

# LM123, LM123A
# LM223, LM223A
# LM323, LM323A

## Specifications and Applications Information

### 3 AMPERE, 5 VOLT POSITIVE VOLTAGE REGULATOR

The LM123, A/LM223, A/LM323, A are a family of monolithic integrated circuits which supply a fixed positive 5.0 volt output with a load driving capability in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. An improved series with superior electrical characteristics and a 2% output voltage tolerance is available as A-suffix (LM123A/LM223A/LM323A) device types.

These regulators are offered in a hermetic TO-3 metal power package in three operating temperature ranges. A 0°C to +125°C temperature range version is also available in a low cost TO-220 plastic power package.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series pass transistor to supply up to 15 amperes at 5.0 volts.

- Output Current in Excess of 3.0 Amperes
- Available with 2% Output Voltage Tolerance
- No external Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Thermal Regulation and Ripple Rejection Have Specified Limits

### MAXIMUM RATINGS

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Input Voltage | | $V_{in}$ | 20 | Vdc |
| Power Dissipation | | $P_D$ | Internally Limited | |
| Operating Junction Temperature Range | LM123, A<br>LM223, A<br>LM323, A | $T_J$ | -55 to +150<br>-25 to +150<br>0 to +125 | °C |
| Storage Temperature Range | | $T_{stg}$ | -65 to +150 | °C |
| Lead Temperature (Soldering, 10 s) | | $T_{solder}$ | 300 | °C |

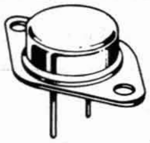
### ORDERING INFORMATION

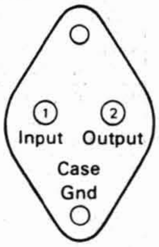
| Device | Output Voltage Tolerance | Junction Temperature Range | Package |
|---|---|---|---|
| LM123K | 6% | -55 to +150°C | Metal Power |
| LM123AK | 2% | | |
| LM223K | 6% | -25 to +150°C | |
| LM223AK | 2% | | |
| LM323K | 4% | 0 to +125°C | |
| LM323AK | 2% | | |
| LM323T | 4% | | Plastic Power |
| LM323AT | 2% | | |

**3-AMPERE, 5 VOLT POSITIVE VOLTAGE REGULATOR**

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

**K SUFFIX**
**METAL PACKAGE**
**CASE 1-03**
**TO-204AA**
**(TO-3)**

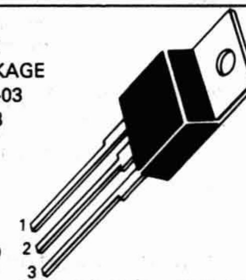




(Bottom View)

Pin 1. INPUT
2. OUTPUT
CASE GROUND

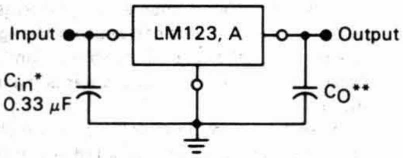
**T SUFFIX**
**PLASTIC PACKAGE**
**CASE 221A-03**
**TO-220AB**



Pin 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2)

**STANDARD APPLICATION**



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.5 V above the output voltage even during the low point on the input ripple voltage.

* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

** = $C_O$ is not needed for stability; however, it does improve transient response.

**ELECTRICAL CHARACTERISTICS** ($T_J = T_{low}$ to $T_{high}$ [see Note 1] unless otherwise specified.)

| Characteristic | Symbol | LM123A/LM223A/LM323A | | | LM123/LM223 | | | LM323 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($V_{in}$ = 7.5 V, 0 ≤ $I_{out}$ ≤ 3.0 A, $T_J$ = 25°C) | $V_O$ | 4.9 | 5.0 | 5.1 | 4.7 | 5.0 | 5.3 | 4.8 | 5.0 | 5.2 | V |
| Output Voltage (7.5 V ≤ $V_{in}$ ≤ 15 V, 0 ≤ $I_{out}$ ≤ 3.0 A, P ≤ $P_{max}$ [Note 2]) | $V_O$ | 4.8 | 5.0 | 5.2 | 4.6 | 5.0 | 5.4 | 4.75 | 5.0 | 5.25 | V |
| Line Regulation (7.5 V ≤ $V_{in}$ ≤ 15 V, $T_J$ = 25°C) (Note 3) | $Reg_{line}$ | — | 1.0 | 15 | — | 1.0 | 25 | — | 1.0 | 25 | mV |
| Load Regulation ($V_{in}$ = 7.5 V, 0 ≤ $I_{out}$ ≤ 3.0 A, $T_J$ = 25°C) (Note 3) | $Reg_{load}$ | — | 10 | 50 | — | 10 | 100 | — | 10 | 100 | mV |
| Thermal Regulation (Pulse = 10 ms, P = 20 W, $T_A$ = 25°C) | $Reg_{therm}$ | — | 0.001 | 0.01 | — | 0.002 | 0.03 | — | 0.002 | 0.03 | %$V_O$/W |
| Quiescent Current (7.5 V ≤ $V_{in}$ ≤ 15 V, 0 ≤ $I_{out}$ ≤ 3.0 A) | $I_B$ | — | 3.5 | 10 | — | 3.5 | 20 | — | 3.5 | 20 | mA |
| Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, $T_J$ = 25°C) | $V_N$ | — | 40 | — | — | 40 | — | — | 40 | — | µ$V_{rms}$ |
| Ripple Rejection (8.0 V ≤ $V_{in}$ ≤ 18 V, $I_{out}$ = 2.0 A, f = 120 Hz, $T_J$ = 25°C) | RR | 66 | 75 | — | 62 | 75 | — | 62 | 75 | — | dB |
| Short Circuit Current Limit<br>($V_{in}$ = 15 V, $T_J$ = 25°C)<br>($V_{in}$ = 7.5 V, $T_J$ = 25°C) | $I_{SC}$ | <br>—<br>— | <br>4.5<br>5.5 | <br>—<br>— | <br>—<br>— | <br>4.5<br>5.5 | <br>—<br>— | <br>—<br>— | <br>4.5<br>5.5 | <br>—<br>— | A |
| Long Term Stability | S | — | — | 35 | — | — | 35 | — | — | 35 | mV |
| Thermal Resistance Junction to Case (Note 4) | $R_{\theta JC}$ | — | 2.0 | — | — | 2.0 | — | — | 2.0 | — | °C/W |

Note 1. $T_{low}$ = −55°C for LM123, A $T_{high}$ = +150°C for LM123, A
= −25°C for LM223, A = +150°C for LM223, A
= 0°C for LM323, A = +125°C for LM323, A

Note 2. Although power dissipation is internally limited, specifications apply only for P ≤ $P_{max}$
$P_{max}$ = 30 W for K (TO-3) package
$P_{max}$ = 25 W for T (TO-220) package

Note 3. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1.0 ms and a duty cycle ≤ 5%.

Note 4. Without a heat sink, the thermal resistance ($R_{\theta JA}$) is 35°C/W for the TO-3, and 65°C/W for the TO-220 packages. With a heat sink, the effective thermal resistance can approach the specified values of 2.0 °C/W, depending on the efficiency of the heat sink.

## VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 µs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM123A to a 20 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical LM123A to a 20 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

SCHEMATIC DIAGRAM

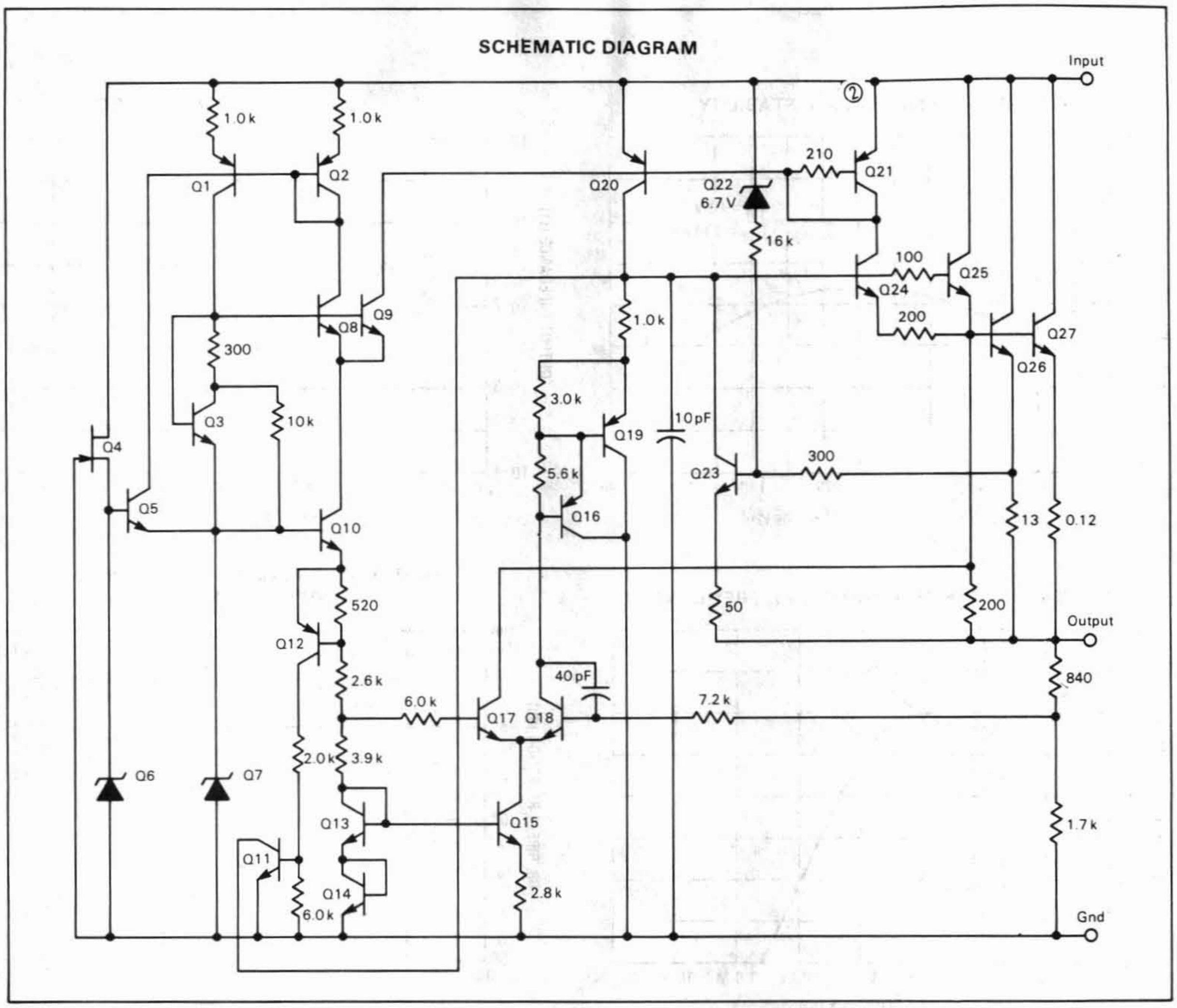
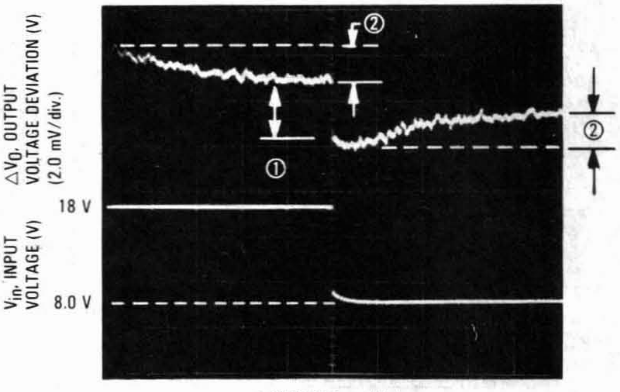
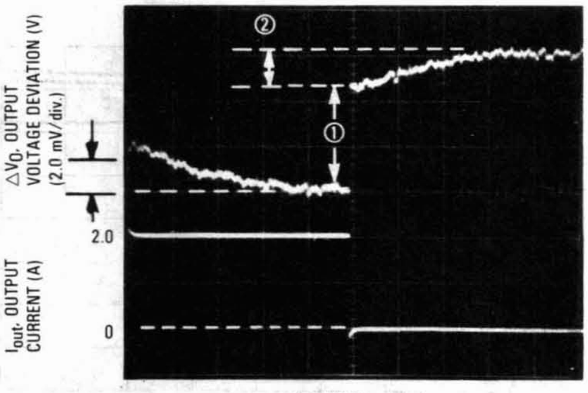

Input
②
1.0 k
1.0 k
Q1
Q2
Q20
210
Q21
Q22
6.7 V
16 k
100
Q25
Q24
200
Q27
Q26
Q9
Q8
1.0 k
300
Q3
10 k
3.0 k
Q19
10 pF
Q4
5.6 k
300
Q23
Q5
Q16
13
0.12
Q10
520
50
200
Output
Q12
2.6 k
40 pF
840
6.0 k
Q17
Q18
7.2 k
2.0 k
3.9 k
Q6
Q7
Q13
Q15
1.7 k
Q11
Q14
2.8 k
6.0 k
Gnd

FIGURE 1 — LINE AND THERMAL REGULATION



LM123A
$V_O$ = 5.0 V
$V_{in}$ = 8.0 V → 18 V → 8.0 V ① = $Reg_{line}$ = 2.4 mV
$I_{out}$ = 2.0 A ② = $Reg_{therm}$ = 0.0015%$V_O$/W

FIGURE 2 — LOAD AND THERMAL REGULATION



LM123A
$V_O$ = 5.0 V
$V_{in}$ = 15 ① = $Reg_{load}$ = 4.4 mV
$I_{out}$ = 0 A → 2.0 A → 0 A ② = $Reg_{therm}$ = 0.0015%$V_O$/W

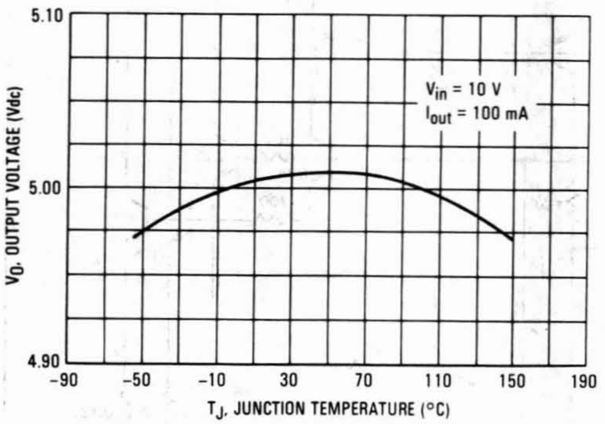


FIGURE 3 — TEMPERATURE STABILITY

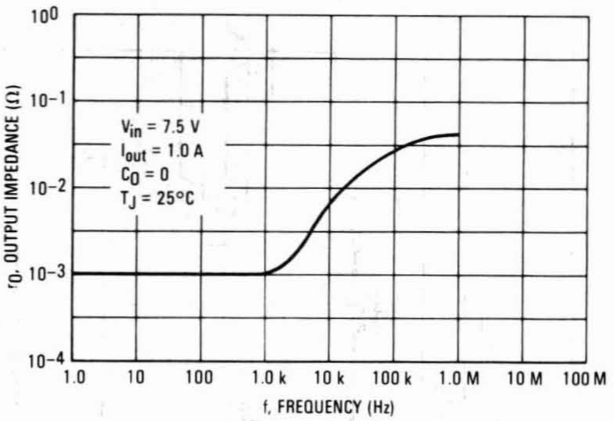


FIGURE 4 — OUTPUT IMPEDANCE

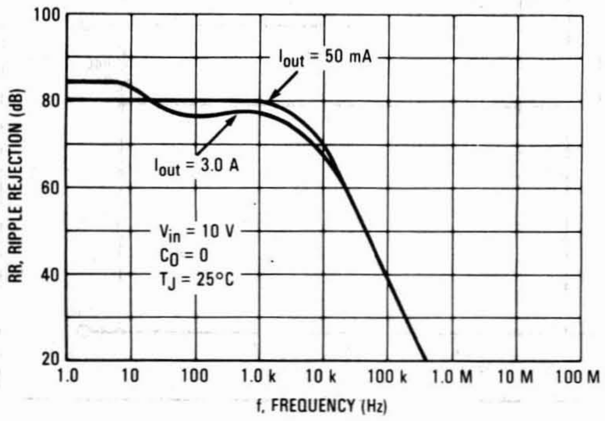


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

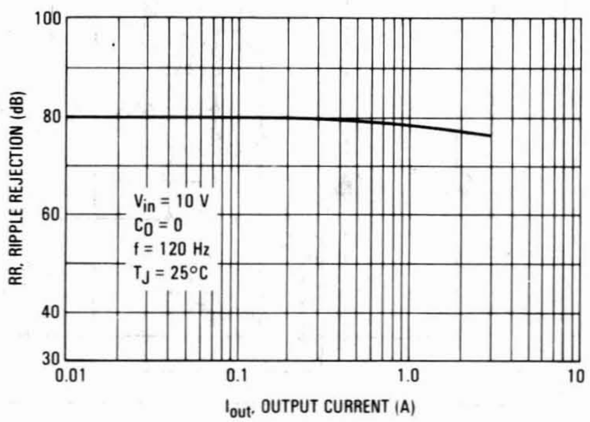


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

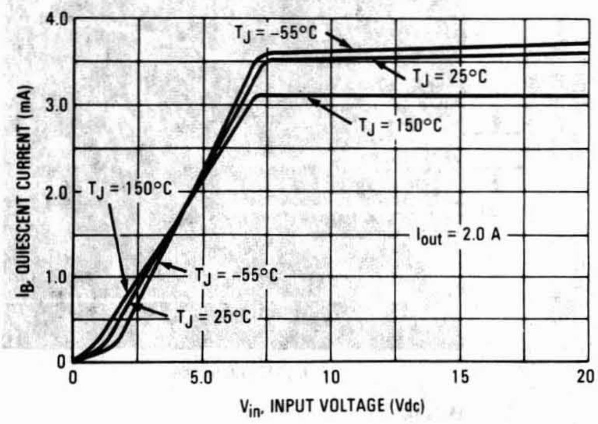


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

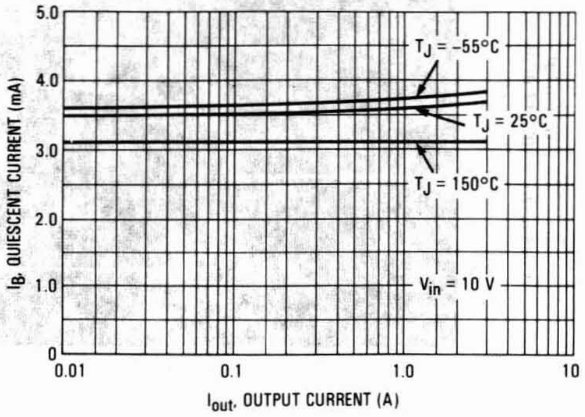


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT

FIGURE 9 — DROPOUT VOLTAGE

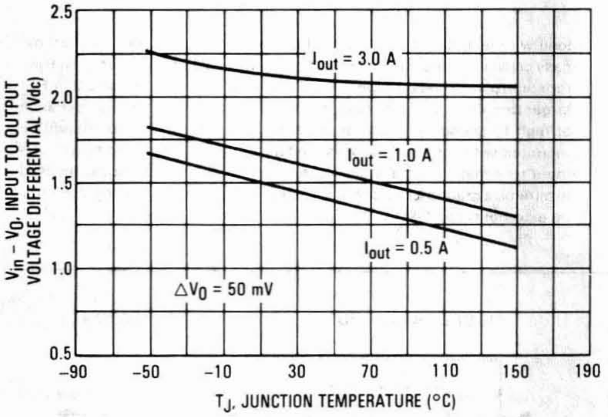


FIGURE 10 — SHORT CIRCUIT CURRENT

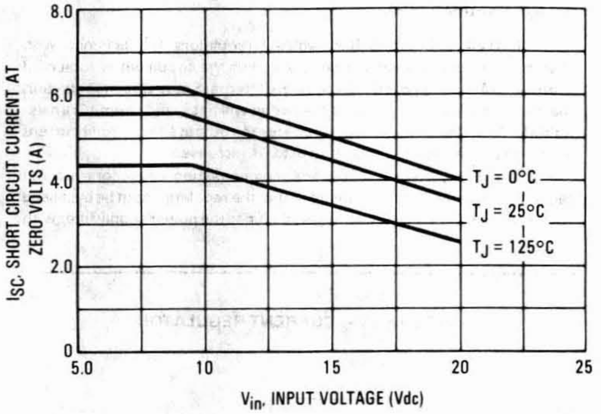


FIGURE 11 — LINE TRANSIENT RESPONSE

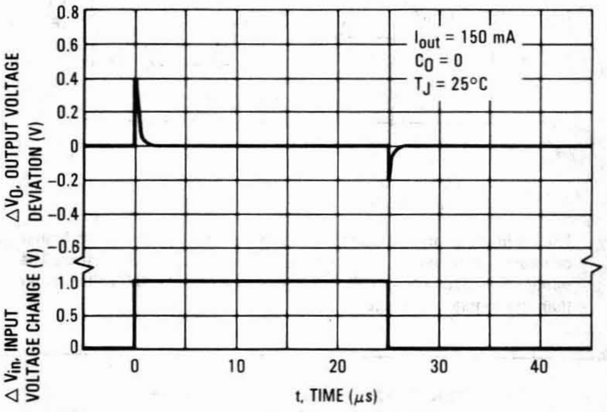


FIGURE 12 — LOAD TRANSIENT RESPONSE

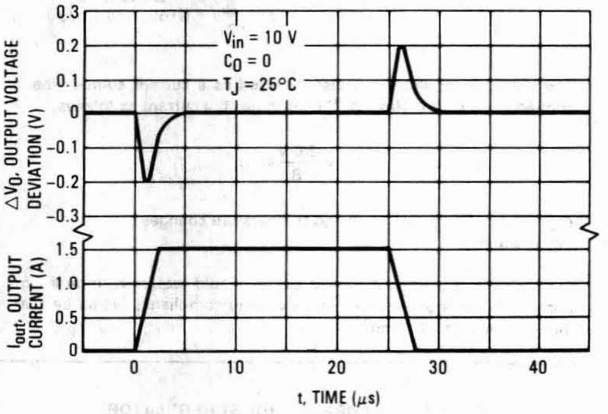


FIGURE 13 — MAXIMUM AVERAGE POWER DISSIPATION FOR LM123K and LM223K

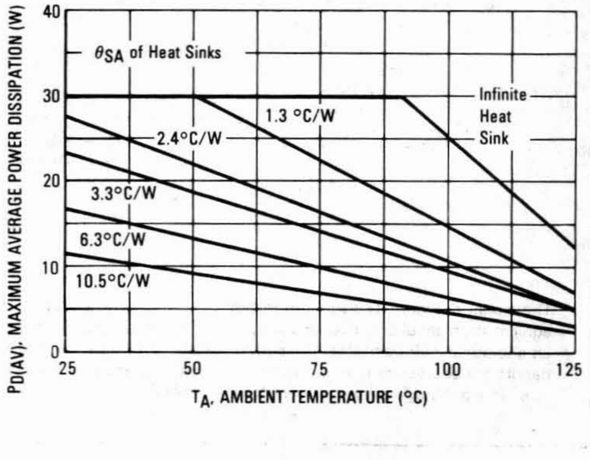
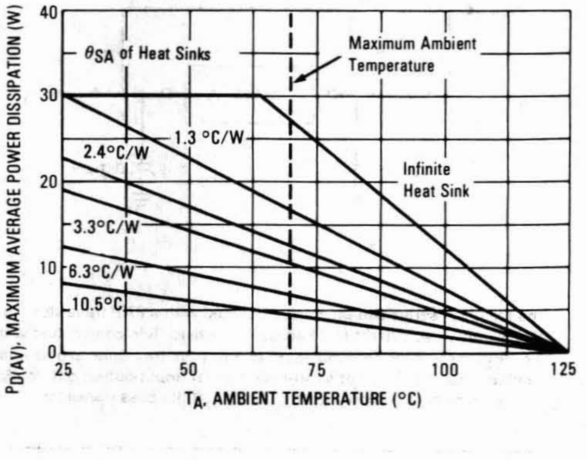


FIGURE 14 — MAXIMUM AVERAGE POWER DISSIPATION FOR LM323K



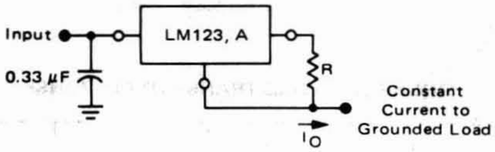
## APPLICATIONS INFORMATION

### Design Considerations

The LM123,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



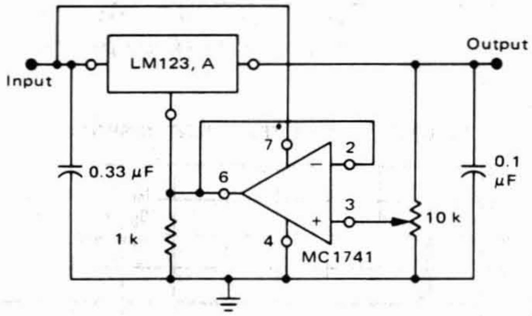
**The LM123,A regulator can also be used as a current source when connected as above. Resistor R determines the current as follows:**

$$I_O = \frac{5.0\ V}{R} + I_B$$

**$\Delta I_B \cong 0.7$ mA over line, load and temperature changes**
**$I_B \cong 3.5$ mA**

**For example, a 2-ampere current source would require R to be a 2.5 ohm, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 volts.**

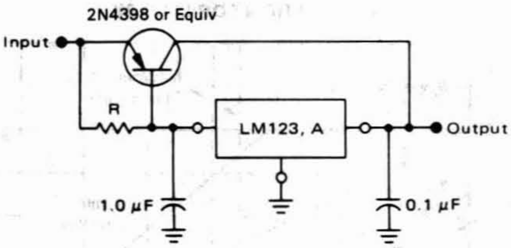
FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



$V_O$, 8.0 V to 20 V
$V_{in} - V_O \geqslant 2.5$ V

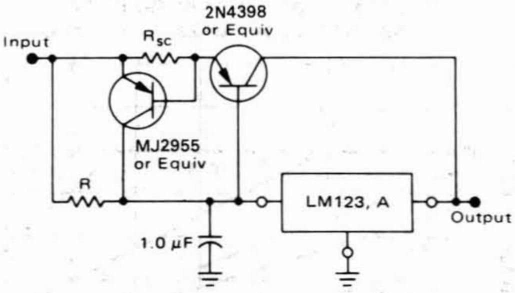
**The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.**

FIGURE 17 — CURRENT BOOST REGULATOR



**The LM123,A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the $V_{BE}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the $V_{BE}$ of the pass transistor.**

FIGURE 18 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



**The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, $R_{SC}$, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.**

# LM137
# LM237
# LM337

## Specifications and Applications Information

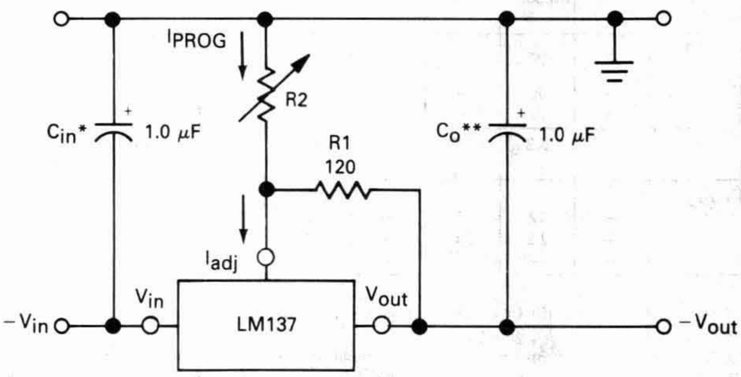
### 3-TERMINAL ADJUSTABLE OUTPUT NEGATIVE VOLTAGE REGULATOR

The LM137/237/337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of −1.2 V to −37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM137 series serve a wide variety of applications including local, on-card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM137 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in TO-3 and TO-220 Packages
- Output Current in Excess of 0.5 Ampere in TO-39 Package
- Output Adjustable Between −1.2 V and −37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting, Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

### STANDARD APPLICATION



*$C_{in}$ is required if regulator is located more than 4 inches from power supply filter. A 1 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

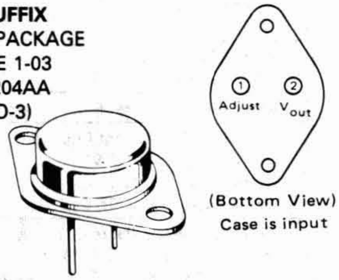
**$C_O$ is necessary for stability. A 1 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

$$V_{out} = -1.25\ V\left(1 + \frac{R2}{R1}\right)$$

### 3-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

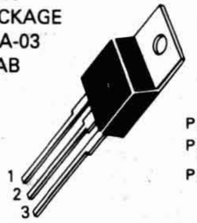
**K SUFFIX**
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)



(Bottom View)
Case is input

Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

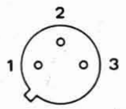
**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220AB



Pin 1 Adjust
Pin 2 $V_{in}$
Pin 3 $V_{out}$

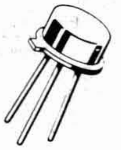
Heatsink surface connected to Pin 2

**H SUFFIX**
METAL PACKAGE
CASE 79-02
TO-205AD
(TO-39)



(Bottom View)

(Case is input)



Pin 1 Adjust
Pin 2 Output
Pin 3 Input

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| LM137H | $T_J$ = −55°C to +150°C | Metal Can |
| LM137K | $T_J$ = −55°C to +150°C | Metal Power |
| LM237H | $T_J$ = −25°C to +150°C | Metal Can |
| LM237K | $T_J$ = −25°C to +150°C | Metal Power |
| LM337H | $T_J$ = 0°C to +125°C | Metal Can |
| LM337K | $T_J$ = 0°C to +125°C | Metal Power |
| LM337T | $T_J$ = 0°C to +125°C | Plastic Power |

## MAXIMUM RATINGS

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Input-Output Voltage Differential | | $V_I$-$V_O$ | 40 | Vdc |
| Power Dissipation | | $P_D$ | Internally Limited | |
| Operating Junction Temperature Range | LM137<br>LM237<br>LM337 | $T_J$ | -55 to +150<br>-25 to +150<br>0 to +125 | °C |
| Storage Temperature Range | | $T_{stg}$ | -65 to +150 | °C |

## ELECTRICAL CHARACTERISTICS

($|V_I - V_O| = 5$ V, $I_O = 0.5$ A for K and T packages; $I_O = 0.1$ A for H package; $T_J = T_{low}$ to $T_{high}$ [see Note 1], $I_{max}$ and $P_{max}$ per Note 2, unless otherwise specified.)

| Characteristic | Figure | Symbol | LM137/237 | | | LM337 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Line Regulation (Note 3)<br>$T_A = 25°C$, $3.0 \text{ V} \leq \lvert V_I\text{-}V_O\rvert \leq 40$ V | 1 | $Reg_{line}$ | — | 0.01 | 0.02 | — | 0.01 | 0.04 | %/V |
| Load Regulation (Note 3)<br>$T_A = 25°C$, $10 \text{ mA} \leq I_O \leq I_{max}$<br>$\lvert V_O\rvert \leq 5.0$ V<br>$\lvert V_O\rvert \geq 5.0$ V | 2 | $Reg_{load}$ | <br><br>—<br>— | <br><br>15<br>0.3 | <br><br>25<br>0.5 | <br><br>—<br>— | <br><br>15<br>0.3 | <br><br>50<br>1.0 | <br><br>mV<br>% $V_O$ |
| Thermal Regulation<br>10 mS Pulse, $T_A = 25°C$ | — | $Reg_{therm}$ | — | 0.002 | 0.02 | — | 0.003 | 0.04 | % $V_O$/W |
| Adjustment Pin Current | 3 | $I_{Adj}$ | — | 65 | 100 | — | 65 | 100 | μA |
| Adjustment Pin Current Change<br>$2.5 \text{ V} \leq \lvert V_I\text{-}V_O\rvert \leq 40$ V<br>$10 \text{ mA} \leq I_L \leq I_{max}$,<br>$P_D \leq P_{max}$, $T_A = 25°C$ | 1,2 | $\Delta I_{Adj}$ | — | 2.0 | 5.0 | — | 2.0 | 5.0 | μA |
| Reference Voltage (Note 4) $T_A = +25°C$<br>$3.0 \text{ V} \leq \lvert V_I\text{-}V_O\rvert \leq 40$ V, $10 \text{ mA} \leq I_O \leq$ $I_{max}$, $P_D \leq P_{max}$, $T_J = T_{low}$ to $T_{high}$ | 3 | $V_{ref}$ | −1.225<br>−1.20 | −1.250<br>−1.25 | −1.275<br>−1.30 | −1.213<br>−1.20 | −1.250<br>−1.25 | −1.287<br>−1.30 | V |
| Line Regulation (Note 3)<br>$3.0 \text{ V} \leq \lvert V_I\text{-}V_O\rvert \leq 40$ V | 1 | $Reg_{line}$ | — | 0.02 | 0.05 | — | 0.02 | 0.07 | %/V |
| Load Regulation (Note 3)<br>$10 \text{ mA} \leq I_O \leq I_{max}$<br>$\lvert V_O\rvert \leq 5.0$ V<br>$\lvert V_O\rvert \geq 5.0$ V | 2 | $Reg_{load}$ | <br><br>—<br>— | <br><br>20<br>0.3 | <br><br>50<br>1.0 | <br><br>—<br>— | <br><br>20<br>0.3 | <br><br>70<br>1.5 | <br><br>mV<br>% $V_O$ |
| Temperature Stability ($T_{low} \leq T_J \leq T_{high}$) | 3 | $T_S$ | — | 0.6 | — | — | 0.6 | — | % $V_O$ |
| Minimum Load Current to<br>Maintain Regulation ($\lvert V_I\text{-}V_O\rvert \leq 10$ V)<br>($\lvert V_I\text{-}V_O\rvert \leq 40$ V) | 3 | $I_{Lmin}$ | <br>—<br>— | <br>1.2<br>2.5 | <br>3.0<br>5.0 | <br>—<br>— | <br>1.5<br>2.5 | <br>6.0<br>10 | mA |
| Maximum Output Current<br>$\lvert V_I\text{-}V_O\rvert \leq 15$ V, $P_D \leq P_{max}$<br>K and T Packages<br>H Package<br>$\lvert V_I\text{-}V_O\rvert = 40$ V, $P_D \leq P_{max}$, $T_J = 25°C$<br>K and T Packages<br>H Package | 3 | $I_{max}$ | <br><br>1.5<br>0.5<br><br>0.24<br>0.15 | <br><br>2.2<br>0.8<br><br>0.4<br>0.20 | <br><br>—<br>—<br><br>—<br>— | <br><br>1.5<br>0.5<br><br>0.15<br>0.10 | <br><br>2.2<br>0.8<br><br>0.4<br>0.20 | <br><br>—<br>—<br><br>—<br>— | A |
| RMS Noise, % of $V_O$<br>$T_A = 25°C$, $10 \text{ Hz} \leq f \leq 10$ kHz | — | N | — | 0.003 | — | — | 0.003 | — | % $V_O$ |
| Ripple Rejection, $V_O = -10$ V, f = 120 Hz<br>(Note 5)<br>Without $C_{Adj}$<br>$C_{Adj} = 10$ μF | 4 | RR | <br><br>—<br>66 | <br><br>60<br>77 | <br><br>—<br>— | <br><br>—<br>66 | <br><br>60<br>77 | <br><br>—<br>— | dB |
| Long-Term Stability, $T_J = T_{high}$ (Note 6)<br>$T_A = 25°C$ for Endpoint Measurements | 3 | S | — | 0.3 | 1.0 | — | 0.3 | 1.0 | %/1.0 k Hrs. |
| Thermal Resistance Junction to Case<br>H Package (TO-39)<br>K Package (TO-3)<br>T Package (TO-220) | — | $R_{\theta JC}$ | <br>—<br>—<br>— | <br>12<br>2.3<br>— | <br>15<br>3.0<br>— | <br>—<br>—<br>— | <br>12<br>2.3<br>4.0 | <br>15<br>3.0<br>— | °C/W |

NOTES:

(1) $T_{low}$ = -55°C for LM137 $T_{high}$ = +150°C for LM137
= -25°C for LM237 = +150°C for LM237
= 0°C for LM337 = +125°C for LM337

(2) $I_{max}$ = 1.5 A for K (TO-3) and T (TO-220 Packages
= 0.5 A for H (TO-39) Package
$P_{max}$ = 20 W for K (TO-3) and T (TO-220) Packages
= 2 W for H (TO-39) Package

(3) Load and line regulation are specified at a constant junction temperature. Pulse testing with a low duty cycle is used. Change in $V_O$ because of heating effects is covered under the Thermal Regulation specification.

(4) Selected devices with tightened tolerance reference voltage available.

(5) $C_{adj}$, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

(7) Power dissipation within an I.C. voltage regulator produces a temperature gradient on the die, affecting individual I.C. components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

## SCHEMATIC DIAGRAM

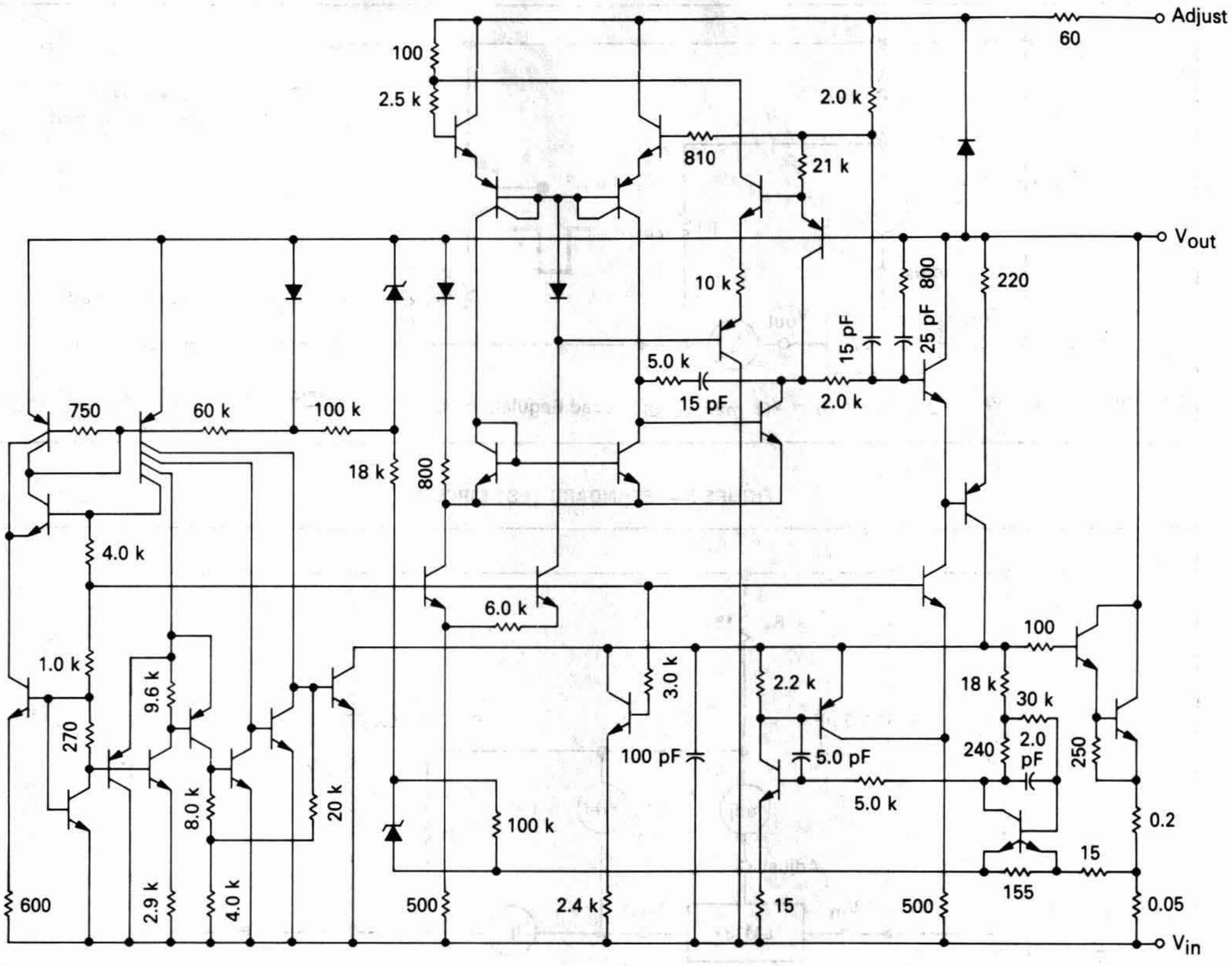
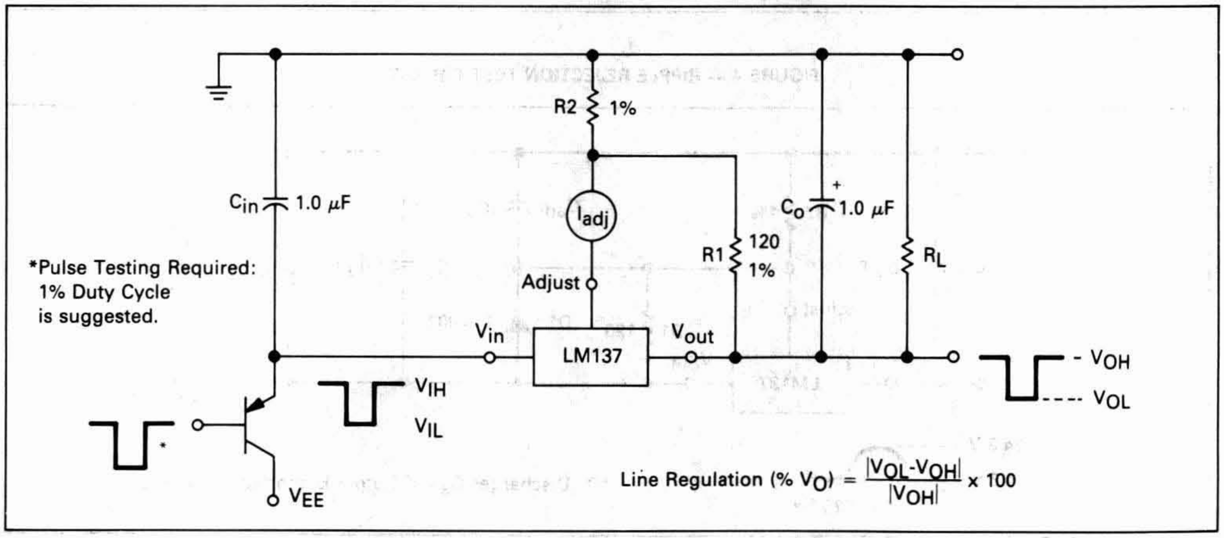

Adjust
60
100
2.5 k
2.0 k
810
21 k
Vout
10 k
220
800
25 pF
15 pF
5.0 k
15 pF
2.0 k
750
60 k
100 k
18 k
800
4.0 k
6.0 k
100
1.0 k
9.6 k
270
3.0 k
2.2 k
18 k
30 k
100 pF
5.0 pF
240
2.0 pF
250
8.0 k
20 k
5.0 k
100 k
0.2
15
155
600
2.9 k
4.0 k
500
2.4 k
15
500
0.05
Vin

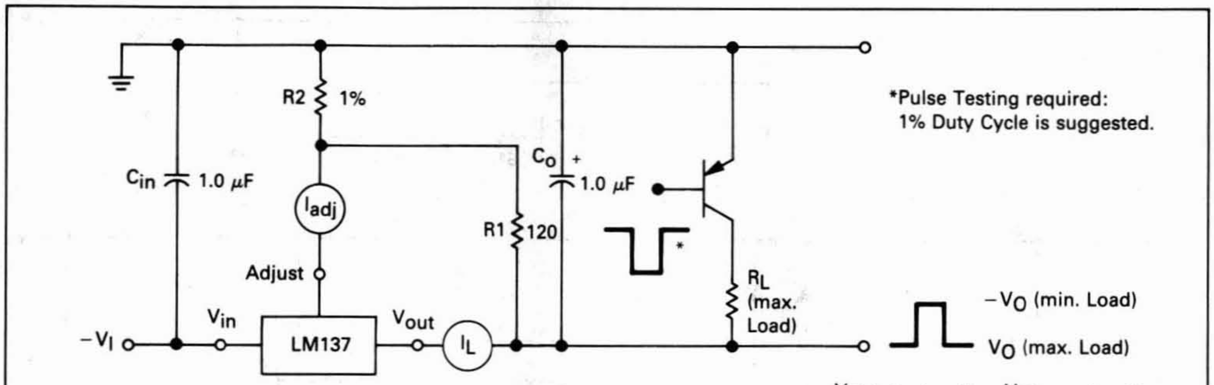
FIGURE 1 — LINE REGULATION AND $\Delta I_{Adj}$/LINE TEST CIRCUIT


R2
1%
$C_{in}$
1.0 μF
$I_{adj}$
Adjust
R1
120
1%
$C_O$
+
1.0 μF
$R_L$
$V_{in}$
LM137
$V_{out}$
$V_{IH}$
$V_{IL}$
*
$V_{EE}$
$V_{OH}$
$V_{OL}$

*Pulse Testing Required:
1% Duty Cycle
is suggested.

$$\text{Line Regulation } (\%\ V_O) = \frac{|V_{OL}-V_{OH}|}{|V_{OH}|} \times 100$$

FIGURE 2 — LOAD REGULATION AND $\Delta I_{Adj}$/LOAD TEST CIRCUIT

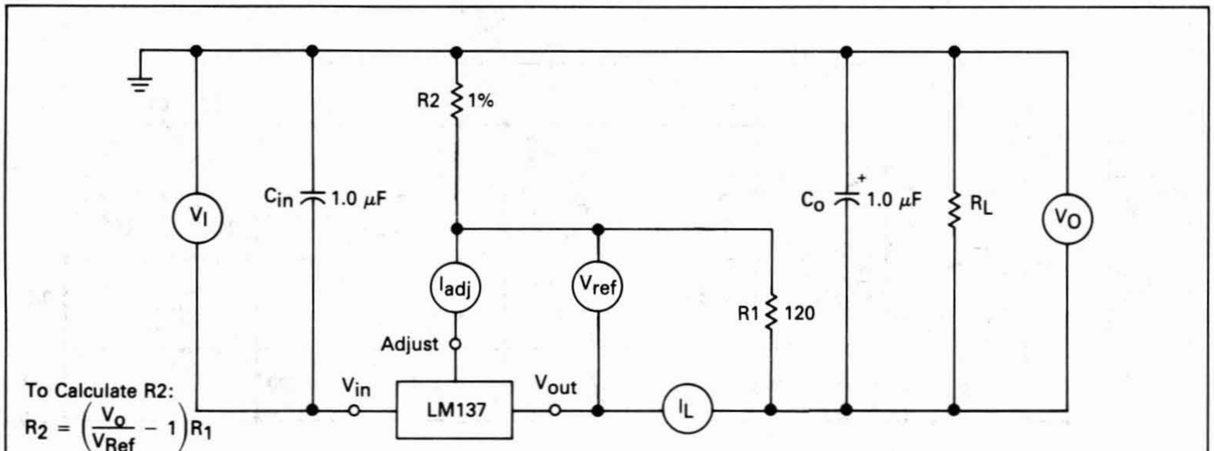

R2 1%
$C_{in}$ 1.0 μF
$I_{adj}$
Adjust
$C_O$ + 1.0 μF
R1 120
*
$R_L$ (max. Load)
$-V_I$
$V_{in}$
LM137
$V_{out}$
$I_L$
$-V_O$ (min. Load)
$V_O$ (max. Load)

*Pulse Testing required:
1% Duty Cycle is suggested.

Load Regulation (mV) = $V_O$ (min. Load) − $V_O$ (max. Load)

$$\text{Load Regulation (\% } V_O) = \frac{V_O \text{ (min. Load)} - V_O \text{(max. Load)}}{V_O \text{ (min. Load)}} \times 100$$

FIGURE 3 — STANDARD TEST CIRCUIT


R2 1%
$V_I$
$C_{in}$ 1.0 μF
$C_O$ + 1.0 μF
$R_L$
$V_O$
$I_{adj}$
$V_{ref}$
R1 120
Adjust
$V_{in}$
LM137
$V_{out}$
$I_L$

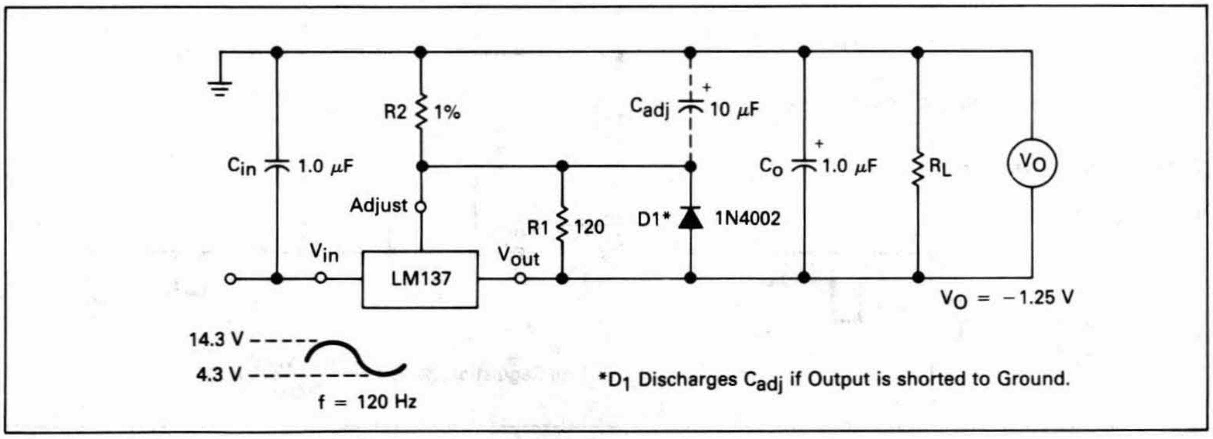
To Calculate R2:

$$R_2 = \left(\frac{V_O}{V_{Ref}} - 1\right)R_1$$

This assumes $I_{adj}$ is negligible.

Pulse Testing Required:
1% Duty Cycle is suggested.

FIGURE 4 — RIPPLE REJECTION TEST CIRCUIT


R2 1%
$C_{adj}$ + 10 μF
$C_{in}$ 1.0 μF
$C_O$ + 1.0 μF
$R_L$
$V_O$
Adjust
R1 120
D1* 1N4002
$V_{in}$
LM137
$V_{out}$
$V_O$ = −1.25 V
14.3 V
4.3 V
f = 120 Hz

*$D_1$ Discharges $C_{adj}$ if Output is shorted to Ground.

FIGURE 5 – LOAD REGULATION

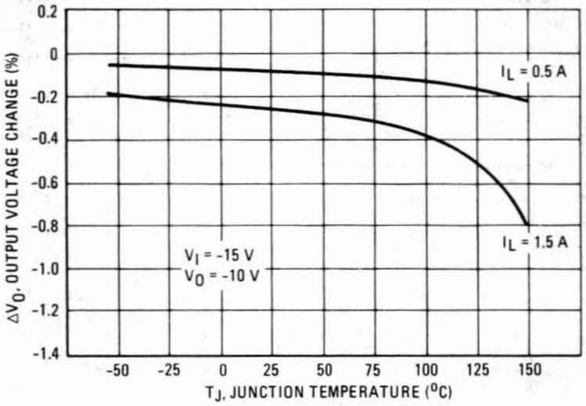


FIGURE 6 – CURRENT LIMIT

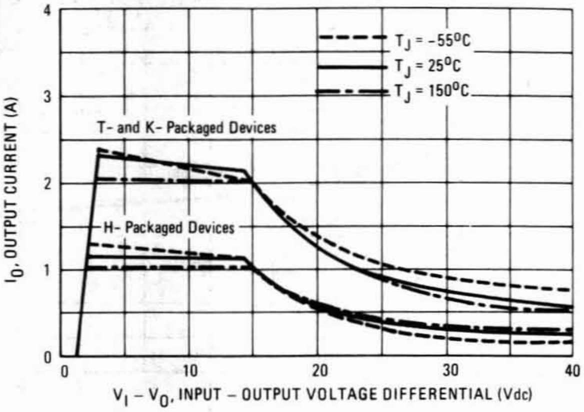


FIGURE 7 – ADJUSTMENT PIN CURRENT

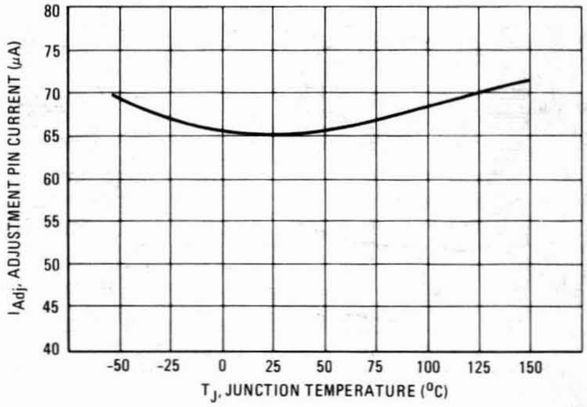


FIGURE 8 – DROPOUT VOLTAGE

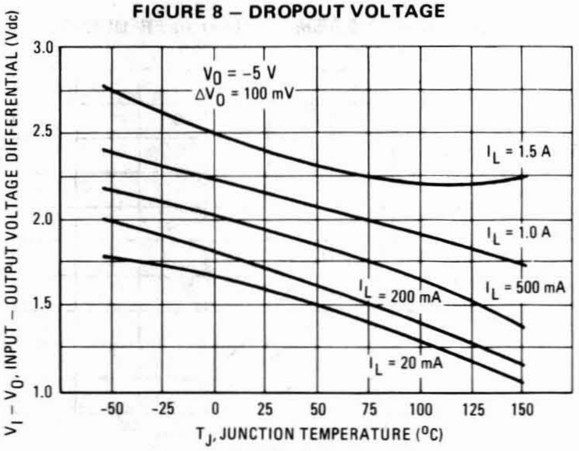


FIGURE 9 – TEMPERATURE STABILITY

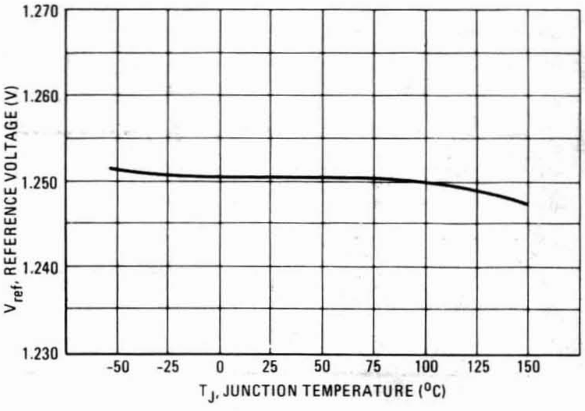


FIGURE 10 – MINIMUM OPERATING CURRENT

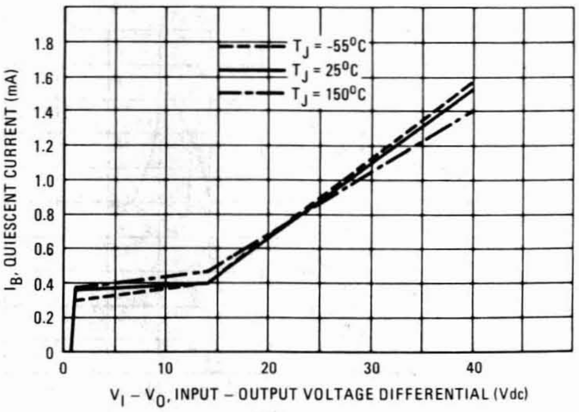


**FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE**

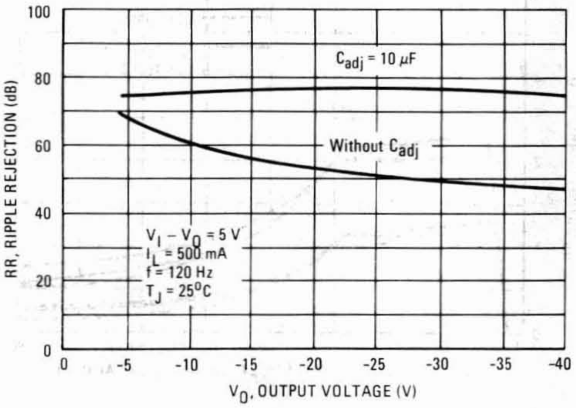


**FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT**

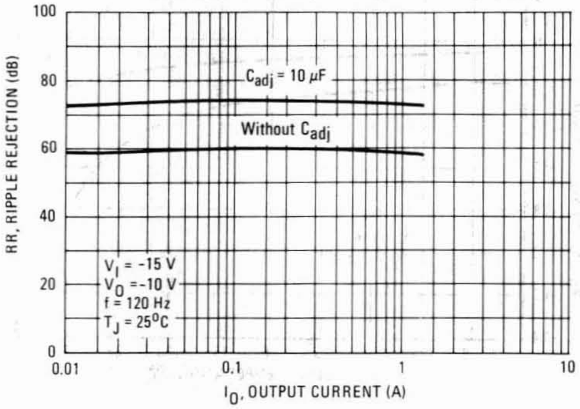


**FIGURE 13 — RIPPLE REJECTION versus FREQUENCY**

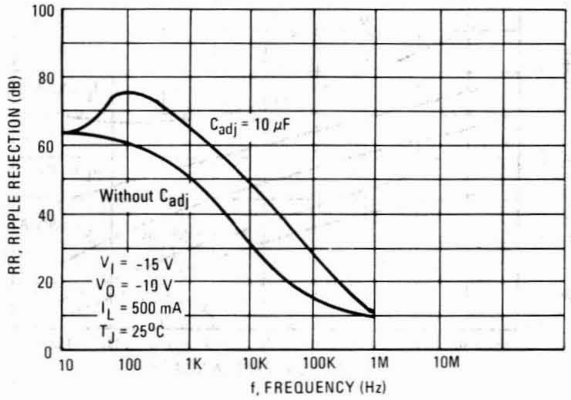


**FIGURE 14 — OUTPUT IMPEDANCE**

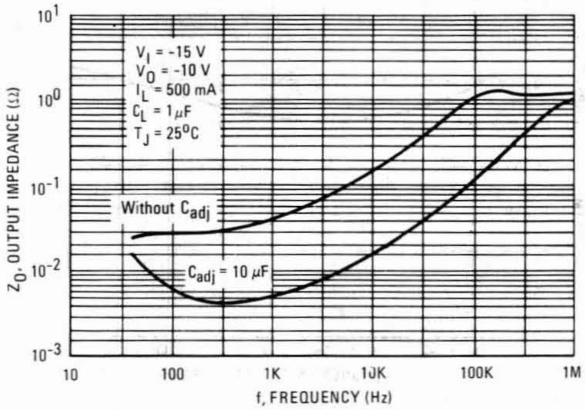


**FIGURE 15 — LINE TRANSIENT RESPONSE**

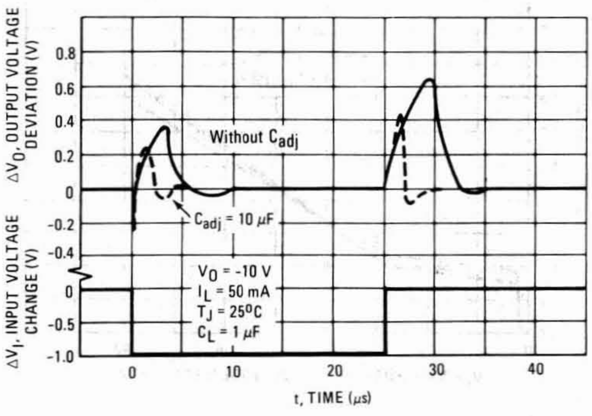
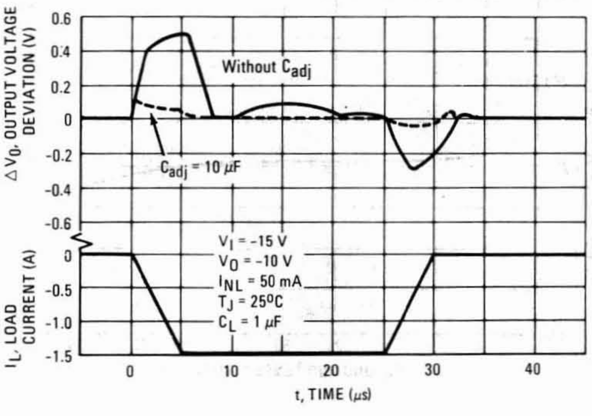


**FIGURE 16 — LOAD TRANSIENT RESPONSE**



## APPLICATIONS INFORMATION

### BASIC CIRCUIT OPERATION

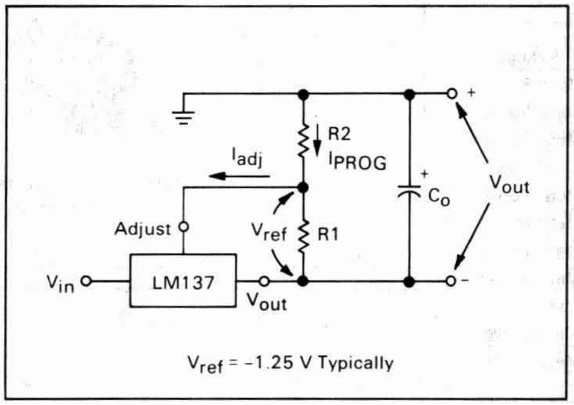
The LM137 is a 3-terminal floating regulator. In operation, the LM137 develops and maintains a nominal −1.25 volt reference ($V_{ref}$) between its output and adjustment terminals. This reference voltage is converted to a programming current ($I_{PROG}$) by R1 (see Figure 17), and this constant current flows through R2 from ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{adj}\,R2$$

Since the current into the adjustment terminal ($I_{adj}$) represents an error term in the equation, the LM137 was designed to control $I_{adj}$ to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will increase.

Since the LM137 is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



### LOAD REGULATION

The LM137 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

### EXTERNAL CAPACITORS

A 1 μF tantalum input bypass capacitor ($C_{in}$) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor ($C_{adj}$) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

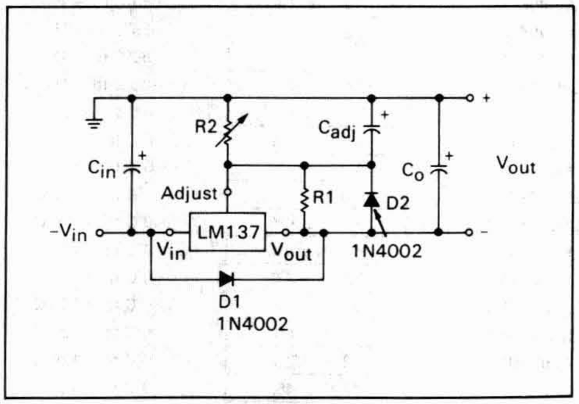
An output capacitor ($C_o$) in the form of a 1 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability.

### PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM137 with the recommended protection diodes for output voltages in excess of −25 V or high capacitance values ($C_o > 25$ μF, $C_{adj} > 10$ μF). Diode $D_1$ prevents $C_o$ from discharging thru the I.C. during an input short circuit. Diode $D_2$ protects against capacitor $C_{adj}$ discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents $C_{adj}$ from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES



**MOTOROLA**

# LM140,A Series
# LM340,A Series

## Specifications and Applications Information

### THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

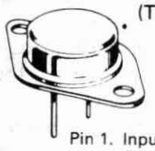
### THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.0 ampere. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on A-suffix 5.0, 12 and 15 volt device types.

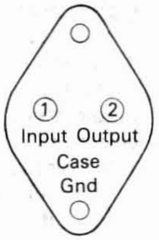
Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to boost output current capability at the nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

**K SUFFIX**
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)

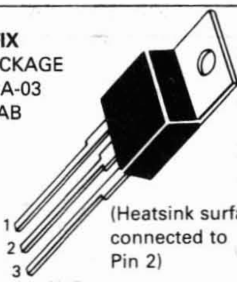


Pin 1. Input
2. Output
Case Ground



(Bottom View)

**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220AB



Pin 1. Input
2. Ground
3. Output

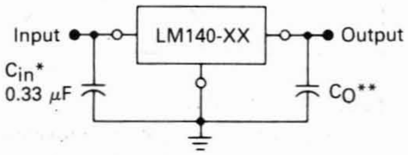
(Heatsink surface connected to Pin 2)

### ORDERING INFORMATION

| Device | Output Voltage and Tolerance | Operating Junction Temperature Range | Package |
|---|---|---|---|
| LM140K-5.0 | 5.0 V ± 4% | −55°C to +150°C | Metal Power |
| LM140AK-5.0 | 5.0 V ± 2% | −55°C to +150°C | Metal Power |
| LM140K-6.0 | 6.0 V ± 4% | −55°C to +150°C | Metal Power |
| LM140K-8.0 | 8.0 V ± 4% | −55°C to +150°C | Metal Power |
| LM140K-12 | 12 V ± 4% | −55°C to +150°C | Metal Power |
| LM140AK-12 | 12 V ± 2% | −55°C to +150°C | Metal Power |
| LM140K-15 | 15 V ± 4% | −55°C to +150°C | Metal Power |
| LM140AK-15 | 15 V ± 2% | −55°C to +150°C | Metal Power |
| LM140K-18 | 18 V ± 4% | −55°C to +150°C | Metal Power |
| LM140K-24 | 24 V ± 4% | −55°C to +150°C | Metal Power |
| LM340K-5.0 | 5.0 V ± 4% | 0°C to +125°C | Metal Power |
| LM340AK-5.0 | 5.0 V ± 2% | 0°C to +125°C | |
| LM340T-5.0 | 5.0 V ± 4% | 0°C to +125°C | Plastic Power |
| LM340AT-5.0 | 5.0 V ± 2% | 0°C to +125°C | |
| LM340K-6.0 | 6.0 V ± 4% | 0°C to +125°C | Metal Power |
| LM340T-6.0 | 6.0 V ± 4% | 0°C to +125°C | Plastic Power |
| LM340K-8.0 | 8.0 V ± 4% | 0°C to +125°C | Metal Power |
| LM340T-8.0 | 8.0 V ± 4% | 0°C to +125°C | Plastic Power |
| LM340K-12 | 12 V ± 4% | 0°C to +125°C | Metal Power |
| LM340AK-12 | 12 V ± 2% | 0°C to +125°C | |
| LM340T-12 | 12 V ± 4% | 0°C to +125°C | Plastic Power |
| LM340AT-12 | 12 V ± 2% | 0°C to +125°C | |
| LM340K-15 | 15 V ± 4% | 0°C to +125°C | Metal Power |
| LM340AK-15 | 15 V ± 2% | 0°C to +125°C | |
| LM340T-15 | 15 V ± 4% | 0°C to +125°C | Plastic Power |
| LM340AT-15 | 15 V ± 2% | 0°C to +125°C | |
| LM340K-18 | 18 V ± 4% | 0°C to +125°C | Metal Power |
| LM340T-18 | 18 V ± 4% | 0°C to +125°C | Plastic Power |
| LM340K-24 | 24 V ± 4% | 0°C to +125°C | Metal Power |
| LM340T-24 | 24 V ± 4% | 0°C to +125°C | Plastic Power |

***2% regulators are available in 5, 12 and 15 volt devices**

### STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.7 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

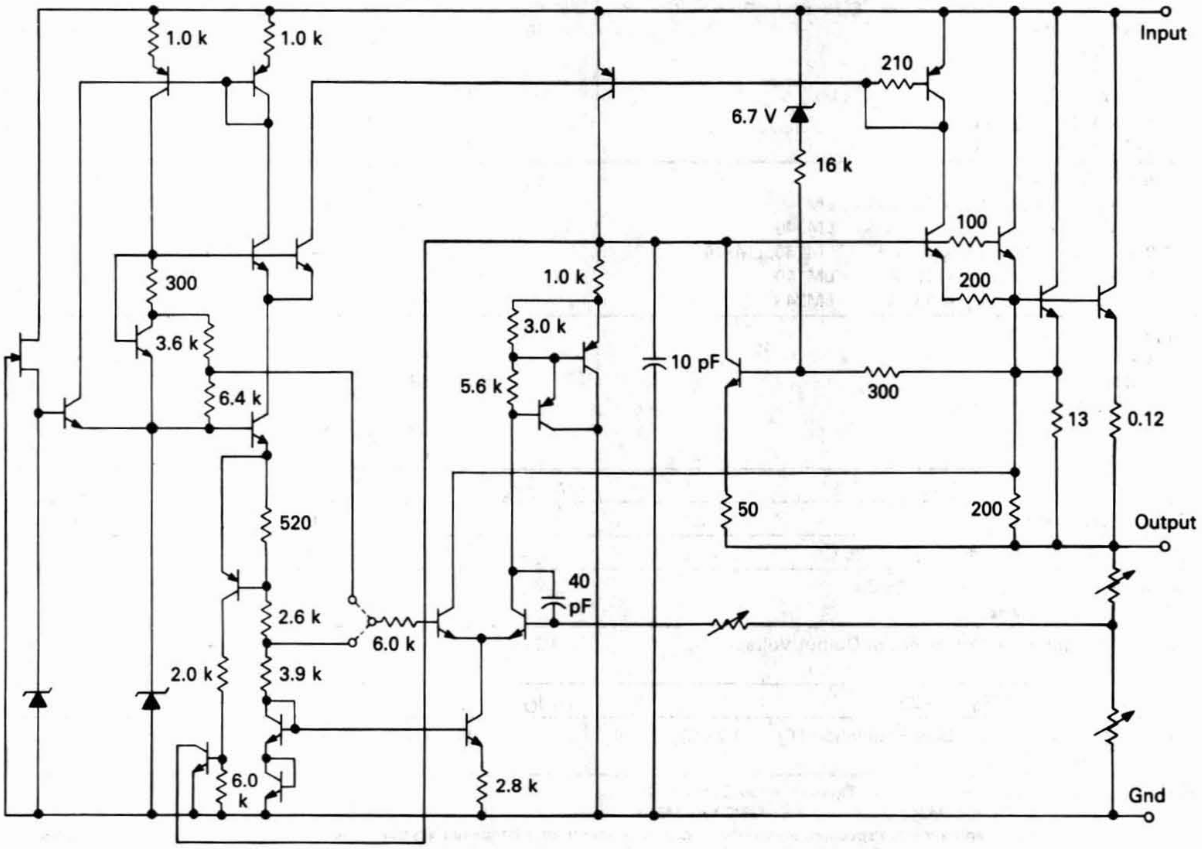
* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_O$ is not needed for stability; however, it does improve transient response. If needed, use a 0.1 μF ceramic disc.

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (5.0 V − 18 V)<br>(24 V) | $V_{in}$ | 35<br>40 | Vdc |
| Power Dissipation and Thermal Characteristics | | | |
| Plastic Package | | | |
| $T_A$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_A$ = +25°C | $1/\theta_{JA}$ | 15.4 | mW/°C |
| Thermal Resistance, Junction to Air | $\theta_{JA}$ | 65 | °C/W |
| $T_C$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_C$ = +75°C (See Figure 1) | $1/\theta_{JC}$ | 200 | mW/°C |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | 5.0 | °C/W |
| Metal Package | | | |
| $T_C$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_A$ = +25°C | $1/\theta_{JA}$ | 22.5 | mW/°C |
| Thermal Resistance, Junction to Air | $\theta_{JA}$ | 45 | °C/W |
| $T_C$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_C$ = +65°C (See Figure 2) | $1/\theta_{JC}$ | 182 | mW/°C |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | 5.5 | °C/W |
| Storage Junction Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Operating Junction Temperature Range | $T_J$ | | °C |
| LM140,A | | −55 to +150 | |
| LM340,A | | 0 to +150 | |

## EQUIVALENT SCHEMATIC DIAGRAM


1.0 k
1.0 k
Input
210
6.7 V
16 k
100
200
300
3.6 k
6.4 k
1.0 k
3.0 k
5.6 k
10 pF
300
13
0.12
520
50
200
Output
40 pF
2.6 k
6.0 k
2.0 k
3.9 k
6.0 k
2.8 k
Gnd

## DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

### LM140/340 — 5.0

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 10 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ (Note 1), unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C)<br>$I_O$ = 5.0 mA to 1.0 A | $V_O$ | 4.8 | 5.0 | 5.2 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | mV |
| 8.0 to 20 Vdc | | — | — | 50 | |
| 7.0 to 25 Vdc ($T_J$ = +25°C) | | — | — | 50 | |
| 8.0 to 12 Vdc, $I_O$ = 1.0 A | | — | — | 25 | |
| 7.3 to 20 Vdc, $I_O$ = 1.0 A ($T_J$ = +25°C) | | — | — | 50 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | — | 50 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A ($T_J$ = +25°C) | | — | — | 50 | |
| 250 mA ≤ $I_O$ ≤ 750 mA ($T_J$ = +25°C) | | — | — | 25 | |
| Output Voltage | $V_O$ | | | | Vdc |
| LM140<br>8.0 ≤ $V_{in}$ ≤ 20 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 4.75 | — | 5.25 | |
| LM340<br>7.0 ≤ $V_{in}$ ≤ 20 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 4.75 | — | 5.25 | |
| Quiescent Current<br>$I_O$ = 1.0 A | $I_B$ | | | | mA |
| LM140 | | — | — | 7.0 | |
| LM340 | | — | — | 8.5 | |
| LM140 ($T_J$ = +25°C) | | — | 4.0 | 6.0 | |
| LM340 ($T_J$ = +25°C) | | — | 4.0 | 8.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | mA |
| 8.0 ≤ $V_{in}$ ≤ 25 Vdc, $I_O$ = 500 mA LM140 | | — | — | 0.8 | |
| 7.0 ≤ $V_{in}$ ≤ 25 Vdc, $I_O$ = 500 mA LM340 | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 10 V LM140, LM340 | | — | — | 0.5 | |
| 8.0 ≤ $V_{in}$ ≤ 20 Vdc, $I_O$ = 1.0 A LM140 | | — | — | 0.8 | |
| 7.5 ≤ $V_{in}$ ≤ 20 Vdc, $I_O$ = 1.0 A LM340 | | — | — | 1.0 | |
| Ripple Rejection | RR | | | | dB |
| LM140 | | 68 | — | — | |
| LM340 | | 62 | — | — | |
| $I_O$ = 1.0 A ($T_J$ = +25°C) | | | | | |
| LM140 | | 68 | 80 | — | |
| LM340 | | 62 | 80 | — | |
| Dropout Voltage | $V_{in}-V_O$ | — | 1.7 | — | Vdc |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | mΩ |
| Short-Circuit Current Limit ($T_J$ = +25°C) | $I_{sc}$ | — | 2.0 | — | A |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 40 | — | µV |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA | $TCV_O$ | — | ±0.6 | — | mV/°C |
| Peak Output Current ($T_J$ = +25°C) | $I_O$ | — | 2.4 | — | A |
| Input Voltage to Maintain Line Regulation ($T_J$ = +25°C)<br>$I_O$ = 1.0 A | | 7.3 | — | — | Vdc |

**NOTES:** 1. $T_{low}$ = −55°C for LM140 $T_{high}$ = +150°C for LM140
= 0°C for LM340 = +125°C for LM340

2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

### LM140A/340A — 5.0

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 10 V, $I_O$ = 1.0 A, $T_J$ = $T_{low}$ to $T_{high}$ (Note 1), unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C)<br>$I_O$ = 5.0 mA to 1.0 A | $V_O$ | 4.9 | 5.0 | 5.1 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | mV |
| 7.5 to 20 Vdc, $I_O$ = 500 mA | | — | — | 10 | |
| 7.3 to 20 Vdc ($T_J$ = +25°C) | | — | 3.0 | 10 | |
| 8.0 to 12 Vdc | | — | — | 12 | |
| 8.0 to 12 Vdc ($T_J$ = +25°C) | | — | — | 4.0 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | — | 25 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A ($T_J$ = +25°C) | | — | — | 25 | |
| 250 mA ≤ $I_O$ ≤ 750 mA ($T_J$ = +25°C) | | — | — | 15 | |
| Output Voltage<br>7.5 ≤ $V_{in}$ ≤ 20 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | $V_O$ | 4.8 | — | 5.2 | Vdc |
| Quiescent Current | $I_B$ | — | — | 6.5 | mA |
| ($T_J$ = +25°C) | | — | 3.5 | 6.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | mA |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 10 V | | — | — | 0.5 | |
| 8.0 ≤ $V_{in}$ ≤ 25 Vdc, $I_O$ = 500 mA | | — | — | 0.8 | |
| 7.5 ≤ $V_{in}$ ≤ 20 Vdc, $I_O$ = 1.0 A ($T_J$ = +25°C) | | — | — | 0.8 | |
| Ripple Rejection<br>8.0 ≤ $V_{in}$ ≤ 18 Vdc, f = 120 Hz | RR | | | | dB |
| $I_O$ = 500 mA | | 68 | — | — | |
| $I_O$ = 1.0 A ($T_J$ = +25°C) | | 68 | 80 | — | |
| Dropout Voltage | $V_{in} - V_O$ | — | 1.7 | — | Vdc |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | mΩ |
| Short-Circuit Current Limit ($T_J$ = +25°C) | $I_{sc}$ | — | 2.0 | — | A |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 40 | — | μV |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA | $TCV_O$ | — | ±0.6 | — | mV/°C |
| Peak Output Current ($T_J$ = +25°C) | $I_O$ | — | 2.4 | — | A |
| Input Voltage to Maintain Line Regulation ($T_J$ = +25°C) | | 7.3 | — | — | Vdc |

**NOTES:**

1. $T_{low}$ = −55°C for LM140A $T_{high}$ = +150°C for LM140A
   = 0°C for LM340A = +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**LM140/340 — 6.0**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 11 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ (Note 1), unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C)<br>$I_O$ = 5.0 mA to 1.0 A | $V_O$ | 5.75 | 6.0 | 6.25 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | mV |
| 9.0 to 21 Vdc | | — | — | 60 | |
| 8.0 to 25 Vdc ($T_J$ = +25°C) | | — | — | 60 | |
| 9.0 to 13 Vdc, $I_O$ = 1.0 A | | — | — | 30 | |
| 8.3 to 21 Vdc, $I_O$ = 1.0 A ($T_J$ = +25°C) | | — | — | 60 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | — | 60 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A ($T_J$ = +25°C) | | — | — | 60 | |
| 250 mA ≤ $I_O$ ≤ 750 mA ($T_J$ = +25°C) | | — | — | 30 | |
| Output Voltage | $V_O$ | | | | Vdc |
| LM140 | | | | | |
| 9.0 ≤ $V_{in}$ ≤ 21 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 5.7 | — | 6.3 | |
| LM340 | | | | | |
| 8.0 ≤ $V_{in}$ ≤ 21 Vdc, 6.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 5.7 | — | 6.3 | |
| Quiescent Current | $I_B$ | | | | mA |
| $I_O$ = 1.0 A | | | | | |
| LM140 | | — | — | 7.0 | |
| LM340 | | — | — | 8.5 | |
| LM140 ($T_J$ = +25°C) | | — | 4.0 | 6.0 | |
| LM340 ($T_J$ = +25°C) | | — | 4.0 | 8.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | mA |
| 9.0 ≤ $V_{in}$ ≤ 25 Vdc, $I_O$ = 500 mA LM140 | | — | — | 0.8 | |
| 8.0 ≤ $V_{in}$ ≤ 25 Vdc, $I_O$ = 500 mA LM340 | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 11 V LM140, LM340 | | — | — | 0.5 | |
| 9.0 ≤ $V_{in}$ ≤ 21 Vdc, $I_O$ = 1.0 A LM140 | | — | — | 0.8 | |
| 8.6 ≤ $V_{in}$ ≤ 21 Vdc, $I_O$ = 1.0 A LM340 | | — | — | 1.0 | |
| Ripple Rejection | RR | | | | dB |
| LM140 | | 65 | — | — | |
| LM340 | | 59 | — | — | |
| $I_O$ = 1.0 A ($T_J$ = +25°C) | | | | | |
| LM140 | | 65 | 78 | — | |
| LM340 | | 59 | 78 | — | |
| Dropout Voltage | $V_{in} - V_O$ | — | 1.7 | — | Vdc |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | mΩ |
| Short-Circuit Current Limit ($T_J$ = +25°C) | $I_{sc}$ | — | 1.9 | — | A |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 45 | — | µV |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA | $TCV_O$ | — | ±0.7 | — | mV/°C |
| Peak Output Current ($T_J$ = +25°C) | $I_O$ | — | 2.4 | — | A |
| Input Voltage to Maintain Line Regulation ($T_J$ = +25°C)<br>$I_O$ = 1.0 A | | 8.3 | — | — | Vdc |

**NOTES:**

1. $T_{low}$ = −55°C for LM140 $T_{high}$ = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**LM140/340 — 8.0**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 14 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ (Note 1), unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C)<br>$I_O$ = 5.0 mA to 1.0 A | $V_O$ | 7.7 | 8.0 | 8.3 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | mV |
| 11 to 23 Vdc | | — | — | 80 | |
| 10.5 to 25 Vdc ($T_J$ = +25°C) | | — | — | 80 | |
| 11 to 17 Vdc, $I_O$ = 1.0 A | | — | — | 40 | |
| 10.5 to 23 Vdc, $I_O$ = 1.0 A ($T_J$ = +25°C) | | — | — | 80 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | — | 80 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A ($T_J$ = +25°C) | | — | — | 80 | |
| 250 mA ≤ $I_O$ ≤ 750 mA ($T_J$ = +25°C) | | — | — | 40 | |
| Output Voltage | $V_O$ | | | | Vdc |
| LM140<br>11.5 ≤ $V_{in}$ ≤ 23 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 7.6 | — | 8.4 | |
| LM340<br>10.5 ≤ $V_{in}$ ≤ 23 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 7.6 | — | 8.4 | |
| Quiescent Current<br>$I_O$ = 1.0 A | $I_B$ | | | | mA |
| LM140 | | — | — | 7.0 | |
| LM340 | | — | — | 8.5 | |
| LM140 ($T_J$ = +25°C) | | — | 4.0 | 6.0 | |
| LM340 ($T_J$ = +25°C) | | — | 4.0 | 8.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | mA |
| 11.5 ≤ $V_{in}$ ≤ 25 Vdc, $I_O$ = 500 mA LM140 | | — | — | 0.8 | |
| 10.5 ≤ $V_{in}$ ≤ 25 Vdc, $I_O$ = 500 mA LM340 | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 14 V LM140, LM340 | | — | — | 0.5 | |
| 11.5 ≤ $V_{in}$ ≤ 23 Vdc, $I_O$ = 1.0 A LM140 | | — | — | 0.8 | |
| 10.6 ≤ $V_{in}$ ≤ 23 Vdc, $I_O$ = 1.0 A LM340 | | — | — | 1.0 | |
| Ripple Rejection | RR | | | | dB |
| LM140 | | 62 | — | — | |
| LM340 | | 56 | — | — | |
| $I_O$ = 1.0 A ($T_J$ = +25°C)<br>LM140 | | 62 | 76 | — | |
| LM340 | | 56 | 76 | — | |
| Dropout Voltage | $V_{in}-V_O$ | — | 1.7 | — | Vdc |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | mΩ |
| Short-Circuit Current Limit ($T_J$ = +25°C) | $I_{sc}$ | — | 1.5 | — | A |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 52 | — | μV |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA | $TCV_O$ | — | ±1.0 | — | mV/°C |
| Peak Output Current ($T_J$ = +25°C) | $I_O$ | — | 2.4 | — | A |
| Input Voltage to Maintain Line Regulation ($T_J$ = +25°C)<br>$I_O$ = 1.0 A | | 10.5 | — | — | Vdc |

**NOTES:**

1. $T_{low}$ = −55°C for LM140 $T_{high}$ = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

### LM140/340 — 12

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 19 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ (Note 1), unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C)<br>$I_O$ = 5.0 mA to 1.0 A | $V_O$ | 11.5 | 12 | 12.5 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | mV |
| 15 to 27 Vdc | | — | — | 120 | |
| 14.6 to 30 Vdc ($T_J$ = +25°C) | | — | — | 120 | |
| 16 to 22 Vdc, $I_O$ = 1.0 A | | — | — | 60 | |
| 14.6 to 27 Vdc, $I_O$ = 1.0 A ($T_J$ = +25°C) | | — | — | 120 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | — | 120 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A ($T_J$ = +25°C) | | — | — | 120 | |
| 250 mA ≤ $I_O$ ≤ 750 mA ($T_J$ = +25°C) | | — | — | 60 | |
| Output Voltage | $V_O$ | | | | Vdc |
| LM140<br>15.5 ≤ $V_{in}$ ≤ 27 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 11.4 | — | 12.6 | |
| LM340<br>14.5 ≤ $V_{in}$ ≤ 27 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 11.4 | — | 12.6 | |
| Quiescent Current<br>$I_O$ = 1.0 A | $I_B$ | | | | mA |
| LM140 | | — | — | 7.0 | |
| LM340 | | — | — | 8.5 | |
| LM140 ($T_J$ = +25°C) | | — | 4.0 | 6.0 | |
| LM340 ($T_J$ = +25°C) | | — | 4.0 | 8.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | mA |
| 15 ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 500 mA LM140 | | — | — | 0.8 | |
| 14.5 ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 500 mA LM340 | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 19 V LM140, LM340 | | — | — | 0.5 | |
| 15 ≤ $V_{in}$ ≤ 27 Vdc, $I_O$ = 1.0 A LM140 | | — | — | 0.8 | |
| 14.8 ≤ $V_{in}$ ≤ 27 Vdc, $I_O$ = 1.0 A LM340 | | — | — | 1.0 | |
| Ripple Rejection | RR | | | | dB |
| LM140 | | 61 | — | — | |
| LM340 | | 55 | — | — | |
| $I_O$ = 1.0 A ($T_J$ = +25°C)<br>LM140 | | 61 | 72 | — | |
| LM340 | | 55 | 72 | — | |
| Dropout Voltage | $V_{in} - V_O$ | — | 1.7 | — | Vdc |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | mΩ |
| Short-Circuit Current Limit ($T_J$ = +25°C) | $I_{sc}$ | — | 1.1 | — | A |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 75 | — | μV |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA | $TCV_O$ | — | ±1.5 | — | mV/°C |
| Peak Output Current ($T_J$ = +25°C) | $I_O$ | — | 2.4 | — | A |
| Input Voltage to Maintain Line Regulation ($T_J$ = +25°C)<br>$I_O$ = 1.0 A | | 14.6 | — | — | Vdc |

**NOTES:**

1. $T_{low}$ = −55°C for LM140   $T_{high}$ = +150°C for LM140
   =   = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## LM140A/340A — 12

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 19 V, $I_O$ = 1.0 A, $T_J$ = $T_{low}$ to $T_{high}$ (Note 1), unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C)<br>$I_O$ = 5.0 mA to 1.0 A | $V_O$ | 11.75 | 12 | 12.25 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | mV |
| 14.8 to 27 Vdc, $I_O$ = 500 mA | | — | — | 18 | |
| 14.5 to 27 Vdc ($T_J$ = +25°C) | | — | 4.0 | 18 | |
| 16 to 22 Vdc | | — | — | 30 | |
| 16 to 22 Vdc ($T_J$ = +25°C) | | — | — | 9.0 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | — | 60 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A ($T_J$ = +25°C) | | — | — | 32 | |
| 250 mA ≤ $I_O$ ≤ 750 mA ($T_J$ = +25°C) | | — | — | 19 | |
| Output Voltage<br>14.8 ≤ $V_{in}$ ≤ 27 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | $V_O$ | 11.5 | — | 12.5 | Vdc |
| Quiescent Current | $I_B$ | — | — | 6.5 | mA |
| ($T_J$ = +25°C) | | — | 3.5 | 6.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | mA |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 19 V | | — | — | 0.5 | |
| 15 ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 500 mA | | — | — | 0.8 | |
| 14.8 ≤ $V_{in}$ ≤ 27 Vdc, $I_O$ = 1.0 A ($T_J$ = +25°C) | | — | — | 0.8 | |
| Ripple Rejection<br>15 ≤ $V_{in}$ ≤ 25 Vdc, f = 120 Hz | RR | | | | dB |
| $I_O$ = 500 mA | | 61 | — | — | |
| $I_O$ = 1.0 A, ($T_J$ = +25°C) | | 61 | 72 | — | |
| Dropout Voltage | $V_{in} - V_O$ | — | 1.7 | — | Vdc |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | mΩ |
| Short-Circuit Current Limit ($T_J$ = +25°C) | $I_{sc}$ | — | 1.1 | — | A |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 75 | — | μV |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA | $TCV_O$ | — | ±1.5 | — | mV/°C |
| Peak Output Current ($T_J$ = +25°C) | $I_O$ | — | 2.4 | — | A |
| Input Voltage to Maintain Line Regulation ($T_J$ = +25°C) | | 14.5 | — | — | Vdc |

**NOTES:**

1. $T_{low}$ = −55°C for LM140A $T_{high}$ = +150°C for LM140A
   = 0°C for LM340A = +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**LM140A/340 — 15**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 23 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ (Note 1), unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 14.4 | 15 | 15.6 | Vdc |
| $I_O$ = 5.0 mA to 1.0 A | | | | | |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | mV |
| 18.5 to 30 Vdc | | — | — | 150 | |
| 17.5 to 30 Vdc ($T_J$ = +25°C) | | — | — | 150 | |
| 20 to 26 Vdc, $I_O$ = 1.0 A | | — | — | 75 | |
| 17.7 to 30 Vdc, $I_O$ = 1.0 A ($T_J$ = +25°C) | | — | — | 150 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | — | 150 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A ($T_J$ = +25°C) | | — | — | 150 | |
| 250 mA ≤ $I_O$ ≤ 750 mA ($T_J$ = +25°C) | | — | — | 75 | |
| Output Voltage | $V_O$ | | | | Vdc |
| LM140 | | | | | |
| 18.5 ≤ $V_{in}$ ≤ 30 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 14.25 | — | 15.75 | |
| LM340 | | | | | |
| 17.5 ≤ $V_{in}$ ≤ 30 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 14.25 | — | 15.75 | |
| Quiescent Current | $I_B$ | | | | mA |
| $I_O$ = 1.0 A | | | | | |
| LM140 | | — | — | 7.0 | |
| LM340 | | — | — | 8.5 | |
| LM140 ($T_J$ = +25°C) | | — | 4.0 | 6.0 | |
| LM340 ($T_J$ = +25°C) | | — | 4.0 | 8.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | mA |
| 18.5 ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 500 mA LM140 | | — | — | 0.8 | |
| 17.5 ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 500 mA LM340 | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 23 V LM140, LM340 | | — | — | 0.5 | |
| 18.5 ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 1.0 A LM140 | | — | — | 0.8 | |
| 17.9 ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 1.0 A LM340 | | — | — | 1.0 | |
| Ripple Rejection | RR | | | | dB |
| LM140 | | 60 | — | — | |
| LM340 | | 54 | — | — | |
| $I_O$ = 1.0 A ($T_J$ = +25°C) | | | | | |
| LM140 | | 60 | 70 | — | |
| LM340 | | 54 | 70 | — | |
| Dropout Voltage | $V_{in} - V_O$ | — | 1.7 | — | Vdc |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | mΩ |
| Short-Circuit Current Limit ($T_J$ = +25°C) | $I_{sc}$ | — | 800 | — | A |
| Output Noise Voltage ($T_A$ = +25°C) | $V_n$ | — | 90 | — | µV |
| 10 Hz ≤ f ≤ 100 kHz | | | | | |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±1.8 | — | mV/°C |
| $I_O$ = 5.0 mA | | | | | |
| Peak Output Current ($T_J$ = +25°C) | $I_O$ | — | 2.4 | — | A |
| Input Voltage to Maintain Line Regulation ($T_J$ = +25°C) | | 17.7 | — | — | Vdc |
| $I_O$ = 1.0 A | | | | | |

**NOTES:**

1. $T_{low}$ = −55°C for LM140 $T_{high}$ = +150°C for LM140
 = = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**LM140A/340A — 15**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 23 V, $I_O$ = 1.0 A, $T_J$ = $T_{low}$ to $T_{high}$ (Note 1), unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C)<br>$I_O$ = 5.0 mA to 1.0 A | $V_O$ | 14.7 | 15 | 15.3 | Vdc |
| Line Regulation (Note 2)<br>17.9 to 30 Vdc, $I_O$ = 500 mA<br>17.5 to 30 Vdc ($T_J$ = +25°C)<br>20 to 26 Vdc, $I_O$ = 1.0 A<br>20 to 26 Vdc, $I_O$ = 1.0 A ($T_J$ = +25°C) | $Reg_{line}$ | <br>—<br>—<br>—<br>— | <br>—<br>4.0<br>—<br>— | <br>22<br>22<br>30<br>10 | mV |
| Load Regulation (Note 2)<br>5.0 mA ≤ $I_O$ ≤ 1.0 A<br>5.0 mA ≤ $I_O$ ≤ 1.5 A ($T_J$ = +25°C)<br>250 mA ≤ $I_O$ ≤ 750 mA ($T_J$ = +25°C) | $Reg_{load}$ | <br>—<br>—<br>— | <br>—<br>12<br>— | <br>75<br>35<br>21 | mV |
| Output Voltage<br>17.9 ≤ $V_{in}$ ≤ 30 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | $V_O$ | 14.4 | — | 15.6 | Vdc |
| Quiescent Current<br>($T_J$ = +25°C) | $I_B$ | —<br>— | —<br>3.5 | 6.5<br>6.0 | mA |
| Quiescent Current Change<br>5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 23 V<br>17.9 ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 500 mA<br>17.9 ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 1.0 A ($T_J$ = +25°C) | $\Delta I_B$ | <br>—<br>—<br>— | <br>—<br>—<br>— | <br>0.5<br>0.8<br>0.8 | mA |
| Ripple Rejection<br>18.5 ≤ $V_{in}$ ≤ 28.5 Vdc, f = 120 Hz<br>$I_O$ = 500 mA<br>$I_O$ = 1.0 A, ($T_J$ = +25°C) | RR | <br><br>60<br>60 | <br><br>—<br>70 | <br><br>—<br>— | dB |
| Dropout Voltage | $V_{in} - V_O$ | — | 1.7 | — | Vdc |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | mΩ |
| Short-Circuit Current Limit ($T_J$ = +25°C) | $I_{sc}$ | — | 800 | — | mA |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 90 | — | μV |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA | $TCV_O$ | — | ±1.8 | — | mV/°C |
| Peak Output Current ($T_J$ = +25°C) | $I_O$ | — | 2.4 | — | A |
| Input Voltage to Maintain Line Regulation ($T_J$ = +25°C) | | 17.5 | — | — | Vdc |

**NOTES:**

1. $T_{low}$ = −55°C for LM140A $T_{high}$ = +150°C for LM140A
   = 0°C for LM340A = +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**LM140/340 — 18**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 27 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ (Note 1), unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C)<br>$I_O$ = 5.0 mA to 1.0 A | $V_O$ | 17.3 | 18 | 18.7 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | mV |
| 21.5 to 33 Vdc | | — | — | 180 | |
| 21 to 33 Vdc ($T_J$ = +25°C) | | — | — | 180 | |
| 24 to 30 Vdc, $I_O$ = 1.0 A | | — | — | 90 | |
| 21 to 33 Vdc, $I_O$ = 1.0 A ($T_J$ = +25°C) | | — | — | 180 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | — | 180 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A ($T_J$ = +25°C) | | — | — | 180 | |
| 250 mA ≤ $I_O$ ≤ 750 mA ($T_J$ = +25°C) | | — | — | 90 | |
| Output Voltage | $V_O$ | | | | Vdc |
| LM140<br>22 ≤ $V_{in}$ ≤ 33 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 17.1 | — | 18.9 | |
| LM340<br>21 ≤ $V_{in}$ ≤ 33 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 17.1 | — | 18.9 | |
| Quiescent Current<br>$I_O$ = 1.0 A | $I_B$ | | | | mA |
| LM140 | | — | — | 7.0 | |
| LM340 | | — | — | 8.5 | |
| LM140 ($T_J$ = +25°C) | | — | 4.0 | 6.0 | |
| LM340 ($T_J$ = +25°C) | | — | 4.0 | 8.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | mA |
| 22 ≤ $V_{in}$ ≤ 33 Vdc, $I_O$ = 500 mA LM140 | | — | — | 0.8 | |
| 21 ≤ $V_{in}$ ≤ 33 Vdc, $I_O$ = 500 mA LM340 | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 27 V LM140, LM340 | | — | — | 0.5 | |
| 22 ≤ $V_{in}$ ≤ 33 Vdc, $I_O$ = 1.0 A LM140 | | — | — | 0.8 | |
| 21 ≤ $V_{in}$ ≤ 33 Vdc, $I_O$ = 1.0 A LM340 | | — | — | 1.0 | |
| Ripple Rejection | RR | | | | dB |
| LM140 | | 59 | — | — | |
| LM340 | | 53 | — | — | |
| $I_O$ = 1.0 A ($T_J$ = +25°C) | | | | | |
| LM140 | | 59 | 69 | — | |
| LM340 | | 53 | 69 | — | |
| Dropout Voltage | $V_{in} - V_O$ | — | 1.7 | — | Vdc |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | mΩ |
| Short-Circuit Current Limit ($T_J$ = +25°C) | $I_{sc}$ | — | 500 | — | A |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 110 | — | μV |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA | $TCV_O$ | — | ±2.3 | — | mV/°C |
| Peak Output Current ($T_J$ = +25°C) | $I_O$ | — | 2.4 | — | A |
| Input Voltage to Maintain Line Regulation ($T_J$ = +25°C)<br>$I_O$ = 1.0 A | | 21 | — | — | Vdc |

**NOTES:**

1. $T_{low}$ = −55°C for LM140 $T_{high}$ = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**LM140/340 — 24**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 33 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ (Note 1), unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C)<br>$I_O$ = 5.0 mA to 1.0 A | $V_O$ | 23 | 24 | 25 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | mV |
| 28 to 38 Vdc | | — | — | 240 | |
| 27 to 38 Vdc ($T_J$ = +25°C) | | — | — | 240 | |
| 30 to 36 Vdc, $I_O$ = 1.0 A | | — | — | 120 | |
| 27.1 to 38 Vdc, $I_O$ = 1.0 A ($T_J$ = +25°C) | | — | — | 240 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | — | 240 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A ($T_J$ = +25°C) | | — | — | 240 | |
| 250 mA ≤ $I_O$ ≤ 750 mA ($T_J$ = +25°C) | | — | — | 120 | |
| Output Voltage | $V_O$ | | | | Vdc |
| LM140<br>28 ≤ $V_{in}$ ≤ 38 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 22.8 | — | 25.2 | |
| LM340<br>27 ≤ $V_{in}$ ≤ 38 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_D$ ≤ 15 W | | 22.8 | — | 25.2 | |
| Quiescent Current<br>$I_O$ = 1.0 A | $I_B$ | | | | mA |
| LM140 | | — | — | 7.0 | |
| LM340 | | — | — | 8.5 | |
| LM140 ($T_J$ = +25°C) | | — | 4.0 | 6.0 | |
| LM340 ($T_J$ = +25°C) | | — | 4.0 | 8.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | mA |
| 28 ≤ $V_{in}$ ≤ 38 Vdc, $I_O$ = 500 mA LM140 | | — | — | 0.8 | |
| 27 ≤ $V_{in}$ ≤ 38 Vdc, $I_O$ = 500 mA LM340 | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 33 V LM140, LM340 | | — | — | 0.5 | |
| 28 ≤ $V_{in}$ ≤ 38 Vdc, $I_O$ = 1.0 A LM140 | | — | — | 0.8 | |
| 27.3 ≤ $V_{in}$ ≤ 38 Vdc, $I_O$ = 1.0 A LM340 | | — | — | 1.0 | |
| Ripple Rejection | RR | | | | dB |
| LM140 | | 56 | — | — | |
| LM340 | | 50 | — | — | |
| $I_O$ = 1.0 A ($T_J$ = +25°C)<br>LM140 | | 56 | 66 | — | |
| LM340 | | 50 | 66 | — | |
| Dropout Voltage | $V_{in} - V_O$ | — | 1.7 | — | Vdc |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | mΩ |
| Short-Circuit Current Limit ($T_J$ = +25°C) | $I_{sc}$ | — | 200 | — | A |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 170 | — | µV |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA | $TCV_O$ | — | ±3.0 | — | mV/°C |
| Peak Output Current ($T_J$ = +25°C) | $I_O$ | — | 2.4 | — | A |
| Input Voltage to Maintain Line Regulation ($T_J$ = +25°C)<br>$I_O$ = 1.0 A | | 27.1 | — | — | Vdc |

**NOTES:**

1. $T_{low}$ = −55°C for LM140 $T_{high}$ = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

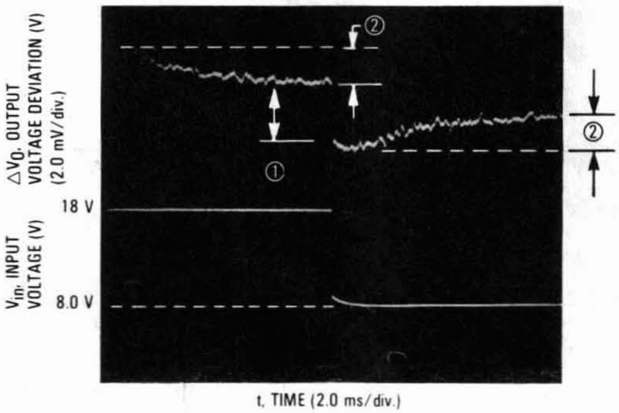
### VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

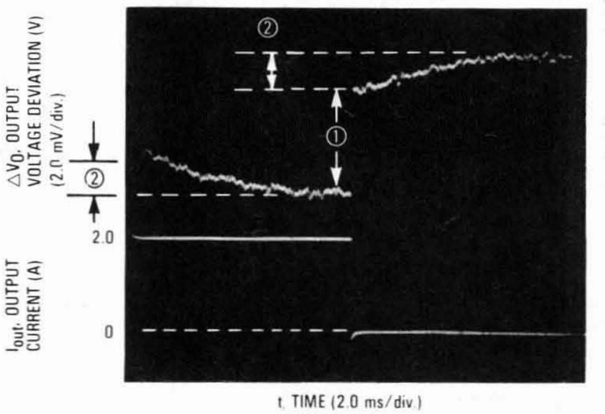
Figure 1 shows the line and thermal regulation response of a typical LM140AK-5.0 to a 10 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical LM140AK-5.0 to a 15 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION



LM140AK-5.0
$V_O$ = 5.0 V
$V_{in}$ = 8.0 V → 18 V → 8.0 V ① = $Reg_{line}$ = 2.4 mV
$I_{out}$ = 1.0 A ② = $Reg_{therm}$ = 0.0030%$V_O$/W

FIGURE 2 — LOAD AND THERMAL REGULATION



LM140AK-5.0
$V_O$ = 5.0 V
$V_{in}$ = 15 ① = $Reg_{load}$ = 4.4 mV
$I_{out}$ = 0 A → 1.5 A → 0 A ② = $Reg_{therm}$ = 0.0020%$V_O$/W

FIGURE 3 — TEMPERATURE STABILITY

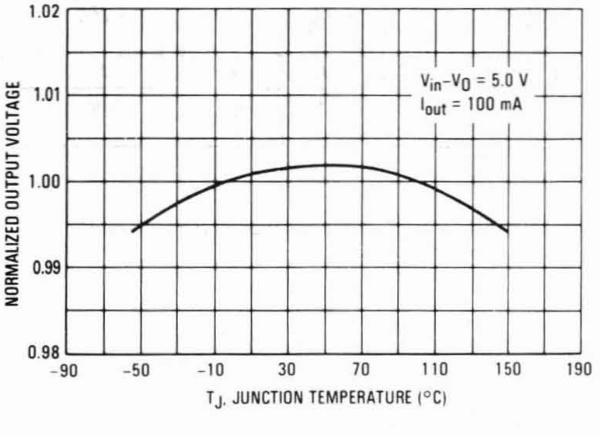


FIGURE 4 — OUTPUT IMPEDANCE

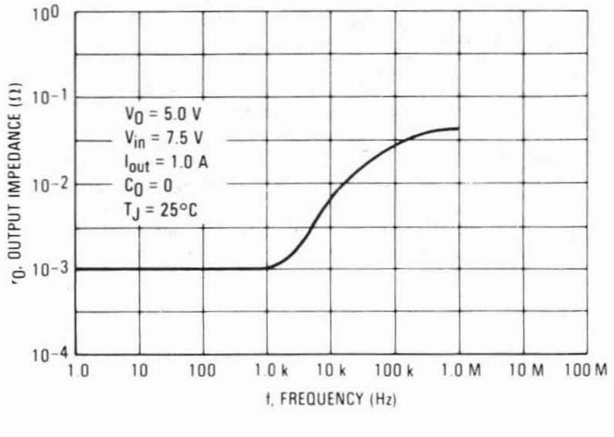


**FIGURE 5 — RIPPLE REJECTION versus FREQUENCY**

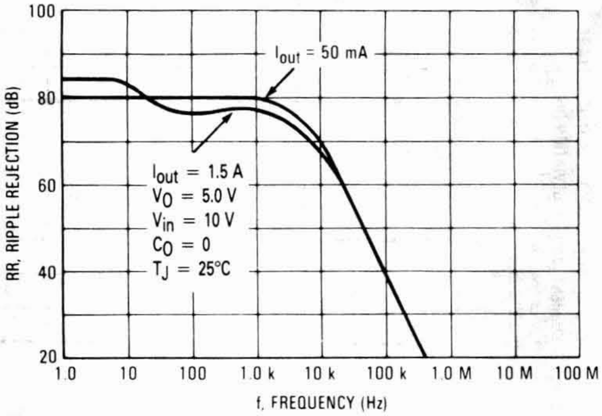


**FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT**

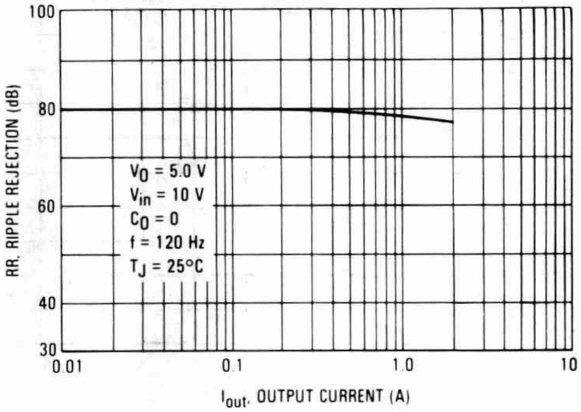


**FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE**

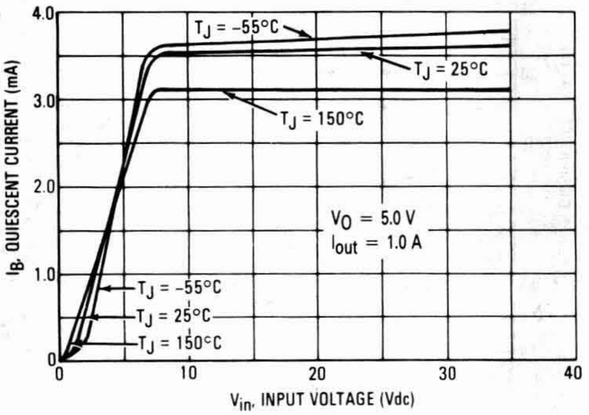


**FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT**

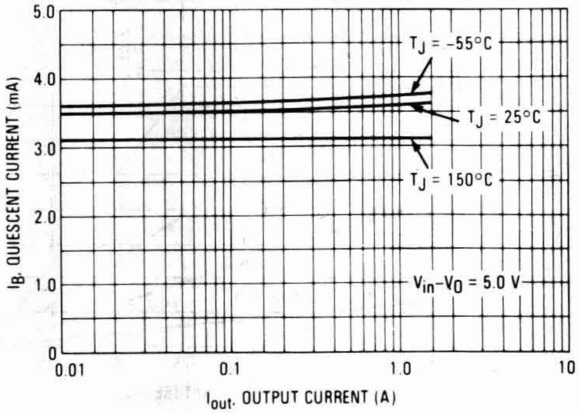


**FIGURE 9 — DROPOUT VOLTAGE**

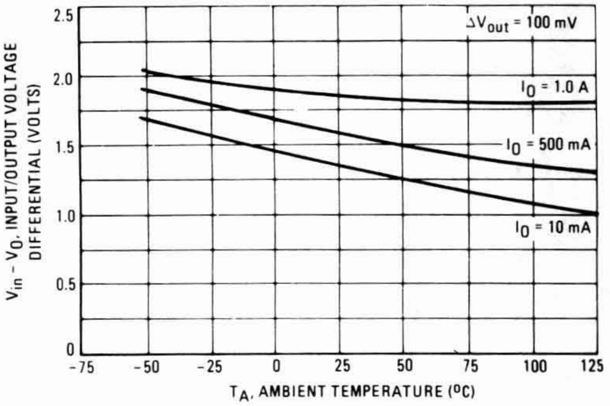


**FIGURE 10 — PEAK OUTPUT CURRENT**

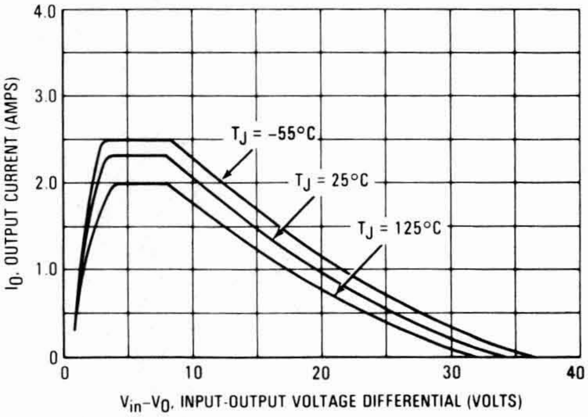


**FIGURE 11 — LINE TRANSIENT RESPONSE**

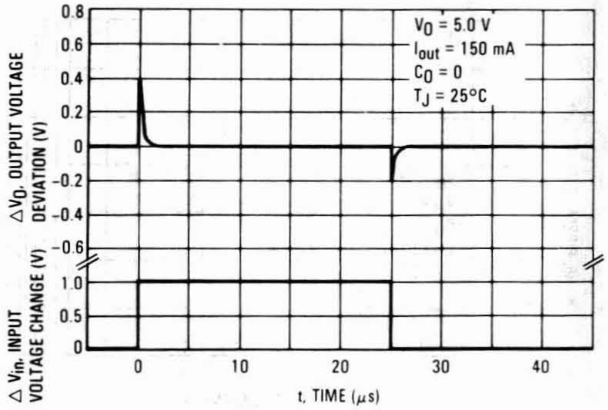


**FIGURE 12 — LOAD TRANSIENT RESPONSE**

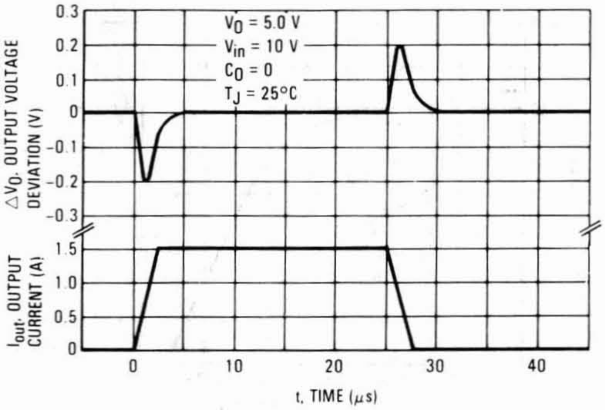


**FIGURE 13 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 221A)**

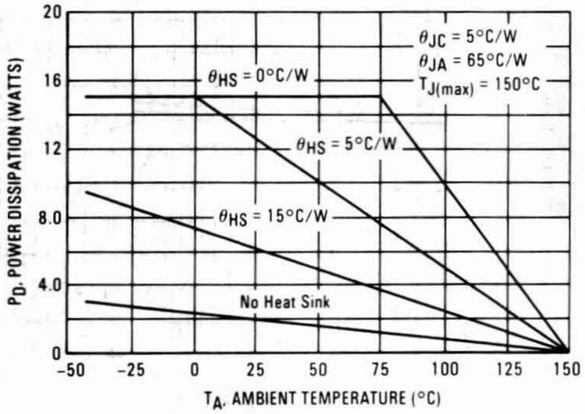
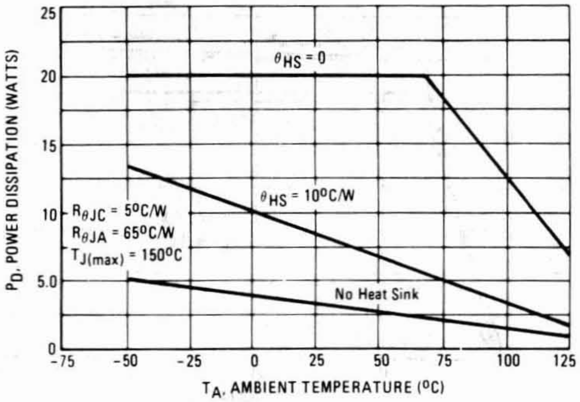


**FIGURE 14 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 1)**



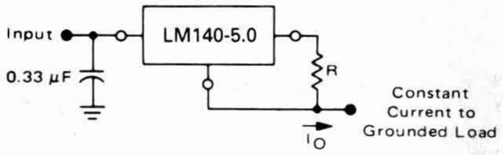
## APPLICATIONS INFORMATION

### Design Considerations

The LM140 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



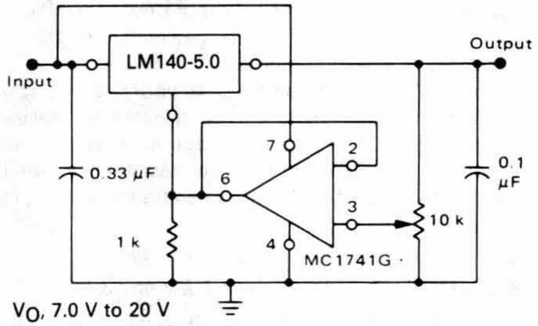
These regulators can also be used as a current source when connected as above. In order to minimize dissipation the LM140-5.0 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7.0 volts.

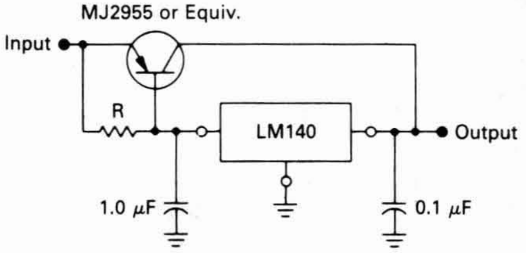
FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



$V_O$, 7.0 V to 20 V
$V_{IN} - V_O \geq 2.0$ V

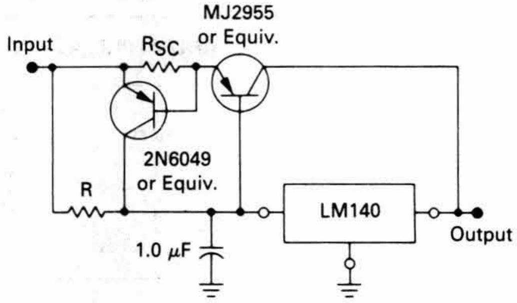
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with thi arrangement is 2.0 volts greater than the regulator voltage.

FIGURE 17 — CURRENT BOOST REGULATOR



The LM140 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the $V_{BE}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by $V_{BE}$ of the pass transistor.

FIGURE 18 — SHORT-CIRCUIT PROTECTION



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, $P_{SC}$, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

**MOTOROLA**

# LM150
# LM250
# LM350

## Specifications and Applications Information

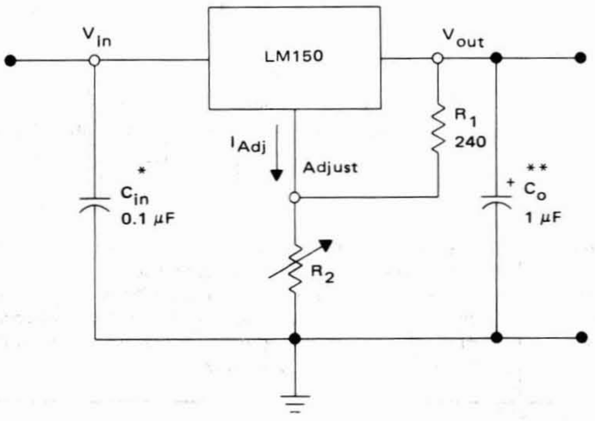
### 3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

The LM150/250/350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3.0 A over an output voltage range of 1.2 V to 33 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM150 series serve a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM150 series can be used as a precision current regulator.

- Guaranteed 3.0 Amps Output Current
- Output Adjustable between 1.2 V and 33 V
- Load Regulation Typically 0.1%
- Line Regulation Typically 0.005%/V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

### STANDARD APPLICATION



* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_o$ is not needed for stability, however it does improve transient response.

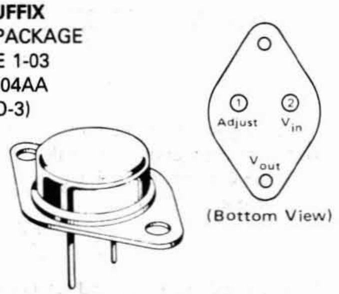
$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

Since $I_{Adj}$ is controlled to less than 100 µA, the error associated with this term is negligible in most applications

### 3-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

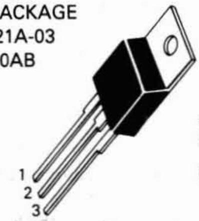
SILICON MONOLITHIC
INTEGRATED CIRCUIT

**K SUFFIX**
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)



Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220AB



Pin 1 Adjust
Pin 2 $V_{out}$
Pin 3 $V_{in}$

Heatsink surface connected to Pin 2

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| LM150K | $T_J$ = −55°C to +150°C | Metal Power |
| LM250K | $T_J$ = −25°C to +150°C | Metal Power |
| LM350K | $T_J$ = 0°C to +125°C | Metal Power |
| LM350T | $T_J$ = 0°C to +125°C | Plastic Power |

### MAXIMUM RATINGS

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Input-Output Voltage Differential | | $V_I$-$V_O$ | 35 | Vdc |
| Power Dissipation | | $P_D$ | Internally Limited | |
| Operating Junction Temperature Range | LM150<br>LM250<br>LM350 | $T_J$ | −55 to +150<br>−25 to +150<br>0 to +125 | °C |
| Storage Temperature Range | | $T_{stg}$ | −65 to +150 | °C |
| Soldering Lead Temperature (10 seconds) | | | 300 | °C |

**ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, $V_I$-$V_O$ = 5.0 V; $I_L$ = 1.5 A; $T_J$ = $T_{low}$ to $T_{high}$; $P_{max}$ [see Note 1].)

| Characteristic | Figure | Symbol | LM150/250 Min | LM150/250 Typ | LM150/250 Max | LM350 Min | LM350 Typ | LM350 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Line Regulation (Note 2)<br>$T_A$ = 25°C, 3.0 V ≤ $V_I$-$V_O$ ≤ 35 V | 1 | $Reg_{line}$ | — | 0.005 | 0.01 | — | 0.005 | 0.03 | %/V |
| Load Regulation (Note 2)<br>$T_A$ = 25°C, 10 mA ≤ $I_L$ ≤ 3.0 A | 2 | $Reg_{load}$ | | | | | | | |
| $V_O$ ≤ 5.0 V | | | — | 5.0 | 15 | — | 5.0 | 25 | mV |
| $V_O$ ≥ 5.0 V | | | — | 0.1 | 0.3 | — | 0.1 | 0.5 | % $V_O$ |
| Thermal Regulation, Pulse = 20 ms,<br>$T_A$ = 25°C | — | $Reg_{therm}$ | — | 0.002 | — | — | 0.002 | — | % $V_O$/W |
| Adjustment Pin Current | 3 | $I_{Adj}$ | — | 50 | 100 | — | 50 | 100 | μA |
| Adjustment Pin Current Change<br>3.0 V ≤ $V_I$-$V_O$ ≤ 35 V<br>10 mA ≤ $I_L$ ≤ 3.0 A, $P_D$ ≤ $P_{max}$ | 1,2 | $\Delta I_{Adj}$ | — | 0.2 | 5.0 | — | 0.2 | 5.0 | μA |
| Reference Voltage (Note 3)<br>3.0 V ≤ $V_I$-$V_O$ ≤ 35 V<br>10 mA ≤ $I_L$ ≤ 3.0 A, $P_D$ ≤ $P_{max}$ | 3 | $V_{ref}$ | 1.20 | 1.25 | 1.30 | 1.20 | 1.25 | 1.30 | V |
| Line Regulation (Note 2)<br>3.0 V ≤ $V_I$-$V_O$ ≤ 35 V | 1 | $Reg_{line}$ | — | 0.02 | 0.05 | — | 0.02 | 0.07 | %/V |
| Load Regulation (Note 2)<br>10 mA ≤ $I_L$ ≤ 3.0 A | 2 | $Reg_{load}$ | | | | | | | |
| $V_O$ ≤ 5.0 V | | | — | 20 | 50 | — | 20 | 70 | mV |
| $V_O$ ≥ 5.0 V | | | — | 0.3 | 1.0 | — | 0.3 | 1.5 | % $V_O$ |
| Temperature Stability ($T_{low}$ ≤ $T_J$ ≤ $T_{high}$) | 3 | $T_S$ | — | 1.0 | — | — | 1.0 | — | % $V_O$ |
| Minimum Load Current to Maintain Regulation ($V_I$-$V_O$ = 35 V) | 3 | $I_{Lmin}$ | — | 3.5 | 5.0 | — | 3.5 | 10 | mA |
| Maximum Output Current | 3 | $I_{max}$ | | | | | | | A |
| $V_I$-$V_O$ ≤ 10 V, $P_D$ ≤ $P_{max}$ | | | 3.0 | 4.5 | — | 3.0 | 4.5 | — | |
| $V_I$-$V_O$ = 30 V, $P_D$ ≤ $P_{max}$, $T_A$ = 25°C | | | 0.3 | 1.0 | — | 0.25 | 1.0 | — | |
| RMS Noise, % of $V_O$<br>$T_A$ = 25°C, 10 Hz ≤ f ≤ 10 kHz | — | N | — | 0.003 | — | — | 0.003 | — | % $V_O$ |
| Ripple Rejection, $V_O$ = 10 V, f = 120 Hz (Note 4) | 4 | RR | | | | | | | dB |
| Without $C_{Adj}$ | | | — | 65 | — | — | 65 | — | |
| $C_{Adj}$ = 10 μF | | | 66 | 80 | — | 66 | 80 | — | |
| Long-Term Stability, $T_J$ = $T_{high}$ (Note 5)<br>$T_A$ = 25°C for Endpoint Measurements | 3 | S | — | 0.3 | 1.0 | — | 0.3 | 1.0 | %/1.0 k Hrs. |
| Thermal Resistance Junction to Case | — | $R_{\theta JC}$ | | | | | | | °C/W |
| Peak (Note 6) K Package (TO-3) | | | — | 2.3 | — | — | 2.3 | — | |
| T Package (TO-220) | | | — | — | — | — | 2.3 | — | |
| Average (Note 7) K Package (TO-3) | | | — | — | 1.5 | — | — | 1.5 | |
| T Package (TO-220) | | | — | — | — | — | — | 1.5 | |

NOTES:

(1) $T_{low}$ = −55°C for LM150 $T_{high}$ = +150°C for LM150
−25°C for LM250 = +150°C for LM250
0°C for LM350 = +125°C for LM350
$P_{max}$ = 30 W for K suffix (TO-3)
$P_{max}$ = 25 W for T suffix (TO-220)

(2) Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(3) Selected devices with tightened tolerance reference voltage available.

(4) $C_{Adj}$, when used, is connected between the adjustment pin and ground.

(5) Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

(6) Thermal Resistance evaluated measuring the hottest temperature on the die using an infrared scanner. This method of evaluation yields very accurate thermal resistance values which are conservative when compared to other measurement techniques.

(7) The average die temperature is used to derive the value of thermal resistance junction to case (average).

SCHEMATIC DIAGRAM

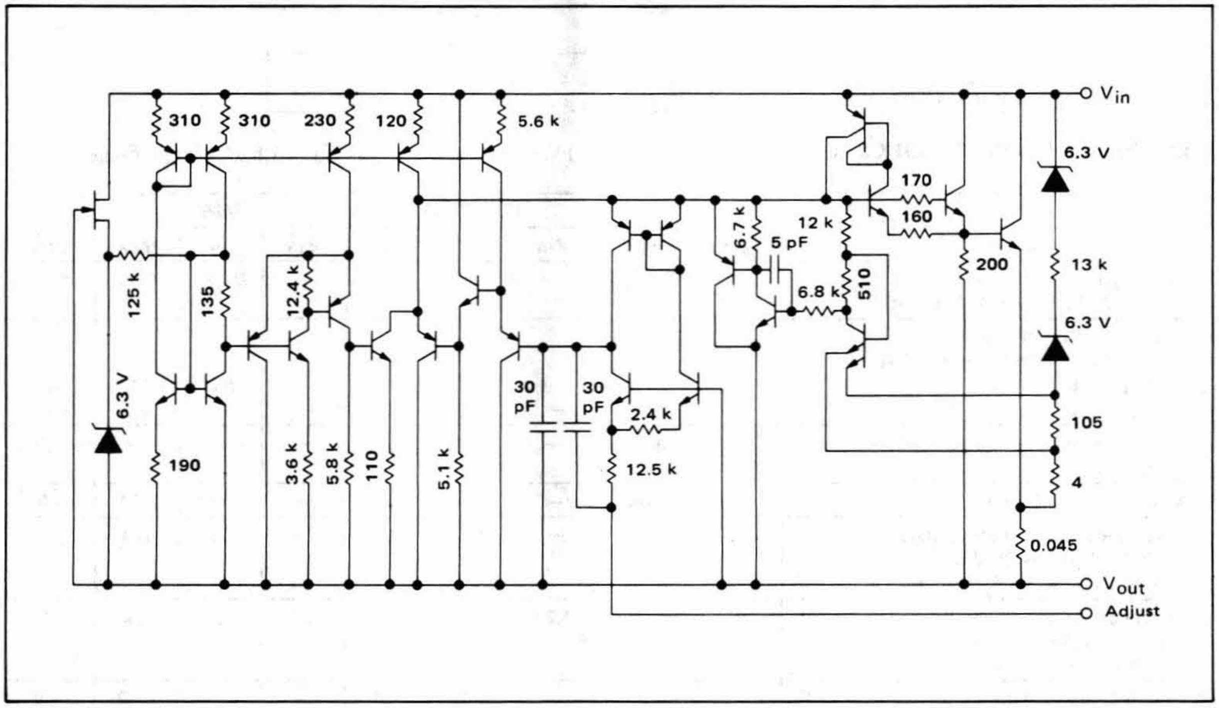
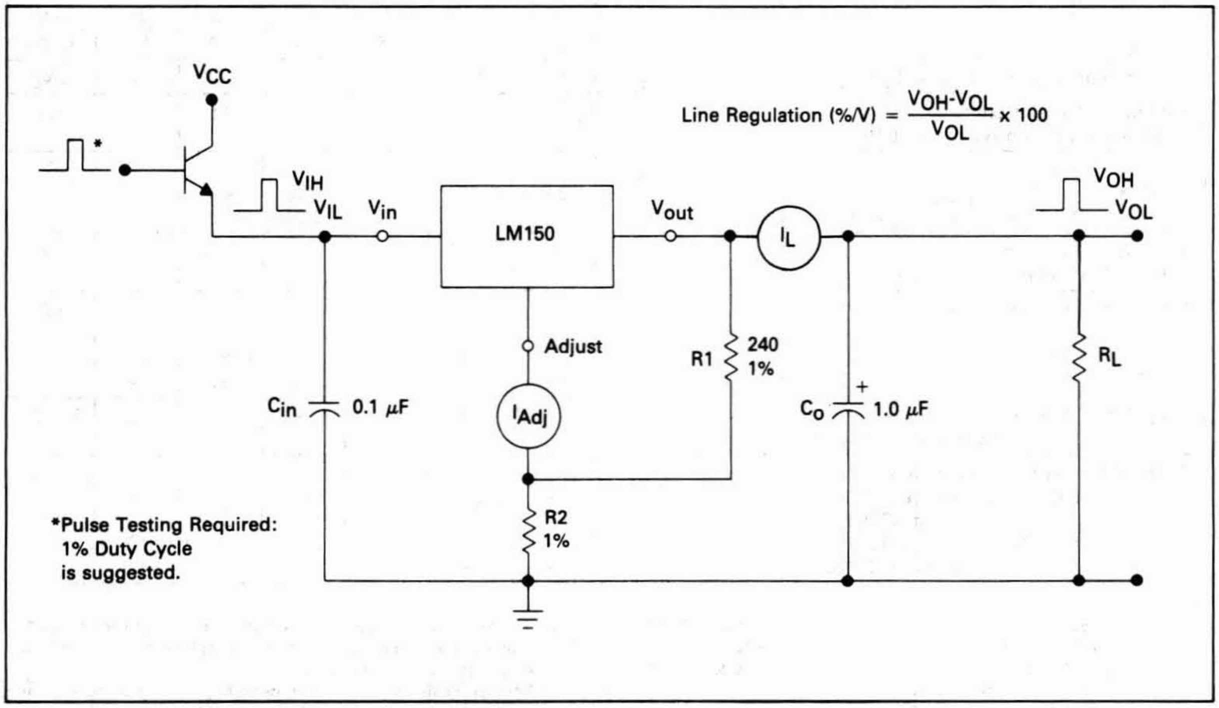

Vin
310
310
230
120
5.6 k
6.3 V
170
160
12 k
6.7 k
5 pF
200
13 k
125 k
135
12.4 k
6.8 k
510
6.3 V
6.3 V
30 pF
30 pF
2.4 k
105
190
3.6 k
5.8 k
110
5.1 k
12.5 k
4
0.045
Vout
Adjust

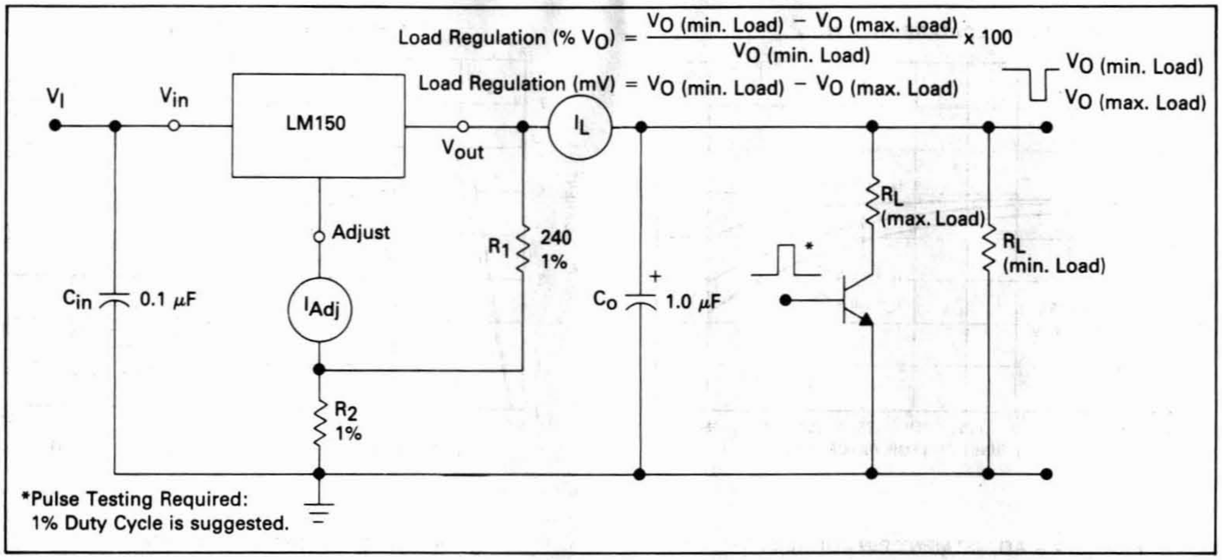
FIGURE 1 — LINE REGULATION AND $\Delta I_{Adj}$/LINE TEST CIRCUIT


VCC
*
VIH
VIL
Vin
LM150
Vout
IL
VOH
VOL
Adjust
R1
240
1%
Cin
0.1 µF
IAdj
Co
+
1.0 µF
RL
R2
1%

$$\text{Line Regulation (\%/V)} = \frac{V_{OH}-V_{OL}}{V_{OL}} \times 100$$

*Pulse Testing Required:
1% Duty Cycle
is suggested.

FIGURE 2 — LOAD REGULATION AND $\Delta I_{Adj}$/LOAD TEST CIRCUIT

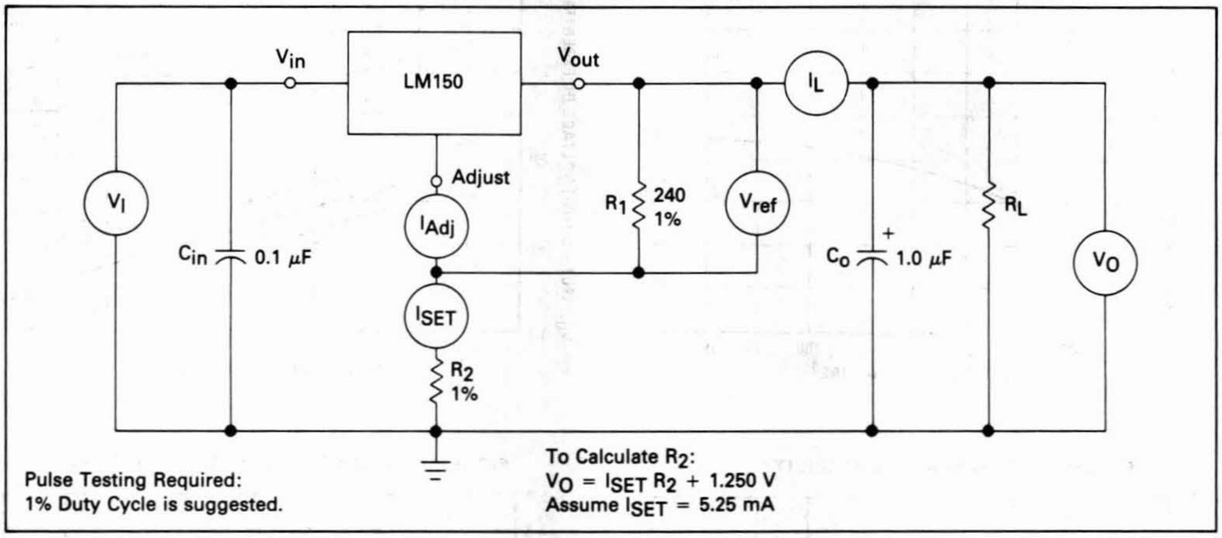

V_I
V_in
LM150
V_out
I_L
Adjust
R_1 240 1%
C_in 0.1 µF
I_Adj
C_O 1.0 µF
R_2 1%
R_L (max. Load)
R_L (min. Load)
*
V_O (min. Load)
V_O (max. Load)

$$\text{Load Regulation } (\%\ V_O) = \frac{V_O\ (\text{min. Load}) - V_O\ (\text{max. Load})}{V_O\ (\text{min. Load})} \times 100$$

$$\text{Load Regulation (mV)} = V_O\ (\text{min. Load}) - V_O\ (\text{max. Load})$$

*Pulse Testing Required:
1% Duty Cycle is suggested.

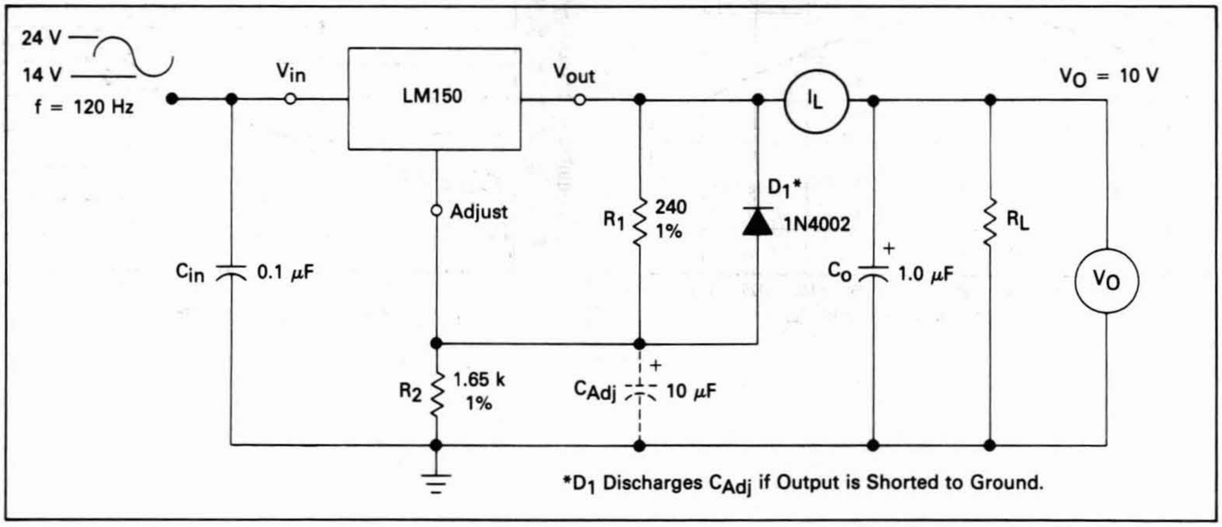
FIGURE 3 — STANDARD TEST CIRCUIT


V_in
LM150
V_out
I_L
V_I
Adjust
I_Adj
R_1 240 1%
V_ref
C_in 0.1 µF
C_O 1.0 µF
R_L
V_O
I_SET
R_2 1%

Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate $R_2$:
$V_O = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

FIGURE 4 — RIPPLE REJECTION TEST CIRCUIT


24 V
14 V
f = 120 Hz
V_in
LM150
V_out
I_L
V_O = 10 V
Adjust
R_1 240 1%
D_1* 1N4002
R_L
C_in 0.1 µF
C_O 1.0 µF
V_O
R_2 1.65 k 1%
C_Adj 10 µF

*$D_1$ Discharges $C_{Adj}$ if Output is Shorted to Ground.

FIGURE 5 — LOAD REGULATION

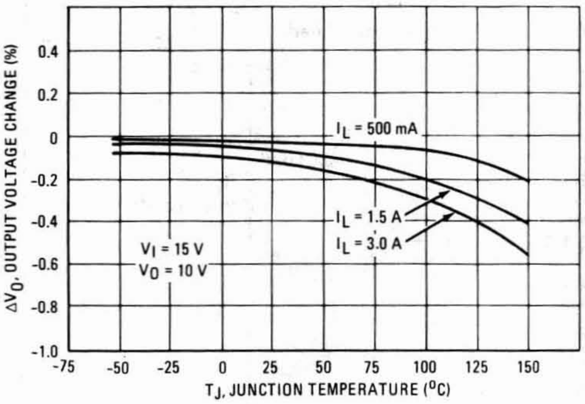


FIGURE 6 — CURRENT LIMIT

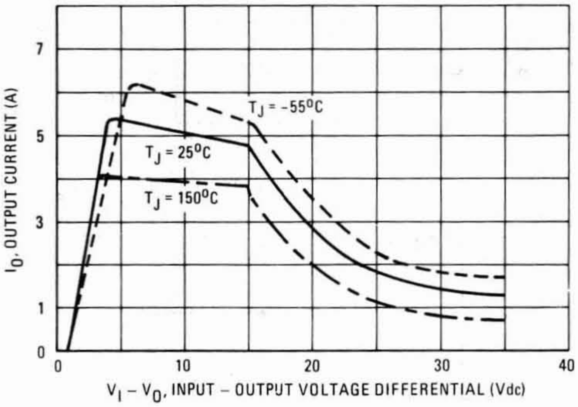


FIGURE 7 — ADJUSTMENT PIN CURRENT

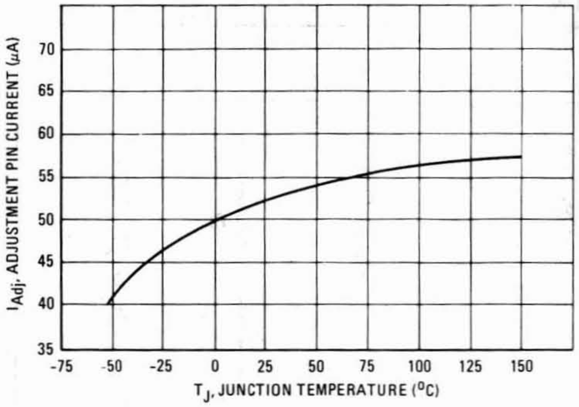


FIGURE 8 — DROPOUT VOLTAGE

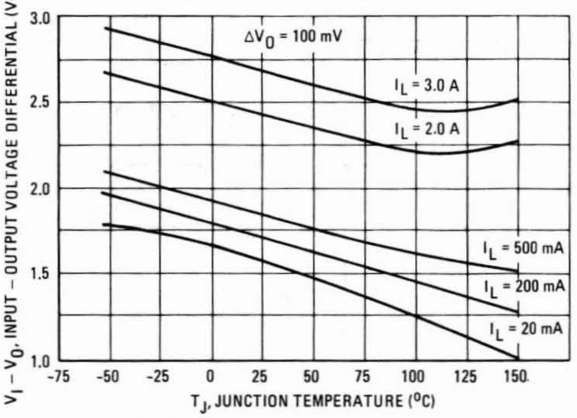


FIGURE 9 — TEMPERATURE STABILITY

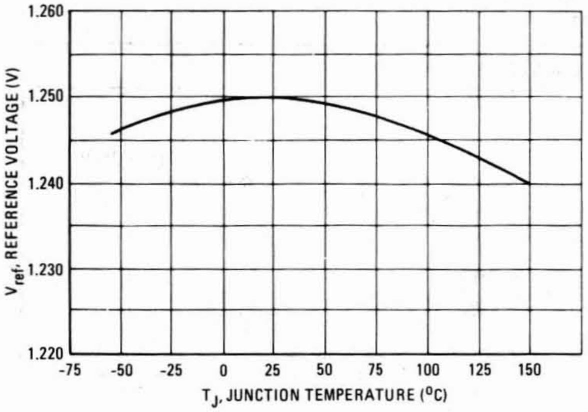


FIGURE 10 — MINIMUM OPERATING CURRENT

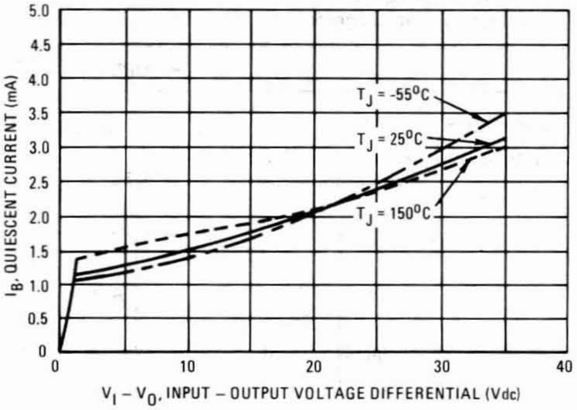


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

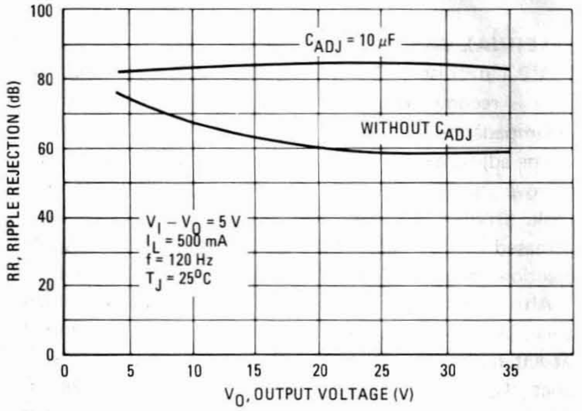


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

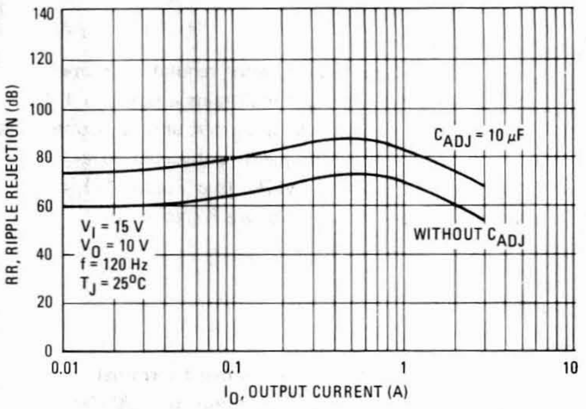


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

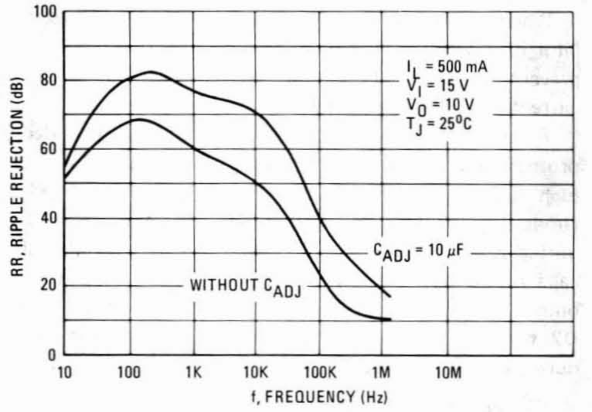


FIGURE 14 — OUTPUT IMPEDANCE

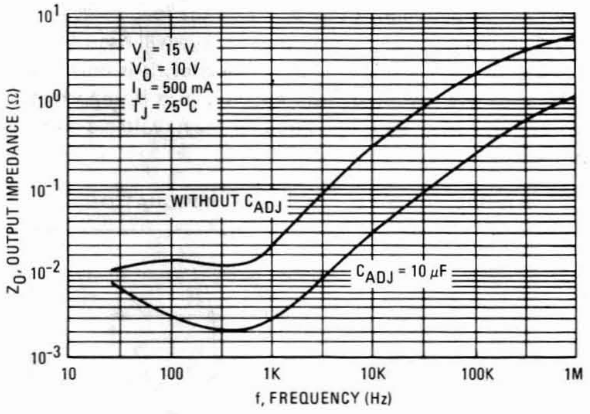


FIGURE 15 — LINE TRANSIENT RESPONSE

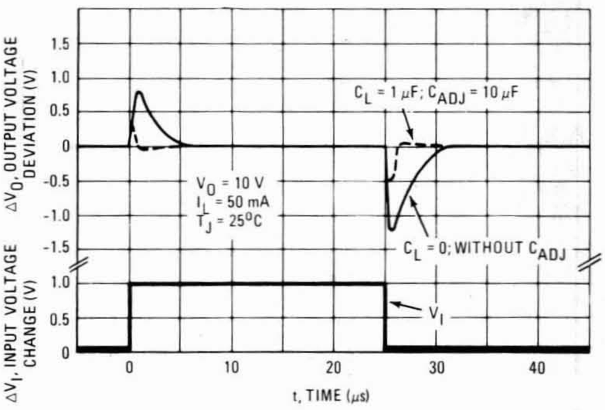
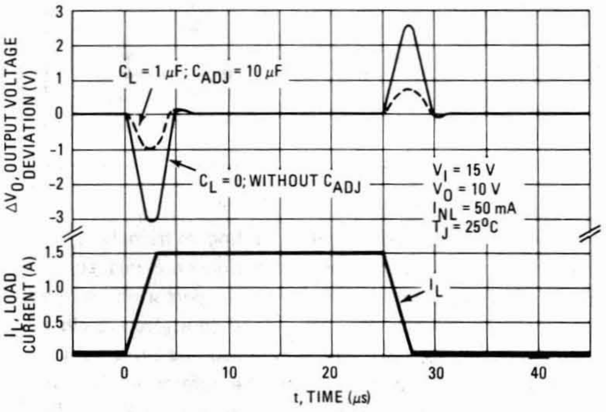


FIGURE 16 — LOAD TRANSIENT RESPONSE



## APPLICATIONS INFORMATION

### BASIC CIRCUIT OPERATION

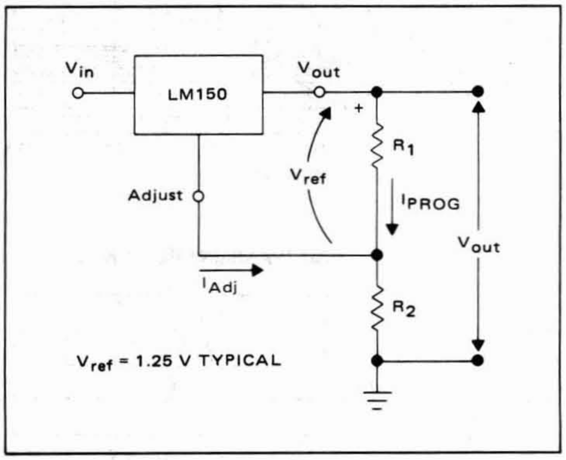
The LM150 is a 3-terminal floating regulator. In operation, the LM150 develops and maintains a nominal 1.25 volt reference ($V_{ref}$) between its output and adjustment terminals. This reference voltage is converted to a programming current ($I_{PROG}$) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref} \left(1 + \frac{R2}{R1}\right) + I_{Adj}\, R2$$

Since the current from the adjustment terminal ($I_{Adj}$) represents an error term in the equation, the LM150 was designed to control $I_{Adj}$ to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM150 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



### LOAD REGULATION

The LM150 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

### EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor ($C_{in}$) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor ($C_{ADJ}$) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM150 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance ($C_o$) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

### PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM150 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_o > 25$ μF, $C_{ADJ} > 10$ μF). Diode $D_1$ prevents $C_o$ from discharging thru the I.C. during an input short circuit. Diode $D_2$ protects against capacitor $C_{ADJ}$ discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents $C_{ADJ}$ from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

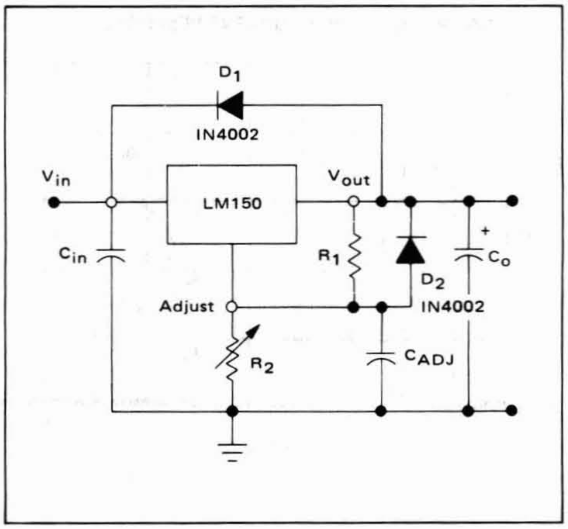
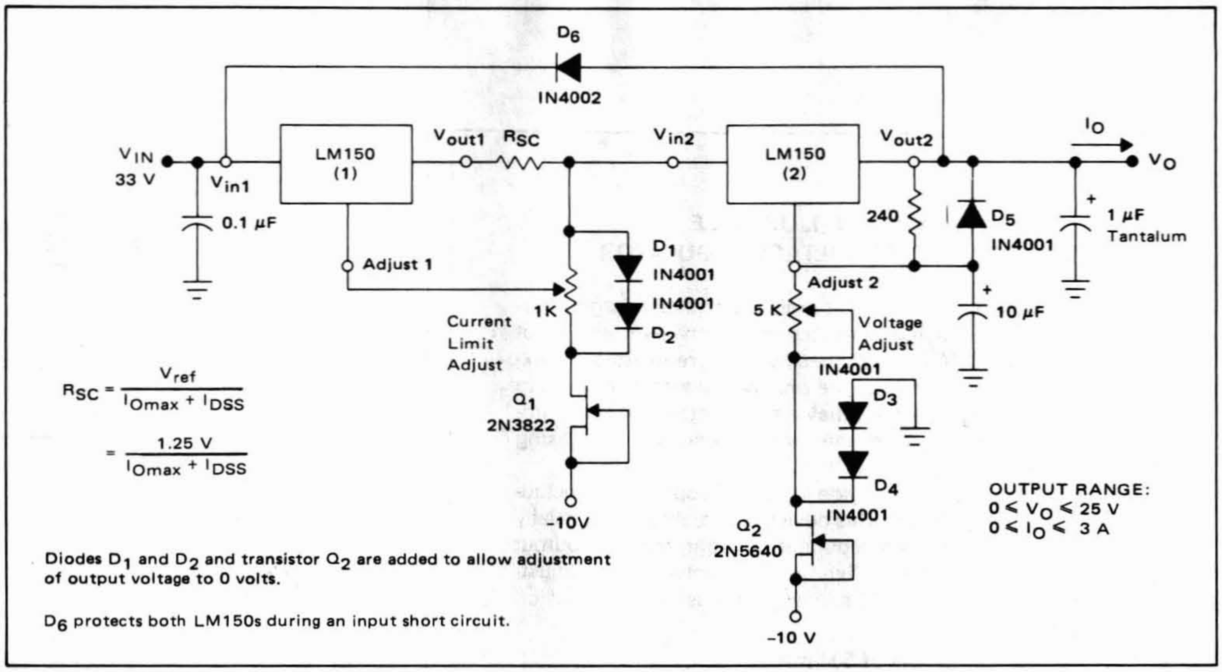


FIGURE 19 – "LABORATORY" POWER SUPPLY WITH ADJUSTABLE CURRENT LIMIT AND OUTPUT VOLTAGE


D6
IN4002
VIN
33 V
Vin1
0.1 μF
LM150
(1)
Vout1
RSC
Vin2
LM150
(2)
Vout2
IO
VO
240
D5
IN4001
1 μF
Tantalum
Adjust 1
D1
IN4001
IN4001
D2
1K
Current
Limit
Adjust
Q1
2N3822
-10V
Adjust 2
5 K
Voltage
Adjust
10 μF
IN4001
D3
D4
IN4001
Q2
2N5640
-10 V

$$R_{SC} = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

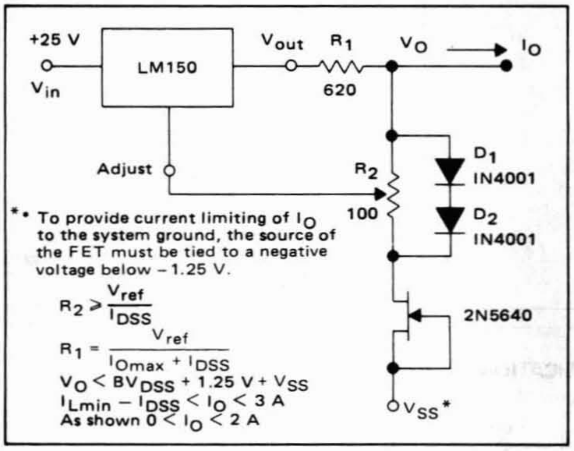
$$= \frac{1.25\ V}{I_{Omax} + I_{DSS}}$$

OUTPUT RANGE:
$0 \leqslant V_O \leqslant 25$ V
$0 \leqslant I_O \leqslant 3$ A

Diodes $D_1$ and $D_2$ and transistor $Q_2$ are added to allow adjustment of output voltage to 0 volts.

$D_6$ protects both LM150s during an input short circuit.

FIGURE 20 – ADJUSTABLE CURRENT LIMITER


+25 V
Vin
LM150
Vout
R1
620
VO
IO
Adjust
R2
100
D1
IN4001
D2
IN4001
2N5640
VSS*

** To provide current limiting of $I_O$ to the system ground, the source of the FET must be tied to a negative voltage below − 1.25 V.

$R_2 \geqslant \frac{V_{ref}}{I_{DSS}}$

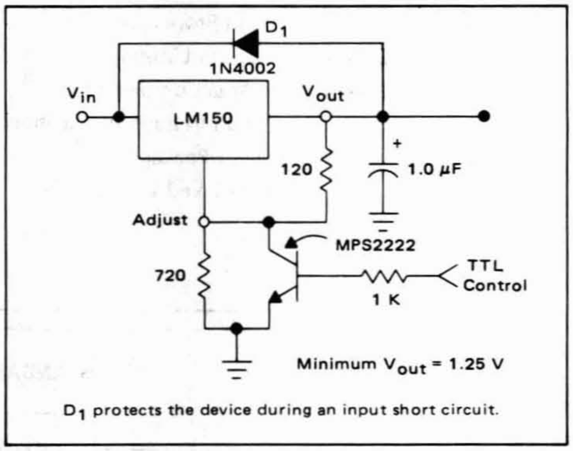
$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$

$V_O < BV_{DSS} + 1.25\ V + V_{SS}$

$I_{Lmin} - I_{DSS} < I_O < 3$ A

As shown $0 < I_O < 2$ A

FIGURE 21 – 5 V ELECTRONIC SHUT DOWN REGULATOR


D1
1N4002
Vin
LM150
Vout
120
1.0 μF
Adjust
MPS2222
720
1 K
TTL
Control

Minimum $V_{out}$ = 1.25 V

$D_1$ protects the device during an input short circuit.

FIGURE 22 – SLOW TURN-ON REGULATOR

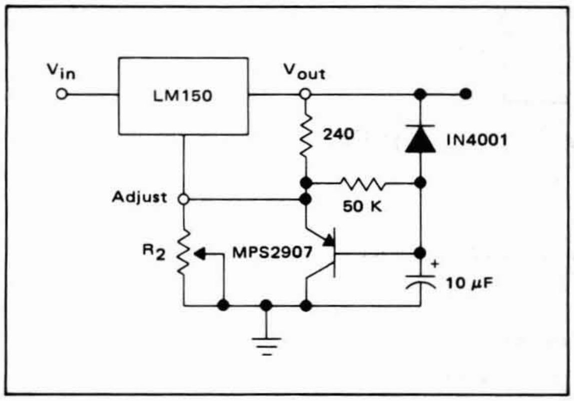
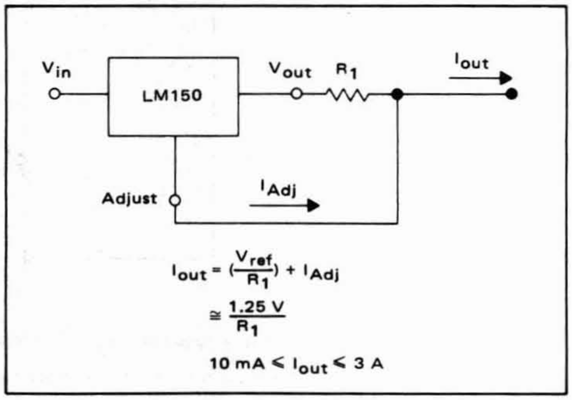

Vin
LM150
Vout
240
IN4001
Adjust
50 K
R2
MPS2907
10 μF

FIGURE 23 – CURRENT REGULATOR


Vin
LM150
Vout
R1
Iout
Adjust
IAdj

$$I_{out} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj}$$

$$\cong \frac{1.25\ V}{R_1}$$

$$10\ mA \leqslant I_{out} \leqslant 3\ A$$

**MOTOROLA**

# LM317M

## 3-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

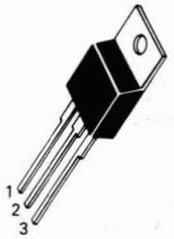
The LM317M are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 500 mA over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM317M series serve a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317M series can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

## MEDIUM-CURRENT 3-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



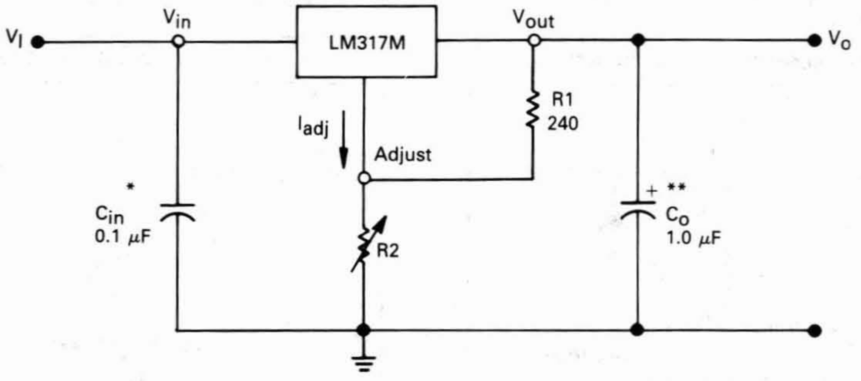
Pin 1. Adjust
2. $V_{out}$
3. $V_{in}$

**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220AB

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| LM317MT | $T_J$ = 0°C to +125°C | Plastic Power |

**STANDARD APPLICATION**



*$C_{in}$ is required if regulator is located in appreciable distance from power supply filter.

**$C_O$ is not needed for stability, however it does improve transient response.

$$V_O = 1.25\ \text{V}\ (1 + \frac{R_2}{R_1}) + I_{adj} R_2$$

Since $I_{adj}$ is controlled to less than 100 μA, the error associated with this term is negligible in most applications.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input-Output Voltage Differential | $V_I$-$V_O$ | 40 | Vdc |
| Power Dissipation | $P_D$ | Internally Limited | |
| Operating Junction Temperature Range | $T_J$ | 0 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

## ELECTRICAL CHARACTERISTICS

($V_I - V_O$ = 5.0 V, $I_O$ = 0.1 A, $T_J = T_{low}$ to $T_{high}$ [see Note 1], $P_{max}$ per Note 2, unless otherwise specified.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Line Regulation (Note 3)<br>$T_A$ = 25°C, 3.0 V ≤ $V_I - V_O$ ≤ 40 V | 1 | $Reg_{line}$ | — | 0.01 | 0.04 | %/V |
| Load Regulation (Note 3)<br>$T_A$ = 25°C, 10 mA ≤ $I_O$ ≤ 0.5 A | 2 | $Reg_{load}$ | | | | |
| $V_O$ ≤ 5.0 V | | | — | 5.0 | 25 | mV |
| $V_O$ ≥ 5.0 V | | | — | 0.1 | 0.5 | % $V_O$ |
| Adjustment Pin Current | 3 | $I_{adj}$ | — | 50 | 100 | μA |
| Adjustment Pin Current Change<br>2.5 V ≤ $V_I - V_O$ ≤ 40 V, 10 mA ≤ $I_L$ ≤ 0.5 A, $P_D$ ≤ $P_{max}$ | 1,2 | $\Delta I_{adj}$ | — | 0.2 | 5.0 | μA |
| Reference Voltage (Note 4)<br>3.0 V ≤ $V_I - V_O$ ≤ 40 V, 10 mA ≤ $I_O$ ≤ 0.5 A, $P_D$ ≤ $P_{max}$ | 3 | $V_{ref}$ | 1.20 | 1.25 | 1.30 | V |
| Line Regulation (Note 3)<br>3.0 V ≤ $V_I - V_O$ ≤ 40 V | 1 | $Reg_{line}$ | — | 0.02 | 0.07 | %/V |
| Load Regulation (Note 3)<br>10 mA ≤ $I_O$ ≤ 0.5 A | 2 | $Reg_{load}$ | | | | |
| $V_O$ ≤ 5.0 V | | | — | 20 | 70 | mV |
| $V_O$ ≥ 5.0 V | | | — | 0.3 | 1.5 | % $V_O$ |
| Temperature Stability ($T_{low}$ ≤ $T_J$ ≤ $T_{high}$) | 3 | $T_S$ | — | 0.7 | — | % $V_O$ |
| Minimum Load Current to Maintain Regulation<br>($V_I - V_O$ = 40 V) | 3 | $I_{Lmin}$ | — | 3.5 | 10 | mA |
| Maximum Output Current | 3 | $I_{max}$ | | | | A |
| $V_I - V_O$ ≤ 15 V, $P_D$ ≤ $P_{max}$ | | | 0.5 | 0.9 | — | |
| $V_I - V_O$ = 40 V, $P_D$ ≤ $P_{max}$, $T_A$ = 25°C | | | 0.15 | 0.25 | — | |
| RMS Noise, % of $V_O$<br>$T_A$ = 25°C, 10 Hz ≤ f ≤ 10 kHz | — | N | — | 0.003 | — | % $V_O$ |
| Ripple Rejection, $V_O$ = 10 V, f = 120 Hz (Note 5) | 4 | RR | | | | dB |
| Without $C_{adj}$ | | | — | 65 | — | |
| $C_{adj}$ = 10 μF | | | 66 | 80 | — | |
| Long Term Stability, $T_J = T_{high}$ (Note 6)<br>$T_A$ = 25°C for Endpoint Measurements | 3 | S | — | 0.3 | 1.0 | %/1.0 k Hrs. |
| Thermal Resistance Junction to Case | — | $R_{\theta JC}$ | — | 7.0 | — | °C/W |

NOTES:

(1) $T_{low}$ to $T_{high}$ = 0°C to +125°C

(2) $P_{max}$ = 7.5 W

(3) Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) $C_{adj}$, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

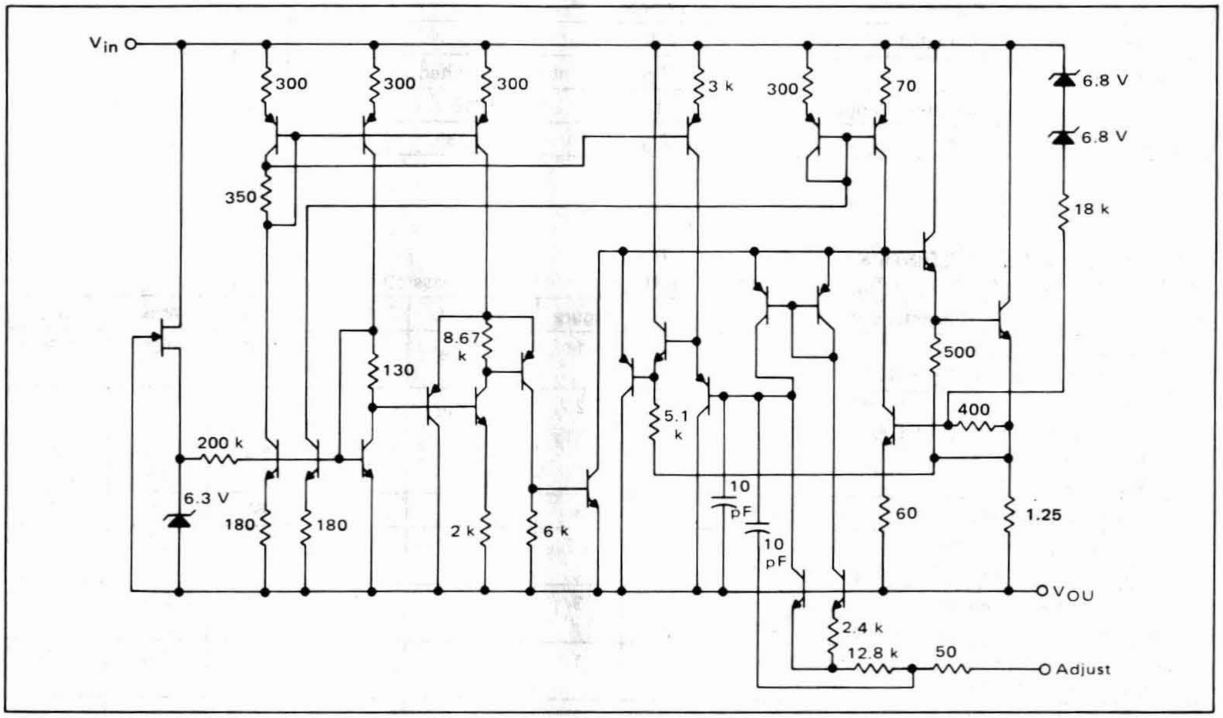
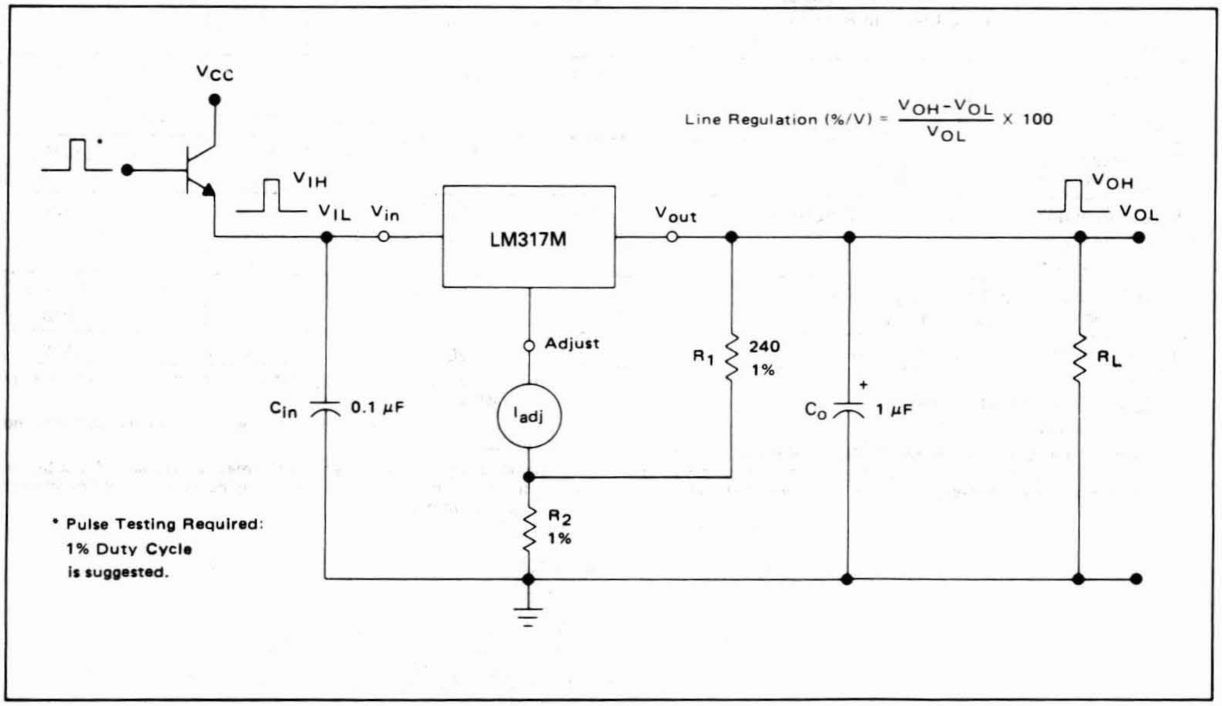

V_in
300
300
300
3 k
300
70
6.8 V
6.8 V
350
18 k
8.67 k
130
500
5.1 k
400
200 k
6.3 V
180
180
2 k
6 k
10 pF
10 pF
60
1.25
V_OUT
2.4 k
12.8 k
50
Adjust

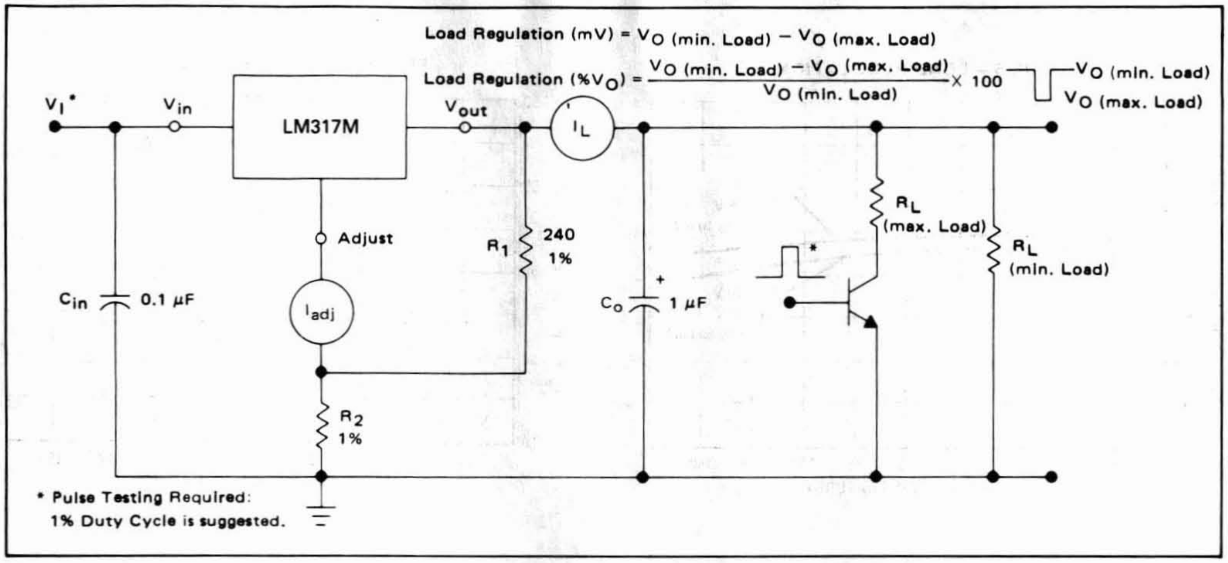
FIGURE 1 – LINE REGULATION AND $\Delta I_{Adj}$/LINE TEST CIRCUIT


V_CC
*
V_IH
V_IL
V_in
LM317M
V_out
V_OH
V_OL
Adjust
I_adj
R_1
240
1%
C_in
0.1 µF
C_O
+
1 µF
R_L
R_2
1%

Line Regulation (%/V) = $\frac{V_{OH} - V_{OL}}{V_{OL}} \times 100$

* Pulse Testing Required:
1% Duty Cycle
is suggested.

FIGURE 2 – LOAD REGULATION AND $\Delta I_{Adj}$/LOAD TEST CIRCUIT



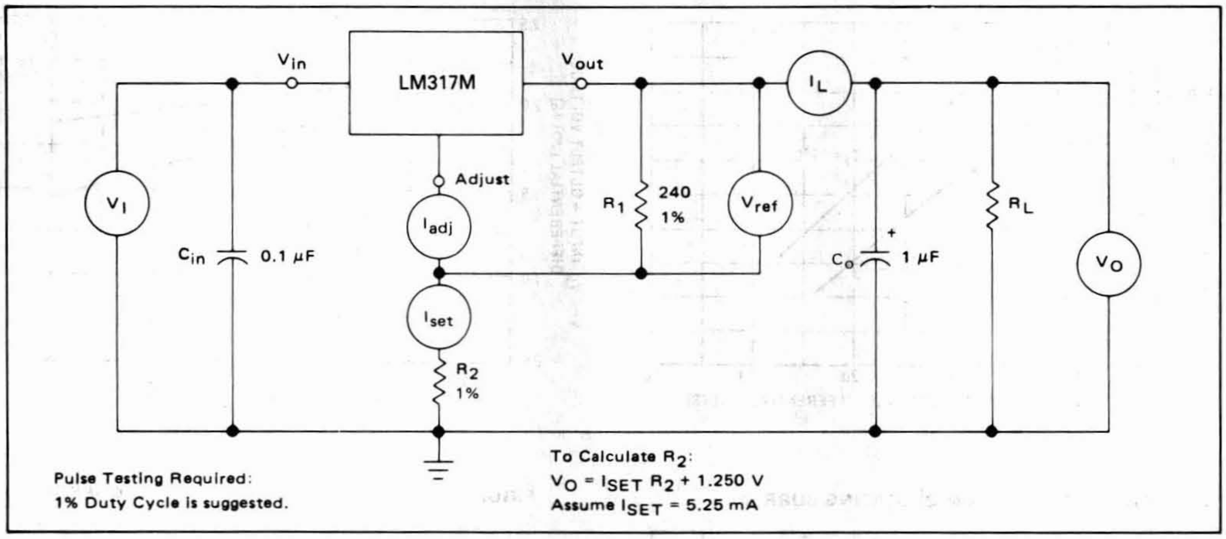
Load Regulation (mV) = $V_O$ (min. Load) − $V_O$ (max. Load)

Load Regulation (%$V_O$) = $\frac{V_O \text{ (min. Load)} - V_O \text{ (max. Load)}}{V_O \text{ (min. Load)}} \times 100$

$V_O$ (min. Load)
$V_O$ (max. Load)
$V_I$*
$V_{in}$
LM317M
$V_{out}$
$I_L$
Adjust
$R_1$
240
1%
$I_{adj}$
$C_{in}$
0.1 µF
$C_o$
+
1 µF
*
$R_L$
(max. Load)
$R_L$
(min. Load)
$R_2$
1%

* Pulse Testing Required:
1% Duty Cycle is suggested.

FIGURE 3 – STANDARD TEST CIRCUIT

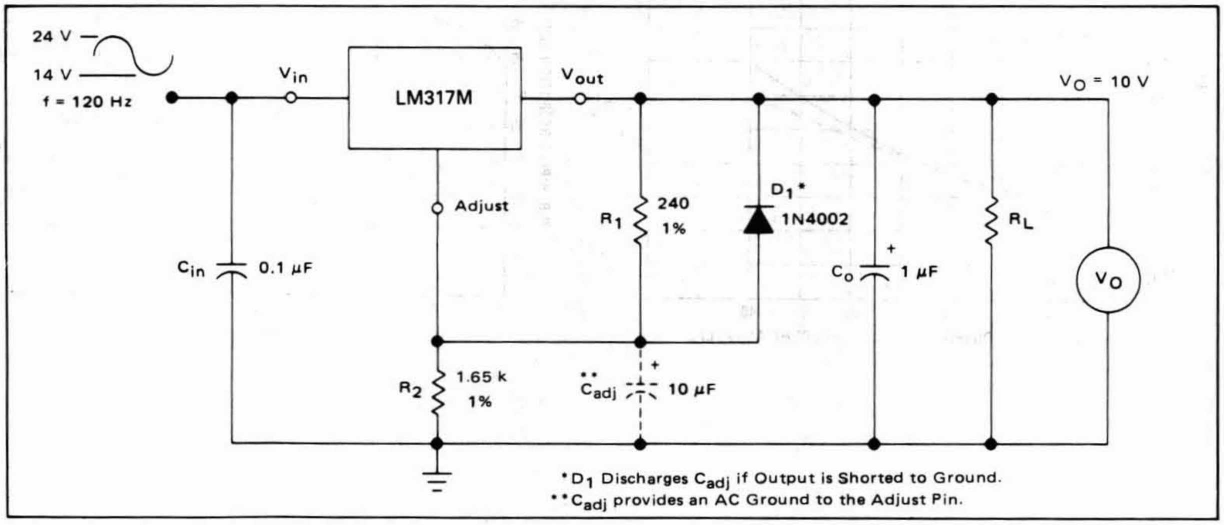


$V_{in}$
LM317M
$V_{out}$
$I_L$
$V_I$
Adjust
$I_{adj}$
$C_{in}$
0.1 µF
$R_1$
240
1%
$V_{ref}$
$C_o$
+
1 µF
$R_L$
$V_O$
$I_{set}$
$R_2$
1%

Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate $R_2$:
$V_O = I_{SET} R_2 + 1.250$ V
Assume $I_{SET}$ = 5.25 mA

FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT



24 V
14 V
f = 120 Hz
$V_{in}$
LM317M
$V_{out}$
$V_O$ = 10 V
Adjust
$R_1$
240
1%
$D_1$*
1N4002
$C_{in}$
0.1 µF
$C_o$
+
1 µF
$R_L$
$V_O$
$R_2$
1.65 k
1%
**
$C_{adj}$
+
10 µF

*$D_1$ Discharges $C_{adj}$ if Output is Shorted to Ground.
**$C_{adj}$ provides an AC Ground to the Adjust Pin.

FIGURE 5 – LOAD REGULATION

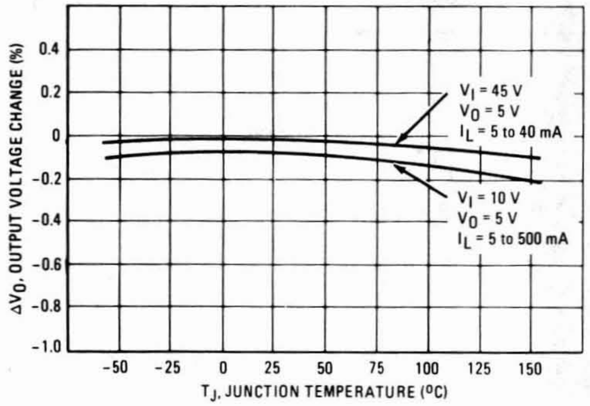


FIGURE 6 – RIPPLE REJECTION

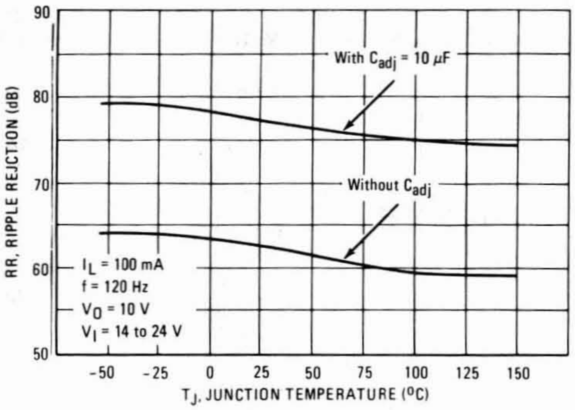


FIGURE 7 – CURRENT LIMIT

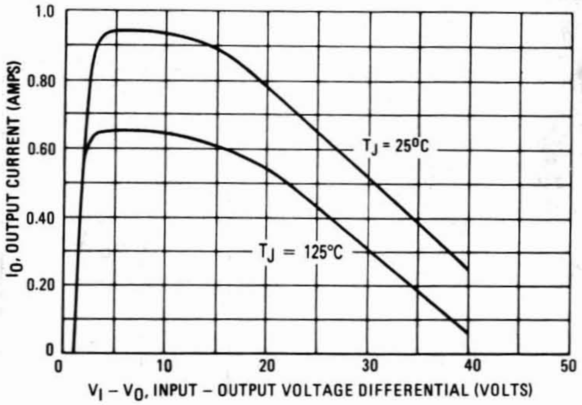


FIGURE 8 – DROPOUT VOLTAGE

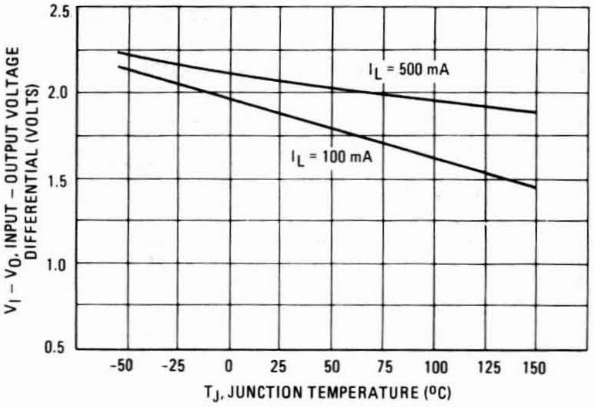


FIGURE 9 – MINIMUM OPERATING CURRENT

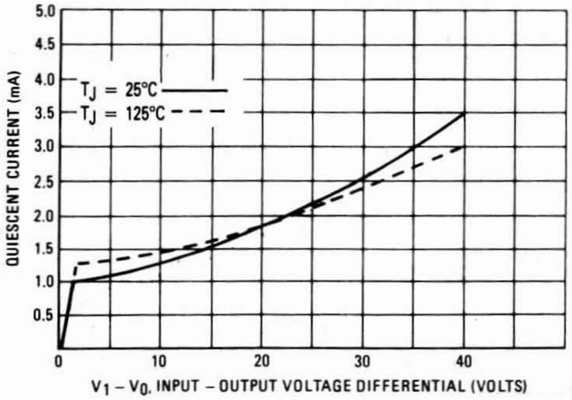


FIGURE 10 – RIPPLE REJECTION versus FREQUENCY

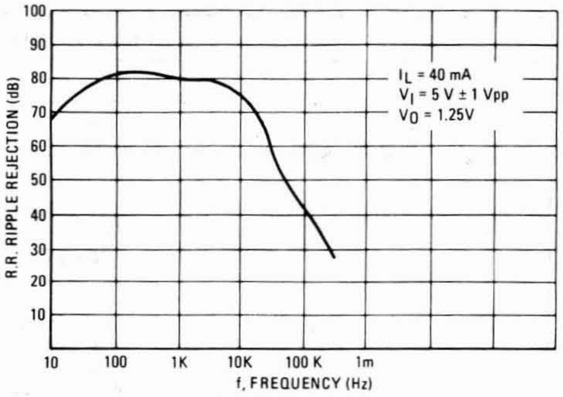


**FIGURE 11 – TEMPERATURE STABILITY**

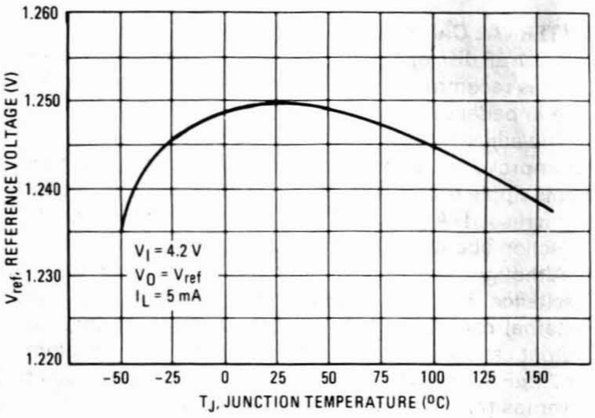


**FIGURE 12 – ADJUSTMENT PIN CURRENT**

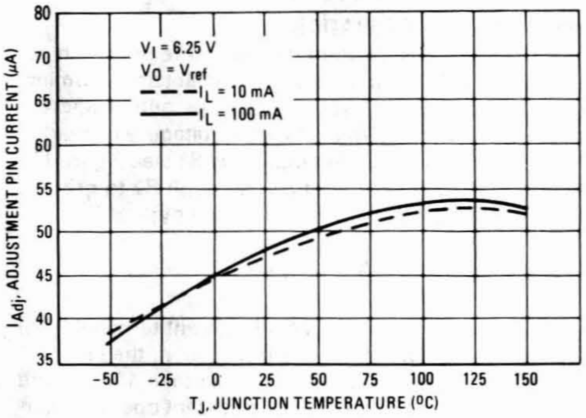


**FIGURE 13 – LINE REGULATION**

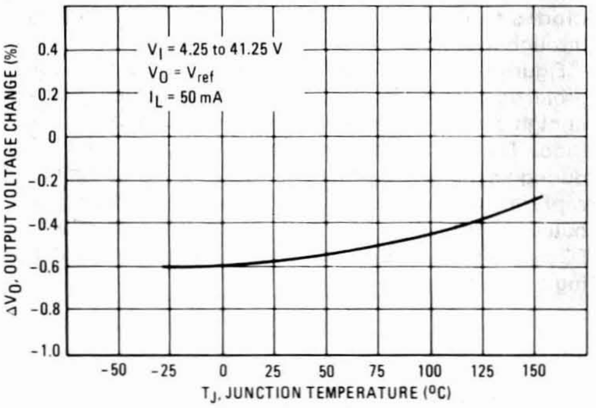


**FIGURE 14 – OUTPUT NOISE**

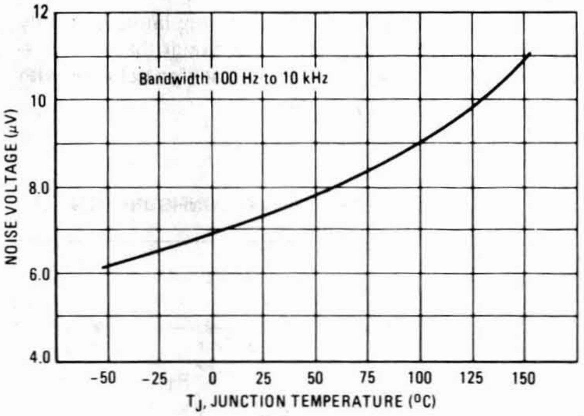


**FIGURE 15 – LINE TRANSIENT RESPONSE**

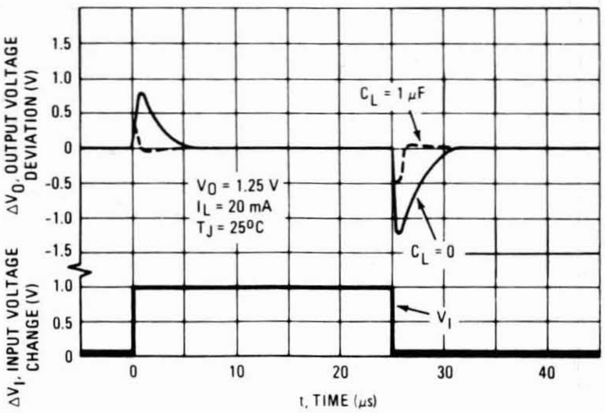
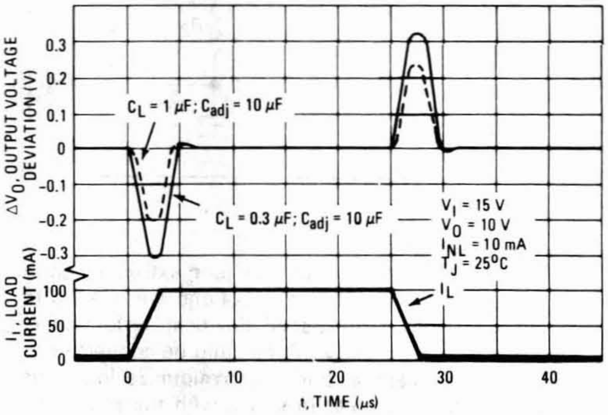


**FIGURE 16 – LOAD TRANSIENT RESPONSE**



## APPLICATIONS INFORMATION

### BASIC CIRCUIT OPERATION

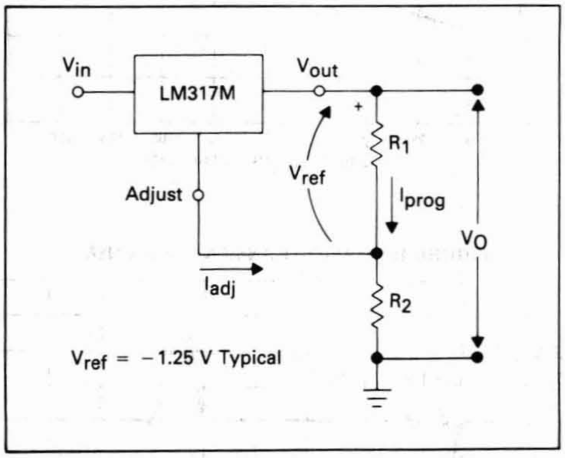
The LM317M is a 3-terminal floating regulator. In operation, the LM317M develops and maintains a nominal 1.25 volt reference ($V_{ref}$) between its output and adjustment terminals. This reference voltage is converted to a programming current ($I_{prog}$) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_O = V_{ref}\,(1 + \frac{R2}{R1}) + I_{adj}R2$$

Since the current from the adjustment terminal ($I_{adj}$) represents an error term in the equation, the LM317M was designed to control $I_{adj}$ to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317M is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 — BASIC CIRCUIT CONFIGURATION



### LOAD REGULATION

The LM317M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

### EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor ($C_{in}$) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor ($C_{adj}$) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

Although the LM317M is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance ($C_O$) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

### PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capcitors from discharging through low current points into the regulator.

Figure 18 shows the LM317M with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25$ μF, $C_{adj} > 5.0$ μF). Diode D1 prevents $C_O$ from discharging thru the I.C. during an input short circuit. Diode D2 protects against capacitor $C_{adj}$ discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents $C_{adj}$ from discharging through the I.C. during an input short circuit.

FIGURE 18 — VOLTAGE REGULATOR WITH PROTECTION DIODES

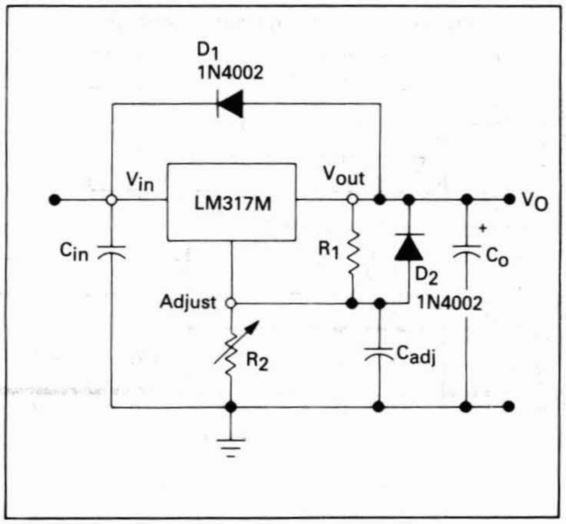
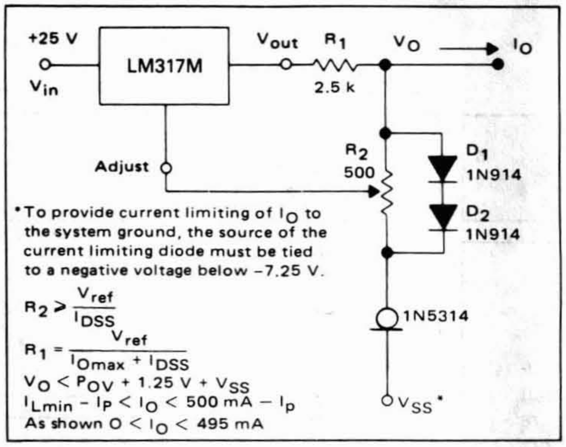


FIGURE 19 – ADJUSTABLE CURRENT LIMITER


+25 V
$V_{in}$
LM317M
$V_{out}$
$R_1$
2.5 k
$V_O$
$I_O$
Adjust
$R_2$
500
$D_1$
1N914
$D_2$
1N914
1N5314
$V_{SS}$*

*To provide current limiting of $I_O$ to the system ground, the source of the current limiting diode must be tied to a negative voltage below −7.25 V.

$R_2 \geqslant \frac{V_{ref}}{I_{DSS}}$

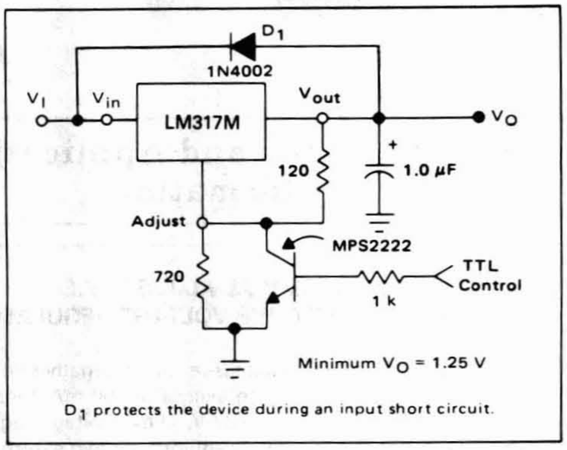
$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$

$V_O < P_{OV} + 1.25\ V + V_{SS}$

$I_{Lmin} - I_P < I_O < 500\ mA - I_p$

As shown $0 < I_O < 495$ mA

FIGURE 20 – 5 V ELECTRONIC SHUTDOWN REGULATOR


$D_1$
1N4002
$V_I$
$V_{in}$
LM317M
$V_{out}$
$V_O$
+
120
1.0 µF
Adjust
MPS2222
720
TTL Control
1 k

Minimum $V_O$ = 1.25 V

$D_1$ protects the device during an input short circuit.

FIGURE 21 – SLOW TURN-ON REGULATOR

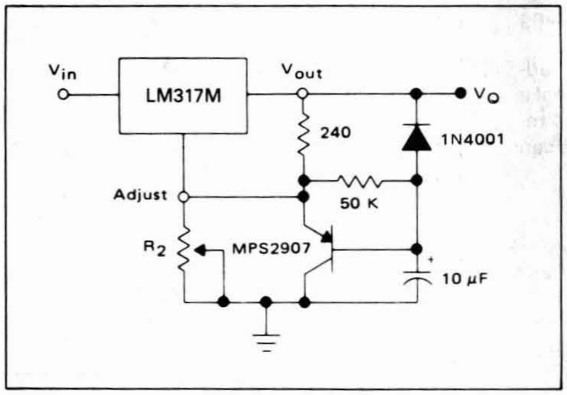
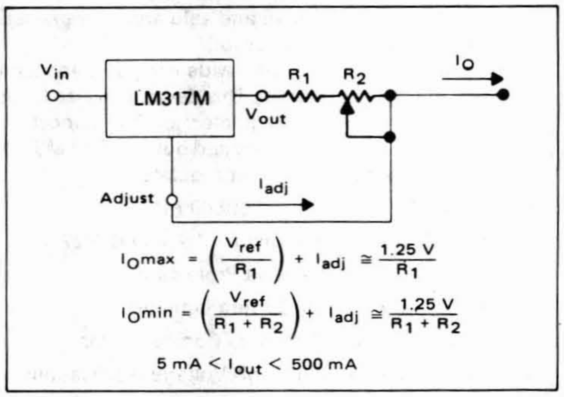

$V_{in}$
LM317M
$V_{out}$
$V_O$
240
1N4001
Adjust
50 K
$R_2$
MPS2907
+
10 µF

FIGURE 22 – CURRENT REGULATOR


$V_{in}$
LM317M
$R_1$
$R_2$
$I_O$
$V_{out}$
$I_{adj}$
Adjust

$$I_{Omax} = \left(\frac{V_{ref}}{R_1}\right) + I_{adj} \cong \frac{1.25\ V}{R_1}$$

$$I_{Omin} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{adj} \cong \frac{1.25\ V}{R_1 + R_2}$$

5 mA < $I_{out}$ < 500 mA

**MOTOROLA**

# LM337M

## Specifications and Applications Information

### MEDIUM-CURRENT 3-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

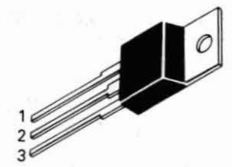
SILICON MONOLITHIC INTEGRATED CIRCUIT

### 3-TERMINAL ADJUSTABLE OUTPUT NEGATIVE VOLTAGE REGULATOR

The LM337M are adjustable 3-terminal negative voltage regulators capable of supplying in excess of 500 mA over an output voltage range of −1.2 V to −37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM337M series serve a wide variety of applications including local, on-card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM337M series can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable Between −1.2 V and −37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages



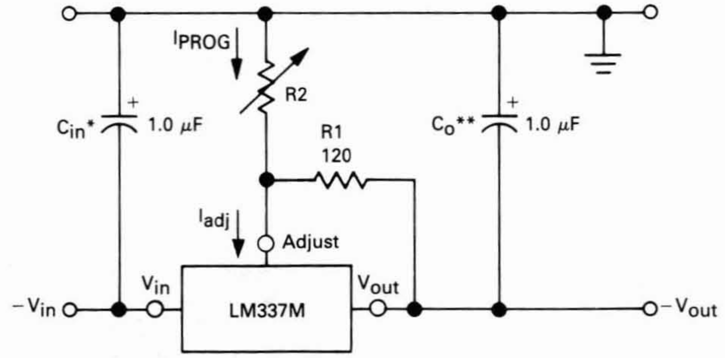
Pin 1. Adjust
2. $V_{in}$
3. $V_{out}$

**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220B

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| LM337MT | $T_J$ = 0°C to +125°C | Plastic Power |

**STANDARD APPLICATION**



*$C_{in}$ is required if regulator is located more than 4 inches from power supply filter. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommended.

**$C_O$ is necessary for stability. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommended.

$$V_{out} = -1.25\text{ V}\left(1 + \frac{R2}{R1}\right)$$

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input-Output Voltage Differential | $V_I$-$V_O$ | 40 | Vdc |
| Power Dissipation | $P_D$ | Internally Limited | |
| Operating Junction Temperature Range | $T_J$ | 0 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

## ELECTRICAL CHARACTERISTICS

($\lvert V_I - V_O \rvert$ = 5.0 V, $I_O$ = 0.1; $T_J$ = $T_{low}$ to $T_{high}$ [see Note 1], $P_{max}$ per Note 2, unless otherwise specified.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Line Regulation (Note 3)<br>$T_A$ = 25°C, 3.0 V ≤ $\lvert V_I - V_O \rvert$ ≤ 40 V | 1 | $Reg_{line}$ | — | 0.01 | 0.04 | %/V |
| Load Regulation (Note 3)<br>$T_A$ = 25°C, 10 mA ≤ $I_O$ ≤ 0.5 A | 2 | $Reg_{load}$ | | | | |
| $\lvert V_O \rvert$ ≤ 5.0 V | | | — | 15 | 50 | mV |
| $\lvert V_O \rvert$ ≥ 5.0 V | | | — | 0.3 | 1.0 | % $V_O$ |
| Thermal Regulation<br>10 ms Pulse, $T_A$ = 25°C | — | $Reg_{therm}$ | — | 0.03 | 0.04 | %$V_O$/W |
| Adjustment Pin Current | 3 | $I_{adj}$ | — | 65 | 100 | µA |
| Adjustment Pin Current Change<br>2.5 V ≤ $\lvert V_I - V_O \rvert$ ≤ 40 V, 10 mA ≤ $I_L$ ≤ 0.5 A,<br>$P_D$ ≤ $P_{max}$, $T_A$ = 25°C | 1,2 | $\Delta I_{adj}$ | — | 2.0 | 5.0 | µA |
| Reference Voltage (Note 4)<br>3.0 V ≤ $\lvert V_I - V_O \rvert$ ≤ 40 V, 10 mA ≤ $I_O$ ≤ 0.5 A, | 3 | $V_{ref}$ | | | | V |
| $P_D$ ≤ $P_{max}$, $T_A$ = 25°C | | | −1.213 | −1.250 | −1.287 | |
| $T_{low}$ to $T_{high}$ | | | −1.20 | −1.25 | −1.30 | |
| Line Regulation (Note 3)<br>3.0 V ≤ $\lvert V_I - V_O \rvert$ ≤ 40 V | 1 | $Reg_{line}$ | — | 0.02 | 0.07 | %/V |
| Load Regulation (Note 3)<br>10 mA ≤ $I_O$ ≤ 0.5 A | 2 | $Reg_{load}$ | | | | |
| $\lvert V_O \rvert$ ≤ 5.0 V | | | — | 20 | 70 | mV |
| $\lvert V_O \rvert$ ≥ 5.0 V | | | — | 0.3 | 1.5 | % $V_O$ |
| Temperature Stability ($T_{low}$ ≤ $T_J$ ≤ $T_{high}$) | 3 | $T_S$ | — | 0.6 | — | % $V_O$ |
| Minimum Load Current to | 3 | $I_{Lmin}$ | | | | mA |
| Maintain Regulation ($\lvert V_I - V_O \rvert$ ≤ 10 V) | | | — | 1.5 | 6.0 | |
| ($\lvert V_I - V_O \rvert$ ≤ 40 V) | | | — | 2.5 | 10 | |
| Maximum Output Current | 3 | $I_{max}$ | | | | A |
| $\lvert V_I - V_O \rvert$ ≤ 15 V, $P_D$ ≤ $P_{max}$ | | | 0.5 | 0.9 | — | |
| $\lvert V_I - V_O \rvert$ = 40 V, $P_D$ ≤ $P_{max}$, $T_A$ = 25°C | | | 0.1 | 0.25 | — | |
| RMS Noise, % of $V_O$<br>$T_A$ = 25°C, 10 Hz ≤ f ≤ 10 kHz | — | N | — | 0.003 | — | % $V_O$ |
| Ripple Rejection, $V_O$ = −10 V, f = 120 Hz (Note 5) | 4 | RR | | | | dB |
| Without $C_{adj}$ | | | — | 60 | — | |
| $C_{adj}$ = 10 µF | | | 66 | 77 | — | |
| Long Term Stability, $T_J$ = $T_{high}$ (Note 6)<br>$T_A$ = 25°C for Endpoint Measurements | 3 | S | — | 0.3 | 1.0 | %/1.0 k Hrs. |
| Thermal Resistance Junction to Case | — | $R_{\theta JC}$ | — | 7.0 | — | °C/W |

NOTES:

(1) $T_{low}$ to $T_{high}$ = 0°C to +125°C

(2) $P_{max}$ = 7.5 W

(3) Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) $C_{adj}$, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

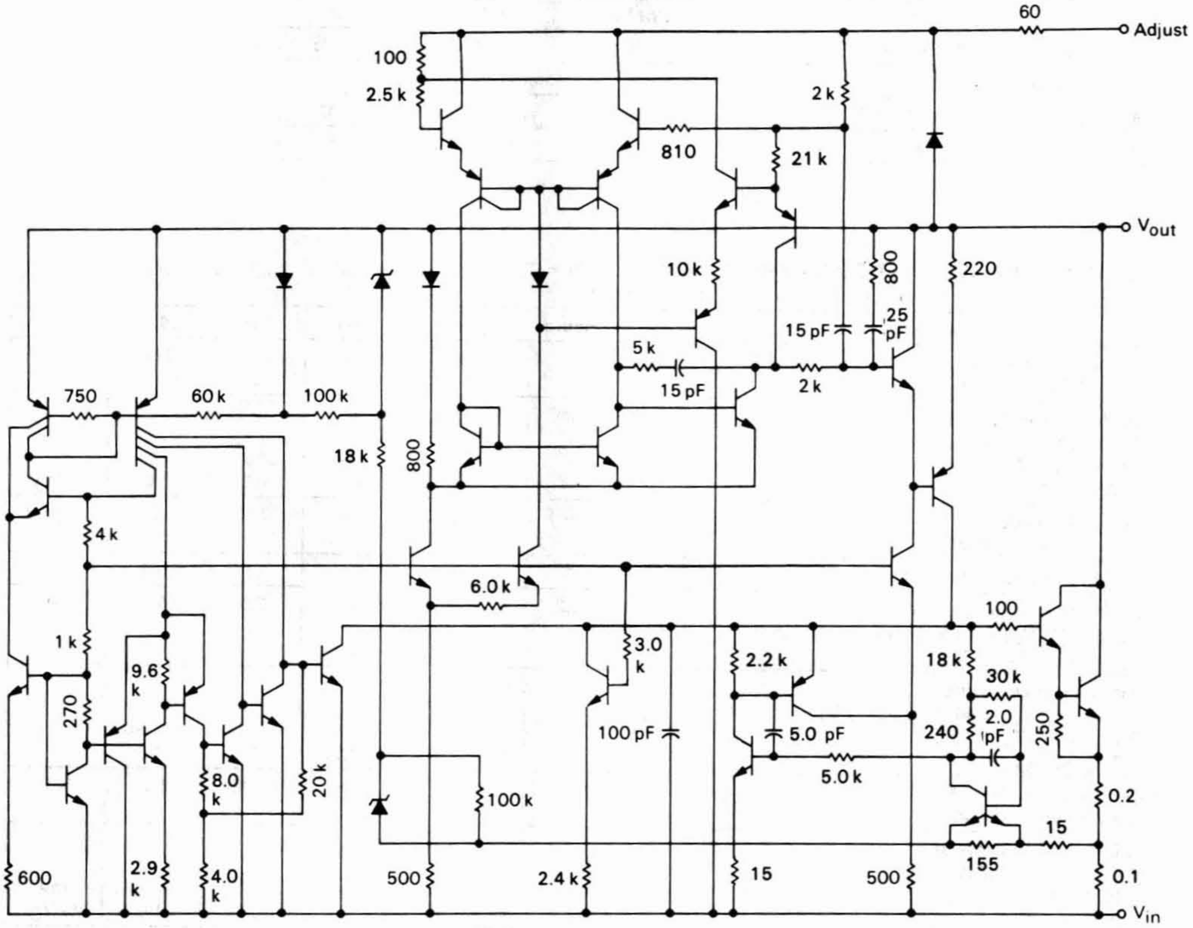
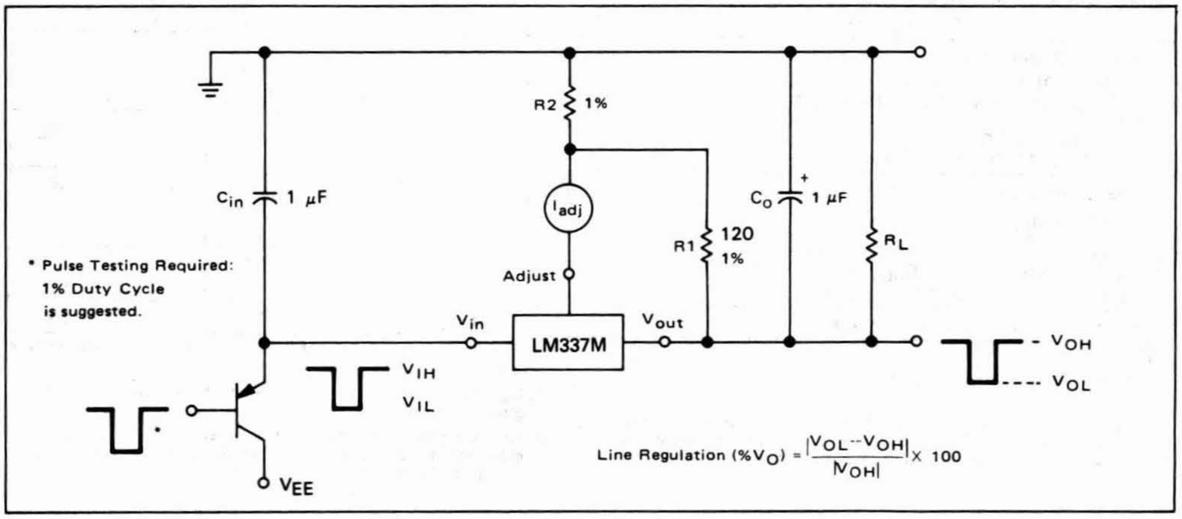

60
Adjust
100
2.5 k
2 k
810
21 k
Vout
10 k
800
220
15 pF
25 pF
5 k
15 pF
2 k
750
60 k
100 k
18 k
800
4 k
6.0 k
1 k
9.6 k
270
3.0 k
2.2 k
18 k
30 k
2.0 pF
240
250
100 pF
5.0 pF
5.0 k
8.0 k
20 k
100 k
0.2
15
155
600
2.9 k
4.0 k
500
2.4 k
15
500
0.1
Vin

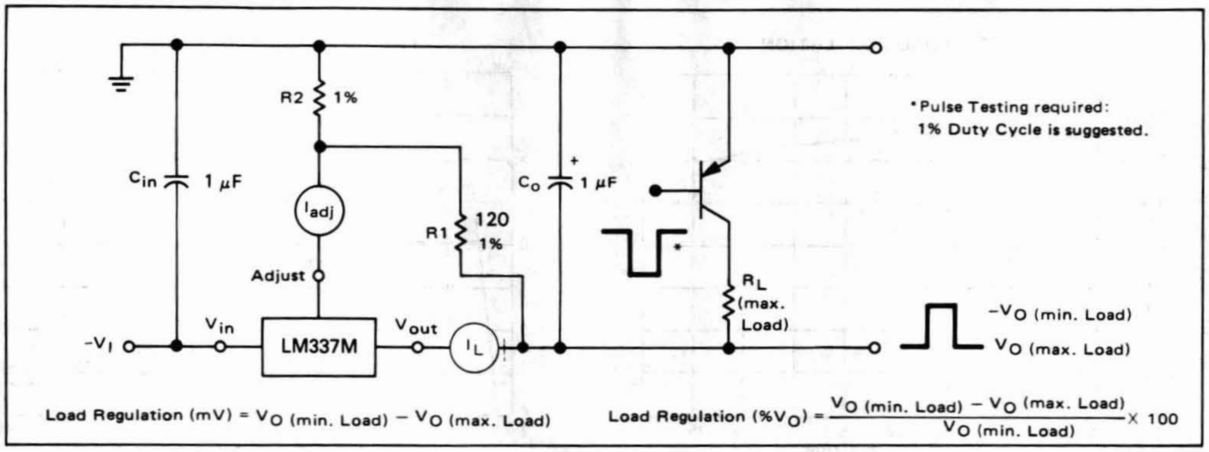
FIGURE 1 – LINE REGULATION AND $\Delta I_{adj}$/LINE TEST CIRCUIT


R2 1%
Cin 1 μF
Iadj
Adjust
Co 1 μF
R1 120 1%
RL
Vin
LM337M
Vout
VIH
VIL
VOH
VOL
VEE

* Pulse Testing Required:
1% Duty Cycle
is suggested.

$$\text{Line Regulation } (\%V_O) = \frac{|V_{OL} - V_{OH}|}{|V_{OH}|} \times 100$$

FIGURE 2 – LOAD REGULATION AND $\Delta I_{adj}$/LOAD TEST CIRCUIT

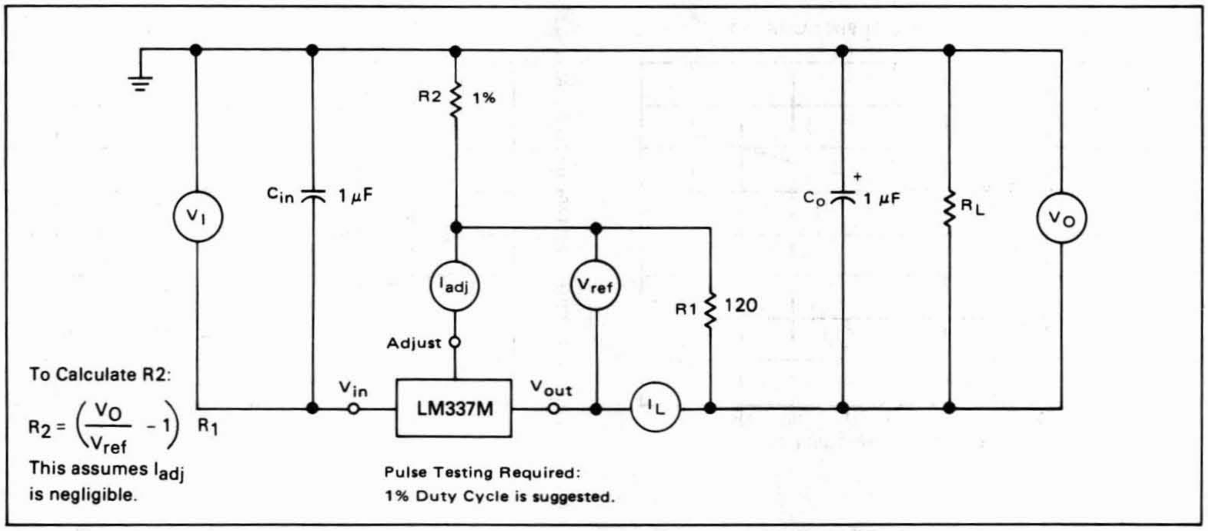

R2 1%
$C_{in}$ 1 μF
$I_{adj}$
R1 120 1%
Adjust
$C_O$ 1 μF
+
$R_L$ (max. Load)
$-V_I$
$V_{in}$
LM337M
$V_{out}$
$I_L$
$-V_O$ (min. Load)
$V_O$ (max. Load)

*Pulse Testing required: 1% Duty Cycle is suggested.

Load Regulation (mV) = $V_O$ (min. Load) − $V_O$ (max. Load)

$$\text{Load Regulation } (\%V_O) = \frac{V_O \text{ (min. Load)} - V_O \text{ (max. Load)}}{V_O \text{ (min. Load)}} \times 100$$

FIGURE 3 – STANDARD TEST CIRCUIT


R2 1%
$V_I$
$C_{in}$ 1 μF
$I_{adj}$
$V_{ref}$
R1 120
Adjust
$V_{in}$
LM337M
$V_{out}$
$I_L$
$C_O$ 1 μF
+
$R_L$
$V_O$

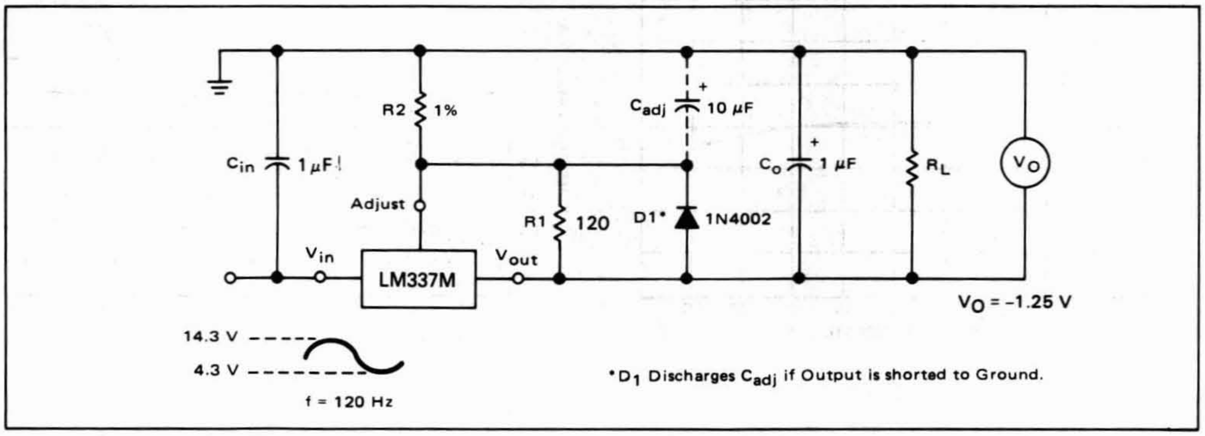
To Calculate R2:

$$R_2 = \left(\frac{V_O}{V_{ref}} - 1\right) R_1$$

This assumes $I_{adj}$ is negligible.

Pulse Testing Required: 1% Duty Cycle is suggested.

FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT


R2 1%
$C_{in}$ 1 μF
Adjust
$V_{in}$
LM337M
$V_{out}$
R1 120
$C_{adj}$ 10 μF
+
D1* 1N4002
$C_O$ 1 μF
+
$R_L$
$V_O$
14.3 V
4.3 V
f = 120 Hz

$V_O = -1.25$ V

*$D_1$ Discharges $C_{adj}$ if Output is shorted to Ground.

FIGURE 5 – LOAD REGULATION

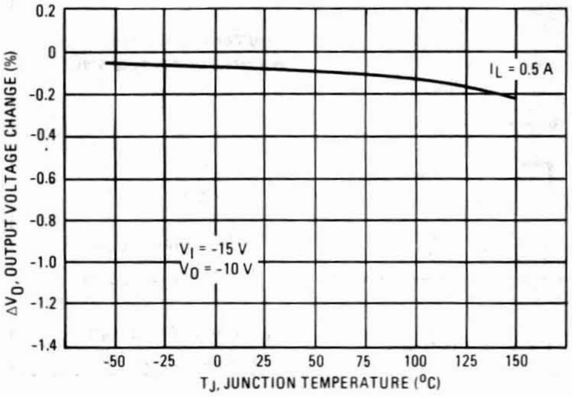


FIGURE 6 – CURRENT LIMIT

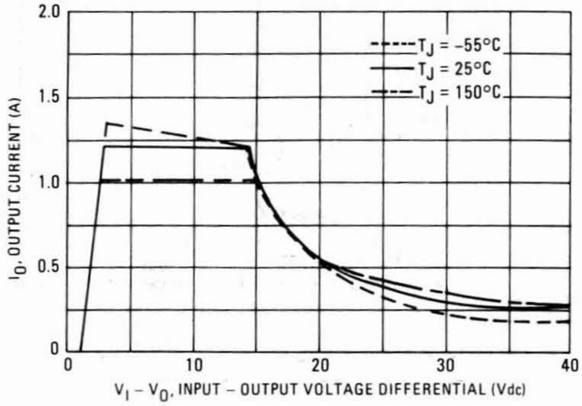


FIGURE 7 – ADJUSTMENT PIN CURRENT

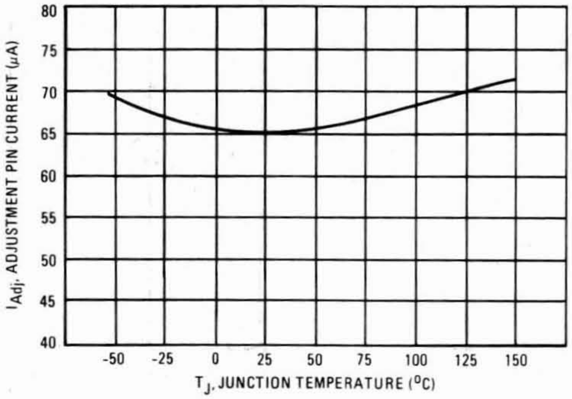


FIGURE 8 – DROPOUT VOLTAGE

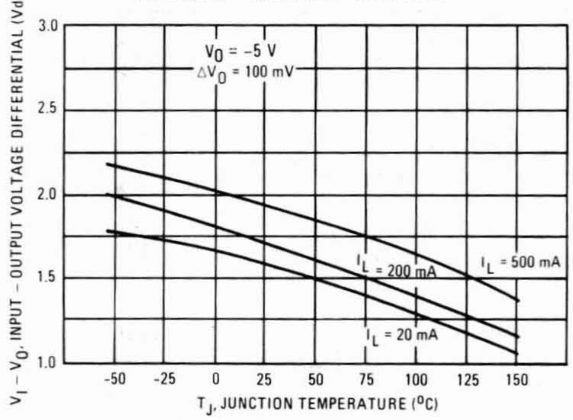


FIGURE 9 – TEMPERATURE STABILITY

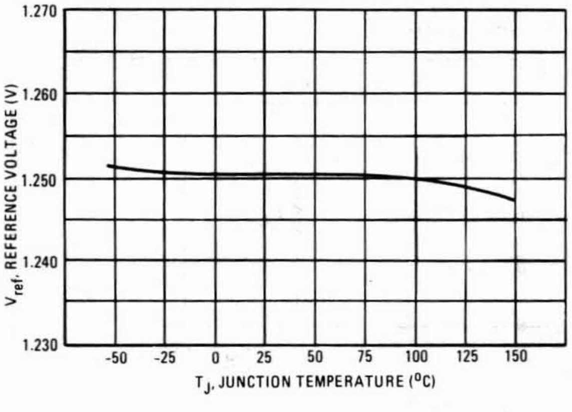


FIGURE 10 – MINIMUM OPERATING CURRENT

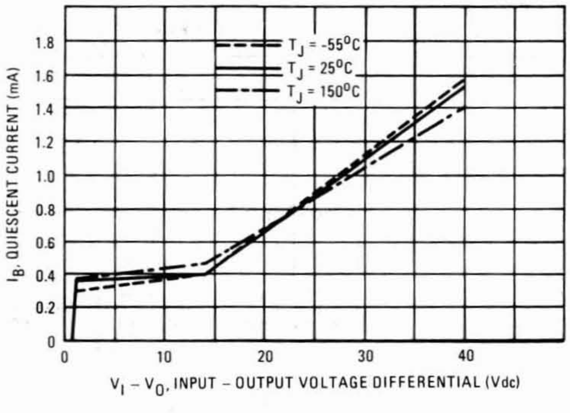


FIGURE 11 – RIPPLE REJECTION VS OUTPUT VOLTAGE

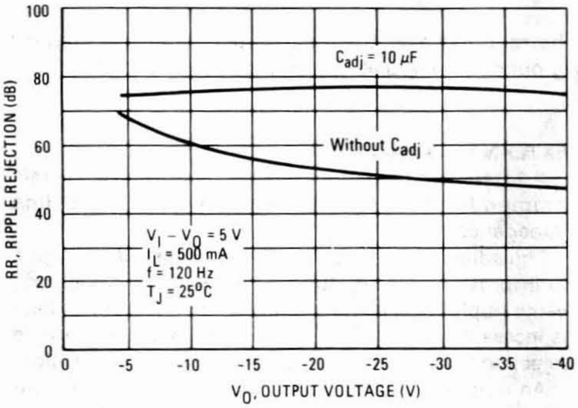


FIGURE 12 – RIPPLE REJECTION VS. OUTPUT CURRENT

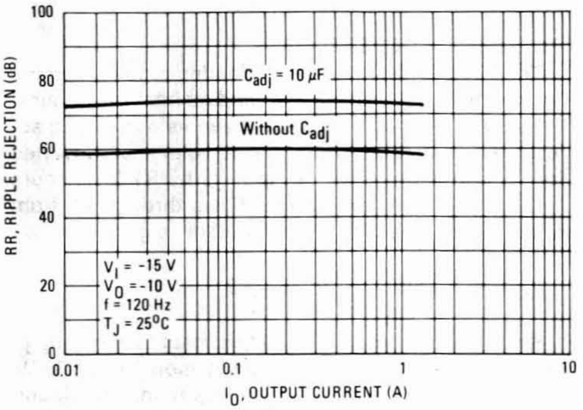


FIGURE 13 – RIPPLE REJECTION VS. FREQUENCY

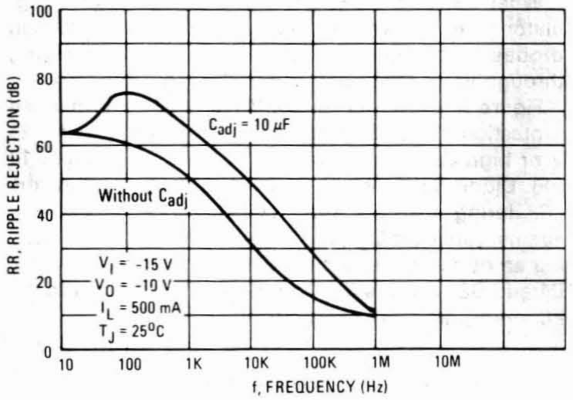


FIGURE 14 – OUTPUT IMPEDANCE

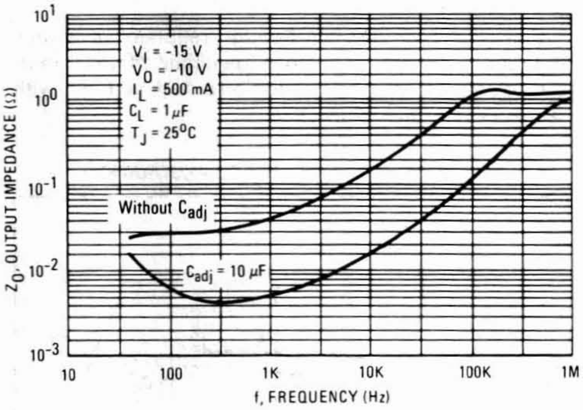


FIGURE 15 – LINE TRANSIENT RESPONSE

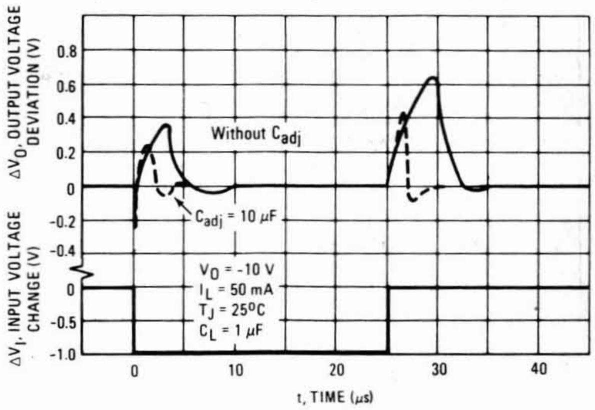
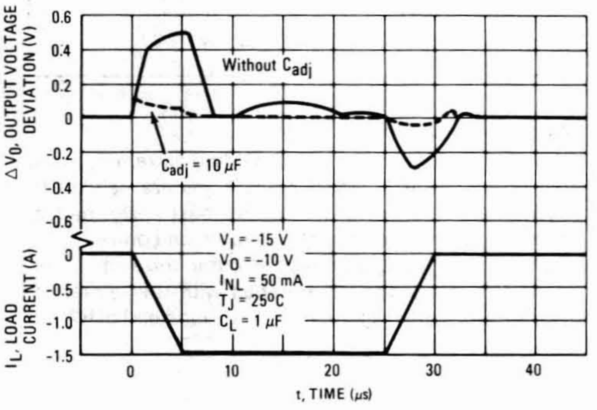


FIGURE 16 – LOAD TRANSIENT RESPONSE



## APPLICATIONS INFORMATION

### BASIC CIRCUIT OPERATION

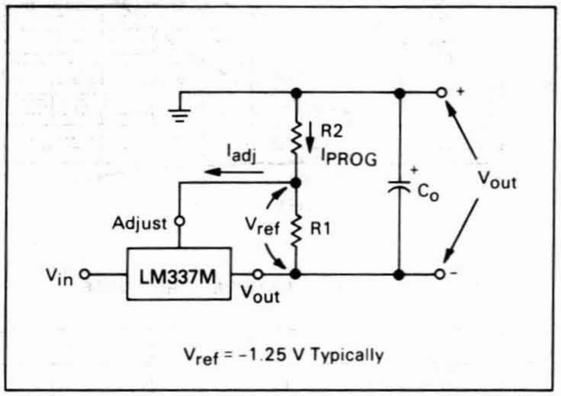
The LM337M is a 3-terminal floating regulator. In operation, the LM337M develops and maintains a nominal −1.25 volt reference ($V_{ref}$) between its output and adjustment terminals. This reference voltage is converted to a programming current ($I_{PROG}$) by R1 (see Figure 17), and this constant current flows through R2 from ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{adj}R2$$

Since the current into the adjustment terminal ($I_{adj}$) represents an error term in the equation, the LM337M was designed to control $I_{adj}$ to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will increase.

Since the LM337M is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17— BASIC CIRCUIT CONFIGURATION



$V_{ref}$ = −1.25 V Typically

### LOAD REGULATION

The LM337M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

### EXTERNAL CAPACITORS

A 1.0 μF tantalum input bypass capacitor ($C_{in}$) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor ($C_{adj}$) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

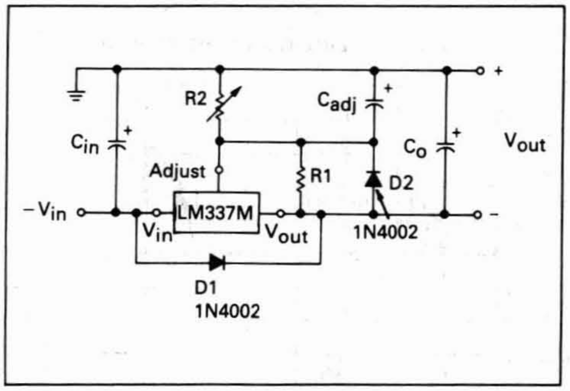
An output capacitor ($C_o$) in the form of a 1.0 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability.

### PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337M with the recommended protection diodes for output voltages in excess of −25 V or high capacitance values ($C_o > 25$ μF, $C_{adj} > 10$ μF). Diode $D_1$ prevents $C_o$ from discharging thru the I.C. during an input short circuit. Diode $D_2$ protects against capacitor $C_{adj}$ discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents $C_{adj}$ from discharging through the I.C. during an input short circuit.

FIGURE 18— VOLTAGE REGULATOR WITH PROTECTION DIODES



**MOTOROLA**

# MC1466L
# MC1566L

## Specifications and Applications Information

### MONOLITHIC VOLTAGE AND CURRENT REGULATOR

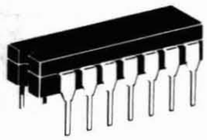
This unique "floating" regulator can deliver hundreds of volts — limited only by the breakdown voltage of the external series pass transistor. Output voltage and output current are adjustable. The MC1466/MC1566 integrated circuit voltage and current regulator is designed to give "laboratory" power-supply performance.

- Voltage/Current Regulation with Automatic Crossover
- Excellent Line Voltage Regulation, 0.02% +1.0 mV
- Excellent Load Voltage Regulation, 0.01% +1.0 mV
- Excellent Current Regulation, 0.1% +1.0 mA
- Short-Circuit Protection
- Output Voltage Adjustable to Zero Volts
- Internal Reference Voltage
- Adjustable Internal Current Source

### PRECISION WIDE-RANGE VOLTAGE and CURRENT REGULATOR

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

CERAMIC PACKAGE
CASE 632-02
MO-001AA

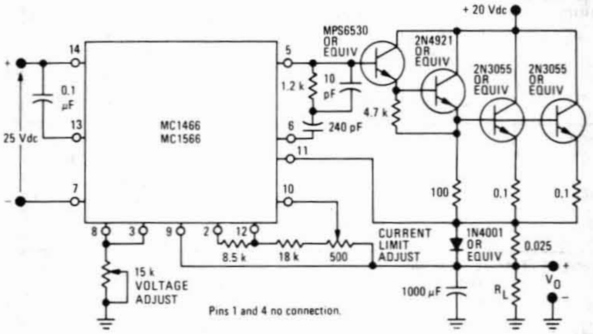


**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1466L | 0°C to +70° C | Ceramic DIP |
| MC1566L | −55°C to +125°C | Ceramic DIP |

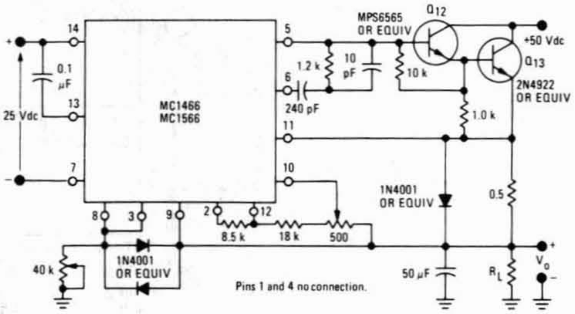
## TYPICAL APPLICATIONS

**FIGURE 1 – 0-TO-15 VDC, 10-AMPERES REGULATOR**


+ 20 Vdc
MPS6530 OR EQUIV
2N4921 OR EQUIV
2N3055 OR EQUIV
2N3055 OR EQUIV
14
5
+
0.1 µF
1.2 k
10 pF
4.7 k
13
6
240 pF
25 Vdc
MC1466
MC1566
11
7
10
−
100
0.1
0.1
8
3
9
2
12
CURRENT LIMIT ADJUST
1N4001 OR EQUIV
0.025
8.5 k
18 k
500
+
15 k VOLTAGE ADJUST
1000 µF
$R_L$
$V_O$
−

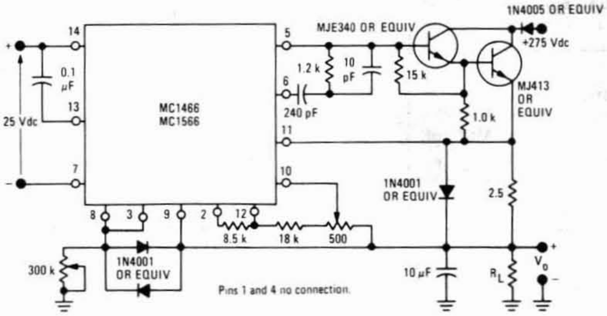
Pins 1 and 4 no connection.

**FIGURE 2 – 0-TO-40 VDC, 0.5-AMPERE REGULATOR**


MPS6565 OR EQUIV
$Q_{12}$
+50 Vdc
$Q_{13}$
2N4922 OR EQUIV
14
5
+
0.1 µF
1.2 k
10 pF
10 k
6
13
240 pF
25 Vdc
MC1466
MC1566
1.0 k
11
7
10
−
1N4001 OR EQUIV
0.5
8
3
9
2
12
8.5 k
18 k
500
+
40 k
1N4001 OR EQUIV
50 µF
$R_L$
$V_o$
−

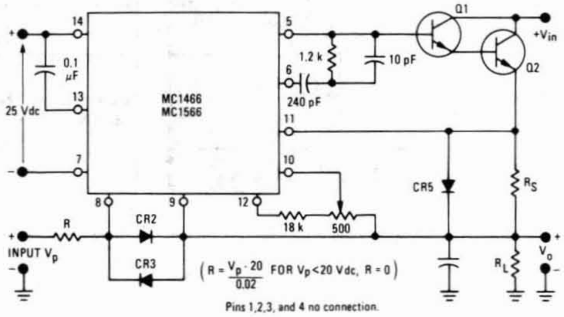
Pins 1 and 4 no connection.

**FIGURE 3 – 0-TO-250 VDC, 0.1-AMPERE REGULATOR**


1N4005 OR EQUIV
MJE340 OR EQUIV
+275 Vdc
14
5
+
1.2 k
10 pF
15 k
0.1 µF
6
13
MJ413 OR EQUIV
240 pF
25 Vdc
MC1466
MC1566
1.0 k
11
7
10
−
1N4001 OR EQUIV
2.5
8
3
9
2
12
8.5 k
18 k
500
+
300 k
1N4001 OR EQUIV
10 µF
$R_L$
$V_o$
−

Pins 1 and 4 no connection.

**FIGURE 4 – REMOTE PROGRAMMING**


Q1
14
5
+$V_{in}$
+
1.2 k
10 pF
0.1 µF
6
Q2
13
240 pF
25 Vdc
MC1466
MC1566
11
7
−
10
CR5
$R_S$
8
9
12
R
CR2
18 k
500
+
INPUT $V_p$
−
CR3
$R_L$
$V_o$
−

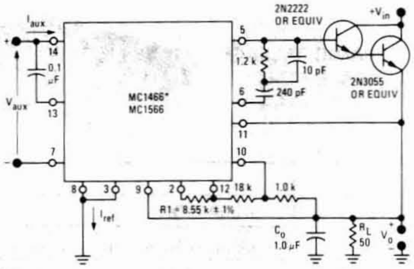
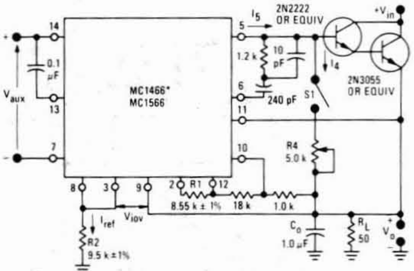
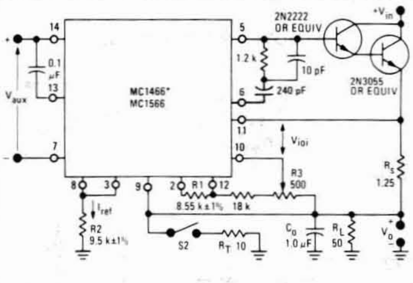
$\left( R = \frac{V_p - 20}{0.02} \text{ FOR } V_p < 20 \text{ Vdc, } R = 0 \right)$

Pins 1,2,3, and 4 no connection.

**MAXIMUM RATINGS** ($T_A$ = +25° unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Auxiliary Voltage | $V_{aux}$ | | Vdc |
| MC1466 | | 30 | |
| MC1566 | | 35 | |
| Power Dissipation (Package Limitation) | $P_D$ | 750 | mW |
| Derate above $T_A$ = +50°C | $1/\theta_{JA}$ | 6.0 | mW/°C |
| Operating Temperature Range | $T_A$ | | °C |
| MC1466 | | 0 to +70 | |
| MC1566 | | −55 to +125 | |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = +25°C, $V_{aux}$ = +25 Vdc unless otherwise noted)

| Characteristic Definition | Characteristic | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
|  $I_{aux}$<br>+<br>−<br>$V_{aux}$<br>14<br>0.1 µF<br>13<br>7<br>MC1466*<br>MC1566<br>5<br>6<br>11<br>10<br>1.2 k<br>10 pF<br>240 pF<br>2N2222 OR EQUIV<br>2N3055 OR EQUIV<br>+$V_{in}$<br>8<br>3<br>9<br>2<br>12<br>18 k<br>1.0 k<br>R1 = 8.55 k ± 1%<br>$I_{ref}$<br>$C_o$ 1.0 µF<br>$R_L$ 50<br>$V_o$ | Auxiliary Voltage (See Notes 1 & 2)<br>(Voltage from pin 14 to pin 7) | $V_{aux}$ | | | | Vdc |
| | MC1466 | | 21 | – | 30 | |
| | MC1566 | | 20 | – | 35 | |
| | Auxiliary Current | $I_{aux}$ | | | | mAdc |
| | MC1466 | | – | 9.0 | 12 | |
| | MC1566 | | – | 7.0 | 10 | |
| | Internal Reference Voltage<br>(Voltage from pin 12 to pin 7) | $V_{IR}$ | | | | Vdc |
| | MC1466 | | 17.3 | 18.2 | 19.7 | |
| | MC1566 | | 17.5 | 18.2 | 19 | |
| | Reference Current (See Note 3) | $I_{ref}$ | | | | mAdc |
| | MC1466 | | 0.8 | 1.0 | 1.2 | |
| | MC1566 | | 0.9 | 1.0 | 1.1 | |
| | Input Current-Pin 8 | $I_8$ | | | | µAdc |
| | MC1466 | | – | 6.0 | 12 | |
| | MC1566 | | – | 3.0 | 8.0 | |
| | Power Dissipation | $P_D$ | | | | mW |
| | MC1466 | | – | – | 360 | |
| | MC1566 | | – | – | 300 | |
|  +<br>−<br>$V_{aux}$<br>14<br>0.1 µF<br>13<br>7<br>MC1466*<br>MC1566<br>$I_5$<br>5<br>6<br>11<br>10<br>1.2 k<br>10 pF<br>240 pF<br>2N2222 OR EQUIV<br>2N3055 OR EQUIV<br>+$V_{in}$<br>$I_4$<br>S1<br>R4 5.0 k<br>8<br>3<br>9<br>2<br>R1<br>12<br>8.55 k ± 1%<br>18 k<br>1.0 k<br>$I_{ref}$<br>$V_{iov}$<br>R2 9.5 k ± 1%<br>$C_o$ 1.0 µF<br>$R_L$ 50<br>$V_o$ | Input Offset Voltage, Voltage Control Amplifier (See Note 4) | $V_{iov}$ | | | | mVdc |
| | MC1466 | | 0 | 15 | 40 | |
| | MC1566 | | 3.0 | 15 | 35 | |
| | Load Voltage Regulation<br>(See Note 5) | $\Delta V_{iov}$ | | | | mV |
| | MC1466 | | – | 1.0 | 3.0 | |
| | MC1566 | | – | 0.7 | 1.0 | |
| | MC1466 | $\Delta V_{ref}/V_{ref}$ | – | 0.015 | 0.03 | % |
| | MC1566 | | – | 0.004 | 0.01 | |
| | Line Voltage Regulation<br>(See Note 6) | $\Delta V_{iov}$ | | | | mV |
| | MC1466 | | – | 1.0 | 3.0 | |
| | MC1566 | | – | 0.7 | 2.0 | |
| | MC1466 | $\Delta V_{ref}/V_{ref}$ | – | 0.015 | 0.03 | % |
| | MC1566 | | – | 0.004 | 0.02 | |
| | Temperature Coefficient of Output Voltage | $TCV_o$ | | | | %/°C |
| | ($T_A$ = 0 to +75°C) MC1466 | | – | 0.01 | – | |
| | ($T_A$ = −55 to +25°C) MC1566 | | – | 0.006 | – | |
| | ($T_A$ = +25 to +125°C) MC1566 | | – | 0.004 | – | |
|  +<br>−<br>$V_{aux}$<br>14<br>0.1 µF<br>13<br>7<br>MC1466*<br>MC1566<br>5<br>6<br>11<br>10<br>1.2 k<br>10 pF<br>240 pF<br>2N2222 OR EQUIV<br>2N3055 OR EQUIV<br>+$V_{in}$<br>$V_{ioi}$<br>R3 500<br>$R_s$ 1.25<br>8<br>3<br>9<br>2<br>R1<br>12<br>8.55 k ± 1%<br>18 k<br>$I_{ref}$<br>R2 9.5 k ± 1%<br>S2<br>$R_T$ 10<br>$C_o$ 1.0 µF<br>$R_L$ 50<br>$V_o$ | Input Offset Voltage, Current Control Amplifier (See Note 4)<br>(Voltage from pin 10 to pin 11) | $V_{ioi}$ | | | | mVdc |
| | MC1466 | | 0 | 15 | 40 | |
| | MC1566 | | 3.0 | 15 | 35 | |
| | Load Current Regulation<br>(See Note 7) | $\Delta I_L/I_L$ | | | | % |
| | MC1466 | | – | 0.2 | – | |
| | MC1566 | | – | 0.1 | – | |
| | MC1466 | $\Delta I_{ref}$ | – | – | 1.0 | mAdc |
| | MC1566 | | – | – | 1.0 | |

*Pins 1 and 4 no connection.

NOTE 1:
The instantaneous input voltage, $V_{aux}$, must not exceed the maximum value of 30 volts for the MC1466 or 35 volts for the MC1566. The instantaneous value of $V_{aux}$ must be greater than 20 volts for the MC1566 or 21 volts for the MC1466 for proper internal regulation.

NOTE 2:
The auxiliary supply voltage $V_{aux}$, must "float" and be electrically isolated from the unregulated high voltage supply, $V_{in}$.

NOTE 3:
Reference current may be set to any value of current less than 1.2 mAdc by applying the relationship:

$$I_{ref}\,(mA) = \frac{8.55}{R_1\,(k\Omega)}$$

NOTE 4:
A built-in offset voltage (15 mVdc nominal) is provided so that the power supply output voltage or current may be adjusted to zero.

NOTE 5:
Load Voltage Regulation is a function of two additive components, $\Delta V_{iov}$ and $\Delta V_{ref}$, where $\Delta V_{iov}$ is the change in input offset voltage (measured between pins 8 and 9) and $\Delta V_{ref}$ is the change in voltage across R2 (measured between pin 8 and ground). Each component may be measured separately or the sum may be measured across the load. The measurement procedure for the test circuit shown is:

a. With S1 open ($I_4$ = 0) measure the value of $V_{iov\,(1)}$ and $V_{ref\,(1)}$

b. Close S1, adjust R4 so that $I_4$ = 500 µA and note $V_{iov\,(2)}$ and $V_{ref\,(2)}$.

Then $\Delta V_{iov} = V_{iov\,(1)} - V_{iov\,(2)}$

% Reference Regulation =

$$\frac{[V_{ref\,(1)} - V_{ref\,(2)}]}{V_{ref\,(1)}}\,(100\%) = \frac{\Delta V_{ref}}{V_{ref}}\,(100\%)$$

Load Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\,(100\%) + \Delta V_{iov}\,.$$

NOTE 6:
Line Voltage Regulation is a function of the same two additive components as Load Voltage Regulation, $\Delta V_{iov}$ and $\Delta V_{ref}$ (see note 5). The measurement procedure is:

**a. Set the auxiliary voltage, $V_{aux}$, to 22 volts for the MC1566 or the MC1466. Read the value of $V_{iov\,(1)}$ and $V_{ref\,(1)}$.**

**b. Change the $V_{aux}$ to 28 volts for the MC1566 or the MC1466 and note the value of $V_{iov\,(2)}$ and $V_{ref(2)}$. Then compute Line Voltage Regulation:**

$$\Delta V_{iov} = \Delta V_{iov\,(1)} - V_{iov\,(2)}$$

% Reference Regulation =

$$\frac{[V_{ref\,(1)} - V_{ref\,(2)}]}{V_{ref\,(1)}}\,(100\%) = \frac{\Delta V_{ref}}{V_{ref}}\,(100\%)$$

Line Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\,(100\%) + \Delta V_{iov}\,.$$

NOTE 7:
Load Current Regulation is measured by the following procedure:

a. With S2 open, adjust R3 for an initial load current, $I_{L(1)}$, such that $V_o$ is 8.0 Vdc.

b. With S2 closed, adjust $R_T$ for $V_o$ = 1.0 Vdc and read $I_{L(2)}$. Then Load Current Regulation =

$$\frac{[I_{L(2)} - I_{L(1)}]}{I_{L(1)}}\,(100\%) + I_{ref}$$

where $I_{ref}$ is 1.0 mAdc, Load Current Regulation is specified in this manner because $I_{ref}$ passes through the load in a direction opposite that of load current and does not pass through the current sense resistor, $R_S$.

FIGURE 5

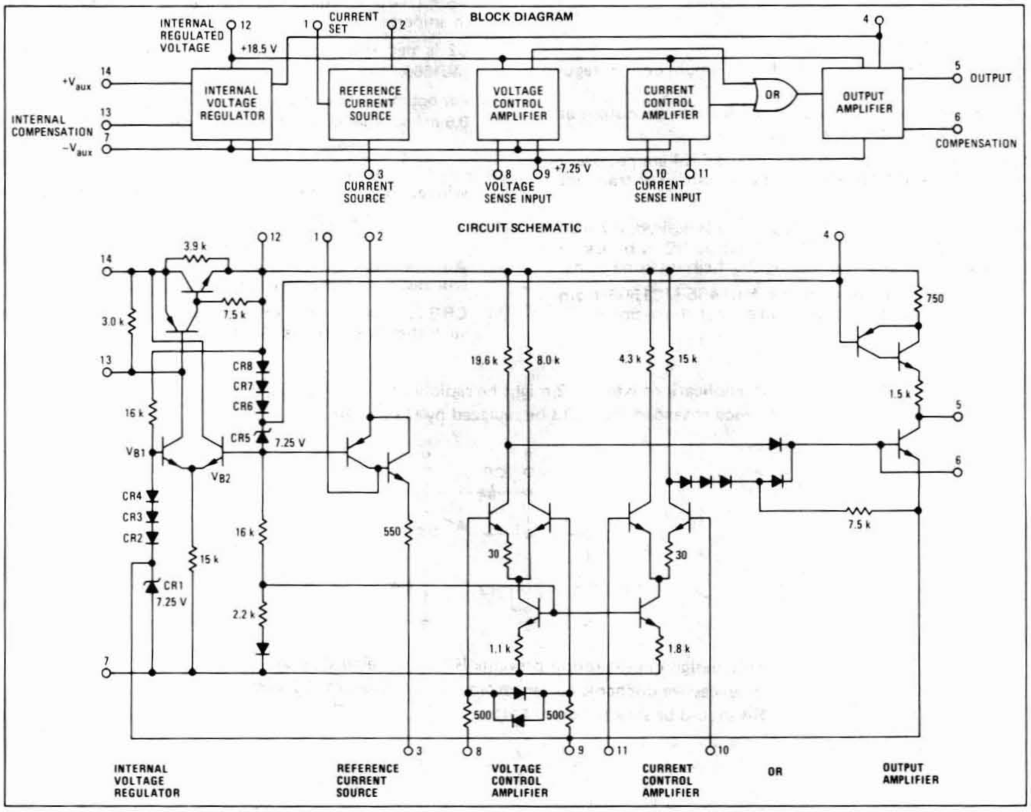
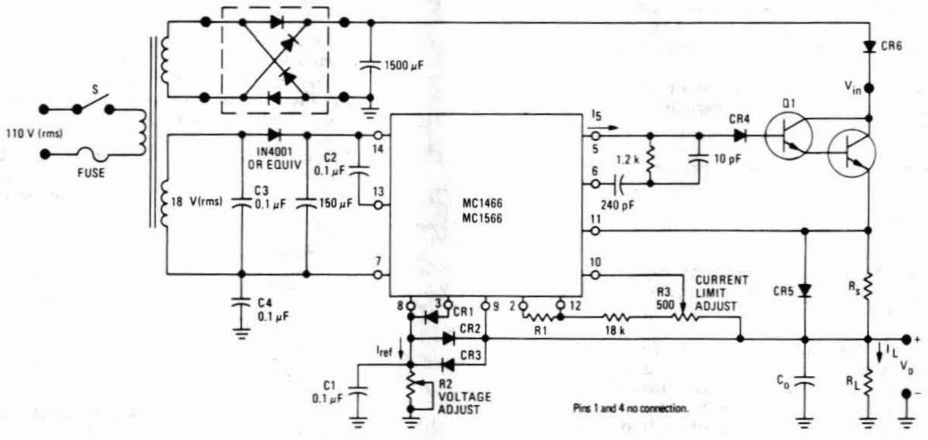

BLOCK DIAGRAM
INTERNAL REGULATED VOLTAGE
12
1
CURRENT SET
2
4
+18.5 V
14
+V_aux
13
INTERNAL COMPENSATION
7
−V_aux
INTERNAL VOLTAGE REGULATOR
REFERENCE CURRENT SOURCE
VOLTAGE CONTROL AMPLIFIER
CURRENT CONTROL AMPLIFIER
OR
OUTPUT AMPLIFIER
5
OUTPUT
6
COMPENSATION
3
CURRENT SOURCE
8
9
+7.25 V
VOLTAGE SENSE INPUT
10
11
CURRENT SENSE INPUT
CIRCUIT SCHEMATIC
3.9 k
7.5 k
3.0 k
CR8
CR7
CR6
CR5
7.25 V
16 k
VB1
VB2
CR4
CR3
CR2
15 k
CR1
7.25 V
16 k
2.2 k
550
19.6 k
8.0 k
4.3 k
15 k
30
30
1.1 k
1.8 k
500
500
750
1.5 k
7.5 k
INTERNAL VOLTAGE REGULATOR
REFERENCE CURRENT SOURCE
VOLTAGE CONTROL AMPLIFIER
CURRENT CONTROL AMPLIFIER
OR
OUTPUT AMPLIFIER

FIGURE 6 – TYPICAL CIRCUIT CONNECTION



Pins 1 and 4 no connection.

## NORMAL DESIGN PROCEDURE AND DESIGN CONSIDERATIONS

1. Constant Voltage:

   For constant voltage operation, output voltage $V_o$ is given by:

   $$V_o = (I_{ref})\,(R_2)$$

   where R2 is the resistance from pin 8 to ground and $I_{ref}$ is the output current of pin 3.

   The recommended value of $I_{ref}$ is 1.0 mAdc. Resistor R1 sets the value of $I_{ref}$:

   $$I_{ref} = \frac{8.5}{R_1}$$

   where R1 is the resistance between pins 2 and 12.

2. Constant Current:

   For constant current operation:

   (a) Select $R_s$ for a 250 mV drop at the maximum desired regulated output current, $I_{max}$.

   (b) Adjust potentiometer R3 to set constant current output at desired value between zero and $I_{max}$.

3. If $V_{in}$ is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466/MC1566 during short-circuit or transient conditions.

4. In applications where very low output noise is desired, R2 may be bypassed with C1 (0.1 μF to 2.0 μF). When R2 is bypassed, CR1 is necessary for protection during short-circuit conditions.

5. CR5 is recommended to protect the MC1466/MC1566 from simultaneous pass transistor failure and output short-circuit.

6. The RC network (10 pF, 240 pF, 1.2 kΩ) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if $f_T$ of Q1 and Q2 is greater than 0.5 MHz.

7. For remote sense applications, the positive voltage sense terminal (Pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R2) is connected to the negative load terminal through a separate sense lead.

8. $C_o$ may be selected by using the relationship:

   $C_o = (100\ \mu F)\, I_{L(max)}$, where $I_{L(max)}$ is the maximum load current in amperes.

9. C2 is necessary for the internal compensation of the MC1466/MC1566.

10. For optimum regulation, current out of Pin 5, $I_5$ should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:

    $$\frac{I_{max}}{\beta 1 \beta 2} \leqslant 0.5 \text{ mAdc}$$

    where: $I_{max}$ = maximum short-circuit load current (mAdc)

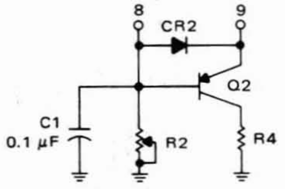
    $\beta 1$ = minimum beta of Q1

    $\beta 2$ = minimum beta of Q2

    Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5$ mAdc will result in a degradation in regulation.

11. CR6 is recommended when $V_o > 150$ Vdc and should be rated such that Peak Inverse Voltage $> V_o$.

12. In applications where R2 might be rapidly reduced in value, it is recommended that CR3 be replaced by Q2 and R4.



This design consideration prevents R2 from being destroyed by excessive discharge current from $C_o$. Components Q2 and R4 should be selected such that:

$$R4 = \frac{R2}{10} \text{ and}$$

$$V_{(BR)CEO} \text{ of } Q2 \geqslant V_o$$

## OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1566/MC1466 voltage and current regulator and also provides information on useful applications.

### SUBJECT SEQUENCE

Theory of Operation
Applications
Transient Failures
Voltage/Current-Mode Indicator

## THEORY OF OPERATION

The schematic of Figure 5 can be simplified by breaking it down into basic functions, beginning with a simplified version of the voltage reference, Figure 7. Zener diodes CR1 and CR5 with their associated forward biased diodes CR2 through CR4 and CR6 through CR8 form the stable reference needed to balance the differential amplifier. At balance ($V_{B1} = V_{B2}$), the output voltage, ($V_{12} - V_7$), is at a value that is twice the drop across either of the two diode strings: $V_{12} - V_7 = 2\,(V_{CR1} + V_{CR2} + V_{CR3} + V_{CR4})$. Other voltages, temperature compensated or otherwise, are also derived from these diodes strings for use in other parts of the circuit.

The voltage controlled current source (Figure 8) is a PNP-NPN composite which, due to the high NPN beta, yields a good working PNP from a lateral device working at a collector current of only a few microamperes. Its base voltage ($V_{B2}$) is derived from a temperature compensated portion of the diode string and consequently the overall current is dependent on the value of emitter resistor R1. Temperature compensation of the base emitter junction of Q3 is not important because approximately 9 volts exists between $V_{B2}$ and $V_{12}$, making the $\Delta V_{BE}$'s very small in percentage. Circuit reference voltage is derived from the product of $I_R$ and $R_R$; if $I_R$ is set at 1 mA (R1 = 8.5 kΩ), then $R_R$ (in kΩ) = $V_o$. Other values of current may be used as long as the following restraints are kept in mind: 1) package dissipation will be increased by about 11 mW/mA and 2) bias current for the voltage control amplifier is 3 μA, temperature dependent, and is extracted from the reference current. The reference current should

FIGURE 7 – REFERENCE VOLTAGE REGULATOR

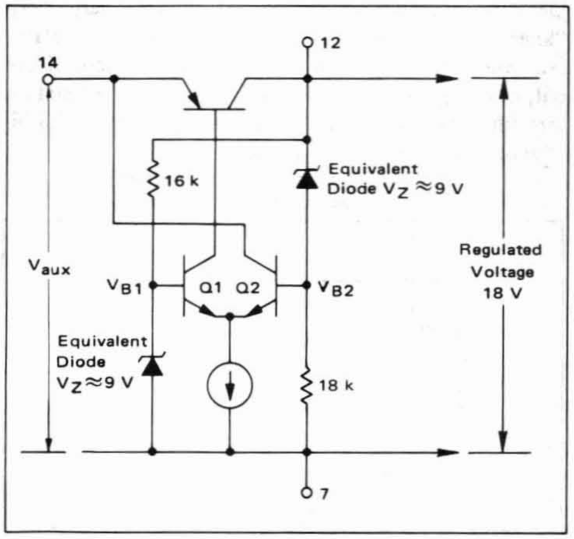
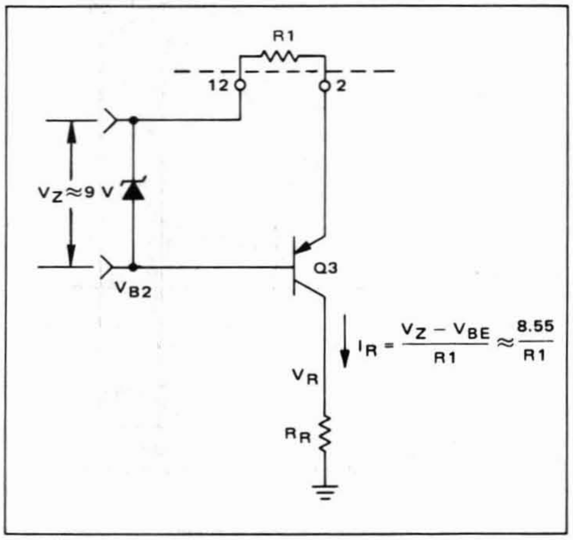

12
14
16 k
Equivalent Diode $V_Z \approx 9$ V
Regulated Voltage 18 V
$V_{aux}$
$V_{B1}$
Q1 Q2
$V_{B2}$
Equivalent Diode $V_Z \approx 9$ V
18 k
7

FIGURE 8 – VOLTAGE CONTROLLED CURRENT SOURCE



be at least two orders of magnitude above the largest expected bias current.

Loop amplification in the constant voltage mode is supplied by the voltage controlled amplifier (Figure 9), a standard high-gain differential amplifier. The inputs are diode-protected against differential overvoltages and an emitter degenerating resistor, $R_{OS}$, has been added to one of the transistors. For an emitter current in both Q5 and Q6 of 1/2 milliampere there will exist a preset offset voltage in this differential amplifier of 15 mV to insure that the output voltage will be zero when the reference voltage is zero. Without $R_{OS}$, the output voltage could be a few millivolts above zero due to the inherent offset. Since the load resistor is so large in this stage compared with the load (Q9) it will be more instructive to look at the gain on a transconductance basis rather than voltage gain. Transconductance of the differential stage is defined for small signals as:

$$g_m = \frac{1}{2r_e + R_E} \qquad (1)$$

where

$$r_e \approx \frac{0.026}{I_E} \text{ and}$$

$R_E$ = added emitter degenerating resistance.

For $I_E = 0.5$ mA,

$$g_m = \frac{1}{104 + 30} = \frac{1}{134} = 7.5 \text{ mA/volt.} \qquad (2)$$

FIGURE 9 – VOLTAGE CONTROL AMPLIFIER

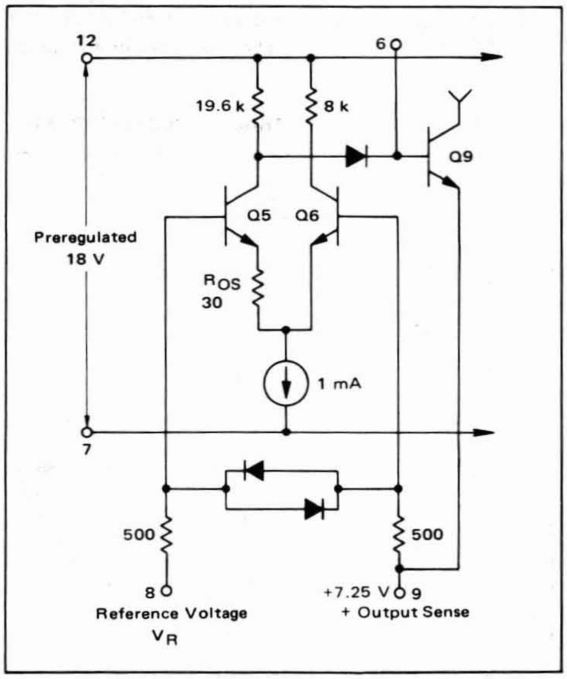
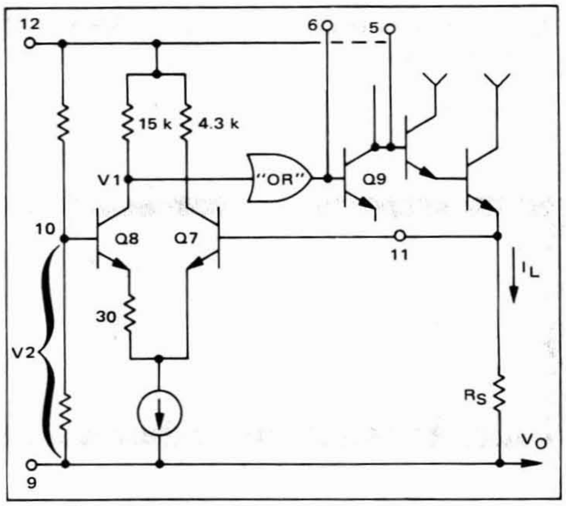


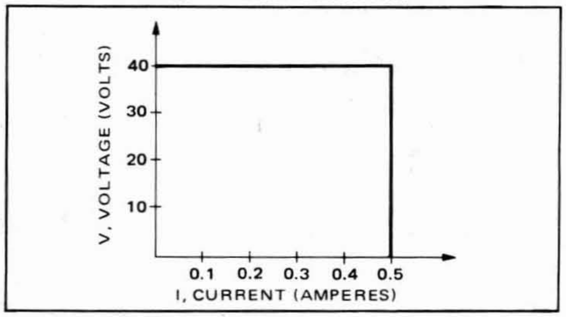
FIGURE 10 – CURRENT CONTROL CIRCUIT



This level is further boosted by the output stage such that in the constant voltage mode overall transconductance is about 300 mA/volt.

A second differential stage nearly identical to the first stage, serves as the current control amplifier (Figure 10). The gain of this stage insures a rapid crossover from the constant voltage to constant current modes and provides a convenient point to control the maximum deliverable load current. In use, a reference voltage derived from the preregulator and a voltage divider is applied to pin 10 while the output current is sampled across $R_S$ by pin 11. When $I_L$ $R_S$ is 15 mV below the reference value, voltage $V_1$ begins to rapidly rise, eventually gaining complete control of Q9 and limiting output current to a value of $V_2/R_S$. If $V_2$ is derived from a variable source, short circuit current may be controlled over the complete output current capability of the regulator. Since the constant-voltage to constant-current change-over requires only a few millivolts the voltage regulation maintains its quality to the current limit and accordingly shows a very sharp "knee" (1% +1 mA, Figure 11). Note that the regulator can switch back into the constant voltage mode if the output voltage reaches a value greater than $V_R$. Operation through zero milliamperes is guaranteed by the inclusion of another emitter offsetting resistor.

FIGURE 11 – $V_I$ CURVE FOR 0-TO-40 V, 0.5-AMPERE REGULATOR



Transistor Q9 and five diodes comprise the essential parts of the output stage (Figure 12). The diodes perform an "OR" function which allows only one mode of operation at a time - constant current or constant voltage. However, an additional stage (Q9) must be included to invert the logic and make it compatible with the driving requirements of series pass transistors as well as provide additional gain. A 1.5 mA collector current source sets the maximum deliverable output current and boosts the output impedance to that of the current source.

Note that the negative (substrate) side of the MC1566/MC1466 is 7.25 volts lower than the output voltage, and the reference regulator guarantees that the positive side is 11 volts above the output. Thus the IC remains at a voltage (relative to ground) solely dependent on the output, "floating" above and below $V_O$. $V_{CE}$ across Q9 is only two or three $V_{BE}$'s depending on the number of transistors used in the series pass configuration.

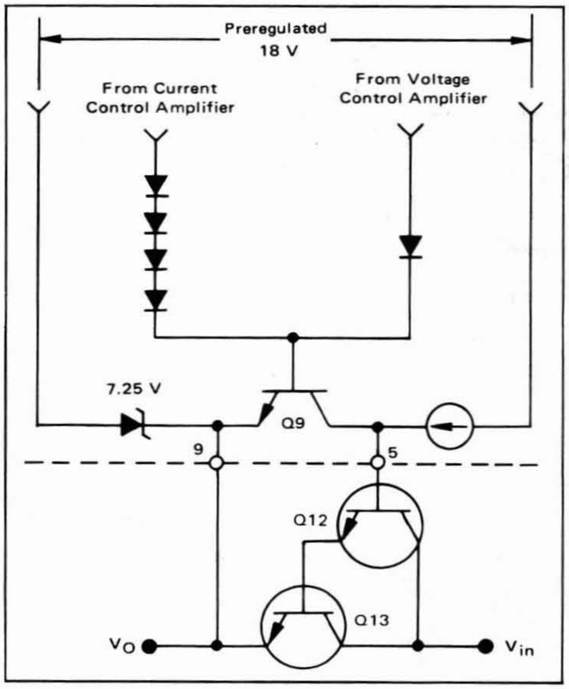
Performance characteristics of the regulator may be approximately calculated for a given circuit (Figure 2). Assuming that the two added transistors (Q12 and Q13) have minimum beta's of 20, then the overall regulator transconductance will be:

$$g_{mT} = (400)\,300\ \text{mA/volt} = 120\ \text{A/volt}. \qquad (3)$$

For a change in current of 500 mA the output voltage will drop only:

$$\Delta V = \frac{0.5}{120} = 4.2\ \text{mV}. \qquad (4)$$

FIGURE 12 – MC1566 OUTPUT STAGE


Preregulated
18 V
From Current Control Amplifier
From Voltage Control Amplifier
7.25 V
Q9
9
5
Q12
Q13
Vo
Vin

The analysis thus far does not consider changes in $V_R$ due to output current changes. If $I_L$ increases by 500 mA the collector current of Q9 decreases by 1.25 mA, causing the collector current of Q5 to increase by 30 $\mu$A. Accordingly, $I_R$ will be decreased by $\approx$0.30 $\mu$A which will drop the output by 0.03%. This figure may be improved considerably by either using high beta devices as the pass transistors, or by increasing $I_R$. Note again, however, that the maximum power rating of the package must be kept in mind. For example if $I_R$ = 4 mA, power dissipation is

$$P_D = 20\ \text{V}\ (8\ \text{mA}) + (11\ \text{V} \times 3\ \text{mA}) = 193\ \text{mW}. \qquad (5)$$

This indicates that the circuit may be safely operated up to 118°C using 20 volts at the auxiliary supply voltage. If, however, the auxiliary supply voltage is 35 volts,

$$P_D = 35\ \text{V}\ (8\ \text{mA}) + 26\ \text{V}\ (3\ \text{mA}) = 358\ \text{mW}. \qquad (6)$$

which dictates that the maximum operating temperature must be less than 91°C to keep package dissipation within specified limits.

Line voltage regulation is also a function of the voltage change between pins 8 and 9, and the change of $V_{ref}$. In this case, however, these voltages change due to changes in the internal regulator's voltages, which in turn are caused by changes in $V_{aux}$. Note that line voltage regulation is not a function of $V_{in}$. Note also that the instantaneous value of $V_{aux}$ must always be between 20 and 35 volts.

Figure 6 shows six external diodes ($CR_1$ to $CR_6$) added for protective purposes. $CR_1$ should be used if the output voltage is less than 20 volts and $CR_2$, $CR_3$ are absent. For $V_O$ higher than 20 volts, $CR_1$ should be discarded in favor of $CR_2$ and $CR_3$. Diode $CR_4$ prevents IC failure if the series pass transistors develop collector-base shorts while the main power transistor suffers a simultaneous open emitter. If the possibility of such a transistor failure mode seems remote, $CR_4$ may be deleted. To prevent instantaneous differential and common-mode breakdown of the current sense amplifier, $CR_5$ must be placed across the current limit resistor $R_S$.

Load transients occasionally produce a damaging reversal of current flow from output to input $V_O > 150$ volts (which will destroy the IC). Diode $CR_6$ prevents such reversal and renders the circuit immune from destruction for such conditions, e.g., adding a large output capacitor after the supply is turned "on". Diodes $CR_1$, $CR_2$, $CR_3$, and $CR_5$ may be general purpose silicon units such as 1N4001 or equivalent whereas $CR_4$ and $CR_6$ should have a peak inverse voltage rating equal to $V_{in}$ or greater.

## APPLICATIONS

Figure 2 shows a typical 0-to-40 volts, 0.5-ampere regulator with better than 0.01% performance, The RC network between pins 5 and 6 and the capacitor between pins 13 and 14 provide frequency compensation for the MC1566/MC1466. The external pass transistors are used to boost load current, since the output current of the regulator is less than 2 mA.

Figure 1 is a 0-to-15 volts, 10-ampere regulator with the pass transistor configuration necessary to boost the load current to 10 amperes. Note that $C_O$ has been increased to 1000 $\mu$F following the general rule:

$$C_O = 100\ \mu F/A\ I_L.$$

The prime advantage of the MC1566/MC1466 is its use as a high voltage regulator, as shown in Figure 3. This 0-to-250 volts 0.1-ampere regulator is typical of high voltage applications, limited only by the breakdown and safe areas of the output pass transistors.

The primary limiting factor in high voltage series regulators is the pass transistor. Figure 13 shows a safe area curve for the MJ413. Looking at Figure 3, we see that if the output is shorted, the transistor will have a collector current of 100 mA, with a $V_{CE}$ approximately equal to 260 volts. Thus this point falls on the dc line of the safe area curve, insuring that the transistor will not enter secondary breakdown.

In this respect (Safe Operating Area) the foldback circuit of Figure 14 is superior for handling high voltages and yet is short-circuit protected. This is due to the fact that load current is diminished as output voltage drops ($V_{CE}$ increases as $V_O$ drops) as seen in Figure 15. By careful design the load current at a short, $I_{SC}$ can be made low enough such that the combined $V_{CE}$ ($V_{in}$) and $I_{SC}$ still falls within the dc safe operating area of the transistor. For the illustrated design (Figure 14), an input voltage of 210 volts is compatible with a short-circuit current of 100 mA. Yet current foldback allows us to design for a maximum regulated load current of 500 mA. The pertinent design equations are:

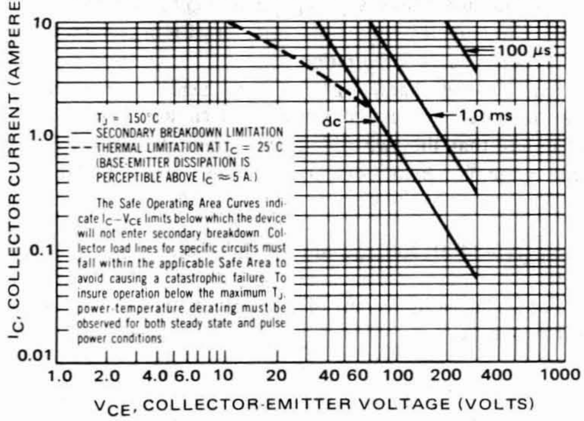
$$\text{Let } R_2\ (k\Omega) = V_O$$

$$\alpha = \frac{0.25}{V_O}\left[\frac{I_k}{I_{SC}} - 1\right]$$

$$R_1\ (k\Omega) = \frac{\alpha}{1-\alpha}\ V_O$$

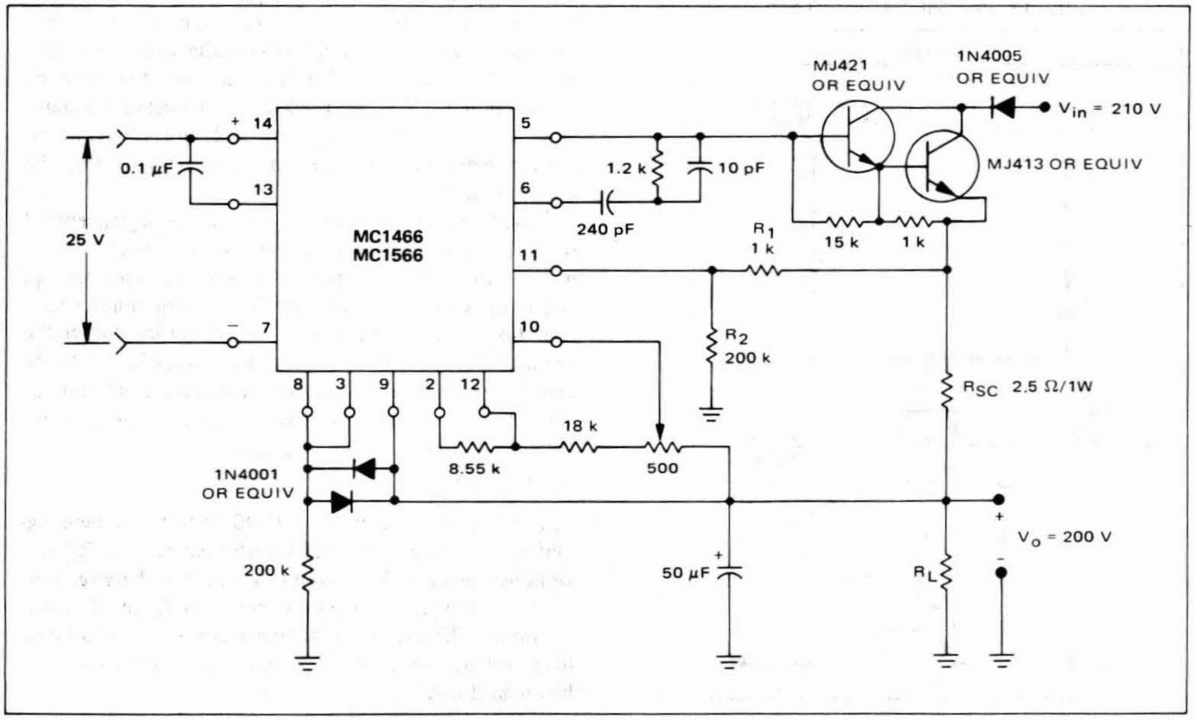
$$R_{SC} = \frac{0.25}{(1-\alpha)\ I_{SC}}$$

FIGURE 13 – SAFE AREA CURVE FOR THE MJ413



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum $T_J$, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 14 – A 200 V, 0.5-AMPERE REGULATOR WITH CURRENT FOLDBACK



The terms $I_{SC}$ and $I_k$ correspond to the short-circuit current and maximum available load current as shown in Figure 15.

FIGURE 15 – TYPICAL FOLDBACK PERFORMANCE

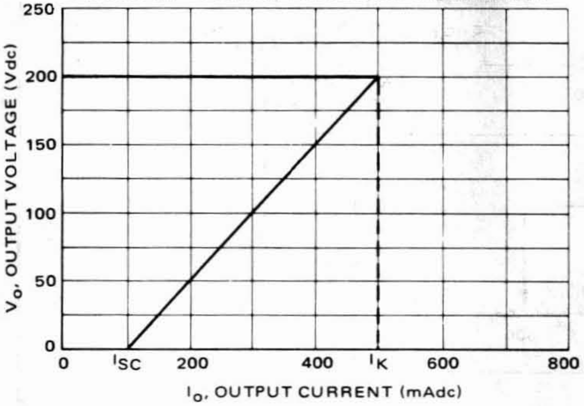


Figure 16 shows a remote sense application which should be used when high current or long wire lengths are used. This type of wiring is recommended for any application where the best possible regulation is desired. Since the sense lines draw only a small current, large voltage drops do not destroy the excellent regulation of the MC1566/ MC1466.

## TRANSIENT FAILURES

In industrial areas where electrical machinery is used the normal ac line often contains bursts of voltage running from hundreds to thousands of volts in magnitude and only microseconds in duration. Under some conditions this energy is dissipated across the internal zener connected between pins 9 and 7. This transient condition may produce a total failure of the regulator device without any apparent explanation. This type of failure is identified by absence of the 7-volt zener (CR1) between pin 9 and pin 7. To prevent this failure mode the use of a shielded power transformer is recommended, as shown in Figure 6. In addition, it is recommended that C1, C3 and C4 be included to aid in transient repression. These capacitors should have good high frequency characteristics.

If the possibility of transients on the output exists, the addition of a resistor and zener diode between pins 9 and 7 as shown on Figure 17 should be added.

## VOLTAGE/CURRENT – MODE INDICATOR

There may be times when it is desirable to know when the MC1566/MC1466 is in the constant current mode or constant voltage mode. A mode indicator can be easily added to provide this feature. Figure 18 shows how a PNP transistor has replaced a protection doide between pins 8 and 9 of Figure 2. When the MC1566/MC1466 goes from constant voltage mode to constant current mode, $V_O$ will drop below $V_8$ and the PNP transistor will turn on. The 1-mA current supplied by pin 8 will now be shunted to base of Q2 thereby turning on the indicator device I1.

FIGURE 16 – REMOTE SENSE

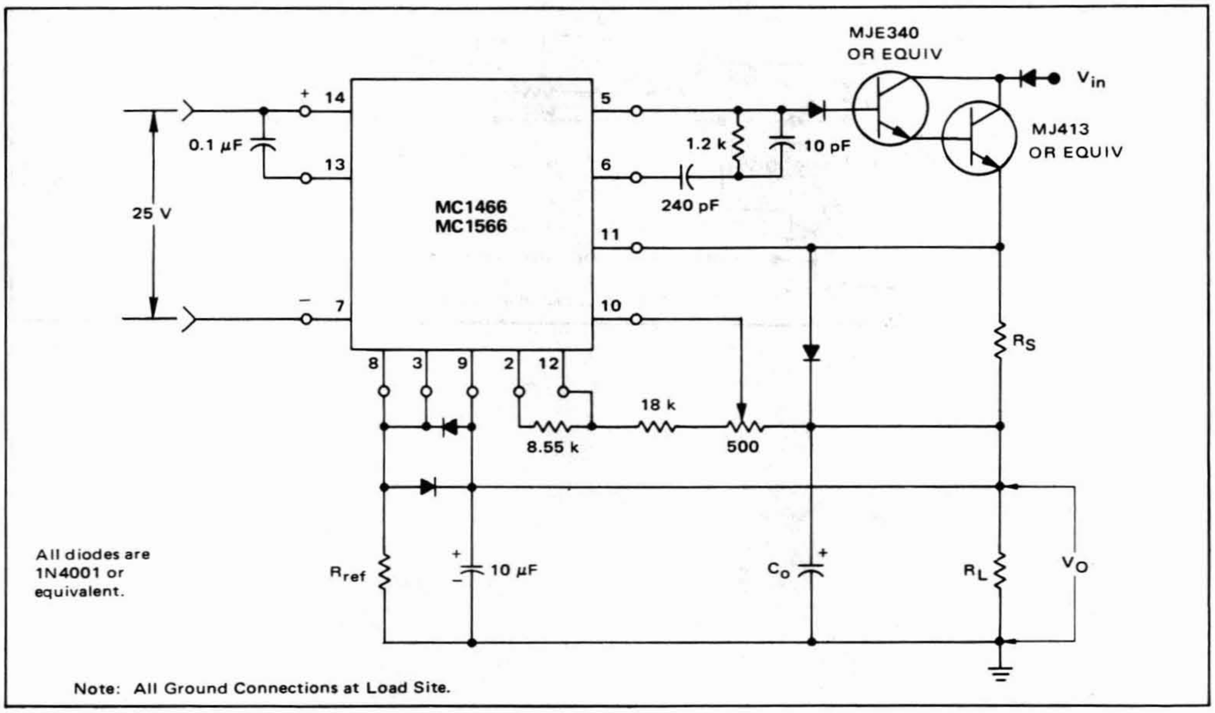
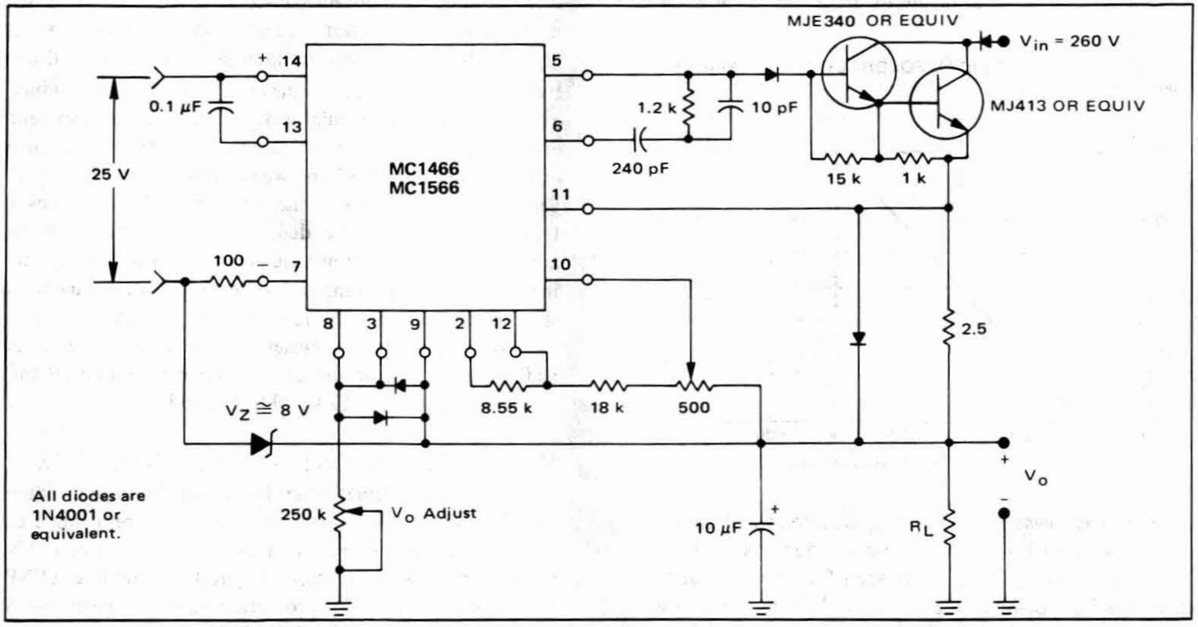
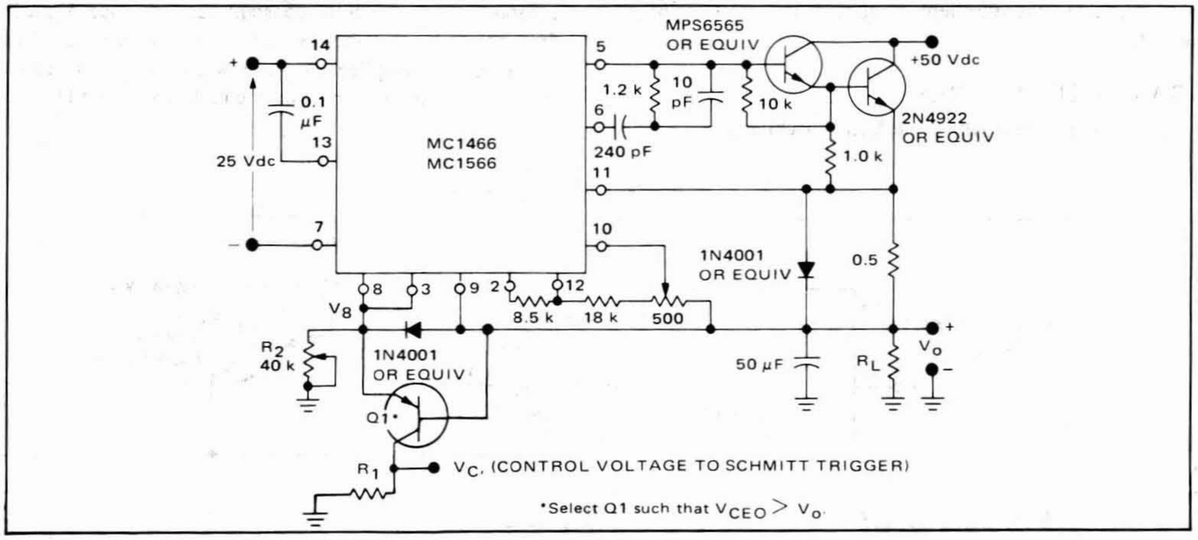


FIGURE 17 – A 0-TO-250 VOLT, 0.1-AMPERE REGULATOR


MJE340 OR EQUIV
$V_{in}$ = 260 V
MJ413 OR EQUIV
MC1466
MC1566
14
13
5
6
11
10
7
8
3
9
2
12
0.1 μF
25 V
100
1.2 k
10 pF
240 pF
15 k
1 k
2.5
8.55 k
18 k
500
$V_Z \cong 8$ V
250 k
$V_o$ Adjust
10 μF
$R_L$
$V_o$

All diodes are 1N4001 or equivalent.

FIGURE 18 – 0-TO-40 Vdc, 0.5-AMPERE REGULATOR WITH MODE INDICATOR


MPS6565 OR EQUIV
+50 Vdc
2N4922 OR EQUIV
MC1466
MC1566
14
13
5
6
11
10
7
8
3
9
2
12
0.1 μF
25 Vdc
1.2 k
10 pF
10 k
240 pF
1.0 k
1N4001 OR EQUIV
0.5
8.5 k
18 k
500
$V_8$
$R_2$ 40 k
1N4001 OR EQUIV
Q1*
$R_1$
$V_C$, (CONTROL VOLTAGE TO SCHMITT TRIGGER)
50 μF
$R_L$
$V_o$

*Select Q1 such that $V_{CEO} > V_o$.

**MOTOROLA**

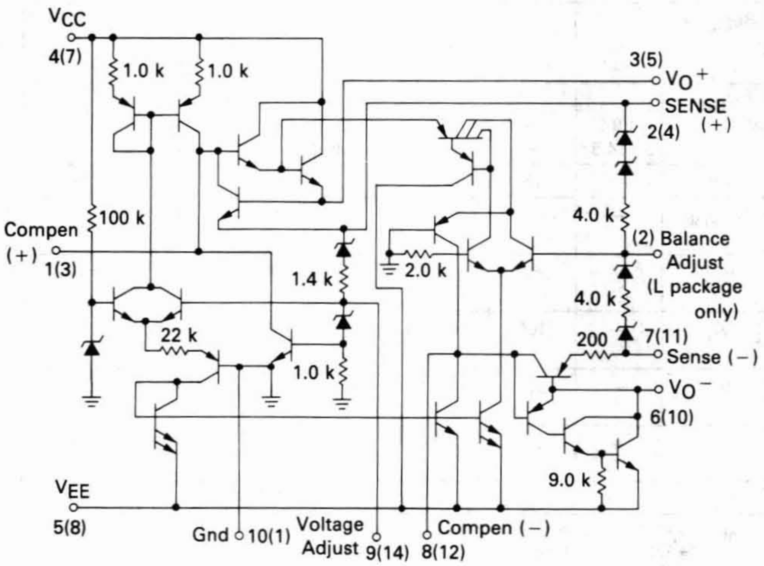
# MC1468
# MC1568

## DUAL ±15-VOLT REGULATOR

The MC1568/MC1468 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100 mA. Internally, the device is set for ±15-volt outputs but an external adjustment can be used to change both outputs simultaneously from 8.0 to 20 volts. Input voltages up to ±30 volts can be used and there is provision for adjustable current limiting.

- Internally Set to ±15 V Tracking Outputs
- Output Currents to 100 mA
- Outputs Balanced to within 1.0% (MC1568)
- Line and Load Regulation of 0.06%
- 1.0% Maximum Output Variation Due to Temperature Changes
- Standby Current Drain of 3.0 mA
- Externally Adjustable Current Limit
- Remote Sensing Provisions

### CIRCUIT SCHEMATIC

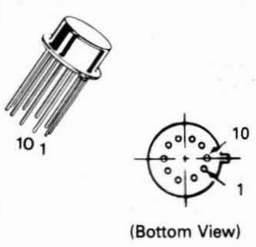


$V_{CC}$
4(7)
1.0 k
1.0 k
3(5)
$V_O$+
SENSE (+)
2(4)
4.0 k
(2) Balance Adjust (L package only)
4.0 k
200
7(11)
Sense (−)
$V_O$−
6(10)
Compen (+) 1(3)
100 k
1.4 k
2.0 k
22 k
1.0 k
9.0 k
$V_{EE}$
5(8)
Gnd 10(1)
Voltage Adjust 9(14)
Compen (−) 8(12)

Pin numbers adjacent to terminals are for the G suffix package and pin numbers in parentheses are for the L suffix package.

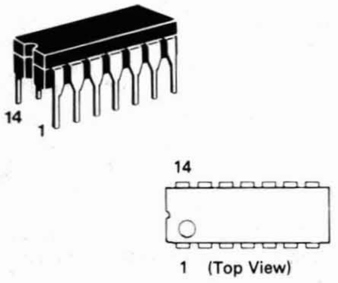
## DUAL ±15-VOLT TRACKING REGULATOR

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



10
1
10
1
(Bottom View)

**G SUFFIX**
METAL PACKAGE
CASE 603C-01
(TO-100)



14
1
14
1
(Top View)

**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA
(TO-116)

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1468G | 0°C to +70°C | Metal Can |
| MC1468L | 0°C to +70°C | Ceramic DIP |
| MC1568G | −55°C to +125°C | Metal Can |
| MC1568L | −55°C to +125°C | Ceramic DIP |

**MAXIMUM RATINGS** ($T_C$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | | Unit |
|---|---|---|---|---|
| Input Voltage | $V_{CC}, \|V_{EE}\|$ | 30 | | Vdc |
| Peak Load Current | $I_{pk}$ | 100 | | mA |
| Power Dissipation and Thermal Characteristics | | **G Package** | **L Package** | |
| $T_A$ = +25°C | $P_D$ | 0.83 | 1.25 | Watts |
| Derate above $T_A$ = +25°C | $1/\theta_{JA}$ | 6.6 | 10 | mW/°C |
| Thermal Resistance, Junction to Air | $\theta_{JA}$ | 150 | 100 | °C/W |
| $T_C$ = +25°C | $P_D$ | 1.8 | 2.5 | Watts |
| Derate above $T_C$ = +25°C | $1/\theta_{JC}$ | 14.3 | 20 | mW/°C |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | 70 | 50 | °C/W |
| Storage Junction to Temperature Range | $T_J$, $T_{stg}$ | −65 to +150 | | °C |
| Minimum Short-Circuit Resistance | $R_{SC}$(min) | 4.0 | | Ohms |

**OPERATING TEMPERATURE RANGE**

| | | | |
|---|---|---|---|
| Ambient Temperature | $T_A$ | | °C |
| MC1468 | | 0 to +70 | |
| MC1568 | | −55 to +125 | |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +20 V, $V_{EE}$ = −20 V, C1 = C2 = 1500 pF, C3 = C4 = 1.0 μF, $R_{SC}{}^+ = R_{SC}{}^-$ = 4.0 Ω, $I_L{}^+ = I_L{}^-$ = 0, $T_C$ = +25°C unless otherwise noted.) (See Figure 1.)

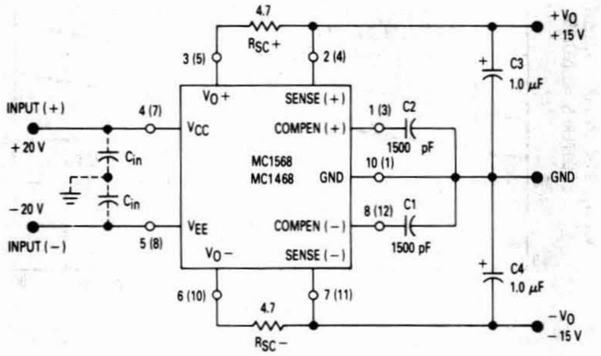
| Characteristic | Symbol | MC1568 | | | MC1468 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage | $V_O$ | ±14.8 | ±15 | ±15.2 | ±14.5 | ±15 | ±15.5 | Vdc |
| Input Voltage | $V_{in}$ | — | — | ±30 | — | — | ±30 | Vdc |
| Input-Output Voltage Differential | $\|V_{in}\text{-}V_O\|$ | 2.0 | — | — | 2.0 | — | — | Vdc |
| Output Voltage Balance (L package only) | $V_{Bal}$ | — | ±50 | ±150 | — | ±50 | ±300 | mV |
| Line Regulation Voltage | $Reg_{line}$ | | | | | | | mV |
| ($V_{in}$ = 18 V to 30 V) | | — | — | 10 | — | — | 10 | |
| ($T_{low}$① to $T_{high}$②) | | — | — | 20 | — | — | 20 | |
| Load Regulation Voltage | $Reg_{load}$ | | | | | | | mV |
| ($I_L$ = 0 to 50 mA, $T_J$ = constant) | | — | — | 10 | — | — | 10 | |
| ($T_A$ = $T_{low}$ to $T_{high}$) | | — | — | 30 | — | — | 30 | |
| Output Voltage Range | $V_{OR}$ | | | | | | | Vdc |
| L Package (See Figure 4) | | ±8.0 | — | ±20 | ±8.0 | — | ±20 | |
| G Package (See Figures 2 and 13) | | ±14.5 | — | ±20 | ±14.5 | — | ±20 | |
| Ripple Rejection (f = 120 Hz) | RR | — | 75 | — | — | 75 | — | dB |
| Output Voltage Temperature Stability ($T_{low}$ to $T_{high}$) | $\|TS_{V_O}\|$ | — | 0.3 | 1.0 | — | 0.3 | 1.0 | % |
| Short-Circuit Current Limit ($R_{SC}$ = 10 ohms) | $I_{SC}$ | — | 60 | — | — | 60 | — | mA |
| Output Noise Voltage (BW = 100 Hz–10 kHz) | $V_n$ | — | 100 | — | — | 100 | — | μV(RMS) |
| Positive Standby Current ($V_{in}$ = +30 V) | $I_B{}^+$ | — | 2.4 | 4.0 | — | 2.4 | 4.0 | mA |
| Negative Standby Current ($V_{in}$ = −30 V) | $I_B{}^-$ | — | 1.0 | 3.0 | — | 1.0 | 3.0 | mA |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 0.2 | — | — | 0.2 | — | %/k Hr |

① $T_{low}$ = 0°C for MC1468
= −55°C for MC1568

② $T_{high}$ = +70°C for MC1468
= +125°C for MC1568

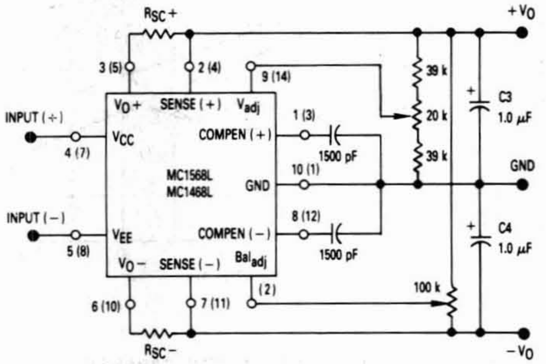
## TYPICAL APPLICATIONS

### FIGURE 1 — BASIC 50-mA REGULATOR


4.7
RSC+
3 (5)
2 (4)
+VO
+15 V
C3
1.0 µF
INPUT (+)
+20 V
4 (7)
VO+
SENSE (+)
VCC
COMPEN (+)
1 (3)
C2
1500 pF
Cin
MC1568
MC1468
10 (1)
GND
GND
−20 V
Cin
INPUT (−)
VEE
5 (8)
8 (12)
C1
COMPEN (−)
1500 pF
VO−
SENSE (−)
C4
1.0 µF
6 (10)
7 (11)
4.7
RSC−
−VO
−15 V

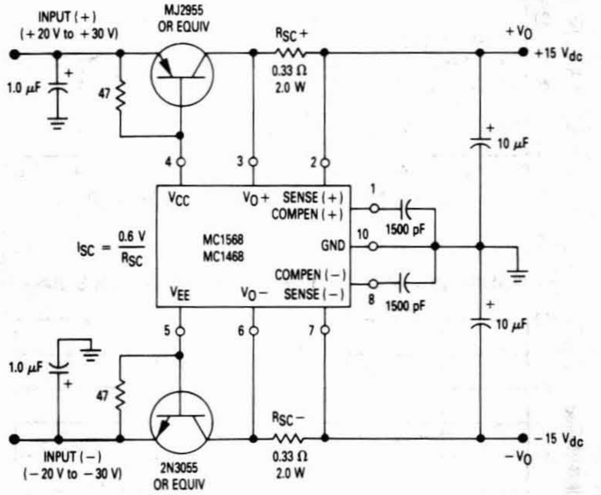
C1 and C2 should be located as close to the device as possible. A 0.1 µF ceramic capacitor ($C_{in}$) may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors. C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation, it may be necessary to bypass C4 with a 0.1 µF ceramic disc capacitor.

### FIGURE 2 — VOLTAGE ADJUST AND BALANCE ADJUST CIRCUIT
### ($14.5\ V \leq V_{out} \leq 20\ V$)

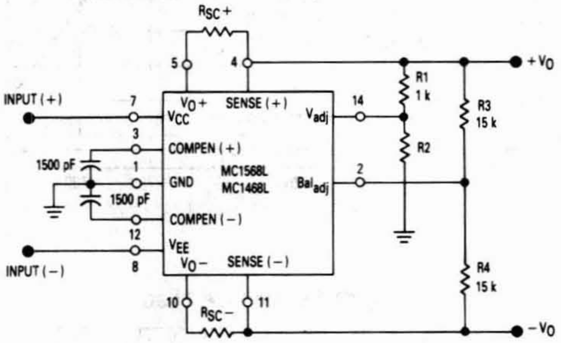

RSC+
+VO
3 (5)
2 (4)
9 (14)
39 k
20 k
39 k
C3
1.0 µF
INPUT (+)
4 (7)
VO+
SENSE (+)
Vadj
VCC
COMPEN (+)
1 (3)
1500 pF
MC1568L
MC1468L
10 (1)
GND
GND
INPUT (−)
5 (8)
VEE
COMPEN (−)
8 (12)
1500 pF
C4
1.0 µF
VO−
SENSE (−)
Baladj
(2)
100 k
6 (10)
7 (11)
RSC−
−VO

Balance adjust available in MC1568L, MC1468L ceramic dual in-line package only.

### FIGURE 3 — ±1.5-AMPERE REGULATOR
### (Short-Circuit Protected, with Proper Heatsinking)


INPUT (+)
(+20 V to +30 V)
MJ2955
OR EQUIV
RSC+
+VO
+15 Vdc
0.33 Ω
2.0 W
1.0 µF
47
10 µF
4
3
2
1
VCC
VO+
SENSE (+)
COMPEN (+)
1500 pF
10
ISC = 0.6 V / RSC
MC1568
MC1468
GND
COMPEN (−)
VEE
VO−
SENSE (−)
8
1500 pF
10 µF
5
6
7
1.0 µF
47
RSC−
−15 Vdc
−VO
INPUT (−)
(−20 V to −30 V)
2N3055
OR EQUIV
0.33 Ω
2.0 W

### FIGURE 4 — OUTPUT VOLTAGE ADJUSTMENT FOR $8.0\ V \leq |\pm V_O| \leq 14.5\ V$
### (Ceramic-Packaged Devices Only)


RSC+
5
4
+VO
R1
1 k
INPUT (+)
7
VO+
SENSE (+)
14
VCC
Vadj
R3
15 k
3
COMPEN (+)
R2
1500 pF
1
GND
MC1568L
MC1468L
2
Baladj
1500 pF
COMPEN (−)
12
VEE
INPUT (−)
8
VO−
SENSE (−)
R4
15 k
10
RSC−
11
−VO

The presence of $Bal_{adj}$, pin 2, on devices housed in the dual in-line package (L suffix) allows the user to adjust the output voltages down to ±8.0 V. The required value of resistor R2 can be calculated from

$$R2 = \frac{R1\ R_{int}\ (\phi + V_z)}{R_{int}\ (V_O - \phi - V_z) - \phi\ R1}$$

Where: $R_{int}$ = An Internal Resistor = R1 = 1.0 kΩ
$\phi = 0.68\ V$
$V_z = 6.6\ V$

Some common design values are listed below:

| $\pm V_O$(V) | R2 | $T_C\ V_O$ (%/°C) | $I_B$ + (mA) |
|---|---|---|---|
| 14 | 1.2 k | 0.003 | 10 |
| 12 | 1.8 k | 0.022 | 7.2 |
| 10 | 3.5 k | 0.025 | 5.0 |
| 8.0 | ∞ | 0.028 | 2.6 |

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +20 V, $V_{EE}$ = −20 V, $V_O$ = ±15 V, $T_A$ = +25°C unless otherwise noted.)

FIGURE 5 — LOAD REGULATION

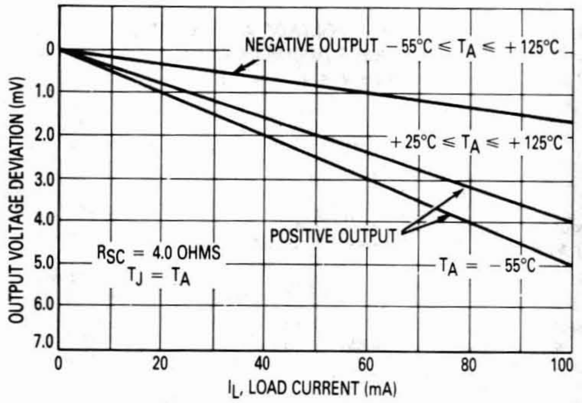


FIGURE 6 — REGULATOR DROPOUT VOLTAGE

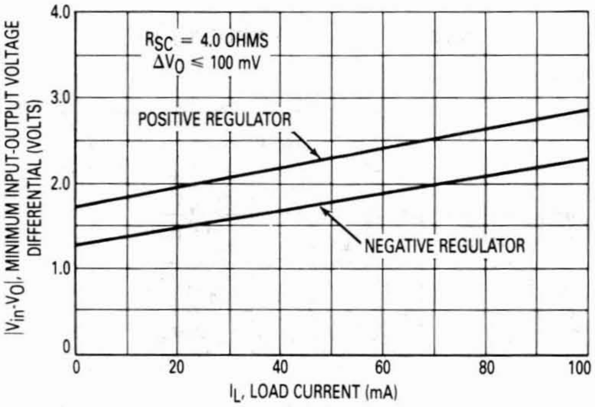


FIGURE 7 — MAXIMUM CURRENT CAPABILITY

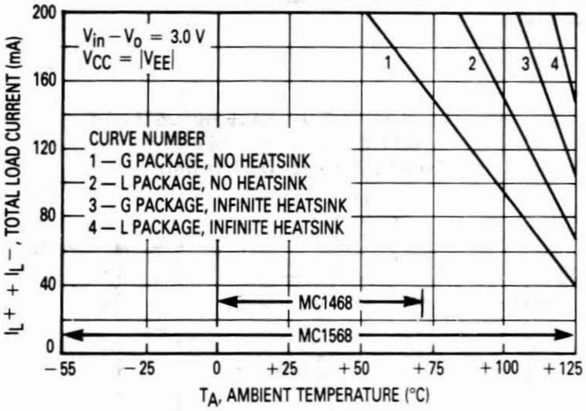


FIGURE 8 — MAXIMUM CURRENT CAPABILITY

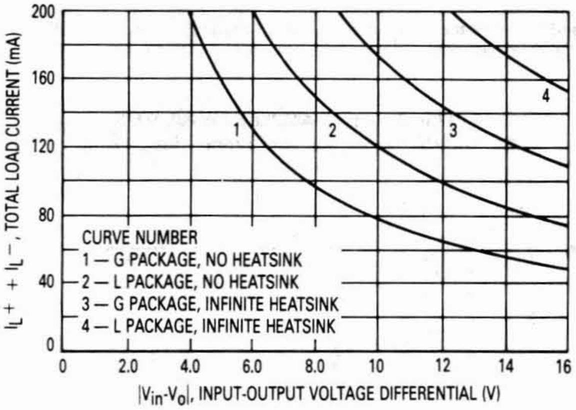


FIGURE 9 — $I_{SC}$ versus $R_{SC}$

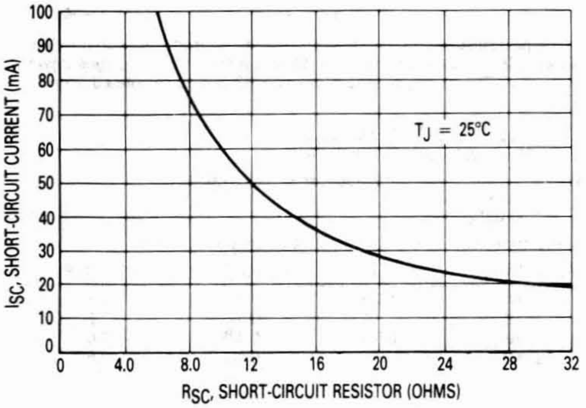
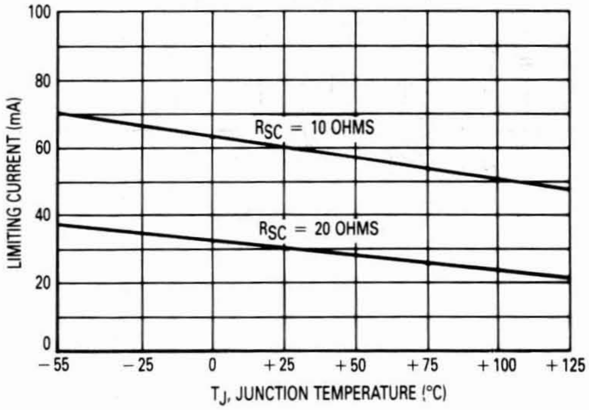


FIGURE 10 — CURRENT-LIMITING CHARACTERISTICS



## TYPICAL CHARACTERISTICS (continued)

($V_{CC}$ = +20 V, $V_{EE}$ = −20 V, $V_O$ = ±15 V, $T_A$ = +25°C unless otherwise noted.)

**FIGURE 11 — STANDBY CURRENT DRAIN**

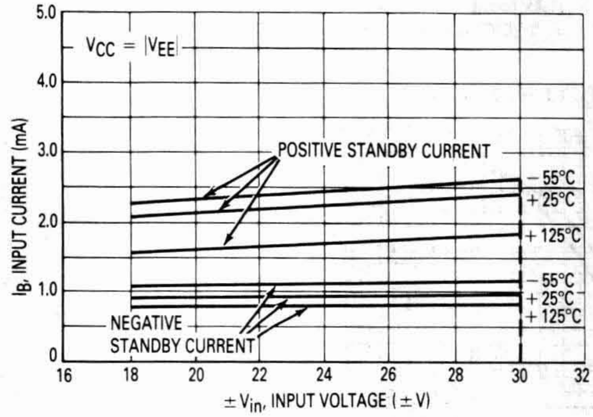


**FIGURE 12 — STANDBY CURRENT DRAIN**

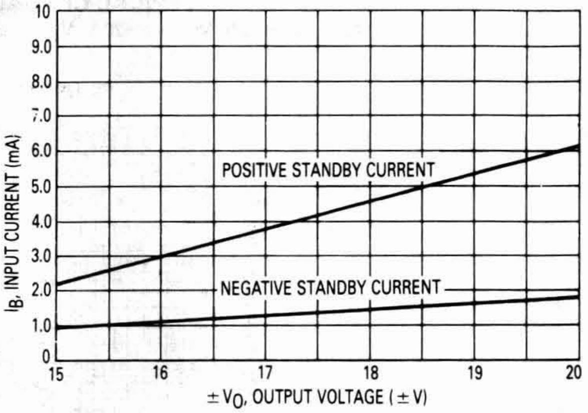


**FIGURE 13 — TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE**

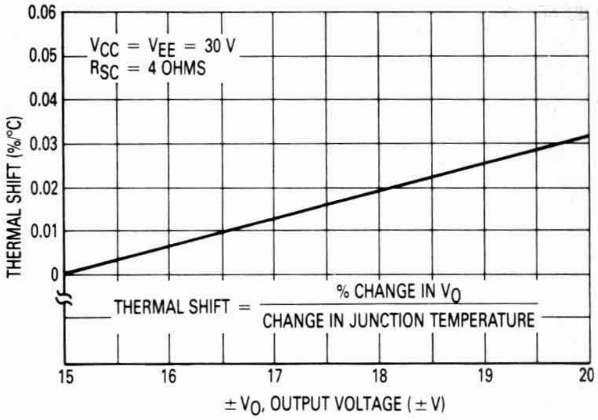


**FIGURE 14 — LOAD TRANSIENT RESPONSE**

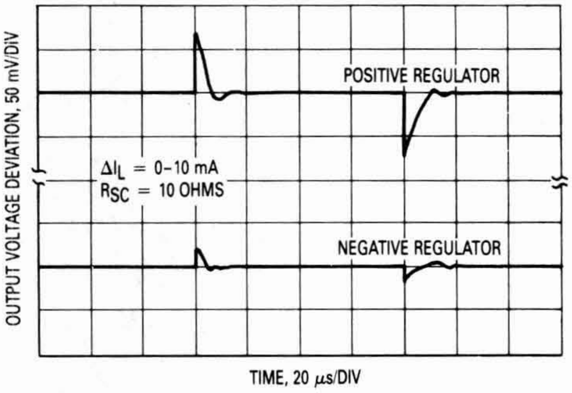


**FIGURE 15 — LINE TRANSIENT RESPONSE**

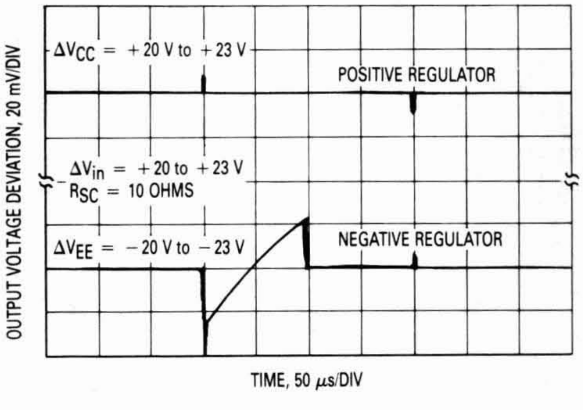
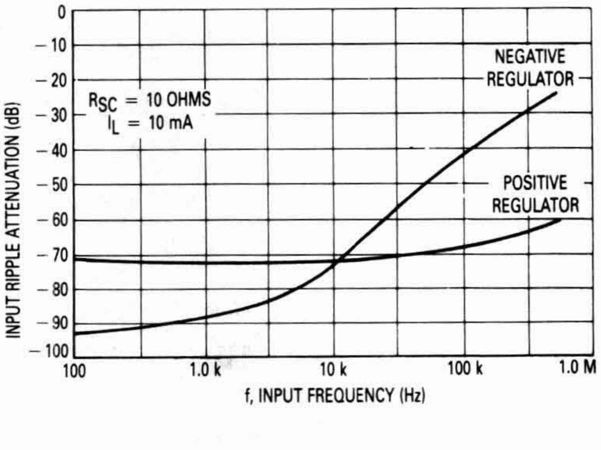


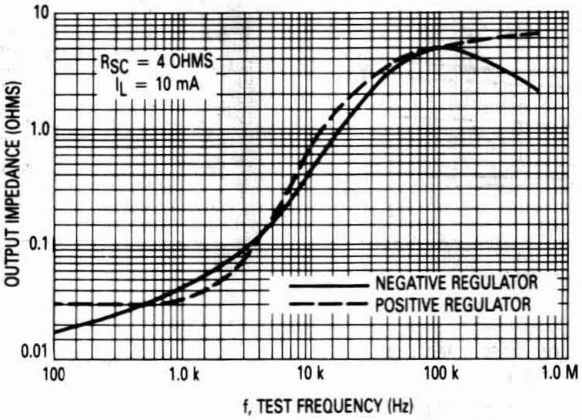
**FIGURE 16 — RIPPLE REJECTION**



## TYPICAL CHARACTERISTICS (continued)

($V_{CC}$ = +20 V, $V_{EE}$ = −20 V, $V_O$ = ±15 V, $T_A$ = +25°C unless otherwise noted.)

### FIGURE 17 — OUTPUT IMPEDANCE



**ORDERING INFORMATION**

| Device | Alternate | Temperature Range | Package |
|---|---|---|---|
| MC1723CD | LM723CH, μA723HC | 0°C to +70°C | SO-14 |
| MC1723CG | LM723CD, μA723DC | 0°C to +70°C | Metal Can |
| MC1723CL | LM723CN, μA723PC | 0°C to +70°C | Ceramic DIP |
| MC1723CP | | 0°C to +70°C | Plastic DIP |
| MC1723G | | −55°C to +125°C | Metal Can |
| MC1723L | | −55°C to +125°C | Ceramic DIP |

# MC1723
# MC1723C

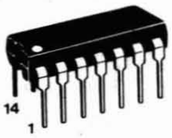
## VOLTAGE REGULATOR

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

## MONOLITHIC VOLTAGE REGULATOR

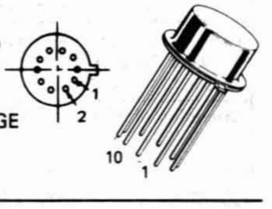
The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (-55°C to +125°C) and the MC1723C over the commercial temperature range (0 to +70°C)

- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short-Circuit Protection

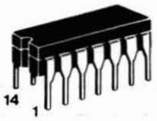


**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

(Bottom View)



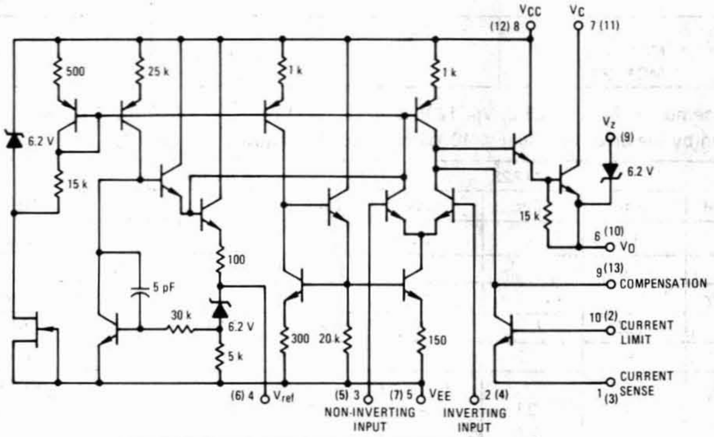
**G SUFFIX**
METAL PACKAGE
CASE 603-04
(TO-100)



**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA

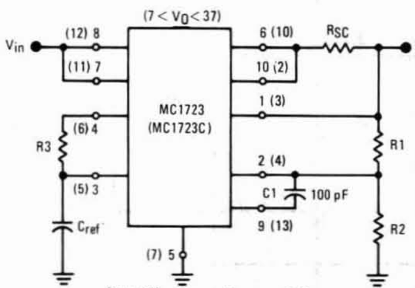
**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14

**FIGURE 1 – CIRCUIT SCHEMATIC**


VCC (12) 8
VC 7 (11)
500
25 k
1 k
1 k
6.2 V
15 k
Vz (9)
6.2 V
15 k
6 (10) VO
9 (13) COMPENSATION
100
5 pF
30 k
6.2 V
5 k
300
20 k
150
10 (2) CURRENT LIMIT
CURRENT SENSE 1 (3)
(6) 4 Vref
(5) 3 NON-INVERTING INPUT
(7) 5 VEE
2 (4) INVERTING INPUT

PIN NUMBERS ADJACENT TO TERMINALS ARE FOR THE METAL PACKAGE;
PIN NUMBERS IN PARENTHESIS ARE FOR DUAL IN-LINE PACKAGES.

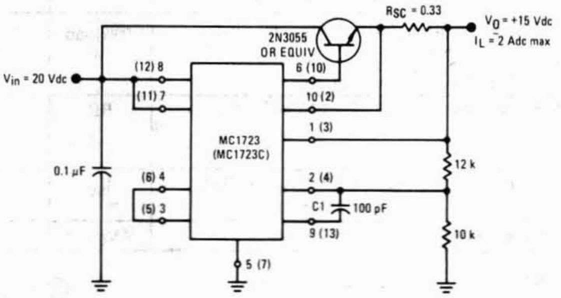
**FIGURE 2 – TYPICAL CIRCUIT CONNECTION**


(7 < VO < 37)
Vin
(12) 8
(11) 7
(6) 4
R3
(5) 3
Cref
(7) 5
MC1723
(MC1723C)
6 (10)
RSC
VO
10 (2)
1 (3)
R1
2 (4)
C1
100 pF
9 (13)
R2

$V_O \cong 7\left(\frac{R1 + R2}{R2}\right)$ $I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}}$ at $T_J = +25^oC$

For best results $10\ k < R2 < 100\ k$
For minimum drift $R3 = R1 \| R2$

**FIGURE 3 – TYPICAL NPN CURRENT BOOST CONNECTION**


RSC = 0.33
VO = +15 Vdc
IL = 2 Adc max
2N3055
OR EQUIV
Vin = 20 Vdc
(12) 8
(11) 7
6 (10)
10 (2)
1 (3)
MC1723
(MC1723C)
0.1 μF
(6) 4
(5) 3
2 (4)
C1
100 pF
9 (13)
12 k
10 k
5 (7)

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Pulse Voltage from $V_{CC}$ to $V_{EE}$ (50 ms) | $V_{in(p)}$ | 50 | $V_{peak}$ |
| Continuous Voltage from $V_{CC}$ to $V_{EE}$ | $V_{in}$ | 40 | Vdc |
| Input-Output Voltage Differential | $V_{in} - V_O$ | 40 | Vdc |
| Maximum Output Current | $I_L$ | 150 | mAdc |
| Current from $V_{ref}$ | $I_{ref}$ | 15 | mAdc |
| Current from $V_z$ | $I_z$ | 25 | mA |
| Voltage Between Non-Inverting Input and $V_{EE}$ | $V_{ie}$ | 8.0 | Vdc |
| Differential Input Voltage | $V_{id}$ | ±5.0 | Vdc |
| Power Dissipation and Thermal Characteristics | | | |
| Plastic Package | | | |
| $T_A$ = +25°C | $P_D$ | 1.25 | W |
| Derate above $T_A$ = +25°C | $1/\theta_{JA}$ | 10 | mW/°C |
| Thermal Resistance, Junction to Air | $\theta_{JA}$ | 100 | °C/W |
| Metal Package | | | |
| $T_A$ = +25°C | $P_D$ | 1.0 | Watt |
| Derate above $T_A$ = +25°C | $1/\theta_{JA}$ | 6.6 | mW/°C |
| Thermal Resistance, Junction to Air | $\theta_{JA}$ | 150 | °C/W |
| $T_C$ = +25°C | $P_D$ | 2.1 | Watts |
| Derate above $T_A$ = +25°C | $1/\theta_{JA}$ | 14 | mW/°C |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | 35 | °C/W |
| Dual In-Line Ceramic Package | $P_D$ | 1.5 | Watt |
| Derate above $T_A$ = +25°C | $1/\theta_{JA}$ | 10 | mW/°C |
| Thermal Resistance, Junction to Air | $\theta_{JA}$ | 100 | °C/W |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | | °C |
| Metal Package | | -65 to +150 | |
| Dual In-Line Ceramic | | -65 to +175 | |
| Operating Ambient Temperature Range | $T_A$ | | °C |
| MC1723C | | 0 to +70 | |
| MC1723 | | -55 to +125 | |

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted: $T_A$ = +25°C, $V_{in}$ 12 Vdc, $V_O$ = 5.0 Vdc, $I_L$ = 1.0 mAdc, $R_{SC}$ = 0, C1 = 100 pF, $C_{ref}$ = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 2)

| Characteristic | Symbol | MC1723 | | | MC1723C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage Range | $V_{in}$ | 9.5 | – | 40 | 9.5 | – | 40 | Vdc |
| Output Voltage Range | $V_O$ | 2.0 | – | 37 | 2.0 | – | 37 | Vdc |
| Input-Output Voltage Differential | $V_{in}-V_O$ | 3.0 | – | 38 | 3.0 | – | 38 | Vdc |
| Reference Voltage | $V_{ref}$ | 6.95 | 7.15 | 7.35 | 6.80 | 7.15 | 7.50 | Vdc |
| Standby Current Drain ($I_L$ = 0, $V_{in}$ = 30 V) | $I_{IB}$ | – | 2.3 | 3.5 | – | 2.3 | 4.0 | mAdc |
| Output Noise Voltage (f = 100 Hz to 10 kHz) | $V_n$ | | | | | | | μV(RMS) |
| $C_{ref}$ = 0 | | – | 20 | – | – | 20 | – | |
| $C_{ref}$ = 5.0 μF | | – | 2.5 | – | – | 2.5 | – | |
| Average Temperature Coefficient of Output Voltage ($T_{low}$ ① < $T_A$ < $T_{high}$ ②) | $TCV_O$ | – | 0.002 | 0.015 | – | 0.003 | 0.015 | %/°C |
| Line Regulation | $Reg_{line}$ | | | | | | | $\%V_O$ |
| ($T_A$ = +25°C) 12 V < $V_{in}$ < 15 V | | – | 0.01 | 0.1 | – | 0.01 | 0.1 | |
| ($T_A$ = +25°C) 12 V ≤ $V_{in}$ < 40 V | | – | 0.02 | 0.2 | – | 0.1 | 0.5 | |
| ($T_{low}$ ① < $T_A$ < $T_{high}$ ②) 12 V < $V_{in}$ < 15 V | | – | – | 0.3 | – | – | 0.3 | |
| Load Regulation (1.0 mA < $I_L$ < 50 mA) | $Reg_{load}$ | | | | | | | $\%V_O$ |
| $T_A$ = +25°C | | – | 0.03 | 0.15 | – | 0.03 | 0.2 | |
| $T_{low}$ ① < $T_A$ < $T_{high}$ ② | | – | – | 0.6 | – | – | 0.6 | |
| Ripple Rejection (f = 50 Hz to 10 kHz) | RR | | | | | | | dB |
| $C_{ref}$ = 0 | | – | 74 | – | – | 74 | – | |
| $C_{ref}$ = 5.0 μF | | – | 86 | – | – | 86 | – | |
| Short Circuit Current Limit ($R_{SC}$ = 10 Ω, $V_O$ = 0) | $I_{sc}$ | – | 65 | – | – | 65 | – | mAdc |
| Long Term Stability | $\Delta V_O/\Delta t$ | – | 0.1 | – | – | 0.1 | – | %/1000 Hr |

① $T_{low}$ = 0°C for MC1723C
= -55°C for MC1723

② $T_{high}$ = +70° C for MC1723C
= +125°C for MC1723

## TYPICAL CHARACTERISTICS

($V_{in}$ = 12 Vdc, $V_O$ = 5.0 Vdc, $I_L$ = 1.0 mAdc, $R_{SC}$ = 0, $T_A$ = +25°C unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

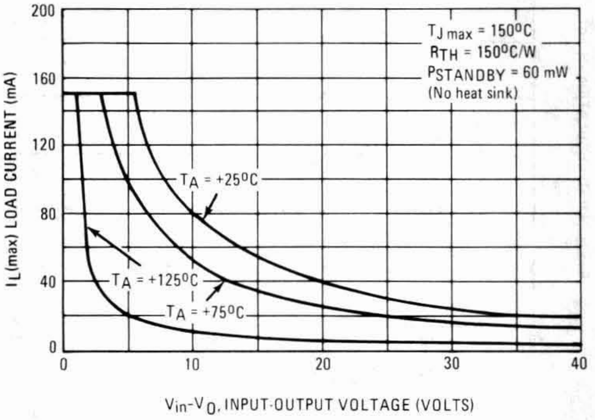


FIGURE 5 – LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

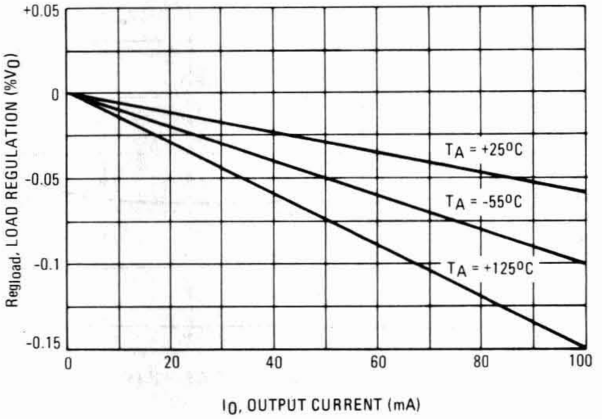


FIGURE 6 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

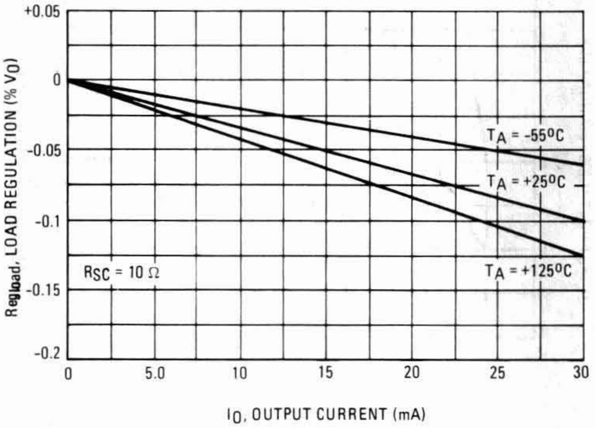


FIGURE 7 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

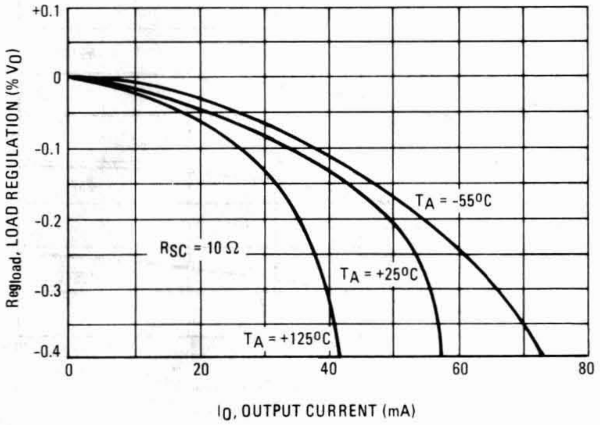


FIGURE 8 – CURRENT LIMITING CHARACTERISTICS

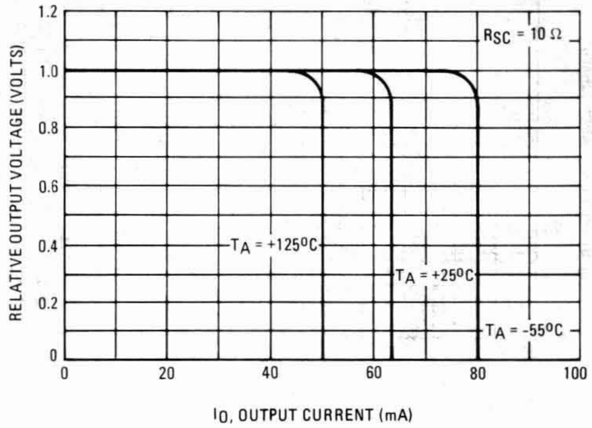
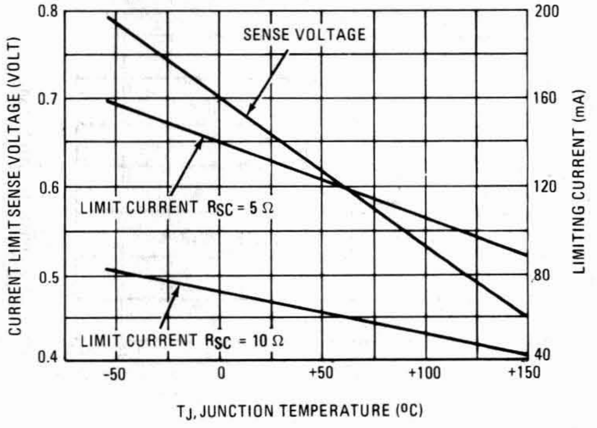
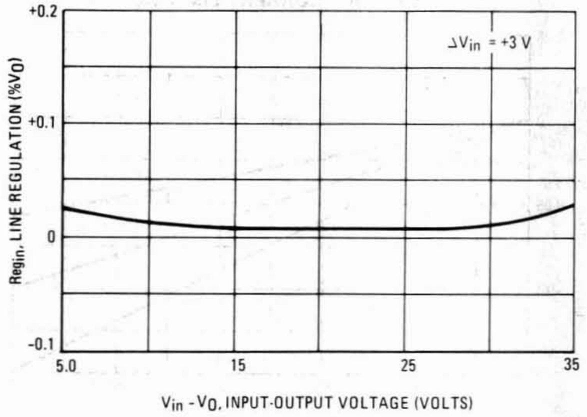


FIGURE 9 – CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE

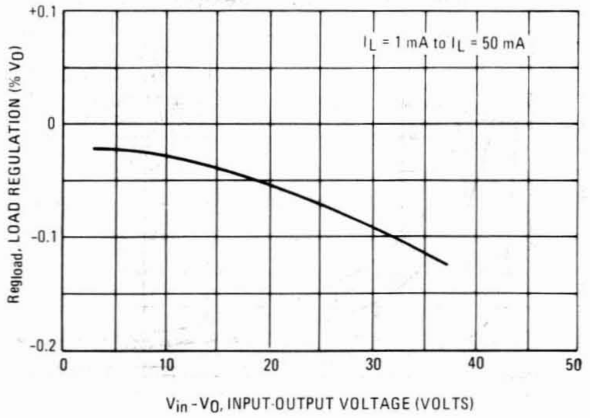


## TYPICAL CHARACTERISTICS (continued)

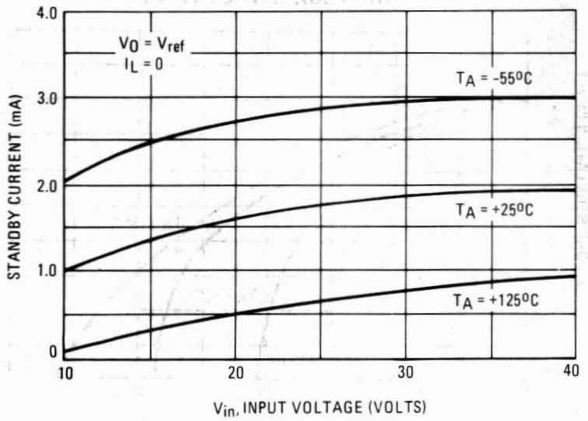
### FIGURE 10 – LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



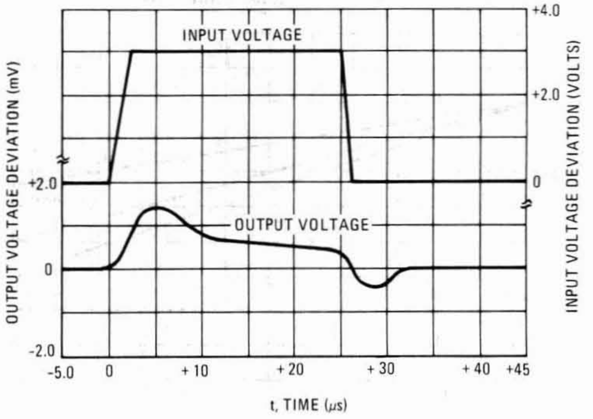
### FIGURE 11 – LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



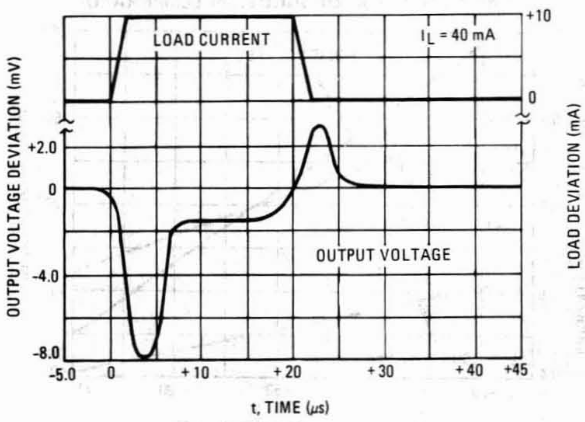
### FIGURE 12 – STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



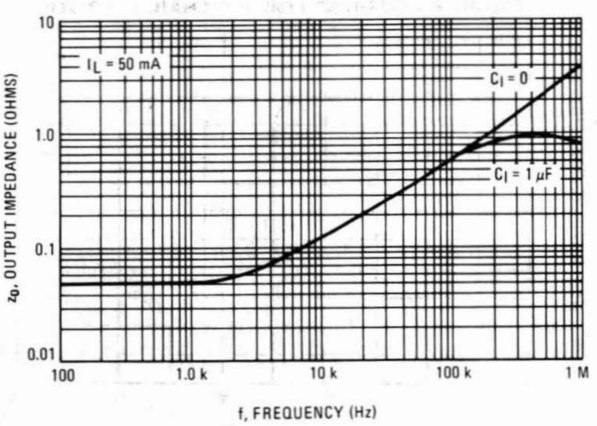
### FIGURE 13 – LINE TRANSIENT RESPONSE



### FIGURE 14 – LOAD TRANSIENT RESPONSE



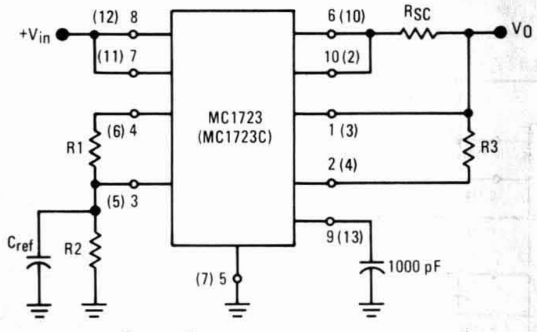
### FIGURE 15 – OUTPUT IMPEDANCE AS FUNCTION OF FREQUENCY



## TYPICAL APPLICATIONS

Pin numbers adjacent to terminals are for the metal package;
pin numbers in parenthesis are for the dual in-line packages.

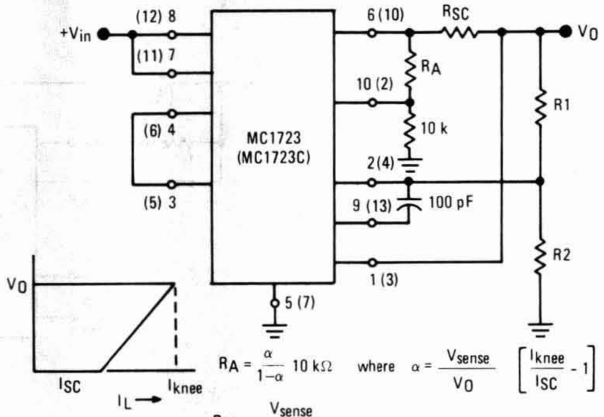
**FIGURE 16 – TYPICAL CONNECTION FOR $2 < V_O < 7$**


+Vin
(12) 8
(11) 7
6 (10)
RSC
VO
10 (2)
MC1723
(MC1723C)
(6) 4
R1
1 (3)
R3
2 (4)
(5) 3
9 (13)
Cref
R2
(7) 5
1000 pF

$V_O \cong 7\left[\frac{R2}{R1+R2}\right]$  $I_{SC} = \frac{V_{sense}}{R_{SC}} \cong \frac{0.66}{R_{SC}}$ at $T_J = +25^{\circ}C$

For best results 10 k < R1 + R2 < 100 k.
For minimum drift R3 = R1||R2.

**FIGURE 17 – MC1723,C FOLDBACK CONNECTION**


+Vin
(12) 8
(11) 7
(6) 4
(5) 3
MC1723
(MC1723C)
6 (10)
RSC
VO
RA
10 (2)
10 k
2 (4)
9 (13)
100 pF
1 (3)
5 (7)
R1
R2
VO
ISC
Iknee
IL

$R_A = \frac{\alpha}{1-\alpha}\ 10\ k\Omega$  where $\alpha = \frac{V_{sense}}{V_O}\left[\frac{I_{knee}}{I_{SC}} - 1\right]$

$R_{SC} = \frac{V_{sense}}{(1-\alpha)\ I_{SC}}$

**FIGURE 18 – +5 V, 1-AMPERE SWITCHING REGULATOR**

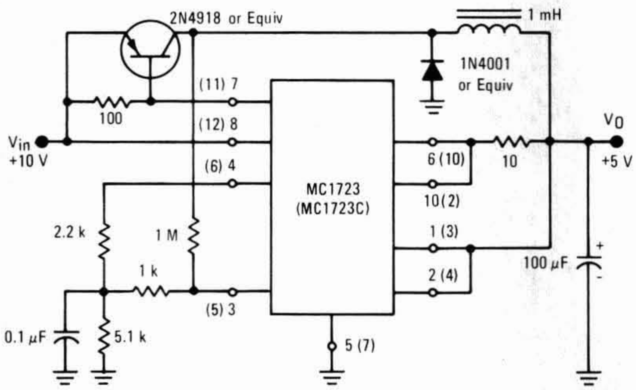

2N4918 or Equiv
1 mH
1N4001
or Equiv
(11) 7
100
(12) 8
Vin
+10 V
VO
+5 V
(6) 4
6 (10)
10
MC1723
(MC1723C)
10 (2)
2.2 k
1 M
1 (3)
1 k
100 μF
2 (4)
(5) 3
0.1 μF
5.1 k
5 (7)

**FIGURE 19 – +5 V, 1-AMPERE HIGH EFFICIENCY REGULATOR**

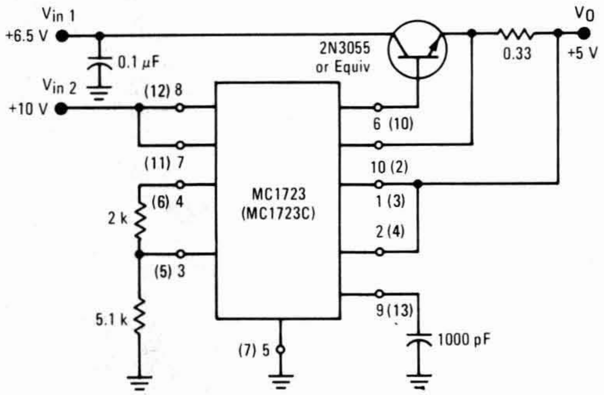

Vin 1
+6.5 V
0.1 μF
Vin 2
+10 V
2N3055
or Equiv
VO
0.33
+5 V
(12) 8
6 (10)
(11) 7
10 (2)
MC1723
(MC1723C)
(6) 4
2 k
1 (3)
2 (4)
(5) 3
9 (13)
5.1 k
(7) 5
1000 pF

**FIGURE 20 – +15 V, 1-AMPERE REGULATOR WITH REMOTE SENSE**

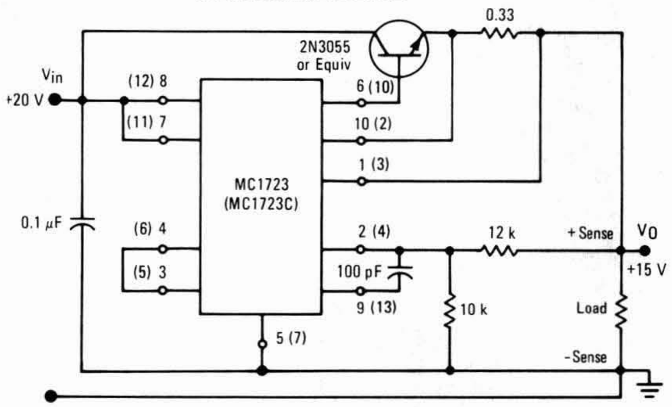
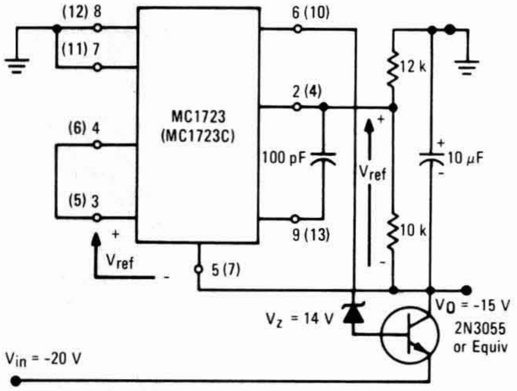
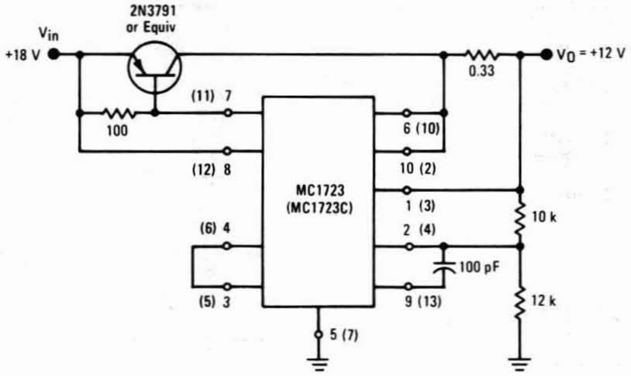

0.33
2N3055
or Equiv
Vin
+20 V
(12) 8
6 (10)
(11) 7
10 (2)
1 (3)
MC1723
(MC1723C)
0.1 μF
(6) 4
2 (4)
12 k
+ Sense
VO
+15 V
(5) 3
100 pF
9 (13)
10 k
Load
5 (7)
-Sense

**FIGURE 21 – -15 V NEGATIVE REGULATOR**


(12) 8
(11) 7
6 (10)
12 k
2 (4)
MC1723
(MC1723C)
(6) 4
100 pF
Vref
10 μF
(5) 3
9 (13)
10 k
Vref
5 (7)
VO = -15 V
VZ = 14 V
2N3055
or Equiv
Vin = -20 V

## TYPICAL APPLICATIONS (continued)

FIGURE 22 – +12 V, 1-AMPERE REGULATOR
USING PNP CURRENT BOOST


2N3791
or Equiv
$V_{in}$
+18 V
$V_O$ = +12 V
0.33
100
(11) 7
(12) 8
(6) 4
(5) 3
MC1723
(MC1723C)
6 (10)
10 (2)
1 (3)
2 (4)
9 (13)
5 (7)
10 k
100 pF
12 k

MOTOROLA

# MC3420
# MC3520

## Specifications and Applications Information

## SWITCHMODE REGULATOR CONTROL CIRCUIT

SILICON MONOLITHIC
INTEGRATED CIRCUITS

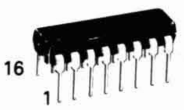
### SWITCHMODE REGULATOR CONTROL CIRCUIT

The MC3520/3420 is an inverter control unit which provides all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

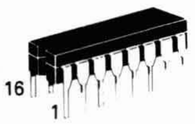
These devices are designed to supply the pulse width modulated drive to the bases of two external power transistors. Other applications where these devices can be used are in transformerless voltage doublers, transformer coupled dc-to-dc converters and other power control functions.

The MC3520 is specified over the military operating range of −55°C to +125°C. The MC3420 is specified from 0°C to +70°C.

- Includes Symmetrical Oscillator
- On Chip Pulse Width Modulator, Voltage Reference, Dead Time Comparator, and Phase Splitter
- Output Frequency Adjustable (2.0 kHz to 100 kHz)
- Inhibit and Symmetry Correction Inputs Available
- Controlled Start-Up
- Frequency and Dead Time are Independently Adjustable (0% to 100%)
- Can be Slaved to Other MC3420s
- Open Collector Outputs
- Output Capability 50 mA (Max.)
- On Chip Protection Against Double Pulsing of Same Output During Load Transient Condition

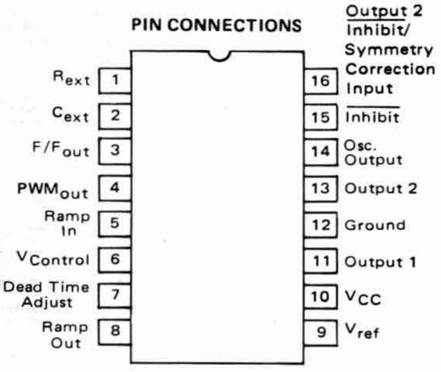


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05
(MC3420
only)



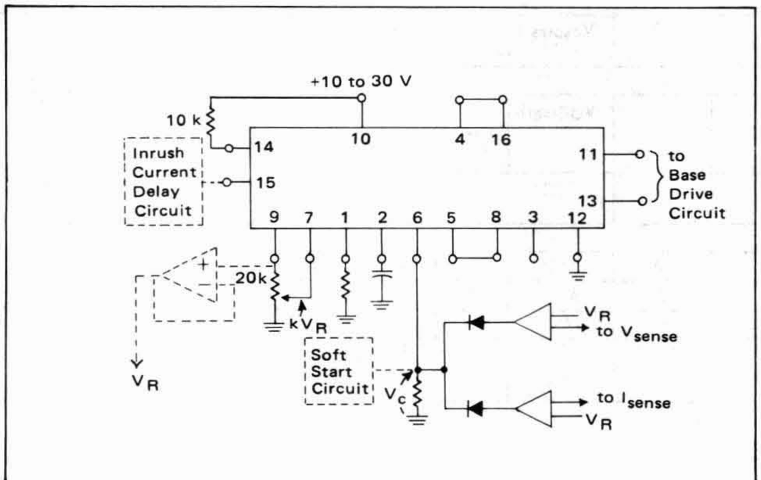
**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

PIN CONNECTIONS


Rext 1
Cext 2
F/Fout 3
PWMout 4
Ramp In 5
VControl 6
Dead Time Adjust 7
Ramp Out 8
16 Output 2 Inhibit/ Symmetry Correction Input
15 Inhibit
14 Osc. Output
13 Output 2
12 Ground
11 Output 1
10 VCC
9 Vref

(Top View)

FIGURE 1–TYPICAL APPLICATION


+10 to 30 V
10 k
10
4
16
14
15
Inrush Current Delay Circuit
11
13
to Base Drive Circuit
9
7
1
2
6
5
8
3
12
20k
kVR
VR
Soft Start Circuit
VC
VR
to Vsense
to Isense
VR

ORDERING INFORMATION

| DEVICE | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| MC3420P | 0 to +70°C | Plastic DIP |
| MC3420L | 0 to +70°C | Ceramic DIP |
| MC3520L | -55 to +125°C | Ceramic DIP |

## MAXIMUM RATINGS

| Rating | Symbol | MC3520 | MC3420 | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 30 | | V |
| Output Voltage (pins 11 and 13) | $V_{out}$ | 40 | | V |
| Oscillator Output Voltage (pin 14) | $V_{14}$ | 30 | | V |
| Voltage at pin 4 | $V_4$ | 2.0 | | V |
| Voltage at pins 3 and 8 | $V_3, V_8$ | 5.0 | | V |
| Voltage at pin 5 | $V_5$ | 7.0 | | V |
| Power Dissipation | $P_D$ | See Thermal Information | | |
| Operating Junction Temperature | $T_J$ | | | °C |
| Plastic Package | | – | 125 | |
| Ceramic Package | | 150 | 150 | |
| Operating Ambient Temperature Range | $T_A$ | -55 to +125 | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | -65 to +150 | °C |

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 10 to 30 V, $T_A$ = 25°C unless otherwise noted.)

| Characteristic | Figure | Symbol | MC3520 | | | MC3420 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| **REFERENCE SECTION** | | | | | | | | | |
| Reference Voltage<br>($I_{ref}$ = 400 µA) | 5 | $V_{ref}$ | 7.6 | 7.8 | 8.0 | 7.4 | 7.8 | 8.2 | V |
| Temperature Coefficient of Reference Voltage<br>($V_{CC}$ = 15 V, $I_{ref}$ = 400 µA) | 5 | $TCV_{ref}$ | – | 0.008 | 0.03 | – | 0.008 | 0.03 | %/°C |
| Input Regulation of Reference Voltage | 5 | $Reg_{line}$ | | | | | | | mV/V |
| ($I_{ref}$ = 400 µA) | | | – | 3.0 | 7.5 | – | 4.0 | 7.5 | |
| ($I_{ref}$ = 1.0 mA) | | | – | 5.0 | – | – | 5.0 | – | |
| **DC SUPPLY SECTION** | | | | | | | | | |
| Supply Voltage | 5 | $V_{in}$ | 10 | – | 30 | 10 | – | 30 | V |
| Supply Current<br>($R_{ext}$ = 10 kΩ, excluding load and current and reference current) | 5 | $I_D$ | – | – | 16 | – | – | 22 | mA |
| **OSCILLATOR SECTION** | | | | | | | | | |
| Line Frequency Stability | 5 | | | | | | | | |
| (f = 20 kHz) | | Δf | – | – | 3.0 | – | – | 5.0 | % |
| (f = 20 kHz, $V_{CC}$ = 15 V, $T_{low}$ to $T_{high}$) | | Δf | – | 0.03 | – | – | 0.04 | – | %/°C |
| Maximum Output Frequency<br>($V_{CC}$ = 15 V) | 6 | $f_{max}$ | 100 | 200 | – | 100 | 200 | – | kHz |
| Minimum Output Frequency<br>($V_{CC}$ = 15 V) | 6 | $f_{min}$ | – | 2.0 | 5.0 | – | 2.0 | 5.0 | kHz |
| Oscillator Output Saturation Voltage<br>($I_{14\ sink}$ = 5.0 mA) | 11 | $V_{osc(sat)}$ | – | 0.2 | 0.5 | – | 0.2 | 0.5 | V |
| **OUTPUT SECTION** | | | | | | | | | |
| Output Saturation Voltage | 7 | $V_{CE(sat)}$ | | | | | | | V |
| ($I_L$ = 40 mA, $T_{high}$ to $T_{low}$) | | | – | 0.33 | 0.5 | – | 0.33 | 0.5 | |
| ($I_L$ = 25 mA, $T_{high}$ to $T_{low}$) | | | – | 0.22 | – | – | 0.22 | – | |
| Output Leakage Current<br>($V_{CE}$ = 40 V, Pins 11 and 13) | 8 | $I_{CE}$ | – | – | 50 | – | – | 50 | µA |
| **COMPARATOR SECTION** | | | | | | | | | |
| Pulse Width Adjustment Range | 9 | ΔPW | 0 | – | 100 | 0 | – | 100 | % |
| Dead Time Adjustment Range | 9 | ΔDT | 0 | – | 100 | 0 | – | 100 | % |
| Temperature Coefficient of Dead Time | – | TCDT | – | 0.1 | – | – | 0.1 | – | %/°C |
| Comparator Bias Currents | 12, 13 | $I_{IB}$ | – | 5.0 | 15 | – | 5.0 | 15 | µA |
| | 14 | $I_{IB}$ | – | 10 | 30 | – | 10 | 30 | µA |

**ELECTRICAL CHARACTERISTICS (continued)**

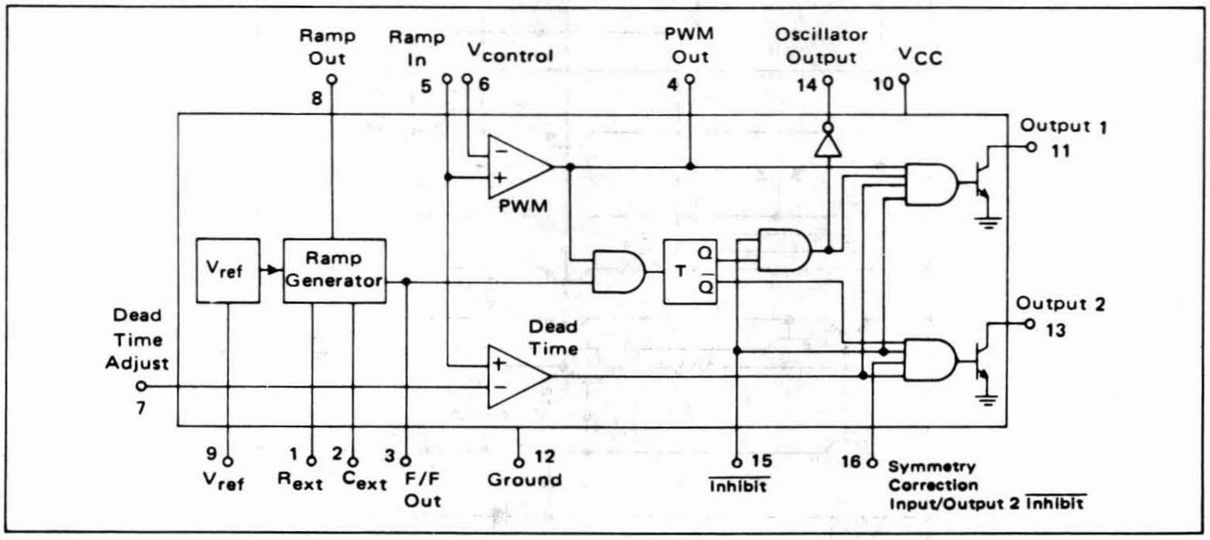
| Characteristic | Figure | Symbol | MC3520 Min | MC3520 Typ | MC3520 Max | MC3420 Min | MC3420 Typ | MC3420 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| **AUXILIARY INPUTS/OUTPUTS** | | | | | | | | | |
| Ramp Voltage | 5 | | | | | | | | V |
| Peak High | | $V_{ramp(Hi)}$ | 5.5 | 6.0 | 6.5 | 5.5 | 6.0 | 6.5 | |
| Peak Low | | $V_{ramp(Low)}$ | 2.0 | 2.4 | 2.8 | 2.0 | 2.4 | 2.8 | |
| Ramp Voltage Change ($V_{ramp\ Hi} - V_{ramp\ Low}$) | 5 | $\Delta V_{ramp}$ | 3.0 | 3.5 | 4.0 | 3.0 | 3.5 | 4.0 | V |
| Ramp Out Sink Current | 5 | $I_{sink}$ | – | 400 | – | – | 400 | – | µA |
| Ramp Out Source Current | 5 | $I_{source}$ | – | 3.0 | – | – | 3.0 | – | mA |
| $\overline{\text{Inhibit}}$ Input Current – High ($V_{IH} = 2.0$ V) | 10 | $I_{IH}$ | – | – | 40 | – | – | 40 | µA |
| $\overline{\text{Inhibit}}$ Input Current – Low ($V_{IL} = 0.8$ V) | 10 | $I_{IL}$ | – | -25 | -180 | – | -25 | -180 | µA |
| Symmetry Correction Input/Output 2 Inhibit Current – High ($V_{SY} = 2.0$ V, Pin 16) | 10 | $I_{SY/H}$ | – | – | 40 | – | – | 40 | µA |
| Symmetry Correction Input/Output 2 Inhibit Current – Low ($V_{SY} = 0.8$ V, Pin 16) | 10 | $I_{SY/L}$ | – | -10 | -180 | – | -10 | -180 | µA |
| $F/F_{out}$ Source Current | – | $I_{source}$ | – | 2.0 | – | – | 2.0 | – | mA |
| **OUTPUT AC CHARACTERISTICS** ($T_A = T_{high}$, $V_{CC} = +15$ V, f = 20 kHz) | | | | | | | | | |
| Rise Time | 15 | $t_r$ | – | 40 | – | – | 40 | – | ns |
| Fall Time | 15 | $t_f$ | – | 150 | – | – | 150 | – | ns |
| Overlap Time | 15 | $t_{ov}$ | – | 275 | – | – | 275 | – | ns |
| Assymmetry (Duty Cycle = 50%) | 15 | $\frac{t_{on1} - t_{on2}}{t_{on1}}$ | – | ±1.0 | – | – | ±1.0 | – | % |

NOTE:

$T_{high}$ = +125°C for MC3520
+70°C for MC3420

$T_{low}$ = -55°C for MC3520
0°C for MC3420

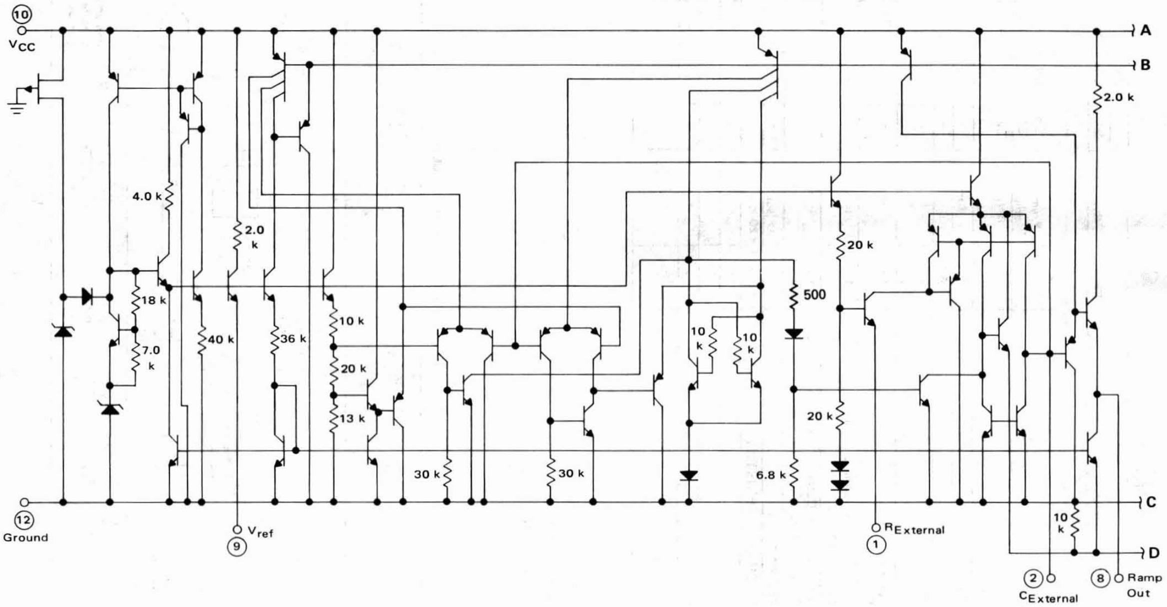
**FIGURE 2–EQUIVALENT CIRCUIT**



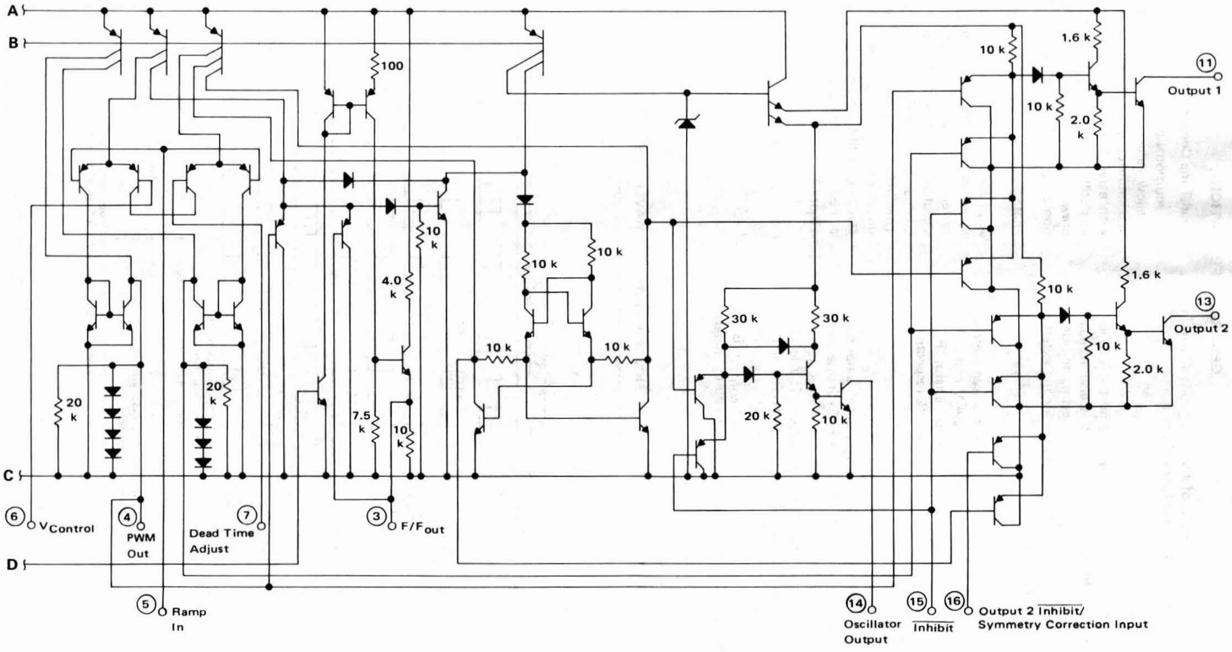
Ramp Out
8
Ramp In
5
$V_{control}$
6
PWM Out
4
Oscillator Output
14
$V_{CC}$
10
Output 1
11
Output 2
13
PWM
$V_{ref}$
Ramp Generator
T
Q
$\overline{Q}$
Dead Time
Dead Time Adjust
7
9
$V_{ref}$
1
$R_{ext}$
2
$C_{ext}$
3
F/F Out
12
Ground
15
$\overline{\text{Inhibit}}$
16
Symmetry Correction Input/Output 2 $\overline{\text{Inhibit}}$

FIGURE 3 – CIRCUIT SCHEMATIC

(continued next page)


10
VCC
12
Ground
9
Vref
4.0 k
18 k
7.0 k
40 k
2.0 k
36 k
10 k
20 k
13 k
30 k
30 k
10 k
10 k
500
20 k
20 k
6.8 k
2.0 k
10 k
1
RExternal
2
CExternal
8
Ramp Out
A
B
C
D

(continued) FIGURE 3 – CIRCUIT SCHEMATIC


A
B
C
D
100
10 k
4.0 k
7.5 k
10 k
20 k
20 k
10 k
10 k
10 k
10 k
30 k
30 k
20 k
10 k
10 k
1.6 k
10 k
2.0 k
10 k
1.6 k
10 k
2.0 k
⑥ V_Control
④ PWM Out
⑦ Dead Time Adjust
③ F/F_out
⑤ Ramp In
⑭ Oscillator Output
⑮ Inhibit
⑯ Output 2 Inhibit/ Symmetry Correction Input
⑪ Output 1
⑬ Output 2

## GENERAL INFORMATION

The internal block diagram of the MC3420 is shown in Figure 2, and consists of the following sections:

### Voltage Reference

A stable reference voltage is generated by the MC3420 primarily for internal use. However, it is also available externally at Pin 9 ($V_{ref}$) for use in setting the dead time (Pin 7) and for use as a reference for the external control loop error amplifiers.

### Ramp Generator

The ramp generator section produces a symmetrical triangular waveform ramping between 2.4 V and 6.0 V, with frequency determined by an external resistor ($R_{ext}$) and capacitor ($C_{ext}$) tied from Pins 1 and 2, respectively, to ground.

### PWM Comparator

The output of the ramp generator at pin 8 is normally connected to Pin 5, RAMP IN. The PWM (pulse width modulation) comparator compares the voltage at Pin 6 ($V_{control}$) to the ramp generator output. The level of $V_{control}$ determines the outputs' pulse width or duty cycle. The duty cycle of each output can vary, exclusive of dead time, from 50% (when $V_{control}$ is at approximately 2.4 V) to 0% ($V_{control}$ approximately 6.0 V).

### Dead Time Comparator

An additional comparator has been included in MC3420 to allow independent adjustment of system dead time or maximum duty cycle. By dividing down $V_{ref}$ at Pin 9 with a resistive divider or potentiometer, and applying this voltage to Pin 7, a stable dead time is obtained for prevention of inverter switching transistor cross conduction at high duty cycles due to storage time delays.

### Phase Splitter

A phase splitter is included to obtain two 180° out of phase outputs for use in multiple transistor inverter systems. It consists of a toggle flip-flop whose clock signal is derived by "ANDing" the output of the PWM comparator and a signal from the ramp generator section. This "AND" gate ensures that the outputs truly alternate under control loop transient conditions. Better understanding of this feature and MC3420 operation may be gained by studying the circuit waveforms, shown in Figure 4.

FIGURE 4 – INTERNAL WAVEFORMS

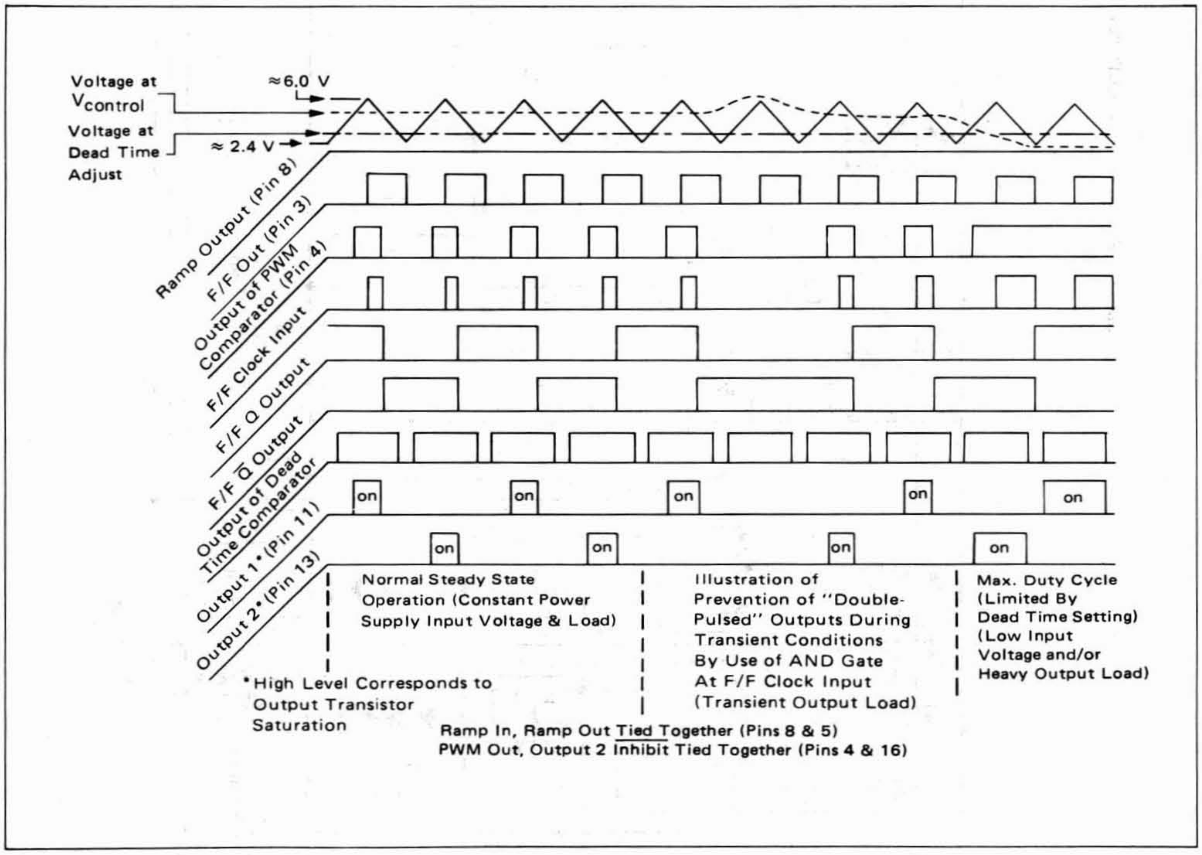

Voltage at $V_{control}$
≈6.0 V
Voltage at Dead Time Adjust
≈ 2.4 V
Ramp Output (Pin 8)
F/F Out (Pin 3)
Output of PWM Comparator (Pin 4)
F/F Clock Input
F/F Q Output
F/F $\bar{Q}$ Output
Output of Dead Time Comparator
Output 1* (Pin 11)
Output 2* (Pin 13)
on
Normal Steady State Operation (Constant Power Supply Input Voltage & Load)
Illustration of Prevention of "Double-Pulsed" Outputs During Transient Conditions By Use of AND Gate At F/F Clock Input (Transient Output Load)
Max. Duty Cycle (Limited By Dead Time Setting) (Low Input Voltage and/or Heavy Output Load)
*High Level Corresponds to Output Transistor Saturation
Ramp In, Ramp Out Tied Together (Pins 8 & 5)
PWM Out, Output 2 $\overline{\text{Inhibit}}$ Tied Together (Pins 4 & 16)

FIGURE 5 – STANDARD AC, DC TEST CIRCUIT

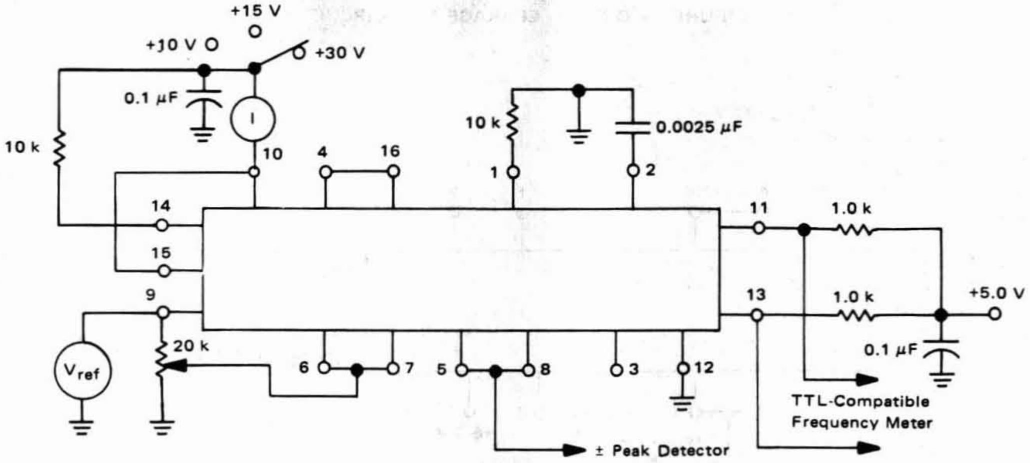

+15 V
+10 V
+30 V
0.1 µF
I
10 k
10
4
16
10 k
0.0025 µF
1
2
14
15
9
11
13
1.0 k
1.0 k
+5.0 V
0.1 µF
20 k
Vref
6
7
5
8
3
12
TTL-Compatible
Frequency Meter
± Peak Detector

FIGURE 6 – FREQUENCY LIMIT TEST CIRCUIT

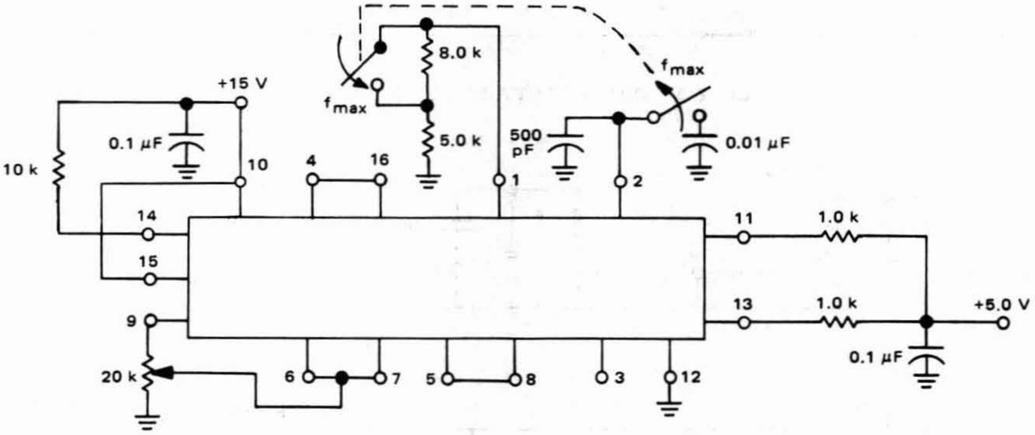
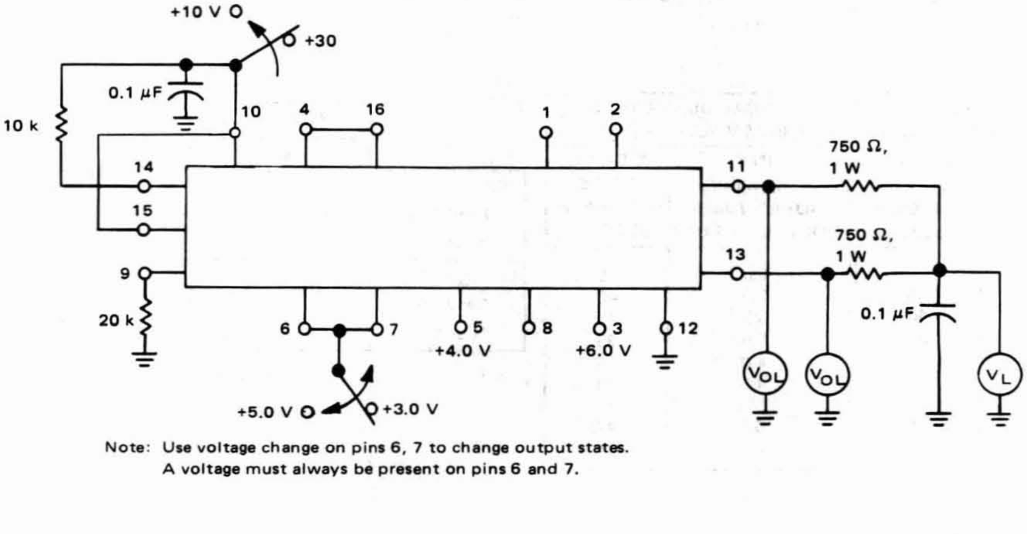
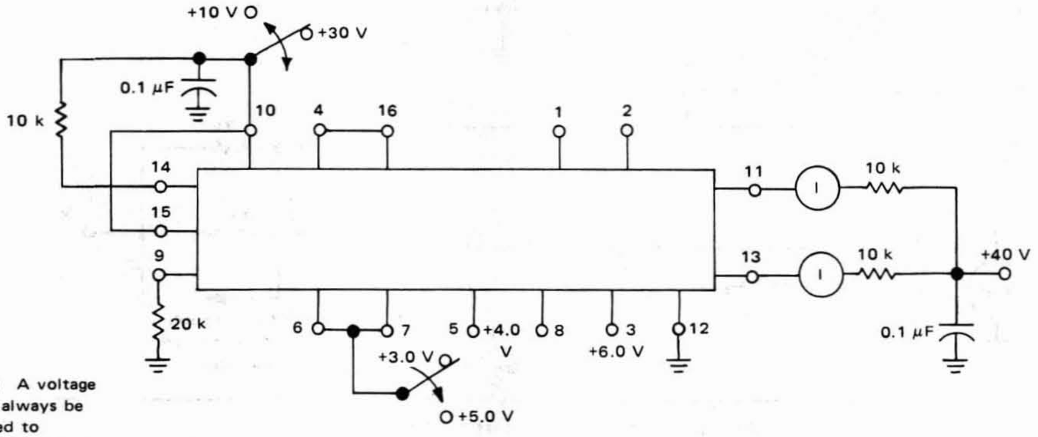

8.0 k
fmax
fmax
+15 V
5.0 k
500
pF
0.01 µF
0.1 µF
10 k
10
4
16
1
2
14
15
9
11
13
1.0 k
1.0 k
+5.0 V
0.1 µF
20 k
6
7
5
8
3
12

FIGURE 7 – OUTPUT SATURATION TEST CIRCUIT


+10 V
+30
0.1 µF
10 k
10
4
16
1
2
14
15
9
11
13
750 Ω,
1 W
750 Ω,
1 W
0.1 µF
20 k
6
7
5
8
3
12
+4.0 V
+6.0 V
+5.0 V
+3.0 V
VOL
VOL
VL

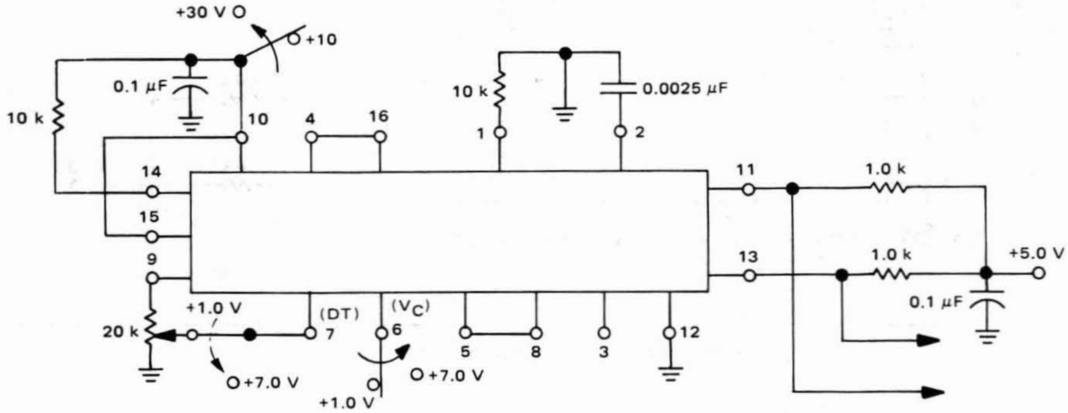
Note: Use voltage change on pins 6, 7 to change output states.
A voltage must always be present on pins 6 and 7.

FIGURE 8 – OUTPUT LEAKAGE TEST CIRCUIT


+10 V
+30 V
0.1 µF
10 k
10
4
16
1
2
14
15
9
11
10 k
13
10 k
+40 V
20 k
6
7
5
+4.0 V
8
3
+6.0 V
12
+3.0 V
+5.0 V
0.1 µF

Note: A voltage must always be applied to pins 6 and 7.

FIGURE 9 – OUTPUT DUTY CYCLE TEST CIRCUIT


+30 V
+10
0.1 µF
10 k
10
4
16
10 k
1
0.0025 µF
2
14
15
9
11
1.0 k
13
1.0 k
+5.0 V
0.1 µF
20 k
+1.0 V
(DT)
7
(V_C)
6
+7.0 V
+1.0 V
+7.0 V
5
8
3
12

| TYPICAL DUTY CYCLE versus DEAD TIME VOLTAGE | |
|---|---|
| PIN 7. DEAD TIME VOLTAGE (V) ($V_{control}$ = 2.0 V) | % DUTY CYCLE (FOR EACH OUTPUT) |
| 2.0 | 50 |
| 2.5 | 46 |
| 3.0 | 40 |
| 3.5 | 33 |
| 4.0 | 26 |
| 4.5 | 18 |
| 5.0 | 11 |
| 5.5 | 4.0 |
| 6.0 | 0 |

| TYPICAL DUTY CYCLE versus PWM VOLTAGE ($V_{control}$) | |
|---|---|
| PIN 6. $V_{control}$ (V) (DEAD TIME VOLTAGE = 1.0 V) | % DUTY CYCLE (FOR EACH OUTPUT) |
| 2.0 | 50 |
| 2.5 | 46 |
| 3.0 | 40 |
| 3.5 | 33 |
| 4.0 | 26 |
| 4.5 | 18 |
| 5.0 | 11 |
| 5.5 | 4.0 |
| 6.0 | 0 |

| | $V_6$ | $V_7$ | |
|---|---|---|---|
| | Volts | | |
| 100% Adjust | | | |
| Dead Time | 1.0 | 1.0 | (Pin 11 + Pin 13 = Logic "1") |
| Pulse Width | 1.0 | 1.0 | |
| 0% Adjust | | | |
| Dead Time | 7.0 | 1.0 | (Pin 11)(Pin 13) = Logic "1" |
| Pulse Width | 1.0 | 7.0 | |

NOTE: Logic "1" is TTL-Compatible $V_{OH}$.

FIGURE 10 – INHIBIT/SYMMETRY TEST CIRCUIT

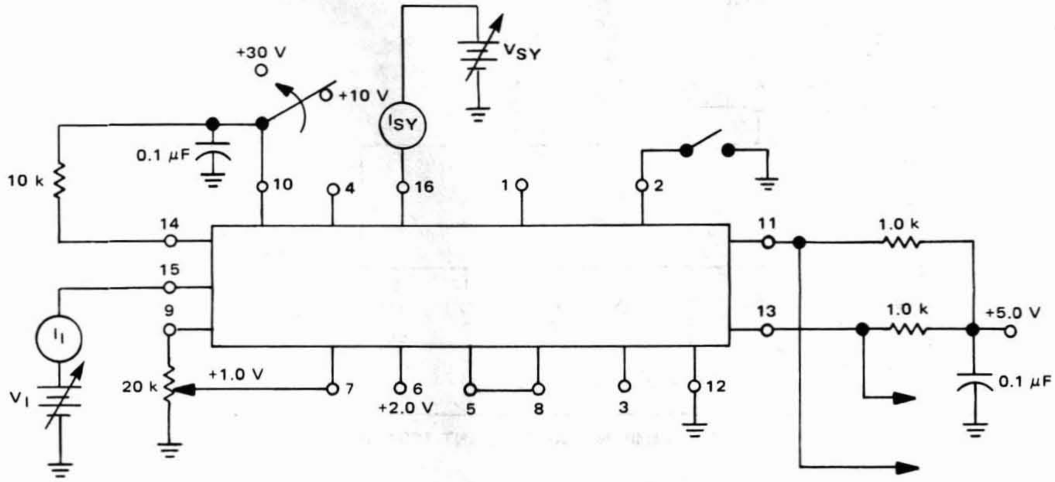

+30 V
+10 V
$V_{SY}$
$I_{SY}$
0.1 µF
10 k
10
4
16
1
2
14
11
1.0 k
15
9
13
1.0 k
+5.0 V
$I_I$
$V_I$
20 k
+1.0 V
7
6
+2.0 V
5
8
3
12
0.1 µF

FIGURE 11 – OSCILLATOR OUTPUT (pin 14) TEST CIRCUIT

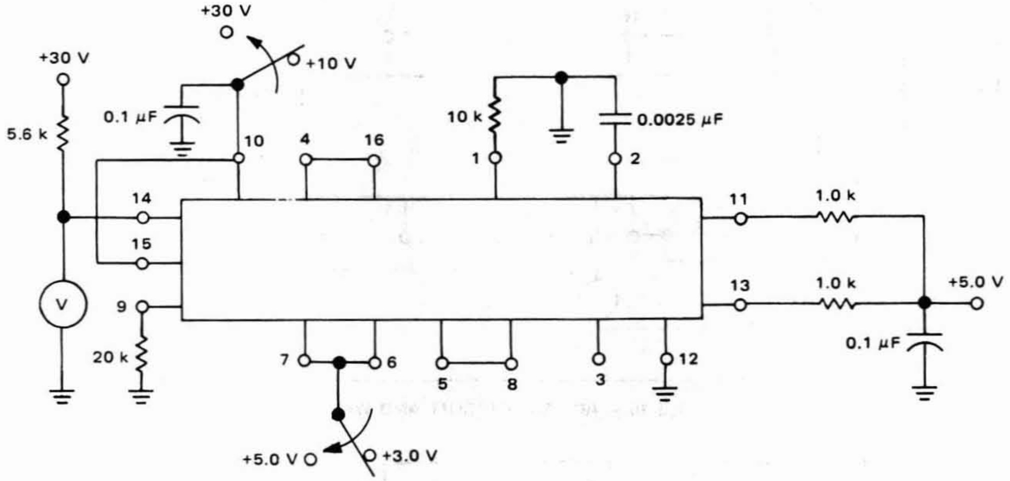

+30 V
+30 V
+10 V
5.6 k
0.1 µF
10
4
16
10 k
1
0.0025 µF
2
14
15
11
1.0 k
13
1.0 k
+5.0 V
V
9
20 k
7
6
5
8
3
12
0.1 µF
+5.0 V
+3.0 V

FIGURE 12 – $V_{Control}$ BIAS CURRENT TEST CIRCUIT

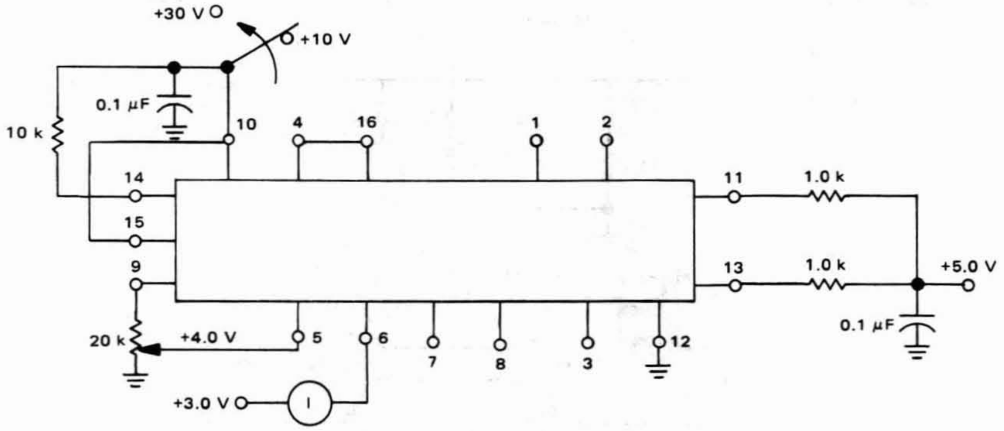

+30 V
+10 V
0.1 µF
10 k
10
4
16
1
2
14
15
9
11
1.0 k
13
1.0 k
+5.0 V
0.1 µF
20 k
+4.0 V
5
6
7
8
3
12
+3.0 V
I

FIGURE 13 – DEAD TIME BIAS CURRENT TEST CIRCUIT

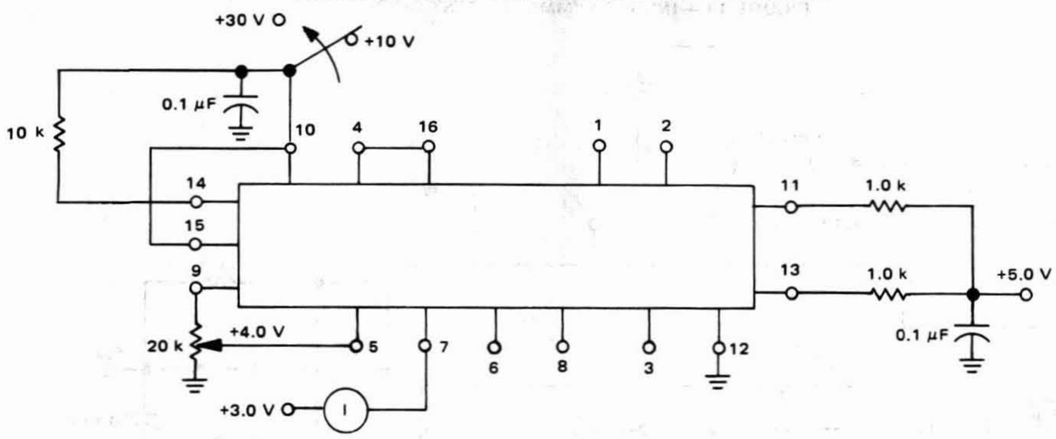

+30 V
+10 V
0.1 µF
10 k
10
4
16
1
2
14
15
9
11
1.0 k
13
1.0 k
+5.0 V
0.1 µF
20 k
+4.0 V
5
7
6
8
3
12
+3.0 V
I

FIGURE 14 – RAMP IN BIAS CURRENT TEST CIRCUIT

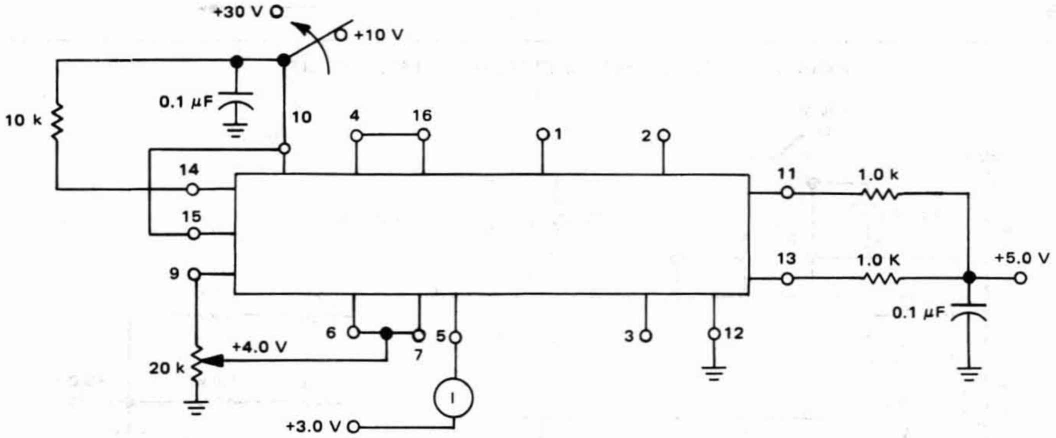
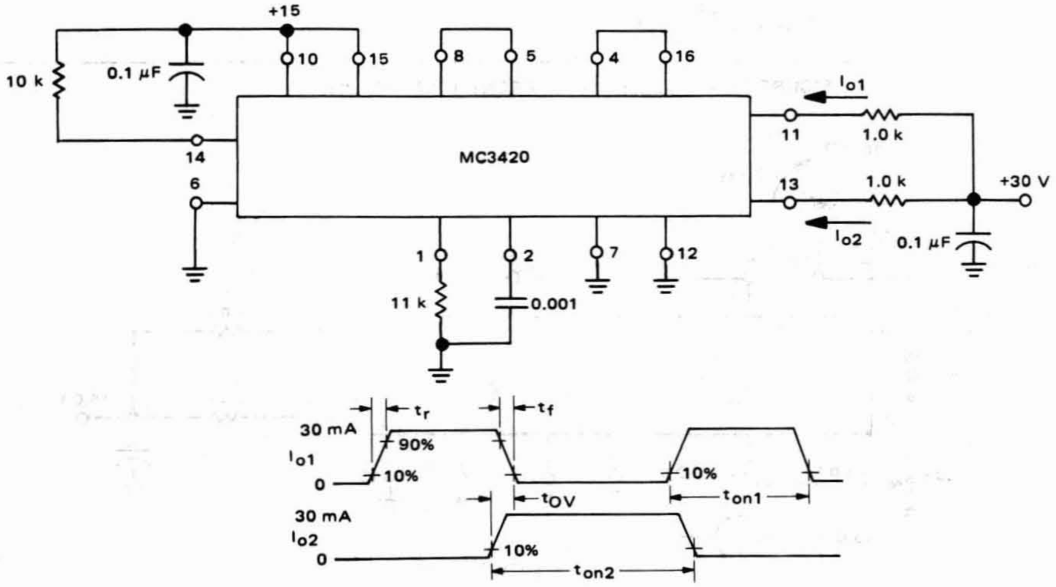

+30 V
+10 V
0.1 µF
10 k
10
4
16
1
2
14
15
9
11
1.0 k
13
1.0 K
+5.0 V
0.1 µF
6
7
5
3
12
+4.0 V
20 k
I
+3.0 V

FIGURE 15 – AC TEST CIRCUIT AND WAVEFORMS


+15
10 k
0.1 µF
10
15
8
5
4
16
$I_{o1}$
11
1.0 k
14
MC3420
6
13
1.0 k
+30 V
$I_{o2}$
0.1 µF
1
2
7
12
11 k
0.001
$t_r$
$t_f$
30 mA
90%
$I_{o1}$
0
10%
10%
$t_{OV}$
$t_{on1}$
30 mA
$I_{o2}$
0
10%
$t_{on2}$

## TYPICAL CHARACTERISTICS

FIGURE 16 – OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

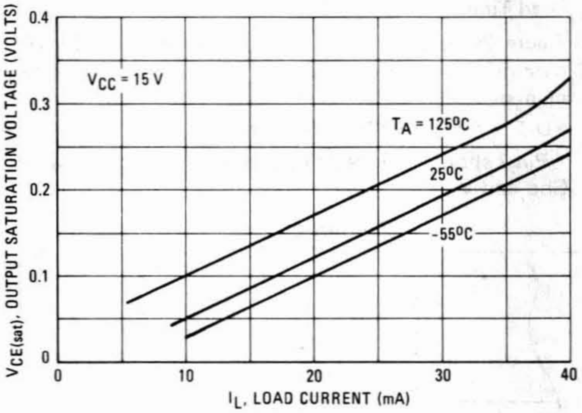


FIGURE 17 – REFERENCE VOLTAGE versus REFERENCE CURRENT

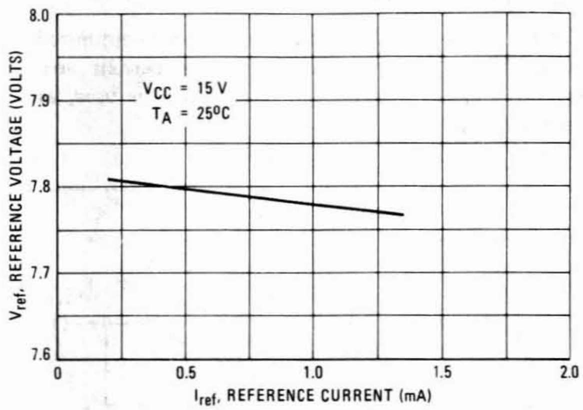


FIGURE 18 – DRAIN CURRENT versus EXTERNAL RESISTANCE

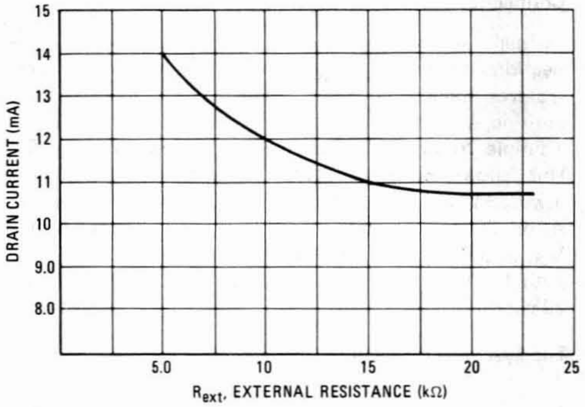


FIGURE 19 – PEAK FLIP-FLOP$_{out}$ VOLTAGE versus EXTERNAL RESISTANCE

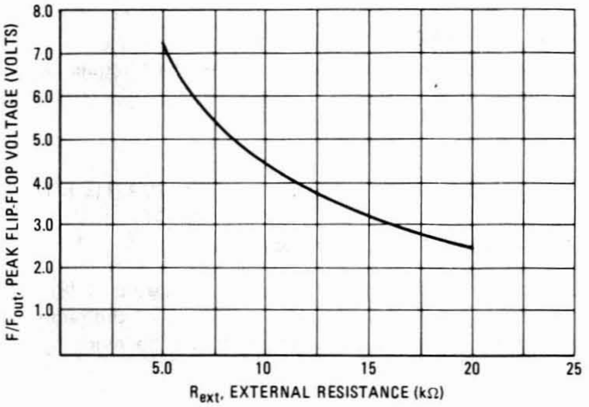


FIGURE 20 – DRAIN CURRENT versus TEMPERATURE

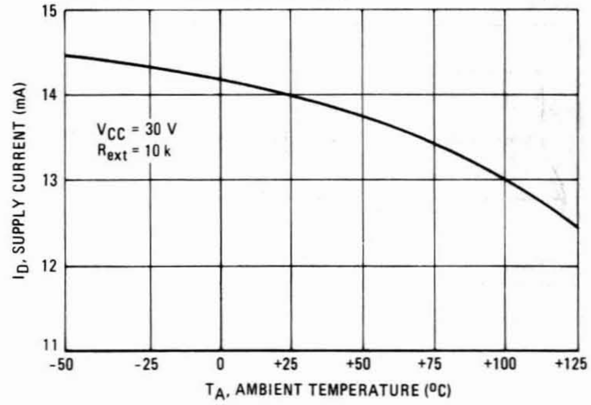
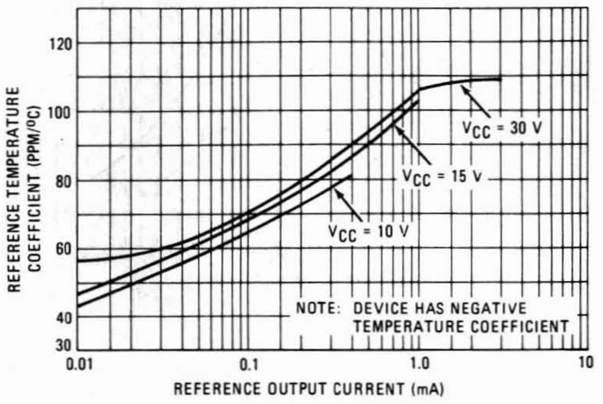


FIGURE 21 – REFERENCE VOLTAGE TEMPERATURE COEFFICIENT versus OUTPUT CURRENT

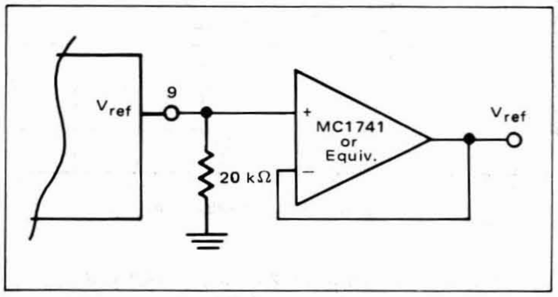


## OPERATION AND APPLICATIONS INFORMATION

### The Voltage Reference

The temperature coefficient of $V_{ref}$ has been optimized for a 400 $\mu$A ($\cong$20 k$\Omega$) load. If increased current capability is required, an op amp buffer may be used, as shown in Figure 22.

FIGURE 22


Vref
9
20 kΩ
+
−
MC1741
or
Equiv.
Vref

### Output Frequency

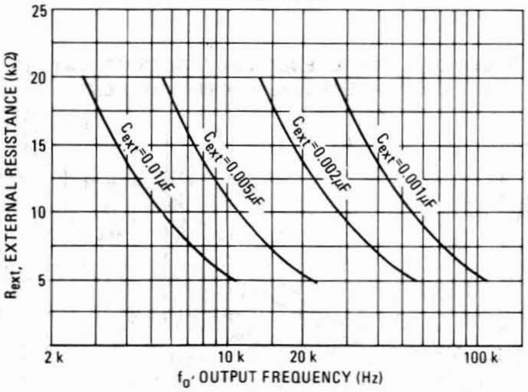
The values of $R_{ext}$ and $C_{ext}$ for a given output frequency, $f_o$, can be found from:

$$f_o \cong \frac{0.55}{R_{ext}\,C_{ext}}\;;\; 5.0\ \text{k}\Omega \leqslant R_{ext} \leqslant 20\ \text{k}\Omega \quad \text{(Eq. 1)}$$

or from the graph shown in Figure 23.

Note that $f_o$ refers to the frequency of Output 1 (Pin 11) or Output 2 (Pin 13). The frequency of the ramp generator output waveform at Pin 8 will be twice $f_o$.

FIGURE 23

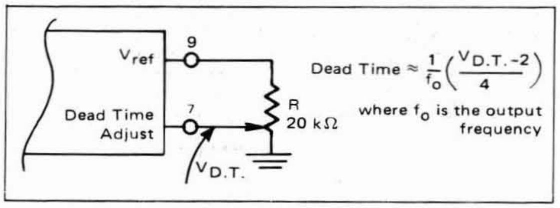


### Dead Time

Figure 24 illustrates how to set or adjust the MC3420 outputs' dead time or maximum duty cycle. For minimum dead time drift with temperature or supply voltage, $V_{D.T.}$ should be derived from $V_{ref}$ as shown.

**Pin 7 should always be tied to some voltage between Gnd and $V_{ref}$.**

FIGURE 24


Vref
9
Dead Time
Adjust
7
R
20 kΩ
VD.T.
Dead Time ≈ 1/fo ((VD.T. − 2)/4)
where fo is the output frequency

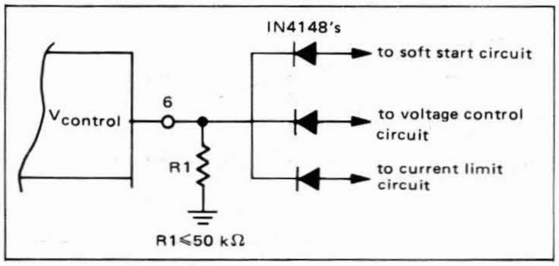
### Connections to the $V_{control}$ Pin

In many systems, it is necessary to make multiple connections to the $V_{control}$ Pin in order to implement features in addition to voltage regulation such as current limiting, soft start, etc. These can be made by the use of a simple "diode-OR" connection, as shown in Figure 25. This allows whichever control element is seeking the lowest PWM duty cycle to dominate. Note that a resistor, R1, whose value is $\leqslant$ 50 k$\Omega$ is placed from the $V_{control}$ Pin to ground. This is necessary to provide a dc path for the PWM comparator input bias current under all conditions.

The system duty cycle is given by:

$$\text{D.C. (\%)} \cong \frac{V_{Control} - 2}{4} \times 100 \qquad \text{(Eq. 2)}$$

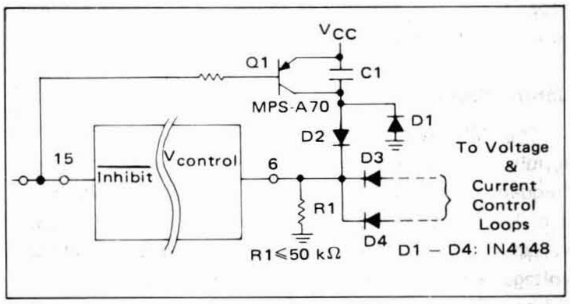
FIGURE 25


IN4148's
to soft start circuit
to voltage control circuit
to current limit circuit
Vcontrol
6
R1
R1≤50 kΩ

### Soft Start

In most PWM switching supplies, a soft start feature is desired to prevent output voltage overshoots and magnetizing current imbalances in the power transformer primary. This feature forces the duty cycle of the switching elements to gradually increase from zero to their normal operating point during initial system power-up or after an inhibit. This feature can be easily implemented with the MC3420. One method is shown in Figure 26.

FIGURE 26


VCC
Q1
C1
MPS-A70
D1
D2
15
Inhibit
Vcontrol
6
D3
To Voltage
&
Current
Control
Loops
R1
D4
R1≤50 kΩ
D1 – D4: IN4148

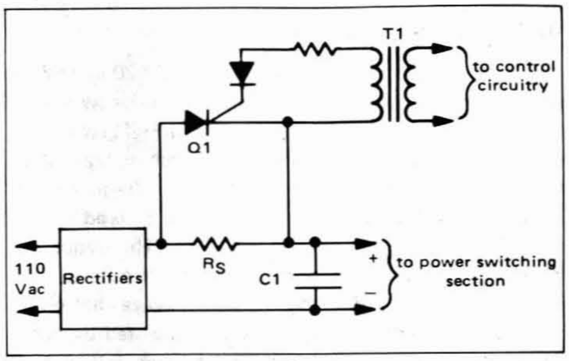
After an inhibit command or during power-up, the voltage on R1 and Pin 6 exponentially decays from $V_{CC}$ toward ground with a time constant of R1C1, allowing a gradual increase in duty cycle. Diodes D2 – D4 provide a diode-or function at the $V_{control}$ Pin, while Q1 serves to reset the timing capacitor, C1, when an inhibit command is received thereby reinitializing the soft-start feature. D1 allows C1 to reset when power ($V_{CC}$) is turned off.

### Inrush Current Limiting

Since many PWM switching supplies are operated directly off the rectified 110 Vac line with capacitive input filters, some means of preventing rectifier failure due to inrush surge currents is usually necessary. One method which can be used is shown in Figure 27.

In this circuit, a series resistor, $R_S$, is used to provide inrush surge current limiting. After the filter capacitor, C1, is charged, Q1 receives a trigger signal from the control circuitry through T1 and shorts $R_S$ out of the circuit, eliminating its otherwise larger power dissipation. The trigger signal for Q1 may be derived from either the oscillator output (Pin 14) or one of the MC3420's outputs. If the oscillator output is used, it will be necessary to provide a time delay on the inhibit pin to keep it low until the input filter capacitor, C1, has had time to charge, whereas the initial portion of the soft start timing cycle can be used for this delay if this signal is derived from one of the output pins. However, using the Oscillator Output Pin does offer the advantage that its waveform has a constant 50% duty cycle, independent of the outputs' duty cycle which can simplify the design of a drive circuit for T1.

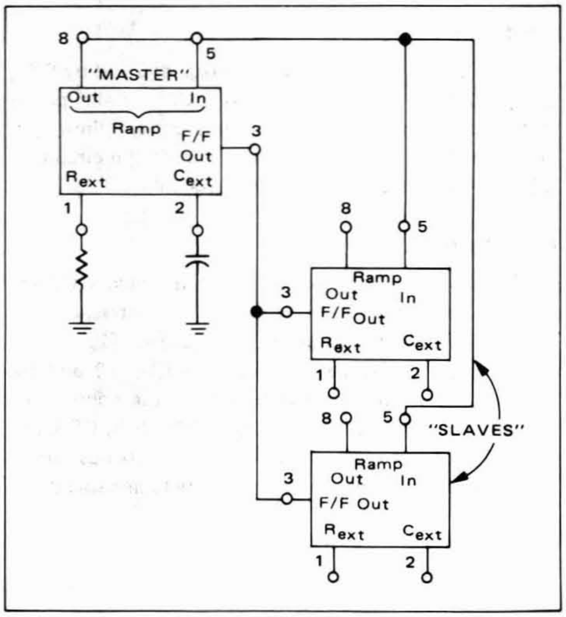
FIGURE 27


T1
to control circuitry
Q1
110 Vac
Rectifiers
RS
C1
+
–
to power switching section

### Slaving

In some applications, as when one PWM inverter/converter is used to feed another, it may be desired that their frequencies be synchronized. This can be done with multiple MC3420s as shown in Figure 28. By omitting their $R_{ext}$ and $C_{ext}$, up to two MC3420s may be slaved to a master MC3420.

FIGURE 28 – SLAVING THE MC3420


8
5
"MASTER"
Out
In
Ramp
F/F Out
3
Rext
Cext
1
2
8
5
Ramp
Out
In
3
F/F Out
Rext
Cext
1
2
8
5
"SLAVES"
Ramp
Out
In
3
F/F Out
Rext
Cext
1
2

### 15 V, 2 A DC-to-DC Converter

Figure 29 illustrates the use of the MC3520 in a PWM switching power supply utilizing a single series switching element (see Appendix for description of PWM switching supply configurations). The series switching transistor, Q1, chops the dc input voltage, $V_{in}$, at a frequency of ≅ 25 kHz, and the resulting waveform is filtered by L1 and C1 to provide the dc output voltage. The frequency is set by R4 and C3, and since the outputs of the MC3520 are wire-ORed together, fo is twice that given by Equation 1 and Figure 23. $V_o$ is regulated by comparing its value to the MC3520's reference voltage and amplifying the error voltage with U1. The output of U1 is fed into the MC3520 to provide PWM to Q1, thereby controlling its duty cycle and thus the value of $V_o$.

C2 provides a soft-start feature during power up to prevent output voltage overshoots and excessive start up currents through Q1.

Short circuit protection is provided by $R_{SC}$, Q3 and Q4. When an overcurrent condition occurs, Q3 is turned on by the voltage across $R_{SC}$; Q3 drives Q4 on, which raises the voltage at pin 6 ($V_{control}$) of the MC3520, reducing Q1's duty cycle and maintaining a constant output current of ≅ 2.5 A.

### 5 V, 50 A Line-Operated Supply

A 5 V, 50 A line-operated 20 kHz switching power supply using the MC3520 is shown in Figures 30a and b. An explanation of the operation of each section of the supply follows.

#### Input Section

The 120 Vac line is full wave voltage doubled by CR1, CR2, C1 and C2 to provide 310 Vdc to the power section of the supply. Inrush surge current limiting is provided by R1, which is shorted out of the circuit by Q1 after C1 and C2 are initially charged.

#### Power Section

The supply utilizes two switching transistors, Q2 and Q3, in a half-bridge configuration (see Appendix) to drive the high frequency power transformer, T2.

The bases of Q2 and Q3 are driven by T3 and T4, respectively, to provide isolation from the control and base drive sections of the supply. CR3, CR5, CR6, and CR8 constitute anti-saturation (Baker) clamps which provide increased and more uniform switching speeds for Q2 and Q3. CR4 and CR7 allow reverse base currents during turn off.

#### Output Section

The output of T2 is rectified by Schottky diodes, CR9 and CR10. VR1 is a transient suppressor to protect CR9 and CR10 from transients that might cause reverse breakdown. L1 and C4 constitute the output filter. C4 should have very low ESR (equivalent series resistance) at 20 kHz to provide the most effective filtering. L2 and C5 make up a high-frequency filter to reduce commutation spikes which pass L1 due to its interwinding capacitance. $R_{SC}$ provides output overcurrent sensing to the control section.

#### Control Section

The MC3520 provides the PWM control for the supply. R2 is adjusted to obtain a 20 kHz operating frequency. R3 adjusts the dead time (≅ 5 μs each half-cycle). U1A and U1B are the output current and output voltage error amplifiers, respectively. R5 sets the output voltage while R4 determines the output current limit. C7 and C8 are the current and voltage loop compensation capacitors.

C6 provides the soft-start feature while Q4 ensures a soft-start after each system inhibit (pin 15 low).

#### Base Drive Section

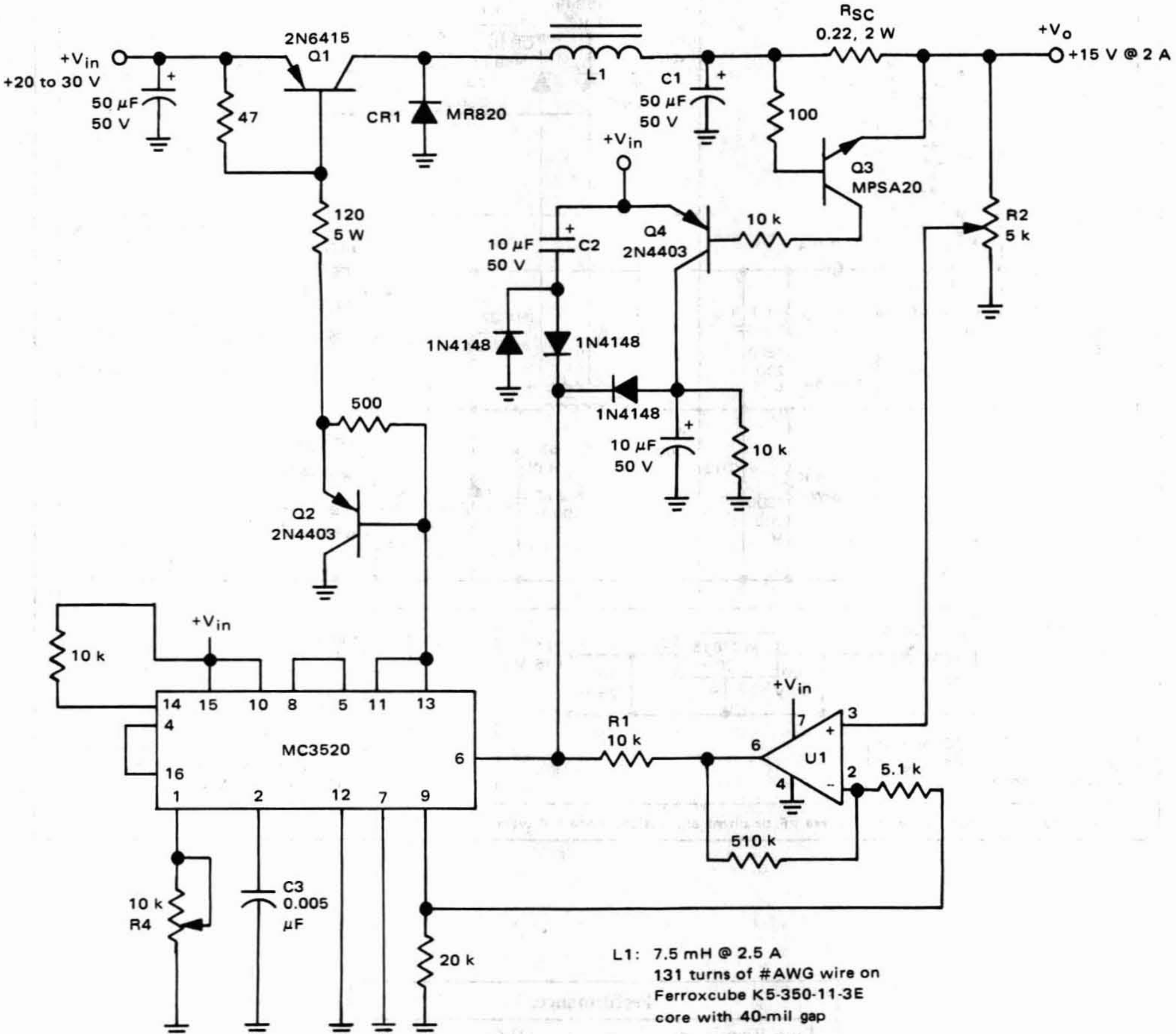
Turn on drive to the power section switching transistors occurs when each of the outputs of the MC3520 saturate. Q5 or Q6 are therefore turned on, and 15 V applied to the primaries of T3 or T4, supplying forward base drive to Q2 or Q3.

Turn off drive occurs when Q5 or Q6 turn off, and the magnetizing energy stored in T3 or T4's core is transformed into a negative "flyback" voltage at their secondaries, providing reverse base drive to Q2 or Q3. CR11 and CR12 act as clamps, to prevent this flyback voltage from exceeding -5 V at T3 or T4's secondary (30 V on Q5 or Q6's collector).

#### Q1 Driver Section

Q7 and T1 provide the gate drive to Q1. Q7 starts operating after an initial delay of 100 ms created by the soft-start circuit, thereby allowing C1 and C2 to charge up before firing Q1.

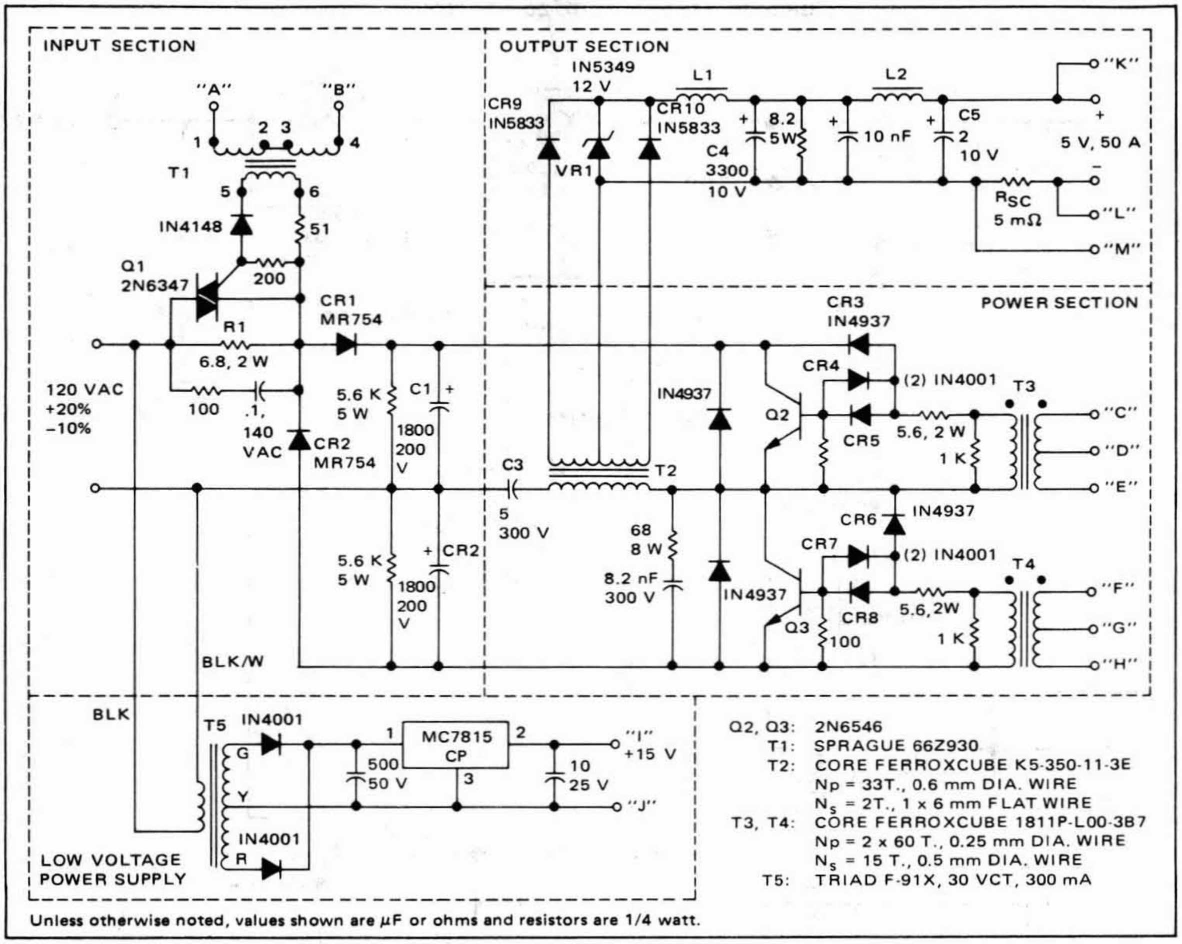
FIGURE 29 — 15 V, 2A DC-TO-DC CONVERTER


+Vin
+20 to 30 V
50 µF
50 V
47
2N6415
Q1
CR1
MR820
L1
C1
50 µF
50 V
RSC
0.22, 2 W
100
Q3
MPSA20
+Vo
+15 V @ 2 A
R2
5 k
+Vin
10 µF
50 V
C2
Q4
2N4403
10 k
120
5 W
1N4148
1N4148
1N4148
10 µF
50 V
10 k
500
Q2
2N4403
10 k
+Vin
14
15
10
8
5
11
13
4
MC3520
6
16
1
2
12
7
9
R1
10 k
+Vin
7
3
6
U1
4
2
5.1 k
510 k
10 k
R4
C3
0.005
µF
20 k

L1: 7.5 mH @ 2.5 A
131 turns of #AWG wire on
Ferroxcube K5-350-11-3E
core with 40-mil gap

U1: MC1741CP1

**FIGURE 30a – 5 V, 50A LINE-OPERATED SUPPLY** (continued on following page)

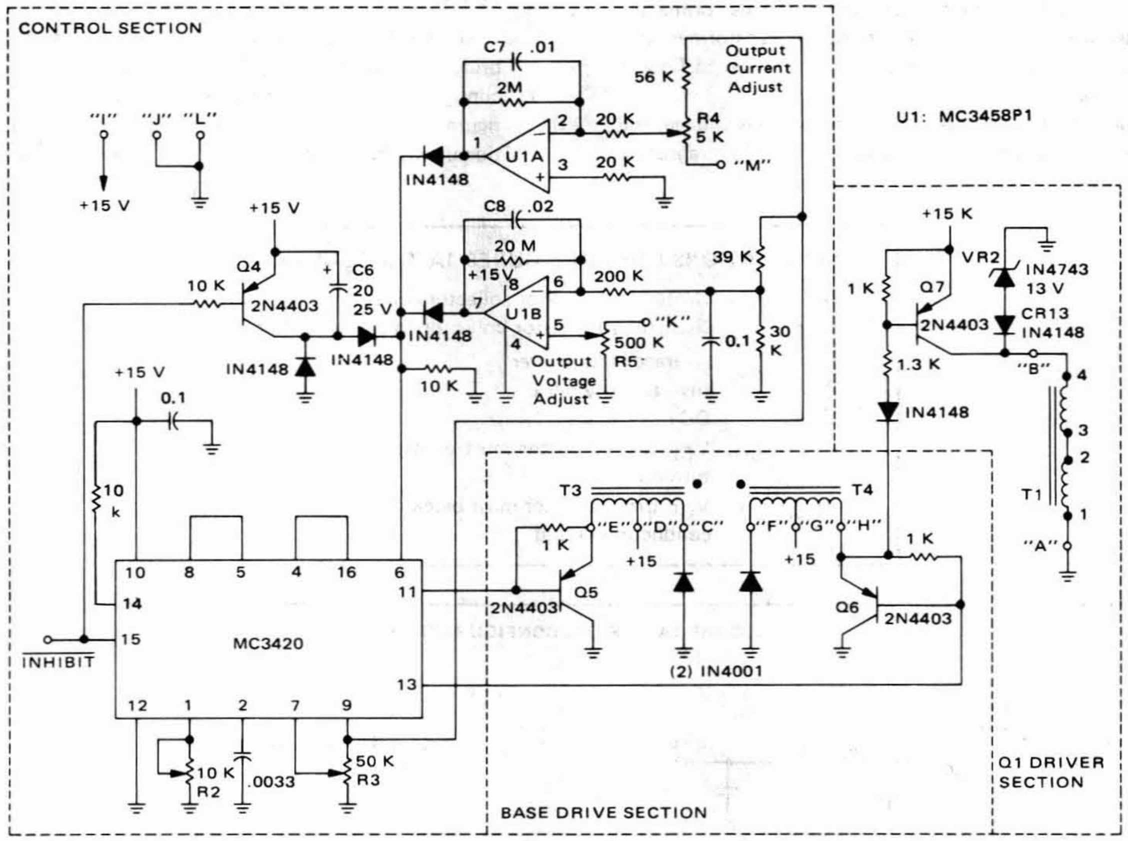

INPUT SECTION
"A"
"B"
1
2 3
4
T1
5
6
IN4148
51
Q1
2N6347
200
R1
6.8, 2 W
CR1
MR754
120 VAC
+20%
−10%
100
.1,
140
VAC
CR2
MR754
5.6 K
5 W
C1
1800
200
V
CR2
BLK/W
BLK
OUTPUT SECTION
IN5349
12 V
L1
L2
"K"
CR9
IN5833
CR10
IN5833
VR1
8.2
5W
C4
3300
10 V
10 nF
C5
2
10 V
5 V, 50 A
+
−
RSC
5 mΩ
"L"
"M"
POWER SECTION
CR3
IN4937
CR4
(2) IN4001
T3
IN4937
Q2
CR5
5.6, 2 W
1 K
"C"
"D"
"E"
C3
5
300 V
T2
68
8 W
8.2 nF
300 V
CR6
IN4937
CR7
(2) IN4001
T4
IN4937
Q3
CR8
5.6,2W
100
1 K
"F"
"G"
"H"
T5
IN4001
G
Y
R
1
MC7815
CP
2
3
500
50 V
10
25 V
"I"
+15 V
"J"
LOW VOLTAGE
POWER SUPPLY

Q2, Q3: 2N6546
T1: SPRAGUE 66Z930
T2: CORE FERROXCUBE K5-350-11-3E
Np = 33T., 0.6 mm DIA. WIRE
$N_s$ = 2T., 1 x 6 mm FLAT WIRE
T3, T4: CORE FERROXCUBE 1811P-L00-3B7
Np = 2 x 60 T., 0.25 mm DIA. WIRE
$N_s$ = 15 T., 0.5 mm DIA. WIRE
T5: TRIAD F-91X, 30 VCT, 300 mA

Unless otherwise noted, values shown are μF or ohms and resistors are 1/4 watt.

| Performance | |
|---|---|
| Line Regulation: | 0.4% |
| Load Regulation: | 0.25% |
| Output Ripple and Noise: | 60 mV p-p<br>25 mV rms |
| Line current surge at turn-on: | 35 A max |
| Efficiency: | 80% |

**FIGURE 30b**


CONTROL SECTION
C7
.01
2M
Output
Current
Adjust
56 K
R4
5 K
20 K
20 K
"M"
U1A
U1: MC3458P1
"I"
"J"
"L"
+15 V
+15 V
IN4148
C8
.02
20 M
39 K
Q4
C6
20
25 V
10 K
2N4403
+15 V
U1B
200 K
"K"
500 K
R5
0.1
30 K
IN4148
IN4148
IN4148
Output
Voltage
Adjust
10 K
+15 V
0.1
+15 K
VR2
IN4743
13 V
CR13
IN4148
1 K
Q7
2N4403
1.3 K
"B"
IN4148
T3
T4
T1
"E"
"D"
"C"
"F"
"G"
"H"
1 K
+15
+15
1 K
"A"
10 k
MC3420
Q5
2N4403
Q6
2N4403
(2) IN4001
INHIBIT
10 K
R2
.0033
50 K
R3
BASE DRIVE SECTION
Q1 DRIVER
SECTION

Unless otherwise noted, values shown are μF or ohms and resistors are 1/4 watt.

## APPENDIX: BASIC PWM SWITCHING SUPPLY POWER CIRCUIT CONFIGURATIONS

The material given in this section is intended to acquaint the designer with the basic switching transistor configurations used in PWM power supplies. Circuit configurations, collector voltage and current waveforms of the switching transistors, and required transistor specifications for the most commonly utilized configurations are shown in Figures 1A through 4A. It should be noted that the waveforms and specifications are idealized, in that the effects of leakage inductance voltage spikes, stray circuit capacitance, snubber networks, clamp diode overshoots, diode reverse recovery and saturation voltages have been neglected. For more information on these effects, the configurations, or switching supplies in general, consult the references listed in the References section.

### Series Configuration

The single transistor series configuration is shown in Figure 1A. This configuration is usually limited to applications in which $0.2\ V_{CC} < V_o < 0.8\ V_{CC}$ and where input-output isolation is not required.

### Push-Pull Configuration

Figure 2A shows the two-transistor push-pull configuration. Unlike the series configuration, it can be used to either step-up or step-down the input voltage, $V_{CC}$, and also provides input-output isolation. It does, however, have the disadvantage that additional circuitry must be used to provide symmetry correction for the prevention of transformer saturation.

### Half-Bridge Configuration

The half-bridge configuration, shown in Figure 3A, does not suffer from the symmetry problems of the push-pull configuration since the transformer primary is capacitively coupled. This prevents transformer core saturation since no net dc current is allowed to flow in its primary.

Note that for the same input power, bus voltage, and duty cycle, the half-bridge requires switching transistors which have twice the current and half the voltage requirements as those of the push-pull configuration.

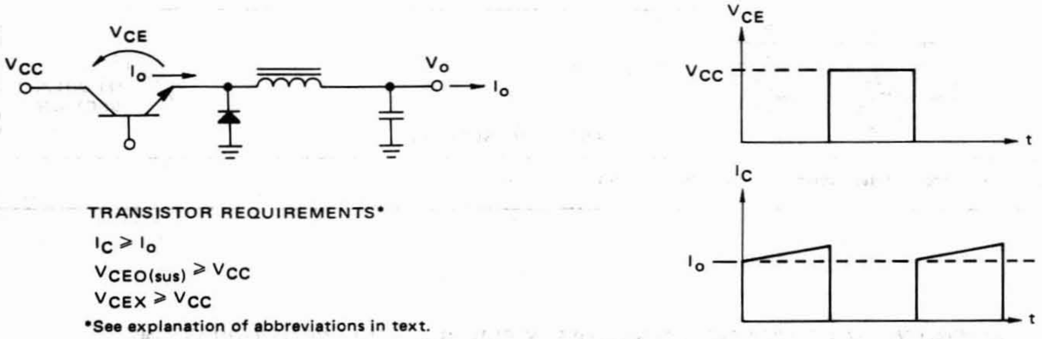
### Full-Bridge Configuration

By replacing the bridge capacitors, C, of the half-bridge configuration of Figure 4A results. With this configuration, double the power of the half-bridge configuration can be obtained at the expense of two additional switching transistors and their associated circuitry.

### ABBREVIATIONS USED IN FIGURES 1A THROUGH 4A

| | |
|---|---|
| $I_C$: | Switching transistor collector current |
| $V_{CE}$: | Switching transistor collector-to-emitter-voltage |
| $P_{in}$: | Average input power |
| D.C.: | Inverter duty cycle |
| $V_{CC}$: | DC bus voltage |
| $V_{CEO(sus)}$: | $V_{CE}$ that transistor must withstand during turn-on |
| $V_{CEX}$: | $V_{CE}$ that transistor must block during non-conduction period. |

FIGURE 1A – SERIES CONFIGURATION



TRANSISTOR REQUIREMENTS*

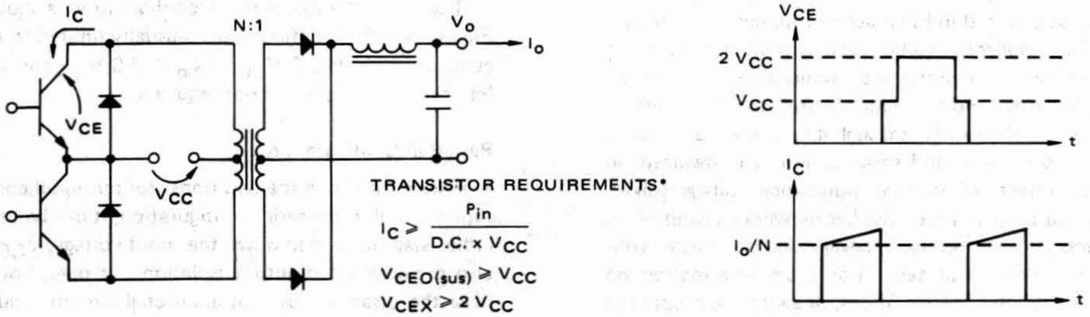
$I_C \geq I_o$

$V_{CEO(sus)} \geq V_{CC}$

$V_{CEX} \geq V_{CC}$

*See explanation of abbreviations in text.

FIGURE 2A – PUSH-PULL CONFIGURATION



TRANSISTOR REQUIREMENTS*

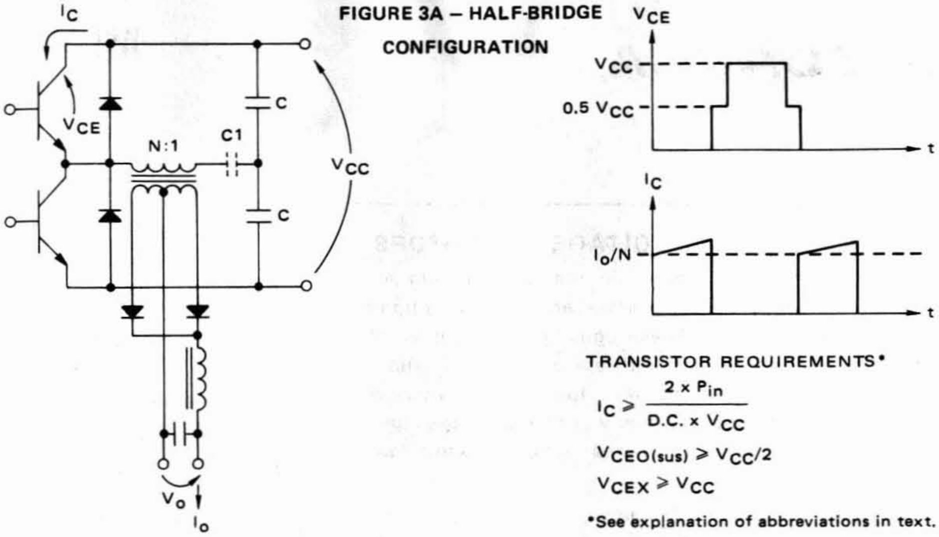
$I_C \geq \frac{P_{in}}{D.C. \times V_{CC}}$

$V_{CEO(sus)} \geq V_{CC}$

$V_{CEX} \geq 2\,V_{CC}$

*See explanation of abbreviations in text.

FIGURE 3A – HALF-BRIDGE CONFIGURATION



TRANSISTOR REQUIREMENTS*

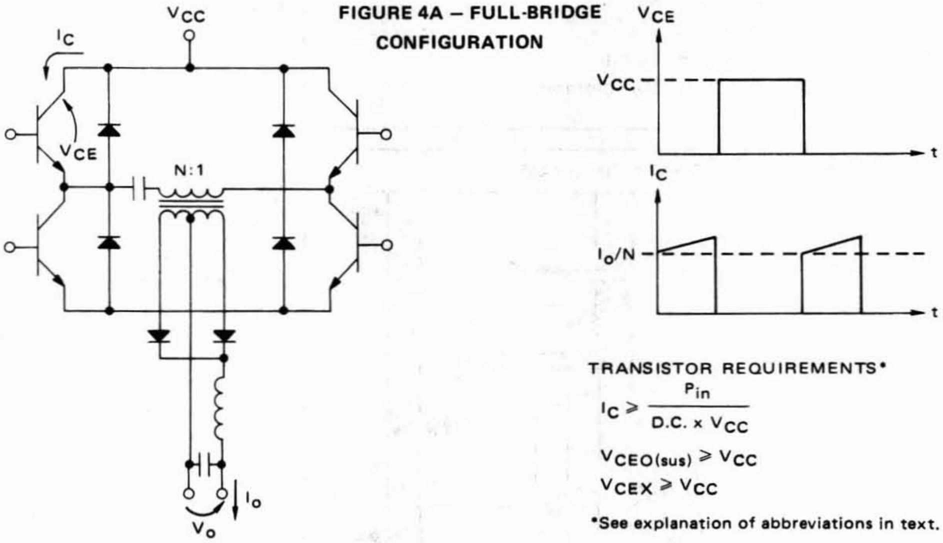
$$I_C \geq \frac{2 \times P_{in}}{D.C. \times V_{CC}}$$

$V_{CEO(sus)} \geq V_{CC}/2$

$V_{CEX} \geq V_{CC}$

*See explanation of abbreviations in text.

FIGURE 4A – FULL-BRIDGE CONFIGURATION



TRANSISTOR REQUIREMENTS*

$$I_C \geq \frac{P_{in}}{D.C. \times V_{CC}}$$

$V_{CEO(sus)} \geq V_{CC}$

$V_{CEX} \geq V_{CC}$

*See explanation of abbreviations in text.

## REFERENCES

More detailed information on switching power supplies may be obtained by consulting the following articles:

1. L. Jansson: "A Survey of Converter Circuits for SMPS," Mullard Technical Communications #119, July 1973.
2. R. Haver: "A New Approach to Switching Regulators," Motorola AN-719, May 1974.
3. R. Haver: "Switched Mode Power Supplies, a 5 V, 40 A Design," Motorola AN-737, December 1974.
4. W. Hersom: "Optimizing the High Current Transistor Converter," *Solid State Power Conversion,* March/April 1975.
5. W. Hirshberg: "Simplify Converter Designs with Flyback," *Solid State Power Conversion,* March/April 1975.
6. P. Wood: "Design of a 5 V, 100 Watt Power Supply, TRW AN #122, February 1975.
7. J. Turnbull: "Radio Frequency Interference Suppression in SMPS," Ferroxcube AN-F601.
8. W. Hetterscheid: "Base Circuit Design for High-Voltage Switching Transistors in Power Converters," Mullard Technical Communications (North American Phillips) #473, November 1974.
9. B. George: "6 V 100 A Switched-Mode Power Supply Operating Directly from the Mains," Mullard Technical Communications (North American Phillips) #123, July 1974.
10. B. Bailey: "Circuit Design and Semiconductor Selection for Square-Wave and Sine-Wave Inverters," *Proc. of Powercon 2,* October 1975.
11. B. Bailey: "Safe Reverse Bias Operation—A New Approach," *Proc. of Powercon 3,* June 1976.
12. Gutmann and Suva: "A Line-Operated, Regulated 5 V/50 A Switching Power Supply," Motorola AN-767, September 1976.

**MOTOROLA**

# MC7800 Series

## THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

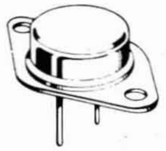
These voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

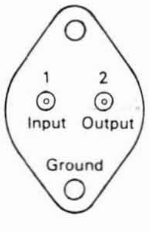
- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in 2% and 4% Tolerance

## THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

**SILICON MONOLITHIC INTEGRATED CIRCUITS**

**K SUFFIX**
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)



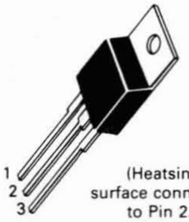


(Bottom View)

Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

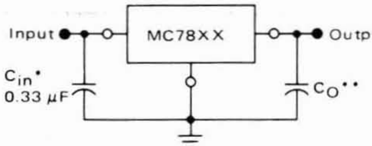
**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220AB

Pin 1. Input
2. Ground
3. Output



(Heatsink surface connected to Pin 2.)

### STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

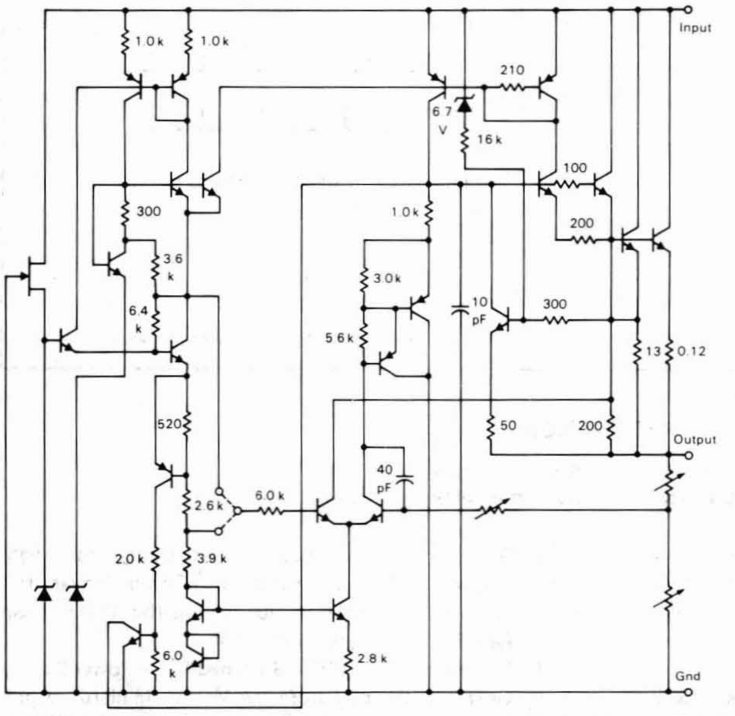
XX = these two digits of the type number indicate voltage.

* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_O$ is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

### EQUIVALENT SCHEMATIC DIAGRAM



## ORDERING INFORMATION

| Device | Output Voltage Tolerance | Temperature Range | Package |
|---|---|---|---|
| MC78XXK | 4% | -55 to +150°C | Metal Power |
| MC78XXAK | 2% | | |
| MC78XXBK | 4% | -40 to +125°C | |
| MC78XXCK | 4% | 0 to +125°C | |
| MC78XXACK | 2% | | |
| MC78XXCT | 4% | | Plastic Power |
| MC78XXACT | 2% | | |
| MC78XXBT | 4% | -40 to +125°C | |

| TYPE NO./VOLTAGE | | | |
|---|---|---|---|
| MC7805 | 5.0 Volts | MC7815 | 15 Volts |
| MC7806 | 6.0 Volts | MC7818 | 18 Volts |
| MC7808 | 8.0 Volts | MC7824 | 24 Volts |
| MC7812 | 12 Volts | | |

**MC7800 Series MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (5.0 V - 18 V) | $V_{in}$ | 35 | Vdc |
| (24 V) | | 40 | |
| Power Dissipation and Thermal Characteristics | | | |
| Plastic Package | | | |
| $T_A$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_A$ = +25°C | $1/\theta_{JA}$ | 15.4 | mW/°C |
| Thermal Resistance, Junction to Air | $\theta_{JA}$ | 65 | °C/W |
| $T_C$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_C$ = +75°C (See Figure 1) | $1/\theta_{JC}$ | 200 | mW/°C |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | 5.0 | °C/W |
| Metal Package | | | |
| $T_A$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_A$ = +25°C | $1/\theta_{JA}$ | 22.5 | mW/°C |
| Thermal Resistance, Junction to Air | $\theta_{JA}$ | 45 | °C/W |
| $T_C$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_C$ = +65°C (See Figure 2) | $1/\theta_{JC}$ | 182 | mW/°C |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | 5.5 | °C/W |
| Storage Junction Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Operating Junction Temperature Range | $T_J$ | | °C |
| MC7800, A | | -55 to +150 | |
| MC7800C, AC | | 0 to +150 | |
| MC7800, B | | -40 to +150 | |

## DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

### MC7805, B, C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 10 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted).

| Characteristic | Symbol | MC7805 | | | MC7805B | | | MC7805C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 4.8 | 5.0 | 5.2 | 4.8 | 5.0 | 5.2 | 4.8 | 5.0 | 5.2 | Vdc |
| Output Voltage | $V_O$ | | | | | | | | | | Vdc |
| (5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_O$ ≤ 15 W) | | | | | | | | | | | |
| 7.0 Vdc ≤ $V_{in}$ ≤ 20 Vdc | | — | — | — | — | — | — | 4.75 | 5.0 | 5.25 | |
| 8.0 Vdc ≤ $V_{in}$ ≤ 20 Vdc | | 4.65 | 5.0 | 5.35 | 4.75 | 5.0 | 5.25 | — | — | — | |
| Line Regulation ($T_J$ = +25°C, Note 2) | $Reg_{line}$ | | | | | | | | | | mV |
| 7.0 Vdc ≤ $V_{in}$ ≤ 25 Vdc | | — | 2.0 | 50 | — | 7.0 | 100 | — | 7.0 | 100 | |
| 8.0 Vdc ≤ $V_{in}$ ≤ 12 Vdc | | — | 1.0 | 25 | — | 2.0 | 50 | — | 2.0 | 50 | |
| Load Regulation ($T_J$ = +25°C, Note 2) | $Reg_{load}$ | | | | | | | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 25 | 100 | — | 40 | 100 | — | 40 | 100 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 8.0 | 25 | — | 15 | 50 | — | 15 | 50 | |
| Quiescent Current ($T_J$ = +25°C) | $I_B$ | — | 3.2 | 6.0 | — | 4.3 | 8.0 | — | 4.3 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | | | | mA |
| 7.0 Vdc ≤ $V_{in}$ ≤ 25 Vdc | | — | — | — | — | — | — | — | — | 1.3 | |
| 8.0 Vdc ≤ $V_{in}$ ≤ 25 Vdc | | — | 0.3 | 0.8 | — | — | 1.3 | — | — | — | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 0.04 | 0.5 | — | — | 0.5 | — | — | 0.5 | |
| Ripple Rejection<br>8.0 Vdc ≤ $V_{in}$ ≤ 18 Vdc, f = 120 Hz | RR | 68 | 75 | — | — | 68 | — | — | 68 | — | dB |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | — | 10 | — | µV/ $V_O$ |
| Output Resistance f = 1.0 kHz | $r_O$ | — | 17 | — | — | 17 | — | — | 17 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C)<br>$V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±0.6 | — | — | -1.1 | — | — | -1.1 | — | mV/ °C |

### MC7805A, AC

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 10 V, $I_O$ = 1.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted)

| Characteristics | Symbol | MC7805A | | | MC7805AC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 4.9 | 5.0 | 5.1 | 4.9 | 5.0 | 5.1 | Vdc |
| Output Voltage<br>(5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_O$ ≤ 15 W)<br>7.5 Vdc ≤ $V_{in}$ ≤ 20 Vdc | $V_O$ | 4.8 | 5.0 | 5.2 | 4.8 | 5.0 | 5.2 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | | | | mV |
| 7.5 Vdc ≤ $V_{in}$ ≤ 25 Vdc, $I_O$ = 500 mA | | — | 2.0 | 10 | — | 7.0 | 50 | |
| 8.0 Vdc ≤ $V_{in}$ ≤ 12 Vdc | | — | 3.0 | 10 | — | 10 | 50 | |
| 8.0 Vdc ≤ $V_{in}$ ≤ 12 Vdc, $T_J$ = +25°C | | — | 1.0 | 4.0 | — | 2.0 | 25 | |
| 7.3 Vdc ≤ $V_{in}$ ≤ 20 Vdc, $T_J$ = +25°C | | — | 2.0 | 10 | — | 7.0 | 50 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A, $T_J$ = +25°C | | — | 2.0 | 25 | — | 25 | 100 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 2.0 | 25 | — | 25 | 100 | |
| 250 mA ≤ $I_O$ ≤ 750mA, $T_J$ = +25°C | | — | 1.0 | 15 | — | — | — | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 1.0 | 25 | — | 8.0 | 50 | |
| Quiescent Current | $I_B$ | — | — | 5.0 | — | — | 6.0 | mA |
| $T_J$ = +25°C | | — | 3.2 | 4.0 | — | 4.3 | 6.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | mA |
| 8.0 Vdc ≤ $V_{in}$ ≤ 25 Vdc, $I_O$ = 500 mA | | — | 0.3 | 0.5 | — | — | 0.8 | |
| 7.5 Vdc ≤ $V_{in}$ ≤ 20 Vdc, $T_J$ = +25°C | | — | 0.2 | 0.5 | — | — | 0.8 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 0.04 | 0.2 | — | — | 0.5 | |
| Ripple Rejection | RR | | | | | | | dB |
| 8.0 Vdc ≤ $V_{in}$ ≤ 18 Vdc, f = 120 Hz, $T_J$ = +25°C | | 68 | 75 | — | — | — | — | |
| 8.0 Vdc ≤ $V_{in}$ ≤ 18 Vdc, f = 120 Hz, $I_O$ = 500 mA | | 68 | 75 | — | — | 68 | — | |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | µV/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | — | 17 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C)<br>$V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±0.6 | — | — | -1.1 | — | mV/°C |

NOTES: 1. $T_{low}$ = -55°C for MC78XX, A
= 0° for MC78XXC, AC
= -40°C for MC78XXB

$T_{high}$ = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. **Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.**

### MC7806, B, C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 11 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted).

| Characteristic | Symbol | MC7806 | | | MC7806B | | | MC7806C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 5.75 | 6.0 | 6.25 | 5.75 | 6.0 | 6.25 | 5.75 | 6.0 | 6.25 | Vdc |
| Output Voltage<br>(5.0 mA ⩽ $I_O$ ⩽ 1.0 A, $P_O$ ⩽ 15 W) | $V_O$ | | | | | | | | | | Vdc |
| 8.0 Vdc ⩽ $V_{in}$ ⩽ 21 Vdc | | — | — | — | — | — | — | 5.7 | 6.0 | 6.3 | |
| 9.0 Vdc ⩽ $V_{in}$ ⩽ 21 Vdc | | 5.65 | 6.0 | 6.35 | 5.7 | 6.0 | 6.3 | — | — | — | |
| Line Regulation ($T_J$ = +25°C, Note 2) | $Reg_{line}$ | | | | | | | | | | mV |
| 8.0 Vdc ⩽ $V_{in}$ ⩽ 25 Vdc | | — | 3.0 | 60 | — | 9.0 | 120 | — | 9.0 | 120 | |
| 9.0 Vdc ⩽ $V_{in}$ ⩽ 13 Vdc | | — | 2.0 | 30 | — | 3.0 | 60 | — | 3.0 | 60 | |
| Load Regulation ($T_J$ = +25°C, Note 2) | $Reg_{load}$ | | | | | | | | | | mV |
| 5.0 mA ⩽ $I_O$ ⩽ 1.5 A | | — | 27 | 100 | — | 43 | 120 | — | 43 | 120 | |
| 250 mA ⩽ $I_O$ ⩽ 750 mA | | — | 9.0 | 30 | — | 16 | 60 | — | 16 | 60 | |
| Quiescent Current ($T_J$ = +25°C) | $I_B$ | — | 3.2 | 6.0 | — | 4.3 | 8.0 | — | 4.3 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | | | | mA |
| 8.0 Vdc ⩽ $V_{in}$ ⩽ 25 Vdc | | — | — | — | — | — | — | — | — | 1.3 | |
| 9.0 Vdc ⩽ $V_{in}$ ⩽ 25 Vdc | | — | 0.3 | 0.8 | — | — | 1.3 | — | — | — | |
| 5.0 mA ⩽ $I_O$ ⩽ 1.0 A | | — | 0.04 | 0.5 | — | — | 0.5 | — | — | 0.5 | |
| Ripple Rejection<br>9.0 Vdc ⩽ $V_{in}$ ⩽ 19 Vdc, f = 120 Hz | RR | 65 | 73 | — | — | 65 | — | — | 65 | — | dB |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ⩽ f ⩽ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | — | 10 | — | μV/ $V_O$ |
| Output Resistance f = 1.0 kHz | $r_O$ | — | 17 | — | — | 17 | — | — | 17 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C)<br>$V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±0.7 | — | — | -0.8 | — | — | -0.8 | — | mV/ °C |

### MC7806A, AC

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 11 V, $I_O$ = 1.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted)

| Characteristics | Symbol | MC7806A | | | MC7806AC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 5.88 | 6.0 | 6.12 | 5.88 | 6.0 | 6.12 | Vdc |
| Output Voltage<br>(5.0 mA ⩽ $I_O$ ⩽ 1.0 A, $P_O$ ⩽ 15 W)<br>8.6 Vdc ⩽ $V_{in}$ ⩽ 21 Vdc | $V_O$ | 5.76 | 6.0 | 6.24 | 5.76 | 6.0 | 6.24 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | | | | mV |
| 8.6 Vdc ⩽ $V_{in}$ ⩽ 25 Vdc, $I_O$ = 500 mA | | — | 3.0 | 11 | — | 9.0 | 60 | |
| 9.0 Vdc ⩽ $V_{in}$ ⩽ 13 Vdc | | — | 5.0 | 15 | — | 11 | 60 | |
| 9.0 Vdc ⩽ $V_{in}$ ⩽ 13 Vdc, $T_J$ = +25°C | | — | 2.0 | 5.0 | — | 3.0 | 30 | |
| 8.3 Vdc ⩽ $V_{in}$ ⩽ 21 Vdc, $T_J$ = +25°C | | — | 4.0 | 11 | — | 9.0 | 60 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | | | | mV |
| 5.0 mA ⩽ $I_O$ ⩽ 1.5 A, $T_J$ = +25°C | | — | 2.0 | 25 | — | 43 | 100 | |
| 5.0 mA ⩽ $I_O$ ⩽ 1.0 A | | — | 2.0 | 25 | — | 43 | 100 | |
| 250 mA ⩽ $I_O$ ⩽ 750mA, $T_J$ = +25°C | | — | 1.0 | 15 | — | — | — | |
| 250 mA ⩽ $I_O$ ⩽ 750 mA | | — | 1.0 | 25 | — | 16 | 50 | |
| Quiescent Current | $I_B$ | — | — | 5.0 | — | — | 6.0 | mA |
| $T_J$ = +25°C | | — | 3.2 | 4.0 | — | 4.3 | 6.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | mA |
| 9.0 Vdc ⩽ $V_{in}$ ⩽ 25 Vdc, $I_O$ = 500 mA | | — | 0.3 | 0.5 | — | — | 0.8 | |
| 8.6 Vdc ⩽ $V_{in}$ ⩽ 21 Vdc, $T_J$ = +25°C | | — | 0.2 | 0.5 | — | — | 0.8 | |
| 5.0 mA ⩽ $I_O$ ⩽ 1.0 A | | — | 0.04 | 0.2 | — | — | 0.5 | |
| Ripple Rejection | RR | | | | | | | dB |
| 9.0 Vdc ⩽ $V_{in}$ ⩽ 19 Vdc, f = 120 Hz, $T_J$ = +25°C | | 65 | 73 | — | — | — | — | |
| 9.0 Vdc ⩽ $V_{in}$ ⩽ 19 Vdc, f = 120 Hz, $I_O$ = 500 mA | | 65 | 73 | — | — | 65 | — | |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ⩽ f ⩽ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | μV/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | — | 17 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C)<br>$V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±0.7 | — | — | -0.8 | — | mV/°C |

NOTES: 1. $T_{low}$ = -55°C for MC78XX, A
= 0° for MC78XXC, AC
= -40°C for MC78XXB

$T_{high}$ = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

### MC7808, B, C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 14 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted).

| Characteristic | Symbol | MC7808 | | | MC7808B | | | MC7808C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 7.7 | 8.0 | 8.3 | 7.7 | 8.0 | 8.3 | 7.7 | 8.0 | 8.3 | Vdc |
| Output Voltage<br>(5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_O$ ≤ 15 W) | $V_O$ | | | | | | | | | | Vdc |
| 10.5 Vdc ≤ $V_{in}$ ≤ 23 Vdc | | — | — | — | — | — | — | 7.6 | 8.0 | 8.4 | |
| 11.5 Vdc ≤ $V_{in}$ ≤ 23 Vdc | | 7.6 | 8.0 | 8.4 | 7.6 | 8.0 | 8.4 | — | — | — | |
| Line Regulation ($T_J$ = +25°C, Note 2) | $Reg_{line}$ | | | | | | | | | | mV |
| 10.5 Vdc ≤ $V_{in}$ ≤ 25 Vdc | | — | 3.0 | 80 | — | 12 | 160 | — | 12 | 160 | |
| 11 Vdc ≤ $V_{in}$ ≤ 17 Vdc | | — | 2.0 | 40 | — | 5.0 | 80 | — | 5.0 | 80 | |
| Load Regulation ($T_J$ = +25°C, Note 2) | $Reg_{load}$ | | | | | | | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 28 | 100 | — | 45 | 160 | — | 45 | 160 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 9.0 | 40 | — | 16 | 80 | — | 16 | 80 | |
| Quiescent Current ($T_J$ = +25°C) | $I_B$ | — | 3.2 | 6.0 | — | 4.3 | 8.0 | — | 4.3 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | | | | mA |
| 10.5 Vdc ≤ $V_{in}$ ≤ 25 Vdc | | — | — | — | — | — | — | — | — | 1.0 | |
| 11.5 Vdc ≤ $V_{in}$ ≤ 25 Vdc | | — | 0.3 | 0.8 | — | — | 1.0 | — | — | — | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 0.04 | 0.5 | — | — | 0.5 | — | — | 0.5 | |
| Ripple Rejection<br>11.5 Vdc ≤ $V_{in}$ ≤ 21.5 Vdc, f = 120 Hz | RR | 62 | 70 | — | — | 62 | — | — | 62 | — | dB |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | — | 10 | — | µV/ $V_O$ |
| Output Resistance f = 1.0 kHz | $r_O$ | — | 18 | — | — | 18 | — | — | 18 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C)<br>$V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±1.0 | — | — | -0.8 | — | — | -0.8 | — | mV/ °C |

### MC7808A, AC

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 14 V, $I_O$ = 1.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted)

| Characteristics | Symbol | MC7808A | | | MC7808AC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 7.84 | 8.0 | 8.16 | 7.84 | 8.0 | 8.16 | Vdc |
| Output Voltage<br>(5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_O$ ≤ 15 W)<br>10.6 Vdc ≤ $V_{in}$ ≤ 23 Vdc | $V_O$ | 7.7 | 8.0 | 8.3 | 7.7 | 8.0 | 8.3 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | | | | mV |
| 10.6 Vdc ≤ $V_{in}$ ≤ 25 Vdc, $I_O$ = 500 mA | | — | 4.0 | 13 | — | 12 | 80 | |
| 11 Vdc ≤ $V_{in}$ ≤ 17 Vdc | | — | 6.0 | 20 | — | 15 | 80 | |
| 11 Vdc ≤ $V_{in}$ ≤ 17 Vdc, $T_J$ = +25°C | | — | 2.0 | 6.0 | — | 5.0 | 40 | |
| 10.4 Vdc ≤ $V_{in}$ ≤ 23 Vdc, $T_J$ = +25°C | | — | 4.0 | 13 | — | 12 | 80 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A, $T_J$ = +25°C | | — | 2.0 | 25 | — | 45 | 100 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 2.0 | 25 | — | 45 | 100 | |
| 250 mA ≤ $I_O$ ≤ 750mA, $T_J$ = +25°C | | — | 1.0 | 15 | — | — | — | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 1.0 | 25 | — | 16 | 50 | |
| Quiescent Current | $I_B$ | — | — | 5.0 | — | — | 6.0 | mA |
| $T_J$ = +25°C | | — | 3.2 | 4.0 | — | 4.3 | 6.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | mA |
| 11 Vdc ≤ $V_{in}$ ≤ 25 Vdc, $I_O$ = 500 mA | | — | 0.3 | 0.5 | — | — | 0.8 | |
| 10.6 Vdc ≤ $V_{in}$ ≤ 23 Vdc, $T_J$ = +25°C | | — | 0.2 | 0.5 | — | — | 0.8 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 0.04 | 0.2 | — | — | 0.5 | |
| Ripple Rejection | RR | | | | | | | dB |
| 11.5 Vdc ≤ $V_{in}$ ≤ 21.5 Vdc, f = 120 Hz, $T_J$ = +25°C | | 62 | 70 | — | — | — | — | |
| 11.5 Vdc ≤ $V_{in}$ ≤ 21.5 Vdc, f = 120 Hz, $I_O$ = 500 mA | | 62 | 70 | — | — | 62 | — | |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | µV/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | — | 18 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C)<br>$V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±1.0 | — | — | -0.8 | — | mV/°C |

NOTES: 1. $T_{low}$ = −55°C for MC78XX, A
= 0° for MC78XXC, AC
= −40°C for MC78XXB

$T_{high}$ = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**MC7812, B, C**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 19 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted).

| Characteristic | Symbol | MC7812 | | | MC7812B | | | MC7812C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 11.5 | 12 | 12.5 | 11.5 | 12 | 12.5 | 11.5 | 12 | 12.5 | Vdc |
| Output Voltage<br>(5.0 mA $\leq I_O \leq$ 1.0 A, $P_O \leq$ 15 W) | $V_O$ | | | | | | | | | | Vdc |
| 14.5 Vdc $\leq V_{in} \leq$ 27 Vdc | | — | — | — | — | — | — | 11.4 | 12 | 12.6 | |
| 15.5 Vdc $\leq V_{in} \leq$ 27 Vdc | | 11.4 | 12 | 12.6 | 11.4 | 12 | 12.6 | — | — | — | |
| Line Regulation ($T_J$ = +25°C, Note 2) | $Reg_{line}$ | | | | | | | | | | mV |
| 14.5 Vdc $\leq V_{in} \leq$ 30 Vdc | | — | 5.0 | 120 | — | 13 | 240 | — | 13 | 240 | |
| 16 Vdc $\leq V_{in} \leq$ 22 Vdc | | — | 3.0 | 60 | — | 6.0 | 120 | — | 6.0 | 120 | |
| Load Regulation ($T_J$ = +25°C, Note 2) | $Reg_{load}$ | | | | | | | | | | mV |
| 5.0 mA $\leq I_O \leq$ 1.5 A | | — | 30 | 120 | — | 46 | 240 | — | 46 | 240 | |
| 250 mA $\leq I_O \leq$ 750 mA | | — | 10 | 60 | — | 17 | 120 | — | 17 | 120 | |
| Quiescent Current ($T_J$ = +25°C) | $I_B$ | — | 3.4 | 6.0 | — | 4.4 | 8.0 | — | 4.4 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | | | | mA |
| 14.5 Vdc $\leq V_{in} \leq$ 30 Vdc | | — | — | — | — | — | — | — | — | 1.0 | |
| 15 Vdc $\leq V_{in} \leq$ 30 Vdc | | — | 0.3 | 0.8 | — | — | 1.0 | — | — | — | |
| 5.0 mA $\leq I_O \leq$ 1.0 A | | — | 0.04 | 0.5 | — | — | 0.5 | — | — | 0.5 | |
| Ripple Rejection<br>15 Vdc $\leq V_{in} \leq$ 25 Vdc, f = 120 Hz | RR | 61 | 68 | — | — | 60 | — | — | 60 | — | dB |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz $\leq$ f $\leq$ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | — | 10 | — | µV/ $V_O$ |
| Output Resistance f = 1.0 kHz | $r_O$ | — | 18 | — | — | 18 | — | — | 18 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C)<br>$V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±1.5 | — | — | -1.0 | — | — | -1.0 | — | mV/ °C |

**MC7812A, AC**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 19 V, $I_O$ = 1.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted)

| Characteristics | Symbol | MC7812A | | | MC7812AC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 11.75 | 12 | 12.25 | 11.75 | 12 | 12.25 | Vdc |
| Output Voltage<br>(5.0 mA $\leq I_O \leq$ 1.0 A, $P_O \leq$ 15 W)<br>14.8 Vdc $\leq V_{in} \leq$ 27 Vdc | $V_O$ | 11.5 | 12 | 12.5 | 11.5 | 12 | 12.5 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | | | | mV |
| 14.8 Vdc $\leq V_{in} \leq$ 30 Vdc, $I_O$ = 500 mA | | — | 5.0 | 18 | — | 13 | 120 | |
| 16 Vdc $\leq V_{in} \leq$ 22 Vdc | | — | 8.0 | 30 | — | 16 | 120 | |
| 16 Vdc $\leq V_{in} \leq$ 22 Vdc, $T_J$ = +25°C | | — | 3.0 | 9.0 | — | 6.0 | 60 | |
| 14.5 Vdc $\leq V_{in} \leq$ 27 Vdc, $T_J$ = +25°C | | — | 5.0 | 18 | — | 13 | 120 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | | | | mV |
| 5.0 mA $\leq I_O \leq$ 1.5 A, $T_J$ = +25°C | | — | 2.0 | 25 | — | 46 | 100 | |
| 5.0 mA $\leq I_O \leq$ 1.0 A | | — | 2.0 | 25 | — | 46 | 100 | |
| 250 mA $\leq I_O \leq$ 750mA, $T_J$ = +25°C | | — | 1.0 | 15 | — | — | — | |
| 250 mA $\leq I_O \leq$ 750 mA | | — | 1.0 | 25 | — | 17 | 50 | |
| Quiescent Current | $I_B$ | — | — | 5.0 | — | — | 6.0 | mA |
| $T_J$ = +25°C | | — | 3.4 | 4.0 | — | 4.4 | 6.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | mA |
| 15 Vdc $\leq V_{in} \leq$ 30 Vdc, $I_O$ = 500 mA | | — | 0.3 | 0.5 | — | — | 0.8 | |
| 14.8 Vdc $\leq V_{in} \leq$ 27 Vdc, $T_J$ = +25°C | | — | 0.2 | 0.5 | — | — | 0.8 | |
| 5.0 mA $\leq I_O \leq$ 1.0 A | | — | 0.04 | 0.2 | — | — | 0.5 | |
| Ripple Rejection | RR | | | | | | | dB |
| 15 Vdc $\leq V_{in} \leq$ 25 Vdc, f = 120 Hz, $T_J$ = +25°C | | 61 | 68 | — | — | — | — | |
| 15 Vdc $\leq V_{in} \leq$ 25 Vdc, f = 120 Hz, $I_O$ = 500 mA | | 61 | 68 | — | — | 60 | — | |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz $\leq$ f $\leq$ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | µV/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | — | 18 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C)<br>$V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±1.5 | — | — | -1.0 | — | mV/°C |

NOTES: 1. $T_{low}$ = −55°C for MC78XX, A; = 0° for MC78XXC, AC; = −40°C for MC78XXB. $T_{high}$ = +150°C for MC78XX, A; = +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**MC7815, B, C**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 23 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted).

| Characteristic | Symbol | MC7815 | | | MC7815B | | | MC7815C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 14.4 | 15 | 15.6 | 14.4 | 15 | 15.6 | 14.4 | 15 | 15.6 | Vdc |
| Output Voltage | $V_O$ | | | | | | | | | | Vdc |
| (5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_O$ ≤ 15 W) | | | | | | | | | | | |
| 17.5 Vdc ≤ $V_{in}$ ≤ 30 Vdc | | — | — | — | — | — | — | 14.25 | 15 | 15.75 | |
| 18.5 Vdc ≤ $V_{in}$ ≤ 30 Vdc | | 14.25 | 15 | 15.75 | 14.25 | 15 | 15.75 | — | — | — | |
| Line Regulation ($T_J$ = +25°C, Note 2) | $Reg_{line}$ | | | | | | | | | | mV |
| 17.5 Vdc ≤ $V_{in}$ ≤ 30 Vdc | | — | 6.0 | 150 | — | 13 | 300 | — | 13 | 300 | |
| 20 Vdc ≤ $V_{in}$ ≤ 26 Vdc | | — | 3.0 | 75 | — | 6.0 | 150 | — | 6.0 | 150 | |
| Load Regulation ($T_J$ = +25°C, Note 2) | $Reg_{load}$ | | | | | | | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 32 | 150 | — | 52 | 300 | — | 52 | 300 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 10 | 75 | — | 20 | 150 | — | 20 | 150 | |
| Quiescent Current ($T_J$ = +25°C) | $I_B$ | — | 3.4 | 6.0 | — | 4.4 | 8.0 | — | 4.4 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | | | | mA |
| 17.5 Vdc ≤ $V_{in}$ ≤ 30 Vdc | | — | — | — | — | — | — | — | — | 1.0 | |
| 18.5 Vdc ≤ $V_{in}$ ≤ 30 Vdc | | — | 0.3 | 0.8 | — | — | 1.0 | — | — | — | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 0.04 | 0.5 | — | — | 0.5 | — | — | 0.5 | |
| Ripple Rejection<br>18.5 Vdc ≤ $V_{in}$ ≤ 28.5 Vdc, f = 120 Hz | RR | 60 | 66 | — | — | 58 | — | — | 58 | — | dB |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | — | 10 | — | µV/ $V_O$ |
| Output Resistance f = 1.0 kHz | $r_O$ | — | 19 | — | — | 19 | — | — | 19 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C)<br>$V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±1.8 | — | — | -1.0 | — | — | -1.0 | — | mV/ °C |

**MC7815A, AC**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 23 V, $I_O$ = 1.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted)

| Characteristics | Symbol | MC7815A | | | MG7815AC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 14.7 | 15 | 15.3 | 14.7 | 15 | 15.3 | Vdc |
| Output Voltage<br>(5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_O$ ≤ 15 W)<br>17.9 Vdc ≤ $V_{in}$ ≤ 30 Vdc | $V_O$ | 14.4 | 15 | 15.6 | 14.4 | 15 | 15.6 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | | | | mV |
| 17.9 Vdc ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 500 mA | | — | 6.0 | 22 | — | 13 | 150 | |
| 20 Vdc ≤ $V_{in}$ ≤ 26 Vdc | | — | 6.0 | 22 | — | 16 | 150 | |
| 20 Vdc ≤ $V_{in}$ ≤ 26 Vdc, $T_J$ = +25°C | | — | 3.0 | 10 | — | 6.0 | 75 | |
| 17.5 Vdc ≤ $V_{in}$ ≤ 30 Vdc, $T_J$ = +25°C | | — | 6.0 | 22 | — | 13 | 150 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A, $T_J$ = +25°C | | — | 2.0 | 25 | — | 52 | 100 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 2.0 | 25 | — | 52 | 100 | |
| 250 mA ≤ $I_O$ ≤ 750mA, $T_J$ = +25°C | | — | 1.0 | 15 | — | — | — | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 1.0 | 25 | — | 20 | 50 | |
| Quiescent Current | $I_B$ | — | — | 5.5 | — | — | 6.0 | mA |
| $T_J$ = +25°C | | — | 3.4 | 4.5 | — | 4.4 | 6.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | mA |
| 17.5 Vdc ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 500 mA | | — | 0.3 | 0.5 | — | — | 0.8 | |
| 17.5 Vdc ≤ $V_{in}$ ≤ 30 Vdc, $T_J$ = +25°C | | — | 0.2 | 0.5 | — | — | 0.8 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 0.04 | 0.2 | — | — | 0.5 | |
| Ripple Rejection | RR | | | | | | | dB |
| 18.5 Vdc ≤ $V_{in}$ ≤ 28.5 Vdc, f = 120 Hz, $T_J$ = +25°C | | 60 | 66 | — | — | — | — | |
| 18.5 Vdc ≤ $V_{in}$ ≤ 28.5 Vdc, f = 120 Hz, $I_O$ = 500 mA | | 60 | 66 | — | — | 58 | — | |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | µV/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | — | 19 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C)<br>$V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±1.8 | — | — | -1.0 | — | mV/°C |

NOTES: 1. $T_{low}$ = −55°C for MC78XX, A
= 0° for MC78XXC, AC
= −40°C for MC78XXB

$T_{high}$ = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**MC7818, B, C**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 27 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted).

| Characteristic | Symbol | MC7818 | | | MC7818B | | | MC7818C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 17.3 | 18 | 18.7 | 17.3 | 18 | 18.7 | 17.3 | 18 | 18.7 | Vdc |
| Output Voltage (5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_O$ ≤ 15 W) | $V_O$ | | | | | | | | | | Vdc |
| 21 Vdc ≤ $V_{in}$ ≤ 33 Vdc | | — | — | — | — | — | — | 17.1 | 18 | 18.9 | |
| 22 Vdc ≤ $V_{in}$ ≤ 33 Vdc | | 17.1 | 18 | 18.9 | 17.1 | 18 | 18.9 | — | — | — | |
| Line Regulation ($T_J$ = +25°C, Note 2) | $Reg_{line}$ | | | | | | | | | | mV |
| 21 Vdc ≤ $V_{in}$ ≤ 33 Vdc | | — | 7.0 | 180 | — | 25 | 360 | — | 25 | 360 | |
| 24 Vdc ≤ $V_{in}$ ≤ 30 Vdc | | — | 4.0 | 90 | — | 10 | 180 | — | 10 | 180 | |
| Load Regulation ($T_J$ = +25°C, Note 2) | $Reg_{load}$ | | | | | | | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 35 | 180 | — | 55 | 360 | — | 55 | 360 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 12 | 90 | — | 22 | 180 | — | 22 | 180 | |
| Quiescent Current ($T_J$ = +25°C) | $I_B$ | — | 3.5 | 6.0 | — | 4.5 | 8.0 | — | 4.5 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | | | | mA |
| 21 Vdc ≤ $V_{in}$ ≤ 33 Vdc | | — | — | — | — | — | — | — | — | 1.0 | |
| 22 Vdc ≤ $V_{in}$ ≤ 33 Vdc | | — | 0.3 | 0.8 | — | — | 1.0 | — | — | — | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 0.04 | 0.5 | — | — | 0.5 | — | — | 0.5 | |
| Ripple Rejection 22 Vdc ≤ $V_{in}$ ≤ 32 Vdc, f = 120 Hz | RR | 59 | 65 | — | — | 57 | — | — | 57 | — | dB |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C) 10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | — | 10 | — | µV/ $V_O$ |
| Output Resistance f = 1.0 kHz | $r_O$ | — | 19 | — | — | 19 | — | — | 19 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C) $V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±2.3 | — | — | -1.0 | — | — | -1.0 | — | mV/ °C |

**MC7818A, AC**

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 27 V, $I_O$ = 1.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted)

| Characteristics | Symbol | MC7818A | | | MC7818AC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 17.64 | 18 | 18.36 | 17.64 | 18 | 18.36 | Vdc |
| Output Voltage (5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_O$ ≤ 15 W) 21 Vdc ≤ $V_{in}$ ≤ 33 Vdc | $V_O$ | 17.3 | 18 | 18.7 | 17.3 | 18 | 17.3 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | | | | mV |
| 21 Vdc ≤ $V_{in}$ ≤ 33 Vdc, $I_O$ = 500 mA | | — | 7.0 | 31 | — | 25 | 180 | |
| 24 Vdc ≤ $V_{in}$ ≤ 30 Vdc | | — | 12 | 45 | — | 28 | 180 | |
| 24 Vdc ≤ $V_{in}$ ≤ 30 Vdc, $T_J$ = +25°C | | — | 4.0 | 15 | — | 10 | 90 | |
| 20.6 Vdc ≤ $V_{in}$ ≤ 33 Vdc, $T_J$ = +25°C | | — | 7.0 | 31 | — | 25 | 180 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A, $T_J$ = +25°C | | — | 2.0 | 25 | — | 55 | 100 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 2.0 | 25 | — | 55 | 100 | |
| 250 mA ≤ $I_O$ ≤ 750mA, $T_J$ = +25°C | | — | 1.0 | 15 | — | — | — | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 1.0 | 25 | — | 22 | 50 | |
| Quiescent Current | $I_B$ | — | — | 5.5 | — | — | 6.0 | mA |
| $T_J$ = +25°C | | — | 3.4 | 4.5 | — | 4.5 | 6.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | mA |
| 21 Vdc ≤ $V_{in}$ ≤ 33 Vdc, $I_O$ = 500 mA | | — | 0.3 | 0.5 | — | — | 0.8 | |
| 21 Vdc ≤ $V_{in}$ ≤ 33 Vdc, $T_J$ = +25°C | | — | 0.2 | 0.5 | — | — | 0.8 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 0.04 | 0.2 | — | — | 0.5 | |
| Ripple Rejection | RR | | | | | | | dB |
| 22 Vdc ≤ $V_{in}$ ≤ 32 Vdc, f = 120 Hz, $T_J$ = +25°C | | 59 | 65 | — | — | — | — | |
| 22 Vdc ≤ $V_{in}$ ≤ 32 Vdc, f = 120 Hz, $I_O$ = 500 mA | | 59 | 65 | — | — | 57 | — | |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C) 10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | µV/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | — | 19 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C) $V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±2.3 | — | — | -1.0 | — | mV/°C |

NOTES: 1. $T_{low}$ = -55°C for MC78XX, A
= 0° for MC78XXC, AC
= -40°C for MC78XXB

$T_{high}$ = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

### MC7824, B, C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 33 V, $I_O$ = 500 mA, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted).

| Characteristic | Symbol | MC7824 | | | MC7824B | | | MC7824C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 23 | 24 | 25 | 23 | 24 | 25 | 23 | 24 | 25 | Vdc |
| Output Voltage (5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_O$ ≤ 15 W) | $V_O$ | | | | | | | | | | Vdc |
| 27 Vdc ≤ $V_{in}$ ≤ 38 Vdc | | — | — | — | — | — | — | 22.8 | 24 | 25.2 | |
| 28 Vdc ≤ $V_{in}$ ≤ 38 Vdc | | 22.8 | 24 | 25.2 | 22.8 | 24 | 25.2 | — | — | — | |
| Line Regulation ($T_J$ = +25°C, Note 2) | $Reg_{line}$ | | | | | | | | | | mV |
| 27 Vdc ≤ $V_{in}$ ≤ 38 Vdc | | — | 10 | 240 | — | 31 | 480 | — | 31 | 480 | |
| 30 Vdc ≤ $V_{in}$ ≤ 36 Vdc | | — | 5.0 | 120 | — | 14 | 240 | — | 14 | 240 | |
| Load Regulation ($T_J$ = +25°C, Note 2) | $Reg_{load}$ | | | | | | | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 40 | 240 | — | 60 | 480 | — | 60 | 480 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 15 | 120 | — | 25 | 240 | — | 25 | 240 | |
| Quiescent Current ($T_J$ = +25°C) | $I_B$ | — | 3.6 | 6.0 | — | 4.6 | 8.0 | — | 4.6 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | | | | mA |
| 27 Vdc ≤ $V_{in}$ ≤ 38 Vdc | | — | — | — | — | — | — | — | — | 1.0 | |
| 28 Vdc ≤ $V_{in}$ ≤ 38 Vdc | | — | 0.3 | 0.8 | — | — | 1.0 | — | — | — | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 0.04 | 0.5 | — | — | 0.5 | — | — | 0.5 | |
| Ripple Rejection 28 Vdc ≤ $V_{in}$ ≤ 38 Vdc, f = 120 Hz | RR | 56 | 62 | — | — | 54 | — | — | 54 | — | dB |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C) 10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | — | 10 | — | µV/ $V_O$ |
| Output Resistance f = 1.0 kHz | $r_O$ | — | 20 | — | — | 20 | — | — | 20 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C) $V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±3.0 | — | — | -1.5 | — | — | -1.5 | — | mV/ °C |

### MC7824A, AC

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 33 V, $I_O$ = 1.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1] unless otherwise noted)

| Characteristics | Symbol | MC7824A | | | MC7824AC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 23.5 | 24 | 24.5 | 23.5 | 24 | 24.5 | Vdc |
| Output Voltage (5.0 mA ≤ $I_O$ ≤ 1.0 A, $P_O$ ≤ 15 W) 27.3 Vdc ≤ $V_{in}$ ≤ 38 Vdc | $V_O$ | 23 | 24 | 25 | 23 | 24 | 25 | Vdc |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | | | | mV |
| 27 Vdc ≤ $V_{in}$ ≤ 38 Vdc, $I_O$ = 500 mA | | — | 10 | 36 | — | 31 | 240 | |
| 30 Vdc ≤ $V_{in}$ ≤ 36 Vdc | | — | 15 | 60 | — | 35 | 240 | |
| 30 Vdc ≤ $V_{in}$ ≤ 36 Vdc, $T_J$ = +25°C | | — | 5.0 | 19 | — | 14 | 120 | |
| 26.7 Vdc ≤ $V_{in}$ ≤ 38 Vdc, $T_J$ = +25°C | | — | 10 | 36 | — | 31 | 240 | |
| Load Regulation (Note 2) | $Reg_{load}$ | | | | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A, $T_J$ = +25°C | | — | 2.0 | 25 | — | 60 | 100 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 2.0 | 25 | — | 60 | 100 | |
| 250 mA ≤ $I_O$ ≤ 750mA, $T_J$ = +25°C | | — | 1.0 | 15 | — | — | — | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 1.0 | 25 | — | 25 | 50 | |
| Quiescent Current | $I_B$ | — | — | 6.0 | — | — | 6.0 | mA |
| $T_J$ = +25°C | | — | 3.6 | 5.0 | — | 4.6 | 6.0 | |
| Quiescent Current Change | $\Delta I_B$ | | | | | | | mA |
| 27.3 Vdc ≤ $V_{in}$ ≤ 38 Vdc, $I_O$ = 500 mA | | — | 0.3 | 0.5 | — | — | 0.8 | |
| 27.3 Vdc ≤ $V_{in}$ ≤ 38 Vdc, $T_J$ = +25°C | | — | 0.2 | 0.5 | — | — | 0.8 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 0.04 | 0.2 | — | — | 0.5 | |
| Ripple Rejection | RR | | | | | | | dB |
| 28 Vdc ≤ $V_{in}$ ≤ 38 Vdc, f = 120 Hz, $T_J$ = +25°C | | 56 | 62 | — | — | — | — | |
| 28 Vdc ≤ $V_{in}$ ≤ 38 Vdc, f = 120 Hz, $I_O$ = 500 mA | | 56 | 62 | — | — | 54 | — | |
| Dropout Voltage ($I_O$ = 1.0 A, $T_J$ = +25°C) | $V_{in} - V_O$ | — | 2.0 | 2.5 | — | 2.0 | — | Vdc |
| Output Noise Voltage ($T_A$ = +25°C) 10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 10 | 40 | — | 10 | — | µV/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 2.0 | — | — | 20 | — | mΩ |
| Short-Circuit Current Limit ($T_A$ = +25°C) $V_{in}$ = 35 Vdc | $I_{sc}$ | — | 0.2 | 1.2 | — | 0.2 | — | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | 1.3 | 2.5 | 3.3 | — | 2.2 | — | A |
| Average Temperature Coefficient of Output Voltage | $TCV_O$ | — | ±3.0 | — | — | -1.5 | — | mV/°C |

NOTES: 1. $T_{low}$ = −55°C for MC78XX, A
= 0° for MC78XXC, AC
= −40°C for MC78XXB

$T_{high}$ = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## TYPICAL CHARACTERISTICS

($T_A$ = +25°C unless otherwise noted.)

FIGURE 1 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 221A)

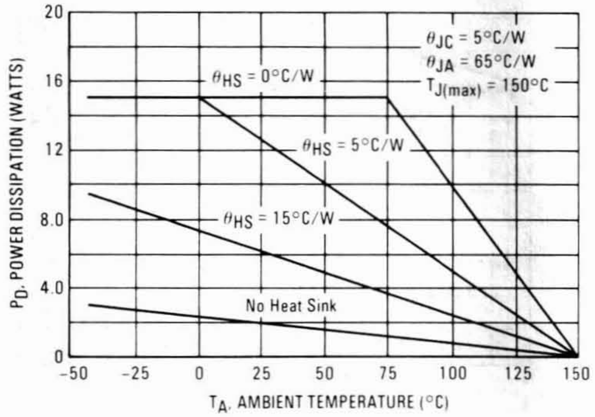


FIGURE 2 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 1)

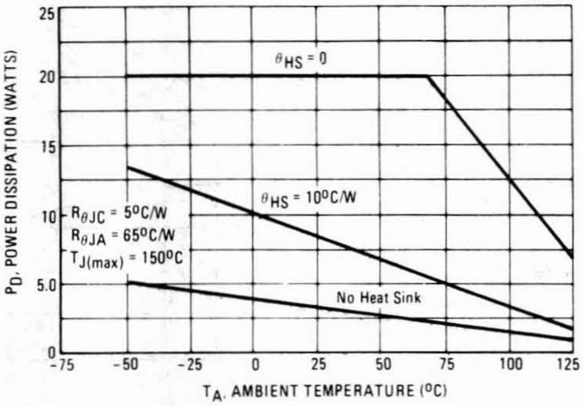


FIGURE 3 — INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC, B)

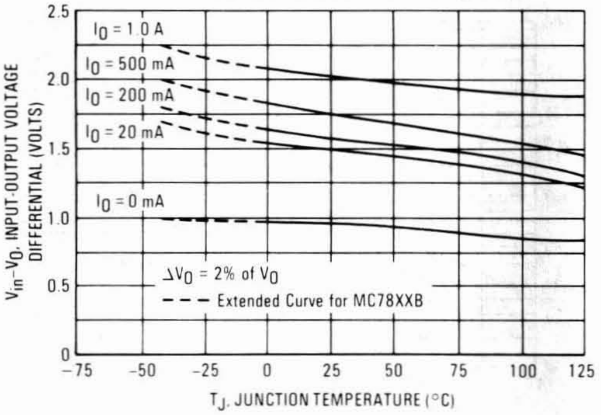


FIGURE 4 – INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XX, A)

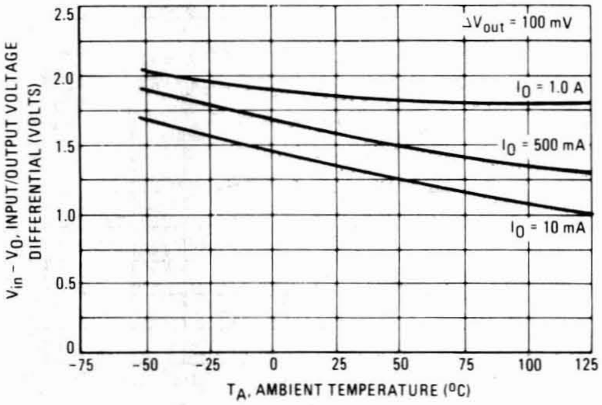


FIGURE 5 — PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE (MC78XXC, AC, B)

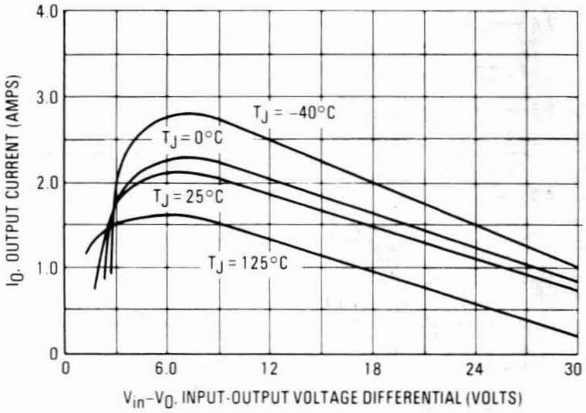
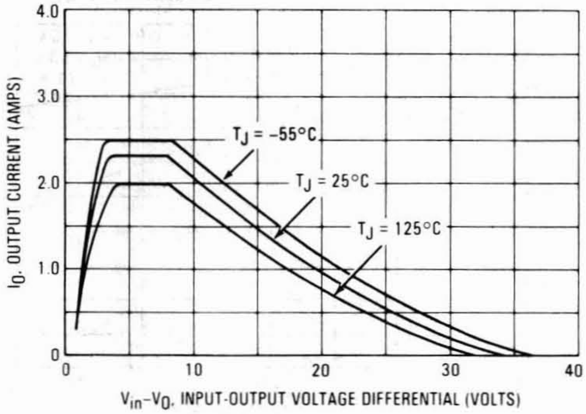


FIGURE 6 — PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE (MC78XX, A)



## TYPICAL CHARACTERISTICS (continued)

## ($T_A$ = 25°C unless otherwise noted.)

FIGURE 7 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES (MC78XXC, AC)

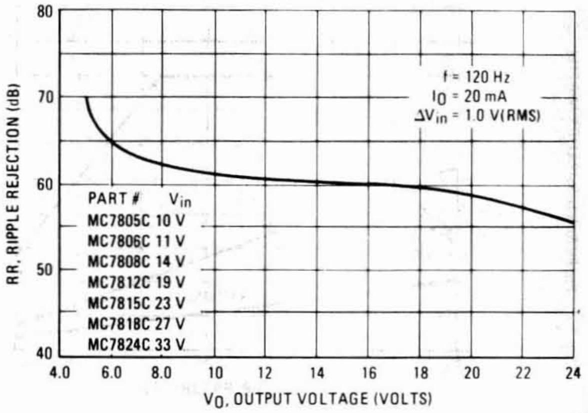


FIGURE 8 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY (MC78XXC, AC, A)

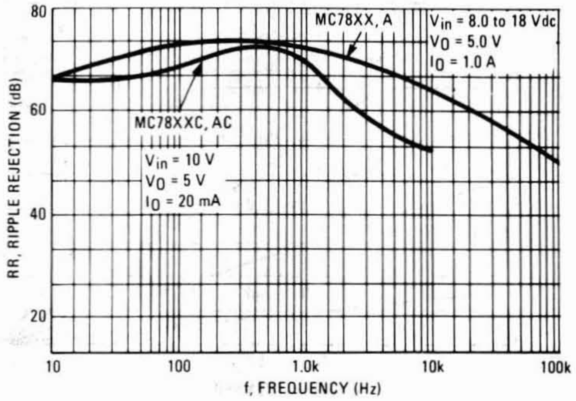


FIGURE 9 — OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC, B)

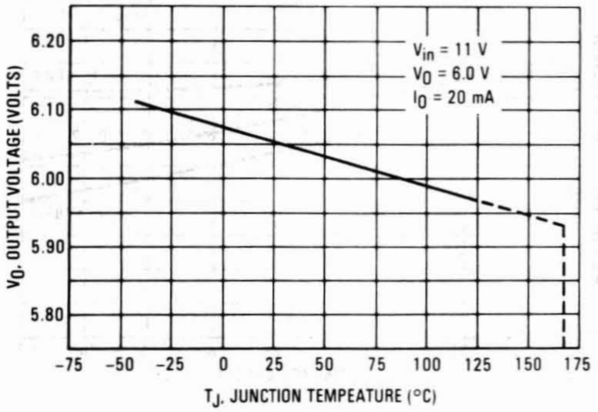


FIGURE 10 – OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE (MC78XXC, AC)

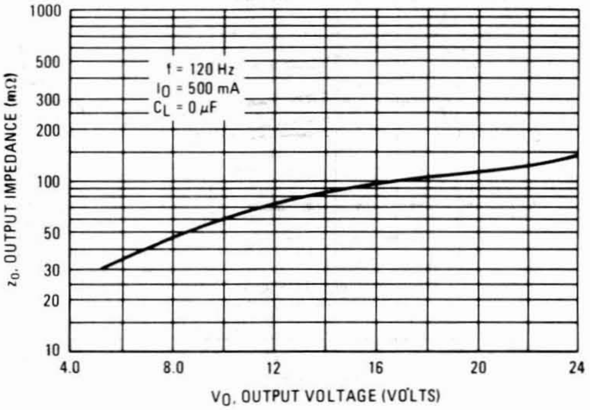


FIGURE 11 — QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE (MC78XXC, AC, B)

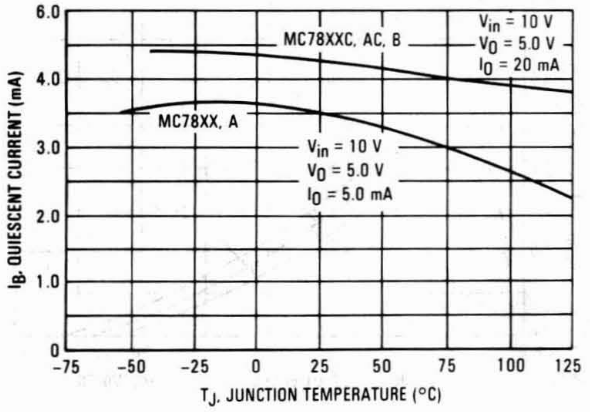
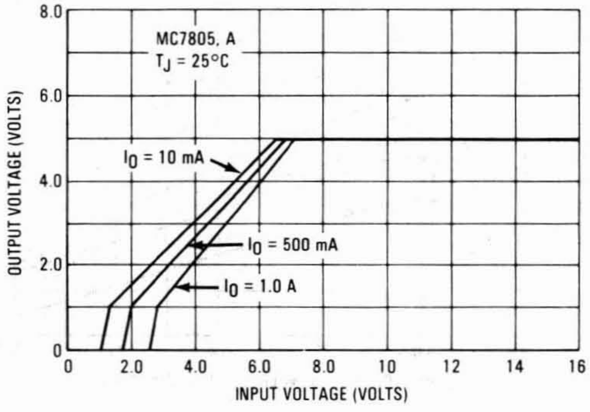


FIGURE 12 — DROPOUT CHARACTERISTICS (MC78XX, A)



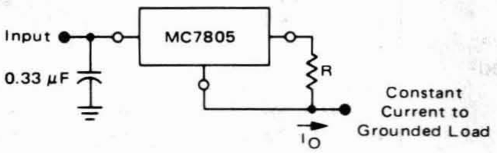
## APPLICATIONS INFORMATION

**Design Considerations**

The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 13 – CURRENT REGULATOR



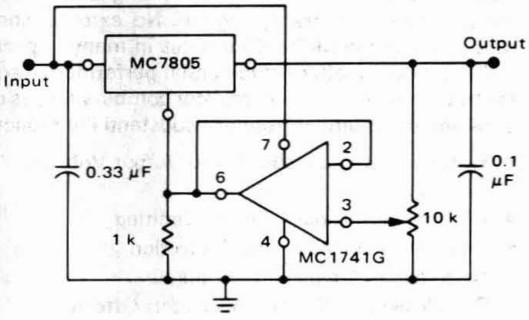
The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

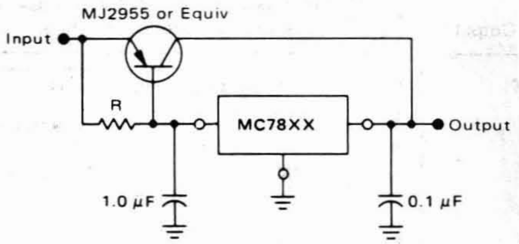
FIGURE 14 – ADJUSTABLE OUTPUT REGULATOR



$V_O$, 7.0 V to 20 V
$V_{IN} - V_O \geqslant 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

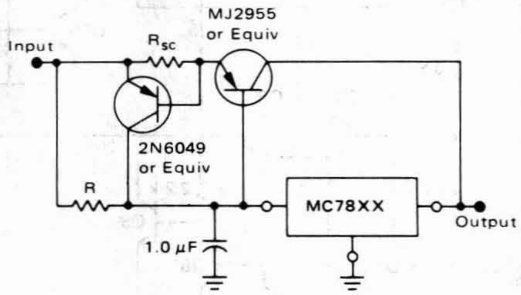
FIGURE 15 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the $V_{BE}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by $V_{BE}$ of the pass transistor.

FIGURE 16 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 15 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, $R_{SC}$, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

MOTOROLA

# MC78L00C,AC Series

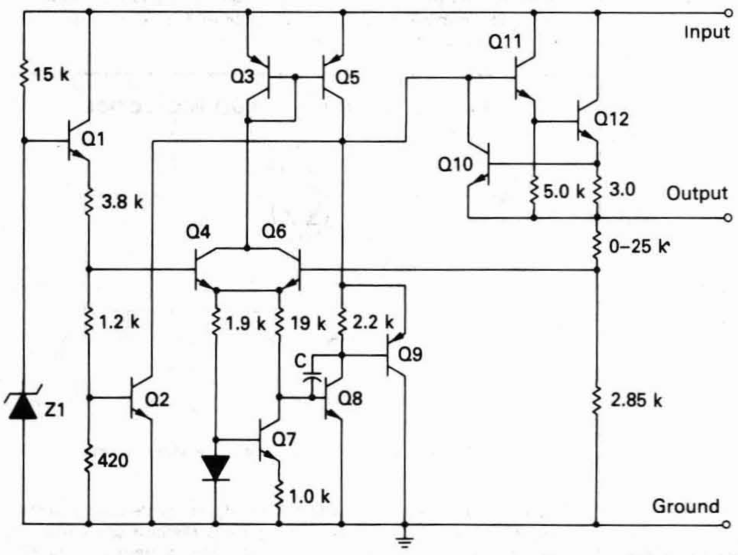
## THREE-TERMINAL LOW CURRENT POSITIVE VOLTAGE REGULATORS

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode-resistor combination, as output impedance and quiescent current are substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

### REPRESENTATIVE CIRCUIT SCHEMATIC



### ORDERING INFORMATION

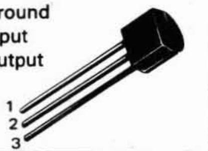
| Device | Junction Temperature Range | Package |
|---|---|---|
| MC78LXXACD | $T_J$ = 0°C to +125°C | SO-8 |
| MC78LXXACG | | Metal Can |
| MC78LXXACP | | Plastic Transistor |
| MC78LXXCD | | SO-8 |
| MC78LXXCG | | Metal Can |
| MC78LXXCP | | Plastic Transistor |

XX indicates nominal voltage

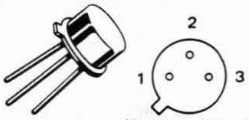
## THREE-TERMINAL LOW CURRENT POSITIVE FIXED VOLTAGE REGULATORS

**P SUFFIX**
CASE 29-02
TO-226AA
(TO-92)

Pin 1. Ground
2. Input
3. Output

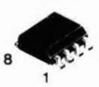


**G SUFFIX**
CASE 79-03
(TO-39)



Pin 1. Ground
2. Output
3. Input

(Bottom View)
(Case Connected To Pin 3)

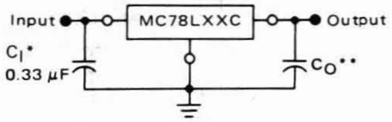


**D SUFFIX***
PLASTIC PACKAGE
CASE 751-01
SOP-8

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

***Surface Mount pin-out is different than standard package pin-out for this device. Please refer to Chapter 7 for details.**

### STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = $C_I$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_O$ is not needed for stability; however, it does improve transient response.

| Device No. ±10% | Device No. ±5% | Nominal Voltage |
|---|---|---|
| MC78L05C | MC78L05AC | 5.0 |
| MC78L08C | MC78L08AC | 8.0 |
| MC78L12C | MC78L12AC | 12 |
| MC78L15C | MC78L15AC | 15 |
| MC78L18C | MC78L18AC | 18 |
| MC78L24C | MC78L24AC | 24 |

**MC78L00 Series MAXIMUM RATINGS** ($T_A$ = +125°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (2.6 V–8.0 V)<br>(12 V–18 V)<br>(24 V) | $V_I$ | 30<br>35<br>40 | Vdc |
| Storage Junction Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Operating Junction Temperature Range | $T_J$ | 0 to +150 | °C |

**MC78L05C, MC78L05AC ELECTRICAL CHARACTERISTICS** ($V_I$ = 10 V, $I_O$ = 40 mA, $C_I$ = 0.33 μF, $C_O$ = 0.1 μF, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | MC78L05AC Min | MC78L05AC Typ | MC78L05AC Max | MC78L05C Min | MC78L05C Typ | MC78L05C Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 4.8 | 5.0 | 5.2 | 4.6 | 5.0 | 5.4 | Vdc |
| Line Regulation<br>($T_J$ = +25°C, $I_O$ = 40 mA)<br>7.0 Vdc ≤ $V_I$ ≤ 20 Vdc<br>8.0 Vdc ≤ $V_I$ ≤ 20 Vdc | $Reg_{line}$ | —<br>— | 55<br>45 | 150<br>100 | —<br>— | 55<br>45 | 200<br>150 | mV |
| Load Regulation<br>($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 100 mA)<br>($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 40 mA) | $Reg_{load}$ | —<br>— | 11<br>5.0 | 60<br>30 | —<br>— | 11<br>5.0 | 60<br>30 | mV |
| Output Voltage<br>(7.0 Vdc ≤ $V_I$ ≤ 20 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA)<br>($V_I$ = 10 V, 1.0 mA ≤ $I_O$ ≤ 70 mA) | $V_O$ | 4.75<br>4.75 | —<br>— | 5.25<br>5.25 | 4.5<br>4.5 | —<br>— | 5.5<br>5.5 | Vdc |
| Input Bias Current<br>($T_J$ = +25°C)<br>($T_J$ = +125°C) | $I_{IB}$ | —<br>— | 3.8<br>— | 6.0<br>5.5 | —<br>— | 3.8<br>— | 6.0<br>5.5 | mA |
| Input Bias Current Change<br>(8.0 Vdc ≤ $V_I$ ≤ 20 Vdc)<br>(1.0 mA ≤ $I_O$ ≤ 40 mA) | $\Delta I_{IB}$ | —<br>— | —<br>— | 1.5<br>0.1 | —<br>— | —<br>— | 1.5<br>0.2 | mA |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 40 | — | — | 40 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 12 | — | — | 12 | — | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 40 mA, f = 120 Hz, 8.0 V ≤ $V_I$ ≤ 18 V, $T_J$ = +25°C) | RR | 41 | 49 | — | 40 | 49 | — | dB |
| Input-Output Voltage Differential ($T_J$ = +25°C) | $V_I/V_O$ | — | 1.7 | — | — | 1.7 | — | Vdc |

**MC78L08C, MC78L08AC ELECTRICAL CHARACTERISTICS** ($V_I$ = 14 V, $I_O$ = 40 mA, $C_I$ = 0.33 μF, $C_O$ = 0.1 μF, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | MC78L08AC Min | MC78L08AC Typ | MC78L08AC Max | MC78L08C Min | MC78L08C Typ | MC78L08C Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 7.7 | 8.0 | 8.3 | 7.36 | 8.0 | 8.64 | Vdc |
| Line Regulation<br>($T_J$ = +25°C, $I_O$ = 40 mA)<br>10.5 Vdc ≤ $V_I$ ≤ 23 Vdc<br>11 Vdc ≤ $V_I$ ≤ 23 Vdc | $Reg_{line}$ | —<br>— | 20<br>12 | 175<br>125 | —<br>— | 20<br>12 | 200<br>150 | mV |
| Load Regulation<br>($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 100 mA)<br>($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 40 mA) | $Reg_{load}$ | —<br>— | 15<br>8.0 | 80<br>40 | —<br>— | 15<br>6.0 | 80<br>40 | mV |
| Output Voltage<br>(10.5 Vdc ≤ $V_I$ ≤ 23 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA)<br>($V_I$ = 14 V, 1.0 mA ≤ $I_O$ ≤ 70 mA) | $V_O$ | 7.6<br>7.6 | —<br>— | 8.4<br>8.4 | 7.2<br>7.2 | —<br>— | 8.8<br>8.8 | Vdc |
| Input Bias Current<br>($T_J$ = +25°C)<br>($T_J$ = +125°C) | $I_{IB}$ | —<br>— | 3.0<br>— | 6.0<br>5.5 | —<br>— | 3.0<br>— | 6.0<br>5.5 | mA |
| Input Bias Current Change<br>(11 Vdc ≤ $V_I$ ≤ 23 Vdc)<br>(1.0 mA ≤ $I_O$ ≤ 40 mA) | $\Delta I_{IB}$ | —<br>— | —<br>— | 1.5<br>0.1 | —<br>— | —<br>— | 1.5<br>0.2 | mA |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 60 | — | — | 52 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 20 | — | — | 20 | — | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 40 mA, f = 120 Hz, 12 V ≤ $V_I$ ≤ 23 V, $T_J$ = +25°C) | RR | 37 | 57 | — | 36 | 55 | — | dB |
| Input-Output Voltage Differential ($T_J$ = +25°C) | $V_I/V_O$ | — | 1.7 | — | — | 1.7 | — | Vdc |

**MC78L12C, MC78L12AC ELECTRICAL CHARACTERISTICS** ($V_I$ = 19 V, $I_O$ = 40 mA, $C_I$ = 0.33 μF, $C_O$ = 0.1 μF, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | MC78L12AC | | | MC78L12C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 11.5 | 12 | 12.5 | 11.1 | 12 | 12.9 | Vdc |
| Line Regulation ($T_J$ = +25°C, $I_O$ = 40 mA) | $Reg_{line}$ | | | | | | | mV |
| 14.5 Vdc ≤ $V_I$ ≤ 27 Vdc | | — | 120 | 250 | — | 120 | 250 | |
| 16 Vdc ≤ $V_I$ ≤ 27 Vdc | | — | 100 | 200 | — | 100 | 200 | |
| Load Regulation | $Reg_{load}$ | | | | | | | mV |
| ($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 100 mA) | | — | 20 | 100 | — | 20 | 100 | |
| ($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 40 mA) | | — | 10 | 50 | — | 10 | 50 | |
| Output Voltage | $V_O$ | | | | | | | Vdc |
| (14.5 Vdc ≤ $V_I$ ≤ 27 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA) | | 11.4 | — | 12.6 | 10.8 | — | 13.2 | |
| ($V_I$ = 19 V, 1.0 mA ≤ $I_O$ ≤ 70 mA) | | 11.4 | — | 12.6 | 10.8 | — | 13.2 | |
| Input Bias Current | $I_{IB}$ | | | | | | | mA |
| ($T_J$ = +25°C) | | — | 4.2 | 6.5 | — | 4.2 | 6.5 | |
| ($T_J$ = +125°C) | | — | — | 6.0 | — | — | 6.0 | |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | | | | mA |
| (16 Vdc ≤ $V_I$ ≤ 27 Vdc) | | — | — | 1.5 | — | — | 1.5 | |
| (1.0 mA ≤ $I_O$ ≤ 40 mA) | | — | — | 0.1 | — | — | 0.2 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 80 | — | — | 80 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 24 | — | — | 24 | — | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 40 mA, f = 120 Hz, 15 V ≤ $V_I$ ≤ 25 V, $T_J$ = +25°C) | RR | 37 | 42 | — | 36 | 42 | — | dB |
| Input-Output Voltage Differential ($T_J$ = +25°C) | $V_I/V_O$ | — | 1.7 | — | — | 1.7 | — | Vdc |

**MC78L15C, MC78L15AC ELECTRICAL CHARACTERISTICS** ($V_I$ = 23 V, $I_O$ = 40 mA, $C_I$ = 0.33 μF, $C_O$ = 0.1 μF, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | MC78L15AC | | | MC78L15C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 14.4 | 15 | 15.6 | 13.8 | 15 | 16.2 | Vdc |
| Line Regulation ($T_J$ = +25°C, $I_O$ = 40 mA) | $Reg_{line}$ | | | | | | | mV |
| 17.5 Vdc ≤ $V_I$ ≤ 30 Vdc | | — | 130 | 300 | — | 130 | 300 | |
| 20 Vdc ≤ $V_I$ ≤ 30 Vdc | | — | 110 | 250 | — | 110 | 250 | |
| Load Regulation | $Reg_{load}$ | | | | | | | mV |
| ($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 100 mA) | | — | 25 | 150 | — | 25 | 150 | |
| ($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 40 mA) | | — | 12 | 75 | — | 12 | 75 | |
| Output Voltage | $V_O$ | | | | | | | Vdc |
| (17.5 Vdc ≤ $V_I$ ≤ 30 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA) | | 14.25 | — | 15.75 | 13.5 | — | 16.5 | |
| ($V_I$ = 23 V, 1.0 mA ≤ $I_O$ ≤ 70 mA) | | 14.25 | — | 15.75 | 13.5 | — | 16.5 | |
| Input Bias Current | $I_{IB}$ | | | | | | | mA |
| ($T_J$ = +25°C) | | — | 4.4 | 6.5 | — | 4.4 | 6.5 | |
| ($T_J$ = +125°C) | | — | — | 6.0 | — | — | 6.0 | |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | | | | mA |
| (20 Vdc ≤ $V_I$ ≤ 30 Vdc) | | — | — | 1.5 | — | — | 1.5 | |
| (1.0 mA ≤ $I_O$ ≤ 40 mA) | | — | — | 0.1 | — | — | 0.2 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 90 | — | — | 90 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 30 | — | — | 30 | — | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 40 mA, f = 120 Hz, 18.5 V ≤ $V_I$ ≤ 28.5 V, $T_J$ = +25°C) | RR | 34 | 39 | — | 33 | 39 | — | dB |
| Input-Output Voltage Differential ($T_J$ = +25°C) | $V_I/V_O$ | — | 1.7 | — | — | 1.7 | — | Vdc |

**MC78L18C, MC78L18AC ELECTRICAL CHARACTERISTICS** ($V_I$ = 27 V, $I_O$ = 40 mA, $C_I$ = 0.33 μF, $C_O$ = 0.1 μF, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | MC78L18AC | | | MC78L18C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 17.3 | 18 | 18.7 | 16.6 | 18 | 19.4 | Vdc |
| Line Regulation | $Reg_{line}$ | | | | | | | mV |
| ($T_J$ = +25°C, $I_O$ = 40 mA) | | | | | | | | |
| 21.4 Vdc ≤ $V_I$ ≤ 33 Vdc | | | | | — | 32 | 325 | |
| 20.7 Vdc ≤ $V_I$ ≤ 33 Vdc | | — | 45 | 325 | | | | |
| 22 Vdc ≤ $V_I$ ≤ 33 Vdc | | | | | — | 27 | 275 | |
| 21 Vdc ≤ $V_I$ ≤ 33 Vdc | | — | 35 | 275 | | | | |
| Load Regulation | $Reg_{load}$ | | | | | | | mV |
| ($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 100 mA) | | — | 30 | 170 | — | 30 | 170 | |
| ($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 40 mA) | | — | 15 | 85 | — | 15 | 85 | |
| Output Voltage | $V_O$ | | | | | | | Vdc |
| (21.4 Vdc ≤ $V_I$ ≤ 33 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA) | | | | | 16.2 | — | 19.8 | |
| (20.7 Vdc ≤ $V_I$ ≤ 33 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA) | | 17.1 | — | 18.9 | | | | |
| ($V_I$ = 27 V, 1.0 mA ≤ $I_O$ ≤ 70 mA) | | | | | 16.2 | — | 19.8 | |
| ($V_I$ = 27 V, 1.0 mA ≤ $I_O$ ≤ 70 mA) | | 17.1 | — | 18.9 | | | | |
| Input Bias Current | $I_{IB}$ | | | | | | | mA |
| ($T_J$ = +25°C) | | — | 3.1 | 6.5 | — | 3.1 | 6.5 | |
| ($T_J$ = +125°C) | | — | — | 6.0 | — | — | 6.0 | |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | | | | mA |
| (22 Vdc ≤ $V_I$ ≤ 33 Vdc) | | | | | — | — | 1.5 | |
| (21 Vdc ≤ $V_I$ = 33 Vdc) | | — | — | 1.5 | | | | |
| (1.0 mA ≤ $I_O$ ≤ 40 mA) | | — | — | 0.1 | — | — | 0.2 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 150 | — | — | 150 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 45 | — | — | 45 | — | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 40 mA, f = 120 Hz, 23 V ≤ $V_I$ ≤ 33 V, $T_J$ = +25°C) | RR | 33 | 48 | — | 32 | 46 | — | dB |
| Input-Output Voltage Differential ($T_J$ = +25°C) | $V_I/V_O$ | — | 1.7 | — | — | 1.7 | — | Vdc |

**MC78L24C, MC78L24AC ELECTRICAL CHARACTERISTICS** ($V_I$ = 33 V, $I_O$ = 40 mA, $C_I$ = 0.33 μF, $C_O$ = 0.1 μF, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | MC78L24AC | | | MC78L24C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 23 | 24 | 25 | 22.1 | 24 | 25.9 | Vdc |
| Line Regulation | $Reg_{line}$ | | | | | | | mV |
| ($T_J$ = +25°C, $I_O$ = 40 mA) | | | | | | | | |
| 27.5 Vdc ≤ $V_I$ ≤ 38 Vdc | | — | — | — | — | 35 | 350 | |
| 28 Vdc ≤ $V_I$ ≤ 80 Vdc | | — | 50 | 300 | — | 30 | 300 | |
| 27 Vdc ≤ $V_I$ ≤ 38 Vdc | | — | 60 | 350 | — | — | — | |
| Load Regulation | $Reg_{load}$ | | | | | | | mV |
| ($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 100 mA) | | — | 40 | 200 | — | 40 | 200 | |
| ($T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 40 mA) | | — | 20 | 100 | — | 20 | 100 | |
| Output Voltage | $V_O$ | | | | | | | Vdc |
| (28 Vdc ≤ $V_I$ ≤ 38 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA) | | | | | 21.6 | — | 26.4 | |
| (27 Vdc ≤ $V_I$ ≤ 38 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA) | | 22.8 | — | 25.2 | | | | |
| (28 Vdc ≤ $V_I$ = 33 V, 1.0 mA ≤ $I_O$ ≤ 70 mA) | | | | | 21.6 | — | 26.4 | |
| (27 Vdc ≤ $V_I$ ≤ 33 V, 1.0 mA ≤ $I_O$ ≤ 70 mA) | | 22.8 | — | 25.2 | | | | |
| Input Bias Current | $I_{IB}$ | | | | | | | mA |
| ($T_J$ = +25°C) | | — | 3.1 | 6.5 | — | 3.1 | 6.5 | |
| ($T_J$ = +125°C) | | — | — | 6.0 | — | — | 6.0 | |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | | | | mA |
| (28 Vdc ≤ $V_I$ ≤ 38 Vdc) | | — | — | 1.5 | — | — | 1.5 | |
| (1.0 mA ≤ $I_O$ ≤ 40 mA) | | — | — | 0.1 | — | — | 0.2 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 200 | — | — | 200 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 56 | — | — | 56 | — | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 40 mA, f = 120 Hz, 29 V ≤ $V_I$ ≤ 35 V, $T_J$ = +25°C) | RR | 31 | 45 | — | 30 | 43 | — | dB |
| Input-Output Voltage Differential ($T_J$ = +25°C) | $V_I/V_O$ | — | 1.7 | — | — | 1.7 | — | Vdc |

## TYPICAL CHARACTERISTICS

($T_A = +25^oC$ unless otherwise noted.)

**FIGURE 1 – DROPOUT CHARACTERISTICS**

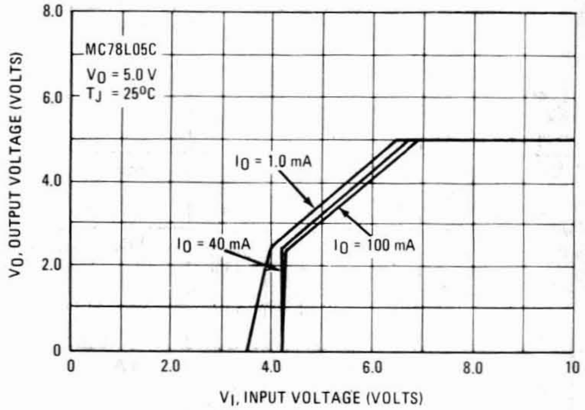


**FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE**

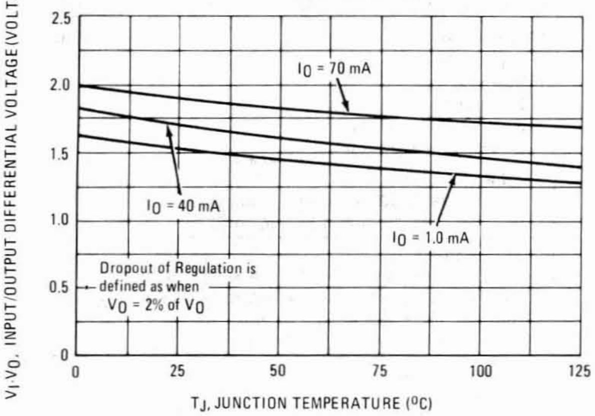


**FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE**

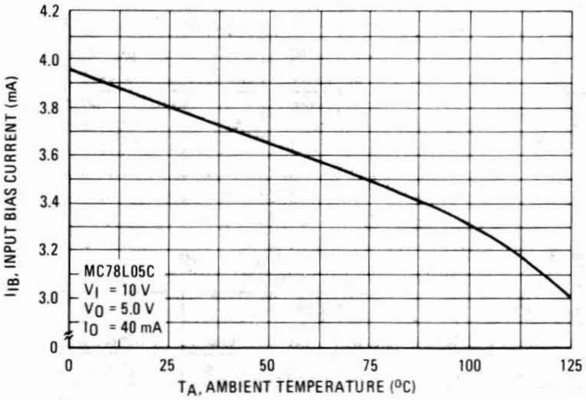


**FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE**

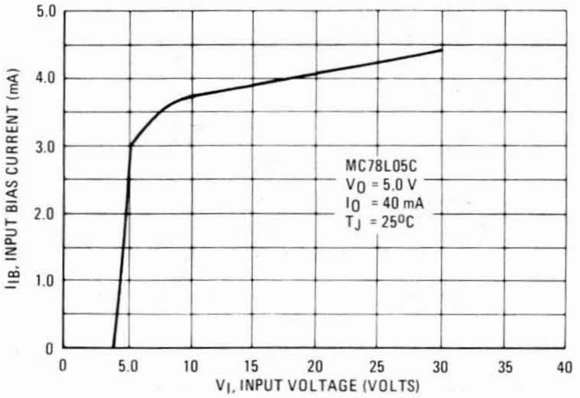


**FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package**

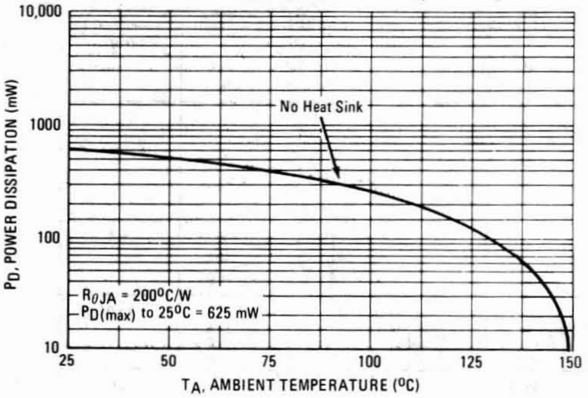
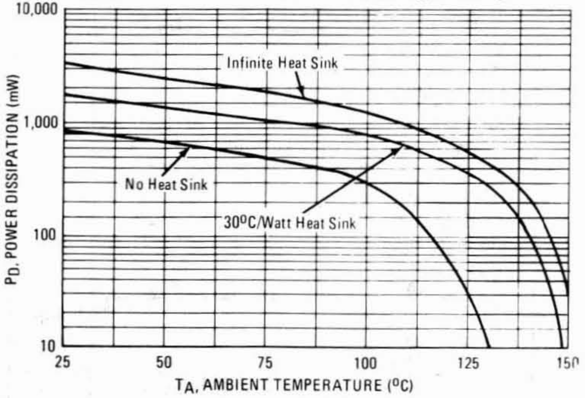


**FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package**



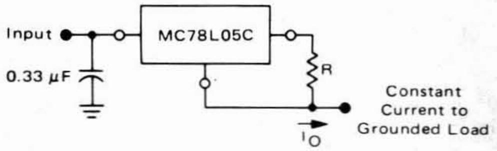
## APPLICATIONS INFORMATION

**Design Considerations**

The MC78L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short-Circuit Protection limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regular has no external sense lead. Bypassing the output is also recommended.

FIGURE 7 – CURRENT REGULATOR



The MC78L00C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_{IB}$$

$I_{IB}$ = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50-ohm, 1/2-W resistor and the output voltage compliance would be the input voltage less 7 volts.

FIGURE 8 – ±15 V TRACKING VOLTAGE REGULATOR

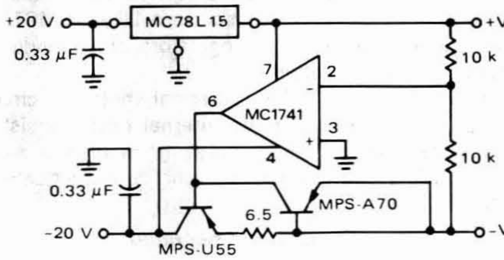
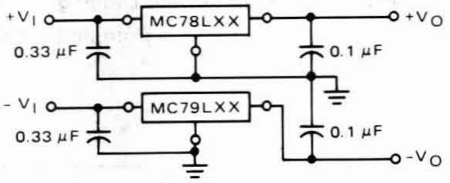


FIGURE 9 – POSITIVE AND NEGATIVE REGULATOR



MOTOROLA

# MC78M00
# Series

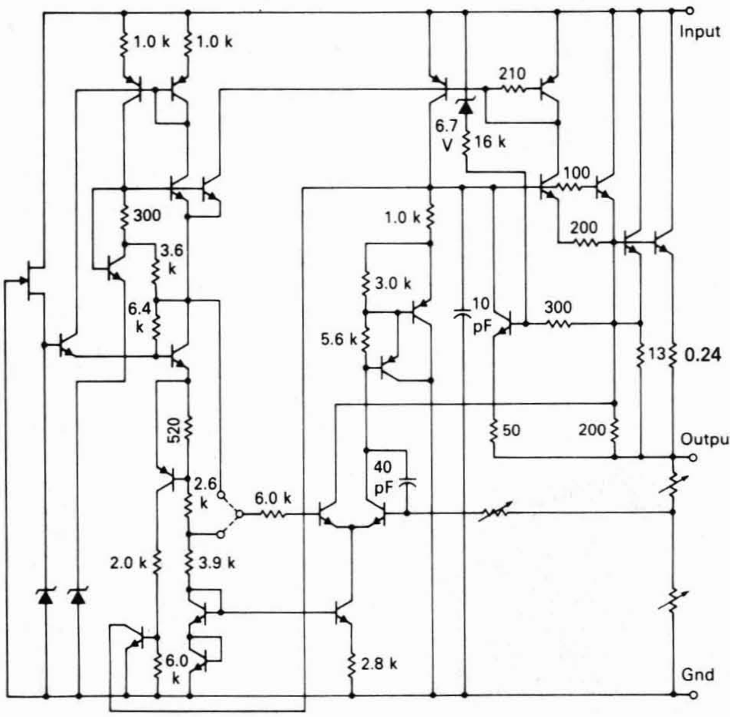
## THREE-TERMINAL MEDIUM CURRENT POSITIVE VOLTAGE REGULATORS

The MC78M00 Series positive voltage regulators are identical to the popular MC7800 Series devices, except that they are specified for only half the output current. Like the MC7800 devices, the MC78M00 three-terminal regulators are intended for local, on-card voltage regulation.

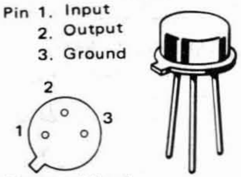
Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

## EQUIVALENT SCHEMATIC DIAGRAM



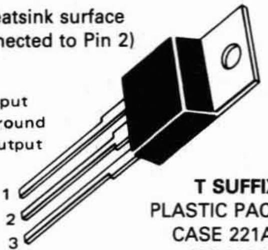
## THREE-TERMINAL MEDIUM CURRENT POSITIVE FIXED VOLTAGE REGULATORS



Pin 1. Input
2. Output
3. Ground

(Bottom View)

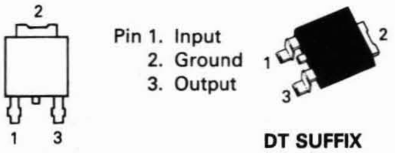
**G SUFFIX**
METAL PACKAGE
CASE 79-03
(Case connected to Pin 3)



(Heatsink surface connected to Pin 2)

Pin 1. Input
2. Ground
3. Output

**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220AB



Pin 1. Input
2. Ground
3. Output

(Heatsink surface is Pin 2)

**DT SUFFIX**
PLASTIC PACKAGE
CASE 369A-01
D-PAK

## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC78MXXCG | $T_J$ = 0°C to +125°C | Metal Can |
| MC78MXXCDT | $T_J$ = 0°C to +125°C | D-PAK |
| MC78MXXCT | | Plastic Power |
| MC78MXXBT | $T_J$ = −40°C to +125°C | Plastic Power |

### TYP NO./VOLTAGE

| | | | |
|---|---|---|---|
| MC78M05B,C | 5.0 Volts | MC78M15B,C | 15 Volts |
| MC78M06B,C | 6.0 Volts | MC78M18B,C | 18 Volts |
| MC78M08B,C | 8.0 Volts | MC78M20B,C | 20 Volts |
| MC78M12B,C | 12 Volts | MC78M24B,C | 24 Volts |

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (5.0 V – 18 V)<br>(20 V – 24 V) | $V_I$ | 35<br>40 | Vdc |
| Power Dissipation (Package Limitation)<br>Plastic Package<br>$T_A$ = 25°C<br>Derate above $T_A$ = 25°C<br>$T_C$ = 25°C<br>Derate above $T_C$ = 110°C<br>Metal Package<br>$T_A$ = 25°C<br>Derate above $T_A$ = 25°C<br>$T_C$ = 25°C<br>Derate above $T_C$ = 85°C | <br><br>$P_D$<br>$\theta_{JA}$<br>$P_D$<br>$\theta_{JC}$<br><br>$P_D$<br>$\theta_{JA}$<br>$P_D$<br>$\theta_{JC}$ | <br><br>Internally Limited<br>70<br>Internally Limited<br>5.0<br><br>Internally Limited<br>185<br>Internally Limited<br>25 | <br><br><br>°C/W<br><br>°C/W<br><br><br>°C/W<br><br>°C/W |
| Operating Junction Temperature Range MC78MXXC<br>MC78MXXB | $T_J$ | 0 to +125<br>−40 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**MC78M05 ELECTRICAL CHARACTERISTICS** ($V_I$ = 10 V, $I_O$ = 200 mA, *$T_{low} < T_J < +125°C$, $P_D \leq 5.0$ W unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 4.8 | 5.0 | 5.2 | Vdc |
| Line Regulation<br>($T_J$ = +25°C)<br>(7.0 Vdc ≤ $V_I$ ≤ 25 Vdc)<br>(8.0 Vdc ≤ $V_I$ ≤ 25 Vdc) | $Reg_{line}$ | <br><br><br>— | <br><br>3.0<br>1.0 | <br><br>100<br>50 | mV |
| Load Regulation<br>($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 500 mA)<br>($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 200 mA) | $Reg_{load}$ | <br>—<br>— | <br>20<br>10 | <br>100<br>50 | mV |
| Output Voltage<br>(8.0 Vdc ≤ $V_I$ ≤ 25 Vdc, 5.0 mA ≤ $I_O$ ≤ 200 mA) | $V_O$ | 4.75 | — | 5.25 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 3.2 | 6.0 | mA |
| Quiescent Current Change<br>(8.0 Vdc ≤ $V_I$ ≤ 25 Vdc)<br>(5.0 mA ≤ $I_O$ ≤ 200 mA) | $\Delta I_{IB}$ | <br>—<br>— | <br>—<br>— | <br>0.8<br>0.5 | mA |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 40 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 20 | — | mV/1.0 k Hrs. |
| Ripple Rejection ($I_O$ = 100 mA, f = 120 Hz, 8.0 V ≤ $V_I$ ≤ 18 V)<br>($I_O$ = 300 mA, f = 120 Hz, 8.0 ≤ $V_I$ ≤ 18 V, $T_J$ = 25°C) | RR | 62<br>62 | —<br>80 | —<br>— | dB |
| Input-Output Voltage Differential<br>($T_J$ = +25°C) | $V_I$-$V_O$ | — | 2.0 | — | Vdc |
| Short-Circuit Current Limit ($T_J$ = +25°C, $V_I$ = 35 V) | $I_{OS}$ | — | 50 | — | mA |
| Average Temperature Coefficient of Output Voltage<br>($I_O$ = 5.0 mA) | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |
| Peak Output Current<br>($T_J$ = 25°C) | $I_O$ | — | 700 | — | mA |

*$T_{low}$ = −40°C for MC78MXXB
= 0°C for MC78MXXC

**MC78M06 ELECTRICAL CHARACTERISTICS** ($V_I$ = 11 V, $I_O$ = 200 mA, *$T_{low} < T_J < +125°C$, $P_D \leq 5.0$ W unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 5.75 | 6.0 | 6.25 | Vdc |
| Line Regulation<br>($T_J$ = +25°C) | $Reg_{line}$ | | | | mV |
| (8.0 Vdc ≤ $V_I$ ≤ 25 Vdc) | | — | 5.0 | 100 | |
| (9.0 Vdc ≤ $V_I$ ≤ 25 Vdc) | | — | 1.5 | 50 | |
| Load Regulation | $Reg_{load}$ | | | | mV |
| ($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 500 mA) | | — | 20 | 120 | |
| ($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 200 mA) | | — | 10 | 60 | |
| Output Voltage<br>(9.0 Vdc ≤ $V_I$ ≤ 25 Vdc, 5.0 mA ≤ $I_O$ ≤ 200 mA) | $V_O$ | 5.7 | — | 6.3 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 3.2 | 6.0 | mA |
| Quiescent Current Change | $\Delta I_{IB}$ | | | | mA |
| (9.0 Vdc ≤ $V_I$ ≤ 25 Vdc) | | — | — | 0.8 | |
| (5.0 mA ≤ $I_O$ ≤ 200 mA) | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 45 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 24 | — | mV/1.0 k Hrs. |
| Ripple Rejection ($I_O$ = 100 mA, f = 120 Hz, 9.0 V ≤ $V_I$ ≤ 19 V) | RR | 59 | — | — | dB |
| ($I_O$ = 300 mA, f = 120 Hz, 9.0 V ≤ $V_I$ ≤ 19 V, $T_J$ = 25°C) | | 59 | 80 | — | |
| Input-Output Voltage Differential<br>($T_A$ = +25°C) | $V_I$-$V_O$ | — | 2.0 | — | Vdc |
| Short-Circuit Current Limit ($T_J$ = +25°C, $V_I$ = 35 V) | $I_{OS}$ | — | 50 | — | mA |
| Average Temperature Coefficient of Output Voltage<br>($I_O$ = 5.0 mA) | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |
| Peak Output Current<br>($T_J$ = 25°C) | $I_O$ | — | 700 | — | mA |

**MC78M08 ELECTRICAL CHARACTERISTICS** ($V_I$ = 14 V, $I_O$ = 200 mA, *$T_{low} < T_J < +125°C$, $P_D \leq 5.0$ W unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 7.7 | 8.0 | 8.3 | Vdc |
| Line Regulation<br>($T_J$ = +25°C) | $Reg_{line}$ | | | | mV |
| (10.5 Vdc ≤ $V_I$ ≤ 25 Vdc) | | — | 6.0 | 100 | |
| (11 Vdc ≤ $V_I$ ≤ 25 Vdc) | | — | 2.0 | 50 | |
| Load Regulation | $Reg_{load}$ | | | | mV |
| ($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 500 mA) | | — | 25 | 160 | |
| ($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 200 mA) | | — | 10 | 80 | |
| Output Voltage<br>(11.5 Vdc ≤ $V_I$ ≤ 25 Vdc, 5.0 mA ≤ $I_O$ ≤ 200 mA) | $V_O$ | 7.6 | — | 8.4 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 3.2 | 6.0 | mA |
| Quiescent Current Change | $\Delta I_{IB}$ | | | | mA |
| (11.5 Vdc ≤ $V_I$ ≤ 25 Vdc) | | — | — | 0.8 | |
| (5.0 mA ≤ $I_O$ ≤ 200 mA) | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 52 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 32 | — | mV/1.0 k Hrs. |
| Ripple Rejection | RR | | | | dB |
| ($I_O$ = 100 mA, f = 120 Hz, 11.5 V ≤ $V_I$ ≤ 21.5 V) | | 56 | — | — | |
| ($I_O$ = 300 mA, f = 120 Hz, 11.5 V ≤ $V_I$ ≤ 21.5 V, $T_J$ = 25°C) | | 56 | 80 | — | |
| Input-Output Voltage Differential<br>($T_J$ = +25°C) | $V_I$-$V_O$ | — | 2.0 | — | Vdc |
| Short-Circuit Current Limit ($T_J$ = +25°C, $V_I$ = 35 V) | $I_{OS}$ | — | 50 | — | mA |
| Average Temperature Coefficient of Output Voltage<br>($I_O$ = 5.0 mA) | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |
| Peak Output Current<br>($T_J$ = 25°C) | $I_O$ | — | 700 | — | mA |

*$T_{low}$ = −40°C for MC78MXXB
= 0°C for MC78MXXC

**MC78M12 ELECTRICAL CHARACTERISTICS** ($V_I$ = 19 V, $I_O$ = 200 mA, *$T_{low}$ < $T_J$ < +125°C, $P_D$ ≤ 5.0 W unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 11.5 | 12 | 12.5 | Vdc |
| Line Regulation<br>($T_J$ = +25°C)<br>(14.5 Vdc ≤ $V_I$ ≤ 30 Vdc)<br>(16 Vdc ≤ $V_I$ ≤ 22 Vdc) | $Reg_{line}$ | —<br>— | 8.0<br>2.0 | 100<br>50 | mV |
| Load Regulation<br>($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 500 mA)<br>($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 200 mA) | $Reg_{load}$ | —<br>— | 25<br>10 | 240<br>120 | mV |
| Output Voltage<br>(15.5 Vdc ≤ $V_I$ ≤ 27 Vdc, 5.0 mA ≤ $I_O$ ≤ 200 mA) | $V_O$ | 11.4 | — | 12.6 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 3.2 | 6.0 | mA |
| Quiescent Current Change<br>(15.5 Vdc ≤ $V_I$ ≤ 30 Vdc)<br>(5.0 mA ≤ $I_O$ ≤ 200 mA) | $\Delta I_{IB}$ | —<br>— | —<br>— | 0.8<br>0.5 | mA |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 75 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 48 | — | mV/1.0 k Hrs. |
| Ripple Rejection ($I_O$ = 100 mA, f = 120 Hz, 15 V ≤ $V_I$ ≤ 25 V)<br>($I_O$ = 300 mA, f = 120 Hz, 15 V ≤ $V_I$ ≤ 25 V, $T_J$ = 25°C) | RR | 55<br>55 | —<br>80 | —<br>— | dB |
| Input-Output Voltage Differential<br>($T_J$ = +25°C) | $V_I$-$V_O$ | — | 2.0 | — | Vdc |
| Short-Circuit Current Limit ($T_J$ = +25°C, $V_I$ = 35 V) | $I_{OS}$ | — | 50 | — | mA |
| Average Temperature Coefficient of Output Voltage<br>($I_O$ = 5.0 mA) | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |
| Peak Output Current<br>($T_J$ = 25°C) | $I_O$ | — | 700 | — | mA |

**MC78M15 ELECTRICAL CHARACTERISTICS** ($V_I$ = 23 V, $I_O$ = 200 mA, *$T_{low}$ < $T_J$ < +125°C, $P_D$ ≤ 5.0 W unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 14.4 | 15 | 15.6 | Vdc |
| Input Regulation<br>($T_J$ = +25°C)<br>(17.5 Vdc ≤ $V_I$ ≤ 30 Vdc)<br>(20 Vdc ≤ $V_I$ ≤ 30 Vdc) | $Reg_{line}$ | —<br>— | 10<br>3.0 | 100<br>50 | mV |
| Load Regulation<br>($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 500 mA)<br>($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 200 mA) | $Reg_{load}$ | —<br>— | 25<br>10 | 300<br>150 | mV |
| Output Voltage<br>(18.5 Vdc ≤ $V_I$ ≤ 30 Vdc, 5.0 mA ≤ $I_O$ ≤ 200 mA) | $V_O$ | 14.25 | — | 15.75 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 3.2 | 6.0 | mA |
| Quiescent Current Change<br>(18.5 Vdc ≤ $V_I$ ≤ 30 Vdc)<br>(5.0 mA ≤ $I_O$ ≤ 200 mA) | $\Delta I_{IB}$ | —<br>— | —<br>— | 0.8<br>0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 90 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 60 | — | mV/1.0 k Hrs. |
| Ripple Rejection<br>($I_O$ = 100 mA, f = 120 Hz, 18.5 V ≤ $V_I$ ≤ 28.5 V)<br>($I_O$ = 300 mA, f = 120 Hz, 18.5 V ≤ $V_I$ ≤ 28.5 V, $T_J$ = 25°C) | RR | 54<br>54 | —<br>70 | —<br>— | dB |
| Input-Output Voltage Differential<br>($T_J$ = +25°C) | $V_I$-$V_O$ | — | 2.0 | — | Vdc |
| Short-Circuit Current Limit ($T_J$ = +25°C, $V_I$ = 35 V) | $I_{OS}$ | — | 50 | — | mA |
| Average Temperature Coefficient of Output Voltage<br>($I_O$ = 5.0 mA) | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |
| Peak Output Current<br>($T_J$ = 25°C) | $I_O$ | — | 700 | — | mA |

*$T_{low}$ = −40°C for MC78MXXB
= 0°C for MC78MXXC

**MC78M18 ELECTRICAL CHARACTERISTICS** ($V_I$ = 27 V, $I_O$ = 200 mA, *$T_{low} < T_J < +125°C$, $P_D \leq 5.0$ W unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 17.3 | 18 | 18.7 | Vdc |
| Line Regulation | $Reg_{line}$ | | | | mV |
| ($T_J$ = +25°C) | | | | | |
| (21 Vdc ≤ $V_I$ ≤ 33 Vdc) | | — | 10 | 100 | |
| (24 Vdc ≤ $V_I$ ≤ 33 Vdc) | | — | 40 | 50 | |
| Load Regulation | $Reg_{load}$ | | | | mV |
| ($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 500 mA) | | — | 30 | 360 | |
| ($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 200 mA) | | — | 10 | 180 | |
| Output Voltage<br>(22 Vdc ≤ $V_I$ ≤ 33 Vdc, 5.0 mA ≤ $I_O$ ≤ 200 mA) | $V_O$ | 17.1 | — | 18.9 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 3.2 | 6.5 | mA |
| Quiescent Current Change | $\Delta I_{IB}$ | | | | mA |
| (22 Vdc ≤ $V_I$ ≤ 33 Vdc) | | — | — | 0.8 | |
| (5.0 mA ≤ $I_O$ ≤ 200 mA) | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 100 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 72 | — | mV/1.0 k Hrs. |
| Ripple Rejection ($I_O$ = 100 mA, f = 120 Hz, 22 V ≤ $V_I$ ≤ 32 V) | RR | 53 | — | — | dB |
| ($I_O$ = 300 mA, f = 120 Hz, 22 V ≤ $V_I$ ≤ 32 V, $T_J$ = 25°C) | | 53 | 70 | — | |
| Input-Output Voltage Differential<br>($T_J$ = +25°C) | $V_I$-$V_O$ | — | 2.0 | — | Vdc |
| Short-Circuit Current Limit ($T_J$ = +25°C, $V_I$ = 35 V) | $I_{OS}$ | — | 50 | — | mA |
| Average Temperature Coefficient of Output Voltage<br>($I_O$ = 5.0 mA) | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |
| Peak Output Current<br>($T_J$ = 25°C) | $I_O$ | — | 700 | — | mA |

**MC78M20 ELECTRICAL CHARACTERISTICS** ($V_I$ = 29 V, $I_O$ = 200 mA, *$T_{low} < T_J < +125°C$, $P_D \leq 5.0$ W unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 19.2 | 20 | 20.8 | Vdc |
| Line Regulation | $Reg_{line}$ | | | | mV |
| ($T_J$ = +25°C) | | | | | |
| (23 Vdc ≤ $V_I$ ≤ 35 Vdc) | | — | 10 | 100 | |
| (24 Vdc ≤ $V_I$ ≤ 35 Vdc) | | — | 5.0 | 50 | |
| Load Regulation | $Reg_{load}$ | | | | mV |
| ($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 500 mA) | | — | 30 | 400 | |
| ($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 200 mA) | | — | 10 | 200 | |
| Output Voltage<br>(24 Vdc ≤ $V_I$ ≤ 35 Vdc, 5.0 mA ≤ $I_O$ ≤ 200 mA) | $V_O$ | 19 | — | 21 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 3.2 | 6.5 | mA |
| Quiescent Current Change | $\Delta I_{IB}$ | | | | mA |
| (24 Vdc ≤ $V_I$ ≤ 35 Vdc) | | — | — | 0.8 | |
| (5.0 mA ≤ $I_O$ ≤ 200 mA) | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 110 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 80 | — | mV/1.0 k Hrs. |
| Ripple Rejection ($I_O$ = 100 mA, f = 120 Hz, 24 V ≤ $V_I$ ≤ 34 V) | RR | 52 | — | — | dB |
| ($I_O$ = 300 mA, f = 120 Hz, 24 V ≤ $V_I$ ≤ 34 V, $T_J$ = 25°C) | | 52 | 70 | — | |
| Input-Output Voltage Differential<br>($T_J$ = +25°C) | $V_I$-$V_O$ | — | 2.0 | — | Vdc |
| Short-Circuit Current Limit ($T_J$ = +25°C, $V_I$ = 35 V) | $I_{OS}$ | — | 50 | — | mA |
| Average Temperature Coefficient of Output Voltage<br>($I_O$ = 5.0 mA) | $\Delta V_O/\Delta T$ | — | −1.1 | — | mV/°C |
| Peak Output Current<br>($T_J$ = 25°C) | $I_O$ | — | 700 | — | mA |

*$T_{low}$ = −40°C for MC78MXXB
= 0°C for MC78MXXC

**MC78M24 ELECTRICAL CHARACTERISTICS** ($V_I$ = 33 V, $I_O$ = 200 mA, *$T_{low} < T_J < +125°C$, $P_D \leq 5.0$ W unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | 23 | 24 | 25 | Vdc |
| Line Regulation | $Reg_{line}$ | | | | mV |
| ($T_J$ = +25°C) | | | | | |
| (27 Vdc ≤ $V_I$ ≤ 38 Vdc) | | — | 10 | 100 | |
| (28 Vdc ≤ $V_I$ ≤ 38 Vdc) | | — | 5.0 | 50 | |
| Load Regulation | $Reg_{load}$ | | | | mV |
| ($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 500 mA) | | — | 30 | 480 | |
| ($T_J$ = +25°C, 5.0 mA ≤ $I_O$ ≤ 200 mA) | | — | 10 | 240 | |
| Output Voltage<br>(28 Vdc ≤ $V_I$ ≤ 38 Vdc, 5.0 mA ≤ $I_O$ ≤ 200 mA) | $V_O$ | 22.8 | — | 25.2 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 3.2 | 7.0 | mA |
| Quiescent Current Change | $\Delta I_{IB}$ | | | | mA |
| (28 Vdc ≤ $V_I$ ≤ 38 Vdc) | | — | — | 0.8 | |
| (5.0 mA ≤ $I_O$ ≤ 200 mA) | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 170 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | 96 | — | mV/1.0 k Hrs. |
| Ripple Rejection ($I_O$ = 100 mA, f = 120 Hz, 28 V ≤ $V_I$ ≤ 38 V) | RR | 50 | — | — | dB |
| ($I_O$ = 300 mA, f = 120 Hz, 28 V ≤ $V_I$ ≤ 38 V, $T_J$ = 25°C) | | 50 | 70 | — | |
| Input-Output Voltage Differential<br>($I_O$ = 5.0 mA) | $V_I$-$V_O$ | — | 2.0 | — | Vdc |
| Short-Circuit Current Limit ($T_J$ = +25°C) | $I_{OS}$ | — | 50 | — | mA |
| Average Temperature Coefficient of Output Voltage<br>($I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C) | $\Delta V_O/\Delta T$ | — | −1.2 | — | mV/°C |
| Peak Output Current<br>($T_J$ = 25°C) | $I_O$ | — | 700 | — | mA |

*$T_{low}$ = −40°C for MC78MXXB
= 0°C for MC78MXXC

## DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

## TYPICAL PERFORMANCE CURVES

FIGURE 1 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE TO-220AB (CASE 221A)

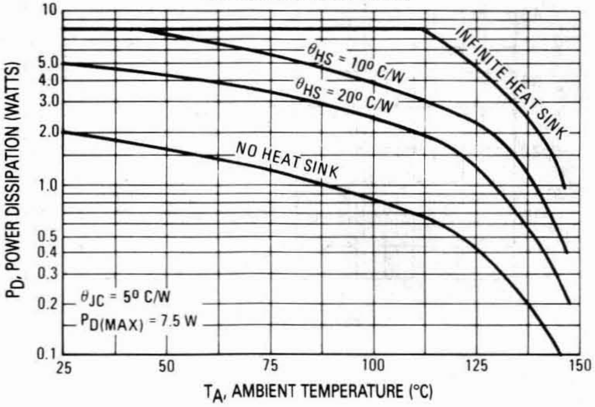
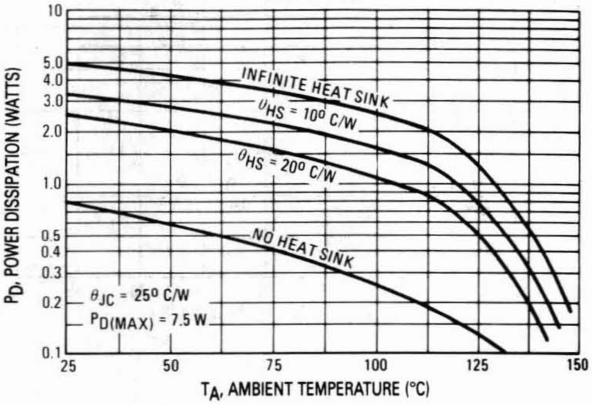


FIGURE 2 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (CASE 79)



## TYPICAL PERFORMANCE CURVES

**FIGURE 3 — PEAK OUTPUT CURRENT versus INPUT/OUTPUT DIFFERENTIAL VOLTAGE**

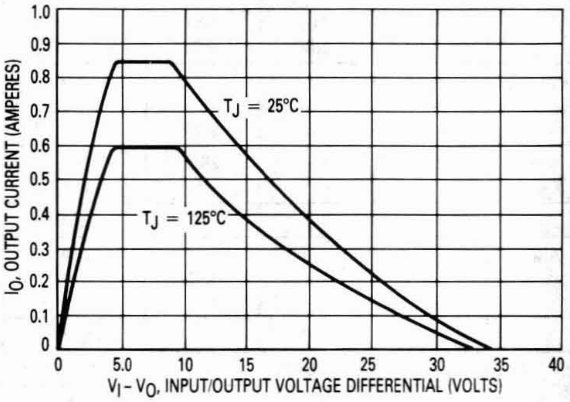


**FIGURE 4 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE**

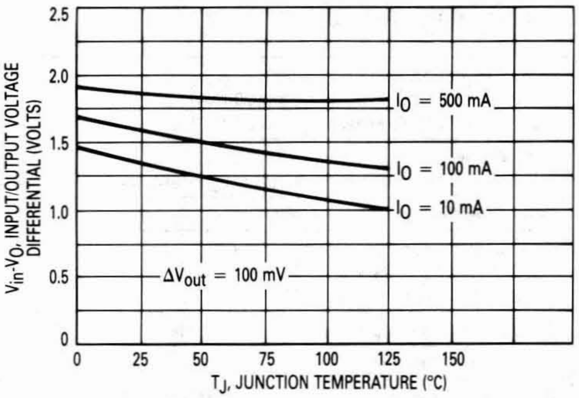


**FIGURE 5 — RIPPLE REJECTION versus FREQUENCY**

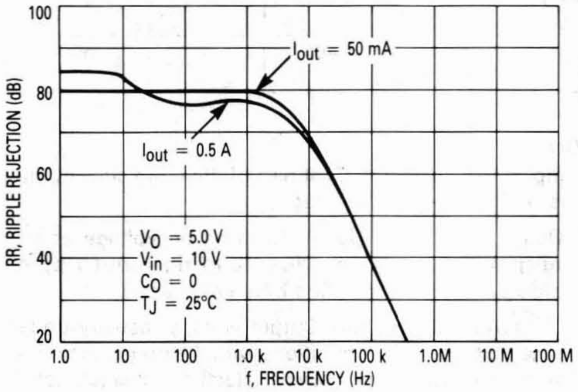


**FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT**

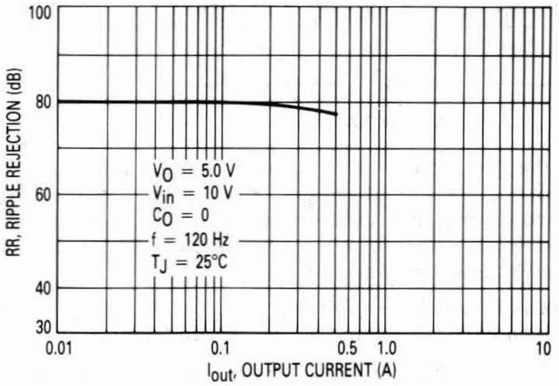


**FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE**

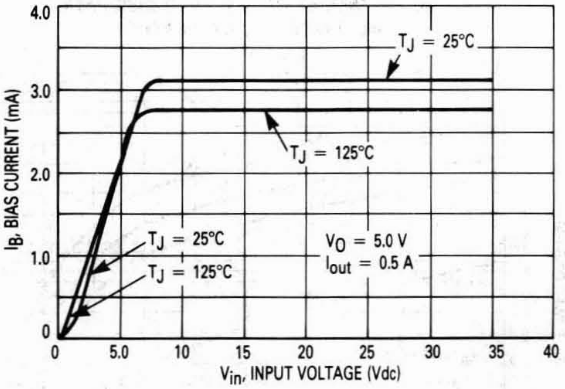
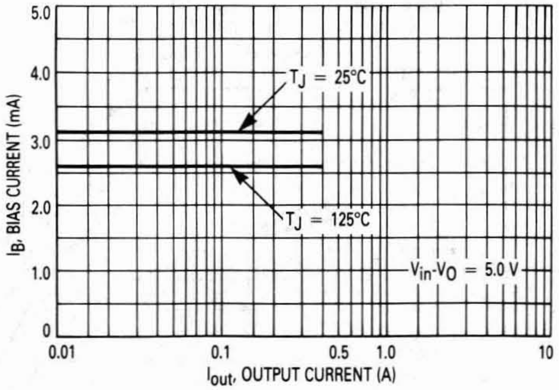


**FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT**



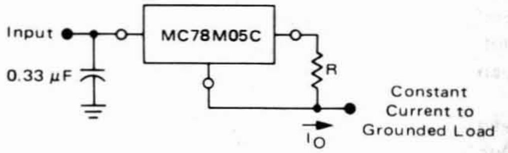
## APPLICATIONS INFORMATION

**Design Considerations**

The MC78M00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the reulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 $\mu$F or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

### FIGURE 9 — CURRENT REGULATOR



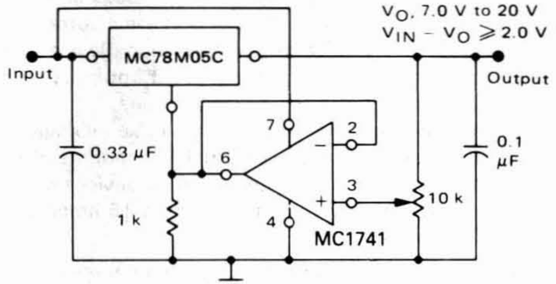
The MC78M00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78M05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ \text{V}}{R} + I_{IB}$$

$I_{IB}$ = 1.5 mA over line and load changes

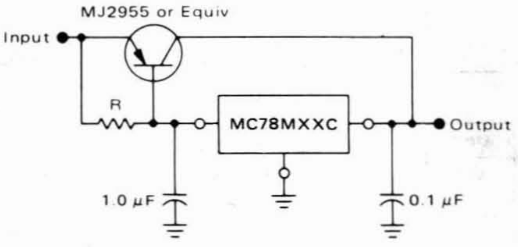
For example, a 500 mA current source would require R to be a 10-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7.0 volts.

### FIGURE 10 — ADJUSTABLE OUTPUT REGULATOR



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

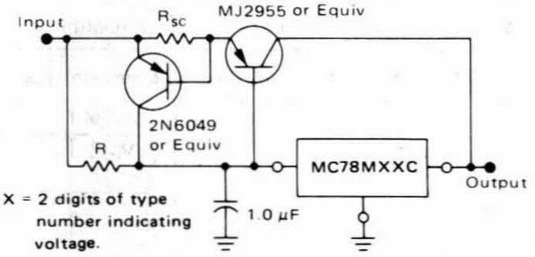
### FIGURE 11 — CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC78M00 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the $V_{BE}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by $V_{BE}$ of the pass transistor.

### FIGURE 12 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION

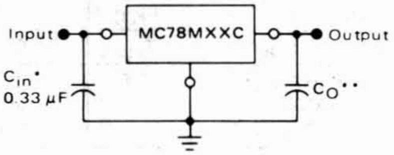


XX = 2 digits of type number indicating voltage.

The circuit of Figure 7 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, $R_{SC}$, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a two-ampere plastic power transistor is specified.

### STANDARD APPLICATION

A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.



* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_O$ improves stability and transient response.

**MOTOROLA**

# MC78T00 Series

## Specifications and Applications Information

### THREE-AMPERE POSITIVE VOLTAGE REGULATORS

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on A-suffix 5.0, 12 and 15 volt device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to supply up to 15 amperes at the nominal output voltage.

- Output Current in Excess of 3.0 Amperes
- Power Dissipation: 30 W (K-Suffix), 25 W (T-Suffix)
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Thermal Regulation is Specified
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (5.0 V–12 V)<br>(15 V–24 V) | $V_{in}$ | 35<br>40 | Vdc |
| Power Dissipation and Thermal Characteristics | | | |
| Plastic Package (Note 2) | | | |
| $T_A$ = +25°C | $P_D$ | Internally Limited | |
| Thermal Resistance, Junction to Air | $R_{\theta JA}$ | 65 | °C/W |
| $T_C$ = +25°C | $P_D$ | Internally Limited | |
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 2.5 | °C/W |
| Metal Package (Note 2) | | | |
| $T_A$ = +25°C | $P_D$ | Internally Limited | |
| Thermal Resistance, Junction to Air | $R_{\theta JA}$ | 35 | °C/W |
| $T_C$ = +25°C | $P_D$ | Internally Limited | |
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 2.5 | °C/W |
| Storage Junction Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Operating Junction Temperature Range | $T_J$ | | °C |
| MC78T00, A | | -55 to +150 | |
| MC78T00C, AC | | 0 to +125 | |

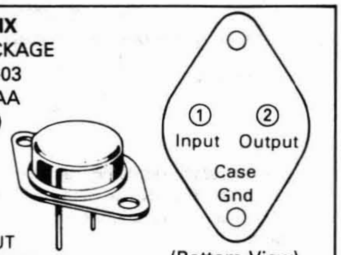
**ORDERING INFORMATION**

| Device | Output Voltage Tolerance | Operating Junction Temperature Range | Package |
|---|---|---|---|
| MC78TXXK | 4% | -55 to +150°C | Metal Power |
| MC78TXXAK | 2%* | | |
| MC78TXXCK | 4% | 0 to +125°C | |
| MC78TXXACK | 2%* | | |
| MC78TXXCT | 4% | | Plastic Power |
| MC78TXXACT | 2%* | | |

**THREE-AMPERE POSITIVE FIXED VOLTAGE REGULATORS**

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

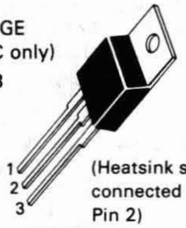
**K SUFFIX**
METAL PACKAGE
CASE 1-03
TO-204AA
(TO-3)



(Bottom View)

Pin 1. INPUT
2. OUTPUT
CASE GROUND

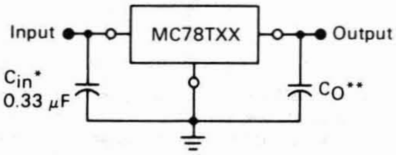
**T SUFFIX**
PLASTIC PACKAGE
(MC78TXXC and AC only)
CASE 221A-03
TO-220AB



Pin 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2)

**STANDARD APPLICATION**



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.2 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details).

** = $C_O$ is not needed for stability; however, it does improve transient response.

| TYPE NO./VOLTAGE | | | |
|---|---|---|---|
| MC78T05 | 5.0 Volts | MC78T15 | 15 Volts |
| MC78T06 | 6.0 Volts | MC78T18 | 18 Volts |
| MC78T08 | 8.0 Volts | MC78T24 | 24 Volts |
| MC78T12 | 12 Volts | | |

## MC78T05, A, AC, C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 10 V, $I_O$ = 3.0 A, $T_J = T_{low}$ to $T_{high}$ [Note 1], $P_O \leq P_{max}$ [Note 2], unless otherwise noted).

| Characteristic | Symbol | MC78T05A, AC | | | MC78T05, C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage<br>($5.0\ mA \leq I_O \leq 3.0\ A$, $T_J = +25°C$)<br>($5.0\ mA \leq I_O \leq 3.0\ A$; $5.0\ mA \leq I_O \leq 2.0\ A$, $7.3\ Vdc \leq V_{in} \leq 20\ Vdc$) | $V_O$ | 4.9<br>4.8 | 5.0<br>5.0 | 5.1<br>5.2 | 4.8<br>4.75 | 5.0<br>5.0 | 5.2<br>5.25 | Vdc |
| Line Regulation (Note 3)<br>($7.2\ Vdc \leq V_{in} \leq 35\ Vdc$, $I_O = 5.0\ mA$, $T_J = +25°C$; $7.2\ Vdc \leq V_{in} \leq 35\ Vdc$, $I_O = 1.0\ A$, $T_J = +25°C$; $7.5\ Vdc \leq V_{in} \leq 20\ Vdc$, $I_O = 2.0\ A$; $8.0\ Vdc \leq V_{in} \leq 12\ Vdc$, $I_O = 3.0\ A$) | $Reg_{line}$ | — | 3.0 | 10 | — | 3.0 | 25 | mV |
| Load Regulation (Note 3)<br>($5.0\ mA \leq I_O \leq 3.0\ A$, $T_J = +25°C$)<br>($5.0\ mA \leq I_O \leq 3.0\ A$) | $Reg_{load}$ | —<br>— | 10<br>15 | 25<br>50 | —<br>— | 10<br>15 | 30<br>80 | mV |
| Thermal Regulation<br>(Pulse = 10 ms, P = 20 W, $T_A$ = +25°C) | $Reg_{therm}$ | — | 0.001 | 0.01 | — | 0.002 | 0.03 | $\%V_O/W$ |
| Quiescent Current<br>($5.0\ mA \leq I_O \leq 3.0\ A$, $T_J = +25°C$)<br>($5.0\ mA \leq I_O \leq 3.0\ A$) | $I_B$ | —<br>— | 3.5<br>4.0 | 5.0<br>6.0 | —<br>— | 3.5<br>4.0 | 5.0<br>6.0 | mA |
| Quiescent Current Change<br>($7.2\ Vdc \leq V_{in} \leq 35\ Vdc$, $I_O = 5.0\ mA$, $T_J = +25°C$; $7.5\ Vdc \leq V_{in} \leq 20\ Vdc$, $I_O = 2.0\ A$; $5.0\ mA \leq I_O \leq 3.0\ A$) | $\Delta I_B$ | — | 0.1 | 0.5 | — | 0.1 | 0.8 | mA |
| Ripple Rejection<br>($8.0\ Vdc \leq V_{in} \leq 18\ Vdc$, f = 120 Hz, $I_O = 2.0\ A$) | RR | 68 | 75 | — | 65 | 75 | — | dB |
| Dropout Voltage ($I_O = 3.0\ A$, $T_J = +25°C$) | $V_{in}-V_O$ | — | 2.2 | 2.5 | — | 2.2 | 2.5 | Vdc |
| Output Noise Voltage<br>($10\ Hz \leq f \leq 100\ kHz$, $T_J = +25°C$) | $V_n$ | — | 10 | — | — | 10 | — | $\mu V/V_O$ |
| Output Resistance (f = 1.0 kHz) | $R_O$ | — | 2.0 | — | — | 2.0 | — | mΩ |
| Short Circuit Current Limit<br>($V_{in}$ = 35 Vdc, $T_J = +25°C$) | $I_{SC}$ | — | 1.5 | 2.5 | — | 1.5 | 2.5 | A |
| Peak Output Current ($T_J = +25°C$) | $I_{max}$ | — | 5.0 | — | — | 5.0 | — | A |
| Average Temperature Coefficient of Output Voltage ($I_O = 5.0\ mA$)<br>MC78T05, MC78T05A<br>MC78T05AC, C | $TCV_O$ | —<br>— | 0.2<br>0.2 | —<br>— | —<br>— | 0.2<br>0.2 | —<br>— | mV/°C |

NOTE 1. $T_{low}$ = −55°C for MC78TXX,A $\quad T_{high}$ = +150°C for MC78TXX,A
= 0°C for MC78TXXC,AC $\quad$ = +125°C for MC78TXXC,AC

2. Although power dissipation is internally limited, specifications apply only for $P_O \leq P_{max}$
$P_{max}$ = 30 W for K(TO-3) package $\quad P_{max}$ = 25 W for T(TO-220) package.

3. Line and load regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC78T06, C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 11 V, $I_O$ = 3.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1], $P_O \leqslant P_{max}$ [Note 2], unless otherwise noted).

| Characteristic | Symbol | MC78T06, C | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Output Voltage | $V_O$ | | | | Vdc |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A, $T_J$ = +25°C) | | 5.75 | 6.0 | 6.25 | |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A;<br>5.0 mA ≤ $I_O$ ≤ 2.0 A, 8.3 Vdc ≤ $V_{in}$ ≤ 21 Vdc) | | 5.7 | 6.0 | 6.3 | |
| Line Regulation (Note 3)<br>(8.25 Vdc ≤ $V_{in}$ ≤ 35 Vdc, $I_O$ = 5.0 mA, $T_J$ = +25°C;<br>8.25 Vdc ≤ $V_{in}$ ≤ 35 Vdc, $I_O$ = 1.0 A, $T_J$ = +25°C;<br>8.6 Vdc ≤ $V_{in}$ ≤ 21 Vdc, $I_O$ = 2.0 A;<br>9.0 Vdc ≤ $V_{in}$ ≤ 13 Vdc, $I_O$ = 3.0 A) | $Reg_{line}$ | — | 4.0 | 30 | mV |
| Load Regulation (Note 3) | $Reg_{load}$ | | | | mV |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A, $T_J$ = +25°C) | | — | 10 | 30 | |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A) | | — | 15 | 80 | |
| Thermal Regulation<br>(Pulse = 10 ms, P = 20 W, $T_A$ = +25°C) | $Reg_{therm}$ | — | 0.002 | 0.03 | %$V_O$/W |
| Quiescent Current | $I_B$ | | | | mA |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A, $T_J$ = +25°C) | | — | 3.5 | 5.0 | |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A) | | — | 4.0 | 6.0 | |
| Quiescent Current Change<br>(8.25 Vdc ≤ $V_{in}$ ≤ 35 Vdc, $I_O$ = 5.0 mA, $T_J$ = +25°C;<br>8.6 Vdc ≤ $V_{in}$ ≤ 21 Vdc, $I_O$ = 2.0 A;<br>5.0 mA ≤ $I_O$ ≤ 3.0 A) | $\Delta I_B$ | — | 0.1 | 0.8 | mA |
| Ripple Rejection<br>(9.0 Vdc ≤ $V_{in}$ ≤ 19 Vdc, f = 120 Hz, $I_O$ = 2.0 A) | RR | 63 | 73 | — | dB |
| Dropout Voltage ($I_O$ = 3.0 A, $T_J$ = +25°C) | $V_{in}-V_O$ | — | 2.2 | 2.5 | Vdc |
| Output Noise Voltage<br>(10 Hz ≤ f ≤ 100 kHz, $T_J$ = +25°C) | $V_n$ | — | 10 | — | μV/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $R_O$ | — | 2.0 | — | mΩ |
| Short Circuit Current Limit<br>($V_{in}$ = 35 Vdc, $T_J$ = +25°C) | $I_{SC}$ | — | 1.5 | 2.5 | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | — | 5.0 | — | A |
| Average Temperature Coefficient<br>of Output Voltage ($I_O$ = 5.0 mA) | $TCV_O$ | | | | mV/°C |
| MC78T06 | | — | 0.3 | — | |
| MC78T06C | | — | 0.3 | — | |

NOTE 1. $T_{low}$ = −55°C for MC78TXX,A  $T_{high}$ = +150°C for MC78TXX,A
= 0°C for MC78TXXC,AC  = +125°C for MC78TXXC,AC

2. Although power dissipation is internally limited, specifications apply only for $P_O \leqslant P_{max}$
$P_{max}$ = 30 W for K(TO-3) package  $P_{max}$ = 25 W for T(TO-220) package.

3. Line and load regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC78T08, C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 14 V, $I_O$ = 3.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1], $P_O \leqslant P_{max}$ [Note 2], unless otherwise noted).

| Characteristic | Symbol | MC78T08, C | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Output Voltage<br>($5.0\ mA \leqslant I_O \leqslant 3.0\ A$, $T_J = +25°C$)<br>($5.0\ mA \leqslant I_O \leqslant 3.0\ A$;<br>$5.0\ mA \leqslant I_O \leqslant 2.0\ A$, $10.4\ Vdc \leqslant V_{in} \leqslant 23\ Vdc$) | $V_O$ | <br>7.7<br>7.6 | <br>8.0<br>8.0 | <br>8.3<br>8.4 | Vdc |
| Line Regulation (Note 3)<br>($10.3\ Vdc \leqslant V_{in} \leqslant 35\ Vdc$, $I_O = 5.0\ mA$, $T_J = +25°C$;<br>$10.3\ Vdc \leqslant V_{in} \leqslant 35\ Vdc$, $I_O = 1.0\ A$, $T_J = +25°C$;<br>$10.7\ Vdc \leqslant V_{in} \leqslant 23\ Vdc$, $I_O = 2.0\ A$;<br>$11\ Vdc \leqslant V_{in} \leqslant 17\ Vdc$, $I_O = 3.0\ A$) | $Reg_{line}$ | — | 4.0 | 35 | mV |
| Load Regulation (Note 3)<br>($5.0\ mA \leqslant I_O \leqslant 3.0\ A$, $T_J = +25°C$)<br>($5.0\ mA \leqslant I_O \leqslant 3.0\ A$) | $Reg_{load}$ | <br>—<br>— | <br>10<br>15 | <br>30<br>80 | mV |
| Thermal Regulation<br>(Pulse = 10 ms, P = 20 W, $T_A$ = +25°C) | $Reg_{therm}$ | — | 0.002 | 0.03 | $\%V_O/W$ |
| Quiescent Current<br>($5.0\ mA \leqslant I_O \leqslant 3.0\ A$, $T_J = +25°C$)<br>($5.0\ mA \leqslant I_O \leqslant 3.0\ A$) | $I_B$ | <br>—<br>— | <br>3.5<br>4.0 | <br>5.0<br>6.0 | mA |
| Quiescent Current Change<br>($10.3\ Vdc \leqslant V_{in} \leqslant 35\ Vdc$, $I_O = 5.0\ mA$, $T_J = +25°C$;<br>$10.7\ Vdc \leqslant V_{in} \leqslant 23\ Vdc$, $I_O = 2.0\ A$;<br>$5.0\ mA \leqslant I_O \leqslant 3.0\ A$) | $\Delta I_B$ | — | 0.1 | 0.8 | mA |
| Ripple Rejection<br>($11\ Vdc \leqslant V_{in} \leqslant 21\ Vdc$, f = 120 Hz, $I_O = 2.0\ A$) | RR | 61 | 71 | — | dB |
| Dropout Voltage ($I_O = 3.0\ A$, $T_J = +25°C$) | $V_{in}-V_O$ | — | 2.2 | 2.5 | Vdc |
| Output Noise Voltage<br>($10\ Hz \leqslant f \leqslant 100\ kHz$, $T_J = +25°C$) | $V_n$ | — | 10 | — | $\mu V/V_O$ |
| Output Resistance (f = 1.0 kHz) | $R_O$ | — | 2.0 | — | mΩ |
| Short Circuit Current Limit<br>($V_{in} = 35\ Vdc$, $T_J = +25°C$) | $I_{SC}$ | — | 1.5 | 2.5 | A |
| Peak Output Current ($T_J = +25°C$) | $I_{max}$ | — | 5.0 | — | A |
| Average Temperature Coefficient<br>of Output Voltage ($I_O = 5.0\ mA$)<br>MC78T08<br>MC78T08C | $TCV_O$ | <br><br>—<br>— | <br><br>0.3<br>0.3 | <br><br>—<br>— | mV/°C |

NOTE 1. $T_{low}$ = −55°C for MC78TXX,A
= 0°C for MC78TXXC,AC

$T_{high}$ = +150°C for MC78TXX,A
= +125°C for MC78TXXC,AC

2. Although power dissipation is internally limited, specifications apply only for $P_O \leqslant P_{max}$
$P_{max}$ = 30 W for K(TO-3) package
$P_{max}$ = 25 W for T(TO-220) package.

3. Line and load regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC78T12, A, AC, C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 19 V, $I_O$ = 3.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1], $P_O \leqslant P_{max}$ [Note 2], unless otherwise noted).

| Characteristic | Symbol | MC78T12A, AC | | | MC78T12, C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage | $V_O$ | | | | | | | Vdc |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A, $T_J$ = +25°C) | | 11.75 | 12 | 12.25 | 11.5 | 12 | 12.5 | |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A;<br>5.0 mA $\leqslant I_O \leqslant$ 2.0 A, 14.5 Vdc $\leqslant V_{in} \leqslant$ 27 Vdc) | | 11.5 | 12 | 12.5 | 11.4 | 12 | 12.6 | |
| Line Regulation (Note 3)<br>(14.5 Vdc $\leqslant V_{in} \leqslant$ 35 Vdc, $I_O$ = 5.0 mA, $T_J$ = +25°C;<br>14.5 Vdc $\leqslant V_{in} \leqslant$ 35 Vdc, $I_O$ = 1.0 A, $T_J$ = +25°C;<br>14.9 Vdc $\leqslant V_{in} \leqslant$ 27 Vdc, $I_O$ = 2.0 A;<br>16 Vdc $\leqslant V_{in} \leqslant$ 22 Vdc, $I_O$ = 3.0 A) | $Reg_{line}$ | — | 6.0 | 18 | — | 6.0 | 45 | mV |
| Load Regulation (Note 3) | $Reg_{load}$ | | | | | | | mV |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A, $T_J$ = +25°C) | | — | 10 | 25 | — | 10 | 30 | |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A) | | — | 15 | 50 | — | 15 | 80 | |
| Thermal Regulation<br>(Pulse = 10 ms, P = 20 W, $T_A$ = +25°C) | $Reg_{therm}$ | — | 0.001 | 0.01 | — | 0.002 | 0.03 | %$V_O$/W |
| Quiescent Current | $I_B$ | | | | | | | mA |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A, $T_J$ = +25°C) | | — | 3.5 | 5.0 | — | 3.5 | 5.0 | |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A) | | — | 4.0 | 6.0 | — | 4.0 | 6.0 | |
| Quiescent Current Change<br>(14.5 Vdc $\leqslant V_{in} \leqslant$ 35 Vdc, $I_O$ = 5.0 mA, $T_J$ = +25°C;<br>14.9 Vdc $\leqslant V_{in} \leqslant$ 27 Vdc, $I_O$ = 2.0 A;<br>5.0 mA $\leqslant I_O \leqslant$ 3.0 A) | $\Delta I_B$ | — | 0.1 | 0.5 | — | 0.1 | 0.8 | mA |
| Ripple Rejection<br>(15 Vdc $\leqslant V_{in} \leqslant$ 25 Vdc, f = 120 Hz, $I_O$ = 2.0 A) | RR | 61 | 67 | — | 57 | 67 | — | dB |
| Dropout Voltage ($I_O$ = 3.0 A, $T_J$ = +25°C) | $V_{in}$-$V_O$ | — | 2.2 | 2.5 | — | 2.2 | 2.5 | Vdc |
| Output Noise Voltage<br>(10 Hz $\leqslant$ f $\leqslant$ 100 kHz, $T_J$ = +25°C) | $V_n$ | — | 10 | — | — | 10 | — | µV/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $R_O$ | — | 2.0 | — | — | 2.0 | — | mΩ |
| Short Circuit Current Limit<br>($V_{in}$ = 35 Vdc, $T_J$ = +25°C) | $I_{SC}$ | — | 1.5 | 2.5 | — | 1.5 | 2.5 | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | — | 5.0 | — | — | 5.0 | — | A |
| Average Temperature Coefficient<br>of Output Voltage ($I_O$ = 5.0 mA) | $TCV_O$ | | | | | | | mV/°C |
| MC78T12, MC78T12A | | — | 0.5 | — | — | 0.5 | — | |
| MC78T12AC, MC7812C | | — | 0.5 | — | — | 0.5 | — | |

NOTE 1. $T_{low}$ = −55°C for MC78TXX,A  $T_{high}$ = +150°C for MC78TXX,A
= 0°C for MC78TXXC,AC  = +125°C for MC78TXXC,AC

2. Although power dissipation is internally limited, specifications apply only for $P_O \leqslant P_{max}$
$P_{max}$ = 30 W for K(TO-3) package  $P_{max}$ = 25 W for T(TO-220) package.

3. Line and load regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC78T15, A, AC, C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 23 V, $I_O$ = 3.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1], $P_O \leq P_{max}$ [Note 2], unless otherwise noted).

| Characteristic | Symbol | MC78T15A, AC | | | MC78T15, C | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage<br>(5.0 mA ≤ $I_O$ ≤ 3.0 A, $T_J$ = +25°C)<br>(5.0 mA ≤ $I_O$ ≤ 3.0 A;<br>5.0 mA ≤ $I_O$ ≤ 2.0 A, 17.5 Vdc ≤ $V_{in}$ ≤ 30 Vdc) | $V_O$ | <br>14.7<br>14.4 | <br>15<br>15 | <br>15.3<br>15.6 | <br>14.4<br>14.25 | <br>15<br>15 | <br>15.6<br>15.75 | Vdc |
| Line Regulation (Note 3)<br>(17.6 Vdc ≤ $V_{in}$ ≤ 40 Vdc, $I_O$ = 5.0 mA, $T_J$ = +25°C;<br>17.6 Vdc ≤ $V_{in}$ ≤ 40 Vdc, $I_O$ = 1.0 A, $T_J$ = +25°C;<br>18 Vdc ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 2.0 A;<br>20 Vdc ≤ $V_{in}$ ≤ 26 Vdc, $I_O$ = 3.0 A) | $Reg_{line}$ | — | 7.5 | 22 | — | 7.5 | 55 | mV |
| Load Regulation (Note 3)<br>(5.0 mA ≤ $I_O$ ≤ 3.0 A, $T_J$ = +25°C)<br>(5.0 mA ≤ $I_O$ ≤ 3.0 A) | $Reg_{load}$ | <br>—<br>— | <br>10<br>15 | <br>25<br>50 | <br>—<br>— | <br>10<br>15 | <br>30<br>80 | mV |
| Thermal Regulation<br>(Pulse = 10 ms, P = 20 W, $T_A$ = +25°C) | $Reg_{therm}$ | — | 0.001 | 0.01 | — | 0.002 | 0.03 | %$V_O$/W |
| Quiescent Current<br>(5.0 mA ≤ $I_O$ ≤ 3.0 A, $T_J$ = +25°C)<br>(5.0 mA ≤ $I_O$ ≤ 3.0 A) | $I_B$ | <br>—<br>— | <br>3.5<br>4.0 | <br>5.0<br>6.0 | <br>—<br>— | <br>3.5<br>4.0 | <br>5.0<br>6.0 | mA |
| Quiescent Current Change<br>(17.6 Vdc ≤ $V_{in}$ ≤ 40 Vdc, $I_O$ = 5.0 mA, $T_J$ = +25°C;<br>18 Vdc ≤ $V_{in}$ ≤ 30 Vdc, $I_O$ = 2.0 A;<br>5.0 mA ≤ $I_O$ ≤ 3.0 A) | $\Delta I_B$ | — | 0.1 | 0.5 | — | 0.1 | 0.8 | mA |
| Ripple Rejection<br>(18.5 Vdc ≤ $V_{in}$ ≤ 28.5 Vdc, f = 120 Hz, $I_O$ = 2.0 A) | RR | 60 | 65 | — | 55 | 65 | — | dB |
| Dropout Voltage ($I_O$ = 3.0 A, $T_J$ = +25°C) | $V_{in}-V_O$ | — | 2.2 | 2.5 | — | 2.2 | 2.5 | Vdc |
| Output Noise Voltage<br>(10 Hz ≤ f ≤ 100 kHz, $T_J$ = +25°C) | $V_n$ | — | 10 | — | — | 10 | — | μV/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $R_O$ | — | 2.0 | — | — | 2.0 | — | mΩ |
| Short Circuit Current Limit<br>($V_{in}$ = 40 Vdc, $T_J$ = +25°C) | $I_{SC}$ | — | 1.0 | 2.0 | — | 1.0 | 2.0 | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | — | 5.0 | — | — | 5.0 | — | A |
| Average Temperature Coefficient<br>of Output Voltage ($I_O$ = 5.0 mA)<br>MC78T15, MC78T15A<br>MC78T15AC, MC7815C | $TCV_O$ | <br><br>—<br>— | <br><br>0.6<br>0.6 | <br><br>—<br>— | <br><br>—<br>— | <br><br>0.6<br>0.6 | <br><br>—<br>— | mV/°C |

NOTE 1. $T_{low}$ = −55°C for MC78TXX,A
= 0°C for MC78TXXC,AC

$T_{high}$ = +150°C for MC78TXX,A
= +125°C for MC78TXXC,AC

2. Although power dissipation is internally limited, specifications apply only for $P_O \leq P_{max}$
$P_{max}$ = 30 W for K(TO-3) package
$P_{max}$ = 25 W for T(TO-220) package.

3. Line and load regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC78T18, C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 27 V, $I_O$ = 3.0 A, $T_J$ = $T_{low}$ to $T_{high}$ [Note 1], $P_O \leqslant P_{max}$ [Note 2], unless otherwise noted).

| Characteristic | Symbol | MC78T18, C | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Output Voltage | $V_O$ | | | | Vdc |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A, $T_J$ = +25°C) | | 17.3 | 18 | 18.7 | |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A;<br>5.0 mA $\leqslant I_O \leqslant$ 2.0 A, 20.6 Vdc $\leqslant V_{in} \leqslant$ 33 Vdc) | | 17.1 | 18 | 18.9 | |
| Line Regulation (Note 3)<br>(20.7 Vdc $\leqslant V_{in} \leqslant$ 40 Vdc, $I_O$ = 5.0 mA, $T_J$ = +25°C;<br>20.7 Vdc $\leqslant V_{in} \leqslant$ 40 Vdc, $I_O$ = 1.0 A, $T_J$ = +25°C;<br>21.2 Vdc $\leqslant V_{in} \leqslant$ 33 Vdc, $I_O$ = 2.0 A;<br>24 Vdc $\leqslant V_{in} \leqslant$ 30 Vdc, $I_O$ = 3.0 A) | $Reg_{line}$ | — | 9.0 | 80 | mV |
| Load Regulation (Note 3) | $Reg_{load}$ | | | | mV |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A, $T_J$ = +25°C) | | — | 10 | 30 | |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A) | | — | 15 | 80 | |
| **Thermal Regulation**<br>**(Pulse = 10 ms, P = 20 W, $T_A$ = +25°C)** | $Reg_{therm}$ | — | 0.002 | 0.03 | %$V_O$/W |
| Quiescent Current | $I_B$ | | | | mA |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A, $T_J$ = +25°C) | | — | 3.5 | 5.0 | |
| (5.0 mA $\leqslant I_O \leqslant$ 3.0 A) | | — | 4.0 | 6.0 | |
| Quiescent Current Change<br>(20.7 Vdc $\leqslant V_{in} \leqslant$ 40 Vdc, $I_O$ = 5.0 mA, $T_J$ = +25°C;<br>21.2 Vdc $\leqslant V_{in} \leqslant$ 33 Vdc, $I_O$ = 2.0 A;<br>5.0 mA $\leqslant I_O \leqslant$ 3.0 A) | $\Delta I_B$ | — | 0.1 | 0.8 | mA |
| Ripple Rejection<br>(22 Vdc $\leqslant V_{in} \leqslant$ 32 Vdc, f = 120 Hz, $I_O$ = 2.0 A) | RR | 54 | 64 | — | dB |
| Dropout Voltage ($I_O$ = 3.0 A, $T_J$ = +25°C) | $V_{in}$-$V_O$ | — | 2.2 | 2.5 | Vdc |
| Output Noise Voltage<br>(10 Hz $\leqslant$ f $\leqslant$ 100 kHz, $T_J$ = +25°C) | $V_n$ | — | 10 | — | $\mu$V/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $R_O$ | — | 2.0 | — | m$\Omega$ |
| Short Circuit Current Limit.<br>($V_{in}$ = 40 Vdc, $T_J$ = +25°C) | $I_{SC}$ | — | 1.0 | 2.0 | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | — | 5.0 | — | A |
| Average Temperature Coefficient<br>of Output Voltage ($I_O$ = 5.0 mA) | $TCV_O$ | | | | mV/°C |
| MC78T18 | | — | 0.7 | — | |
| MC78T18C | | — | 0.7 | — | |

NOTE 1. $T_{low}$ = −55°C for MC78TXX,A $\quad$ $T_{high}$ = +150°C for MC78TXX,A
= 0°C for MC78TXXC,AC $\quad$ = +125°C for MC78TXXC,AC

2. Although power dissipation is internally limited, specifications apply only for $P_O \leqslant P_{max}$
$P_{max}$ = 30 W for K(TO-3) package $\quad$ $P_{max}$ = 25 W for T(TO-220) package.

3. Line and load regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC78T24, C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 33 V, $I_O$ = 3.0 A, $T_J = T_{low}$ to $T_{high}$ [Note 1], $P_O \leqslant P_{max}$ [Note 2], unless otherwise noted).

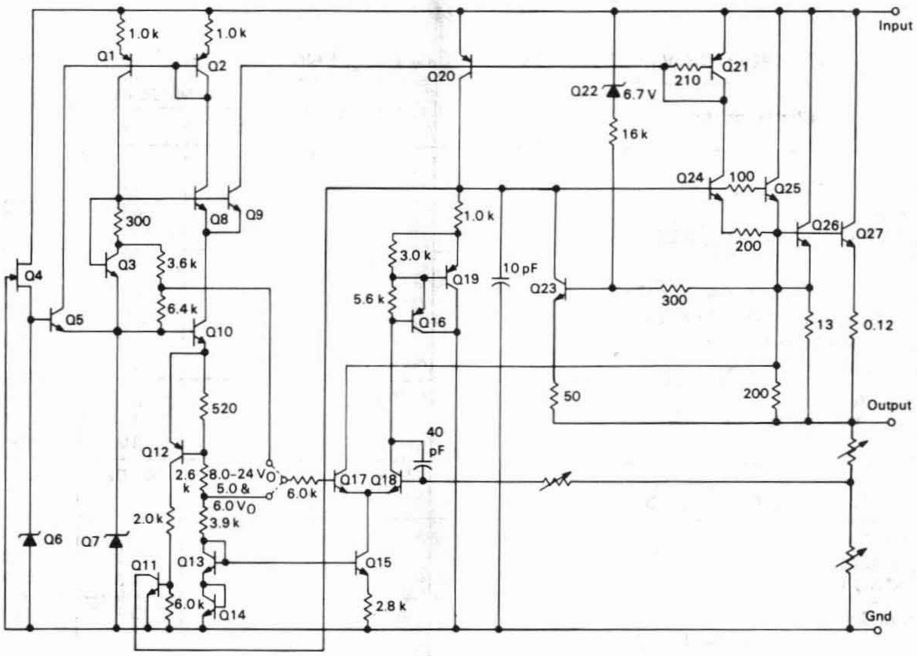
| Characteristic | Symbol | MC78T24, C | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Output Voltage | $V_O$ | | | | Vdc |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A, $T_J$ = +25°C) | | 23 | 24 | 25 | |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A;<br>5.0 mA ≤ $I_O$ ≤ 2.0 A, 27.3 Vdc ≤ $V_{in}$ ≤ 39 Vdc) | | 22.8 | 24 | 25.2 | |
| Line Regulation (Note 3)<br>(27 Vdc ≤ $V_{in}$ ≤ 40 Vdc, $I_O$ = 5.0 mA, $T_J$ = +25°C;<br>27 Vdc ≤ $V_{in}$ ≤ 40 Vdc, $I_O$ = 1.0 A, $T_J$ = +25°C;<br>27.5 Vdc ≤ $V_{in}$ ≤ 39 Vdc, $I_O$ = 2.0 A;<br>30 Vdc ≤ $V_{in}$ ≤ 36 Vdc, $I_O$ = 3.0 A) | $Reg_{line}$ | — | 12 | 90 | mV |
| Load Regulation (Note 3) | $Reg_{load}$ | | | | mV |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A, $T_J$ = +25°C) | | — | 10 | 30 | |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A) | | — | 15 | 80 | |
| Thermal Regulation<br>(Pulse = 10 ms, P = 20 W, $T_A$ = +25°C) | $Reg_{therm}$ | — | 0.002 | 0.03 | %$V_O$/W |
| Quiescent Current | $I_B$ | | | | mA |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A, $T_J$ = +25°C) | | — | 3.5 | 5.0 | |
| (5.0 mA ≤ $I_O$ ≤ 3.0 A) | | — | 4.0 | 6.0 | |
| Quiescent Current Change<br>(27 Vdc ≤ $V_{in}$ ≤ 40 Vdc, $I_O$ = 5.0 mA, $T_J$ = +25°C;<br>27.5 Vdc ≤ $V_{in}$ ≤ 39 Vdc, $I_O$ = 2.0 A;<br>5.0 mA ≤ $I_O$ ≤ 3.0 A) | $\Delta I_B$ | — | 0.1 | 0.8 | mA |
| Ripple Rejection<br>(28 Vdc ≤ $V_{in}$ ≤ 38 Vdc, f = 120 Hz, $I_O$ = 2.0 A) | RR | 51 | 61 | — | dB |
| Dropout Voltage ($I_O$ = 3.0 A, $T_J$ = +25°C) | $V_{in}-V_O$ | — | 2.2 | 2.5 | Vdc |
| Output Noise Voltage<br>(10 Hz ≤ f ≤ 100 kHz, $T_J$ = +25°C) | $V_n$ | — | 10 | — | µV/$V_O$ |
| Output Resistance (f = 1.0 kHz) | $R_O$ | — | 2.0 | — | mΩ |
| Short Circuit Current Limit<br>($V_{in}$ = 40 Vdc, $T_J$ = +25°C) | $I_{SC}$ | — | 1.0 | 2.0 | A |
| Peak Output Current ($T_J$ = +25°C) | $I_{max}$ | — | 5.0 | — | A |
| Average Temperature Coefficient<br>of Output Voltage ($I_O$ = 5.0 mA) | $TCV_O$ | | | | mV/°C |
| MC78T24 | | — | 1.0 | — | |
| MC78T24C | | — | 1.0 | — | |

NOTE 1. $T_{low}$ = −55°C for MC78TXX,A
= 0°C for MC78TXXC,AC
$T_{high}$ = +150°C for MC78TXX,A
= +125°C for MC78TXXC,AC

2. Although power dissipation is internally limited, specifications apply only for $P_O \leqslant P_{max}$
$P_{max}$ = 30 W for K(TO-3) package
$P_{max}$ = 25 W for T(TO-220) package.

3. Line and load regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## SCHEMATIC DIAGRAM


Input
1.0 k
1.0 k
Q1
Q2
Q20
210
Q21
Q22
6.7 V
16 k
Q24
100
Q25
300
Q8
Q9
1.0 k
Q26
Q27
200
Q3
3.6 k
3.0 k
10 pF
Q4
Q19
Q23
300
5.6 k
Q5
6.4 k
Q16
13
0.12
Q10
50
200
Output
520
40 pF
Q12
2.6 k
8.0-24 $V_O$
5.0 & 6.0 $V_O$
6.0 k
Q17
Q18
2.0 k
3.9 k
Q6
Q7
Q11
Q13
Q15
6.0 k
Q14
2.8 k
Gnd

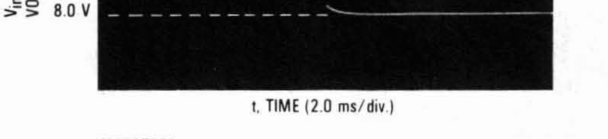
### VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration ($< 100\ \mu s$) and are strictly a function of electrical gain. However, pulse widths of longer duration ($>$ 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

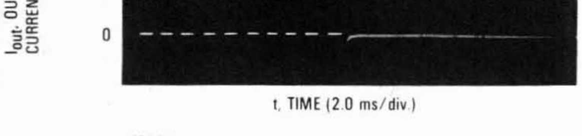
Figure 1 shows the line and thermal regulation response of a typical MC78T05A to a 20 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical MC78T05A to a 20 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②

FIGURE 1 — LINE AND THERMAL REGULATION



MC78T05A
$V_O$ = 5.0 V
$V_{in}$ = 8.0 V → 18 V → 8.0 V ① = $Reg_{line}$ = 2.4 mV
$I_{out}$ = 2.0 A ② = $Reg_{therm}$ = 0.0015%$V_O$/W

FIGURE 2 — LOAD AND THERMAL REGULATION



MC78T05A
$V_O$ = 5.0 V
$V_{in}$ = 15 ① = $Reg_{load}$ = 4.4 mV
$I_{out}$ = 0 A → 2.0 A → 0 A ② = $Reg_{therm}$ = 0.0015%$V_O$/W

FIGURE 3 — TEMPERATURE STABILITY

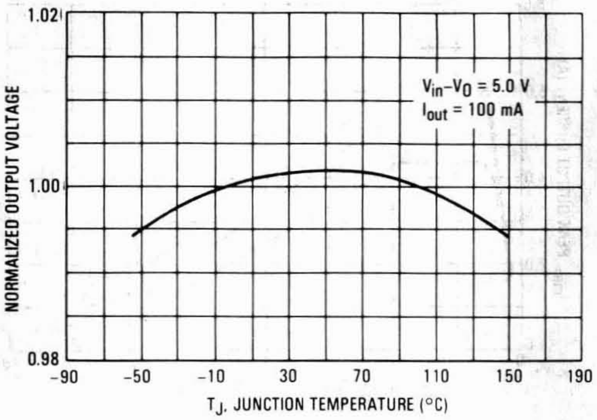


FIGURE 4 — OUTPUT IMPEDANCE

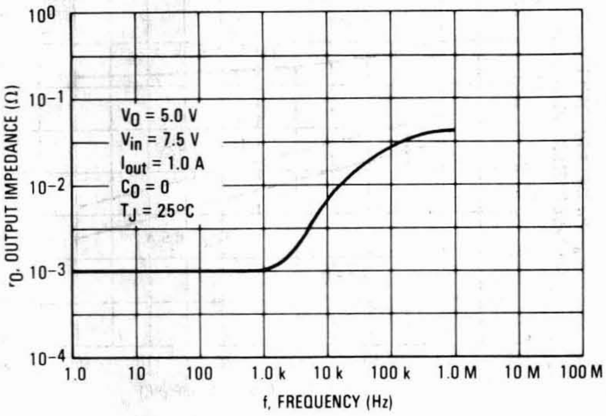


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

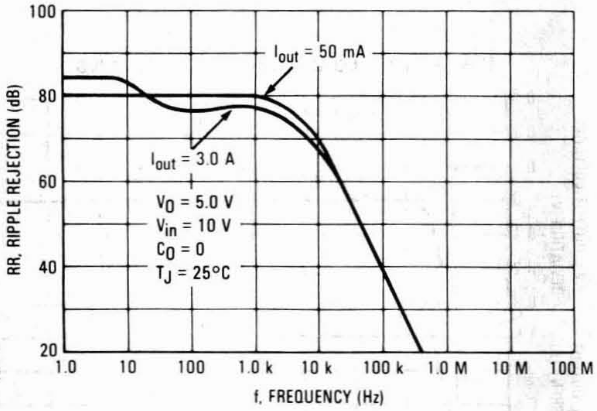


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

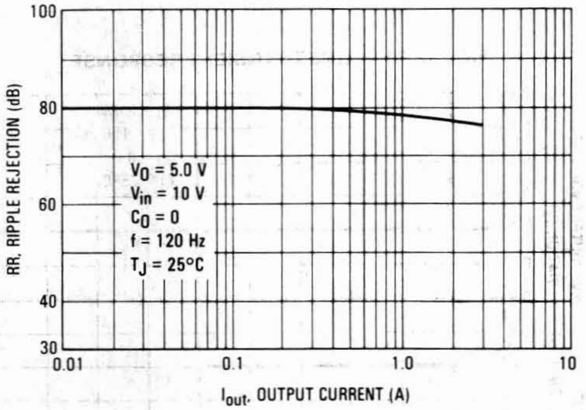


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

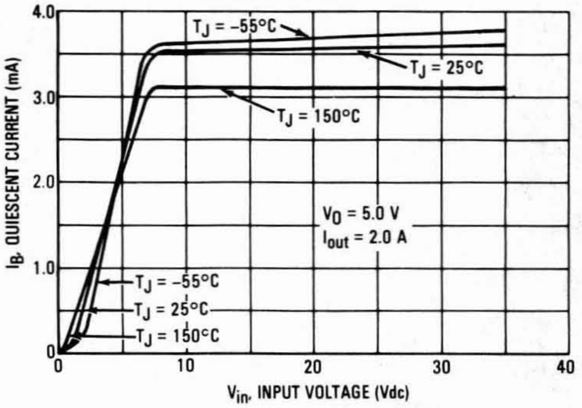


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT

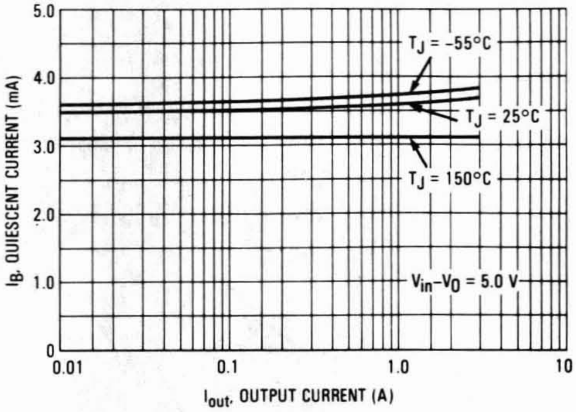


FIGURE 9 — DROPOUT VOLTAGE

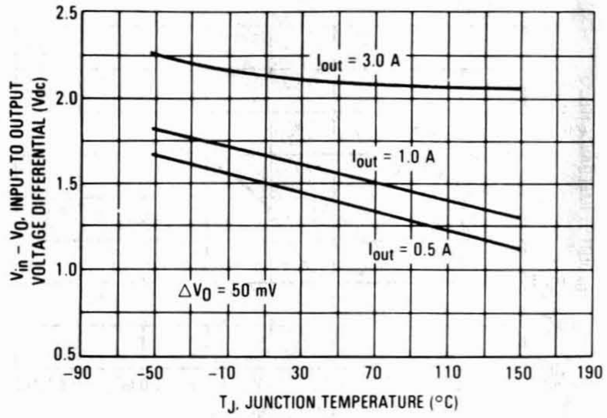


FIGURE 10 — PEAK OUTPUT CURRENT

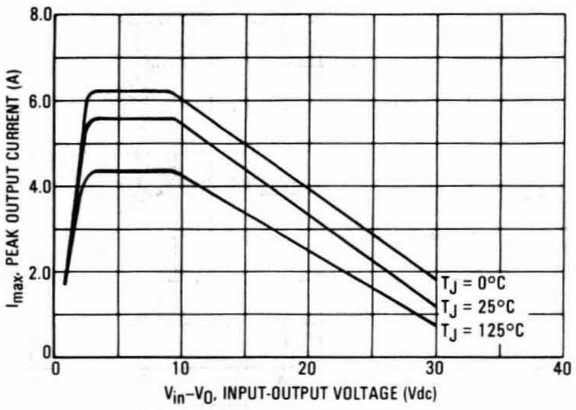


FIGURE 11 — LINE TRANSIENT RESPONSE

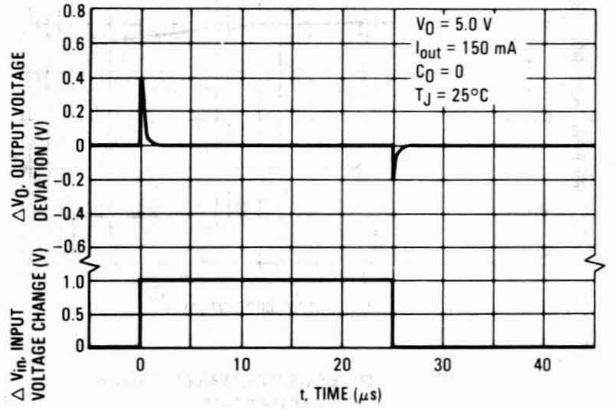


FIGURE 12 — LOAD TRANSIENT RESPONSE

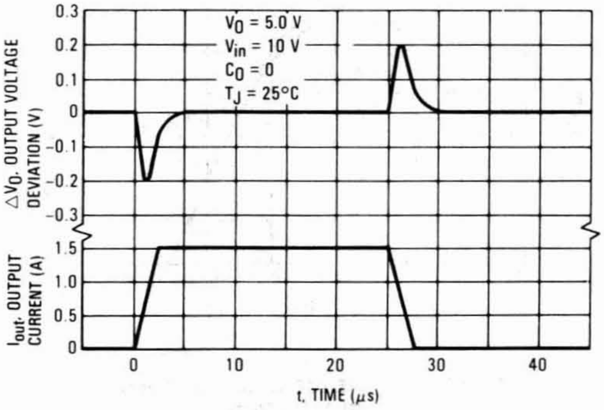


FIGURE 13 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00K, AK

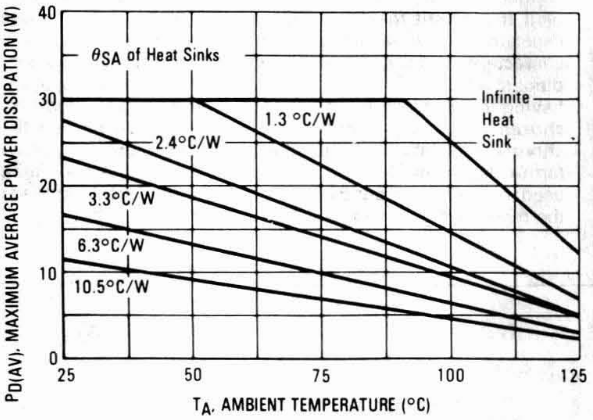


FIGURE 14 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00CK, ACK

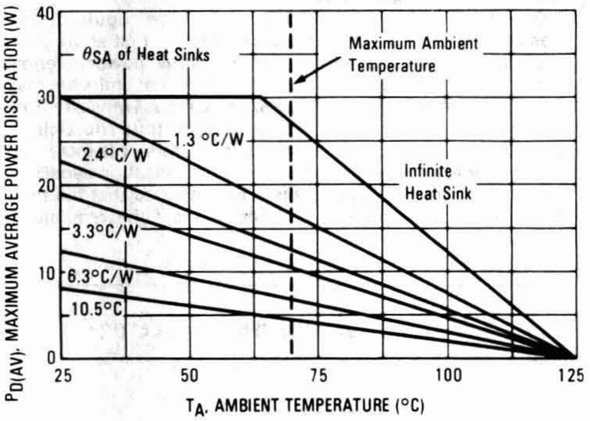
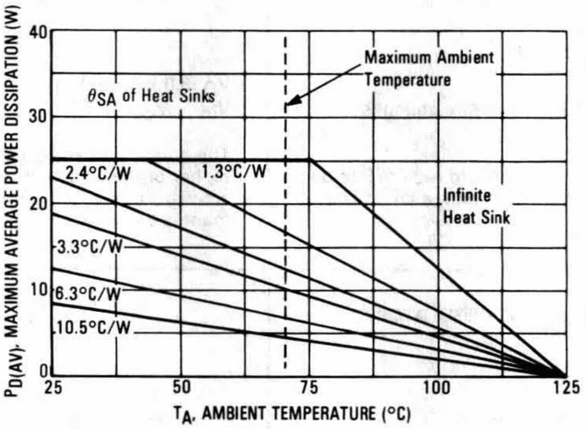


FIGURE 15 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00CT, ACT



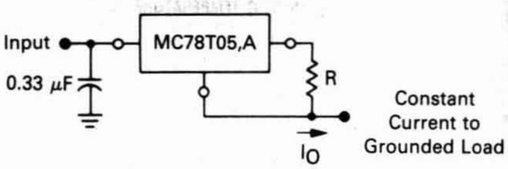
## APPLICATIONS INFORMATION

### DESIGN CONSIDERATIONS

The MC78T00,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

**FIGURE 16 — CURRENT REGULATOR**



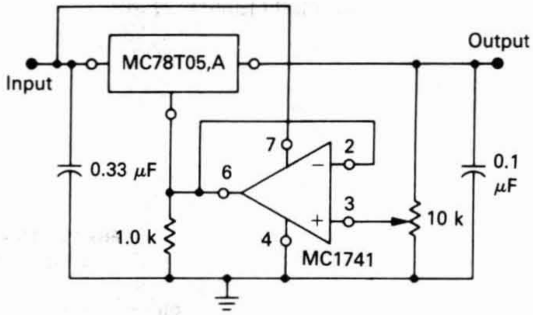
The MC78T05 regulator can also be used as a current source when connected as above. In order to minimize dissipation, the MC78T05 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong 0.7$ mA over line, load and temperature changes
$I_B \cong 3.5$ mA

For example, a 2-ampere current source would require R to be a 2.5 ohm, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

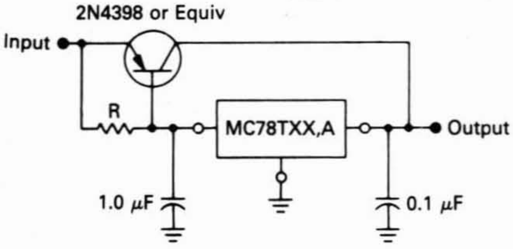
**FIGURE 17 — ADJUSTABLE OUTPUT REGULATOR**



$V_O$, 8.0 V to 20 V
$V_{in} - V_O \geq 2.5$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

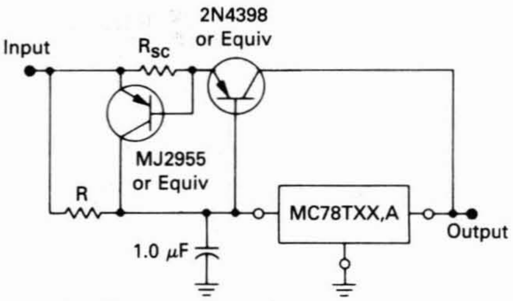
**FIGURE 18 — CURRENT BOOST REGULATOR**



XX = 2 digits of type number indicating voltage.

The MC78T00,A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the $V_{BE}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the $V_{BE}$ of the pass transistor.

**FIGURE 19 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION**



XX = 2 digits of type number indicating voltage.

The circuit of Figure 18 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, $R_{SC}$, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

**MOTOROLA**

# MC7900 Series

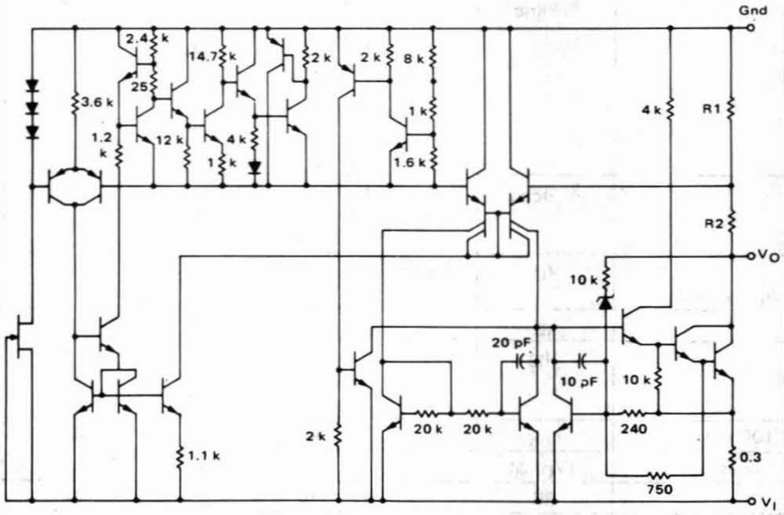
## MC7900 SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC7900 Series of fixed output negative voltage regulators are intended as complements to the popular MC7800 Series devices. These negative regulators are available in the same seven-voltage options as the MC7800 devices. In addition, one extra voltage option commonly employed in MECL systems is also available in the negative MC7900 Series.

Availabe in fixed output voltage options from −5.0 to −24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A and Case 1 (TO-220 and Hermetic TO-3)
- Available in 2% Voltage Tolerance (See Ordering Information)

### SCHEMATIC DIAGRAM

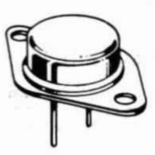


### ORDERING INFORMATION

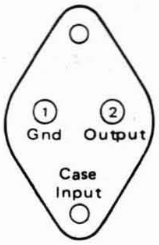
| Device | Output Voltage Tolerance | Junction Temperature Range | Package |
|---|---|---|---|
| MC79XXCK<br>MC79XXACK* | 4%<br>2% | $T_J$ = 0°C to +150°C | Metal Power |
| MC79XXCT<br>MC79XXACT* | 4%<br>2% | $T_J$ = 0°C to +150°C | Plastic Power |

XX indicates nominal voltage.
*2% output voltage tolerance
Available in 5, 12 and 15 volt devices.

## THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

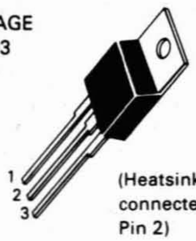


**K SUFFIX**
METAL PACKAGE
CASE 1
(TO-3 TYPE)



(Bottom View)

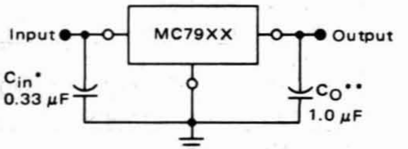
**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220AB



Pin 1. Ground
2. Input
3. Output

(Heatsink surface connected to Pin 2)

### STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_O$ improves stability and transient response.

**DEVICE TYPE/NOMINAL OUTPUT VOLTAGE**

| | | | |
|---|---|---|---|
| MC7905 | 5.0 Volts | MC7912 | 12 Volts |
| MC7905.2 | 5.2 Volts | MC7915 | 15 Volts |
| MC7906 | 6.0 Volts | MC7918 | 18 Volts |
| MC7908 | 8.0 Volts | MC7924 | 24 Volts |

## MC7900 Series MAXIMUM RATINGS ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (−5.0 V ≥ $V_o$ ≥ −18 V) | $V_I$ | −35 | Vdc |
| (24 V) | | −40 | |
| Power Dissipation | | | |
| Plastic Package | | | |
| $T_A$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_A$ = +25°C | $1/R_{\theta JA}$ | 15.4 | mW/°C |
| $T_C$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_C$ = +95°C (See Figure 1) | $1/R_{\theta JC}$ | 200 | mW/°C |
| Metal Package | | | |
| $T_A$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_A$ = +25°C | $1/R_{\theta JA}$ | 22.2 | mW/°C |
| $T_C$ = +25°C | $P_D$ | Internally Limited | Watts |
| Derate above $T_C$ = +65°C | $1/R_{\theta JC}$ | 182 | mW/°C |
| Storage Junction Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature Range | $T_J$ | 0 to +150 | °C |

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Ambient — Plastic Package | $R_{\theta JA}$ | 65 | °C/W |
| — Metal Package | | 45 | |
| Thermal Resistance, Junction to Case — Plastic Package | $R_{\theta JC}$ | 5.0 | °C/W |
| — Metal Package | | 5.5 | |

## MC7905C ELECTRICAL CHARACTERISTICS ($V_I$ = −10 V, $I_O$ = 500 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | −4.8 | −5.0 | −5.2 | Vdc |
| Line Regulation (Note 1) | $Reg_{line}$ | | | | mV |
| ($T_J$ = +25°C, $I_O$ = 100 mA) | | | | | |
| −7.0 Vdc ≥ $V_I$ ≥ −25 Vdc | | — | 7.0 | 50 | |
| −8.0 Vdc ≥ $V_I$ ≥ −12 Vdc. | | — | 2.0 | 25 | |
| ($T_J$ = +25°C, $I_O$ = 500 mA) | | | | | |
| −7.0 Vdc ≥ $V_I$ ≥ −25 Vdc | | — | 35 | 100 | |
| −8.0 Vdc ≥ $V_I$ ≥ −12 Vdc | | — | 8.0 | 50 | |
| Load Regulation ($T_J$ = +25°C) (Note 1) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 11 | 100 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 4.0 | 50 | |
| Output Voltage<br>−7.0 Vdc ≥ $V_I$ ≥ −20 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W | $V_O$ | −4.75 | — | −5.25 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 4.3 | 8.0 | mA |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | mA |
| −7.0 Vdc ≥ $V_I$ ≥ −25 Vdc | | — | — | 1.3 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $e_{on}$ | — | 40 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | — | 20 | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 20 mA, f = 120 Hz) | RR | — | 70 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 1.0 A, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | — | 2.0 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**MC7905AC ELECTRICAL CHARACTERISTICS** ($V_I$ = −10 V, $I_O$ = 500 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | −4.9 | −5.0 | −5.1 | Vdc |
| Line Regulation (Note 1)<br>−8.0 Vdc ≥ $V_I$ ≥ −12 Vdc; $I_O$ = 1.0 A, $T_J$ = 25°C<br>−8.0 Vdc ≥ $V_I$ ≥ −12 Vdc; $I_O$ = 1.0 A<br>−7.5 Vdc ≥ $V_I$ ≥ −25 Vdc; $I_O$ = 500 mA<br>−7.0 Vdc ≥ $V_I$ ≥ −20 Vdc; $I_O$ = 1.0 A, $T_J$ = +25°C | $Reg_{line}$ | <br>—<br>—<br>—<br>— | <br>2.0<br>7.0<br>7.0<br>6.0 | <br>25<br>50<br>50<br>50 | mV |
| Load Regulation (Note 1)<br>5.0 mA ≤ $I_O$ ≤ 1.5 A, $T_J$ = +25°C<br>250 mA ≤ $I_O$ ≤ 750 mA<br>5.0 mA ≤ $I_O$ ≤ 1.0 A | $Reg_{load}$ | <br>—<br>—<br>— | <br>11<br>4.0<br>9.0 | <br>100<br>50<br>100 | mV |
| Output Voltage<br>−7.5 Vdc ≥ $V_I$ ≥ −20 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W | $V_O$ | −4.80 | — | −5.20 | Vdc |
| Input Bias Current | $I_{IB}$ | — | 4.4 | 8.0 | mA |
| Input Bias Current Change<br>−7.5 Vdc ≥ $V_I$ ≥ −25 Vdc<br>5.0 mA ≤ $I_O$ ≤ 1.0 A<br>5.0 mA ≤ $I_O$ ≤ 1.5 A, $T_J$ = 25°C | $\Delta I_{IB}$ | <br>—<br>—<br>— | <br>—<br>—<br>— | <br>1.3<br>0.5<br>0.5 | mA |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $e_{on}$ | — | 40 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | — | 20 | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 20 mA, f = 120 Hz) | RR | — | 70 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 1.0 A, $T_J$ = +25°C | $\|V_I-V_O\|$ | — | 2.0 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |

**MC7905.2C ELECTRICAL CHARACTERISTICS** ($V_I$ = −10 V, $I_O$ = 500 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | −5.0 | −5.2 | −5.4 | Vdc |
| Line Regulation (Note 1)<br>($T_J$ = +25°C, $I_O$ = 100 mA)<br>−7.2 Vdc ≥ $V_I$ ≥ −25 Vdc<br>−8.0 Vdc ≥ $V_I$ ≥ −12 Vdc<br>($T_J$ = +25°C, $I_O$ = 500 mA)<br>−7.2 Vdc ≥ $V_I$ ≥ −25 Vdc<br>−8.0 Vdc ≥ $V_I$ ≥ −12 Vdc | $Reg_{line}$ | <br><br>—<br>—<br><br>—<br>— | <br><br>8.0<br>2.2<br><br>37<br>8.5 | <br><br>52<br>27<br><br>105<br>52 | mV |
| Load Regulation ($T_J$ = +25°C) (Note 1)<br>5.0 mA ≤ $I_O$ ≤ 1.5 A<br>250 mA ≤ $I_O$ ≤ 750 mA | $Reg_{load}$ | <br>—<br>— | <br>12<br>4.5 | <br>105<br>52 | mV |
| Output Voltage<br>−7.2 Vdc ≥ $V_I$ ≥ −20 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W | $V_O$ | −4.95 | — | −5.45 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 4.3 | 8.0 | mA |
| Input Bias Current Change<br>−7.2 Vdc ≥ $V_I$ ≥ −25 Vdc<br>5.0 mA ≤ $I_O$ ≤ 1.5 A | $\Delta I_{IB}$ | <br>—<br>— | <br>—<br>— | <br>1.3<br>0.5 | mA |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $e_{on}$ | — | 42 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | — | 20 | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 20 mA, f = 120 Hz) | RR | — | 68 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 1.0 A, $T_J$ = +25°C | $\|V_I-V_O\|$ | — | 2.0 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**MC7906C ELECTRICAL CHARACTERISTICS** ($V_I$ = −11 V, $I_O$ = 500 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | -5.75 | -6.0 | -6.25 | Vdc |
| Line Regulation (Note 1) | $Reg_{line}$ | | | | mV |
| ($T_J$ = +25°C, $I_O$ = 100 mA) | | | | | |
| −8.0 Vdc ≥ $V_I$ ≥ −25 Vdc | | — | 9.0 | 60 | |
| −9.0 Vdc ≥ $V_I$ ≥ −13 Vdc | | — | 3.0 | 30 | |
| ($T_J$ = +25°C, $I_O$ = 500 mA) | | | | | |
| −8.0 Vdc ≥ $V_I$ ≥ −25 Vdc | | — | 43 | 120 | |
| −9.0 Vdc ≥ $V_I$ ≥ −13 Vdc | | — | 10 | 60 | |
| Load Regulation ($T_J$ = +25°C) (Note 1) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 13 | 120 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 5.0 | 60 | |
| Output Voltage<br>−8.0 Vdc ≥ $V_I$ ≥ −21 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W | $V_O$ | -5.7 | — | -6.3 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 4.3 | 8.0 | mA |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | mA |
| −8.0 Vdc ≥ $V_I$ ≥ −25 Vdc | | — | — | 1.3 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $e_{on}$ | — | 45 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | — | 24 | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 20 mA, f = 120 Hz) | RR | — | 65 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 1.0 A, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | — | 2.0 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | -1.0 | — | mV/°C |

**MC7908C ELECTRICAL CHARACTERISTICS** ($V_I$ = −14 V, $I_O$ = 500 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | -7.7 | -8.0 | -8.3 | Vdc |
| Line Regulation (Note 1) | $Reg_{line}$ | | | | mV |
| ($T_J$ = +25°C, $I_O$ = 100 mA) | | | | | |
| −10.5 Vdc ≥ $V_I$ ≥ −25 Vdc | | — | 12 | 80 | |
| −11 Vdc ≥ $V_I$ ≥ −17 Vdc | | — | 5.0 | 40 | |
| ($T_J$ = +25°C, $I_O$ = 500 mA) | | | | | |
| −10.5 Vdc ≥ $V_I$ ≥ −25 Vdc | | — | 50 | 160 | |
| −11 Vdc ≥ $V_I$ ≥ −17 Vdc | | — | 22 | 80 | |
| Load Regulation ($T_J$ = +25°C) (Note 1) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 26 | 160 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 9.0 | 80 | |
| Output Voltage<br>−10.5 Vdc ≥ $V_I$ ≥ −23 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W | $V_O$ | -7.6 | — | -8.4 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 4.3 | 8.0 | mA |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | mA |
| −10.5 Vdc ≥ $V_I$ ≥ −25 Vdc | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $e_{on}$ | — | 52 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | — | 32 | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 20 mA, f = 120 Hz) | RR | — | 62 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 1.0 A, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | — | 2.0 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | -1.0 | — | mV/°C |

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**MC7912C ELECTRICAL CHARACTERISTICS** ($V_I$ = -19 V, $I_O$ = 500 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | -11.5 | -12 | -12.5 | Vdc |
| Line Regulation (Note 1) | $Reg_{line}$ | | | | mV |
| ($T_J$ = +25°C, $I_O$ = 100 mA) | | | | | |
| -14.5 Vdc ≥ $V_I$ ≥ -30 Vdc | | — | 13 | 120 | |
| -16 Vdc ≥ $V_I$ ≥ -22 Vdc | | — | 6.0 | 60 | |
| ($T_J$ = +25°C, $I_O$ = 500 mA) | | | | | |
| -14.5 Vdc ≥ $V_I$ ≥ -30 Vdc | | — | 55 | 240 | |
| -16 Vdc ≥ $V_I$ ≥ -22 Vdc | | — | 24 | 120 | |
| Load Regulation ($T_J$ = +25°C) (Note 1) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 46 | 240 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 17 | 120 | |
| Output Voltage<br>-14.5 Vdc ≥ $V_I$ ≥ -27 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W | $V_O$ | -11.4 | — | -12.6 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 4.4 | 8.0 | mA |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | mA |
| -14.5 Vdc ≥ $V_I$ ≥ -30 Vdc | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $e_{on}$ | — | 75 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | — | 48 | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 20 mA, f = 120 Hz) | RR | — | 61 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 1.0 A, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | — | 2.0 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | -1.0 | — | mV/°C |

**MC7912AC ELECTRICAL CHARACTERISTICS** ($V_I$ = -19 V, $I_O$ = 500 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | -11.75 | -12 | -12.25 | Vdc |
| Line Regulation (Note 1) | $Reg_{line}$ | | | | mV |
| -16 Vdc ≥ $V_I$ ≥ -22 Vdc; $I_O$ = 1.0 A, $T_J$ = 25°C | | — | 6.0 | 60 | |
| -16 Vdc ≥ $V_I$ ≥ -22 Vdc; $I_O$ = 1.0 A, | | — | 24 | 120 | |
| -14.8 Vdc ≥ $V_I$ ≥ -30 Vdc; $I_O$ = 500 mA | | — | 24 | 120 | |
| -14.5 Vdc ≥ $V_I$ ≥ -27 Vdc; $I_O$ = 1.0 A, $T_J$ = 25°C | | — | 13 | 120 | |
| Load Regulation (Note 1) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A, $T_J$ = 25°C | | — | 46 | 150 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 17 | 75 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 35 | 150 | |
| Output Voltage<br>-14.8 Vdc ≥ $V_I$ ≥ -27 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W | $V_O$ | -11.5 | — | -12.5 | Vdc |
| Input Bias Current | $I_{IB}$ | — | 4.4 | 8.0 | mA |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | mA |
| -15 Vdc ≥ $V_I$ ≥ -30 Vdc | | — | — | 0.8 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | — | 0.5 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A, $T_J$ = 25°C | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $e_{on}$ | — | 75 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | — | 48 | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 20 mA, f = 120 Hz) | RR | — | 61 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 1.0 A, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | — | 2.0 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | -1.0 | — | mV/°C |

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**MC7915C ELECTRICAL CHARACTERISTICS** ($V_I$ = −23 V, $I_O$ = 500 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | −14.4 | −15 | −15.6 | Vdc |
| Line Regulation (Note 1) | $Reg_{line}$ | | | | mV |
| ($T_J$ = +25°C, $I_O$ = 100 mA) | | | | | |
| −17.5 Vdc ≥ $V_I$ ≥ −30 Vdc | | — | 14 | 150 | |
| −20 Vdc ≥ $V_I$ ≥ −26 Vdc | | — | 6.0 | 75 | |
| ($T_J$ = +25°C, $I_O$ = 500 mA) | | | | | |
| −17.5 Vdc ≥ $V_I$ ≥ −30 Vdc | | — | 57 | 300 | |
| −20 Vdc ≥ $V_I$ ≥ −26 Vdc | | — | 27 | 150 | |
| Load Regulation ($T_J$ = +25°C) (Note 1) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 68 | 300 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 25 | 150 | |
| Output Voltage<br>−17.5 Vdc ≥ $V_I$ ≥ −30 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W | $V_O$ | −14.25 | — | −15.75 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 4.4 | 8.0 | mA |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | mA |
| −17.5 Vdc ≥ $V_I$ ≥ −30 Vdc | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $e_{on}$ | — | 90 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | — | 60 | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 20 mA, f = 120 Hz) | RR | — | 60 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 1.0 A, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | — | 2.0 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |

**MC7915AC ELECTRICAL CHARACTERISTICS** ($V_I$ = −23 V, $I_O$ = 500 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | −14.7 | −15 | −15.3 | Vdc |
| Line Regulation (Note 1) | $Reg_{line}$ | | | | mV |
| −20 Vdc ≥ $V_I$ ≥ −26 Vdc; $I_O$ = 1.0 A, $T_J$ = 25°C | | — | 27 | 75 | |
| −20 Vdc ≥ $V_I$ ≥ −26 Vdc; $I_O$ = 1.0 A, | | — | 57 | 150 | |
| −17.9 Vdc ≥ $V_I$ ≥ −30 Vdc; $I_O$ = 500 mA | | — | 57 | 150 | |
| −17.5 Vdc ≥ $V_I$ ≥ −30 Vdc; $I_O$ = 1.0 A, $T_J$ = 25°C | | — | 57 | 150 | |
| Load Regulation (Note 1) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A, $T_J$ = 25°C | | — | 68 | 150 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 25 | 75 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | 40 | 150 | |
| Output Voltage<br>−17.9 Vdc ≥ $V_I$ ≥ −30 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W | $V_O$ | −14.4 | — | −15.6 | Vdc |
| Input Bias Current | $I_{IB}$ | — | 4.4 | 8.0 | mA |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | mA |
| −17.5 Vdc ≥ $V_I$ ≥ −30 Vdc | | — | — | 0.8 | |
| 5.0 mA ≤ $I_O$ ≤ 1.0 A | | — | — | 0.5 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A, $T_J$ = 25°C | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $e_{on}$ | — | 90 | — | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | — | 60 | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 20 mA, f = 120 Hz) | RR | — | 60 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 1.0 A, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | — | 2.0 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**MC7918C ELECTRICAL CHARACTERISTICS** ($V_I$ = -27 V, $I_O$ = 500 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | -17.3 | -18 | -18.7 | Vdc |
| Line Regulation (Note 1) | $Reg_{line}$ | | | | mV |
| ($T_J$ = +25°C, $I_O$ = 100 mA) | | | | | |
| -21 Vdc ≥ $V_I$ ≥ -33 Vdc | | — | 25 | 180 | |
| -24 Vdc ≥ $V_I$ ≥ -30 Vdc | | — | 10 | 90 | |
| ($T_J$ = +25°C, $I_O$ = 500 mA) | | | | | |
| -21 Vdc ≥ $V_I$ ≥ -33 Vdc | | — | 90 | 360 | |
| -24 Vdc ≥ $V_I$ ≥ -30 Vdc | | — | 50 | 180 | |
| Load Regulation ($T_J$ = +25°C) (Note 1) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 110 | 360 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 55 | 180 | |
| Output Voltage<br>-21 Vdc ≥ $V_I$ ≥ -33 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W | $V_O$ | -17.1 | — | -18.9 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 4.5 | 8.0 | mA |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | mA |
| -21 Vdc ≥ $V_I$ ≥ -33 Vdc | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $e_{on}$ | — | 110 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | — | 72 | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 20 mA, f = 120 Hz) | RR | — | 59 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 1.0 A, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | — | 2.0 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | -1.0 | — | mV/°C |

**MC7924C ELECTRICAL CHARACTERISTICS** ($V_I$ = -33 V, $I_O$ = 500 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | -23 | -24 | -25 | Vdc |
| Line Regulation (Note 1) | $Reg_{line}$ | | | | mV |
| ($T_J$ = +25°C, $I_O$ = 100 mA) | | | | | |
| -27 Vdc ≥ $V_I$ ≥ -38 Vdc | | — | 31 | 240 | |
| -30 Vdc ≥ $V_I$ ≥ -36 Vdc | | — | 14 | 120 | |
| ($T_J$ = +25°C, $I_O$ = 500 mA) | | | | | |
| -27 Vdc ≥ $V_I$ ≥ -38 Vdc | | — | 118 | 480 | |
| -30 Vdc ≥ $V_I$ ≥ -36 Vdc | | — | 70 | 240 | |
| Load Regulation ($T_J$ = +25°C) (Note 1) | $Reg_{load}$ | | | | mV |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | 150 | 480 | |
| 250 mA ≤ $I_O$ ≤ 750 mA | | — | 85 | 240 | |
| Output Voltage<br>-27 Vdc ≥ $V_I$ ≥ -38 Vdc, 5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W | $V_O$ | -22.8 | — | -25.2 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 4.6 | 8.0 | mA |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | mA |
| -27 Vdc ≥ $V_I$ ≥ -38 Vdc | | — | — | 1.0 | |
| 5.0 mA ≤ $I_O$ ≤ 1.5 A | | — | — | 0.5 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $e_{on}$ | — | 170 | — | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | — | — | 96 | mV/1.0 k Hrs |
| Ripple Rejection ($I_O$ = 20 mA, f = 120 Hz) | RR | — | 56 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 1.0 A, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | — | 2.0 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | -1.0 | — | mV/°C |

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## TYPICAL CHARACTERISTICS

($T_A$ = +25°C unless otherwise noted.)

**FIGURE 1 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220)**

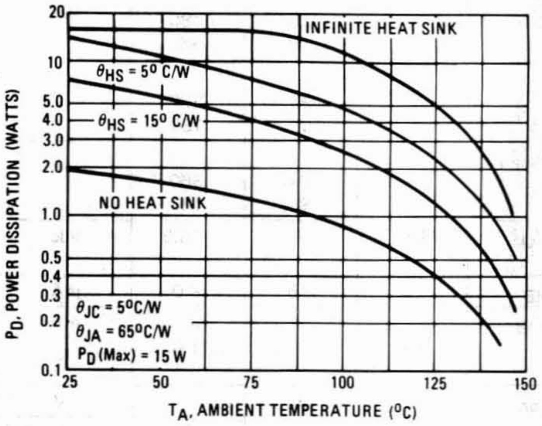


**FIGURE 2 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3)**

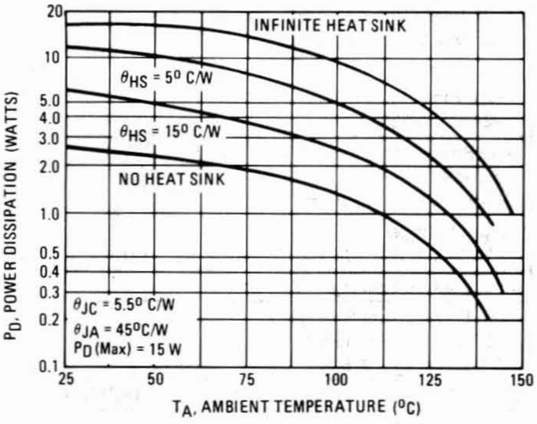


**FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE**

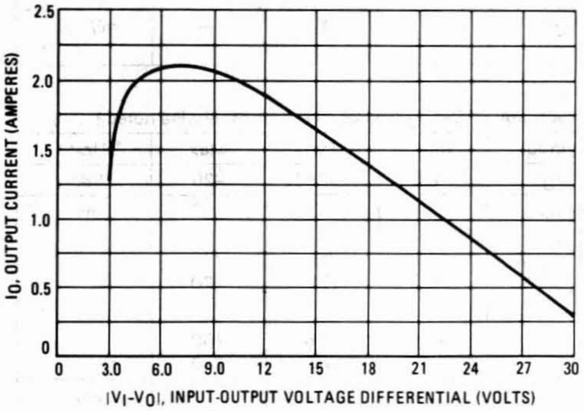


**FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY**

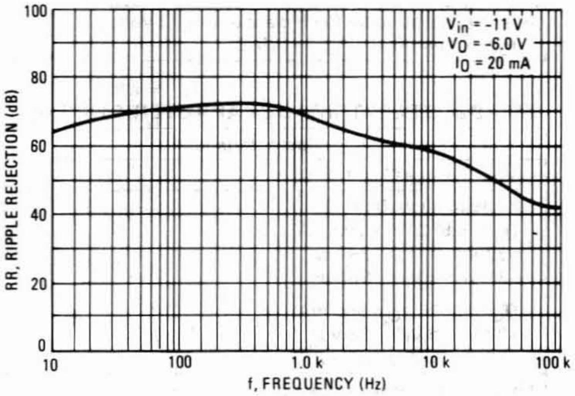


**FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES**

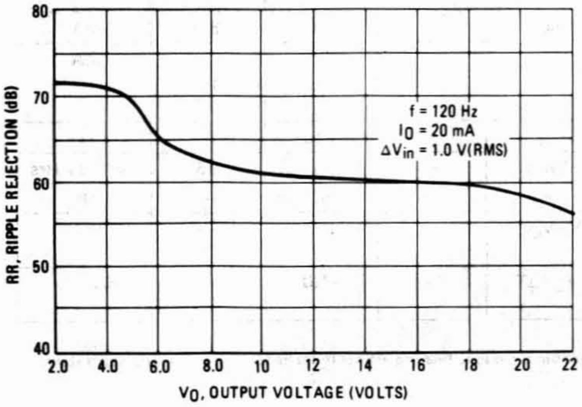
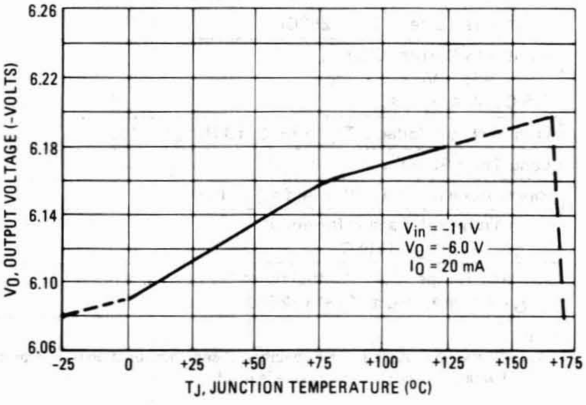
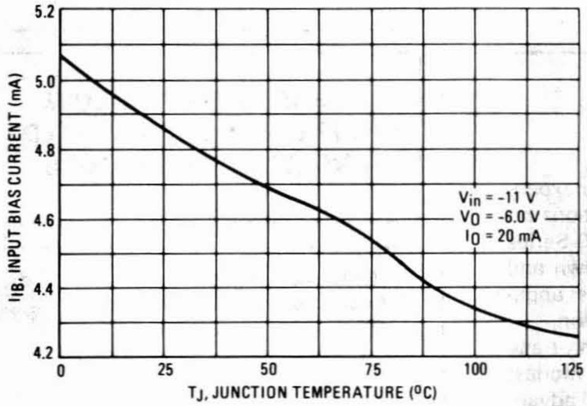


**FIGURE 6 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE**



## TYPICAL CHARACTERISTICS (continued)

### FIGURE 7 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



### DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

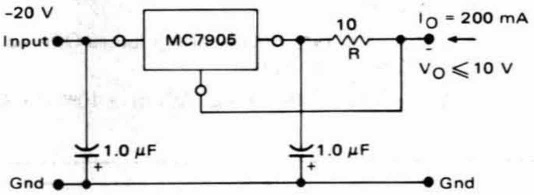
## APPLICATIONS INFORMATION

**Design Considerations**

The MC7900 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

### FIGURE 8 – CURRENT REGULATOR



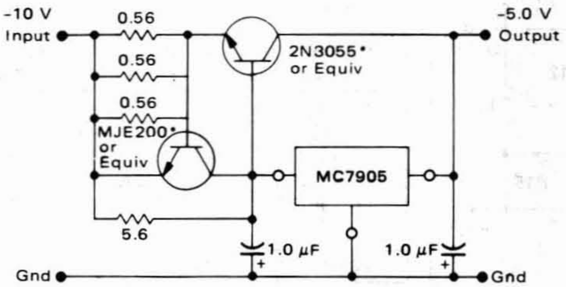
The MC7905, -5.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 5.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

### FIGURE 9 – CURRENT BOOST REGULATOR

(-5.0 V @ 4.0 A, with 5.0 A current limiting)

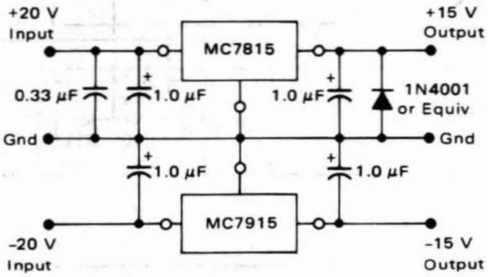


*Mounted on common heat sink, Motorola MS-10 or equivalent.

When a boost transistor is used, short-circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/$R_{SC}$. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

### FIGURE 10 – OPERATIONAL AMPLIFIER SUPPLY

(±15 V @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems whenever the output of the positive regulator (MC7815) is drawn below ground with an output current greater than 200 mA.

# MC79L00C,AC series

## THREE-TERMINAL LOW CURRENT NEGATIVE VOLTAGE REGULATORS

The MC79L00 Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to 100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

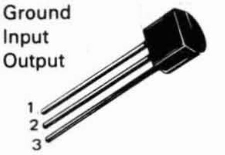
The MC79L00 devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

## THREE-TERMINAL LOW CURRENT NEGATIVE FIXED VOLTAGE REGULATORS

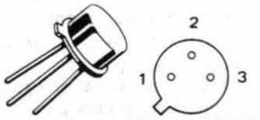
**P SUFFIX**
CASE 29-02
TO-226AA
(TO-92)

Pin 1. Ground
2. Input
3. Output



**G SUFFIX**
CASE 79-03
(TO-39)

Pin 1. Ground
2. Output
3. Input



(Bottom View)
(Case Connected To Pin 3)

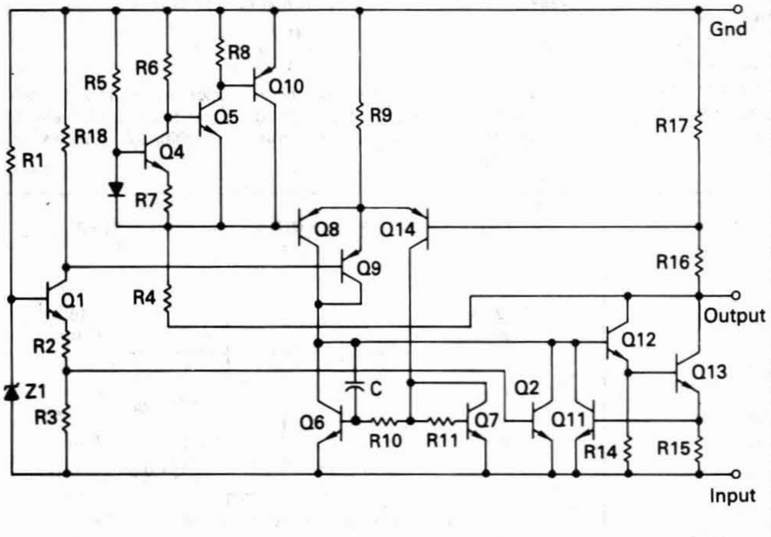
**D SUFFIX***
PLASTIC PACKAGE
CASE 751-01
SOP-8

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

***Surface Mount pin-out is different than standard package pin-out for this device. Please refer to Chapter 7 for details.**

| Device No. ±10% | Device No. ±5% | Nominal Voltage |
|---|---|---|
| MC79L05C | MC79L05AC | −5.0 |
| MC79L12C | MC79L12AC | −12 |
| MC79L15C | MC79L15AC | −15 |
| MC79L18C | MC79L18AC | −18 |
| MC79L24C | MC79L24AC | −24 |

### REPRESENTATIVE CIRCUIT SCHEMATIC



**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC79LXXACD | $T_J$ = 0°C to + 125°C | SOP-8 |
| MC79LXXACG | | Metal Can |
| MC79LXXACP | | Plastic Power |
| MC79LXXCD | | SOP-8 |
| MC79LXXCG | | Metal Can |
| MC79LXXCP | | Plastic Power |

XX indicates nominal voltage

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (−5 V)<br>(−12, −15, −18 V)<br>(−24 V) | $V_I$ | −30<br>−35<br>−40 | Vdc |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature Range | $T_J$ | 0 to +150 | °C |

**MC79L05C, AC Series ELECTRICAL CHARACTERISTICS** ($V_I$ = -10 V, $I_O$ = 40 mA, $C_I$ = 0.33 µF, $C_O$ = 0.1 µF, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | MC79L05C | | | MC79L05AC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | -4.6 | -5.0 | -5.4 | -4.8 | -5.0 | -5.2 | Vdc |
| Input Regulation ($T_J$ = +25°C) | $Reg_{line}$ | | | | | | | mV |
| -7.0 Vdc ≥ $V_I$ ≥ -20 Vdc | | – | – | 200 | – | – | 150 | |
| -8.0 Vdc ≥ $V_I$ ≥ -20 Vdc | | – | – | 150 | – | – | 100 | |
| Load Regulation | $Reg_{load}$ | | | | | | | mV |
| $T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 100 mA | | – | – | 60 | – | – | 60 | |
| 1.0 mA ≤ $I_O$ ≤ 40 mA | | – | – | 30 | – | – | 30 | |
| Output Voltage | $V_O$ | | | | | | | Vdc |
| -7.0 Vdc ≥ $V_I$ ≥ -20 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA | | -4.5 | – | -5.5 | -4.75 | – | -5.25 | |
| $V_I$ = -10 Vdc, 1.0 mA ≤ $I_O$ ≤ 70 mA | | -4.5 | – | -5.5 | -4.75 | – | -5.25 | |
| Input Bias Current | $I_{IB}$ | | | | | | | mA |
| ($T_J$ = +25°C) | | – | – | 6.0 | – | – | 6.0 | |
| ($T_J$ = +125°C) | | – | – | 5.5 | – | – | 5.5 | |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | | | | mA |
| -8.0 Vdc ≥ $V_I$ ≥ -20 Vdc | | – | – | 1.5 | – | – | 1.5 | |
| 1.0 mA ≤ $I_O$ ≤ 40 mA | | – | – | 0.2 | – | – | 0.1 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | – | 40 | – | – | 40 | – | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | – | 12 | – | – | 12 | – | mV/1.0 k Hrs. |
| Ripple Rejection (-8.0 ≥ $V_I$ ≥ 18 Vdc, f = 120 kHz, $T_J$ = 25°C) | RR | 40 | 49 | – | 41 | 49 | – | dB |
| Input-Output Voltage Differential $I_O$ = 40 mA, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | – | 1.7 | – | – | 1.7 | – | Vdc |

**MC79L12C, AC ELECTRICAL CHARACTERISTICS** ($V_I$ = -19 V, $I_O$ = 40 mA, $C_I$ = 0.33 µF, $C_O$ = 0.1 µF, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | MC79L12C | | | MC79L12AC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | -11.1 | -12 | -12.9 | -11.5 | -12 | -12.5 | Vdc |
| Input Regulation ($T_J$ = +25°C) | $Reg_{line}$ | | | | | | | mV |
| -14.5 Vdc ≥ $V_I$ ≥ -27 Vdc | | – | – | 250 | – | – | 250 | |
| -16 Vdc ≥ $V_I$ ≥ -27 Vdc | | – | – | 200 | – | – | 200 | |
| Load Regulation | $Reg_{load}$ | | | | | | | mV |
| $T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 100 mA | | – | – | 100 | – | – | 100 | |
| 1.0 mA ≤ $I_O$ ≤ 40 mA | | – | – | 50 | – | – | 50 | |
| Output Voltage | $V_O$ | | | | | | | Vdc |
| -14.5 Vdc ≥ $V_I$ ≥ -27 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA | | -10.8 | – | -13.2 | -11.4 | – | -12.6 | |
| $V_I$ = -19 Vdc, 1.0 mA ≤ $I_O$ ≤ 70 mA | | -10.8 | – | -13.2 | -11.4 | – | -12.6 | |
| Input Bias Current | $I_{IB}$ | | | | | | | mA |
| ($T_J$ = +25°C) | | – | – | 6.5 | – | – | 6.5 | |
| ($T_J$ = +125°C) | | – | – | 6.0 | – | – | 6.0 | |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | | | | mA |
| -16 Vdc ≥ $V_I$ ≥ -27 Vdc | | – | – | 1.5 | – | – | 1.5 | |
| 1.0 mA ≤ $I_O$ ≤ 40 mA | | – | – | 0.2 | – | – | 0.1 | |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | – | 80 | – | – | 80 | – | µV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | – | 24 | – | – | 24 | – | mV/1.0 k Hrs. |
| Ripple Rejection (-15 ≤ $V_I$ ≤ -25 Vdc, f = 120 Hz, $T_J$ = +25°C) | RR | 36 | 42 | – | 37 | 42 | – | dB |
| Input-Output Voltage Differential $I_O$ = 40 mA, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | – | 1.7 | – | – | 1.7 | – | Vdc |

4

**MC79L15C, AC ELECTRICAL CHARACTERISTICS** ($V_I$ = -23 V, $I_O$ = 40 mA, $C_I$ = 0.33 μF, $C_O$ = 0.1 μF, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | MC79L15C |  |  | MC79L15AC |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | -13.8 | -15 | -16.2 | -14.4 | -15 | -15.6 | Vdc |
| Input Regulation ($T_J$ = +25°C) | $Reg_{line}$ |  |  |  |  |  |  | mV |
| -17.5 Vdc ≥ $V_I$ ≥ -30 Vdc |  | – | – | 300 | – | – | 300 |  |
| -20 Vdc ≥ $V_I$ ≥ -30 Vdc |  | – | – | 250 | – | – | 250 |  |
| Load Regulation | $Reg_{load}$ |  |  |  |  |  |  | mV |
| $T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 100 mA |  | – | – | 150 | – | – | 150 |  |
| 1.0 mA ≤ $I_O$ ≤ 40 mA |  | – | – | 75 | – | – | 75 |  |
| Output Voltage | $V_O$ |  |  |  |  |  |  | Vdc |
| -17.5 Vdc ≥ $V_I$ ≥ -30 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA |  | -13.5 | – | -16.5 | -14.25 | – | -15.75 |  |
| $V_I$ = -23 Vdc, 1.0 mA ≤ $I_O$ ≤ 70 mA |  | -13.5 | – | -16.5 | -14.25 | – | -15.75 |  |
| Input Bias Current | $I_{IB}$ |  |  |  |  |  |  | mA |
| ($T_J$ = +25°C) |  | – | – | 6.5 | – | – | 6.5 |  |
| ($T_J$ = +125°C) |  | – | – | 6.0 | – | – | 6.0 |  |
| Input Bias Current Change | $\Delta I_{IB}$ |  |  |  |  |  |  | mA |
| -20 Vdc ≥ $V_I$ ≥ -30 Vdc |  | – | – | 1.5 | – | – | 1.5 |  |
| 1.0 mA ≤ $I_O$ ≤ 40 mA |  | – | – | 0.2 | – | – | 0.1 |  |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | – | 90 | – | – | 90 | – | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | – | 30 | – | – | 30 | – | mV/1.0 k Hrs. |
| Ripple Rejection (-18.5 ≤ $V_I$ ≤ -28.5 Vdc, f = 120 Hz) | RR | 33 | 39 | – | 34 | 39 | – | dB |
| Input-Output Voltage Differential $I_O$ = 40 mA, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | – | 1.7 | – | – | 1.7 | – | Vdc |

**MC79L18C, AC ELECTRICAL CHARACTERISTICS** ($V_I$ = -27 V, $I_O$ = 40 mA, $C_I$ = 0.33 μF, $C_O$ = 0.1 μF, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | MC79L18C |  |  | MC79L18AC |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ($T_J$ = +25°C) | $V_O$ | -16.6 | -18 | -19.4 | -17.3 | -18 | -18.7 | Vdc |
| Input Regulation ($T_J$ = +25°C) | $Reg_{line}$ |  |  |  |  |  |  | mV |
| -20.7 Vdc ≥ $V_I$ ≥ -33 Vdc |  | – | – | – | – | – | 325 |  |
| -21.4 Vdc ≥ $V_I$ ≥ -33 Vdc |  | – | – | 325 | – | – | – |  |
| -22 Vdc ≥ $V_I$ ≥ -33 Vdc |  | – | – | 275 | – | – | – |  |
| -21 Vdc ≥ $V_I$ ≥ -33 Vdc |  | – | – | – | – | – | 275 |  |
| Load Regulation | $Reg_{load}$ |  |  |  |  |  |  | mV |
| $T_J$ = +25°C, 1.0 mA ≤ $I_O$ ≤ 100 mA |  | – | – | 170 | – | – | 170 |  |
| 1.0 mA ≤ $I_O$ ≤ 40 mA |  | – | – | 85 | – | – | 85 |  |
| Output Voltage | $V_O$ |  |  |  |  |  |  | Vdc |
| -20.7 Vdc ≥ $V_I$ ≥ -33 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA |  | – | – | – | -17.1 | – | -18.9 |  |
| -21.4 Vdc ≥ $V_I$ ≥ -33 Vdc, 1.0 mA ≤ $I_O$ ≤ 40 mA |  | -16.2 | – | -19.8 | – | – | – |  |
| $V_I$ = -27 Vdc, 1.0 mA ≤ $I_O$ ≤ 70 mA |  | -16.2 | – | -19.8 | -17.1 | – | -18.9 |  |
| Input Bias Current | $I_{IB}$ |  |  |  |  |  |  | mA |
| ($T_J$ = +25°C) |  | – | – | 6.5 | – | – | 6.5 |  |
| ($T_J$ = +125°C) |  | – | – | 6.0 | – | – | 6.0 |  |
| Input Bias Current Change | $\Delta I_{IB}$ |  |  |  |  |  |  | mA |
| -21 Vdc ≥ $V_I$ ≥ -33 Vdc |  | – | – | – | – | – | 1.5 |  |
| -27 Vdc ≥ $V_I$ ≥ -33 Vdc |  | – | – | 1.5 | – | – | – |  |
| 1.0 mA ≤ $I_O$ ≤ 40 mA |  | – | – | 0.2 | – | – | 0.1 |  |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | – | 150 | – | – | 150 | – | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | – | 45 | – | – | 45 | – | mV/1.0 k Hrs. |
| Ripple Rejection (-23 ≤ $V_I$ ≤ -33 Vdc, f = 120 Hz, $T_J$ = +25°C) | RR | 32 | 46 | – | 33 | 48 | – | dB |
| Input-Output Voltage Differential $I_O$ = 40 mA, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | – | 1.7 | – | – | 1.7 | – | Vdc |

**MC79L24C, AC ELECTRICAL CHARACTERISTICS** ($V_I = -33$ V, $I_O = 40$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, $0^\circ C < T_J < +125^\circ C$ unless otherwise noted.)

| Characteristic | Symbol | MC79L24C | | | MC79L24AC | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($T_J = +25^\circ C$) | $V_O$ | -22.1 | -24 | -25.9 | -23 | -24 | -25 | Vdc |
| Input Regulation ($T_J = +25^\circ C$) | $Reg_{line}$ | | | | | | | mV |
| $-27$ Vdc $\geq V_I \geq -38$ V | | – | – | – | – | – | 350 | |
| $-27.5$ Vdc $\geq V_I \geq -38$ Vdc | | – | – | 350 | – | – | – | |
| $-28$ Vdc $\geq V_I \geq -38$ Vdc | | – | – | 300 | – | – | 300 | |
| Load Regulation | $Reg_{load}$ | | | | | | | mV |
| $T_J = +25^\circ C$, 1.0 mA $\leq I_O \leq$ 100 mA | | – | – | 200 | – | – | 200 | |
| 1.0 mA $\leq I_O \leq$ 40 mA | | – | – | 100 | – | – | 100 | |
| Output Voltage | $V_O$ | | | | | | | Vdc |
| $-27$ Vdc $\geq V_I \geq -38$ V, 1.0 mA $\leq I_O \leq$ 40 mA | | – | – | – | -22.8 | – | -25.2 | |
| $-28$ Vdc $\geq V_I \geq -38$ Vdc, 1.0 mA $\leq I_O \leq$ 40 mA | | -21.4 | – | -26.4 | – | – | – | |
| $V_I = -33$ Vdc, 1.0 mA $\leq I_O \leq$ 70 mA | | -21.4 | – | -26.4 | -22.8 | – | -25.2 | |
| Input Bias Current | $I_{IB}$ | | | | | | | mA |
| ($T_J = +25^\circ C$) | | – | – | 6.5 | – | – | 6.5 | |
| ($T_J = +125^\circ C$) | | – | – | 6.0 | – | – | 6.0 | |
| Input Bias Current Change | $\Delta I_{IB}$ | | | | | | | mA |
| $-28$ Vdc $\geq V_I \geq -38$ Vdc | | – | – | 1.5 | – | – | 1.5 | |
| 1.0 mA $\leq I_O \leq$ 40 mA | | – | – | 0.2 | – | – | 0.1 | |
| Output Noise Voltage ($T_A = +25^\circ C$, 10 Hz $\leq f \leq$ 100 kHz) | $V_n$ | – | 200 | – | – | 200 | – | μV |
| Long-Term Stability | $\Delta V_O/\Delta t$ | – | 56 | – | – | 56 | – | mV/1.0 k Hrs. |
| Ripple Rejection ($-29 \leq V_I \leq -35$ Vdc, f = 120 Hz, $T_J = 25^\circ C$) | RR | 30 | 43 | – | 31 | 47 | – | dB |
| Input-Output Voltage Differential $I_O = 40$ mA, $T_J = +25^\circ C$ | $\lvert V_I - V_O \rvert$ | – | 1.7 | – | – | 1.7 | – | Vdc |

## APPLICATIONS INFORMATION

### Design Considerations

The MC79L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

**FIGURE 1 — POSITIVE AND NEGATIVE REGULATOR**

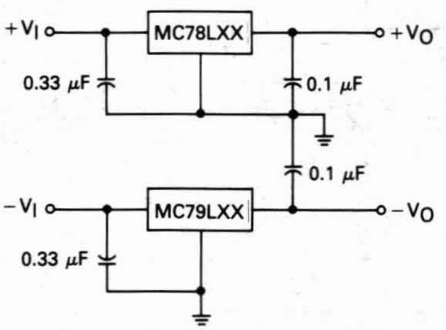
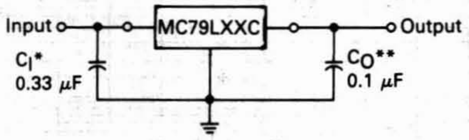


**FIGURE 2 — STANDARD APPLICATION**



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = $C_I$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_O$ improves stability and transient response.

## TYPICAL CHARACTERISTICS

($T_A$ = +25°C unless otherwise noted.)

FIGURE 3 — DROPOUT CHARACTERISTICS

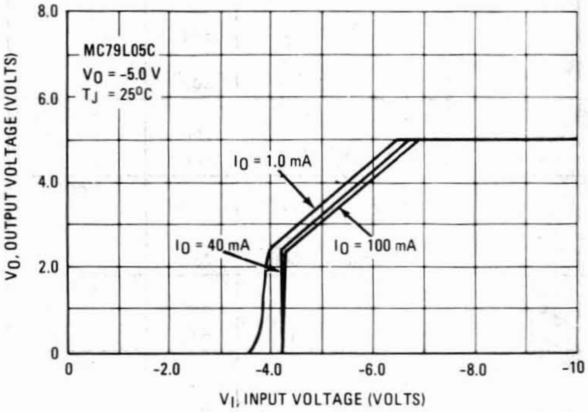


FIGURE 4 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

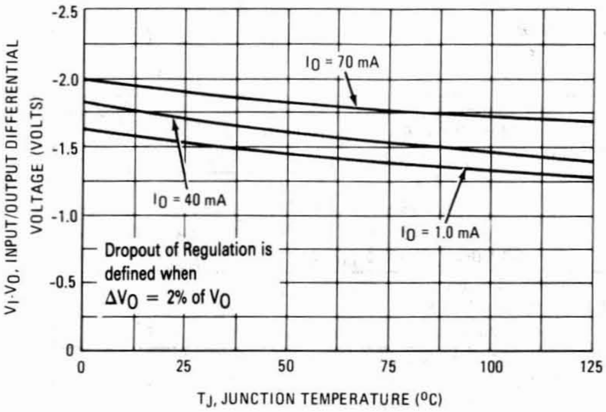


FIGURE 5 — INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

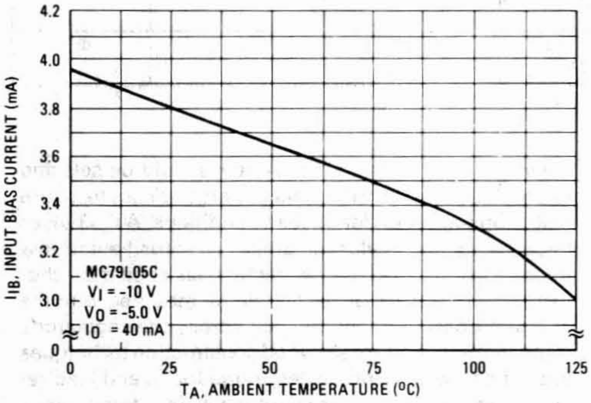


FIGURE 6 — INPUT BIAS CURRENT versus INPUT VOLTAGE

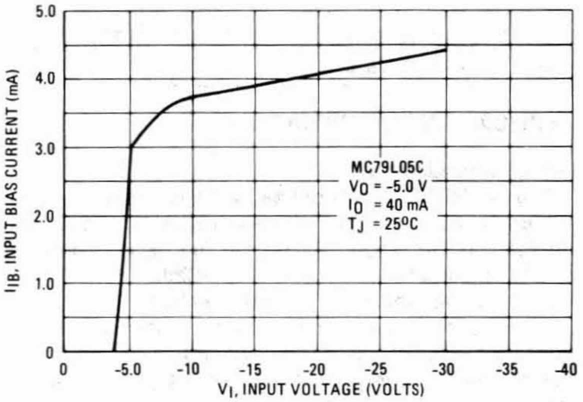


FIGURE 7 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-92 Type Package

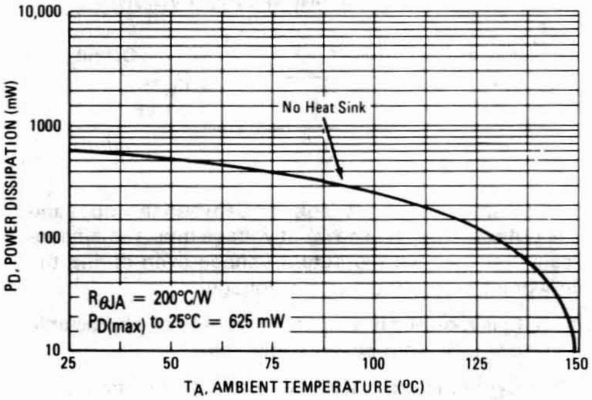
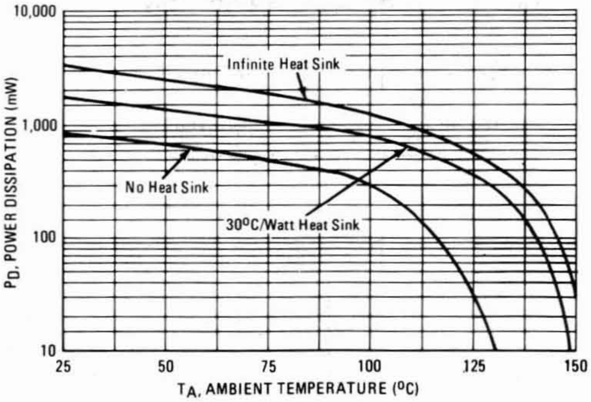


FIGURE 8 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-39 Type Package



**MOTOROLA**

# MC79M00 Series

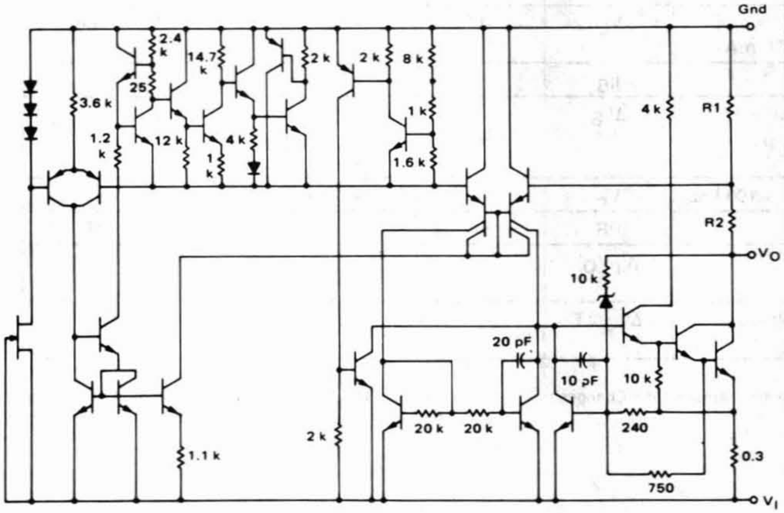
## THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC79M00 Series of fixed output negative voltage regulators are intended as complements to the popular MC78M00 Series devices.

Available in fixed output voltage options of −5.0, −12 and −15 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 0.5 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A (TO-220AB)

### EQUIVALENT SCHEMATIC DIAGRAM



### ORDERING INFORMATION

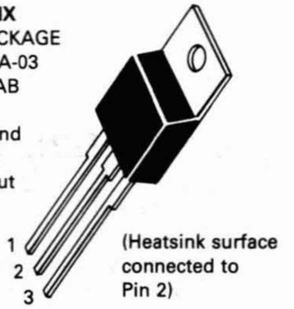
| Device | Output Voltage | Operating Junction Temperature Range | Package |
|---|---|---|---|
| MC79M05CDT | −5.0 Volts | 0°C to +125°C | D-PAK |
| MC79M05CT | | | PLASTIC POWER |
| MC79M12CDT | −12 Volts | | D-PAK |
| MC79M12CT | | | PLASTIC POWER |
| MC79M15CDT | −15 Volts | | D-PAK |
| MC79M15CT | | | PLASTIC POWER |

## THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

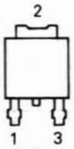
### SILICON MONOLITHIC INTEGRATED CIRCUITS

**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220AB

Pin 1. Ground
2. Input
3. Output

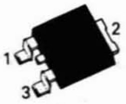


(Heatsink surface connected to Pin 2)



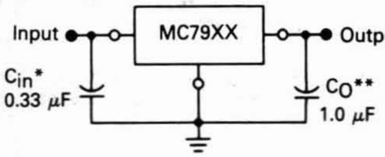
(Heatsink surface is Pin 2)

Pin 1. Input
2. Ground
3. Output



**DT SUFFIX**
PLASTIC PACKAGE
CASE 369A-01
D-PAK

### STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.1 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_O$ improves stability and transient response.

**MC79MXX Series MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage | $V_I$ | −35 | Vdc |
| Power Dissipation<br>Plastic Package<br>$T_A$ = +25°C<br>Derate above $T_A$ = +25°C<br>$T_C$ = +25°C<br>Derate above $T_C$ = +95°C | <br><br>$P_D$<br>$1/R_{\theta JA}$<br>$P_D$<br>$1/R_{\theta JC}$ | <br><br>Internally Limited<br>14.2<br>Internally Limited<br>200 | <br><br>Watts<br>mW/°C<br>Watts<br>mW/°C |
| Storage Junction Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature Range | $T_J$ | 0 to +150 | °C |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 65 | °C/W |
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 5.0 | °C/W |

**MC79M05C ELECTRICAL CHARACTERISTICS** ($V_I$ = −10 V, $I_O$ = 350 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | −4.8 | −5.0 | −5.2 | Vdc |
| Line Regulation ($T_J$ = +25°C) (Note 1)<br>−7.0 Vdc ≥ $V_I$ ≥ −25 Vdc<br>−8.0 Vdc ≥ $V_I$ ≥ −18 Vdc | $Reg_{line}$ | <br>—<br>— | <br>7.0<br>2.0 | <br>50<br>30 | mV |
| Load Regulation ($T_J$ = +25°C) (Note 1)<br>5.0 mA ≤ $I_O$ ≤ 500 mA | $Reg_{load}$ | — | 30 | 100 | mV |
| Output Voltage<br>−7.0 Vdc ≥ $V_I$ ≥ −25 Vdc, 5.0 mA ≤ $I_O$ ≤ 350 mA | $V_O$ | −4.75 | — | −5.25 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 4.3 | 8.0 | mA |
| Input Bias Current Change<br>−8.0 Vdc ≥ $V_I$ ≥ −25 Vdc, $I_O$ = 350 mA<br>5.0 mA ≤ $I_O$ ≤ 350 mA, $V_I$ = −10 V | $\Delta I_{IB}$ | <br>—<br>— | <br>—<br>— | <br>0.4<br>0.4 | mA |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 40 | — | µV |
| Ripple Rejection (f = 120 Hz) | RR | 54 | 66 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 500 mA, $T_J$ = +25°C | $\lvert V_I - V_O \rvert$ | — | 1.1 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | 0.2 | — | mV/°C |

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**MC79M12C ELECTRICAL CHARACTERISTICS** ($V_I$ = −19 V, $I_O$ = 350 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | −11.5 | −12 | −12.5 | Vdc |
| Line Regulation ($T_J$ = +25°C) (Note 1)<br>−14.5 Vdc ≥ $V_I$ ≥ −30 Vdc<br>−15 Vdc ≥ $V_I$ ≥ −25 Vdc | $Reg_{line}$ | <br>—<br>— | <br>5.0<br>3.0 | <br>80<br>50 | mV<br>mV |
| Load Regulation ($T_J$ = +25°C) (Note 1)<br>5.0 mA ≤ $I_O$ ≤ 500 mA | $Reg_{load}$ | — | 30 | 240 | mV |
| Output Voltage<br>−14.5 Vdc ≥ $V_I$ ≥ −30 Vdc, 5.0 mA ≤ $I_O$ ≤ 350 mA | $V_O$ | −11.4 | — | −12.6 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 4.4 | 8.0 | mA |
| Input Bias Current Change<br>−14.5 Vdc ≥ $V_I$ ≥ −30 Vdc, $I_O$ = 350 mA<br>5.0 mA ≤ $I_O$ ≤ 350 mA, $V_I$ = −19 V | $\Delta I_{IB}$ | <br>—<br>— | <br>—<br>— | <br>0.4<br>0.4 | mA |
| Output Noise Voltage ($T_A$ = +25°C, 10Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 75 | — | µV |
| Ripple Rejection (f = 120 Hz) | RR | 54 | 60 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 500 mA, $T_J$ = +25°C | $\|V_I-V_O\|$ | — | 1.1 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | −0.8 | — | mV/°C |

**MC79M15C ELECTRICAL CHARACTERISTICS** ($V_I$ = −23 V, $I_O$ = 350 mA, 0°C < $T_J$ < +125°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage ($T_J$ = +25°C) | $V_O$ | −14.4 | −15 | −15.6 | Vdc |
| Line Regulation ($T_J$ = +25°) (Note 1)<br>−17.5 Vdc ≥ $V_I$ ≥ −30 Vdc<br>−18 Vdc ≥ $V_I$ ≥ −28 Vdc | $Reg_{line}$ | <br>—<br>— | <br>5.0<br>3.0 | <br>80<br>50 | mV |
| Load Regulation ($T_J$ = +25°C) (Note 1)<br>5.0 mA ≤ $I_O$ ≤ 500 mA | $Reg_{load}$ | — | 30 | 240 | mV |
| Output Voltage<br>−17.5 Vdc ≥ $V_I$ ≥ −30 Vdc, 5.0 mA ≤ $I_O$ ≤ 350 mA | $V_O$ | −14.25 | — | −15.75 | Vdc |
| Input Bias Current ($T_J$ = +25°C) | $I_{IB}$ | — | 4.4 | 8.0 | mA |
| Input Bias Current Change<br>−17.5 Vdc ≥ $V_I$ ≥ −30 Vdc, $I_O$ = 350 mA<br>5.0 mA ≤ $I_O$ ≤ 350 mA, $V_I$ = −23 V | $\Delta I_{IB}$ | <br>—<br>— | <br>—<br>— | <br>0.4<br>0.4 | mA |
| Output Noise Voltage ($T_A$ = +25°C, 10 Hz ≤ f ≤ 100 kHz) | $V_n$ | — | 90 | — | µV |
| Ripple Rejection (f = 120 Hz) | RR | 54 | 60 | — | dB |
| Input-Output Voltage Differential<br>$I_O$ = 500 mA, $T_J$ = +25°C | $\|V_I-V_O\|$ | — | 1.1 | — | Vdc |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA, 0°C ≤ $T_J$ ≤ +125°C | $\Delta V_O/\Delta T$ | — | −1.0 | — | mV/°C |

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**MOTOROLA**

# MC34060
# MC35060

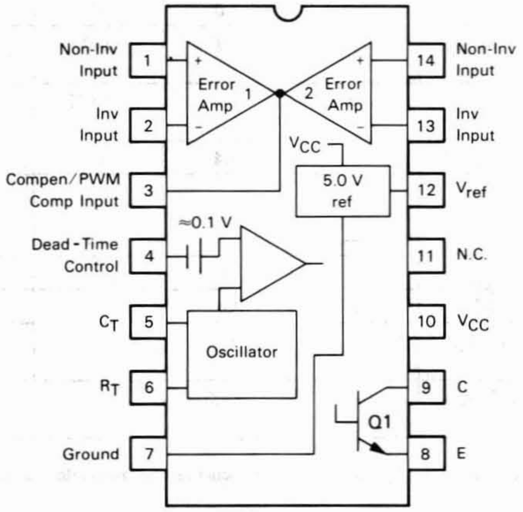
## Specifications and Applications Information

### SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The MC35060 and MC34060 are low cost fixed frequency, pulse width modulation control circuits designed primarily for single ended SWITCHMODE power supply control. These devices feature:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 Volt Reference
- Adjustable Dead Time Control
- Uncommitted Output Transistor for 200 mA Source or Sink

PIN CONNECTIONS

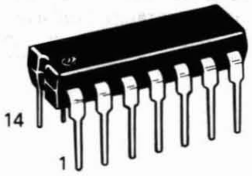

Non-Inv Input
1
Inv Input
2
Compen/PWM Comp Input
3
Dead-Time Control
4
$C_T$
5
$R_T$
6
Ground
7
Error Amp 1
Error Amp 2
$V_{CC}$
5.0 V ref
≈0.1 V
Oscillator
Q1
14
Non-Inv Input
13
Inv Input
12
$V_{ref}$
11
N.C.
10
$V_{CC}$
9
C
8
E

(Top View)

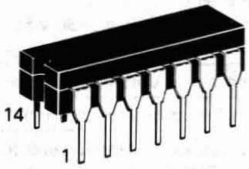
The MC34060 is specified over the commercial operating range of 0°C to +70°C. The MC35060 is specified over the full military range of −55 to +125°C.

### SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

SILICON MONOLITHIC
INTEGRATED CIRCUITS



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05
(MC34060 only)



**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA

ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC35060L | −55 to +125°C | Ceramic DIP |
| MC34060P | 0 to +70°C | Plastic DIP |
| MC34060L | 0 to +70°C | Ceramic DIP |

FIGURE 1 — BLOCK DIAGRAM

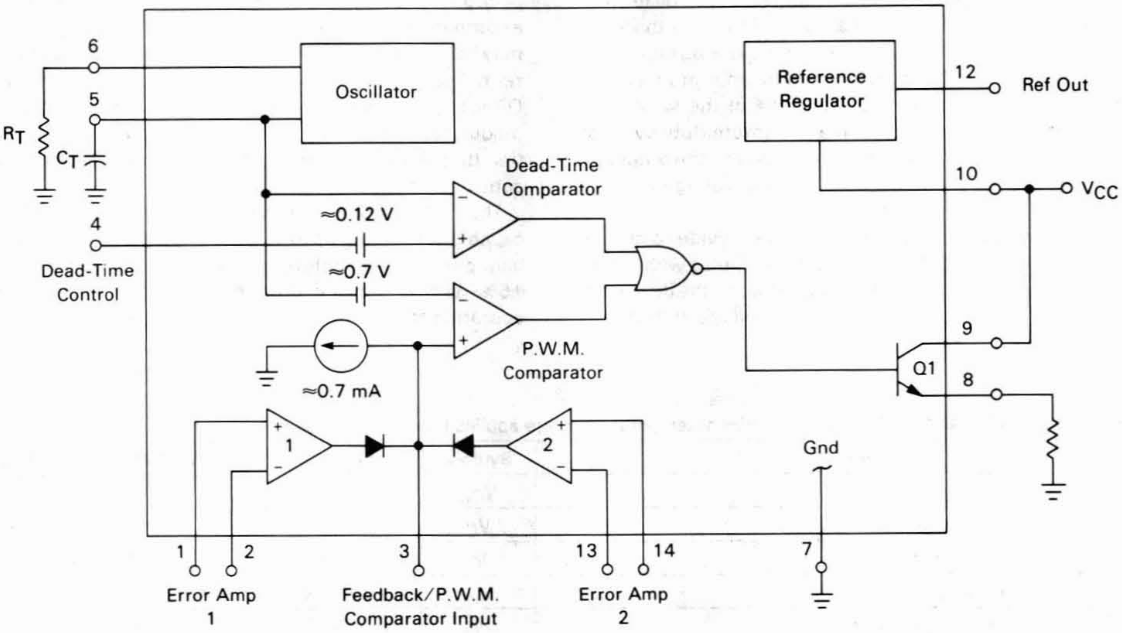
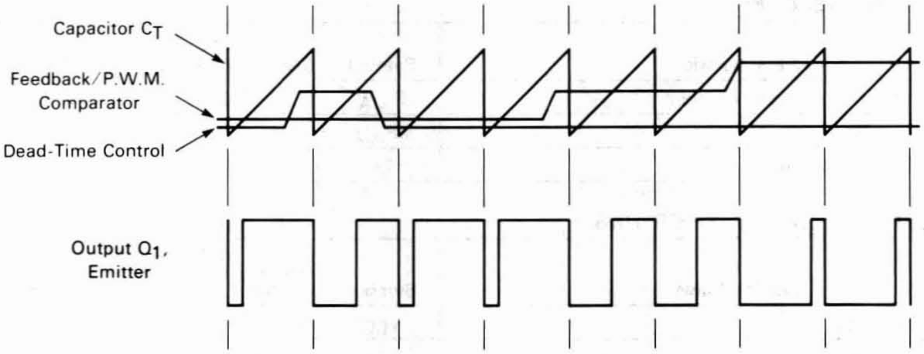

6
5
RT
CT
4
Dead-Time Control
Oscillator
Reference Regulator
12
Ref Out
10
VCC
Dead-Time Comparator
≈0.12 V
≈0.7 V
P.W.M. Comparator
≈0.7 mA
9
Q1
8
1
2
Gnd
1
2
3
13
14
7
Error Amp 1
Feedback/P.W.M. Comparator Input
Error Amp 2

FIGURE 2 — TIMING DIAGRAM


Capacitor CT
Feedback/P.W.M. Comparator
Dead-Time Control
Output Q1, Emitter

**Description**

The MC35060/34060 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, $R_T$ and $C_T$. The oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.1}{R_T \bullet C_T}$$

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor $C_T$ to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to ($V_{CC}$ −2 V), and may be used to sense power supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC35060/34060 has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±5% with a thermal drift of less than 50 mV over an operating temperature range of 0 to +70°C.

**MAXIMUM RATINGS** (Full operating ambient temperature range applies unless otherwise noted)

| Rating | Symbol | MC35060 | MC34060 | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 42 | 42 | V |
| Collector Output Voltage | $V_C$ | 42 | 42 | V |
| Collector Output Current | $I_C$ | 250 | 250 | mA |
| Amplifier Input Voltage | $V_{in}$ | $V_{CC}$ + 0.3 | $V_{CC}$ + 0.3 | V |
| Power Dissipation @ $T_A \leq 45°C$ | $P_D$ | 1000 | 1000 | mW |
| Operating Junction Temperature | $T_J$ | 150 | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | −55 to 125 | 0 to 70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to 150 | −65 to 150 | °C |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | L Suffix Ceramic Package | P Suffix Plastic Package | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 100 | 80 | °C/W |
| Power Derating Factor | $1/R_{\theta JA}$ | 10 | 12.5 | mW/°C |
| Derating Ambient Temperature | $T_A$ | 50 | 45 | °C |

**RECOMMENDED OPERATING CONDITIONS**

| Condition/Value | Symbol | MC35060/MC34060 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Power Supply Voltage | $V_{CC}$ | 7.0 | 15 | 40 | V |
| Collector Output Voltage | $V_C$ | — | 30 | 40 | V |
| Collector Output Current | $I_C$ | — | — | 200 | mA |
| Amplifier Input Voltage | $V_{in}$ | −0.3 | — | $V_{CC}$ −2.0 | V |
| Current Into Feedback Terminal | $I_{f.b.}$ | — | — | 0.3 | mA |
| Reference Output Current | $I_{ref}$ | — | — | 10 | mA |
| Timing Resistor | $R_T$ | 1.8 | 47 | 500 | kΩ |
| Timing Capacitor | $C_T$ | 0.00047 | 0.001 | 10 | µF |
| Oscillator Frequency | $f_{osc}$ | 1.0 | 25 | 200 | kHz |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $f_{osc}$ = 25 kHz unless otherwise noted. For typical values $T_A$ = 25°C, for min/max values $T_A$ is the operating ambient temperature range that applies unless otherwise noted.)

| Characteristic | Symbol | MC35060 | | | MC34060 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **REFERENCE SECTION** | | | | | | | | |
| Reference Voltage<br>($I_O$ = 1.0 mA) | $V_{ref}$ | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| Reference Voltage Change with Temperature<br>($\Delta T_A$ = Min to Max) | $V_{ref(\Delta T)}$ | — | 0.2 | 2.0 | — | 1.3 | 2.6 | % |
| Input Regulation<br>($V_{CC}$ = 7.0 V to 40 V) | $Reg_{line}$ | — | 2.0 | 25 | — | 2.0 | 25 | mV |
| Output Regulation<br>($I_O$ = 1.0 mA to 10 mA) | $Reg_{load}$ | — | 3.0 | 15 | — | 3.0 | 15 | mV |
| Short-Circuit Output Current<br>($V_{ref}$ = 0 V, $T_A$ = 25°C) | $I_{SC}$ | 10 | 35 | 50 | — | 35 | — | mA |
| **OUTPUT SECTION** | | | | | | | | |
| Collector Off-State Current<br>($V_{CC}$ = 40 V, $V_{CE}$ = 40 V) | $I_{C(off)}$ | — | 2.0 | 100 | — | 2.0 | 100 | μA |
| Emitter Off-State Current<br>($V_{CC}$ = 40 V, $V_C$ = 40 V, $V_E$ = 0 V) | $I_{E(off)}$ | — | — | −150 | — | — | −100 | μA |
| Collector-Emitter Saturation Voltage<br>Common-Emitter<br>($V_E$ = 0 V, $I_C$ = 200 mA) | $V_{sat(C)}$ | — | 1.1 | 1.5 | — | 1.1 | 1.3 | V |
| Emitter-Follower<br>($V_C$ = 15 V, $I_E$ = −200 mA) | $V_{sat(E)}$ | — | 1.5 | 2.5 | — | 1.5 | 2.5 | V |
| Output Voltage Rise time ($T_A$ = 25°C) | $t_r$ | | | | | | | ns |
| Common-Emitter (See Figure 12) | | — | 100 | 200 | — | 100 | 200 | |
| Emitter-Follower (See Figure 13) | | — | 100 | 200 | — | 100 | 200 | |
| Output Voltage Fall Time ($T_A$ = 25°C) | $t_f$ | | | | | | | ns |
| Common-Emitter (See Figure 12) | | — | 25 | 100 | — | 25 | 100 | |
| Emitter-Follower (See Figure 13) | | — | 40 | 100 | — | 40 | 100 | |

| Characteristic | Symbol | MC35060/MC34060 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **ERROR AMPLIFIER SECTIONS** | | | | | |
| Input Offset Voltage<br>($V_{O[Pin\ 3]}$ = 2.5 V) | $V_{IO}$ | — | 2.0 | 10 | mV |
| Input Offset Current<br>($V_{C[Pin\ 3]}$ = 2.5 V) | $I_{IO}$ | — | 5.0 | 250 | nA |
| Input Bias Current<br>($V_{O[Pin\ 3]}$ = 2.5 V) | $I_{IB}$ | — | 0.1 | 1.0 | μA |
| Input Common-Mode Voltage Range<br>($V_{CC}$ = 7.0 V to 40 V) | $V_{ICR}$ | -0.3 | — | $V_{CC}$-2.0 | V |
| Open Loop Voltage Gain<br>($\Delta V_O$ = 3.0 V, $V_O$ = 0.5 to 3.5 V, $R_L$ = 2.0 kΩ) | $A_{VOL}$ | 70 | 95 | — | dB |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $f_{osc}$ = 25 kHz unless otherwise noted. For typical values $T_A$ = 25°C, for min/max values $T_A$ is the operating ambient temperature range that applies unless otherwise noted.)

| Characteristic | Symbol | MC35060/MC34060 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **ERROR AMPLIFIER SECTIONS** (Continued) | | | | | |
| Unity-Gain Crossover Frequency<br>($V_O$ = 0.5, to 3.5 V, $R_L$ = 2.0 kΩ) | $f_c$ | — | 350 | — | kHz |
| Phase Margin at Unity-Gain<br>($V_O$ = 0.5 to 3.5 V, $R_L$ = 2.0 kΩ) | $\phi_m$ | — | 65 | — | deg. |
| Common-Mode Rejection Ratio<br>($V_{CC}$ = 40 V) | CMRR | 65 | 90 | — | dB |
| Power Supply Rejection Ratio<br>($\Delta V_{CC}$ = 33 V, $V_O$ = 2.5 V, $R_L$ = 2.0 kΩ) | PSRR | — | 100 | — | dB |
| Output Sink Current<br>($V_{O[Pin\ 3]}$ = 0.7 V) | $I_O-$ | 0.3 | 0.7 | — | mA |
| Output Source Current<br>($V_{O[Pin\ 3]}$ = 3.5 V) | $I_O+$ | −2.0 | −4.0 | — | mA |
| **PWM COMPARATOR SECTION** (Test circuit Figure 11) | | | | | |
| Input Threshold Voltage<br>(Zero Duty Cycle) | $V_{TH}$ | — | 3.5 | 4.5 | V |
| Input Sink Current<br>($V_{[Pin\ 3]}$ = 0.7 V) | $I_I-$ | 0.3 | 0.7 | — | mA |
| **DEAD-TIME CONTROL SECTION** (Test Circuit Figure 11) | | | | | |
| Input Bias Current (Pin 4)<br>($V_{in}$ = 0 to 5.25 V) | $I_{IB(DT)}$ | — | −2.0 | −10 | μA |
| Maximum Output Duty Cycle | $DC_{max}$ | | | | % |
| ($V_{in}$ = 0 V, $C_T$ = 0.1 μF, $R_T$ = 12 kΩ) | | 90 | 96 | 100 | |
| ($V_{in}$ = 0 V, $C_T$ = 0.001 μF, $R_T$ = 47 kΩ) | | — | 92 | 100 | |
| Input Threshold Voltage (Pin 4) | $V_{TH}$ | | | | V |
| (Zero Duty Cycle) | | — | 2.8 | 3.3 | |
| (Maximum Duty Cycle) | | 0 | — | — | |
| **OSCILLATOR SECTION** | | | | | |
| Frequency<br>($C_T$ = 0.001 μF, $R_T$ = 47 kΩ) | $f_{osc}$ | — | 25 | — | kHz |
| Standard Deviation of Frequency*<br>($C_T$ = 0.001 μF, $R_T$ = 47 kΩ) | $\sigma f_{osc}$ | — | 3.0 | — | % |
| Frequency Change with Voltage<br>($V_{CC}$ = 7.0 V to 40 V, $T_A$ = 25°C) | $\Delta f_{osc}(\Delta V)$ | — | 0.1 | — | % |
| Frequency Change with Temperature<br>($\Delta T_A$ = $T_{Alow}$ to $T_{Ahigh}$) | $\Delta f_{osc}(\Delta T)$ | — | ±1.0 | ±2.0 | % |
| **TOTAL DEVICE** | | | | | |
| Standby Supply Current<br>(Pin 6 at $V_{ref}$, all other inputs and outputs open) | $I_{CC}$ | | | | mA |
| ($V_{CC}$ = 15 V) | | — | 5.5 | 10 | |
| ($V_{CC}$ = 40 V) | | — | 7.0 | 15 | |
| Average Supply Current<br>($V_{[Pin\ 4]}$ = 2.0 V, $C_T$ = 0.001, $R_T$ = 47 kΩ). See Figure 11. | $I_S$ | — | 7.0 | — | mA |

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula; $\sigma = \sqrt{\frac{\sum_{n=1}^{N}(x_n - \bar{x})^2}{N-1}}$

**FIGURE 3 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE**

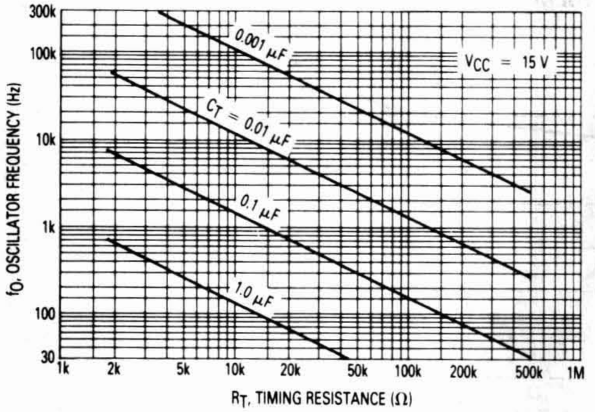


**FIGURE 4 — OPEN LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY**

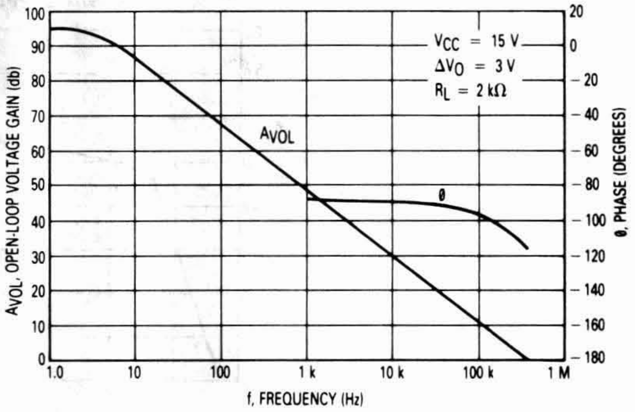


**FIGURE 5 — PERCENT DEAD-TIME versus OSCILLATOR FREQUENCY**

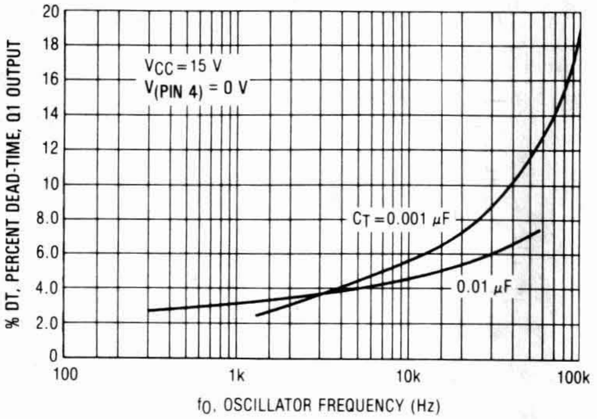


**FIGURE 6 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE**

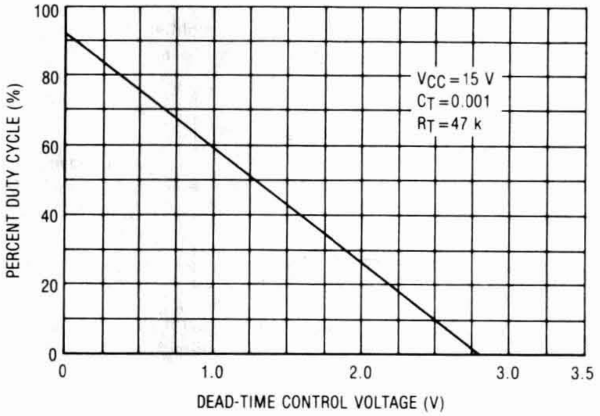


**FIGURE 7 — EMITTER FOLLOWER CONFIGURATION OUTPUT-SATURATION VOLTAGE versus EMITTER CURRENT**

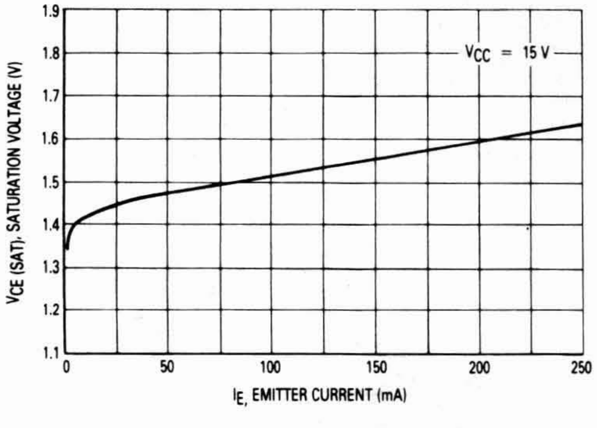


**FIGURE 8 — COMMON EMITTER CONFIGURATION OUTPUT-SATURATION VOLTAGE versus EMITTER CURRENT**

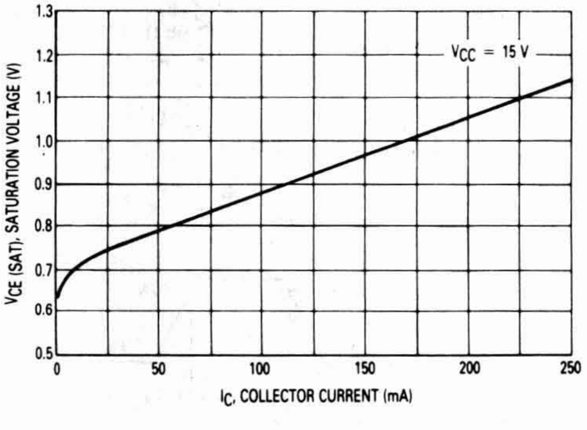


FIGURE 9 — STANDBY-SUPPLY CURRENT versus SUPPLY VOLTAGE

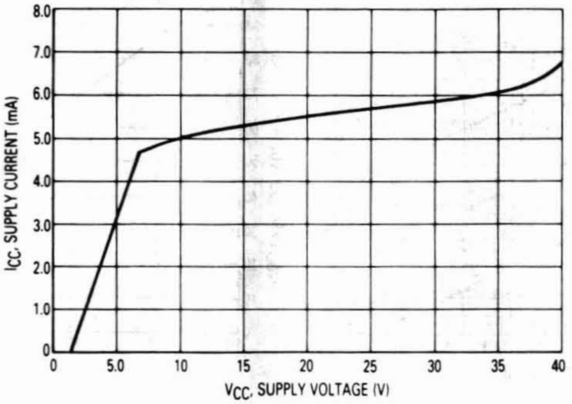


FIGURE 10 — ERROR AMPLIFIER CHARACTERISTICS

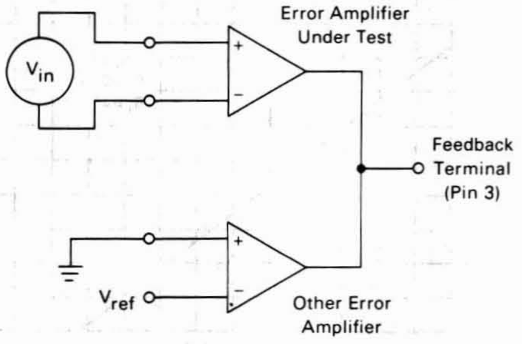

Error Amplifier Under Test
$V_{in}$
+
−
Feedback Terminal (Pin 3)
+
−
$V_{ref}$
Other Error Amplifier

FIGURE 11 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

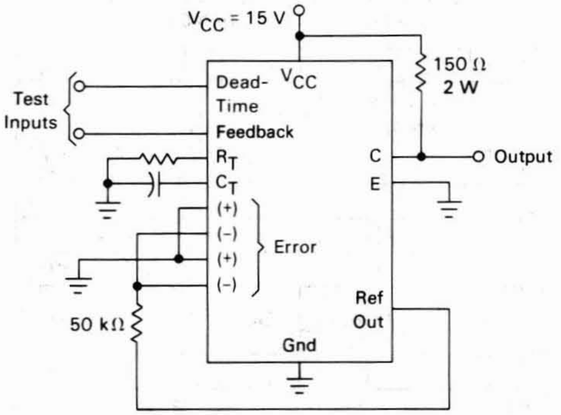

$V_{CC}$ = 15 V
150 Ω
2 W
Test Inputs
Dead-Time
$V_{CC}$
Feedback
$R_T$
$C_T$
C
E
Output
(+)
(−)
(+)
(−)
Error
Ref Out
50 kΩ
Gnd

FIGURE 12 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

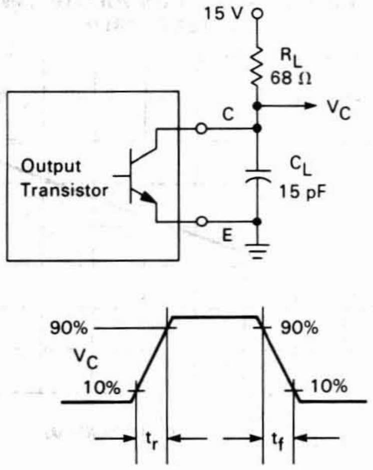

15 V
$R_L$
68 Ω
$V_C$
C
Output Transistor
$C_L$
15 pF
E
90%
90%
$V_C$
10%
10%
$t_r$
$t_f$

FIGURE 13 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

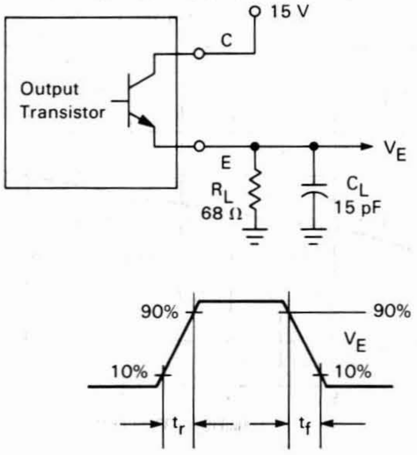
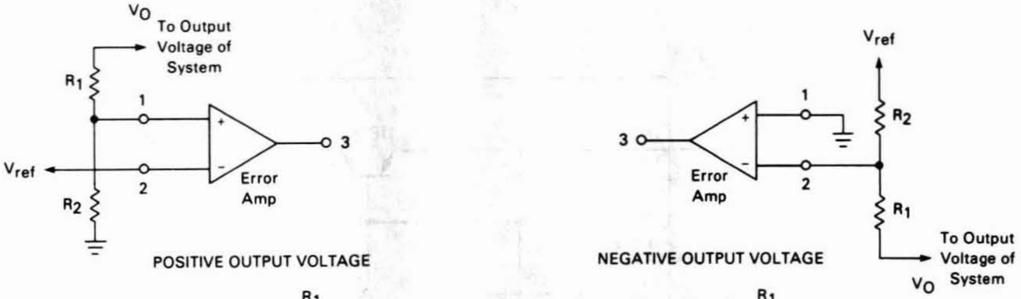

15 V
C
Output Transistor
$V_E$
E
$R_L$
68 Ω
$C_L$
15 pF
90%
90%
$V_E$
10%
10%
$t_r$
$t_f$

FIGURE 14 — ERROR AMPLIFIER SENSING TECHNIQUES


$V_O$
To Output Voltage of System
$R_1$
1
3
$V_{ref}$
2
Error Amp
$R_2$
$V_{ref}$
1
$R_2$
3
Error Amp
2
$R_1$
To Output Voltage of System
$V_O$

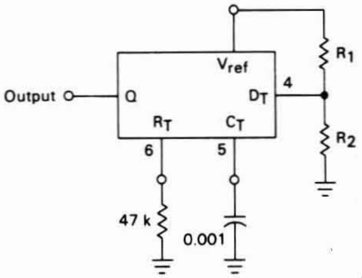
POSITIVE OUTPUT VOLTAGE

$$V_O = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

NEGATIVE OUTPUT VOLTAGE

$$V_O = -V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

FIGURE 15 — DEAD-TIME CONTROL CIRCUIT


$V_{ref}$
$R_1$
Output
Q
$D_T$
4
$R_T$
$C_T$
$R_2$
6
5
47 k
0.001

$$\text{Max \% On Time} \approx 92 - \left(\frac{160}{1 + \frac{R1}{R2}}\right)$$

FIGURE 16 — SOFT-START CIRCUIT

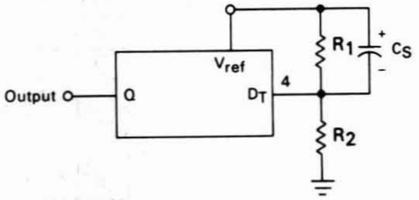

$V_{ref}$
$R_1$
+
$C_S$
–
Output
Q
$D_T$
4
$R_2$

FIGURE 17 — SLAVING TWO OR MORE CONTROL CIRCUITS

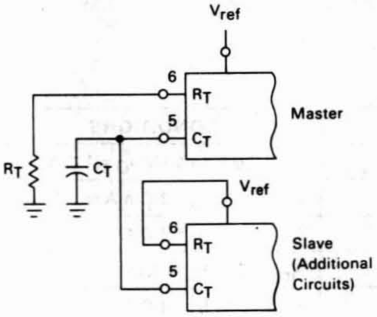
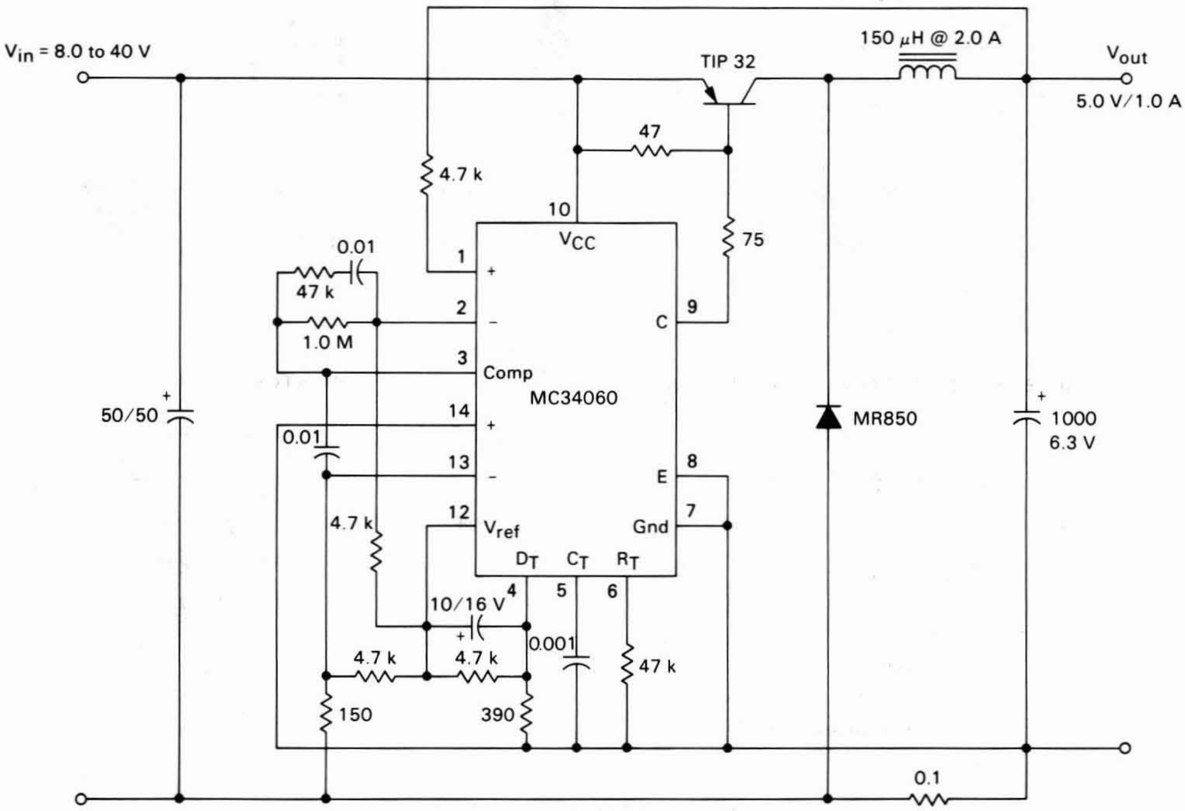

$V_{ref}$
6
$R_T$
Master
5
$C_T$
$R_T$
$C_T$
$V_{ref}$
6
$R_T$
Slave (Additional Circuits)
5
$C_T$

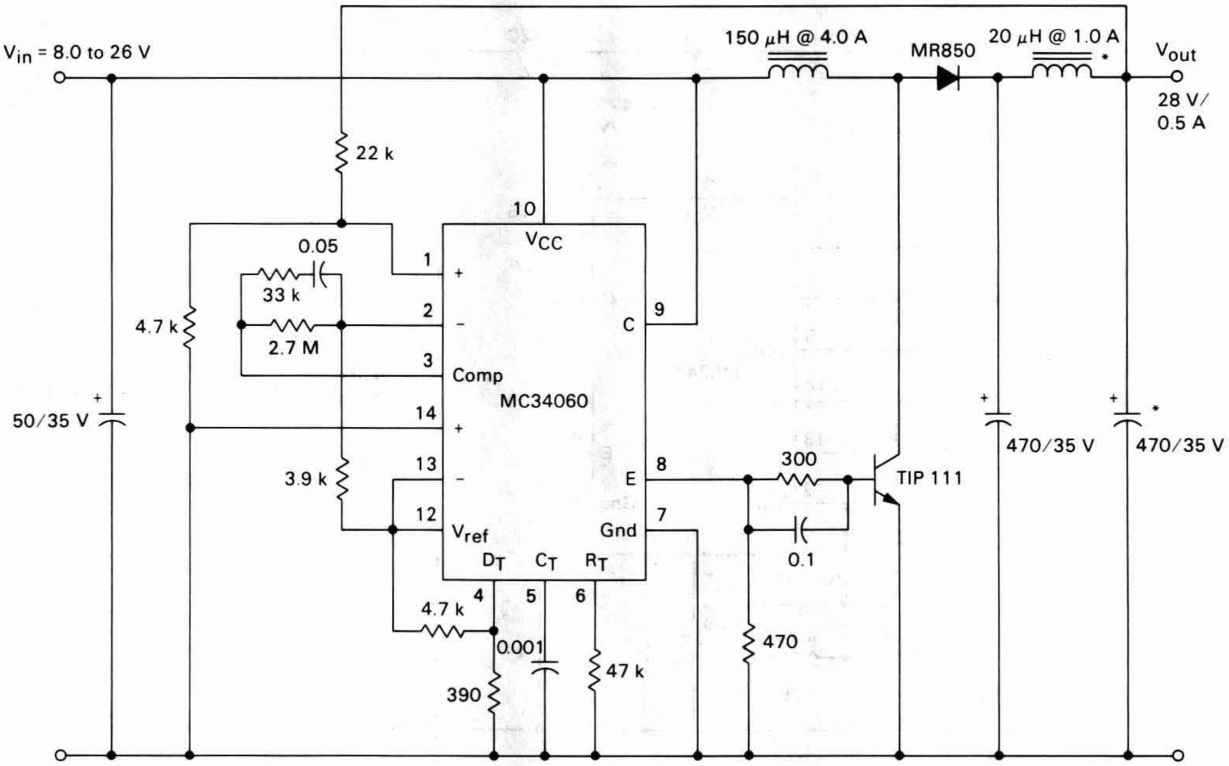
FIGURE 18 — STEP-DOWN CONVERTER WITH SOFT-START AND OUTPUT CURRENT LIMITING



$V_{in}$ = 8.0 to 40 V
TIP 32
150 μH @ 2.0 A
$V_{out}$
5.0 V/1.0 A
47
4.7 k
75
10
$V_{CC}$
0.01
47 k
1.0 M
1
+
2
−
3
Comp
MC34060
9
C
50/50
14
+
0.01
13
−
8
E
7
Gnd
12
$V_{ref}$
4.7 k
$D_T$
$C_T$
$R_T$
4
5
6
10/16 V
0.001
47 k
4.7 k
4.7 k
150
390
MR850
1000
6.3 V
0.1

| TEST | CONDITIONS | RESULTS |
|---|---|---|
| Line Regulation | $V_{in}$ = 8.0 V to 40 V, $I_O$ = 1.0 A | 25 mV  0.5% |
| Load Regulation | $V_{in}$ = 12 V, $I_O$ = 1.0 mA to 1.0 A | 3.0 mV  0.06% |
| Output Ripple | $V_{in}$ = 12 V, $I_O$ = 1.0 A | 75 mV p-p P.A.R.D. |
| Short Circuit Current | $V_{in}$ = 12 V, $R_L$ = 0.1 Ω | 1.6 A |
| Efficiency | $V_{in}$ = 12 V, $I_O$ = 1.0 A | 73% |

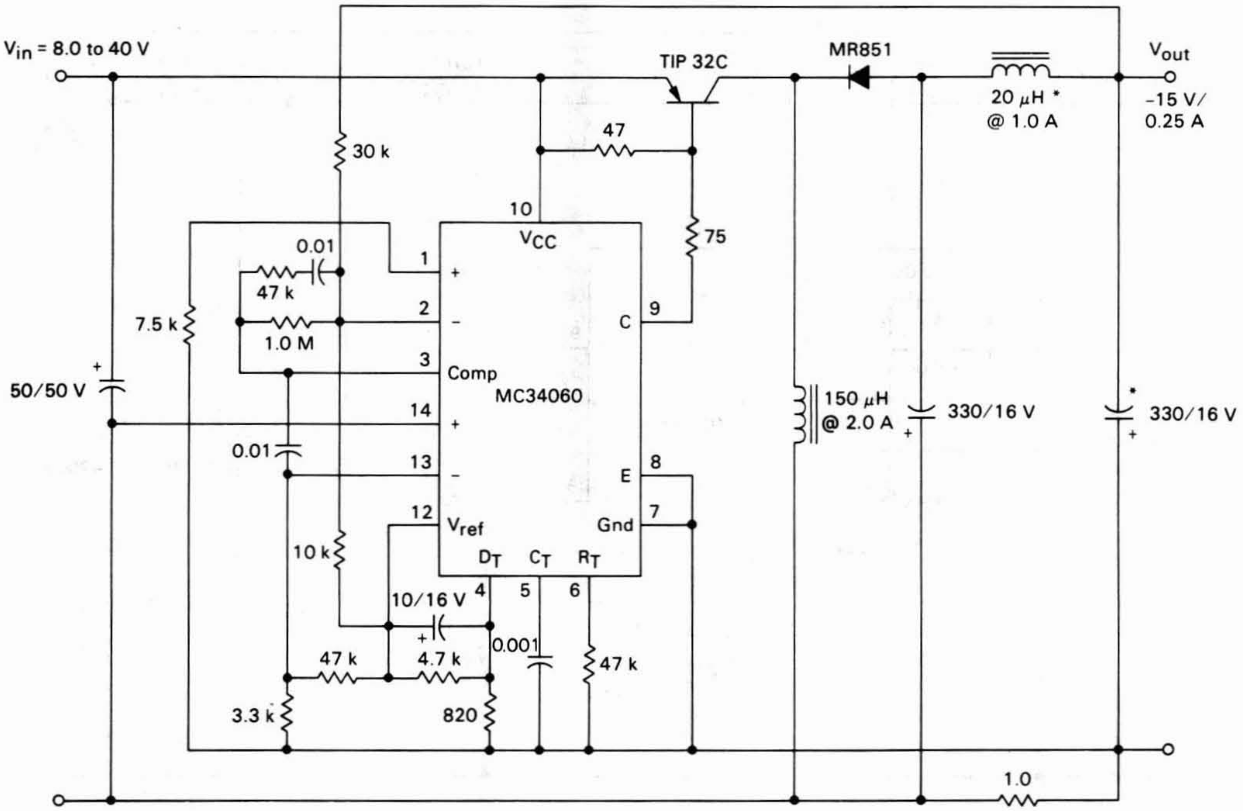
FIGURE 19 — STEP-UP CONVERTER


$V_{in}$ = 8.0 to 26 V
150 μH @ 4.0 A
MR850
20 μH @ 1.0 A
*
$V_{out}$
28 V/
0.5 A
22 k
10
$V_{CC}$
0.05
1
+
33 k
2
−
9
C
4.7 k
2.7 M
3
Comp
MC34060
50/35 V
+
14
+
470/35 V
+
470/35 V
+
*
3.9 k
13
−
8
E
300
TIP 111
12
$V_{ref}$
7
Gnd
$D_T$
$C_T$
$R_T$
0.1
4
5
6
4.7 k
0.001
47 k
470
390

| TEST | CONDITIONS | RESULTS |
|---|---|---|
| Line Regulation | $V_{in}$ = 8.0 V to 26 V, $I_O$ = 0.5 A | 40 mV 0.14% |
| Load Regulation | $V_{in}$ = 12 V, $I_O$ = 1.0 mA to 0.5 A | 5.0 mV 0.18% |
| Output Ripple | $V_{in}$ = 12 V, $I_O$ = 0.5 A | 24 mV p-p P.A.R.D. |
| Efficiency | $V_{in}$ = 12 V, $I_O$ = 0.5 A | 75% |

*Optional circuit to minimize output ripple.

**FIGURE 20 — STEP-UP/DOWN VOLTAGE INVERTING CONVERTER WITH SOFT-START AND CURRENT LIMITING**

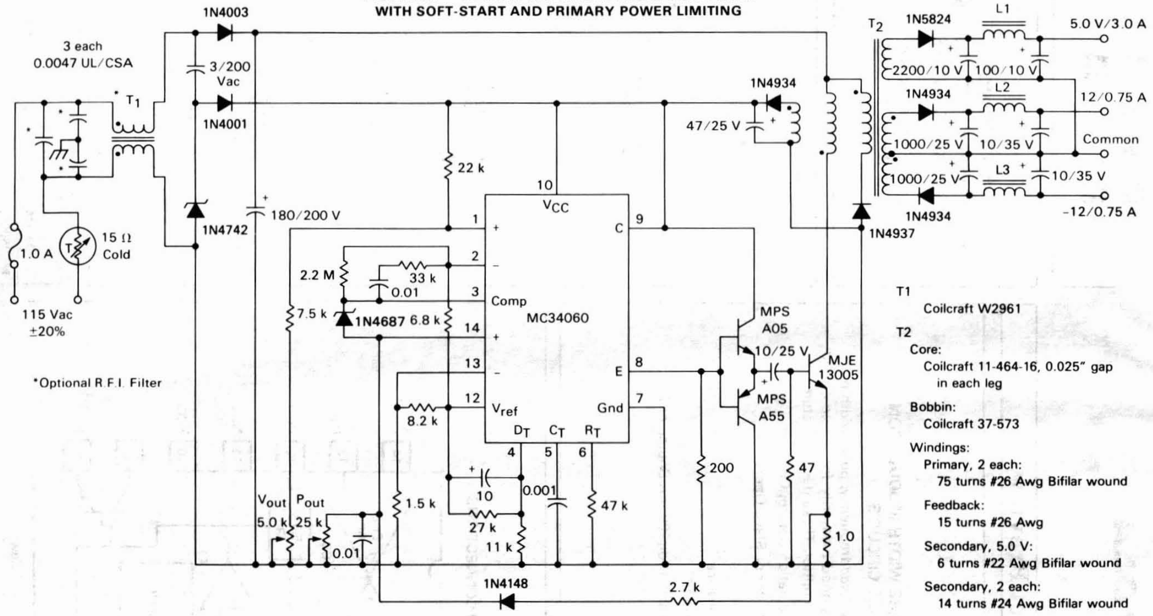


$V_{in}$ = 8.0 to 40 V
TIP 32C
MR851
$V_{out}$
20 μH *
@ 1.0 A
-15 V/
0.25 A
47
30 k
10
$V_{CC}$
75
0.01
1
+
47 k
2
–
9
C
7.5 k
1.0 M
3
Comp
MC34060
50/50 V
+
14
+
150 μH
@ 2.0 A
330/16 V
330/16 V
0.01
13
–
8
E
12
$V_{ref}$
7
Gnd
10 k
$D_T$
$C_T$
$R_T$
4
5
6
10/16 V
+
47 k
4.7 k
0.001
47 k
3.3 k
820
1.0

| TEST | CONDITIONS | RESULTS |
|---|---|---|
| Line Regulation | $V_{in}$ = 8.0 V to 40 V, $I_O$ = 250 mA | 52 mV 0.35% |
| Load Regulation | $V_{in}$ = 12 V, $I_O$ = 1 mA to 250 mA | 47 mV 0.32% |
| Output Ripple | $V_{in}$ = 12 V, $I_O$ = 250 mA | 10 mV p.p. P.A.R.D. |
| Short Circuit Current | $V_{in}$ = 12 V, $R_L$ = 0.1 Ω | 330 mA |
| Efficiency | $V_{in}$ = 12 V, $I_O$ = 250 mA | 86% |

*Optional circuit to minimize output ripple.

FIGURE 21 — 33 WATT OFF-LINE FLYBACK CONVERTER WITH SOFT-START AND PRIMARY POWER LIMITING


1N4003
3 each
0.0047 UL/CSA
T1
3/200 Vac
1N4001
1.0 A
15 Ω Cold
115 Vac ±20%
1N4742
180/200 V
22 k
10
VCC
1
2
3
14
13
12
9
8
7
C
E
Gnd
Comp
MC34060
Vref
DT
CT
RT
4
5
6
2.2 M
33 k
0.01
7.5 k
1N4687
6.8 k
8.2 k
1.5 k
10
27 k
11 k
0.001
47 k
Vout
Pout
5.0 k
25 k
0.01
1N4148
2.7 k
200
47
1.0
MPS A05
MPS A55
10/25 V
MJE 13005
1N4934
47/25 V
1N4937
T2
1N5824
L1
5.0 V/3.0 A
2200/10 V
100/10 V
1N4934
L2
12/0.75 A
1000/25 V
10/35 V
Common
1000/25 V
L3
10/35 V
1N4934
-12/0.75 A

*Optional R.F.I. Filter

| TEST | CONDITIONS | RESULTS |
|---|---|---|
| Line Regulation 5.0 V | $V_{in}$ = 95 to 135 Vac, $I_O$ = 3.0 A | 20 mV 0.40% |
| Line Regulation ±12 V | $V_{in}$ = 95 to 135 Vac, $I_O$ = ±0.75 A | 52 mV 0.26% |
| Load Regulation 5.0 V | $V_{in}$ = 115 Vac, $I_O$ = 1.0 to 4.0 A | 476 mV 9.5% |
| Load Regulation ±12 V | $V_{in}$ = 115 Vac, $I_O$ = ±0.4 to ±0.9 A | 300 mV 2.5% |
| Output Ripple 5.0 V | $V_{in}$ = 115 Vac, $I_O$ = 3.0 A | 45 mV p-p P.A.R.D. |
| Output Ripple ±12 V | $V_{in}$ = 115 Vac, $I_O$ = ±0.75 A | 75 mV p-p P.A.R.D. |
| Efficiency | $V_{in}$ = 115 Vac, $I_O$ 5.0 V = 3.0 A<br>$I_O$ ±12 = ±0.75 A | 74% |

T1
  Coilcraft W2961

T2
  Core:
    Coilcraft 11-464-16, 0.025″ gap in each leg
  Bobbin:
    Coilcraft 37-573
  Windings:
    Primary, 2 each:
      75 turns #26 Awg Bifilar wound
    Feedback:
      15 turns #26 Awg
    Secondary, 5.0 V:
      6 turns #22 Awg Bifilar wound
    Secondary, 2 each:
      14 turns #24 Awg Bifilar wound

L1
  Coilcraft Z7156, 15 μH @ 5.0 A

L2, L3
  Coilcraft Z7157, 25 μH @ 1.0 A

**MOTOROLA**

# MC34060A
# MC35060A
# MC33060A

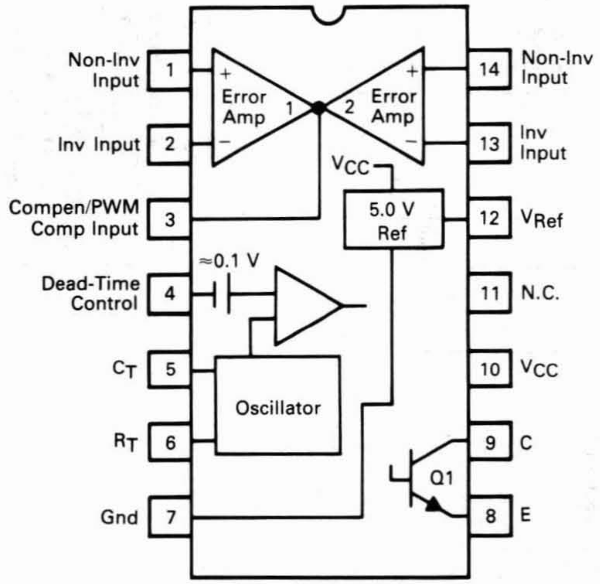
## Product Preview

## SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

These devices are low cost fixed frequency, pulse width modulation control circuits designed primarily for single ended SWITCHMODE power supply control. These devices feature:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 Volt, 1.0% Reference
- Adjustable Dead Time Control
- Uncommitted Output Transistor for 200 mA Source or Sink
- Undervoltage Lockout

### PIN CONNECTIONS

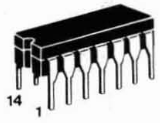


Non-Inv Input 1
Inv Input 2
Compen/PWM Comp Input 3
Dead-Time Control 4
$C_T$ 5
$R_T$ 6
Gnd 7
8 E
9 C
10 $V_{CC}$
11 N.C.
12 $V_{Ref}$
13 Inv Input
14 Non-Inv Input
Error Amp 1
Error Amp 2
+
−
$V_{CC}$
5.0 V Ref
≈0.1 V
Oscillator
Q1

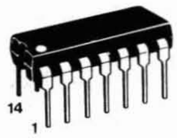
(top view)

## SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

### SILICON MONOLITHIC INTEGRATED CIRCUITS



**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA
(TO-116)



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC35060L | −55 to +125°C | Ceramic DIP |
| MC34060AD | — | SO-14 |
| MC34060P | 0 to +70°C | Plastic DIP |
| MC33060P | −40 to +85°C | Plastic DIP |

**MOTOROLA**

# MC34063
# MC35063
# MC33063

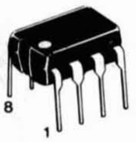
## DC TO DC CONVERTER CONTROL CIRCUITS

The MC34063 Series is a monolithic control circuit containing the primary functions required for dc-to-c converters. The device consists of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current of 1.5 A
- Output Voltage Adjustable from 1.25 to 40 V
- Frequency Operation from 100 Hz to 100 kHz

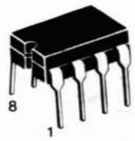
## DC TO DC CONVERTER CONTROL CIRCUITS

**SILICON MONOLITHIC INTEGRATED CIRCUITS**

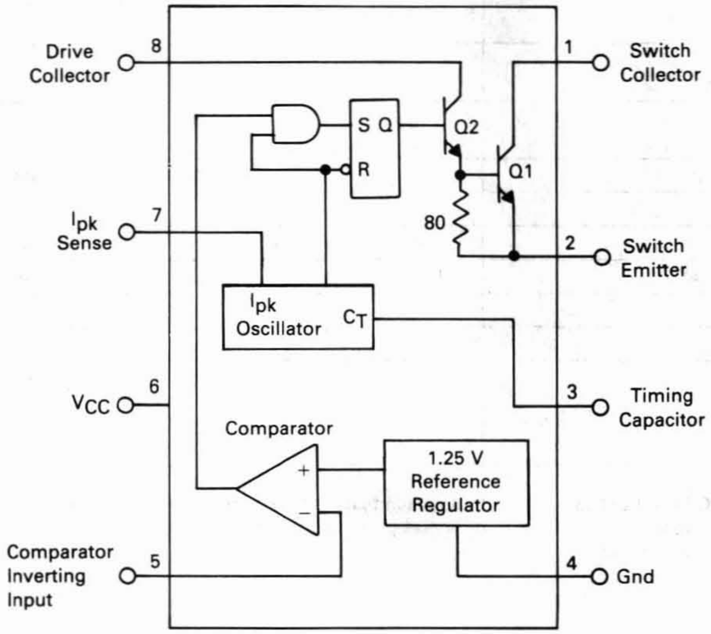


**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04

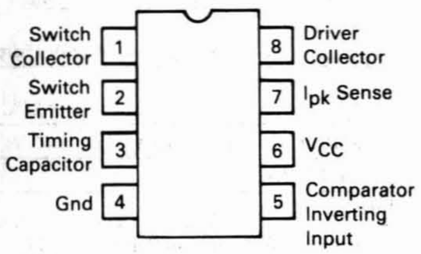
**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02



### FUNCTIONAL BLOCK DIAGRAM


Drive Collector
8
1
Switch Collector
S Q
R
Q2
Q1
80
$I_{pk}$ Sense
7
2
Switch Emitter
$I_{pk}$ Oscillator
$C_T$
$V_{CC}$
6
3
Timing Capacitor
Comparator
+
−
1.25 V Reference Regulator
Comparator Inverting Input
5
4
Gnd

### PIN CONNECTIONS


Switch Collector
1
Switch Emitter
2
Timing Capacitor
3
Gnd
4
8
Driver Collector
7
$I_{pk}$ Sense
6
$V_{CC}$
5
Comparator Inverting Input

(Top View)

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC35063U | − 55 to + 125°C | Ceramic DIP |
| MC33063U | − 40 to + 85°C | Ceramic DIP |
| MC33063P1 | | Plastic DIP |
| MC34063U | 0 to + 70°C | Ceramic DIP |
| MC34063P1 | | Plastic DIP |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 40 | Vdc |
| Comparator Input Voltage Range | $V_{IR}$ | −0.3 to +40 | Vdc |
| Switch Collector Voltage | $V_{C(switch)}$ | 40 | Vdc |
| Switch Emitter Voltage | $V_{E(switch)}$ | 40 | Vdc |
| Switch Collector to Emitter Voltage | $V_{CE(switch)}$ | 40 | Vdc |
| Driver Collector Voltage | $V_{C(driver)}$ | 40 | Vdc |
| Switch Current | $I_{SW}$ | 1.5 | Amps |
| Power Dissipation and Thermal Characteristics<br>Ceramic Package<br>$T_A = +25°C$<br>Derate above $T_A = +25°C$<br>Plastic Package<br>$T_A = +25°C$<br>Derate above $T_A = +25°C$ | <br><br>$P_D$<br>$1/\theta_{JA}$<br><br>$P_D$<br>$1/\theta_{JA}$ | <br><br>1.25<br>10<br><br>1.0<br>10 | <br><br>W<br>mW/°C<br><br>W<br>mW/°C |
| Operating Junction Temperature<br>Ceramic Package<br>Plastic Package | $T_J$ | <br>+150<br>+125 | °C |
| Operating Ambient Temperature Range<br>MC35063<br>MC33063<br>MC34063 | $T_A$ | <br>−55 to +125<br>−40 to +85<br>0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V; $T_A = T_{low}$ to $T_{high}$ [Note 1] unless otherwise specified.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | |
| Charging Current (5.0 V ≤ $V_{CC}$ ≤ 40 V, $T_A$ = 25°C) | $I_{chg}$ | 20 | 35 | 50 | μA |
| Discharge current (5.0 V ≤ $V_{CC}$ ≤ 40 V; $T_A$ = 25°C) | $I_{dischg}$ | 150 | 200 | 250 | μA |
| Voltage Swing ($T_A$ = 25°C) | $V_{osc}$ | — | 0.5 | — | $V_{p-p}$ |
| Discharge to Charge Current Ratio ($I_{pk(sense)} = V_{CC}$, $T_A$ = 25°C) | $I_{dischg}/I_{chg}$ | — | 6.0 | — | — |
| Current Limit Sense Voltage<br>$I_{chg} = I_{dischg}$, $T_A$ = 25°C | $V_{Ipk(sense)}$ | 250 | 300 | 350 | mV |
| **OUTPUT SWITCH (Note 2)** | | | | | |
| Saturation Voltage, Darlington Connection<br>$I_{SW}$ = 1.0 A; $V_{C(driver)} = V_{C(switch)}$ | $V_{CE(sat)}$ | — | 1.0 | 1.3 | V |
| Saturation Voltage<br>$I_{SW}$ = 1.0 A; $I_{C(driver)}$ = 50 mA, (Forced B ≈ 20) | $V_{CE(sat)}$ | — | 0.45 | 0.7 | V |
| DC Current Gain<br>$I_{SW}$ = 1.0 A; $V_{CE}$ = 5.0 V; $T_A$ = 25°C | $h_{FE}$ | 35 | 120 | — | — |
| Collector Off-State Current ($V_{CE}$ = 40 V; $T_A$ = 25°C) | $I_{C(off)}$ | — | 10 | — | nA |
| **COMPARATOR** | | | | | |
| Threshold Voltage | $V_{th}$ | 1.18 | 1.25 | 1.32 | V |
| Threshold Voltage Line Regulation (3.0 V ≤ $V_{CC}$ ≤ 40 V) | $Reg_{line}$ | — | 0.04 | 0.2 | mV/V |
| Input Bias Current ($V_{in}$ = 0 V) | $I_{IB}$ | — | 40 | 400 | nA |
| **TOTAL DEVICE** | | | | | |
| Supply Current<br>5.0 V ≤ $V_{CC}$ ≤ 40 V, $C_T$ = 0.001 μF<br>$I_{pk(sense)} = V_{CC}$, V pin 5 > $V_{th}$,<br>Pin 2 = Gnd, Remaining pins open | $I_{CC}$ | — | 2.4 | 3.5 | mA |

NOTES:

1. $T_{low}$ = −55°C for MC35063 $T_{high}$ = +125°C for MC35063
−40°C for MC33063 +85°C for MC33063
0°C for MC34063 +70°C for MC34063

2. Output switch tests are performed under pulsed conditions to minimize power dissipation.

**FIGURE 1 — OUTPUT SWITCH ON-OFF TIME versus OSCILLATOR TIMING CAPACITOR**

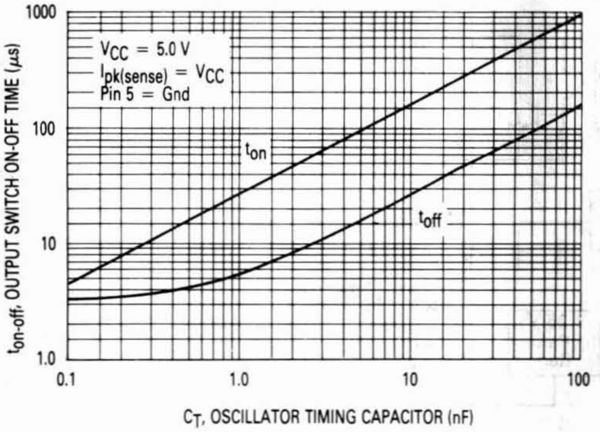


**FIGURE 2 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE**

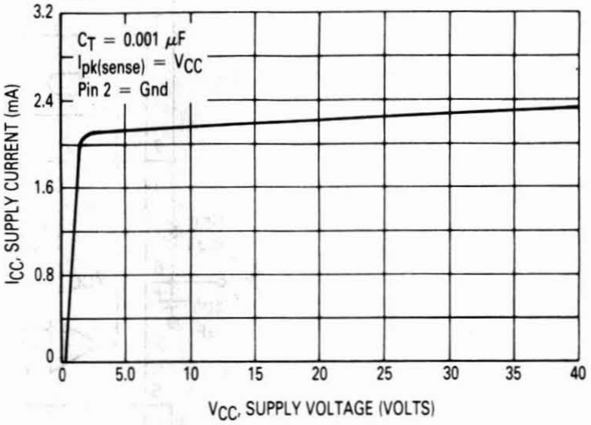


**FIGURE 3 — EMITTER-FOLLOWER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus EMITTER CURRENT**

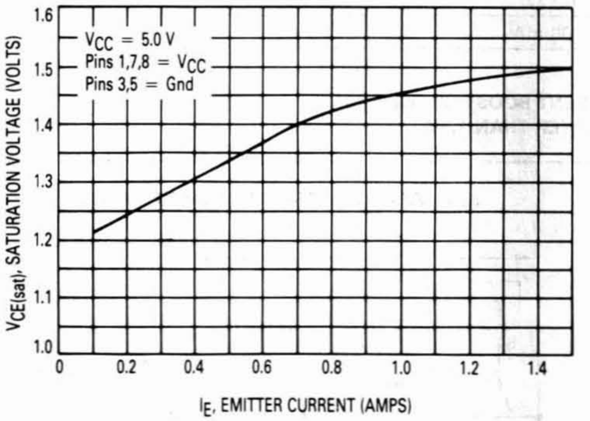


**FIGURE 4 — COMMON-EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT**

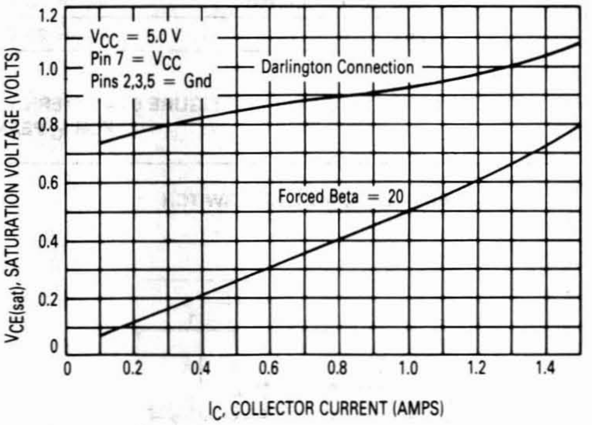
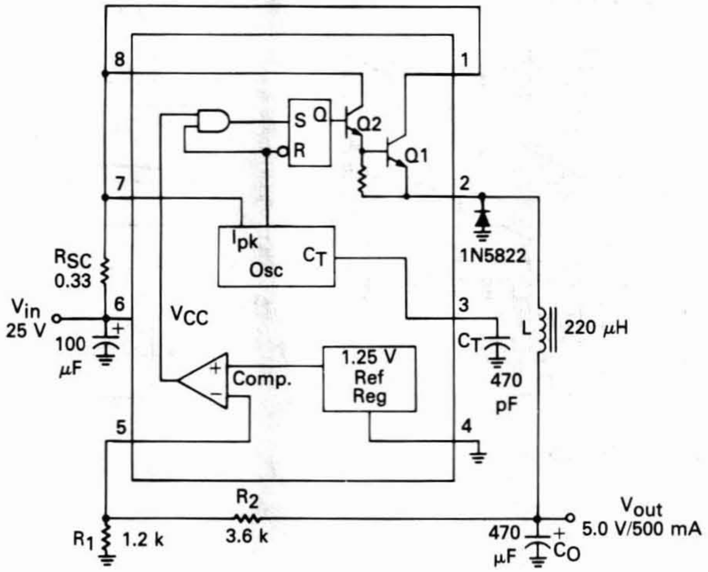
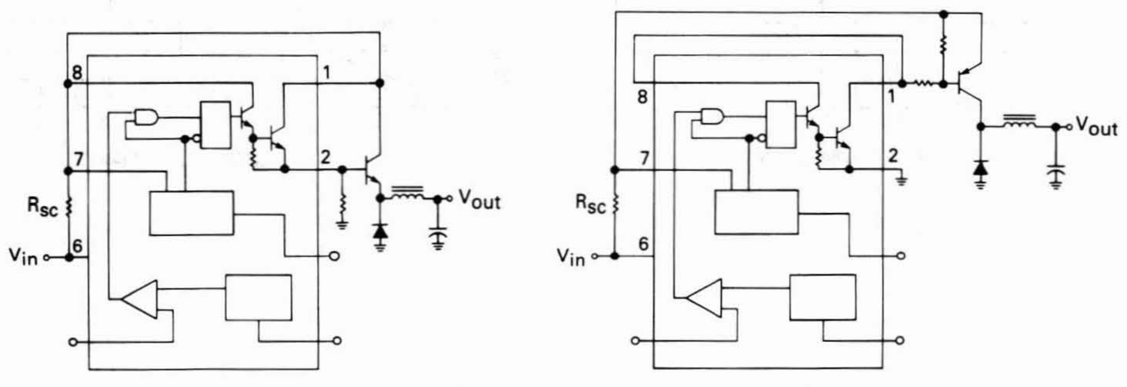


FIGURE 5 — STEP-DOWN CONVERTER


8
1
S
Q
R
Q2
Q1
7
2
Ipk
Osc
$C_T$
1N5822
$R_{SC}$
0.33
$V_{in}$
25 V
6
$V_{CC}$
3
$C_T$
470
pF
L
220 µH
100
µF
+
Comp.
1.25 V
Ref
Reg
5
4
$R_2$
3.6 k
$R_1$
1.2 k
$V_{out}$
5.0 V/500 mA
470
µF
$C_O$

| Test | Conditions | Results |
|---|---|---|
| Line Regulation | $V_{in}$ = 15 to 25 V, $I_o$ = 500 mA | 15 mV |
| Load Regulation | $V_{in}$ = 25 V, $I_o$ = 50 to 500 mA | 5.0 mV |
| Output Ripple | $V_{in}$ = 25 V, $I_o$ = 500 mA | 40 $mV_{p-p}$ |
| Short Circuit Current | $V_{in}$ = 25 V, $R_L$ = 0.1 Ω | 2.3 A |
| Efficiency | $V_{in}$ = 25 V, $I_o$ = 500 mA | 84.7% |

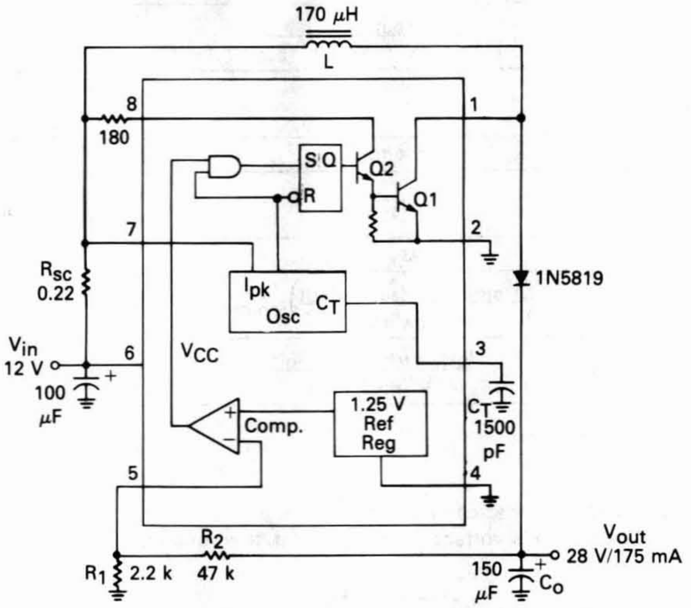
FIGURE 6 — EXTERNAL CURRENT BOOST CONNECTIONS FOR $I_C$ PEAK GREATER THAN 1.5 A


6A — EXTERNAL NPN SWITCH

6B — EXTERNAL PNP SATURATED SWITCH

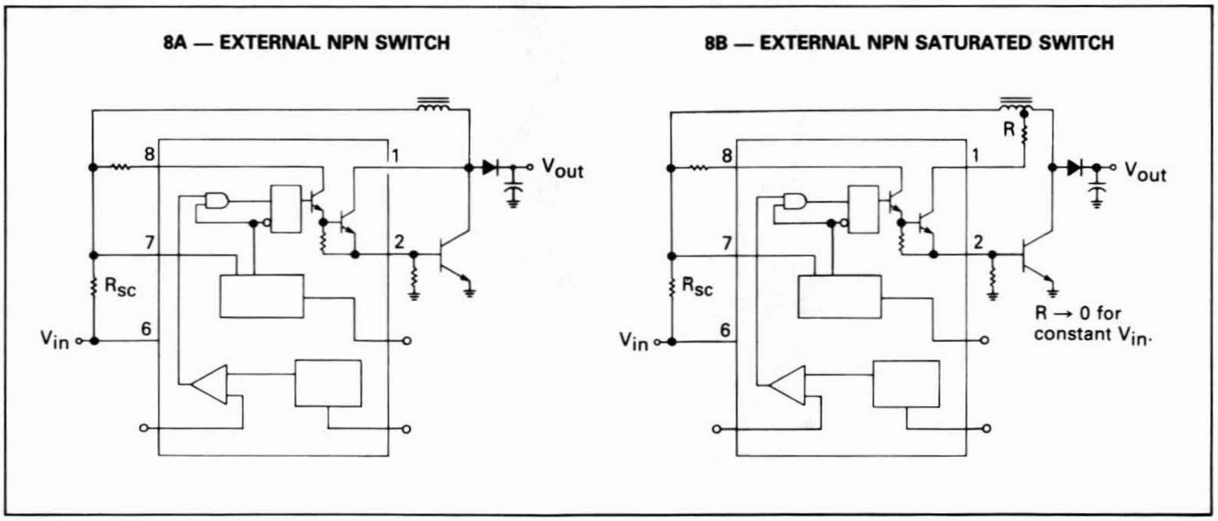
8
1
7
2
$R_{sc}$
6
$V_{in}$
$V_{out}$
8
1
7
2
$R_{sc}$
6
$V_{in}$
$V_{out}$

FIGURE 7 — STEP-UP CONVERTER


170 µH
L
8
180
1
S Q
R
Q2
Q1
7
2
Rsc
0.22
Ipk
Osc
CT
1N5819
Vin
12 V
6
VCC
3
+
100
µF
+
Comp.
−
1.25 V
Ref
Reg
CT
1500
pF
5
4
R2
Vout
28 V/175 mA
R1
2.2 k
47 k
150
µF
+
Co

| Test | Conditions | Results |
|---|---|---|
| Line Regulation | $V_{in}$ = 8.0 to 16 V, $I_O$ = 175 mA | 12 mV |
| Load Regulation | $V_{in}$ = 12 V, $I_O$ = 75 to 175 mA | 45 mV |
| Output Ripple | $V_{in}$ = 12 V, $I_O$ = 175 mA | 150 $mV_{p-p}$ |
| Short Circuit Current | $V_{in}$ = 12 V, $R_L$ = 0.1 Ω | 2.0 A |
| Efficiency | $V_{in}$ = 12 V, $I_O$ = 175 mA | 93% |

FIGURE 8 — EXTERNAL CURRENT BOOST CONNECTIONS FOR $I_C$ PEAK GREATER THAN 1.5 A


8A — EXTERNAL NPN SWITCH

8B — EXTERNAL NPN SATURATED SWITCH

8
1
Vout
7
2
Rsc
Vin
6
8
R
1
Vout
7
2
Rsc
Vin
6
R → 0 for
constant Vin.

FIGURE 9 — DESIGN FORMULA TABLE

| Calculation | Step-Down | Step-Up |
|---|---|---|
| $\frac{t_{on}}{t_{off}}$ | $\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$ | $\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$ |
| $(t_{on} + t_{off})_{max}$ | $\frac{1}{f_{min}}$ | $\frac{1}{f_{min}}$ |
| $C_T$ | $4 \times 10^{-5}\ t_{on}$ | $4 \times 10^{-5}\ t_{on}$ |
| $I_{pk(switch)}$ | $2I_{out(max)}$ | $2I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$ |
| $R_{SC}$ | $0.33/I_{pk(switch)}$ | $0.33/I_{pk(switch)}$ |
| $L_{(min)}$ | $\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$ | $\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$ |
| $C_o$ | $\frac{I_{pk(switch)}(t_{on} + t_{off})}{8\ V_{ripple(p-p)}}$ | $\approx \frac{I_{out}\ t_{on}}{V_{ripple}}$ |

$V_{sat}$ = Saturation voltage of the output switch.
$V_F$ = Forward voltage drop of the ringback rectifier

**The following power supply characteristics must be chosen:**

**$V_{in}$** — Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up converter.

**$V_{out}$** — Desired output voltage, $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$.

**$I_{out}$** — Desired output current.

**$f_{min}$** — Minimum desired output switching frequency at the selected values for $V_{in}$ and $I_O$.

**$V_{ripple(p-p)}$** — Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

**Note:**
**For further information refer to application note AN920A.**

# SG1525A/SG1527A
# SG2525A/SG2527A
# SG3525A/SG3527A

## PULSE WIDTH MODULATOR CONTROL CIRCUITS

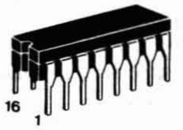
The SG1525A/1527A series of pulse width modulator control-circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on-chip +5.1 volt reference is trimmed to ±1% and the error amplifier has an input common-mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of dead time can be programmed by a single resistor connected between the $C_T$ and Discharge pins. These devices also feature built-in soft-start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft-start capacitor when $V_{CC}$ is below nominal. The output stages are totem-pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG1525A series features NOR Logic resulting in a low output for an off state while the SG1527A series utilizes OR Logic which gives a high output when off. The devices are available in Military, Industrial and Commercial temperature ranges.

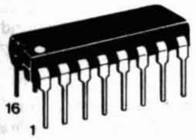
- 8.0 to 35 Volt Operation
- 5.1 Volt ± 1.0% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Dead Time Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse-by-Pulse Shutdown
- Dual Source/Sink Outputs: ± 400 mA Peak

## PULSE WIDTH MODULATOR CONTROL CIRCUITS

**SILICON MONOLITHIC INTEGRATED CIRCUITS**

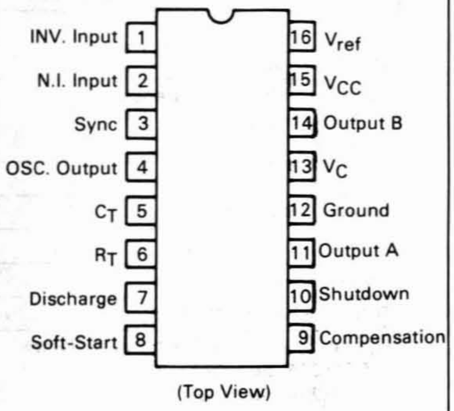
**J SUFFIX**
CERAMIC PACKAGE
CASE 620-02





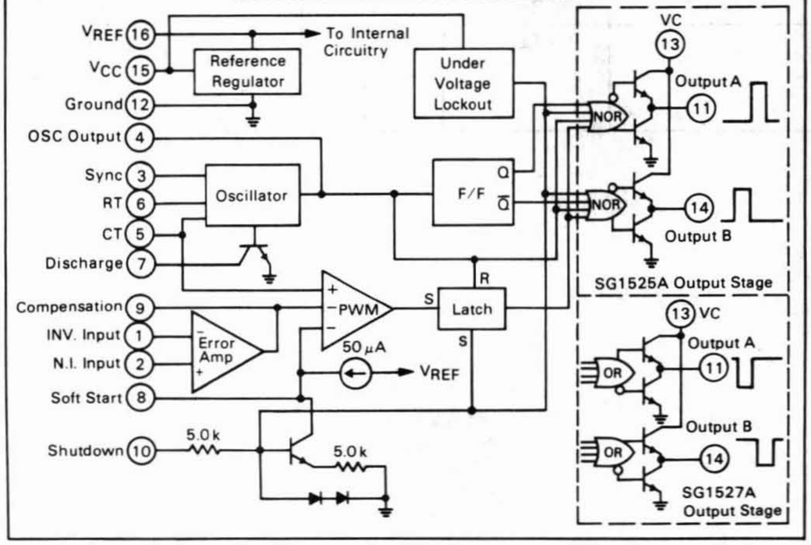
**N SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### PIN CONNECTIONS


INV. Input 1
N.I. Input 2
Sync 3
OSC. Output 4
$C_T$ 5
$R_T$ 6
Discharge 7
Soft-Start 8
16 $V_{ref}$
15 $V_{CC}$
14 Output B
13 $V_C$
12 Ground
11 Output A
10 Shutdown
9 Compensation

(Top View)

### FUNCTIONAL BLOCK DIAGRAM


$V_{REF}$ 16
$V_{CC}$ 15
Ground 12
OSC Output 4
Sync 3
RT 6
CT 5
Discharge 7
Compensation 9
INV. Input 1
N.I. Input 2
Soft Start 8
Shutdown 10
To Internal Circuitry
Reference Regulator
Under Voltage Lockout
Oscillator
F/F
Q
$\overline{Q}$
PWM
Error Amp
50 μA
$V_{REF}$
Latch
R
S
5.0 k
5.0 k
VC
13
Output A
11
NOR
NOR
14
Output B
SG1525A Output Stage
13 VC
Output A
11
OR
OR
Output B
14
SG1527A Output Stage

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| SG1525AJ | −55 to +125°C | Ceramic DIP |
| SG1527AJ | −55 to +125°C | Ceramic DIP |
| SG2525AJ | −25 to +85°C | Ceramic DIP |
| SG2525AN | −25 to +85°C | Plastic DIP |
| SG2527AJ | −25 to +85°C | Ceramic DIP |
| SG2527AN | −25 to +85°C | Plastic DIP |
| SG3525AJ | 0 to +70°C | Ceramic DIP |
| SG3525AN | 0 to +70°C | Plastic DIP |
| SG3527AJ | 0 to +70°C | Ceramic DIP |
| SG3527AN | 0 to +70°C | Plastic DIP |

## MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | +40 | Vdc |
| Collector Supply Voltage | $V_C$ | +40 | Vdc |
| Logic Inputs | — | −0.3 to +5.5 | V |
| Analog Inputs | — | −0.3 to $V_{CC}$ | V |
| Output Current, Source or Sink | $I_O$ | ±500 | mA |
| Reference Output Current | $I_{ref}$ | 50 | mA |
| Oscillator Charging Current | — | 5.0 | mA |
| Power Dissipation (Plastic & Ceramic Package)<br>Note 2, $T_A = +25°C$<br>Note 3, $T_C = +25°C$ | $P_D$ | <br>1000<br>2000 | mW |
| Thermal Resistance Junction to Air<br>Plastic and Ceramic Package | $R_{\theta JA}$ | 100 | °C/W |
| Thermal Resistance Junction to Case<br>Plastic and Ceramic Package | $R_{\theta JC}$ | 60 | °C/W |
| Operating Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range Ceramic Package<br>Plastic Package | $T_{stg}$ | −65 to +150<br>−55 to +125 | °C |
| Lead Temperature (Soldering, 10 Seconds) | $T_{Solder}$ | +300 | °C |

NOTES:
1. Values beyond which damage may occur
2. Derate at 10 mW/°C for ambient temperatures above +50°C
3. Derate at 16 mW/°C for case temperatures above +25°C

## RECOMMENDED OPERATING CONDITIONS

| Characteristic | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | +8.0 | +35 | Vdc |
| Collector Supply Voltage | $V_C$ | +4.5 | +35 | Vdc |
| Output Sink/Source Current<br>(Steady State)<br>(Peak) | $I_O$ | <br>0<br>0 | <br>±100<br>±400 | mA |
| Reference Load Current | $I_{ref}$ | 0 | 20 | mA |
| Oscillator Frequency Range | $f_{osc}$ | 0.1 | 400 | kHz |
| Oscillator Timing Resistor | $R_T$ | 2.0 | 150 | kΩ |
| Oscillator Timing Capacitor | $C_T$ | 0.001 | 0.2 | μF |
| Deadtime Resistor Range | $R_D$ | 0 | 500 | Ω |
| Operating Ambient Temperature Range<br>SG1525A, SG1527A<br>SG2525A, SG2527A<br>SG3525A, SG3527A | $T_A$ | <br>−55<br>−25<br>0 | <br>+125<br>+85<br>+70 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +20 Vdc, $T_A$ = $T_{low}$ to $T_{high}$ [Note 4], unless otherwise specified)

| Characteristic | Symbol | SG1525A/2525A<br>SG1527A/2527A | | | SG3525A<br>SG3527A | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **REFERENCE SECTION** | | | | | | | | |
| Reference Output Voltage ($T_J$ = +25°C) | $V_{ref}$ | 5.05 | 5.10 | 5.15 | 5.00 | 5.10 | 5.20 | Vdc |
| Line Regulation (+8.0 V ≤ $V_{CC}$ ≤ +35 V) | $Reg_{line}$ | — | 10 | 20 | — | 10 | 20 | mV |
| Load Regulation (0 mA ≤ $I_L$ ≤ 20 mA) | $Reg_{load}$ | — | 20 | 50 | — | 20 | 50 | mV |
| Temperature Stability | $\Delta V_{ref}/\Delta T$ | — | 20 | 50 | — | 20 | 50 | mV |
| Total Output Variation Includes Line and Load Regulation over Temperature | $\Delta V_{ref}$ | 5.00 | — | 5.20 | 4.95 | — | 5.25 | Vdc |
| Short Circuit Current ($V_{ref}$ = 0 V, $T_J$ = +25°C) | $I_{SC}$ | — | 80 | 100 | — | 80 | 100 | mA |
| Output Noise Voltage (10 Hz ≤ f ≤ 10 kHz, $T_J$ = +25°C) | $V_n$ | — | 40 | 200 | — | 40 | 200 | $\mu V_{rms}$ |
| Long Term Stability ($T_J$ = +125°C) (Note 5) | S | — | 20 | 50 | — | 20 | 50 | mV/khr |
| **OSCILLATOR SECTION** (Note 6, unless otherwise specified) | | | | | | | | |
| Initial Accuracy ($T_J$ = +25°C) | — | — | ±2.0 | ±6.0 | — | ±2.0 | ±6.0 | % |
| Frequency Stability with Voltage (+8.0 V ≤ $V_{CC}$ ≤ +35 V) | $\frac{\Delta f_{osc}}{\Delta V_{CC}}$ | — | ±0.3 | ±1.0 | — | ±1.0 | ±2.0 | % |
| Frequency Stability with Temperature | $\frac{\Delta f_{osc}}{\Delta T}$ | — | ±3.0 | ±6.0 | — | ±3.0 | ±6.0 | % |
| Minimum Frequency ($R_T$ = 150 kΩ, $C_T$ = 0.2 μF) | $f_{min}$ | — | — | 100 | — | — | 100 | Hz |
| Maximum Frequency ($R_T$ = 2.0 kΩ, $C_T$ = 1.0 nF) | $f_{max}$ | 400 | — | — | 400 | — | — | kHz |
| Current Mirror ($I_{RT}$ = 2.0 mA) | — | 1.7 | 2.0 | 2.2 | 1.7 | 2.0 | 2.2 | mA |
| Clock Amplitude | — | 3.0 | 3.5 | — | 3.0 | 3.5 | — | V |
| Clock Width ($T_J$ = +25°C) | — | 0.3 | 0.5 | 1.0 | 0.3 | 0.5 | 1.0 | μs |
| Sync Threshold | — | 1.2 | 2.0 | 2.8 | 1.2 | 2.0 | 2.8 | V |
| Sync Input Current (Sync Voltage = +3.5 V) | — | — | 1.0 | 2.5 | — | 1.0 | 2.5 | mA |
| **ERROR AMPLIFIER SECTION** ($V_{CM}$ = +5.1 V) | | | | | | | | |
| Input Offset Voltage | $V_{IO}$ | — | 0.5 | 5.0 | — | 2.0 | 10 | mV |
| Input Bias Current | $I_{IB}$ | — | 1.0 | 10 | — | 1.0 | 10 | μA |
| Input Offset Current | $I_{IO}$ | — | — | 1.0 | — | — | 1.0 | μA |
| DC Open Loop Gain ($R_L$ ≥ 10 MΩ) | $A_{VOL}$ | 60 | 75 | — | 60 | 75 | — | dB |
| Low Level Output Voltage | $V_{OL}$ | — | 0.2 | 0.5 | — | 0.2 | 0.5 | V |
| High Level Output Voltage | $V_{OH}$ | 3.8 | 5.6 | — | 3.8 | 5.6 | — | V |
| Common Mode Rejection Ratio (+1.5 V ≤ $V_{CM}$ ≤ +5.2 V) | CMRR | 60 | 75 | — | 60. | 75 | — | dB |
| Power Supply Rejection Ratio (+8.0 V ≤ $V_{CC}$ ≤ +35 V) | PSRR | 50 | 60 | — | 50 | 60 | — | dB |
| **PWM COMPARATOR SECTION** | | | | | | | | |
| Minimum Duty Cycle | $DC_{min}$ | — | — | 0 | — | — | 0 | % |
| Maximum Duty Cycle | $DC_{max}$ | 45 | 49 | — | 45 | 49 | — | % |
| Input Threshold, Zero Duty Cycle (Note 6) | $V_{TH}$ | 0.6 | 0.9 | — | 0.6 | 0.9 | — | V |
| Input Threshold, Maximum Duty Cycle (Note 6) | $V_{TH}$ | — | 3.3 | 3.6 | — | 3.3 | 3.6 | V |
| Input Bias Current | $I_{IB}$ | — | 0.05 | 1.0 | — | 0.05 | 1.0 | μA |

**ELECTRICAL CHARACTERISTICS** (Continued)

| Characteristic | Symbol | SG1525A/2525A<br>SG1527A/2527A Min | Typ | Max | SG3525A<br>SG3527A Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| **SOFT-START SECTION** | | | | | | | | |
| Soft-Start Current ($V_{shutdown}$ = 0 V) | — | 25 | 50 | 80 | 25 | 50 | 80 | μA |
| Soft-Start Voltage ($V_{shutdown}$ = 2.0 V) | — | — | 0.4 | 0.6 | — | 0.4 | 0.6 | V |
| Shutdown Input Current ($V_{shutdown}$ = 2.5 V) | — | — | 0.4 | 1.0 | — | 0.4 | 1.0 | mA |
| **OUTPUT DRIVERS** (Each Output, $V_{CC}$ = +20 V) | | | | | | | | |
| Output Low Level | $V_{OL}$ | | | | | | | V |
| ($I_{sink}$ = 20 mA) | | — | 0.2 | 0.4 | — | 0.2 | 0.4 | |
| ($I_{sink}$ = 100 mA) | | — | 1.0 | 2.0 | — | 1.0 | 2.0 | |
| Output High Level | $V_{OH}$ | | | | | | | V |
| ($I_{source}$ = 20 mA) | | 18 | 19 | — | 18 | 19 | — | |
| ($I_{source}$ = 100 mA) | | 17 | 18 | — | 17 | 18 | — | |
| Under Voltage Lockout (V8 and V9 = High) | $V_{UL}$ | 6.0 | 7.0 | 8.0 | 6.0 | 7.0 | 8.0 | V |
| Collector Leakage, $V_C$ = +35 V (Note 7) | $I_{C(leak)}$ | — | — | 200 | — | — | 200 | μA |
| Rise Time ($C_L$ = 1.0 nF, $T_J$ = 25°C) | $t_r$ | — | 100 | 600 | — | 100 | 600 | ns |
| Fall Time ($C_L$ = 1.0 nF, $T_J$ = 25°C) | $t_f$ | — | 50 | 300 | — | 50 | 300 | ns |
| Shutdown Delay ($V_{SD}$ = +3.0 V, $C_S$ = 0, $T_J$ = +25°C) | $t_{ds}$ | — | 0.2 | 0.5 | — | 0.2 | 0.5 | μs |
| Supply Current, ($V_{CC}$ = +35 V) | $I_{CC}$ | — | 14 | 20 | — | 14 | 20 | mA |

**NOTES:**

4. $T_{low}$ = −55°C for SG1525A/1527A
−25°C for SG2525A/2527A
0°C for SG3525A/3527A

$T_{high}$ = +125°C for SG1525A/1527A
+85°C for SG2525A/2527A
+70°C for SG3525A/3527A

5. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Tested at $f_{osc}$ = 40 kHz ($R_T$ = 3.6 kΩ, $C_T$ = 0.01 μF, $R_D$ = 0 Ω).
7. Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.

## APPLICATION INFORMATION

### SHUTDOWN OPTIONS
### (See Block Diagram, front page)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150 μA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

## TYPICAL CHARACTERISTICS

**FIGURE 1 — SG1525A OSCILLATOR SCHEMATIC**

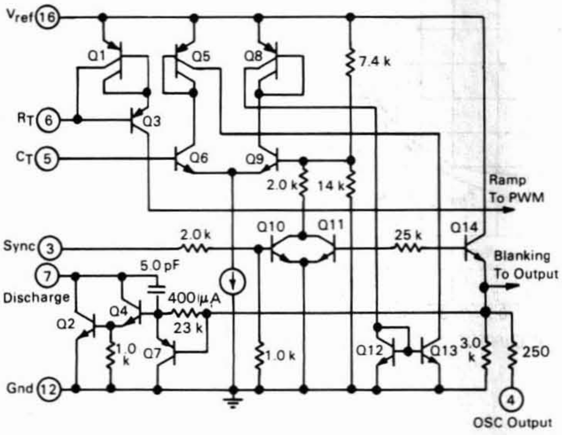

Vref 16
Q1
Q5
Q8
7.4 k
RT 6
Q3
CT 5
Q6
Q9
2.0 k
14 k
Ramp To PWM
Sync 3
2.0 k
Q10
Q11
25 k
Q14
Blanking To Output
7 Discharge
5.0 pF
400 µA
Q2
Q4
23 k
1.0 k
Q7
1.0 k
Q12
Q13
3.0 k
250
Gnd 12
4 OSC Output

**FIGURE 2 — OSCILLATOR CHARGE TIME versus $R_T$**

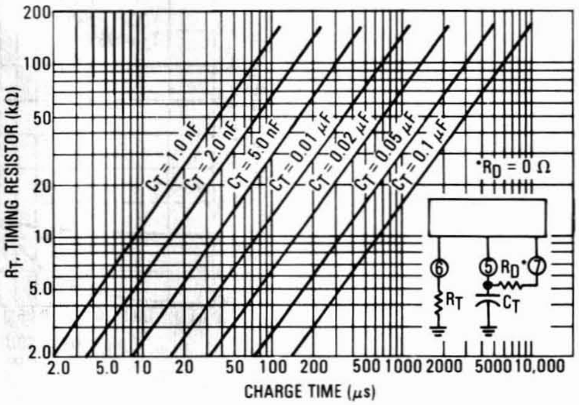


**FIGURE 3 — OSCILLATOR DISCHARGE TIME versus $R_D$**

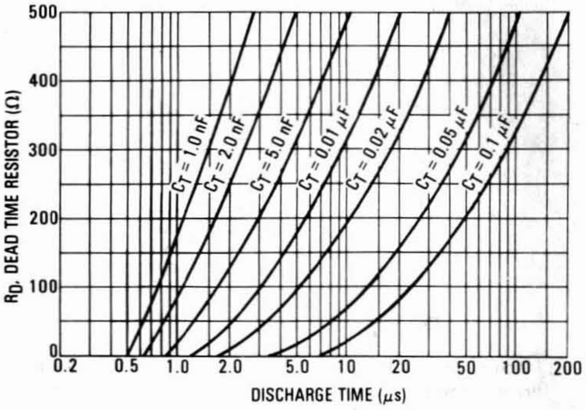


**FIGURE 4 — SG1525A ERROR AMPLIFIER SCHEMATIC**

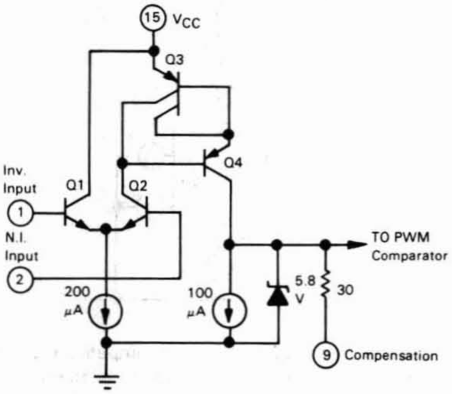

15 VCC
Q3
Q4
Inv. Input
Q1
Q2
1
N.I. Input
2
200 µA
100 µA
5.8 V
30
TO PWM Comparator
9 Compensation

**FIGURE 5 — ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE**

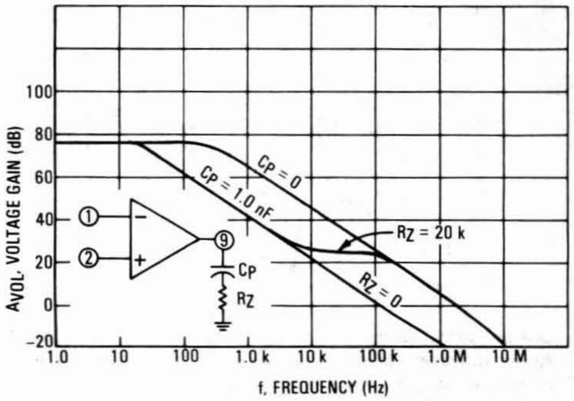


**FIGURE 6 — SG1525A OUTPUT CIRCUIT (1/2 CIRCUIT SHOWN)**

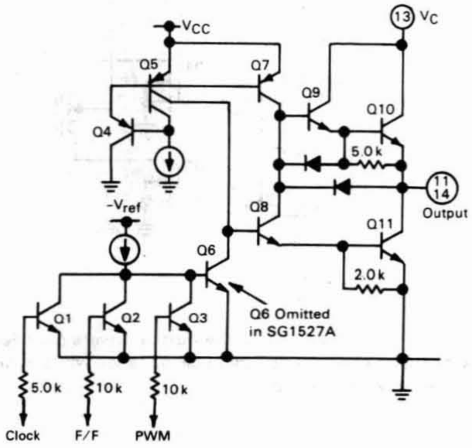

13 VC
VCC
Q5
Q7
Q4
Q9
Q10
5.0 k
11 14 Output
−Vref
Q8
Q11
Q6
2.0 k
Q1
Q2
Q3
Q6 Omitted in SG1527A
5.0 k
10 k
10 k
Clock
F/F
PWM

FIGURE 7 — SG1525A/2525A/3525A
OUTPUT SATURATION CHARACTERISTICS

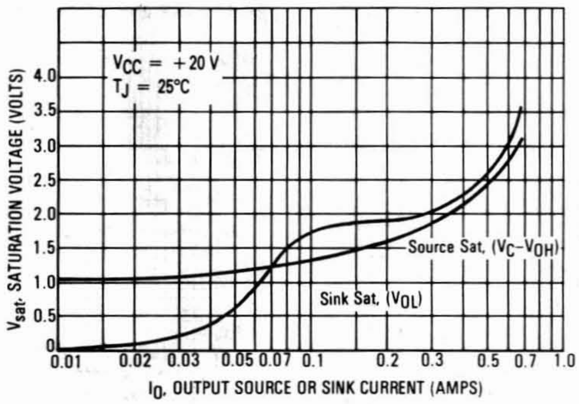
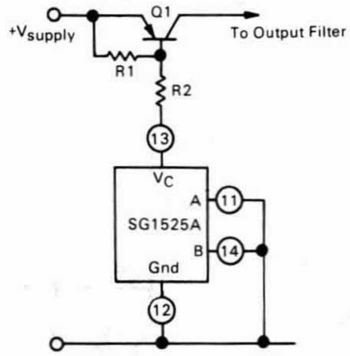
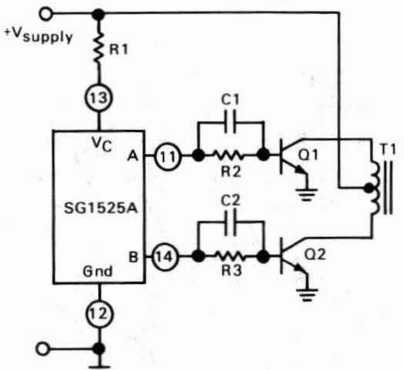


FIGURE 8 — SINGLE ENDED SUPPLY


+$V_{supply}$
Q1
To Output Filter
R1
R2
13
$V_C$
A
11
SG1525A
B
14
Gnd
12

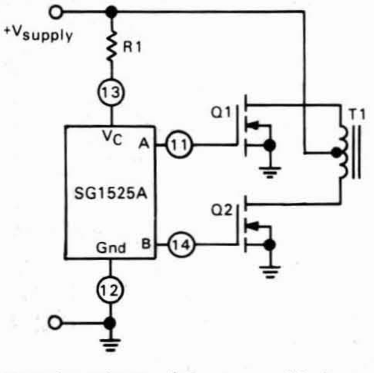
For single-ended supplies, the driver outputs are grounded. The $V_C$ terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

FIGURE 9 — PUSH-PULL CONFIGURATION


+$V_{supply}$
R1
13
C1
$V_C$
A
11
R2
Q1
T1
SG1525A
C2
B
14
R3
Q2
Gnd
12

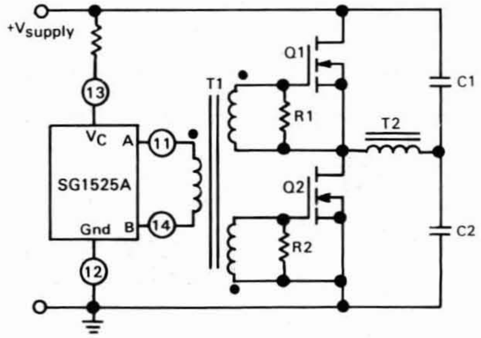
In conventional push-pull bipolar designs, forward base drive is controlled by R1–R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

FIGURE 10 — DRIVING POWER FETS


+$V_{supply}$
R1
13
Q1
T1
$V_C$
A
11
SG1525A
Q2
Gnd
B
14
12

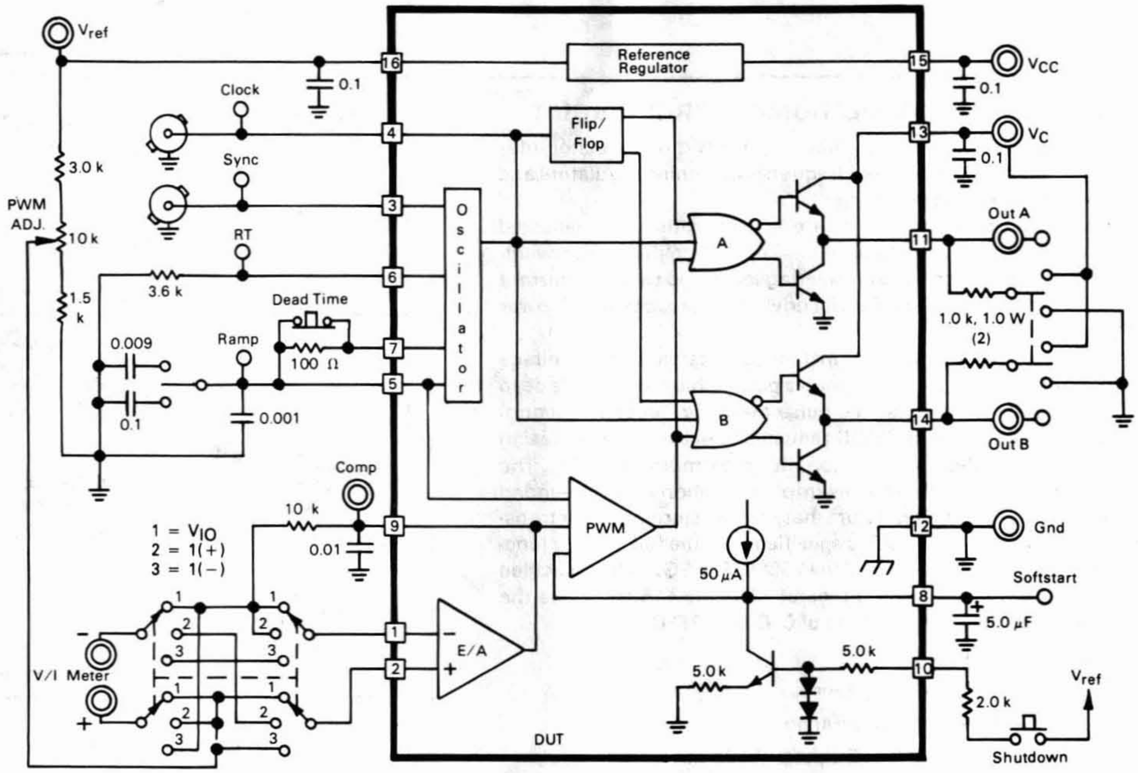
The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

FIGURE 11 — DRIVING TRANSFORMERS IN A HALF-BRIDGE CONFIGURATION


+$V_{supply}$
Q1
C1
13
T1
R1
T2
$V_C$
A
11
SG1525A
Q2
Gnd
B
14
C2
R2
12

Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

**FIGURE 12 — LAB TEST FIXTURE**


Vref
0.1
Clock
Sync
3.0 k
PWM ADJ.
10 k
RT
3.6 k
1.5 k
Dead Time
0.009
Ramp
100 Ω
0.1
0.001
Comp
10 k
0.01
1 = VIO
2 = I(+)
3 = I(−)
V/I Meter
1
2
3
16
4
3
6
7
5
9
1
2
Reference Regulator
Flip/Flop
Oscillator
A
B
PWM
E/A
50 μA
5.0 k
5.0 k
DUT
15
13
11
14
12
8
10
VCC
0.1
VC
0.1
Out A
1.0 k, 1.0 W (2)
Out B
Gnd
Softstart
5.0 μF
Vref
2.0 k
Shutdown

**MOTOROLA**

# SG1526
# SG2526
# SG3526

## PULSE WIDTH MODULATION CONTROL CIRCUIT

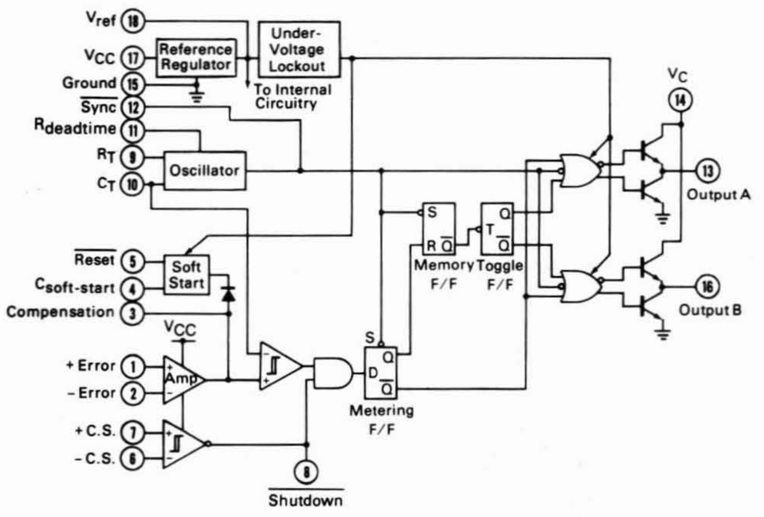
The SG1526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft-start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B-series CMOS compatible. Active low logic design allows easy wired-OR connections for maximum flexibility. The versatility of this device enables implementation in single-ended or push-pull switching regulators that are transformerless or transformer coupled. The SG1526 is specified over the full military junction temperature range of -55°C to +150°C. The SG2526 is specified over a junction temperature range of -40°C to +150°C while the SG3526 is specified over a range of 0°C to +125°C.

- 8.0 to 35 Volt Operation
- 5.0 Volt ±1% Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ±100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

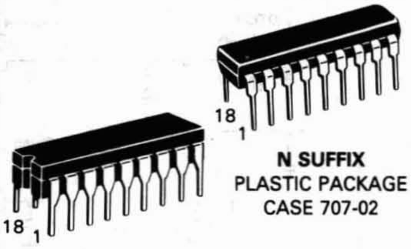
### BLOCK DIAGRAM



Vref ⑱
VCC ⑰
Ground ⑮
Sync ⑫
Rdeadtime ⑪
RT ⑨
CT ⑩
Reference Regulator
Under-Voltage Lockout
To Internal Circuitry
Oscillator
Reset ⑤
Csoft-start ④
Compensation ③
Soft Start
VCC
+ Error ①
- Error ②
Amp
+C.S. ⑦
-C.S. ⑥
S
D
Q
Q̄
Metering F/F
⑧
Shutdown
S
R
Q̄
Memory F/F
T
Q
Q̄
Toggle F/F
VC
⑭
⑬
Output A
⑯
Output B

## PULSE WIDTH MODULATION CONTROL CIRCUITS

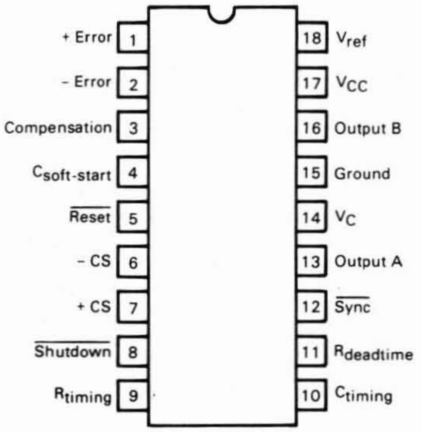
### SILICON MONOLITHIC INTEGRATED CIRCUITS



**N SUFFIX**
PLASTIC PACKAGE
CASE 707-02

**J SUFFIX**
CERAMIC PACKAGE
CASE 726-01

### PIN CONNECTIONS



+ Error 1
- Error 2
Compensation 3
Csoft-start 4
Reset 5
- CS 6
+ CS 7
Shutdown 8
Rtiming 9
18 Vref
17 VCC
16 Output B
15 Ground
14 VC
13 Output A
12 Sync
11 Rdeadtime
10 Ctiming

(Top View)

### ORDERING INFORMATION

| Device | Junction Temperature Range | Package |
|---|---|---|
| SG1526J | -55 to +150°C | Ceramic DIP |
| SG2526J<br>SG2526N | -40 to +150°C | Ceramic DIP<br>Plastic DIP |
| SG3526J<br>SG3526N | 0 to +125°C | Ceramic DIP<br>Plastic DIP |

**MAXIMUM RATINGS** (Note 1)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | +40 | Vdc |
| Collector Supply Voltage | $V_C$ | +40 | Vdc |
| Logic Inputs | — | -0.3 to +5.5 | V |
| Analog Inputs | — | -0.3 to $V_{CC}$ | V |
| Output Current, Source or Sink | $I_O$ | ±200 | mA |
| Reference Output Current | $I_{ref}$ | 50 | mA |
| Logic Sink Current | — | 15 | mA |
| Power Dissipation (Plastic & Ceramic Package)<br>Note 2, $T_A$ = +25°C<br>Note 3, $T_C$ = +25°C | $P_D$ | <br>1000<br>3000 | mW |
| Thermal Resistance Junction to Air (Plastic and Ceramic Package) | $R_{\theta JA}$ | 100 | °C/W |
| Thermal Resistance Junction to Case (Plastic and Ceramic Package) | $R_{\theta JC}$ | 42 | °C/W |
| Operating Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Lead Temperature (Soldering, 10 Seconds) | $T_{Solder}$ | +300 | °C |

Notes:
1. Values beyond which damage may occur
2. Derate at 10 mW/°C for ambient temperatures above +50°C
3. Derate at 24 mW/°C for case temperatures above +25°C

**RECOMMENDED OPERATING CONDITIONS**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | +8.0 | +35 | Vdc |
| Collector Supply Voltage | $V_C$ | +4.5 | +35 | Vdc |
| Output Sink/Source Current (Each Output) | $I_O$ | 0 | ±100 | mA |
| Reference Load Current | $I_{ref}$ | 0 | 20 | mA |
| Oscillator Frequency Range | $f_{osc}$ | 0.001 | 400 | kHz |
| Oscillator Timing Resistor | $R_T$ | 2.0 | 150 | kΩ |
| Oscillator Timing Capacitor | $C_T$ | 0.001 | 20 | μF |
| Available Deadtime Range (40 kHz) | | 3.0 | 50 | % |
| Operating Junction Temperature Range<br>SG1526<br>SG2526<br>SG3526 | $T_J$ | <br>-55<br>-40<br>0 | <br>+150<br>+150<br>+125 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +15 Vdc, $T_J$ = $T_{low}$ to $T_{high}$ [Note 4] unless otherwise specified)

| Characteristic | Symbol | SG1526/2526 | | | SG3526 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **REFERENCE SECTION** (Note 5) | | | | | | | | |
| Reference Output Voltage ($T_J$ = +25°C) | $V_{ref}$ | 4.95 | 5.00 | 5.05 | 4.90 | 5.00 | 5.10 | V |
| Line Regulation (+8.0 V ≤ $V_{CC}$ ≤ +35 V) | $Reg_{line}$ | — | 10 | 20 | — | 10 | 30 | mV |
| Load Regulation, 0 mA ≤ $I_L$ ≤ 20 mA | $Reg_{load}$ | — | 10 | 30 | — | 10 | 50 | mV |
| Temperature Stability | $\Delta V_{ref}/\Delta T_J$ | — | 15 | 50 | — | 15 | 50 | mV |
| Total Reference Output Voltage Variation (+8.0 V ≤ $V_{CC}$ ≤ +35 V, 0 mA ≤ $I_L$ ≤ 20 mA) | $\Delta V_{ref}$ | 4.90 | 5.00 | 5.10 | 4.85 | 5.00 | 5.15 | V |
| Short Circuit Current ($V_{ref}$ = 0 V) | $I_{SC}$ | 25 | 50 | 100 | 25 | 50 | 100 | mA |
| **UNDERVOLTAGE LOCKOUT** | | | | | | | | |
| $\overline{\text{Reset}}$ Output Voltage ($V_{ref}$ = +3.8 V) | — | — | 0.2 | 0.4 | — | 0.2 | 0.4 | V |
| $\overline{\text{Reset}}$ Output Voltage ($V_{ref}$ = +4.8 V) | — | 2.4 | 4.8 | — | 2.4 | 4.8 | — | V |
| **OSCILLATOR SECTION** (Note 6) | | | | | | | | |
| Initial Accuracy ($T_J$ = +25°C) | — | — | ±3.0 | ±8.0 | — | ±3.0 | ±8.0 | % |
| Frequency Stability over Power Supply Range (+8.0 V ≤ $V_{CC}$ ≤ +35 V) | $\frac{\Delta f_{osc}}{\Delta V_{CC}}$ | — | 0.5 | 1.0 | — | 0.5 | 1.0 | % |
| Frequency Stability over Temperature ($\Delta T_J$ = $T_{low}$ to $T_{high}$) | $\frac{\Delta f_{osc}}{\Delta T_J}$ | — | 7.0 | 10 | — | 3.0 | 5.0 | % |
| Minimum Frequency ($R_T$ = 150 kΩ, $C_T$ = 20 μF) | $f_{min}$ | — | — | 1.0 | — | — | 1.0 | Hz |
| Maximum Frequency ($R_T$ = 2.0 kΩ, $C_T$ = 0.001 μF) | $f_{max}$ | 400 | — | — | 400 | — | — | kHz |
| Sawtooth Peak Voltage ($V_{CC}$ = +35 V) | $V_{osc(P)}$ | — | 3.0 | 3.5 | — | 3.0 | 3.5 | V |
| Sawtooth Valley Voltage ($V_{CC}$ = +8.0 V) | $V_{osc(V)}$ | 0.5 | 1.0 | — | 0.5 | 1.0 | — | V |
| **ERROR AMPLIFIER SECTION** (Note 7) | | | | | | | | |
| Input Offset Voltage ($R_S$ ≤ 2.0 kΩ) | $V_{IO}$ | — | 2.0 | 5.0 | — | 2.0 | 10 | mV |
| Input Bias Current | $I_{IB}$ | — | −350 | −1000 | — | −350 | −2000 | nA |
| Input Offset Current | $I_{IO}$ | — | 35 | 100 | — | 35 | 200 | nA |
| DC Open Loop Gain ($R_L$ ≥ 10 MΩ) | $A_{Vol}$ | 64 | 72 | — | 60 | 72 | — | dB |
| High Output Voltage ($V_{Pin\ 1}-V_{Pin\ 2} \geq +150$ mV, $I_{source}$ = 100 μA) | $V_{OH}$ | 3.6 | 4.2 | — | 3.6 | 4.2 | — | V |
| Low Output Voltage ($V_{Pin\ 2}-V_{Pin\ 1} \geq +150$ mV, $I_{sink}$ = 100 μA) | $V_{OL}$ | — | 0.2 | 0.4 | — | 0.2 | 0.4 | V |
| Common Mode Rejection Ratio ($R_S$ ≤ 2.0 kΩ) | CMRR | 70 | 94 | — | 70 | 94 | — | dB |
| Power Supply Rejection Ratio (+12 V ≤ $V_{CC}$ ≤ +18 V) | PSRR | 66 | 80 | — | 66 | 80 | — | dB |
| **PWM COMPARATOR SECTION** (Note 6) | | | | | | | | |
| Minimum Duty Cycle ($V_{compensation}$ = +0.4 V) | $DC_{min}$ | — | — | 0 | — | — | 0 | % |
| Maximum Duty Cycle ($V_{compensation}$ = +3.6 V) | $DC_{max}$ | 45 | 49 | — | 45 | 49 | — | % |

**ELECTRICAL CHARACTERISTICS** (Continued)

| Characteristic | Symbol | SG1526/2526 | | | SG3526 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **DIGITAL PORTS ($\overline{\text{SYNC}}$, $\overline{\text{SHUTDOWN}}$, $\overline{\text{RESET}}$)** | | | | | | | | |
| Output Voltage — High Logic Level ($I_{source}$ = 40 μA) | $V_{OH}$ | 2.4 | 4.0 | — | 2.4 | 4.0 | — | V |
| Output Voltage — Low Logic Level ($I_{sink}$ = 3.6 mA) | $V_{OL}$ | — | 0.2 | 0.4 | — | 0.2 | 0.4 | V |
| Input Current — High Logic Level ($V_{IH}$ = +2.4 V) | $I_{IH}$ | — | -125 | -200 | — | -125 | -200 | μA |
| Input Current — Low Logic Level ($V_{IL}$ = +0.4 V) | $I_{IL}$ | — | -225 | -360 | — | -225 | -360 | μA |
| **CURRENT LIMIT COMPARATOR SECTION** (Note 8) | | | | | | | | |
| Sense Voltage ($R_S \leqslant 50\ \Omega$) | $V_{sense}$ | 90 | 100 | 110 | 80 | 100 | 120 | mV |
| Input Bias Current | $I_{IB}$ | — | -3.0 | -10 | — | -3.0 | -10 | μA |
| **SOFT-START SECTION** | | | | | | | | |
| Error Clamp Voltage ($\overline{\text{Reset}}$ = +0.4 V) | — | — | 0.1 | 0.4 | — | 0.1 | 0.4 | V |
| $C_{Soft\text{-}Start}$ Charging Current ($\overline{\text{Reset}}$ = +2.4 V) | $I_{CS}$ | 50 | 100 | 150 | 50 | 100 | 150 | μA |
| **OUTPUT DRIVERS** (Each Output, $V_C$ = +15 Vdc unless otherwise specified) | | | | | | | | |
| Output High Level<br>$I_{source}$ = 20 mA<br>$I_{source}$ = 100 mA | $V_{OH}$ | <br>12.5<br>12 | <br>13.5<br>13 | <br>—<br>— | <br>12.5<br>12 | <br>13.5<br>13 | <br>—<br>— | V |
| Output Low Level<br>$I_{sink}$ = 20 mA<br>$I_{sink}$ = 100 mA | $V_{OL}$ | <br>—<br>— | <br>0.2<br>1.2 | <br>0.3<br>2.0 | <br>—<br>— | <br>0.2<br>1.2 | <br>0.3<br>2.0 | V |
| Collector Leakage, $V_C$ = +40 V | $I_{C(leak)}$ | — | 50 | 150 | — | 50 | 150 | μA |
| Rise Time ($C_L$ = 1000 pF) | $t_r$ | — | 0.3 | 0.6 | — | 0.3 | 0.6 | μs |
| Fall Time ($C_L$ = 1000 pF) | $t_f$ | — | 0.1 | 0.2 | — | 0.1 | 0.2 | μs |
| Supply Current ($\overline{\text{Shutdown}}$ = +0.4 V, $V_{CC}$ = +35 V, $R_T$ = 4.12 kΩ) | $I_{CC}$ | — | 18 | 30 | — | 18 | 30 | mA |

Notes:

4. $T_{low}$ = -55°C for SG1526
   -40°C for SG2526
   0°C for SG3526
   $T_{high}$ = +150°C for SG1526/2526
   +125°C for SG3526
5. $I_L$ = 0 mA unless otherwise noted.
6. $f_{osc}$ = 40 kHz ($R_T$ = 4.12 kΩ ±1%, $C_T$ = 0.01 μF ±1%, $R_D$ = 0 Ω)
7. $0\ V \leqslant V_{CM} \leqslant +5.2\ V$
8. $0\ V \leqslant V_{CM} \leqslant +12\ V$

## TYPICAL CHARACTERISTICS

FIGURE 1 — SG1526 REFERENCE STABILITY OVER TEMPERATURE

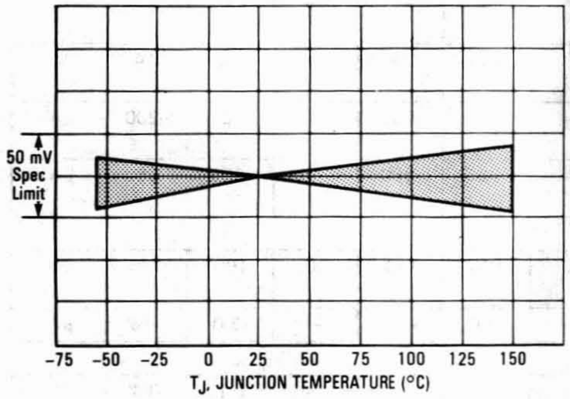


FIGURE 2 — REFERENCE VOLTAGE AS A FUNCTION SUPPLY VOLTAGE

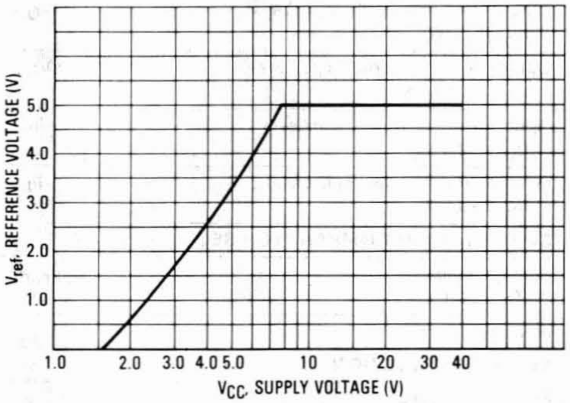


FIGURE 3 — ERROR AMPLIFIER OPEN LOOP FREQUENCY RESPONSE

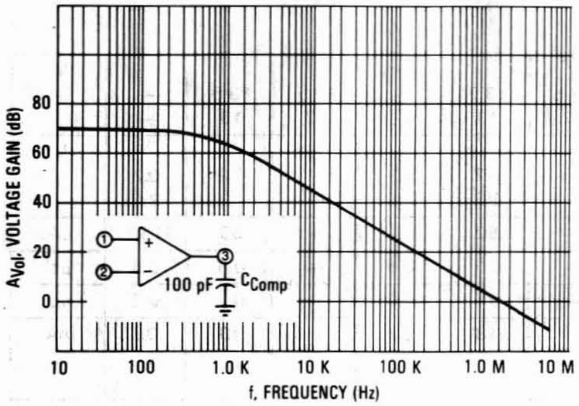


FIGURE 4 — CURRENT LIMIT COMPARATOR THRESHOLD

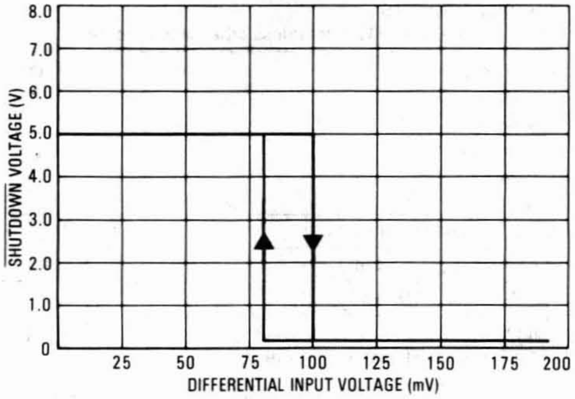


FIGURE 5 — UNDERVOLTAGE LOCKOUT CHARACTERISTIC

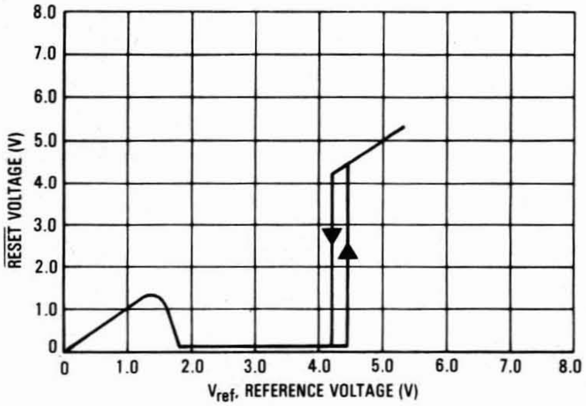


FIGURE 6 — OUTPUT DRIVER SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT

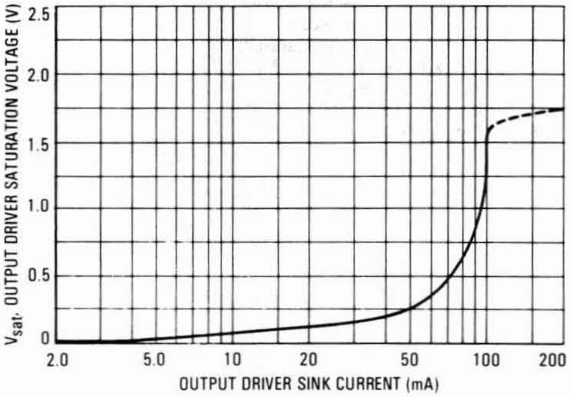


FIGURE 7 — $V_C$ SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT

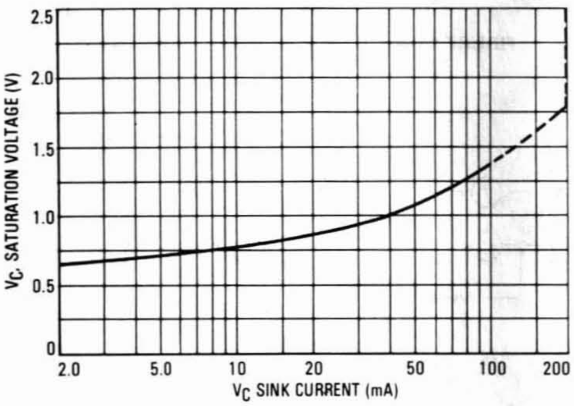


FIGURE 8 — SG1526 OSCILLATOR PERIOD

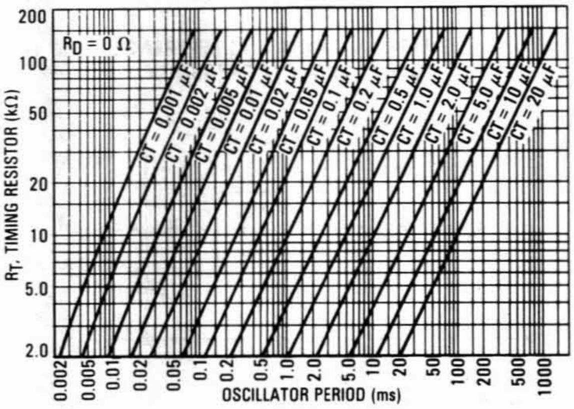


FIGURE 9 — OUTPUT DEADTIME AS A FUNCTION OF DEADTIME RESISTOR VALUE

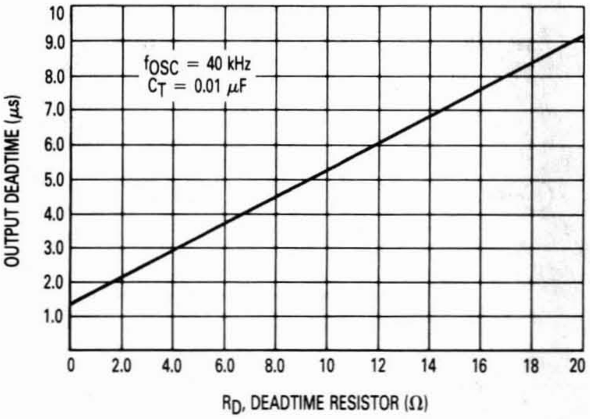


FIGURE 10 — SG1526 ERROR AMPLIFIER

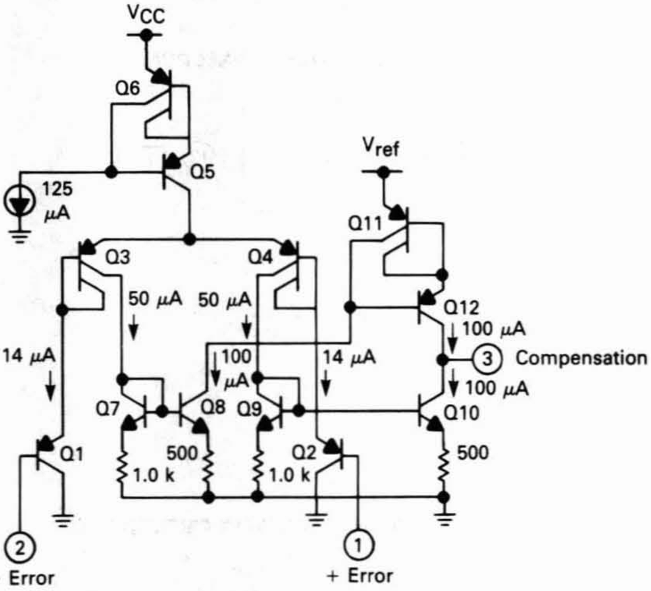

$V_{CC}$
Q6
Q5
125 µA
Q3
Q4
$V_{ref}$
Q11
Q12
50 µA
50 µA
14 µA
100 µA
14 µA
100 µA
3
Compensation
100 µA
Q7
Q8
Q9
Q10
Q1
500
1.0 k
1.0 k
Q2
500
2
− Error
1
+ Error

FIGURE 11 — SG1526 UNDERVOLTAGE LOCKOUT

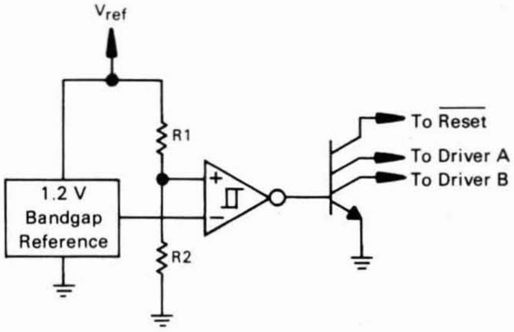
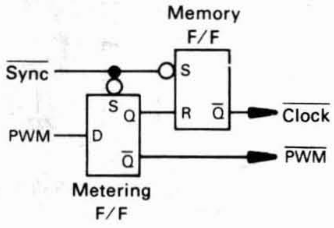

$V_{ref}$
R1
R2
1.2 V Bandgap Reference
+
−
To $\overline{\text{Reset}}$
To Driver A
To Driver B

FIGURE 12 — SG1526 PULSE PROCESSING LOGIC

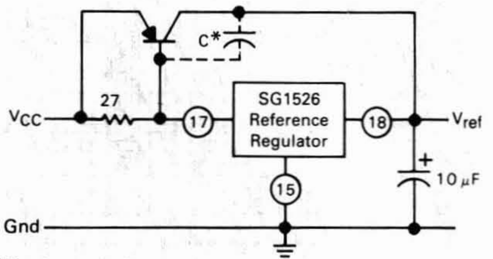

Memory F/F
$\overline{\text{Sync}}$
S
R
$\overline{Q}$
$\overline{\text{Clock}}$
S
Q
PWM
D
$\overline{Q}$
$\overline{\text{PWM}}$
Metering F/F

The metering FLIP-FLOP is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory FLIP-FLOP prevents double pulsing in a push-pull configuration by remembering which output produced the last pulse.

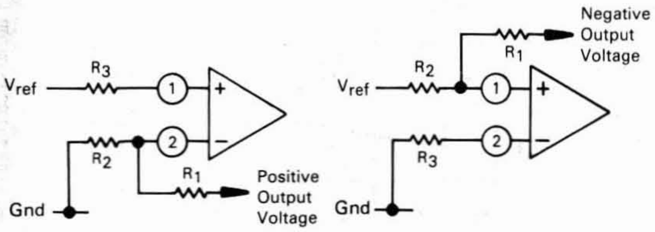
## APPLICATIONS INFORMATION

FIGURE 13 — EXTENDING REFERENCE OUTPUT CURRENT CAPABILITY


C*
27
VCC
17
SG1526
Reference
Regulator
18
Vref
15
10 μF
Gnd

*May be required with some types of transistors

FIGURE 14 — ERROR AMPLIFIER CONNECTIONS


Vref
R3
1
2
R2
R1
Gnd
Positive
Output
Voltage
Negative
Output
Voltage
R1
R2
Vref
1
2
R3
Gnd

$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R2}\right)$

$V_{out} = V_{ref}\left(\frac{R_1}{R2}\right)$

$R_3 = \left(\frac{R_1R_2}{R_1 + R_2}\right)$

FIGURE 15 — OSCILLATOR CONNECTIONS

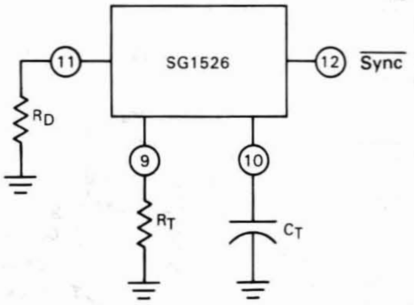
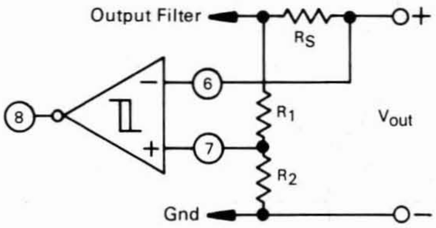

11
SG1526
12
Sync
RD
9
10
RT
CT

FIGURE 16 — FOLDBACK CURRENT LIMITING


Output Filter
RS
+
6
R1
Vout
8
7
R2
Gnd
−

$I_{max} = \frac{\left(0.1\ V + \frac{V_{out}\ R_1}{R1\ +\ R2}\right)}{R_S}$

$I_{SC} = \left(\frac{0.1\ V}{R_S}\right)$

FIGURE 17 — SG1526 SOFT-START CIRCUITRY

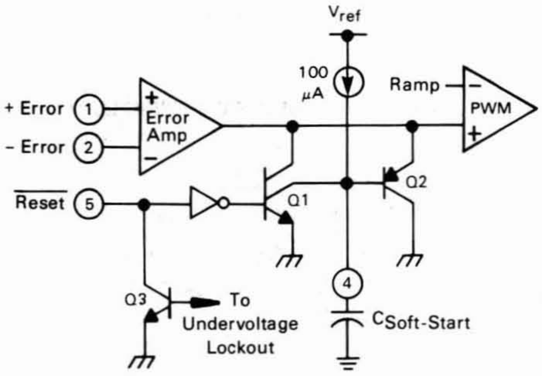
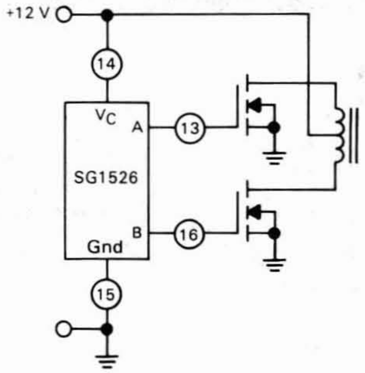

Vref
100 μA
Ramp
PWM
+ Error
1
− Error
2
Error
Amp
Reset
5
Q1
Q2
Q3
To
Undervoltage
Lockout
4
CSoft-Start

FIGURE 18 — DRIVING TMOS POWER FETS


+12 V
14
VC
A
13
SG1526
Gnd
B
16
15

The totem-pole output drivers of the SG1526 are ideally suited for driving the input capacitance of power FETs at high speeds.

FIGURE 19 — HALF-BRIDGE CONFIGURATION

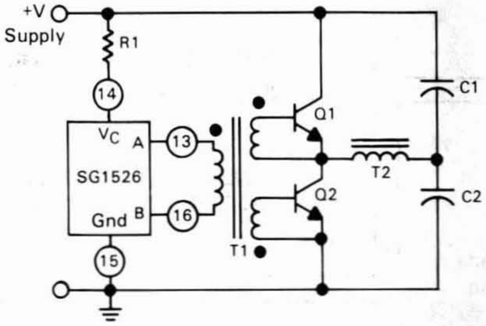
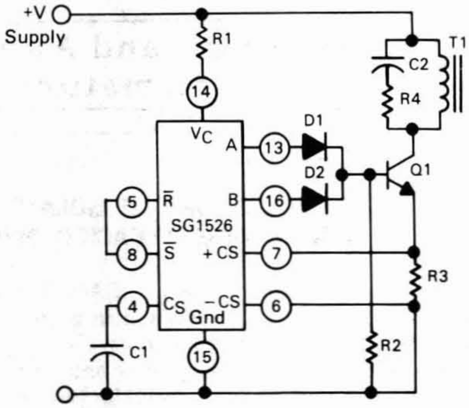

+V
Supply
R1
14
VC
A
13
SG1526
Gnd
B
16
15
Q1
Q2
T1
T2
C1
C2

FIGURE 20 — FLYBACK CONVERTER WITH CURRENT LIMITING


+V
Supply
R1
14
T1
C2
R4
D1
D2
VC
A
13
Q1
5
R̄
B
16
SG1526
8
S̄
+CS
7
R3
4
CS
−CS
Gnd
6
C1
15
R2

In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft-start capacitor.

FIGURE 21 — SINGLE-ENDED CONFIGURATION

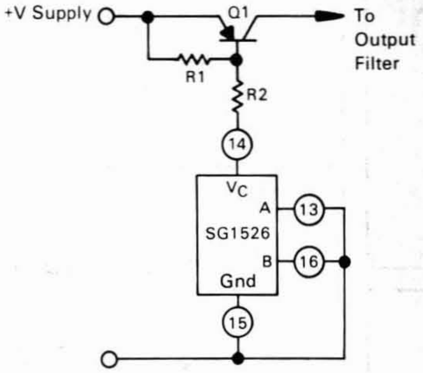
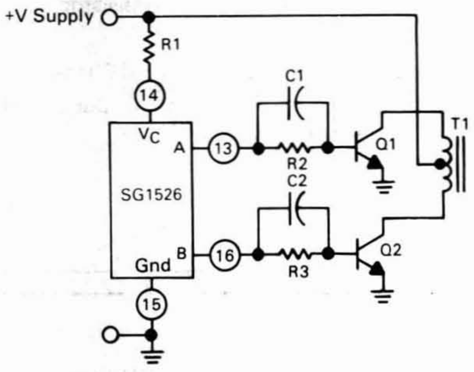

+V Supply
Q1
To
Output
Filter
R1
R2
14
VC
A
13
SG1526
B
16
Gnd
15

FIGURE 22 — PUSH-PULL CONFIGURATION


+V Supply
R1
14
C1
T1
VC
A
13
Q1
R2
C2
SG1526
Gnd
B
16
Q2
R3
15

**MOTOROLA**

# TDA4600

## Specifications and Applications Information

### CONTROL IC FOR LINE ISOLATED FREELY OSCILLATING FLYBACK CONVERTER

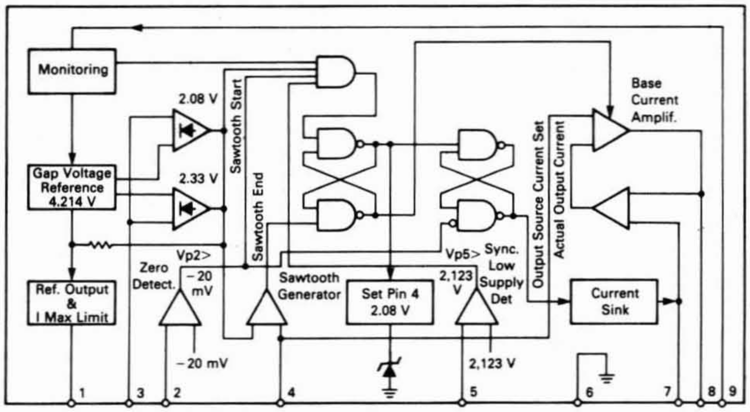
The bipolar integrated circuit TDA4600 drives, regulates and monitors the switching transistor in a power supply based on freely oscillating flyback converters.

Due to the wide regulating range and the high voltage stability during large load changes, SMPS for Hi-Fi equipment and active loudspeakers can be realized as well as applications in TV receivers and video recorders.

The TDA4600 is available in a 9-pin SIP plastic medium-power package. The ambient temperature during operation can be from −15°C to +85°C.

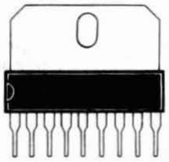
- Wide Operational Range
- High Voltage Stability Even at High Load Changes
- Direct Control of Switching Transistor
- Low Start-Up Current
- Linear Foldback of the Overload Characteristic
- Base Drive Proportional to the Current Through the Power Switching Transistor

### BLOCK DIAGRAM


Monitoring
2.08 V
2.33 V
Sawtooth Start
Sawtooth End
Gap Voltage Reference 4.214 V
Vp2>
Zero Detect.
−20 mV
Ref. Output & I Max Limit
Sawtooth Generator
Set Pin 4 2.08 V
Vp5>
Sync. Low Supply Det
2,123 V
Output Source Current Set
Actual Output Current
Base Current Amplif.
Current Sink
−20 mV
2,123 V
1
3
2
4
5
6
7
8
9

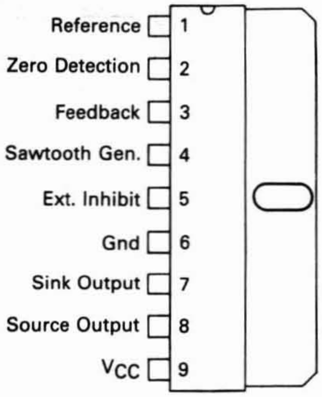
### FLYBACK CONVERTER REGULATOR CONTROL CIRCUIT

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**SIP 9**
PLASTIC
MEDIUM-POWER PACKAGE
CASE 762-01

### PIN CONNECTIONS


Reference 1
Zero Detection 2
Feedback 3
Sawtooth Gen. 4
Ext. Inhibit 5
Gnd 6
Sink Output 7
Source Output 8
VCC 9

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| TDA4600 | −15°C to +85°C | Plastic SIP |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_9$ | 20 | V |
| Sink Output Voltage | $V_7$ | 0 to $V_9$ | V |
| Source Output | $V_8$<br>$V_7$-$V_8$ | 0 to $V_9$<br>±6.0 | V |
| Reference Output | $I_1$ | −10 to +1.0 | mA |
| Zero Passage | $I_2$ | −3.0 to +3.0 | mA |
| Control Amplifier | $I_3$ | −3.0 to 0 | mA |
| Collector Current Balancing | $I_4$ | −2.0 to +5.0 | mA |
| Trigger Input | $I_5$ | −2.0 to +3.0 | mA |
| Sink Output Current | $I_7$ | −1.5 | A |
| Source Output Current | $I_8$ | 1.5 | A |
| Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature | $T_{stg}$ | −40 to +125 | °C |
| Thermal Resistance (Junction-to-Air) | $R_{\theta JA}$ | 70 | °C/W |
| Thermal Resistance (Junction-to-Case) | $R_{\theta JC}$ | 15 | °C/W |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = +25°C unless otherwise noted.)

| Operating Conditions | Symbol | Fig. | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_9$ | | — | — | 18 | V |
| Ambient Temperature | $T_A$ | | −15 | — | 85 | °C |

**START OPERATION**

| | | | | | | |
|---|---|---|---|---|---|---|
| Current Consumption ($V_1$ not yet switched) | $I_9$ | 1 | — | — | 0.5 | mA |
| $V_9$ = 3.0 V | $I_9$ | 1 | — | 1.5 | 2.0 | mA |
| $V_9$ = 5.0 V | $I_9$ | 1 | — | 2.4 | 3.2 | mA |
| $V_9$ = 10 V | $V_9$ | 1 | 11.3 | 11.8 | 12.3 | V |
| Turn-on Point for $V_1$ | | | | | | |

**NORMAL OPERATION** ($V_9$ = 10 V; $V_{reg}$ = −10 V; $V_{pulse}$ = ±0.5 V; f = 20 kHz; duty cycle: ½ after the turn-on process is completed.)

| | | | | | | |
|---|---|---|---|---|---|---|
| Current Consumption $V_{reg}$ = −10 V | $I_9$ | 1 | 110 | 135 | 160 | mA |
| $V_{reg}$ = 0 | $I_9$ | 1 | 55 | 85 | 110 | |
| Reference Voltage $V_1$ < 0.1 mA | $V_1$ | 1 | 4.0 | 4.2 | 4.5 | V |
| $V_1$ = 5.0 mA | $V_1$ | 1 | 4.0 | 4.2 | 4.4 | |
| Reference Voltage Temperature Coefficient | $TC_1$ | 1 | — | 100 | — | ppm/°C |
| Feedback Voltage | $V_2$* | 1 | — | 0.2 | — | V |
| Regulating Voltage $V_{reg}$ = 0 V | $V_3$ | 1 | 2.3 | 2.6 | 2.9 | V |
| Collector Current Balancing Voltage | | | | | | V |
| $V_{reg}$ = 0 V | $V_4$* | 1 | 1.8 | 2.2 | 2.5 | |
| $V_{reg}$ = 0 V/−10 V | $\Delta V_4$* | 1 | 0.3 | 0.4 | 0.5 | |
| Max Trigger Input Voltages Limitation | $V_5$ | 1 | 5.5 | 6.3 | 7.0 | V |
| Output Voltages | | | | | | V |
| $V_{reg}$ = 0 V | $V_7$* | 1 | 2.7 | 3.3 | 4.0 | |
| $V_{reg}$ = 0 V | $V_8$* | 1 | 2.7 | 3.4 | 4.0 | |
| $V_{reg}$ = 0 V/−10 V | $\Delta V_8$* | 1 | 1.4 | 1.8 | 2.2 | |

*Only dc portion.

**PROTECTIVE OPERATION** ($V_9$ = 10 V; $V_{reg}$ = −10 V; $V_{pulse}$ = ±0.5 V; f = 20 kHz; duty cycle: ½)

| | | | | | | |
|---|---|---|---|---|---|---|
| Current Consumption ($V_5 < 1.8$ V) | $I_9$ | 1 | 14 | 20 | 26 | mA |
| Turn-off Voltage ($V_5 < 1.8$ V) | $V_7$<br>$V_4$ | 1<br>1 | 1.3<br>1.8 | 1.5<br>2.1 | 1.8<br>2.5 | V |
| External Trigger Input<br>Enable Voltage ($V_{reg}$ = 0 V)<br>Disabled Voltage ($V_{reg}$ = 0 V) | <br>$V_5$<br>$V_5$ | <br>1<br>1 | <br>—<br>1.8 | <br>2.4<br>2.2 | <br>2.7<br>— | V |
| Supply Voltage Disabling $V_8$ ($V_{reg}$ = 0 V) | $V_9$ | 1 | 6.7 | 7.4 | 7.8 | V |

**RANGE OF OPERATION**

| | | | | | | |
|---|---|---|---|---|---|---|
| Turn-on Time (Secondary Voltages) | +on | 2 | — | 350 | 450 | ms |
| Voltage Change<br>When $S_3$ = Closed ($\Delta P_3$ = 19 W Audio Frequency Output Power)<br>When $S_2$ = Closed ($\Delta P_2$ = 15 W) | <br>$\Delta V_2$<br>$\Delta V_2$ | <br>2<br>2 | <br>—<br>— | <br>100<br>500 | <br>500<br>1000 | mV |
| Standby Operation (Secondary Useable Power = 3.0 W)<br>When $S_1$ = Open | $\Delta V_2$<br>f<br>$P_{prim}$ | 2<br>2<br>2 | —<br>70<br>— | 20<br>75<br>10 | 30<br>—<br>12 | V<br>kHz<br>VA |

The heat sink must be optimized, taking the maximum data ($T_J$, $R_{\theta JC}$, $R_{\theta JA}$, $T_A$) into consideration.

FIGURE 1 — MEASURING CIRCUIT

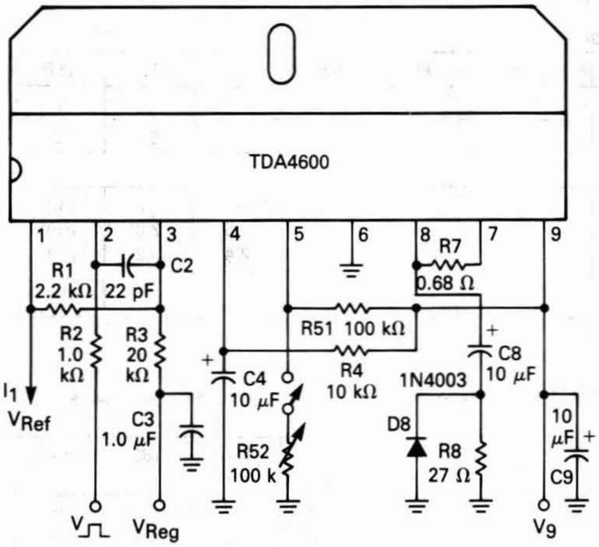
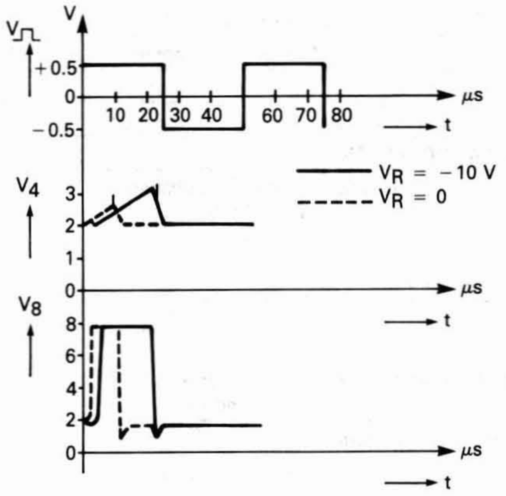


FIGURE 2 — TEST DIAGRAM: NORMAL OPERATION



## CIRCUIT DESCRIPTION

The TDA4600 regulates, controls, and protects the switching transistor in flyback converter power supplies at starting, normal and overload operation.

### A. Starting Behavior

At the start-up there are three consecutive operation states.

1. An internal reference voltage is created. It supplies the voltage regulator and enables the supply to the coupling electrolytic capacitor and the switching transistor. For a supply voltage of $V_9$ = 12 V, the current $I_9$ is less than 3.2 mA.
2. Release of the internal reference voltage $V_1$ = 4.0 V. This voltage is available when $V_9$ = 12 V and

enables all parts of the IC to be supplied from the control logic with thermal and overload protection.

3. Release of control logic — As soon as the reference voltage is available, the control is switched on through an additional stabilization circuit.

This start-up sequence is necessary for driving the switching transistor through the coupling electrolytic capacitor.

**B. Normal Operation**

Zero crossing detection is sensed on Pin 2 and linked to the control logic.

The signal picked up on the feedback winding is applied, after filtering, to Pin 3 (used for input regulation and for overload protection). The regulating section works with an input voltage of about 2.0 V for normal regulation and a current of about 1.4 mA for foldback operation. Together with the collector current simulation Pin 4, the overload recognition defines the operating region of the regulating amplifier depending on the internal reference voltage. The simulation of the collector current is generated by an external RC network at Pin 4 and an internally set voltage level.

For a constant line and for a given output power on the load ($t_{on}$ fixed) less than the maximum output power, a decrease of C Pin 4 produces an increase of the current sent to the base of the power switching transistor. So the foldback point is reached earlier. The regulation range starts from a 2.0 Vdc level which is the bottom of a sawtooth waveform whose top is limited at 4.0 V (reference voltage).

A secondary load of 19 W produces a switching frequency of about 50 kHz at an almost constant duty cycle. Furthermore, when the switchmode power supply delivers approximately 3.0 W, the switching frequency jumps to about 70 kHz. At the same time, the collector peak current falls below 1.0 A.

The comparison of the output level of the regulating amplifier, the overload detection and the collector current simulation drives the control logic. An additional steering control and blocking possibility is offered thru Pin 5. When the voltage applied on Pin 5 falls below 2.2 V, the source output (Pin 8) is blocked.

The control logic is set according to the start-up circuit, the zero crossing detection and the trigger enable. This logic drives the base current amplifier and the base current shutdown. The base current amplifier drives the source output (Pin 8) proportionally to the sawtooth voltage (Pin 4). A current feedback is performed by an external shunt inserted between Pin 8 and the base of the switching power transistor. This shunt value determines the maximum amplitude of the base current drive.

FIGURE 3 — FREQUENCY versus OUTPUT POWER

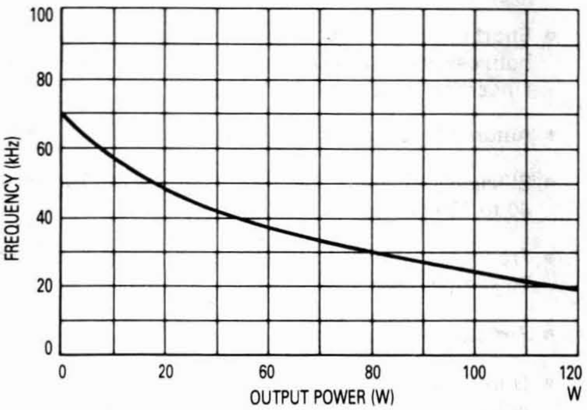
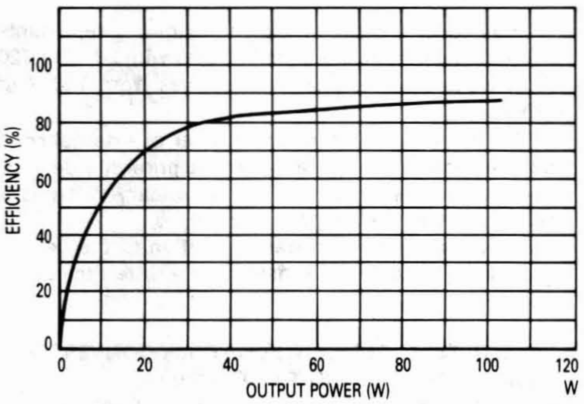


FIGURE 4 — EFFICIENCY versus OUTPUT POWER



**C. Protective Features**

The base current shutdown, released by the control logic, clamps the sink output (Pin 7) at 1.6 V, turning off the switching transistor. This feature will be released if the voltage on Pin 9 is less than 7.4 V, or if the applied voltage on Pin 5 is less than 2.2 V. In case of a short circuit of the secondary windings, the TDA4600 continuously monitors the fault condition.

In standby operation the circuit is set to a high duty cycle. The total power consumption of the power supply is held below 6.0 to 10 W. Once the output is blocked (due to the supply voltage coming down to 7.4 V), a further voltage reduction to 6.0 V switches off the reference voltage.

**FIGURE 5 — LOAD CHARACTERISTICS ($V_2 = f(I_{q2})$)**

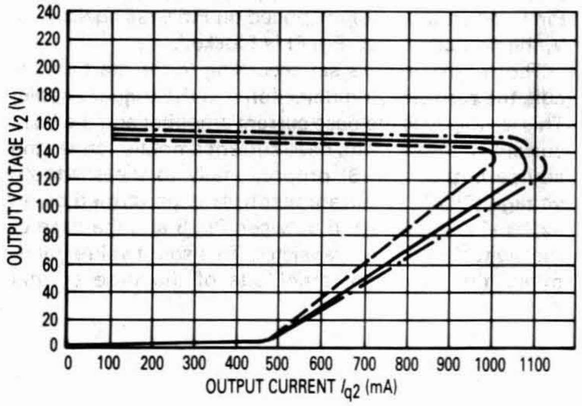
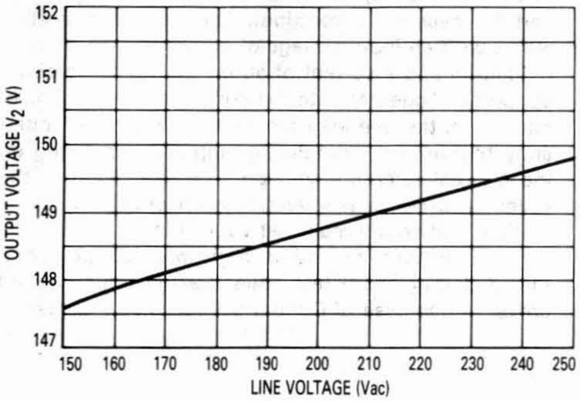


**FIGURE 6 — OUTPUT VOLTAGE $V_2$ (line change)**



## TEST CIRCUIT AND TYPICAL APPLICATION (see Figure 7 on the next page)

This application circuit shown in Figure 7 represents a blocking converter for color TV sets with 30 W to 120 W of output power and line voltages from 160 V to 270 V.

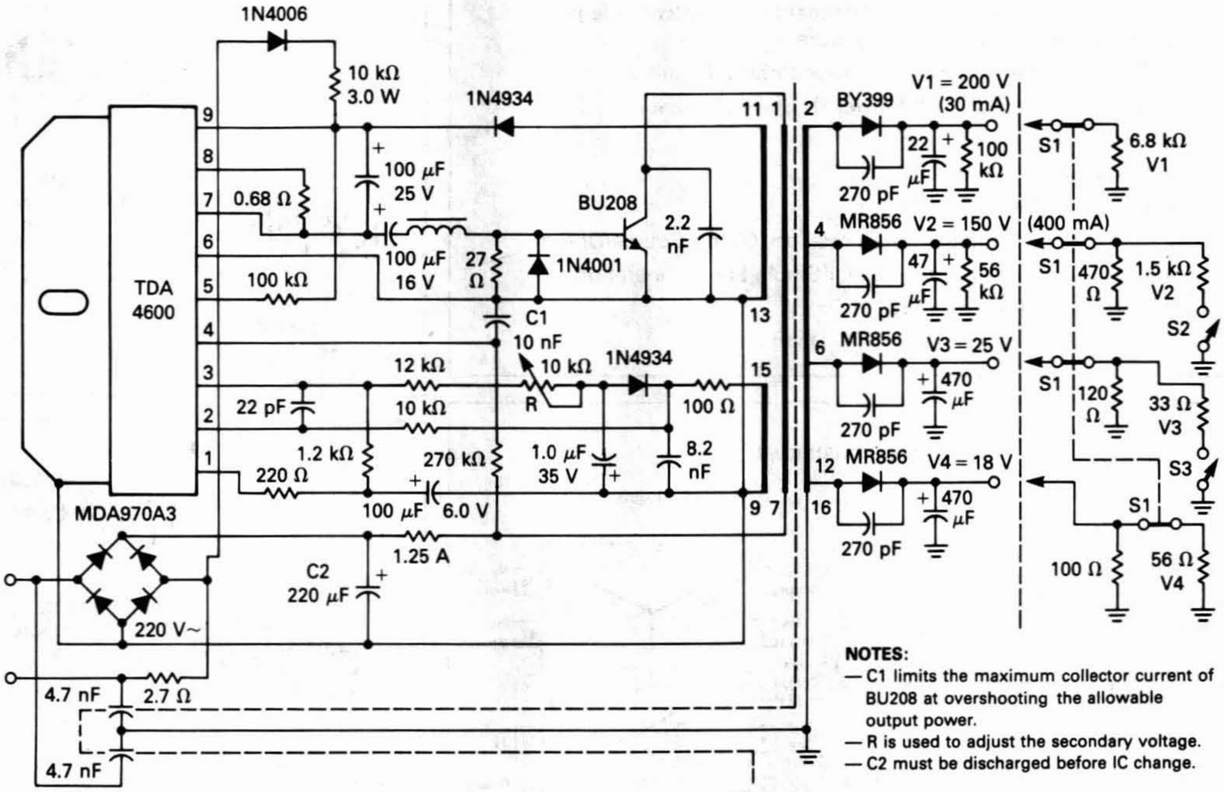
This circuit shows the low number of external components. Inspite of regulation on the primary side, high voltage stability of the various secondary voltages is achieved even with large load changes.

For line isolation and transformation to the desired secondary voltages, a transformer with ferrite core is used.

**SPECIAL FEATURES OF THE FLYBACK CONVERTER POWER SUPPLY USING THE TDA4600**

- Direct driving of the power switching transistor
- Low starting current, defines starting behavior even at slowly rising line voltage
- Short-circuit proof and open-loop resistant circuit. In both cases a power of only 6.0 to 10 W is consumed. Linear foldback characteristic at overload
- Automatic restart after elimination of the overload
- Efficiency of more than 80% at an output power of 40 to 100 W
- Frequency of ocillation between 20 kHz (100 W) and 70 kHz (without load)
- Simple RF I suppression
- Good regulation of load current and line voltage variations. At a line voltage variation between 170 and 240 Vac the output voltage of 150 V will change only by about 2.0 V

FIGURE 7 — TYPICAL 100 WATT APPLICATION


1N4006
10 kΩ
3.0 W
1N4934
TDA
4600
MDA970A3
9
8
7
6
5
4
3
2
1
0.68 Ω
100 kΩ
100 μF
25 V
100 μF
16 V
27
Ω
1N4001
BU208
2.2
nF
C1
10 nF
12 kΩ
10 kΩ
R
1N4934
100 Ω
22 pF
1.2 kΩ
220 Ω
270 kΩ
1.0 μF
35 V
8.2
nF
100 μF
6.0 V
1.25 A
C2
220 μF
220 V~
4.7 nF
2.7 Ω
4.7 nF
11
1
13
15
9
7
2
4
6
12
16
BY399
V1 = 200 V
(30 mA)
22
μF
100
kΩ
270 pF
MR856
V2 = 150 V
(400 mA)
47
μF
56
kΩ
270 pF
MR856
V3 = 25 V
470
μF
270 pF
MR856
V4 = 18 V
470
μF
270 pF
S1
6.8 kΩ
V1
S1
470
Ω
1.5 kΩ
V2
S2
S1
120
Ω
33 Ω
V3
S3
S1
100 Ω
56 Ω
V4

**NOTES:**

- C1 limits the maximum collector current of BU208 at overshooting the allowable output power.
- R is used to adjust the secondary voltage.
- C2 must be discharged before IC change.

**MOTOROLA**

# TL494
# TL495

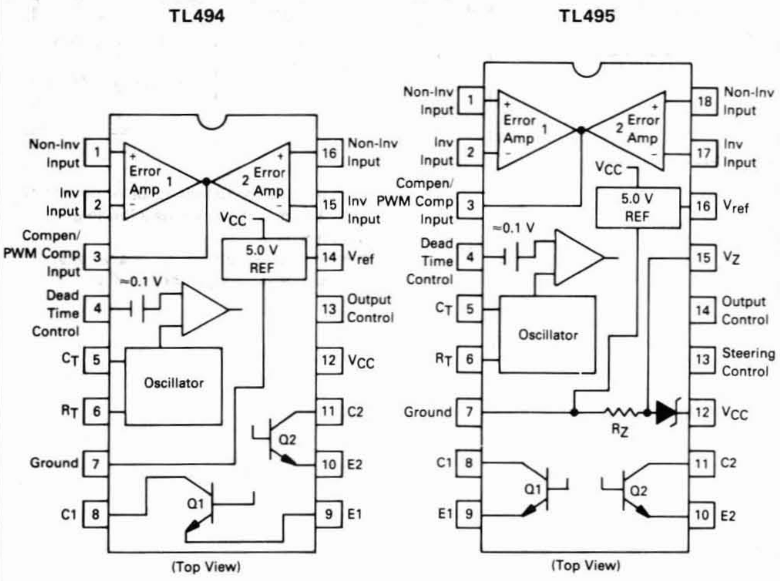
## Specifications and Applications Information

### SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The TL494 and TL495 are fixed frequency, pulse width modulation control circuits designed primarily for Switchmode power supply control. These devices feature:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master Or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5 Volt Reference
- Adjustable Dead-Time Control
- Uncommitted Output Transistors For 200 mA Source Or Sink
- Output Control For Push-Pull Or Single-Ended Operation
- On-Chip 39 Volt Zener (TL495 Only)
- Output Steering Control (TL495 Only)

**PIN CONNECTIONS**

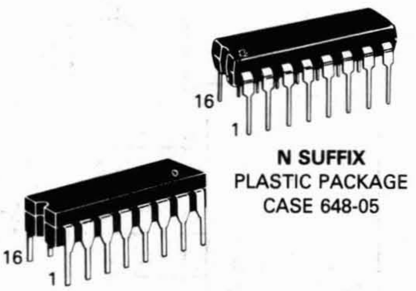

TL494
Non-Inv Input 1
Inv Input 2
Compen/PWM Comp Input 3
Dead Time Control 4
CT 5
RT 6
Ground 7
C1 8
16 Non-Inv Input
15 Inv Input
14 Vref
13 Output Control
12 VCC
11 C2
10 E2
9 E1
Error Amp 1
Error Amp 2
VCC
5.0 V REF
≈0.1 V
Oscillator
Q1
Q2
(Top View)
TL495
Non-Inv Input 1
Inv Input 2
Compen/PWM Comp Input 3
Dead Time Control 4
CT 5
RT 6
Ground 7
C1 8
E1 9
18 Non-Inv Input
17 Inv Input
16 Vref
15 VZ
14 Output Control
13 Steering Control
12 VCC
11 C2
10 E2
RZ
(Top View)

The TL494C/495C are specified over the commercial operating range of 0°C to 70°C. The TL494I/495I are specified over the industrial range of −25°C to 85°C. The TL494M is specified over the full military range of −55°C to 125°C.

### SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

**SILICON MONOLITHIC INTEGRATED CIRCUITS**

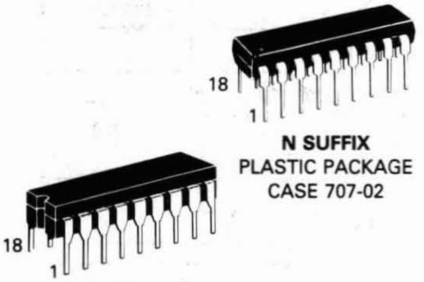
**TL494**



**N SUFFIX**
PLASTIC PACKAGE
CASE 648-05

**J SUFFIX**
CERAMIC PACKAGE
CASE 620-02

**TL495**



**N SUFFIX**
PLASTIC PACKAGE
CASE 707-02

**J SUFFIX**
CERAMIC PACKAGE
CASE 726-01

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| TL494CN | 0 To 70°C | Plastic DIP |
| TL494CJ | 0 To 70°C | Ceramic DIP |
| TL494IN | −25 To 85°C | Plastic DIP |
| TL494IJ | −25 To 85°C | Ceramic DIP |
| TL494MJ | −55 To 125°C | Ceramic DIP |
| | | |
| TL495CN | 0 To 70°C | Plastic DIP |
| TL495CJ | 0 To 70°C | Ceramic DIP |
| TL495IN | −25 To 85°C | Plastic DIP |
| TL495IJ | −25 To 85°C | Ceramic DIP |

FIGURE 1 — BLOCK DIAGRAM

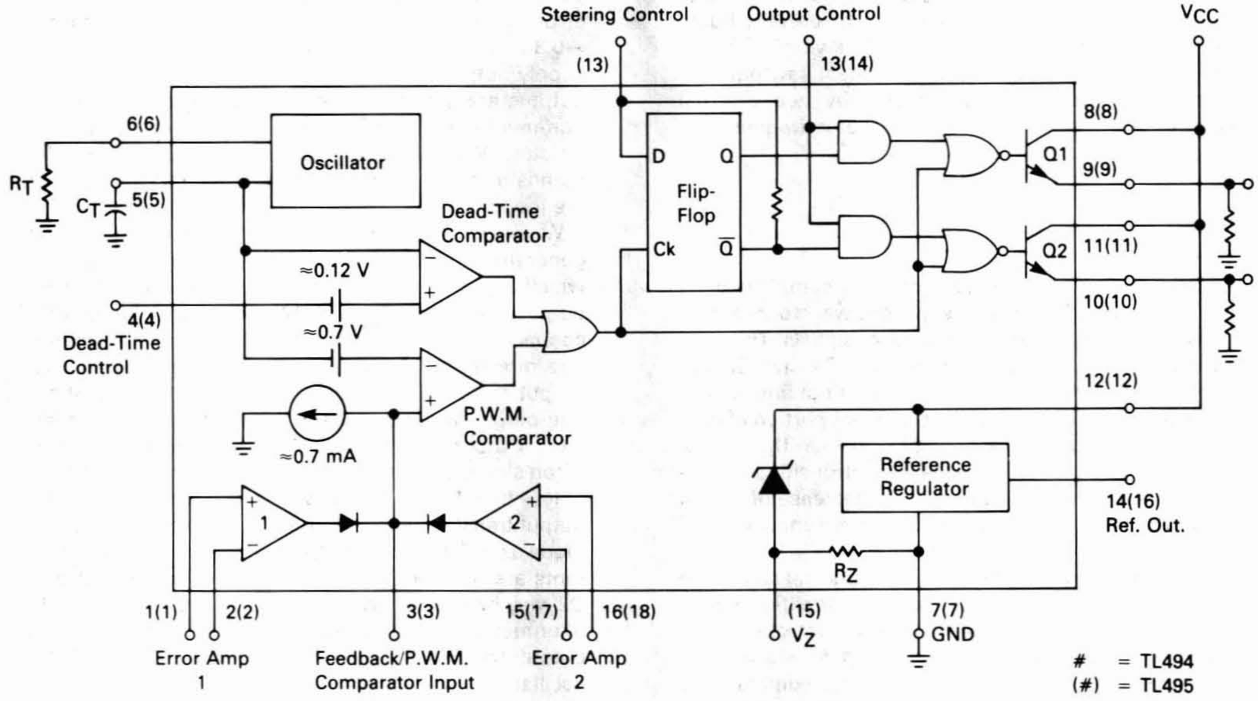
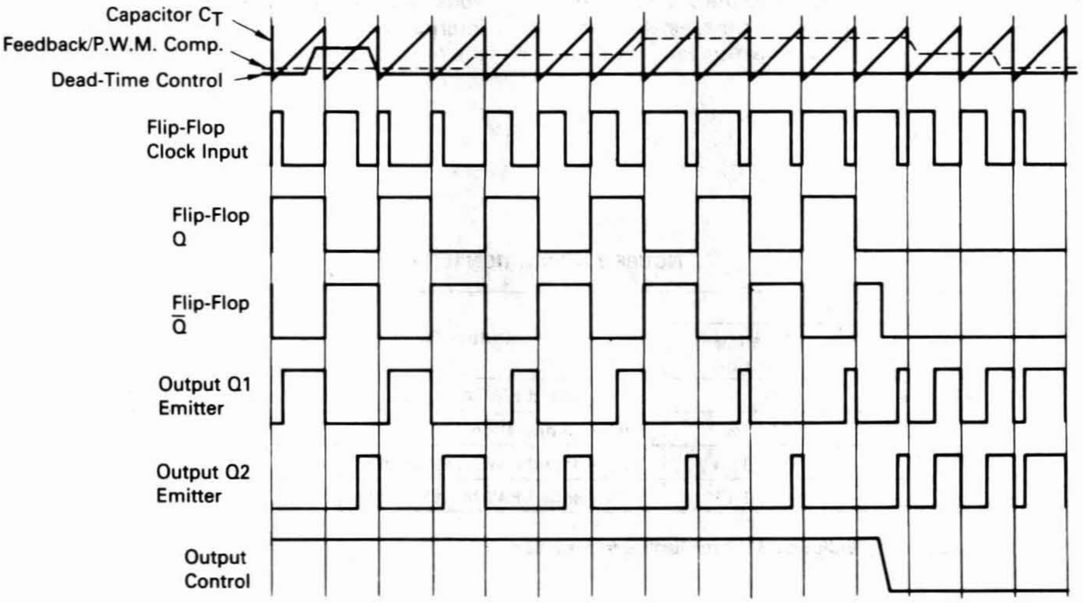

Steering Control
Output Control
VCC
(13)
13(14)
8(8)
6(6)
Oscillator
D
Q
Flip-Flop
Ck
Q̄
Q1
9(9)
RT
CT
5(5)
Dead-Time Comparator
Q2
11(11)
≈0.12 V
10(10)
4(4)
Dead-Time Control
≈0.7 V
12(12)
P.W.M. Comparator
≈0.7 mA
Reference Regulator
14(16)
Ref. Out.
1
2
RZ
1(1)
2(2)
3(3)
15(17)
16(18)
(15)
7(7)
VZ
GND
Error Amp 1
Feedback/P.W.M. Comparator Input
Error Amp 2
# = TL494
(#) = TL495

FIGURE 2 — TIMING DIAGRAM


Capacitor CT
Feedback/P.W.M. Comp.
Dead-Time Control
Flip-Flop Clock Input
Flip-Flop Q
Flip-Flop Q̄
Output Q1 Emitter
Output Q2 Emitter
Output Control

4

## Description

The TL494/495 are fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, $R_T$ and $C_T$. The oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor $C_T$ to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from $-0.3$ V to ($V_{CC} - 2$ V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor $C_T$ is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL494/495 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an accuracy of ±5% with a thermal drift of less than 50 mV over an operating temperature range of 0 to 70°C.

The TL495 contains an on-chip 39 volt zener diode for high voltage applications where $V_{CC}$ is greater than 40 volts, and an output steering control that overrides the internal control of the pulse-steering flip-flop. (Refer to the functional table shown in Figure 3.)

FIGURE 3 — FUNCTIONAL TABLE

| Inputs | | Output Function | $\frac{f_{out}}{f_{osc}} =$ |
|---|---|---|---|
| Output Control | Steering Control | | |
| Grounded | Open | Single-ended P.W.M. at Q1 and Q2 | 1 |
| At $V_{ref}$ | Open | Push-pull operation | 0.5 |
| At $V_{ref}$ | V1 <0.4 V | Single-ended P.W.M. at Q1 only | 1 |
| At $V_{ref}$ | V1 >2.4 V | Single-ended P.W.M. at Q2 only | 1 |

**See Engineering Bulletin EB100 for further information.**

**MAXIMUM RATINGS** (Full operating ambient temperature range applies unless otherwise noted.)

| Rating | Symbol | TL494M | TL494I/TL495I | TL494C/TL495C | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 42 | 42 | 42 | V |
| Collector Output Voltage | $V_{C1}, V_{C2}$ | 42 | 42 | 42 | V |
| Collector Output Current (each transistor) | $I_{C1}, I_{C1}$ | 250 | 250 | 250 | mA |
| Amplifier Input Voltage | $V_{in}$ | $V_{CC}$ + 3.0 | $V_{CC}$ + 3.0 | $V_{CC}$ + 3.0 | V |
| Power Dissipation @ $T_A \leq 45°C$ | $P_D$ | 1000 | 1000 | 1000 | mW |
| Operating Junction Temperature | $T_J$ | 150 | 150 | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | −55 to 125 | −25 to 85 | 0 to 70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | −65 to +150 | −65 to +150 | °C |

**THERMAL CHARACTERISTICS**

| Characteristics | Symbol | J Suffix Ceramic Package | N Suffix Plastic Package | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 100 | 80 | °C/W |
| Power Derating Factor | $1/R_{\theta JA}$ | 10.0 | 12.5 | mW/°C |
| Derating Ambient Temperature | $T_A$ | 50 | 45 | °C |

**RECOMMENDED OPERATING CONDITIONS**

| | | TL494/TL495 | | | |
|---|---|---|---|---|---|
| Condition/Value | Symbol | Min | Typ | Max | Unit |
| Power Supply Voltage | $V_{CC}$ | 7.0 | 15 | 40 | V |
| Collector Output Voltage | $V_{C1}, V_{C2}$ | — | 30 | 40 | V |
| Collector Output Current (each transistor) | $I_{C1}, I_{C2}$ | — | — | 200 | mA |
| Amplifier Input Voltage | $V_{in}$ | −0.3 | — | $V_{CC}$ − 2.0 | V |
| Current Into Feedback Terminal | $I_{f.b.}$ | — | — | 0.3 | mA |
| Reference Output Current | $I_{ref}$ | — | — | 10 | mA |
| Timing Resistor | $R_T$ | 1.8 | 30 | 500 | kΩ |
| Timing Capacitor | $C_T$ | 0.47 | 1.0 | 10,000 | nF |
| Oscillator Frequency | $f_{osc}$ | 1.0 | 40 | 200 | kHz |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $f_{osc}$ = 10 kHz unless otherwise noted.)
For typical values $T_A$ = 25°C, for min/max values $T_A$ is the operating ambient temperature range that applies unless otherwise noted.

| | | TL494M | | | TL494C, I/TL495C,I | | | |
|---|---|---|---|---|---|---|---|---|
| Characteristic | Symbol | Min | Typ | Max | Min | Typ | Max | Unit |
| **REFERENCE SECTION** | | | | | | | | |
| Reference Voltage ($I_O$ = 1.0 mA) | $V_{ref}$ | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| Reference Voltage Change with Temperature ($\Delta T_A$ = Min to Max) | $\Delta V_{ref}$ ($\Delta$T) | — | 0.2 | 2.0 | — | 1.3 | 2.6 | % |
| Input Regulation ($V_{CC}$ = 7.0 V to 40 V) | $Reg_{line}$ | — | 2.0 | 25 | — | 2.0 | 25 | mV |
| Output Regulation ($I_O$ = 1.0 mA to 10 mA) | $Reg_{load}$ | — | 3.0 | 15 | — | 3.0 | 15 | mV |
| Short-Circuit Output Current ($V_{ref}$ = 0 V, $T_A$ = 25°C) | $I_{SC}$ | 10 | 35 | 50 | — | 35 | — | mA |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $f_{osc}$ = 10 kHz unless otherwise noted.)
For typical values $T_A$ = 25°C, for min/max values $T_A$ is the operating ambient temperature range that applies unless otherwise noted.

| Characteristic | Symbol | TL494M | | | TL494C, I/TL495C, I | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **OUTPUT SECTION** | | | | | | | | |
| Collector Off-State Current<br>($V_{CC}$ = 40 V, $V_{CE}$ = 40 V) | $I_{C(off)}$ | — | 2.0 | 100 | — | 2.0 | 100 | μA |
| Emitter Off-State Current<br>($V_{CC}$ = 40 V, $V_C$ = 40 V, $V_E$ = 0 V) | $I_{E(off)}$ | — | — | −150 | — | — | −100 | μA |
| Collector-Emitter Saturation Voltage<br>Common-Emitter<br>($V_E$ = 0 V, $I_C$ = 200 mA) | $V_{sat(C)}$ | — | 1.1 | 1.5 | — | 1.1 | 1.3 | V |
| Emitter-Follower<br>($V_C$ = 15 V, $I_E$ = −200 mA) | $V_{sat(E)}$ | — | 1.5 | 2.5 | — | 1.5 | 2.5 | V |
| Output Control Pin Current<br>Low State<br>($V_{OC}$ ≤ 0.4 V) | $I_{OCL}$ | — | 10 | — | — | 10 | — | μA |
| High State<br>($V_{OC}$ = $V_{ref}$) | $I_{OCH}$ | — | 0.2 | 3.5 | — | 0.2 | 3.5 | mA |
| Output Voltage Rise Time ($T_A$ = 25°C)<br>Common-Emitter (See Figure 13) | $t_r$ | — | 100 | 200 | — | 100 | 200 | ns |
| Emitter-Follower (See Figure 14) | | — | 100 | 200 | — | 100 | 200 | ns |
| Output Voltage Fall Time ($T_A$ = 25°C)<br>Common-Emitter (See Figure 13) | $t_f$ | — | 25 | 100 | — | 25 | 100 | ns |
| Emitter-Follower (See Figure 14) | | — | 40 | 100 | — | 40 | 100 | ns |

| Characteristic | Symbol | TL494/TL495 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **ERROR AMPLIFIER SECTIONS** | | | | | |
| Input Offset Voltage<br>($V_{O\ (Pin\ 3)}$ = 2.5 V) | $V_{IO}$ | — | 2.0 | 10 | mV |
| Input Offset Current<br>($V_{O\ (Pin\ 3)}$ = 2.5 V) | $I_{IO}$ | — | 5.0 | 250 | nA |
| Input Bias Current<br>($V_{O\ (Pin\ 3)}$ = 2.5 V) | $I_{IB}$ | — | 0.1 | 1.0 | μA |
| Input Common-Mode Voltage Range<br>($V_{CC}$ = 7.0 V to 40 V) | $V_{ICR}$ | −0.3 | — | $V_{CC}$ − 2.0 | V |
| Open-Loop Voltage Gain<br>($\Delta V_O$ = 3.0 V, $V_O$ = 0.5 to 3.5 V, $R_L$ = 2.0 kΩ) | $A_{VOL}$ | 70 | 95 | — | dB |
| Unity-Gain Crossover Frequency<br>($V_O$ = 0.5 to 3.5 V, $R_L$ = 2.0 kΩ) | $f_C$ | — | 350 | — | kHz |
| Phase Margin at Unity-Gain<br>($V_O$ = 0.5 to 3.5 V, $R_L$ = 2.0 kΩ) | Øm | — | 65 | — | deg. |
| Common-Mode Rejection Ratio<br>($V_{CC}$ = 40 V) | CMRR | 65 | 90 | | dB |
| Power Supply Rejection Ratio<br>($\Delta V_{CC}$ = 33 V, $V_O$ = 2.5 V, $R_L$ = 2.0 kΩ) | PSRR | — | 100 | — | dB |
| Output Sink Current<br>($V_{O\ (Pin\ 3)}$ = 0.7 V) | $I_{O-}$ | 0.3 | 0.7 | — | mA |
| Output Source Current<br>($V_{O\ (Pin\ 3)}$ = 3.5 V) | $I_{O+}$ | −2.0 | −4.0 | — | mA |

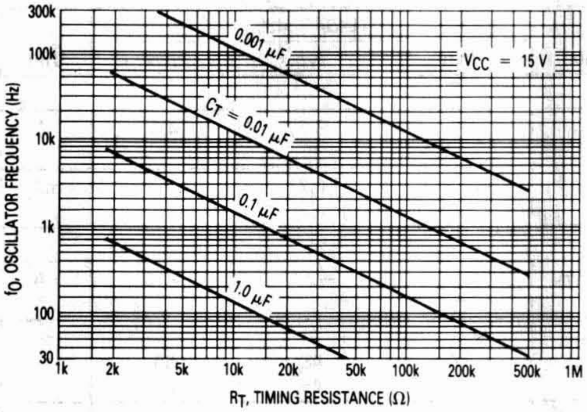
**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 V, $f_{osc}$ = 10 kHz unless otherwise noted.)
For typical values $T_A$ = 25°C, for min/max values $T_A$ is the operating ambient temperature range that applies unless otherwise noted.

| | | TL494/TL495 | | | |
|---|---|---|---|---|---|
| **Characteristic** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| **PWM COMPARATOR SECTION** (Test Circuit Figure 12) | | | | | |
| Input Threshold Voltage<br>(Zero duty cycle) | $V_{TH}$ | — | 3.5 | 4.5 | V |
| Input Sink Current<br>($V_{(Pin\ 3)}$ = 0.7 V) | $I_{I-}$ | 0.3 | 0.7 | — | mA |
| **DEAD-TIME CONTROL SECTION** (Test Circuit Figure 12) | | | | | |
| Input Bias Current (Pin 4)<br>($V_{in}$ = 0 to 5.25 V) | $I_{IB\ (DT)}$ | — | −2.0 | −10 | µA |
| Maximum Duty Cycle, Each Output, Push-Pull Mode | $DC_{max}$ | | | | % |
| ($V_{in}$ = 0 V, $C_T$ = 0.1 µF, $R_T$ = 12 kΩ) | | 45 | 48 | 50 | |
| ($V_{in}$ = 0 V, $C_T$ = 0.001 µF, $R_T$ = 30 kΩ) | | — | 45 | 50 | |
| Input Threshold Voltage (Pin 4) | $V_{TH}$ | | | | V |
| (Zero Duty Cycle) | | — | 2.8 | 3.3 | |
| (Maximum Duty Cycle) | | 0 | — | — | |
| **OSCILLATOR SECTION** | | | | | |
| Frequency<br>($C_T$ = 0.001 µF, $R_T$ = 30 kΩ) | $f_{osc}$ | — | 40 | — | kHz |
| Standard Deviation of Frequency*<br>($C_T$ = 0.001 µF, $R_T$ = 30 kΩ) | $\sigma f_{osc}$ | — | 3.0 | — | % |
| Frequency Change with Voltage<br>($V_{CC}$ = 7.0 V to 40 V, $T_A$ = 25°C) | $\Delta f_{osc\ (\Delta V)}$ | — | 0.1 | — | % |
| Frequency Change with Temperature<br>($\Delta T_A$ = $T_{low}$ to $T_{high}$) (T = 0.01 µF, $R_T$ = 12 k) | $\Delta f_{osc\ (\Delta T)}$ | — | — | 12 | % |

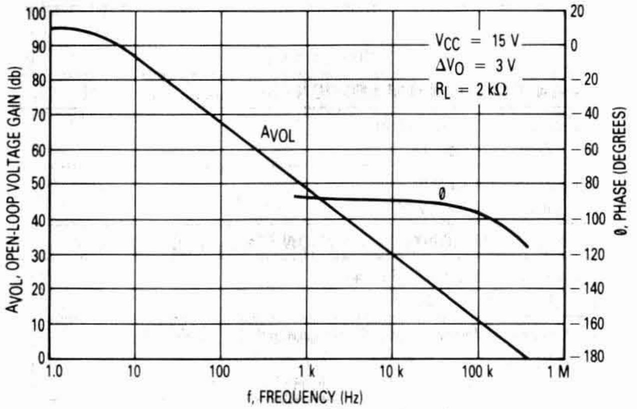
| | | TL495 | | | |
|---|---|---|---|---|---|
| **Characteristic** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| **STEERING CONTROL** | | | | | |
| Input Current Low<br>($V_{(Pin\ 13)}$ = 0.4 V) | $I_{STL}$ | — | −25 | −200 | µA |
| Input Current High | $I_{STH}$ | | | | µA |
| ($V_{(Pin\ 13)}$ = 2.4 V) | | — | 25 | 200 | |
| ($V_{(Pin\ 13)}$ = $V_{ref}$) | | — | 75 | — | |
| **ZENER CHARACTERISTICS** | | | | | |
| Zener Breakdown Voltage<br>($I_Z$ = 2.0 mA) | $V_Z$ | — | 39 | — | V |
| Sink Current<br>($V_{(Pin\ 15)}$ = 1.0 V) | $I_{RZ}$ | — | 0.3 | — | mA |
| **TOTAL DEVICE** | | | | | |
| Standby Supply Current<br>(Pin 6 at $V_{ref}$, All Other Inputs and Outputs Open) | $I_{CC}$ | | | | mA |
| ($V_{CC}$ = 15 V) | | — | 5.5 | 10 | |
| ($V_{CC}$ = 40 V) | | — | 7.0 | 15 | |
| Average Supply Current<br>($V_{(Pin\ 4)}$ = 2.0 V) (See Figure 12.)<br>($C_T$ = 0.001, $R_T$ = 12 kΩ, $V_{CC}$ = 15 V) | — | — | 7.0 | — | mA |

* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\dfrac{\sum_{n=1}^{N} (X_n - \overline{X})^2}{N-1}}$

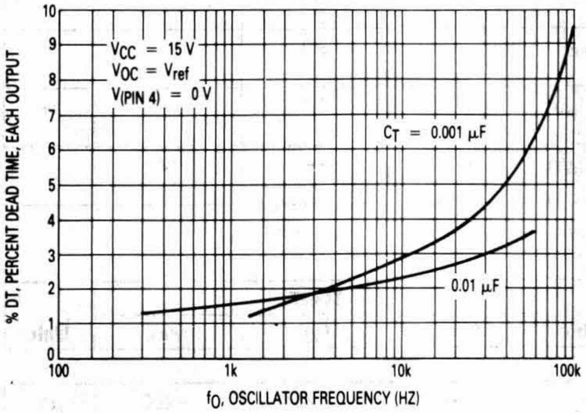
### FIGURE 4 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE



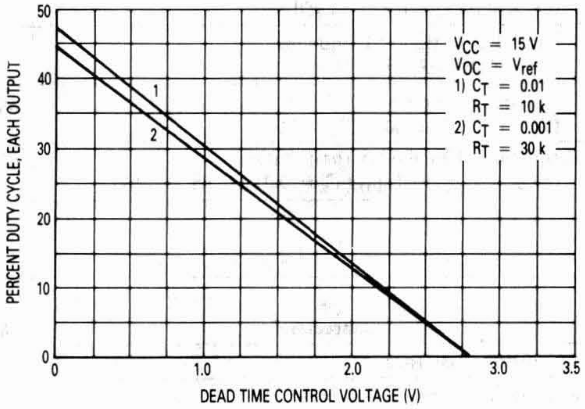
### FIGURE 5 — OPEN LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY



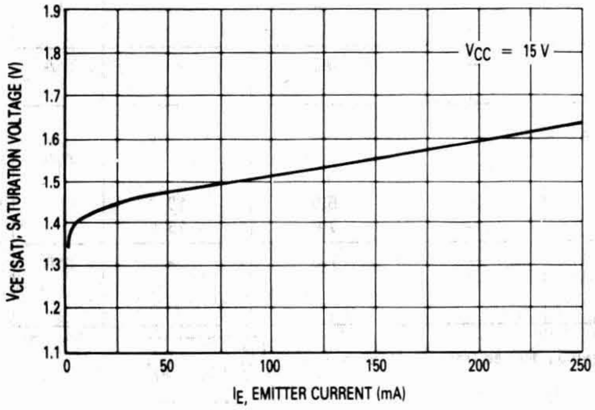
### FIGURE 6 — PERCENT DEAD TIME versus OSCILLATOR FREQUENCY



### FIGURE 7 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE



### FIGURE 8 — EMITTER-FOLLOWER CONFIGURATION, OUTPUT-SATURATION VOLTAGE versus EMITTER CURRENT



### FIGURE 9 — COMMON-EMITTER CONFIGURATION OUTPUT-SATURATION VOLTAGE versus COLLECTOR CURRENT

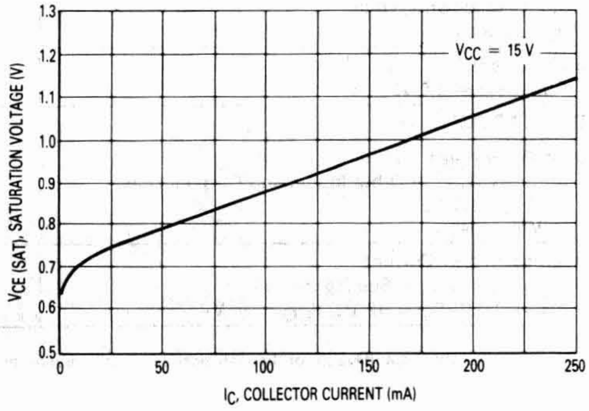


FIGURE 10 — STANDBY-SUPPLY CURRENT versus SUPPLY VOLTAGE

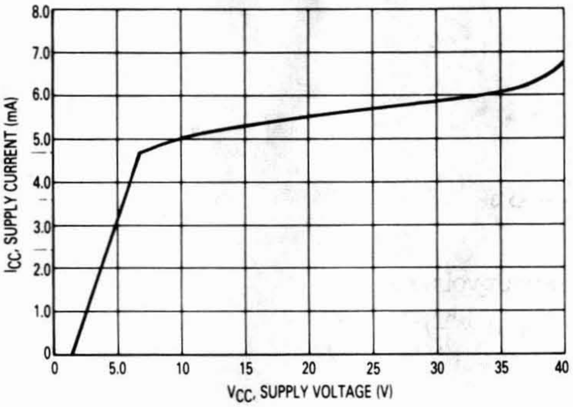


FIGURE 11 — ERROR AMPLIFIER CHARACTERISTICS

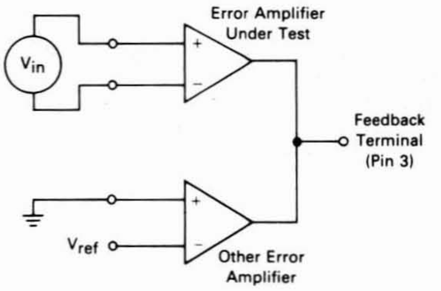

Vin
Error Amplifier
Under Test
+
−
Feedback
Terminal
(Pin 3)
Vref
+
−
Other Error
Amplifier

FIGURE 12 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

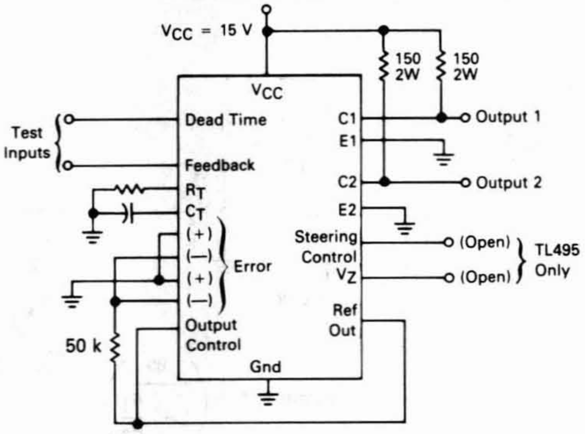

VCC = 15 V
150
2W
150
2W
VCC
Test
Inputs
Dead Time
Feedback
RT
CT
(+)
(−)
(+)
(−)
Error
Output
Control
Gnd
C1
E1
C2
E2
Output 1
Output 2
Steering
Control
VZ
(Open)
(Open)
TL495
Only
Ref
Out
50 k

FIGURE 13 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

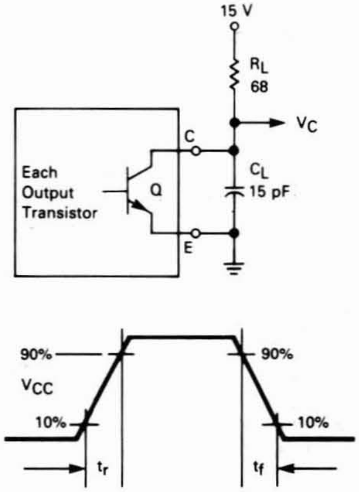

15 V
RL
68
VC
C
CL
15 pF
Each
Output
Transistor
Q
E
90%
90%
VCC
10%
10%
tr
tf

FIGURE 14 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

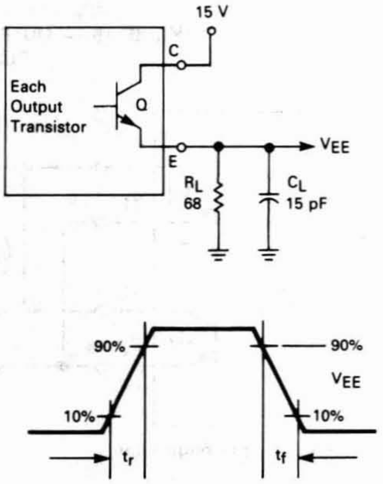
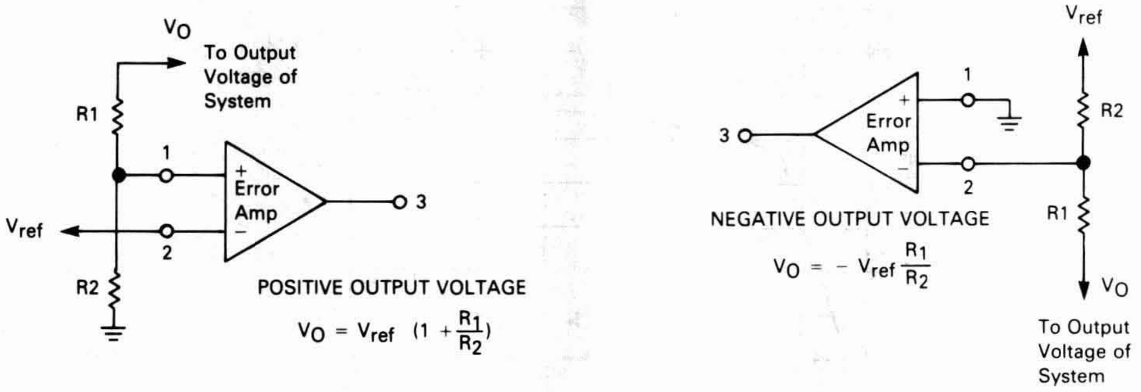
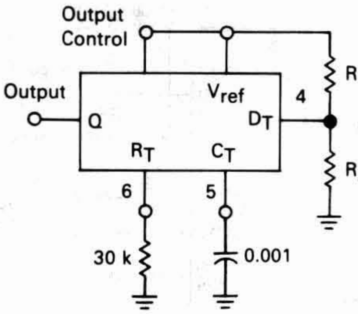

15 V
C
Each
Output
Transistor
Q
VEE
E
RL
68
CL
15 pF
90%
90%
VEE
10%
10%
tr
tf

FIGURE 15 — ERROR-AMPLIFIER SENSING TECHNIQUES



$V_O$
To Output Voltage of System
R1
1
Error Amp
3
$V_{ref}$
2
R2
POSITIVE OUTPUT VOLTAGE
$V_O = V_{ref}\ (1 + \frac{R_1}{R_2})$
$V_{ref}$
1
Error Amp
3
R2
2
NEGATIVE OUTPUT VOLTAGE
R1
$V_O = -V_{ref}\frac{R_1}{R_2}$
$V_O$
To Output Voltage of System

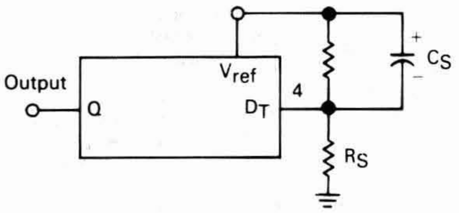
FIGURE 16 — DEAD-TIME CONTROL CIRCUIT



Output Control
Output
Q
$V_{ref}$
$D_T$
4
$R_1$
$R_2$
$R_T$
$C_T$
6
5
30 k
0.001

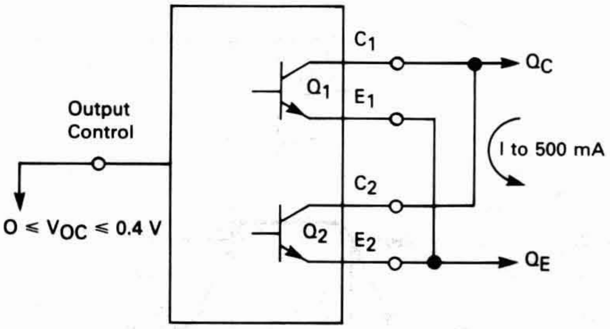
$$\text{Max \% on Time, Each Output} \approx 45 - \left(\frac{80}{1 + \frac{R_1}{R_2}}\right)$$

FIGURE 17 — SOFT-START CIRCUIT



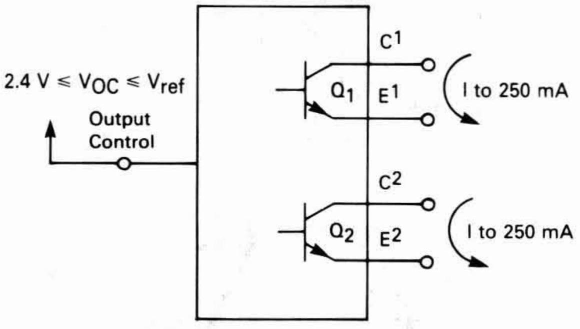
Output
Q
$V_{ref}$
$D_T$
4
$C_S$
$R_S$

FIGURE 18 — OUTPUT CONNECTIONS FOR SINGLE-ENDED AND PUSH-PULL CONFIGURATIONS



$C_1$
$Q_1$
$E_1$
$Q_C$
Output Control
I to 500 mA
$C_2$
$0 \leq V_{OC} \leq 0.4$ V
$Q_2$
$E_2$
$Q_E$

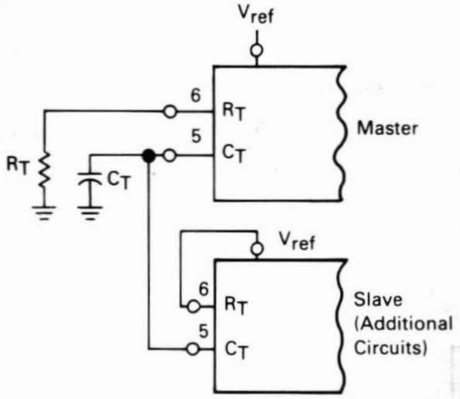
Single Ended Configuration



$C^1$
$2.4 \text{ V} \leq V_{OC} \leq V_{ref}$
$Q_1$
$E^1$
I to 250 mA
Output Control
$C^2$
$Q_2$
$E^2$
I to 250 mA

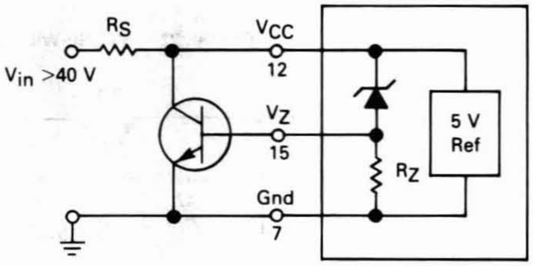
Push-Pull Configuration

**FIGURE 19 — SLAVING TWO OR MORE CONTROL CIRCUITS**



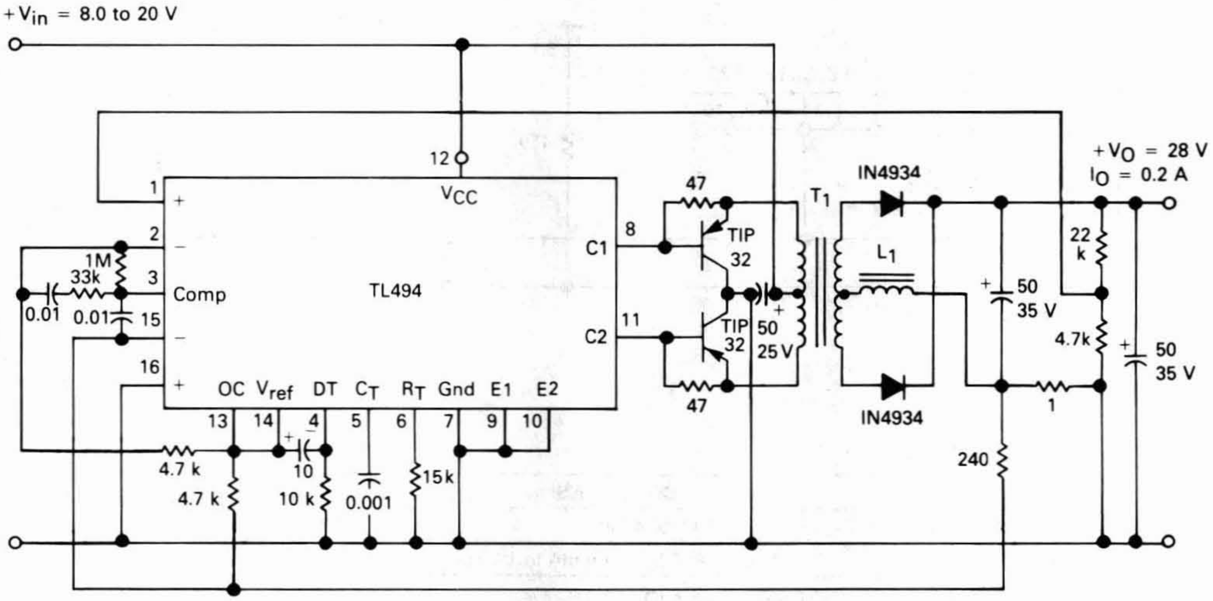
$V_{ref}$
6
$R_T$
5
$C_T$
Master
$R_T$
$C_T$
$V_{ref}$
6
$R_T$
5
$C_T$
Slave
(Additional
Circuits)

**FIGURE 20 — OPERATION WITH $V_{IN} > 40$ V USING INTERNAL ZENER (TL495 ONLY)**



$R_S$
$V_{in}$ >40 V
$V_{CC}$
12
$V_Z$
15
Gnd
7
$R_Z$
5 V
Ref

**FIGURE 21 — PULSE-WIDTH MODULATED PUSH-PULL CONVERTER**



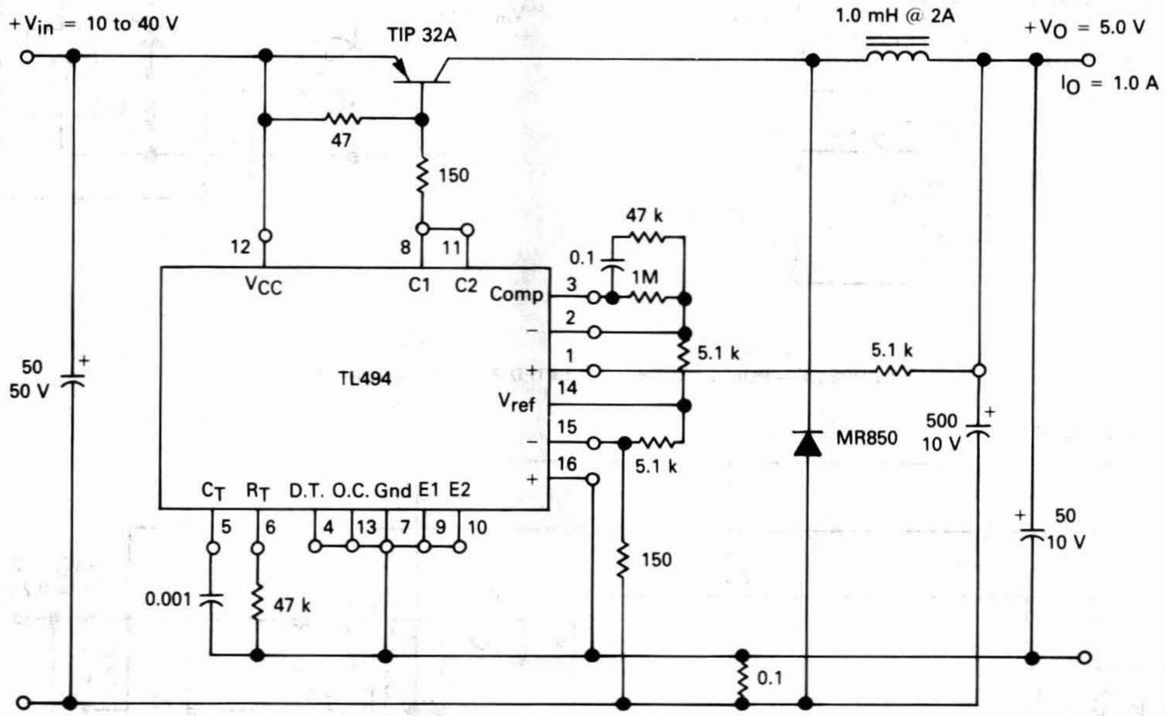
+$V_{in}$ = 8.0 to 20 V
12
$V_{CC}$
TL494
1
+
2
−
3
Comp
15
−
16
+
OC
$V_{ref}$
DT
$C_T$
$R_T$
Gnd
E1
E2
13
14
4
5
6
7
9
10
1M
33k
0.01
0.01
4.7 k
4.7 k
10
10 k
0.001
15k
C1
8
C2
11
47
TIP
32
TIP
32
47
50
25 V
$T_1$
$L_1$
IN4934
IN4934
50
35 V
22
k
4.7k
1
240
50
35 V
+$V_O$ = 28 V
$I_O$ = 0.2 A

All capacitors in µF

L1 — 3.5 mH @ 0.3 A
T1 — Primary: 20T C.T. #28 AWG
Secondary: 120T C.T. #36 AWG
Core: Ferroxcube 1408P-L00-3C8

| TEST | CONDITIONS | RESULTS |
|---|---|---|
| Line Regulation | $V_{in}$ = 8.0 to 20 V | 3.0 mV 0.01% |
| Load Regulation | $V_{in}$ = 12.6 V, $I_O$ = 0.2 to 200 mA | 5.0 mV 0.02% |
| Output Ripple | $V_{in}$ = 12.6 V, $I_O$ = 200 mA | 40 mV P-P P.A.R.D. |
| Short Circuit Current | $V_{in}$ = 12.6 V, $R_L$ = 0.1 Ω | 250 mA |
| Efficiency | $V_{in}$ = 12.6 V, $I_O$ = 200 mA | 72% |

FIGURE 22 — PULSE-WIDTH MODULATED STEP-DOWN CONVERTER


+$V_{in}$ = 10 to 40 V
TIP 32A
1.0 mH @ 2A
+$V_O$ = 5.0 V
$I_O$ = 1.0 A
47
150
47 k
0.1
1M
12
8
11
$V_{CC}$
C1
C2
Comp
3
2
1
14
15
16
−
+
$V_{ref}$
TL494
5.1 k
5.1 k
5.1 k
MR850
500
10 V
50
50 V
50
10 V
$C_T$
$R_T$
D.T.
O.C.
Gnd
E1
E2
5
6
4
13
7
9
10
0.001
47 k
150
0.1

All capacitors in µF

| TEST | CONDITIONS | RESULTS |
|---|---|---|
| Line Regulation | $V_{in}$ = 10 V to 40 V | 14 mV 0.28% |
| Load Regulation | $V_{in}$ = 28 V, $I_O$ = 1.0 mA to 1.0 mA | 3.0 mV 0.06% |
| Output Ripple | $V_{in}$ = 28 V, $I_O$ = 1.0 A | 65 mV P-P P.A.R.D. |
| Short Circuit Current | $V_{in}$ = 28 V, $R_L$ = 0.1 Ω | 1.6 amps |
| Efficiency | $V_{in}$ = 28 V, $I_O$ = 1.0 A | 71% |

**MOTOROLA**

# TL780 Series

## THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

This family of precision fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.5 amperes. Innovative design concepts, coupled with advanced thermal layout techniques has resulted in improved accuracy and excellent load, line and thermal regulation characteristics. Internal current limiting, thermal shutdown and safe-area compensation are employed, making these devices extremely rugged and virtually immune to overload.

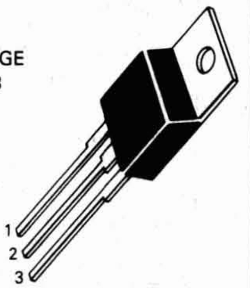
- ±1% Output Voltage Tolerance @ 25°C
- ±2% Output Voltage Tolerance Over Full Operating Temperature Range
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Output Transistor Safe-Area Compensation
- No External Components Required
- Pinout Compatible with MC7800 Series

## THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

**SILICON MONOLITHIC INTEGRATED CIRCUITS**

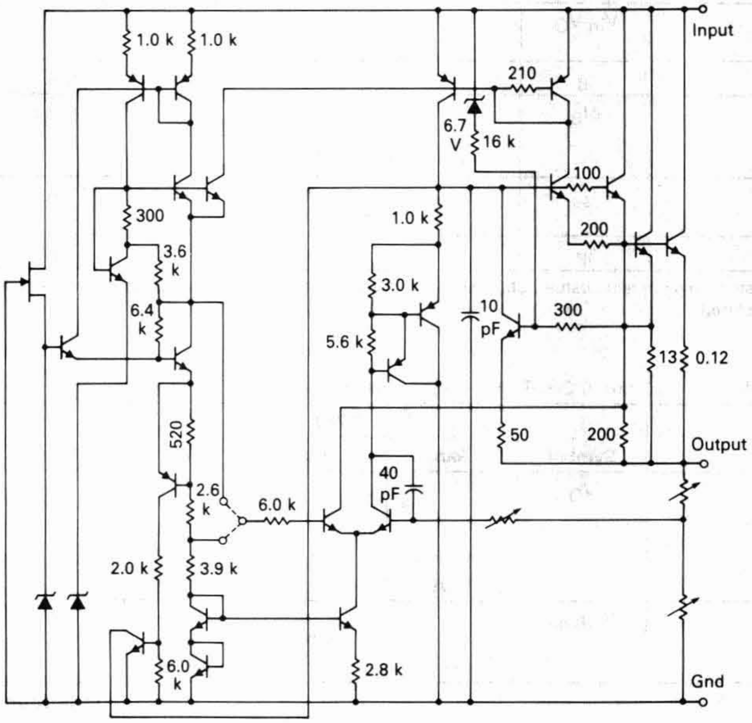
**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220AB

Pin 1. Input
2. Ground
3. Output

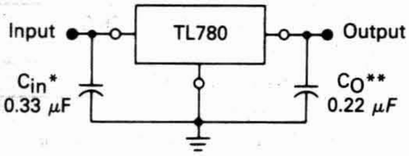


(Heatsink surface connected to Pin 2.)

### EQUIVALENT SCHEMATIC DIAGRAM



### STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = $C_{in}$ is required if regulator is located an appreciable distance from power supply filter.

** = $C_O$ is not needed for stability; however, it does improve transient response.

### ORDERING INFORMATION

| Nominal Output Voltage | Device |
|---|---|
| 5.0 V | TL780-05CKC |
| 12 V | TL780-12CKC |
| 15 V | TL780-15CKC |

**TL780 Series MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage | $V_{in}$ | 35 | Vdc |
| Power Dissipation and Thermal Characteristics | | | |
| $T_A = +25°C$ | $P_D$ | 2.0 | Watts |
| Derate above $T_A = +25°C$ | $1/\theta_{JA}$ | 16 | mW/°C |
| Thermal Resistance, Junction to Air | $\theta_{JA}$ | 62.5 | °C/W |
| $T_C = +25°C$ | $P_D$ | 15 | Watts |
| Derate above $T_C = +75°C$ (See Figure 1) | $1/\theta_{JC}$ | 200 | mW/°C |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | 5.0 | °C/W |
| Operating Junction Temperature Range | $T_J$ | 0 to +150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**TL780-05C**

**ELECTRICAL CHARACTERISTICS** ($V_{in} = 10$ V, $I_O = 500$ mA, $0°C \le T_J \le +125°C$ unless otherwise noted [Note 1])

| Characteristic | Symbol | TL780-05C | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Output Voltage | $V_O$ | | | | V |
| $5.0 \text{ mA} \le I_O \le 1.0$ A, $P \le 15$ W | | | | | |
| $7.0 \text{ V} \le V_{in} \le 20$ V | | | | | |
| $T_J = +25°C$ | | 4.95 | 5.0 | 5.05 | |
| $0°C \le T_J \le +125°C$ | | 4.90 | — | 5.10 | |
| Line Regulation ($T_J = +25°C$) | $Reg_{line}$ | | | | mV |
| $7.0 \text{ V} \le V_{in} \le 25$ V | | — | 0.5 | 5.0 | |
| $8.0 \text{ V} \le V_{in} \le 12$ V | | — | 0.5 | 5.0 | |
| Load Regulation ($T_J = +25°C$) | $Reg_{load}$ | | | | mV |
| $5.0 \text{ mA} \le I_O \le 1.5$ A | | — | 4.0 | 25 | |
| $250 \text{ mA} \le I_O \le 750$ mA | | — | 1.5 | 15 | |
| Ripple Rejection<br>$8.0 \text{ V} \le V_{in} \le 18$ V, f = 120 Hz | RR | 70 | 80 | — | dB |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 0.0035 | — | Ω |
| Average Temperature Coefficient of Output Voltage<br>$I_O = 5.0$ mA | $TCV_O$ | — | 0.06 | — | mV/°C |
| Output Noise Voltage ($T_J = +25°C$)<br>$10 \text{ Hz} \le f \le 100$ kHz | $V_n$ | — | 75 | — | μV |
| Dropout Voltage ($T_J = +25°C$)<br>$I_O = 1.0$ A | $V_{in}$-$V_O$ | — | 2.0 | — | V |
| Bias Current ($T_J = +25°C$) | $I_B$ | — | 3.5 | 8.0 | mA |
| Bias Current Change | $\Delta I_B$ | | | | mA |
| $7.0 \text{ V} \le V_{in} \le 25$ V, $I_O = 500$ mA | | — | 0.7 | 1.3 | |
| $5.0 \text{ mA} \le I_O \le 1.0$ A, $V_{in} = 10$ V | | — | 0.03 | 0.5 | |
| Short-Circuit Output Current ($T_J = +25°C$)<br>$V_{in} = 35$ V | $I_{sc}$ | — | 200 | — | mA |
| Peak Output Current ($T_J = +25°C$) | $I_P$ | — | 2.2 | — | A |

Note 1: Line and load regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

**TL780-12C**

**ELECTRICAL CHARACTERISTICS** ($V_{in} = 19$ V, $I_O = 500$ mA, $0°C \le T_J \le +125°C$ unless otherwise noted [Note 1])

| Characteristic | Symbol | TL780-12C | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Output Voltage | $V_O$ | | | | V |
| $5.0 \text{ mA} \le I_O \le 1.0$ A, $P \le 15$ W | | | | | |
| $14.5 \text{ V} \le V_{in} \le 27$ V | | | | | |
| $T_J = +25°C$ | | 11.88 | 12 | 12.12 | |
| $0°C \le T_J \le +125°C$ | | 11.76 | — | 12.24 | |
| Line Regulation ($T_J = +25°C$) | $Reg_{line}$ | | | | mV |
| $14.5 \text{ V} \le V_{in} \le 30$ | | — | 1.2 | 12 | |
| $16 \text{ V} \le V_{in} \le 22$ | | — | 1.2 | 12 | |

**(continued)**

### TL780-12C (continued)

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 19 V, $I_O$ = 500 mA, 0°C ≤ $T_J$ ≤ +125°C unless otherwise noted [Note 1])

| Characteristic | Symbol | TL780-12C | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Load Regulation ($T_J$ = +25°C)<br>5.0 mA ≤ $I_O$ ≤ 1.5 A<br>250 mA ≤ $I_O$ ≤ 750 mA | $Reg_{load}$ | <br>—<br>— | <br>6.5<br>2.5 | <br>60<br>36 | mV |
| Ripple Rejection<br>15 V ≤ $V_{in}$ ≤ 25 V, f = 120 Hz | RR | 65 | 77 | — | dB |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 0.0035 | — | Ω |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA | $TCV_O$ | — | 0.15 | — | mV/°C |
| Output Noise Voltage ($T_J$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 180 | — | μV |
| Dropout Voltage ($T_J$ = +25°C)<br>$I_O$ = 1.0 A | $V_{in}$-$V_O$ | — | 2.0 | — | V |
| Bias Current ($T_J$ = +25°C) | $I_B$ | — | 3.5 | 8.0 | mA |
| Bias Current Change<br>14.5 V ≤ $V_{in}$ ≤ 30 V, $I_O$ = 500 mA<br>5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 19 V | $\Delta I_B$ | <br>—<br>— | <br>0.4<br>0.03 | <br>1.3<br>0.5 | mA |
| Short-Circuit Output Current ($T_J$ = +25°C)<br>$V_{in}$ = 35 V | $I_{sc}$ | — | 200 | — | mA |
| Peak Output Current ($T_J$ = +25°C) | $I_P$ | — | 2.2 | — | A |

Note 1: Line and load regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

### TL780-15C

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 23 V, $I_O$ = 500 mA, 0°C ≤ $T_J$ ≤ +125°C unless otherwise noted [Note 1])

| Characteristic | Symbol | TL780-15C | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Output Voltage<br>5.0 mA ≤ $I_O$ ≤ 1.0 A, P ≤ 15 W<br>17.5 V ≤ $V_{in}$ ≤ 30 V<br>$T_J$ = +25°C<br>0°C ≤ $T_J$ ≤ +125°C | $V_O$ | <br><br><br>14.85<br>14.70 | <br><br><br>15<br>— | <br><br><br>15.15<br>15.30 | V |
| Line Regulation ($T_J$ = +25°C)<br>17.5 V ≤ $V_{in}$ ≤ 30 V<br>20 V ≤ $V_{in}$ ≤ 26 V | $Reg_{line}$ | <br>—<br>— | <br>1.5<br>1.5 | <br>15<br>15 | mV |
| Load Regulation ($T_J$ = +25°C)<br>5.0 mA ≤ $I_O$ ≤ 1.5 A<br>250 mA ≤ $I_O$ ≤ 750 mA | $Reg_{load}$ | <br>—<br>— | <br>7.0<br>2.5 | <br>75<br>45 | mV |
| Ripple Rejection<br>18.5 V ≤ $V_{in}$ ≤ 28.5 V, f = 120 Hz | RR | 60 | 75 | — | dB |
| Output Resistance (f = 1.0 kHz) | $r_O$ | — | 0.0035 | — | Ω |
| Average Temperature Coefficient of Output Voltage<br>$I_O$ = 5.0 mA | $TCV_O$ | — | 0.18 | — | mV/°C |
| Output Noise Voltage ($T_J$ = +25°C)<br>10 Hz ≤ f ≤ 100 kHz | $V_n$ | — | 225 | — | μV |
| Dropout Voltage ($T_J$ = +25°C)<br>$I_O$ = 1.0 A | $V_{in}$-$V_O$ | — | 2.0 | — | V |
| Bias Current ($T_J$ = +25°C) | $I_B$ | — | 3.6 | 8.0 | mA |
| Bias Current Change<br>17.5 V ≤ $V_{in}$ ≤ 30 V, $I_O$ = 500 mA<br>5.0 mA ≤ $I_O$ ≤ 1.0 A, $V_{in}$ = 23 V | $\Delta I_B$ | <br>—<br>— | <br>0.4<br>0.02 | <br>1.3<br>0.5 | mA |
| Short-Circuit Output Current ($T_J$ = +25°C)<br>$V_{in}$ = 35 V | $I_{sc}$ | — | 200 | — | mA |
| Peak Output Current ($T_J$ = +25°C) | $I_P$ | — | 2.2 | — | A |

Note 1: Line and load regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## TYPICAL PERFORMANCE CHARACTERISTICS

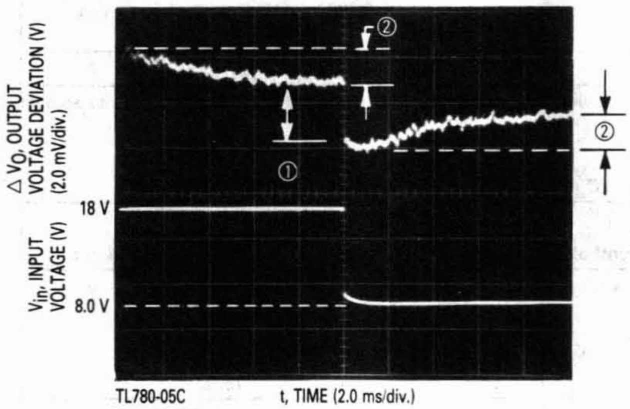
### VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

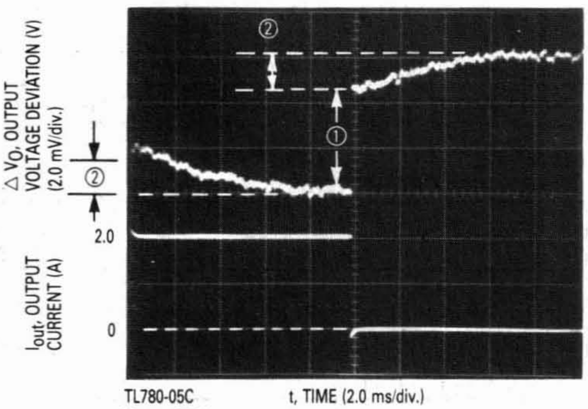
Figure 1 shows the line and thermal regulation response of a typical TL780-05C to a 10 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical TL780-05C to a 15 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION



TL780-05C
$V_O = 5.0$ V
$V_{in} = 8.0\text{ V} \rightarrow 18\text{ V} \rightarrow 8.0\text{ V}$ ① = $Reg_{line} = 2.4$ mV
$I_{out} = 1.0$ A ② = $Reg_{therm} = 0.0030\%\ V_O/W$

FIGURE 2 — LOAD AND THERMAL REGULATION



TL780-05C
$V_O = 5.0$ V
$V_{in} = 15$ ① = $Reg_{line} = 4.4$ mV
$I_{out} = 0\text{ A} \rightarrow 1.5\text{ A} \rightarrow 0\text{ A}$ ② = $Reg_{therm} = 0.0020\%\ V_O/W$

FIGURE 3 — TEMPERATURE STABILITY

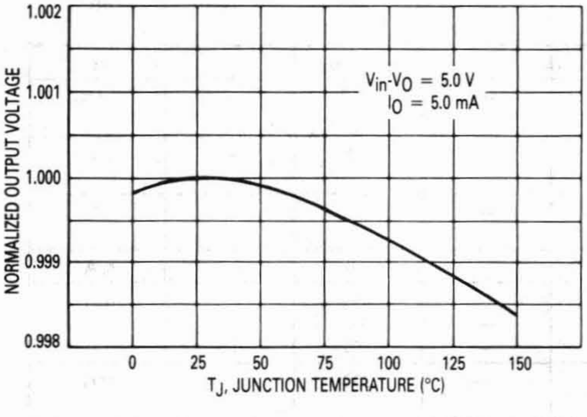


FIGURE 4 — OUTPUT IMPEDANCE

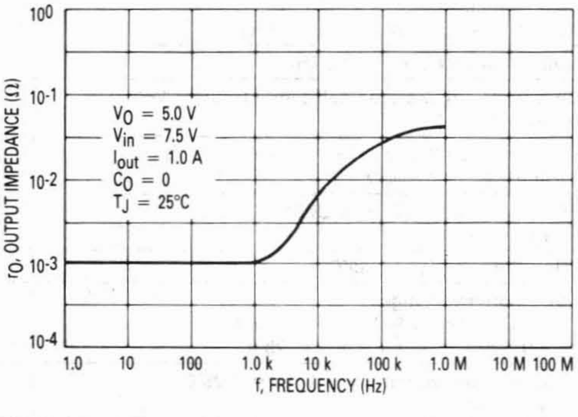


**FIGURE 5 — RIPPLE REJECTION versus FREQUENCY**

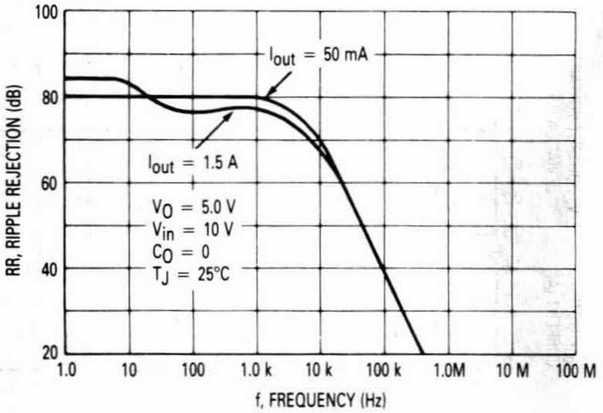


**FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT**

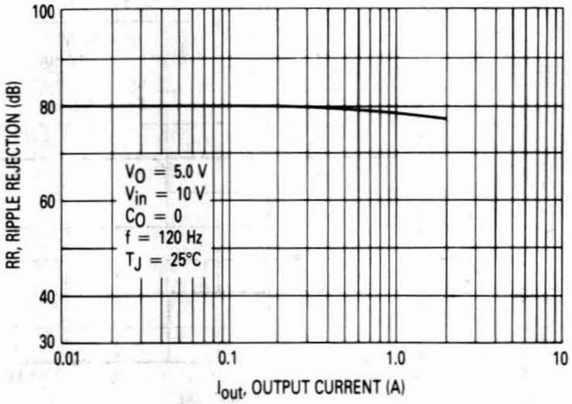


**FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE**

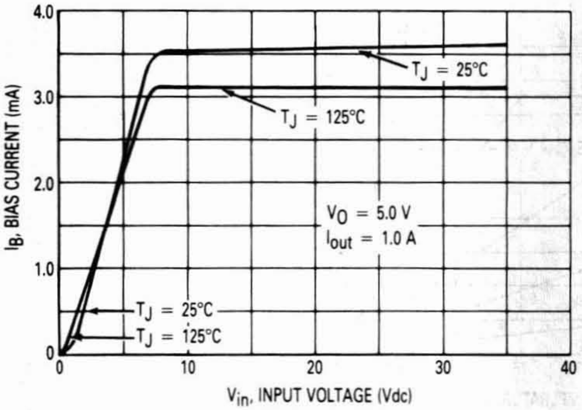


**FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT**

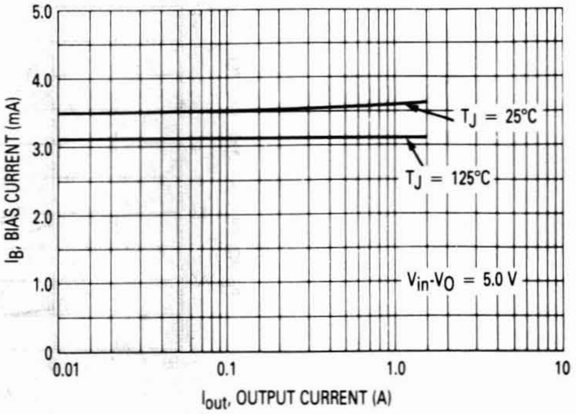


**FIGURE 9 — DROPOUT VOLTAGE**

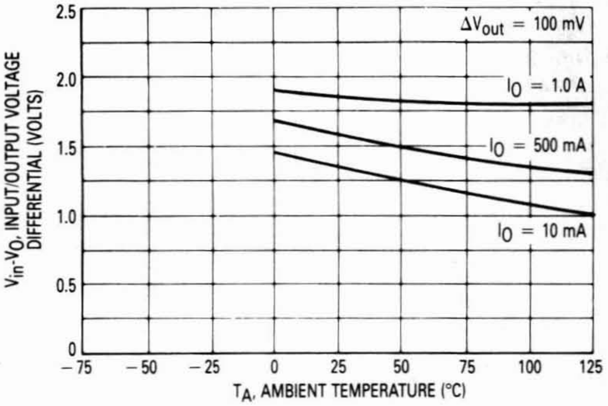


**FIGURE 10 — PEAK OUTPUT CURRENT**

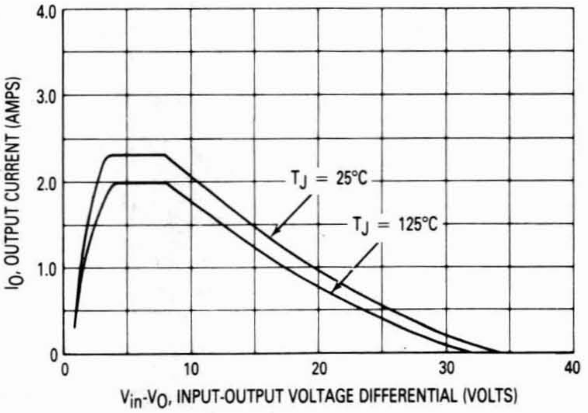


**FIGURE 11 — LINE TRANSIENT RESPONSE**

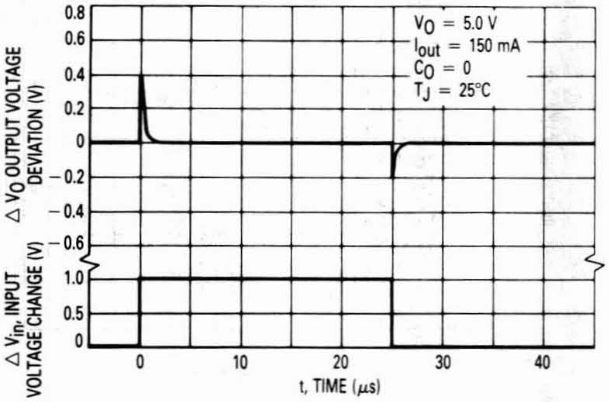


**FIGURE 12 — LOAD TRANSIENT RESPONSE**

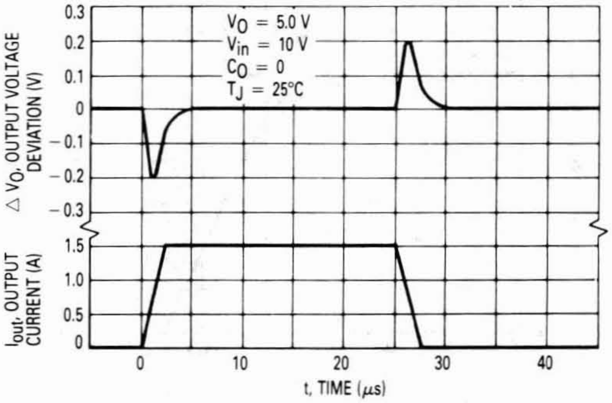
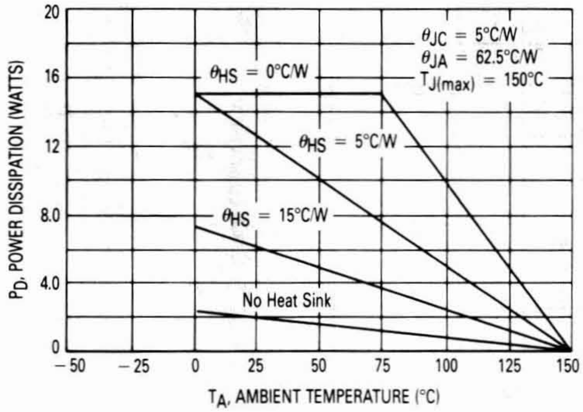


**FIGURE 13 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE**



# μA78S40

## Specifications and Applications Information

### UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

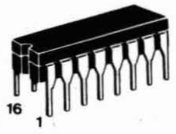
**SILICON MONOLITHIC INTEGRATED CIRCUIT**

### UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

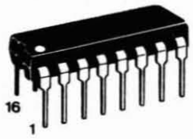
The μA78S40 is a monolithic-switching regulator subsystem, providing all active functions necessary for a switching regulator system. The device consists of a temperature compensated voltage reference, controlled-duty cycle oscillator with an active current limit circuit, comparator, high-current and high-voltage output switch, capable of 1.5 A and 40 V, pinned-out power diode and an uncommitted operational amplifier, which can be powered up or down independent of the IC supply. The switching output can drive external NPN or PNP transistors when voltages greater than 40 V, or currents in excess of 1.5 A, are required. Some of the features are wide-supply voltage range, low standby current, high efficiency and low drift. The μA78S40 is available in both commercial (0°C to +70°C) and military (−55°C to +125°C) temperature ranges.

Some of the applications include use in step-up, step-down, and inverting regulators, with extremely good results obtained in battery-operated systems.

- Output Adjustable from 1.25 V to 40 V
- Peak Output Current of 1.5 A Without External Transistor
- 80 dB Line and Load Regulation
- Operation from 2.5 V to 40 V Supply
- Low Standby Current Drain
- High Gain, High Output Current, Uncommitted Op Amp

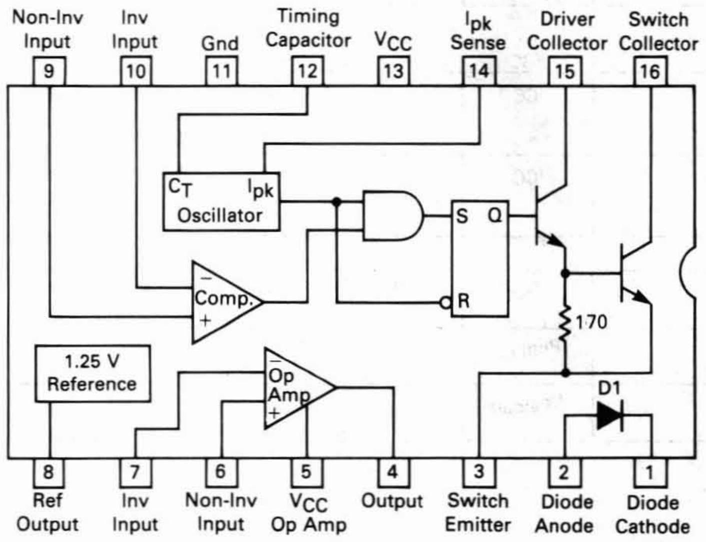


**D SUFFIX**
CERAMIC PACKAGE
CASE 620-02



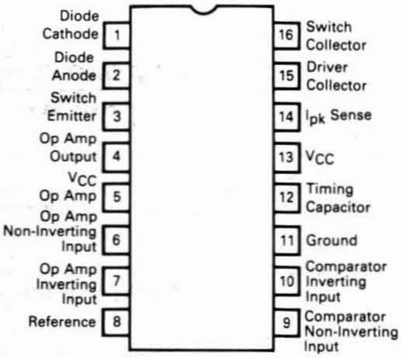
**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### BLOCK DIAGRAM


Non-Inv Input
9
Inv Input
10
Gnd
11
Timing Capacitor
12
$V_{CC}$
13
$I_{pk}$ Sense
14
Driver Collector
15
Switch Collector
16
$C_T$
$I_{pk}$
Oscillator
S
Q
R
Comp.
−
+
170
1.25 V Reference
Op Amp
−
+
D1
8
Ref Output
7
Inv Input
6
Non-Inv Input
5
$V_{CC}$ Op Amp
4
Output
3
Switch Emitter
2
Diode Anode
1
Diode Cathode

(Bottom View)

### PIN CONNECTIONS


Diode Cathode
1
Diode Anode
2
Switch Emitter
3
Op Amp Output
4
$V_{CC}$ Op Amp
5
Op Amp Non-Inverting Input
6
Op Amp Inverting Input
7
Reference
8
Switch Collector
16
Driver Collector
15
$I_{pk}$ Sense
14
$V_{CC}$
13
Timing Capacitor
12
Ground
11
Comparator Inverting Input
10
Comparator Non-Inverting Input
9

(Top View)

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| μA78S40PC | 0°C to +70°C | Plastic DIP |
| μA78S40DC | 0°C to +70°C | Ceramic DIP |
| μA78S40DM | −55°C to +125°C | Ceramic DIP |

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 40 | V |
| Op Amp Power Supply Voltage | $V_{CC}$ (Op Amp) | 40 | V |
| Common Mode Input Range (Comparator and Op Amp) | $V_{ICR}$ | $-0.3$ to $V_{CC}$ | V |
| Differential Input Voltage (Note 2) | $V_{ID}$ | ±30 | V |
| Output Short-Circuit Duration (Op Amp) | — | Continuous | — |
| Reference Output Current | $I_{ref}$ | 10 | mA |
| Voltage from Switch Collectors to Gnd | — | 40 | V |
| Voltage from Switch Emitters to Gnd | — | 40 | V |
| Voltage from Switch Collectors to Emitter | — | 40 | V |
| Voltage from Power Diode to Gnd | — | 40 | V |
| Reverse-Power Diode Voltage | $V_{DR}$ | 40 | V |
| Current through Power Switch | $I_{SW}$ | 1.5 | A |
| Current through Power Diode | $I_D$ | 1.5 | A |
| Power Dissipation and Thermal Characteristics<br>Plastic Package — $T_A = +25°C$<br>Derate above +25°C (Note 1)<br>Ceramic Package — $T_A = 25°C$<br>Derate above +25°C (Note 1) | <br>$P_D$<br>$1/R_{\theta JA}$<br>$P_D$<br>$1/R_{\theta JA}$ | <br>1500<br>14<br>1000<br>8.0 | <br>mW<br>mW/°C<br>mW<br>mW/°C |
| Storage Temperature Range | $T_{stg}$ | $-65$ to $+150$ | °C |
| Operating Temperature Range<br>μA78S40M<br>μA78S40C | $T_A$ | <br>$-55$ to $+125$<br>0 to +70 | °C |

**Notes:**

1. $T_{low}$ = −55°C for μA78S40DM
   = 0°C for μA78S40DC and μA78S40PC
   $T_{high}$ = +125°C for μA78S40DM
   = +70°C for μA78S40DC and μA78S40PC
2. For supply voltages less than 30 V the maximum differential input voltage (Error Amp and Op Amp) is equal to the supply voltage.

**ELECTRICAL CHARACTERISTICS** ($V_{CC} = V_{CC}$ (Op Amp) = 5.0 V, $T_A = T_{low}$ to $T_{high}$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **GENERAL** | | | | | |
| Supply Voltage | $V_{CC}$ | 2.5 | — | 40 | V |
| Supply Current (Op Amp $V_{CC}$ Disconnected)<br>($V_{CC}$ = 5.0 V)<br>($V_{CC}$ = 40 V) | $I_{CC}$ | <br>—<br>— | <br>1.8<br>2.3 | <br>3.5<br>5.0 | mA |
| Supply Current (Op Amp $V_{CC}$ Connected)<br>($V_{CC}$ = 5.0 V)<br>($V_{CC}$ = 40 V) | $I_{CC}$ | <br>—<br>— | <br>—<br>— | <br>4.0<br>5.5 | mA |
| **REFERENCE** | | | | | |
| Reference Voltage ($I_{ref}$ = 1.0 mA) | $V_{ref}$ | 1.180 | 1.245 | 1.310 | V |
| Reference Voltage Line Regulation (3.0 V ≤ $V_{CC}$ ≤ 40 V, $I_{ref}$ = 1.0 mA, $T_A$ = 25°C) | $Reg_{line}$ | — | 0.04 | 0.2 | mV/V |
| Reference Voltage Load Regulation (1.0 mA ≤ $I_{ref}$ ≤ 10 mA, $T_A$ = 25°C) | $Reg_{load}$ | — | 0.2 | 0.5 | mV/mA |

**ELECTRICAL CHARACTERISTICS** (Continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | |
| Charging Current ($T_A$ = 25°C)<br>($V_{CC}$ = 5.0 V)<br>($V_{CC}$ = 40 V) | $I_{chg}$ | <br>20<br>20 | <br>—<br>— | <br>50<br>70 | μA |
| Discharge Current ($T_A$ = 25°C)<br>($V_{CC}$ = 5.0 V)<br>($V_{CC}$ = 40 V) | $I_{dis}$ | <br>150<br>150 | <br>—<br>— | <br>250<br>350 | μA |
| Oscillator Voltage Swing ($T_A$ = 25°C)<br>($V_{CC}$ = 5.0 V) | $V_{osc}$ | — | 0.5 | — | V |
| Ratio of Charge/Discharge Time | $t_{chg}/t_{dis}$ | — | 6.0 | — | — |
| **CURRENT LIMIT** | | | | | |
| Current-Limit Sense Voltage ($T_A$ = 25°C)<br>($V_{CC}$ − $V_{Ipk}$ Sense) | $V_{CLS}$ | 250 | — | 350 | mV |
| **OUTPUT SWITCH** | | | | | |
| Output Saturation Voltage 1<br>($I_{SW}$ = 1.0 A, Pin 15 tied to Pin 16) | $V_{sat1}$ | — | 0.93 | 1.3 | V |
| Output Saturation Voltage 2<br>($I_{SW}$ = 1.0 A, $I_{15}$ = 50 mA) | $V_{sat2}$ | — | 0.5 | 0.7 | V |
| Output Transistor Current Gain ($T_A$ = 25°C)<br>($I_C$ = 1.0 A, $V_{CE}$ = 5.0 V) | $h_{FE}$ | — | 70 | — | — |
| Output Leakage Current ($T_A$ = 25°C)<br>($V_{CE}$ = 40 V) | $I_{C(off)}$ | — | 10 | — | nA |
| **POWER DIODE** | | | | | |
| Forward Voltage Drop ($I_D$ = 1.0 A) | $V_D$ | — | 1.25 | 1.5 | V |
| Diode Leakage Current ($T_A$ = 25°C) ($V_{DR}$ = 40 V) | $I_{DR}$ | — | 10 | — | nA |
| **COMPARATOR** | | | | | |
| Input Offset Voltage ($V_{CM}$ = $V_{Ref}$) | $V_{IO}$ | — | 1.5 | 15 | mV |
| Input Bias Current ($V_{CM}$ = $V_{Ref}$) | $I_{IB}$ | — | 35 | 200 | nA |
| Input Offset Current ($V_{CM}$ = $V_{Ref}$) | $I_{IO}$ | — | 5.0 | 75 | nA |
| Common-Mode Voltage Range ($T_A$ = 25°C) | $V_{ICR}$ | 0 | — | $V_{CC}$ − 2.0 | V |
| Power-Supply Rejection Ratio ($T_A$ = 25°C)<br>(3.0 ≤ $V_{CC}$ ≤ 40 V) | PSRR | 70 | 96 | — | dB |
| **OUTPUT OPERATIONAL AMPLIFIER** | | | | | |
| Input Offset Voltage ($V_{CM}$ = 2.5 V) | $V_{IO}$ | — | 4.0 | 15 | mV |
| Input Bias Current ($V_{CM}$ = 2.5 V) | $I_{IB}$ | — | 30 | 200 | nA |
| Input Offset Current ($V_{CM}$ = 2.5 V) | $I_{IO}$ | — | 5.0 | 75 | nA |
| Voltage Gain + ($T_A$ = 25°C)<br>($R_L$ = 2.0 kΩ to Gnd, 1.0 V ≤ $V_O$ ≤ 2.5 V) | $A_{VOL+}$ | 25 | 250 | — | V/mV |
| Voltage Gain − ($T_A$ = 25°C)<br>($R_L$ = 2.0 kΩ to $V_{CC}$ (Op Amp), 1.0 V ≤ $V_O$ ≤ 2.5 V) | $A_{VOL-}$ | 25 | 250 | — | V/mV |
| Common-Mode Voltage Range ($T_A$ = 25°C) | $V_{ICR}$ | 0 | — | $V_{CC}$ − 2.0 | V |
| Common-Mode Rejection Ratio ($T_A$ = 25°C)<br>($V_{CM}$ = 0 to 3.0 V) | CMRR | 76 | 100 | — | dB |
| Power-Supply Rejection Ratio ($T_A$ = 25°C)<br>(3.0 V ≤ $V_{CC}$ (Op Amp) ≤ 40 V) | PSRR | 76 | 100 | — | dB |
| Output Source Current ($T_A$ = 25°C) | $I_{Source}$ | 75 | 150 | — | mA |
| Output Sink Current ($T_A$ = 25°C) | $I_{Sink}$ | 10 | 35 | — | mA |
| Slew Rate ($T_A$ = 25°C) | SR | — | 0.6 | — | V/μs |
| Output Low Voltage ($T_A$ = 25°C, $I_L$ = −5.0 mA) | $V_{OL}$ | — | — | 1.0 | V |
| Output High Voltage ($T_A$ = 25°C, $I_L$ = 50 mA) | $V_{OH}$ | $V_{CC}$ (Op Amp) −3.0 | — | — | V |

**FIGURE 1 — OUTPUT SWITCH ON/OFF TIME versus OSCILLATOR TIMING CAPACITOR**

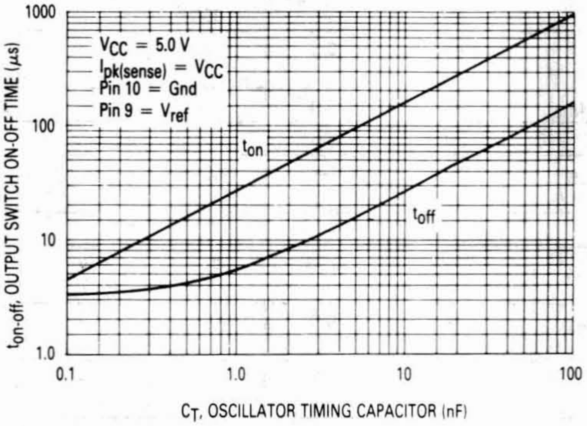


**FIGURE 2 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE**

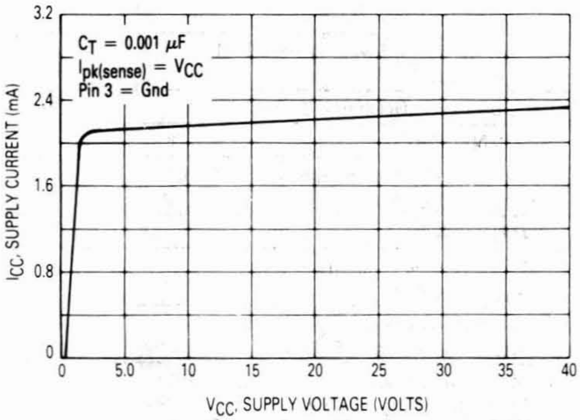


**FIGURE 3 — EMITTER-FOLLOWER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus EMITTER CURRENT**

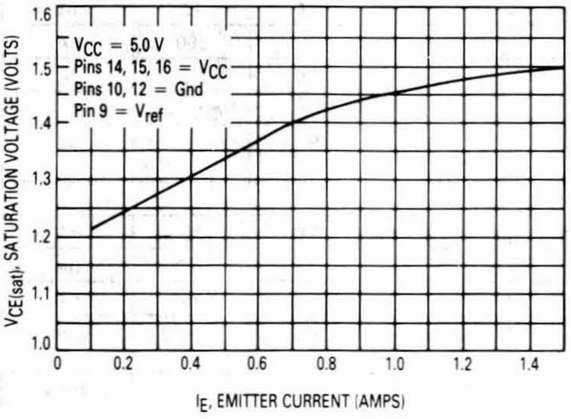


**FIGURE 4 — COMMON-EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT**

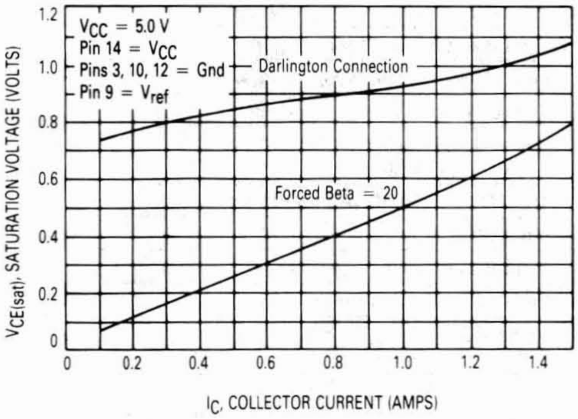


FIGURE 5 — STEP-DOWN CONVERTER

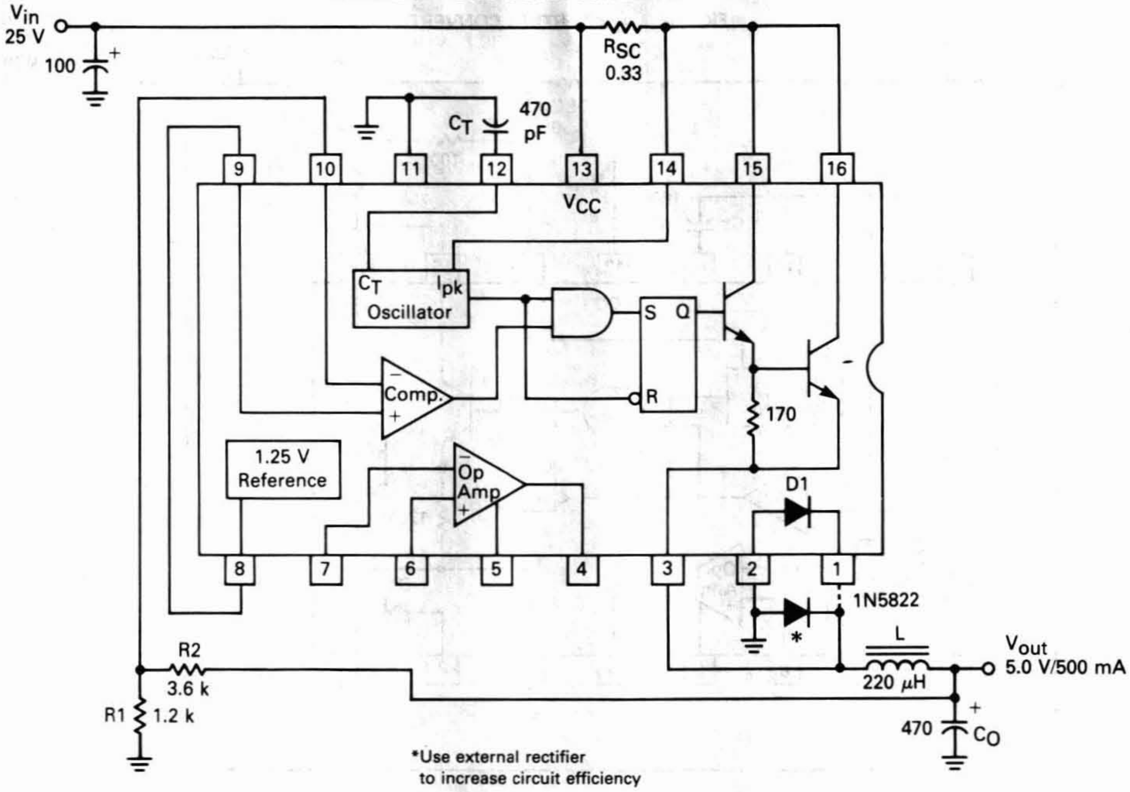

Vin
25 V
100
+
RSC
0.33
CT
470
pF
9
10
11
12
13
14
15
16
VCC
CT
Ipk
Oscillator
S
Q
R
Comp.
−
+
170
1.25 V
Reference
Op
Amp
−
+
D1
8
7
6
5
4
3
2
1
1N5822
*
L
Vout
5.0 V/500 mA
R2
3.6 k
220 μH
R1
1.2 k
470
+
CO
*Use external rectifier
to increase circuit efficiency

FIGURE 6 — STEP-UP CONVERTER

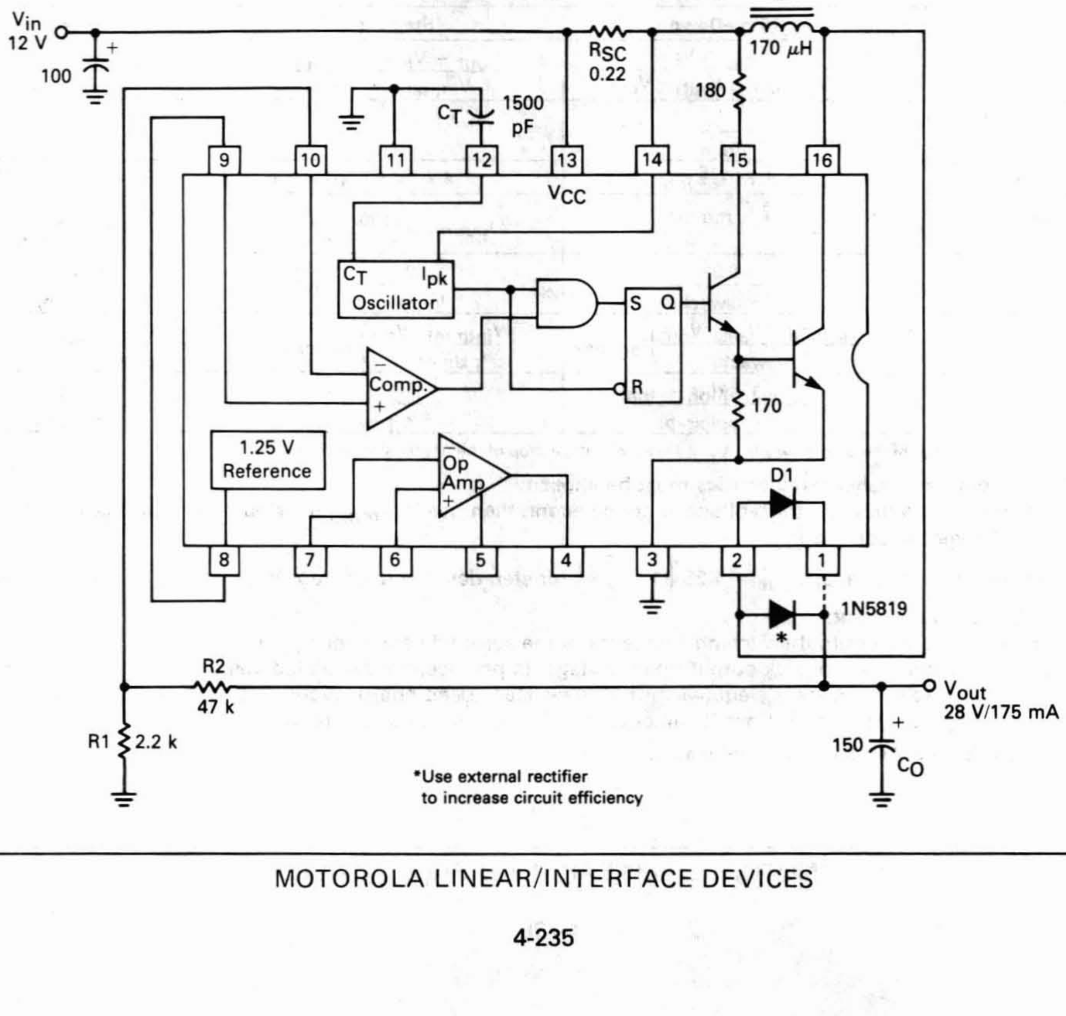

Vin
12 V
+
100
RSC
0.22
L
170 μH
180
CT
1500
pF
9
10
11
12
13
14
15
16
VCC
CT
Ipk
Oscillator
S
Q
R
Comp.
−
+
170
1.25 V
Reference
Op
Amp
−
+
D1
8
7
6
5
4
3
2
1
1N5819
*
R2
47 k
Vout
28 V/175 mA
R1
2.2 k
+
150
CO
*Use external rectifier
to increase circuit efficiency

FIGURE 7 — INVERTING CONVERTER

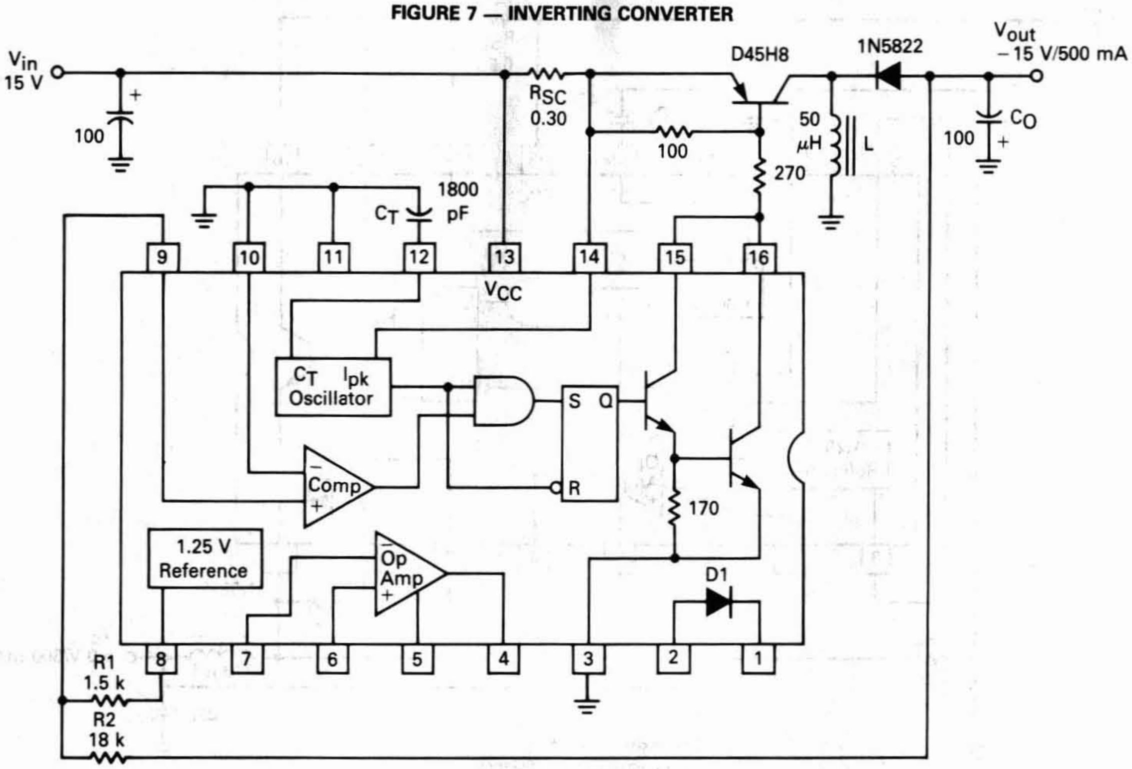


FIGURE 8 — DESIGN FORMULA TABLE

| Calculation | Step-Down | Step-Up | Inverting |
|---|---|---|---|
| $\frac{t_{on}}{t_{off}}$ | $\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$ | $\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$ | $\frac{\lvert V_{out}\rvert + V_F}{V_{in(min)} - V_{sat}}$ |
| $(t_{on} + t_{off})$ max | $\frac{I}{f_{min}}$ | $\frac{I}{f_{min}}$ | $\frac{I}{f_{min}}$ |
| $C_T$ | $4 \times 10^{-5}\ t_{on}$ | $4 \times 10^{-5}\ t_{on}$ | $4 \times 10^{-5}\ t_{on}$ |
| $I_{pk(switch)}$ | $2\ I_{out(max)}$ | $2\ I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$ | $2\ I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$ |
| $R_{SC}$ | $\frac{0.33}{I_{pk(switch)}}$ | $\frac{0.33}{I_{pk(switch)}}$ | $\frac{0.33}{I_{pk(switch)}}$ |
| $L_{(min)}$ | $\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$ | $\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$ | $\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$ |
| $C_O$ | $\frac{I_{pk(switch)}(t_{on} + t_{off})}{8\ V_{ripple(p\text{-}p)}}$ | $\approx \frac{I_{out}\ t_{on}}{V_{ripple}}$ | $\approx \frac{I_{out}\ t_{on}}{V_{ripple}}$ |

$V_{sat}$ = Saturation voltage of the output switch. $V_F$ = Forward voltage drop of the ringback rectifier.

**The following power supply characteristics must be chosen:**

**$V_{in}$** — Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up and inverting convertor.

**$V_{out}$** — Desired output voltage, $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$ for step-down and step-up; $V_{out} = \frac{1.25\ R2}{R1}$ for Inverting.

**$I_{out}$** — Desired output current.

**$f_{min}$** — Minimum desired output switching frequency at the selected values for $V_{in}$ and $I_O$.

**$V_{ripple(p\text{-}p)}$** — Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

**See Application Note AN920A for further information.**

# LM285
# LM385

## MICROPOWER VOLTAGE REFERENCE DIODES

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

**ORDERING INFORMATION**

| Device | Temp. Range | Reverse Breakdown Voltage | Tolerance |
|---|---|---|---|
| LM285Z-1.2 | −40°C to +85°C | 1.235 Volts | ±1.0% |
| LM285Z-2.5 | −40°C to +85°C | 2.500 Volts | ±1.5% |
| LM385BZ-1.2 | 0°C to +70°C | 1.235 Volts | ±1.0% |
| LM385Z-1.2 | 0°C to +70°C | 1.235 Volts | ±2.0% |
| LM385BZ-2.5 | 0°C to +70°C | 2.500 Volts | ±1.5% |
| LM385Z-2.5 | 0°C to +70°C | 2.500 Volts | ±3.0% |

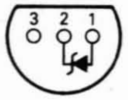
## MICROPOWER VOLTAGE REFERENCE DIODES

The LM285/LM385 series are micropower two-terminal band-gap voltage regulator diodes. Designed to operate over a wide current range of 10 μA to 20 mA, these devices feature exceptionally low dynamic impedance, low noise and stable operation over time and temperature. Tight voltage tolerances are achieved by on-chip trimming. The large dynamic operating range enables these devices to be used in applications with widely varying supplies with excellent regulation. Extremely low operating current make these devices ideal for micropower circuitry like portable instrumentation, regulators and other analog circuitry where extended battery life is required.

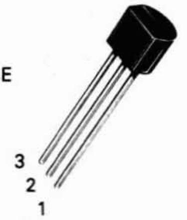
The LM285/LM385 series are packaged in a low cost TO-226AA (TO-92) plastic case and are available in two voltage versions of 1.235 and 2.500 volts as denoted by the device suffix (see ordering information table). The LM285 is specified over a −40°C to +85°C temperature range while the LM385 is rated from 0°C to +70°C.

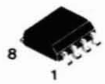
- Operating Current from 10 μA to 20 mA
- 1.0%, 1.5%, 2.0% and 3.0% Initial Tolerance Grades
- Low Temperature Coefficient
- 1.0 Ω Dynamic Impedance
- Available in 1.235 and 2.500 Volt Versions

**Z SUFFIX**
CASE 29-02
TO-226AA
(TO-92)
PLASTIC PACKAGE



(Bottom View)

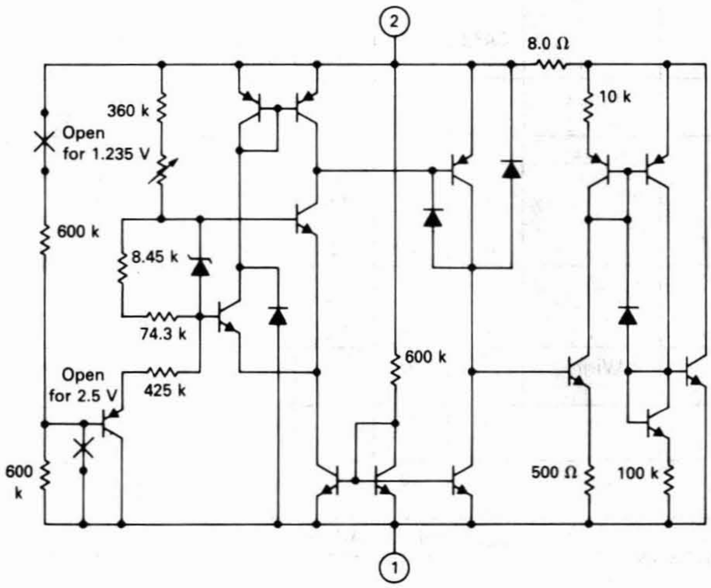




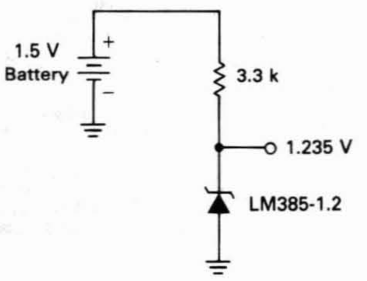
**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8*

***Surface Mount pin-out is different than standard package pin-out for this device. Please refer to Chapter 7 for details.**

### EQUIVALENT CIRCUIT SCHEMATIC



### STANDARD APPLICATION



**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Reverse Current | $I_R$ | 30 | mA |
| Forward Current | $I_F$ | 10 | mA |
| Operating Ambient Temperature Range | $T_A$ | | °C |
| LM285 | | −40 to +85 | |
| LM385 | | 0 to +70 | |
| Operating Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25° unless otherwise noted)

| Characteristic | Symbol | LM285-1.2 | | | LM385-1.2/LM385B-1.2 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Reverse Breakdown Voltage<br>$I_{Rmin} \le I_R \le 20$ mA | $V_{(BR)R}$ | | | | | | | V |
| LM285-1.2/LM385B-1.2 | | 1.223 | 1.235 | 1.247 | 1.223 | 1.235 | 1.247 | |
| LM385-1.2 | | — | — | — | 1.205 | 1.235 | 1.260 | |
| Minimum Operating Current<br>($T_A = T_{low}$ to $T_{high}$ Note 1) | $I_{Rmin}$ | — | 2.5 | 10 | — | 2.5 | 15 | µA |
| Reverse Breakdown Voltage Change with Current | $\Delta V_{(BR)}/\Delta I_R$ | | | | | | | mV |
| $I_{Rmin} \le I_R \le 1.0$ mA, $T_A$ = +25°C | | — | — | 1.0 | — | — | 1.0 | |
| $T_A = T_{low}$ to $T_{high}$ (Note 1) | | — | — | 1.5 | — | — | 1.5 | |
| 1.0 mA $\le I_R \le 20$ mA, $T_A$ = +25°C | | — | — | 10 | — | — | 20 | |
| $T_A = T_{low}$ to $T_{high}$ (Note 1) | | — | — | 20 | — | — | 25 | |
| Reverse Dynamic Impedance | z | | | | | | | Ω |
| $I_R$ = 100 µA, $T_A$ = +25°C | | — | 0.2 | 0.6 | — | 0.4 | 1.0 | |
| $T_A = T_{low}$ to $T_{high}$ (Note 1) | | — | — | 1.5 | — | — | 1.5 | |
| Average Temperature Coefficient<br>10 µA $\le I_R \le 20$ mA, $T_A = T_{low}$ to $T_{high}$ (Note 1) | $\Delta V_{(BR)}/\Delta T$ | — | 20 | — | — | 20 | — | ppm/°C |
| Wideband Noise (RMS)<br>$I_R$ = 100 µA, 10 Hz ≤ f ≤ 10 kHz | n | — | 60 | — | — | 60 | — | µV |
| Long Term Stability<br>$I_R$ = 100 µA, $T_A$ = +25°C ±0.1°C | S | — | 20 | — | — | 20 | — | ppm/kHR |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25° unless otherwise noted)

| Characteristic | Symbol | LM285-2.5 | | | LM385-2.5/LM385B-2.5 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Reverse Breakdown Voltage<br>20 µA $\le I_R \le 20$ mA | $V_{(BR)R}$ | | | | | | | V |
| LM285-2.5/LM385B-2.5 | | 2.462 | 2.5 | 2.538 | 2.462 | 2.5 | 2.538 | |
| LM385-2.5 | | — | — | — | 2.425 | 2.5 | 2.575 | |
| Minimum Operating Current<br>$T_A = T_{low}$ to $T_{high}$ (Note 1) | $I_{Rmin}$ | — | 5.0 | 20 | — | 5.0 | 20 | µA |
| Reverse Breakdown Voltage Change with Current | $\Delta V_{(BR)}/\Delta I_R$ | | | | | | | mV |
| 20 µA $\le I_R \le 1.0$ mA, $T_A$ = +25°C | | — | — | 1.0 | — | — | 2.0 | |
| $T_A = T_{low}$ to $T_{high}$ (Note 1) | | — | — | 1.5 | — | — | 2.5 | |
| 1.0 mA $\le I_R \le 20$ mA, $T_A$ = +25°C | | — | — | 10 | — | — | 20 | |
| $T_A = T_{low}$ to $T_{high}$ (Note 1) | | — | — | 20 | — | — | 25 | |
| Reverse Dynamic Impedance | z | | | | | | | Ω |
| $I_R$ = 100 µA, $T_A$ = +25°C | | — | 0.2 | 0.6 | — | 0.4 | 1.0 | |
| $T_A = T_{low}$ to $T_{high}$ (Note 1) | | — | — | 1.5 | — | — | 1.5 | |
| Average Temperature Coefficient<br>20 µA $\le I_R \le 20$ mA, $T_A = T_{low}$ to $T_{high}$ (Note 1) | $\Delta V_{(BR)}/\Delta T$ | — | 20 | — | — | 20 | — | ppm/°C |
| Wideband Noise (RMS)<br>$I_R$ = 100 µA, 10 Hz ≤ f ≤ 10 kHz | n | — | 120 | — | — | 120 | — | µV |
| Long Term Stability<br>$I_R$ = 100 µA, $T_A$ = +25°C ±0.1°C | S | — | 20 | — | — | 20 | — | ppm/kHR |

**NOTES:** 1. $T_{low}$ = −40°C for LM285-1.2, LM285-2.5
= 0°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5

$T_{high}$ = +85°C for LM285-1.2, LM285-2.5
= +70°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5

## TYPICAL PERFORMANCE CURVES FOR LM285-1.2/385-1.2/385B-1.2

FIGURE 1 — REVERSE CHARACTERISTICS

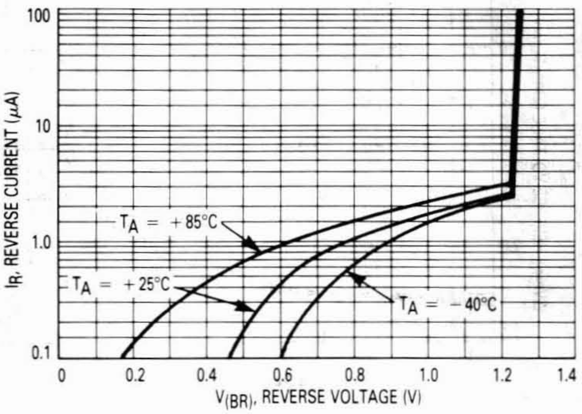


FIGURE 2 — REVERSE CHARACTERISTICS

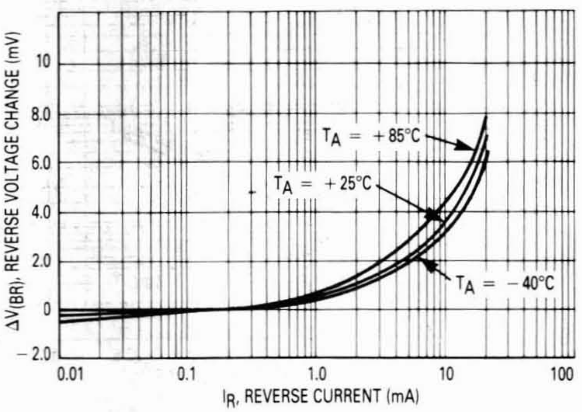


FIGURE 3 — FORWARD CHARACTERISTICS

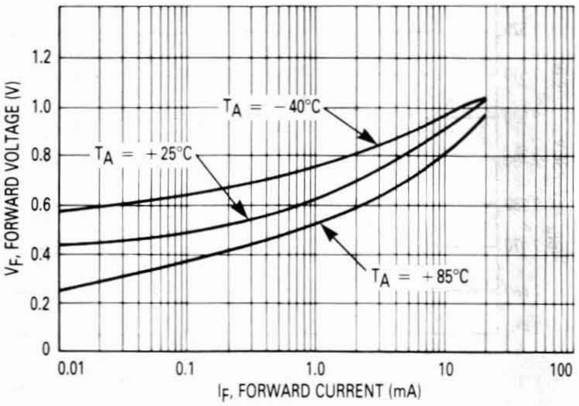


FIGURE 4 — TEMPERATURE DRIFT

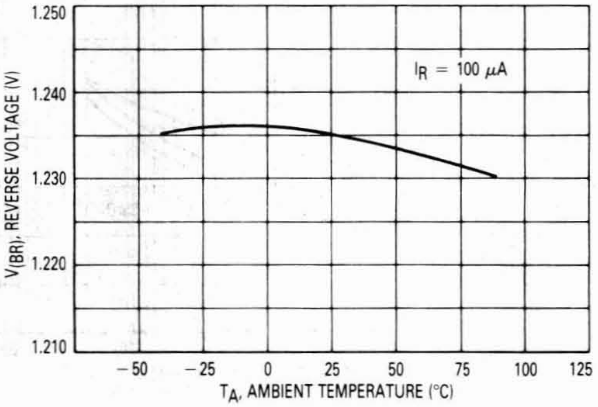


FIGURE 5 — NOISE VOLTAGE

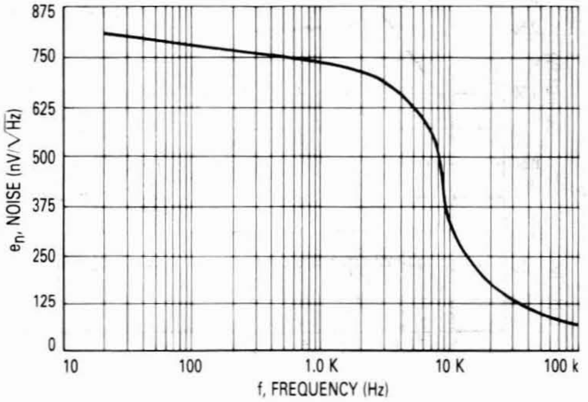
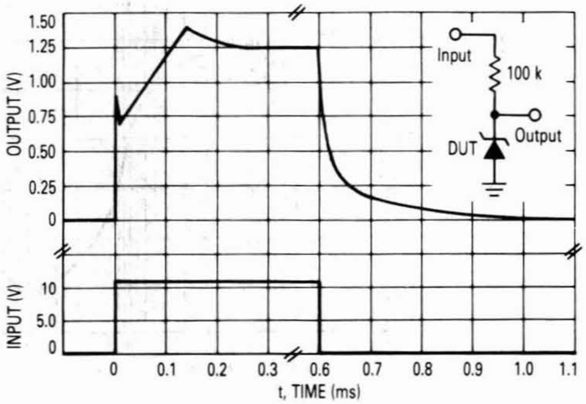


FIGURE 6 — RESPONSE TIME



## TYPICAL PERFORMANCE CURVES FOR LM285-2.5/385-2.5/385B-2.5

FIGURE 7 — REVERSE CHARACTERISTICS

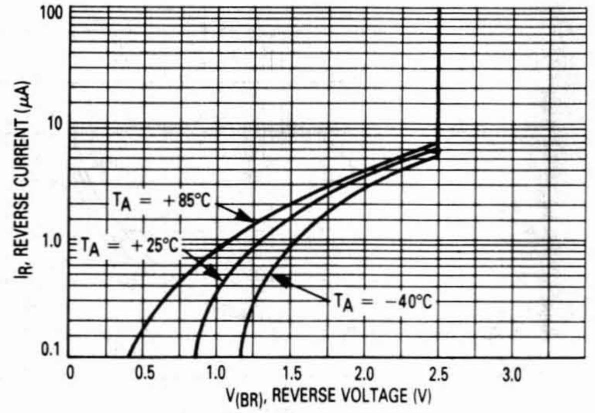


FIGURE 8 — REVERSE CHARACTERISTICS

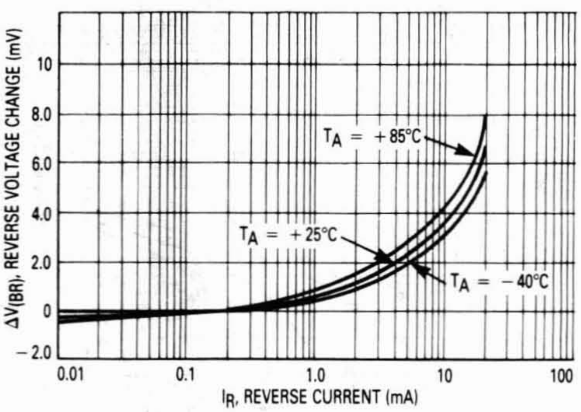


FIGURE 9 — FORWARD CHARACTERISTICS

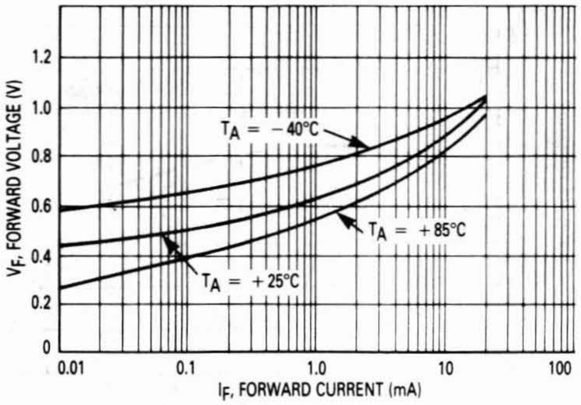


FIGURE 10 — TEMPERATURE DRIFT

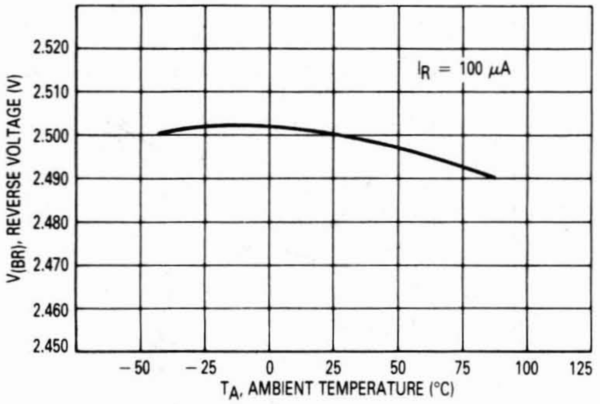


FIGURE 11 — NOISE VOLTAGE

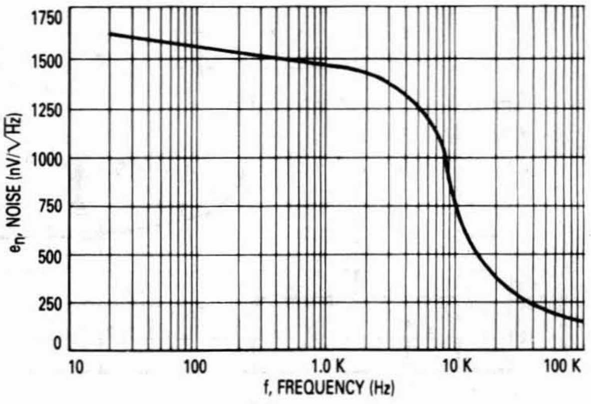
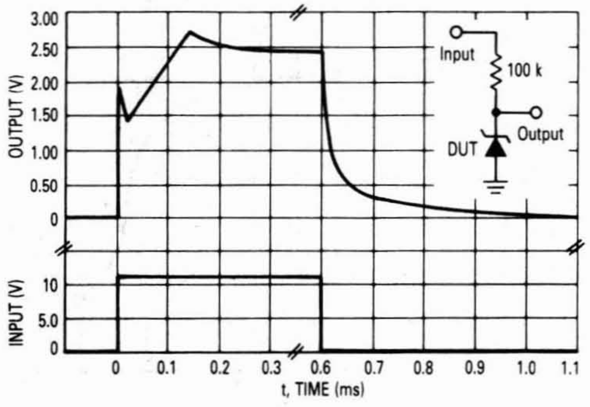


FIGURE 12 — RESPONSE TIME



# MC1400
# MC1500

## Specification and Applications Information

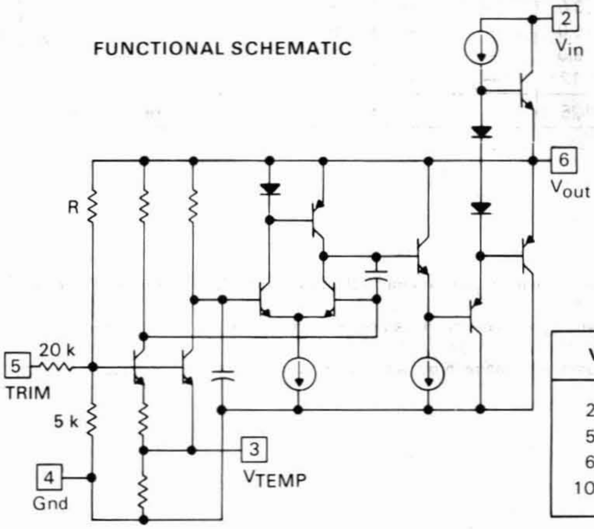
### TIGHT-TOLERANCE, LOW-DRIFT VOLTAGE REFERENCE FAMILY

The MC1400 series of ICs is a family of temperature-compensated voltage references for precision data conversion and instrumentation applications. Advances in thin-film resistors, laser-trimming techniques, ion-implanted devices, and monolithic fabrication techniques make this reference both temperature and time stable in applications demanding accuracy to the 12-bit level.

These devices offer simple, no-external-component operation as three-terminal, positive-voltage references, and also simple, one-external-resistor operation as either positive or negative references. Unique circuitry permits these devices to either source or sink greater than 10 mA of load current with excellent regulation. This feature means that the buffer amplifiers and current sources normally required for precision zener references can be eliminated.

- Four Different Output Voltages: 2.5, 5.0, 6.25, 10 V
- Tight Absolute Accuracy: ±0.2% Maximum Initial Tolerance
- Single-Component Output Trimming Without Degrading Temperature Coefficient
- Wide Input Voltage Range: $(V_{out} + 1.0\ V) \leq V_{in} \leq 40\ V$
- Three-Terminal Operation:
  - Positive References That Can Source and Sink Current
- Two-Terminal Operation:
  - Positive or Negative References
  - Floating References
- Low Current Consumption: 1.0 mA Typical
- Very Low Temperature Coefficient
- Low Output Noise Voltage
- Excellent Ripple Rejection: 87 dB Typical at 120 Hz
- Excellent Long Term Stability: 25 ppm/1000 Hrs Typical

FUNCTIONAL SCHEMATIC



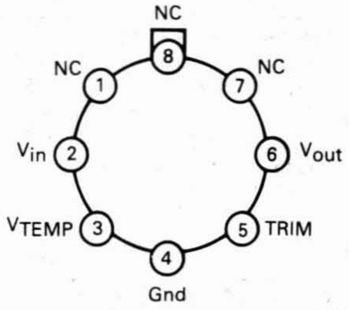
| $V_{out}$ | R |
|---|---|
| 2.5 V | 5 kΩ |
| 5.0 V | 15 kΩ |
| 6.25 V | 20 kΩ |
| 10.0 V | 35 kΩ |

### PRECISION VOLTAGE REFERENCES

2.5, 5.0, 6.25 and 10-VOLT

LASER-TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT

**G SUFFIX**
METAL PACKAGE
CASE 601



(Top View)

**ORDERING INFORMATION**

| Device | Temperature Range |
|---|---|
| **2.5 Volts** | |
| MC1500G2<br>MC1400G2 | −55°C to +125°C<br>0°C to +70°C |
| **5.0 Volts** | |
| MC1500G5<br>MC1400G5 | −55°C to +125°C<br>0°C to +70°C |
| **6.25 Volts** | |
| MC1500G6<br>MC1400G6 | −55°C to +125°C<br>0°C to +70°C |
| **10 Volts** | |
| MC1500G10<br>MC1400G10 | −55°C to +125°C<br>0°C to +70°C |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Applied Voltages | $V_{in}$<br>$V_{TRIM}$ | −0.3 to +40<br>−0.3 to +5.0 | V |
| Load Current<br>$V_{TEMP}$, Pin 3<br>Output, Pin 6 | $I_{TEMP}$<br>$I_{out}$ | ±50<br>±40 | μA<br>mA |
| Output Short Circuit Duration<br>To Ground<br>To $V_{in}$ | $t_{sc}$ | Continuous<br>10 | seconds |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature | $T_J$ | +150 | °C |
| Operating Ambient Temperature Range<br>MC1500<br>MC1400 | $T_A$ | −55 to +125<br>0 to +70 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 15 Volts, $T_A$ = 25°C and Trim Terminal not connected unless otherwise noted)

| Characteristic | Symbol | MC1400 | | | MC1500 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage | $V_O$ | | | | | | | Volts |
| ($I_O$ = 0 mA) G2 | | 2.495 | 2.500 | 2.505 | 2.495 | 2.500 | 2.505 | |
| G5 | | 4.990 | 5.000 | 5.010 | 4.990 | 5.000 | 5.010 | |
| G6 | | 6.240 | 6.250 | 6.260 | 6.240 | 6.250 | 6.260 | |
| G10 | | 9.980 | 10.000 | 10.020 | 9.980 | 10.000 | 10.020 | |
| Output Voltage Tolerance | — | — | 0.05 | 0.20 | — | 0.05 | 0.20 | % |
| Output Trim Range ($R_p$ = 100 kΩ) | $\Delta V_{TRIM}$ | ±6.0 | — | — | ±6.0 | — | — | % |
| Temperature Coefficient (Notes 1, 4)<br>($T_{min}$ to $T_{max}$) MC1400/1500 | $TCV_O$ | — | — | 40 | — | — | 40 | ppm/°C |
| Line Regulation (Note 2) | $Reg_{line}$ | | | | | | | mV |
| ($V_{in}$ = 3.5 V to 40 V) G2 | | — | 1.0 | 3.0 | — | 1.0 | 3.0 | |
| ($V_{in}$ = 6.0 V to 40 V) G5 | | — | 1.5 | 4.0 | — | 1.5 | 4.0 | |
| ($V_{in}$ = 7.5 V to 40 V) G6 | | — | 1.5 | 4.0 | — | 1.5 | 4.0 | |
| ($V_{in}$ = 11.5 V to 40 V) G10 | | — | 2.0 | 4.0 | — | 2.0 | 4.0 | |
| Load Regulation (Note 3) | $Reg_{load}$ | | | | | | | mV |
| ($-10 \leq I_L \leq +10$ mA) G2 | | — | 6.0 | 10 | — | 6.0 | 10 | |
| G5 | | — | 8.0 | 20 | — | 8.0 | 20 | |
| G6 | | — | 8.0 | 20 | — | 8.0 | 20 | |
| G10 | | — | 8.0 | 20 | — | 8.0 | 20 | |
| Quiescent Current ($I_O$ = 0 mA) | $I_I$ | — | 0.77 | 1.5 | — | 0.77 | 1.5 | mA |
| Zener Mode Regulation (Figure 1) | $V_Z$ | | | | | | | mV |
| ($1.0 \leq I_Z \leq 10$ mA) G2 | | — | 3.0 | — | — | 3.0 | — | |
| G5 | | — | 6.0 | — | — | 6.0 | — | |
| G6 | | — | 8.0 | — | — | 8.0 | — | |
| G10 | | — | 12 | — | — | 12 | — | |
| Long Term Stability | — | — | 25 | — | — | 25 | — | ppm/1000 hrs |

**NOTES:**

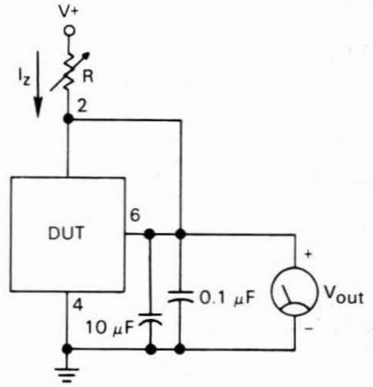
1. $T_{min}$ = −55°C for MC1500
   = 0°C for MC1400
   $T_{max}$ = +125°C for MC1500
   = +70°C for MC1400
2. Line Regulation is defined as the maximum excursion in output voltage over a given change in input voltage with zero load current and junction temperature constant.
3. Load Regulation is defined as the maximum excursion in output voltage over a given change in load current with a constant input supply voltage of +15 volts and a constant junction temperature.
4. Temperature Coefficient of the output voltage ($TCV_O$) is defined as the maximum change in output voltage over applicable temperature divided by the device operating temperature range and expressed as ppm/°C.

**DYNAMIC CHARACTERISTICS** ($V_{in}$ = 15 V, $T_A$ = 25°C all voltage ranges unless otherwise noted)

| Characteristic | Symbol | MC1400 |  |  | MC1500 |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Turn-On Settling Time (Figure 2) (to ±0.01%) | $t_S$ | — | 50 | — | — | 50 | — | μs |
| Output Noise Voltage — P to P (0.1≤f≤10 Hz) | $V_n$ |  |  |  |  |  |  | μV |
| G2 |  | — | 8.0 | — | — | 8.0 | — |  |
| G5 |  | — | 12 | — | — | 12 | — |  |
| G6 |  | — | 14 | — | — | 14 | — |  |
| G10 |  | — | 16 | — | — | 16 | — |  |
| Small-Signal Output Impedance (f = 120 Hz) | $z_o$ | — | 0.3 | — | — | 0.3 | — | Ω |
| Power Supply Rejection Ratio (f = 120 Hz) | PSRR | 60 | 87 | — | 60 | 87 | — | dB |

## TYPICAL CHARACTERISTICS

FIGURE 1 — ZENER MODE REGULATION TEST CIRCUIT



NOTE: $I_z$ is the net current flowing into the device.

FIGURE 2 — TURN-ON SETTLING TIME TEST CIRCUIT

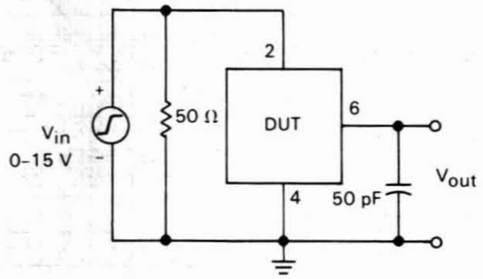


FIGURE 3 — NORMALIZED OUTPUT VOLTAGE versus TEMPERATURE

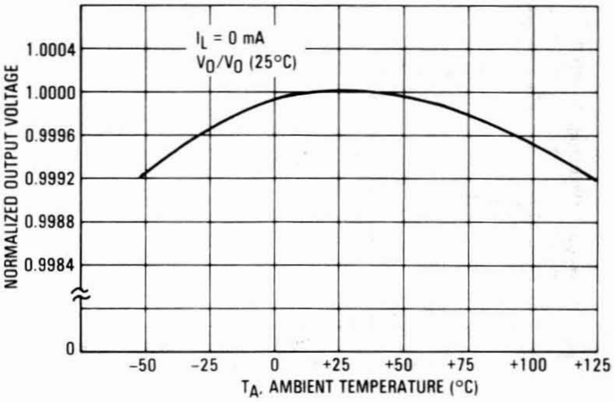


FIGURE 4 — LINE REGULATION versus TEMPERATURE

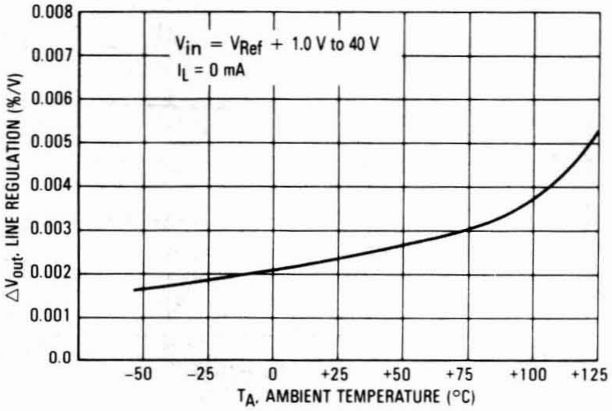


**FIGURE 5 — LOAD REGULATION versus TEMPERATURE**

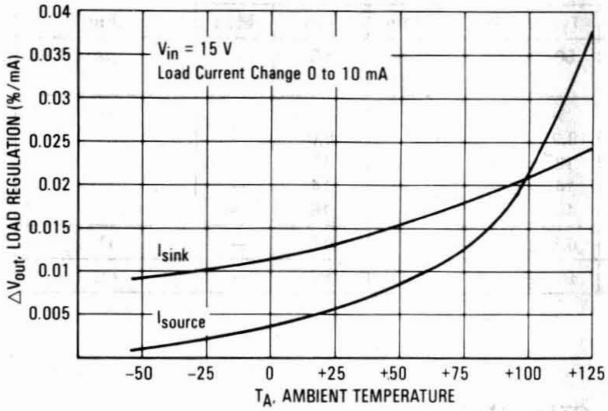


**FIGURE 6 — ZENER MODE REGULATION versus TEMPERATURE**

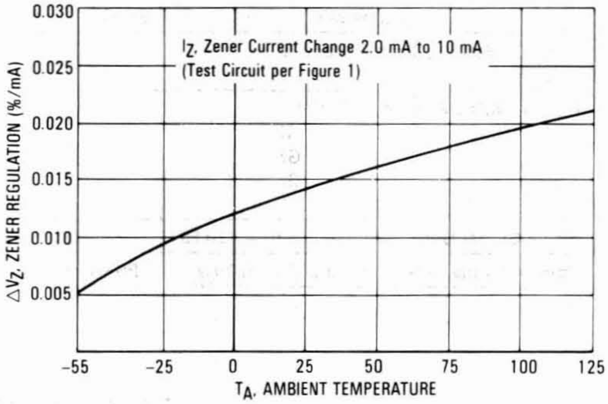


**FIGURE 7 — OUTPUT IMPEDANCE versus FREQUENCY**

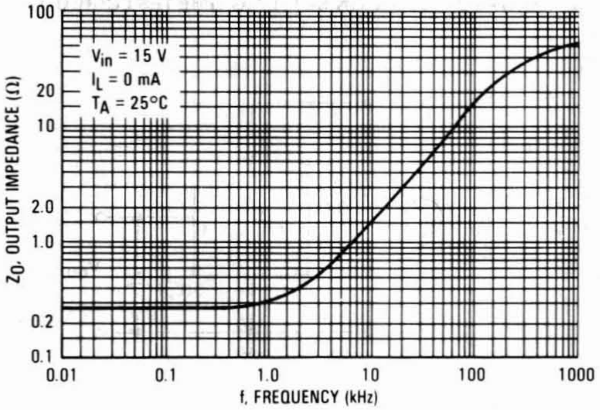


**FIGURE 8 — POWER SUPPLY REJECTION RATIO versus FREQUENCY**

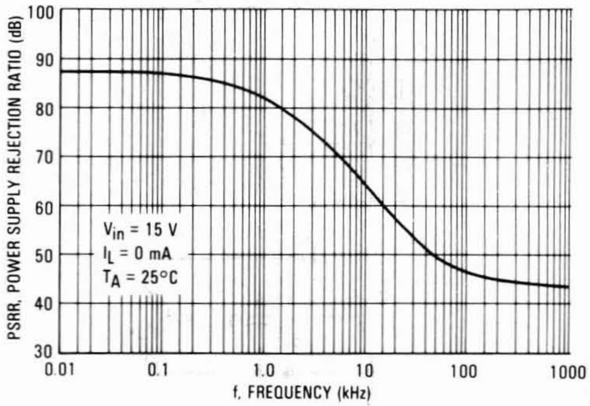


**FIGURE 9 — QUIESCENT CURRENT versus TEMPERATURE**

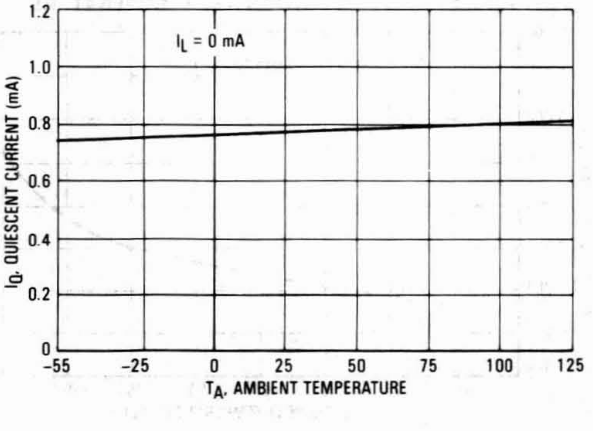
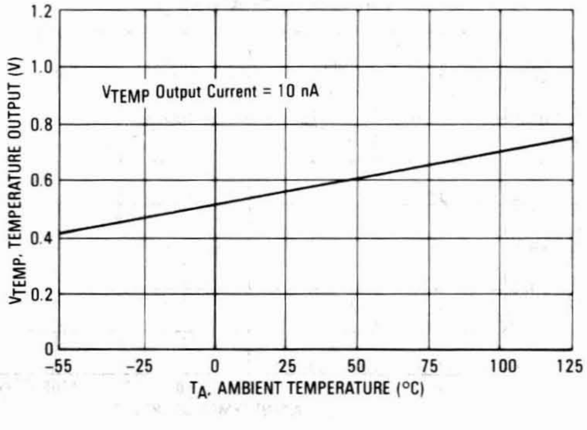
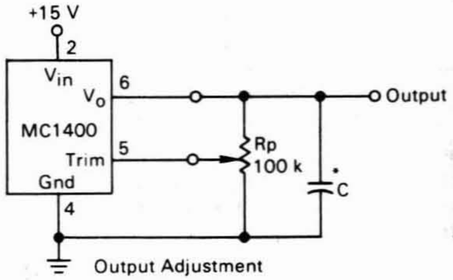


**FIGURE 10 — $V_{TEMP}$, OUTPUT versus TEMPERATURE**



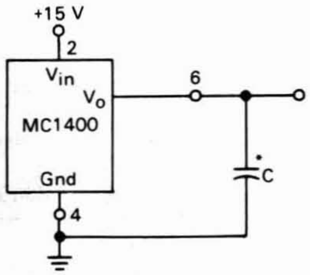
### FIGURE 11 — OUTPUT TRIM CONFIGURATION


+15 V
2
Vin
Vo
6
Output
MC1400
5
Trim
Rp
100 k
*
C
Gnd
4
Output Adjustment

The MC1400 trim terminal can be used to adjust the output voltage over a ±6% range. For example, the output can be set to 10.000 V or to 10.240 V for binary applications. For trimming, Bourns type 3059, 100 kΩ or 200 kΩ trimpot is recommended.

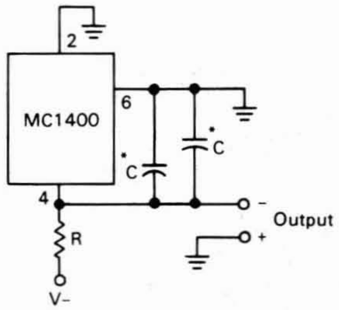
Although the circuit of Figure 11 allows a wide trim range, trimming should be kept to ⩽ ±6% in applications requiring low temperature coefficents.

### FIGURE 12 — FIXED REFERENCE

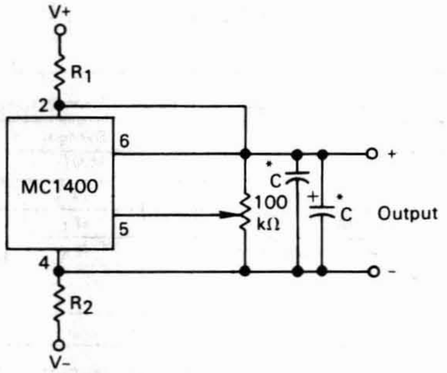

+15 V
2
Vin
Vo
6
MC1400
*
C
Gnd
4

*For better stability, transient response, and minimum noise voltage, the device should be bypassed with a 0.1 μF ceramic capacitor from Pins 6 to 4 as shown.

### FIGURE 13 — NEGATIVE REFERENCE OPERATION


2
MC1400
6
*
C
*
C
4
-
Output
+
R
V-

### FIGURE 14 — TRIMMABLE FLOATING REFERENCE OPERATION


V+
R1
2
6
+
MC1400
*
C
100
kΩ
+
*
C
Output
5
4
-
R2
V-

*For better stability, transient response, and minimum noise voltage, the device should be bypassed with a 0.1 μF ceramic and a 10 μF electrolytic capacitor from Pins 6 to 4 as shown.

**MOTOROLA**

# MC1403,A
# MC1503,A

## LOW-VOLTAGE REFERENCE

A precision band-gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with Motorola MC1506, MC1508, and MC3510 D/A converters, and MC14433 A/D systems. Low temperature drift is a prime design consideration.

- Output Voltage = 2.5 V ±25 mV
- Input Voltage Range = 4.5 V to 40 V
- Quiescent Current = 1.2 mA typ
- Output Current = 10 mA
- Temperature Coefficient = 10 ppm/°C typ
- Guaranteed Temperature Drift Specification
- Equivalent to AD580
- Standard 8-Pin DIP Package

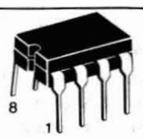
**Typical Applications**

- Voltage Reference for 8-12 Bit D/A Converters
- Low $T_C$ Zener Replacement
- High Stability Current Reference
- Voltmeter System Reference

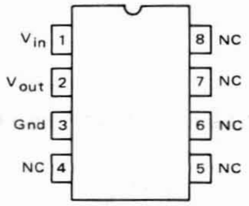
## PRECISION LOW-VOLTAGE REFERENCE

**LASER TRIMMED**
**SILICON MONOLITHIC**
**INTEGRATED CIRCUIT**

**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02



**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8



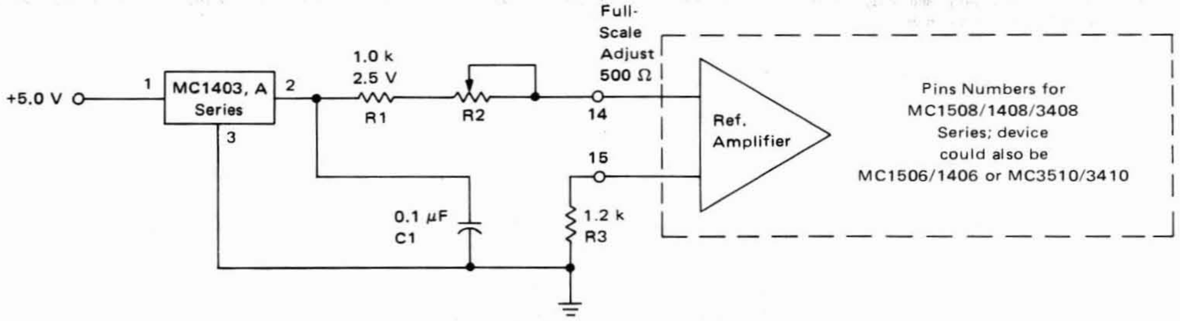
**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage | $V_I$ | 40 | V |
| Storage Temperature | $T_{stg}$ | -65 to 150 | °C |
| Junction Temperature | $T_J$ | +175 | °C |
| Operating Ambient Temeprature Range | $T_A$ | | |
| MC1503,A | | -55 to +125 | °C |
| MC1403,A | | 0 to +70 | °C |

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1503U | −55 to +125°C | Ceramic DIP |
| MC1503AU | | Ceramic DIP |
| MC1403D | 0 to +70°C | SO-8 |
| MC1403U | | Ceramic DIP |
| MC1403AU | | Ceramic DIP |

**FIGURE 1 — A REFERENCE FOR MOTOROLA MONOLITHIC D/A CONVERTERS**



### PROVIDING THE REFERENCE CURRENT FOR MOTOROLA MONOLITHIC D/A CONVERTERS

The MC1403/1503 makes an ideal reference for the Motorola monolithic D/A converters. The MC1406/1506, MC1408/1508, MC3410/3510 and MC3408 D/A converters all require a stable current reference of nominally 2.0 mA. This can be easily obtained from the MC1403/1503 with the addition of a series resistor, R1. A variable resistor, R2, is recommended to provide means for full-scale adjust on the D/A converter.

The resistor R3 improves temperature performance by matching the impedance on both inputs of the D/A reference amplifier. The capacitor decouples any noise present on the reference line. It is essential if the D/A converter is located any appreciable distance from the reference.

A single MC1403/1503 reference can provide the required current input for up to five of the monolithic D/A converters.

**ELECTRICAL CHARACTERISTICS** ($V_I$ = 15 V, $T_A$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage<br>($I_O$ = 0 mA) | $V_O$ | 2.475 | 2.50 | 2.525 | V |
| Temperature Coefficient of Output Voltage | $\Delta V_O/\Delta T$ | | | | ppm/°C |
| MC1503 | | – | – | 55 | |
| MC1503A | | – | – | 25 | |
| MC1403 | | – | 10 | 40 | |
| MC1403A | | – | 10 | 25 | |
| Output Voltage Change<br>(over specified temperature range) | $\Delta V_O$ | | | | mV |
| MC1503 } -55°C to +125°C | | – | – | 25 | |
| MC1503A } -55°C to +125°C | | – | – | 11 | |
| MC1403 } 0°C to +70°C | | – | – | 7.0 | |
| MC1403A } 0°C to +70°C | | – | – | 4.4 | |
| Line Regulation ($I_O$ = 0 mA) | $Reg_{line}$ | | | | mV |
| (15 V ≤ $V_I$ ≤ 40 V) | | – | 1.2 | 4.5 | |
| (4.5 V ≤ $V_I$ ≤ 15 V) | | – | 0.6 | 3.0 | |
| Load Regulation<br>(0 mA < $I_O$ < 10 mA) | $Reg_{load}$ | – | – | 10 | mV |
| Quiescent Current<br>($I_O$ = 0 mA) | $I_I$ | – | 1.2 | 1.5 | mA |

FIGURE 2 – MC1403/1503 SCHEMATIC

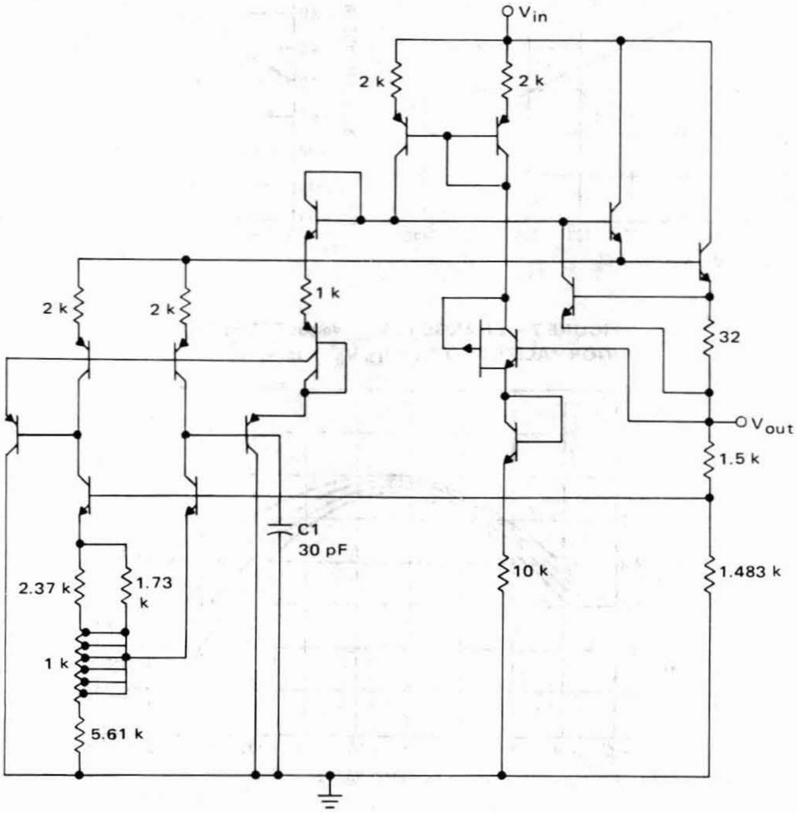


**FIGURE 3 – TYPICAL CHANGE IN $V_{out}$ versus $V_{in}$ (NORMALIZED TO $V_{in}$ = 15 V @ $T_C$ = 25°C)**

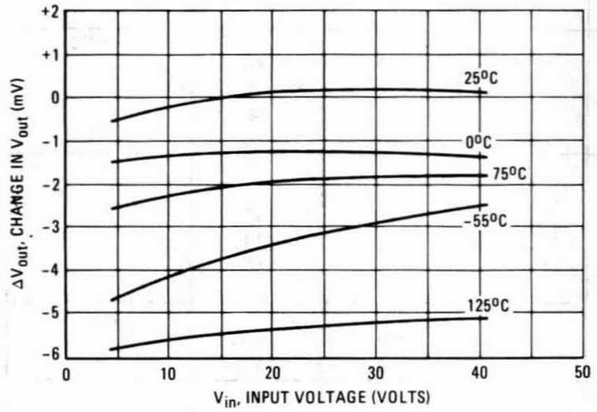


**FIGURE 4 – CHANGE IN OUTPUT VOLTAGE versus LOAD CURRENT (NORMALIZED TO $V_{out}$ @ $V_{in}$ = 15 V, $I_{out}$ = 0 mA)**

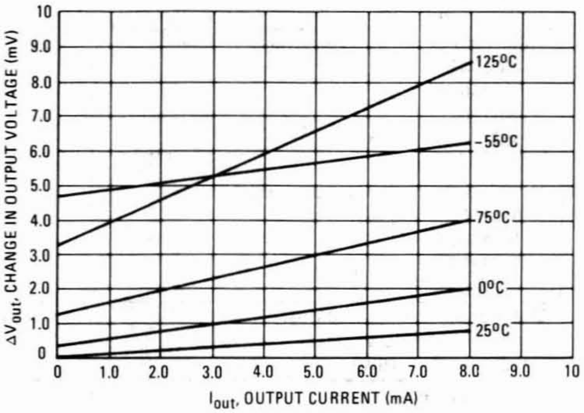


**FIGURE 5 – QUIESCENT CURRENT versus TEMPERATURE ($V_{in}$ = 15 V, $I_{out}$ = 0 mA)**

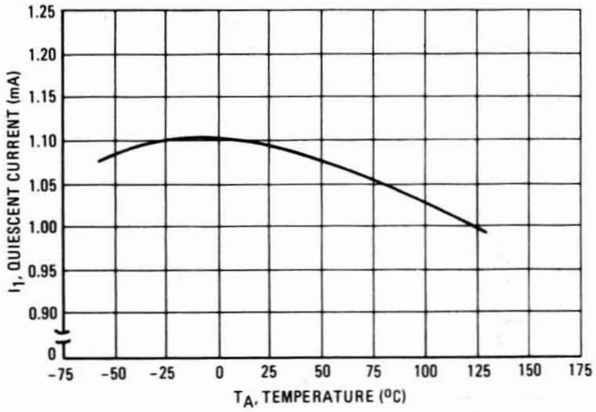


**FIGURE 6 – CHANGE IN $V_{out}$ versus TEMPERATURE (NORMALIZED TO $V_{out}$ @ $V_{in}$ = 15 V)**

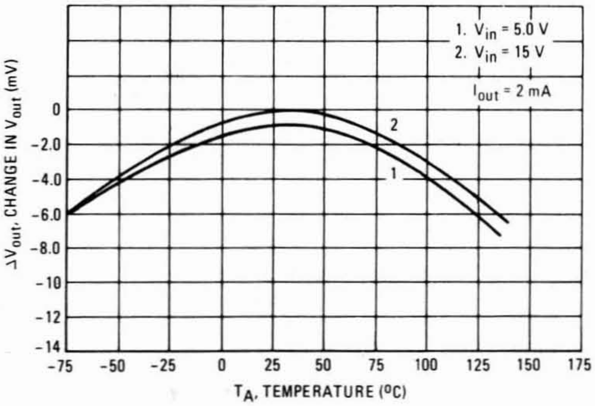
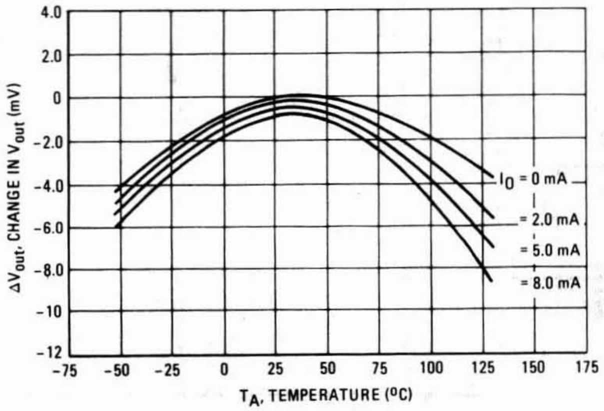


**FIGURE 7 – CHANGE IN $V_{out}$ versus TEMPERATURE (NORMALIZED TO $T_A$ = $I_O$, $V_{in}$ = 15 V, $I_{out}$ = 0 mA)**



## 3-1/2-DIGIT VOLTMETER – COMMON ANODE DISPLAYS, FLASHING OVERRANGE

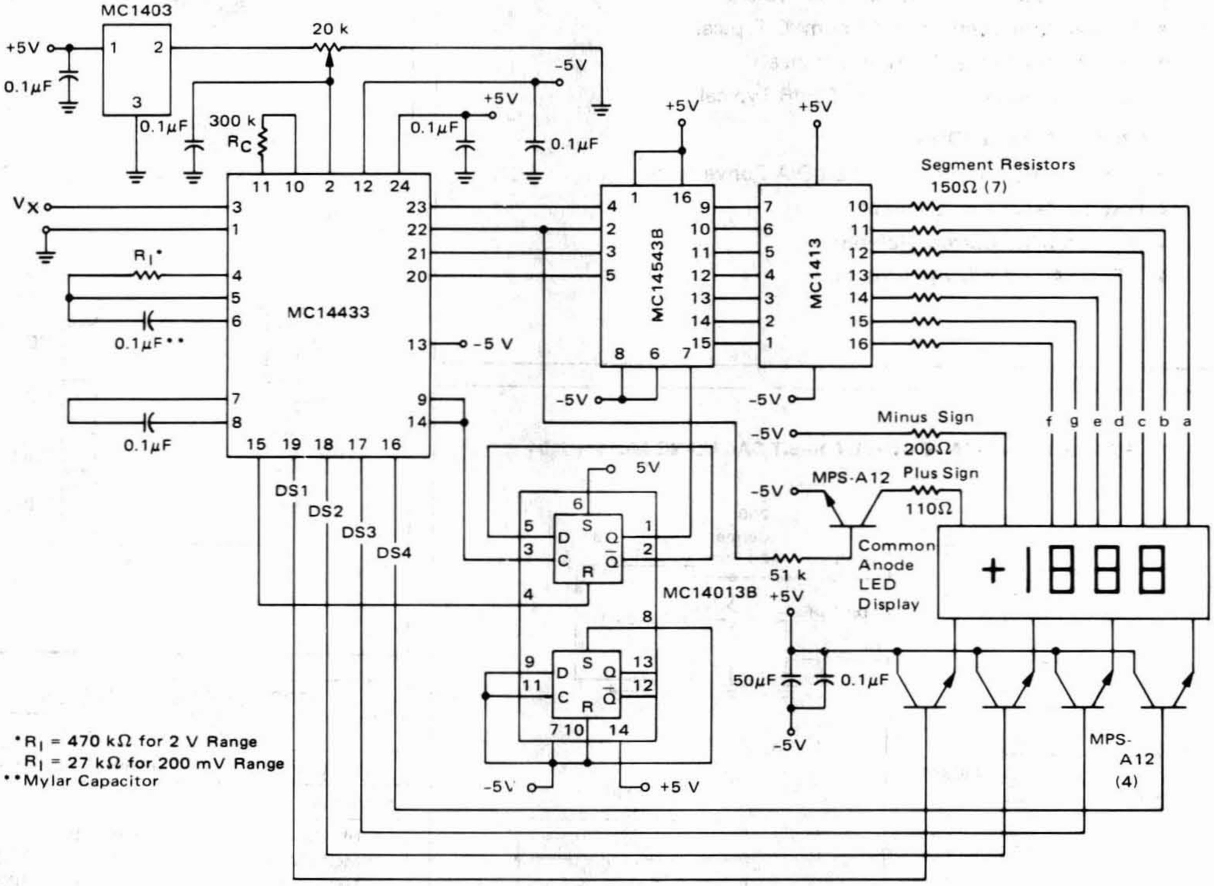
An example of a 3-1/2-digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 8. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, $R_I$ is also changed, as shown on the diagram.

When using $R_C$ equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with 1/2 MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter-follower configuration. The MC14543B, MC14013B and LED displays are referenced to $V_{EE}$ via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in Figure 8.

FIGURE 8 – 3-1/2-DIGIT VOLTMETER


MC1403
+5V
0.1µF
1
2
3
20 k
-5V
+5V
0.1µF
300 k
RC
0.1µF
0.1µF
+5V
+5V
Segment Resistors
150Ω (7)
VX
RI*
0.1µF**
0.1µF
MC14433
11 10 2 12 24
3
1
4
5
6
7
8
23
22
21
20
13
9
14
-5 V
15 19 18 17 16
DS1
DS2
DS3
DS4
MC14543B
MC1413
-5V
-5V
Minus Sign
200Ω
MPS-A12
Plus Sign
110Ω
51 k
Common Anode LED Display
+1888
f g e d c b a
5V
MC14013B
D S Q
C R Q̄
+5V
50µF
0.1µF
-5V
MPS-A12 (4)
-5V
+5 V

*$R_I$ = 470 kΩ for 2 V Range
$R_I$ = 27 kΩ for 200 mV Range
**Mylar Capacitor

**MOTOROLA**

# MC1404
# MC1404A
# MC1504

## VOLTAGE REFERENCE FAMILY

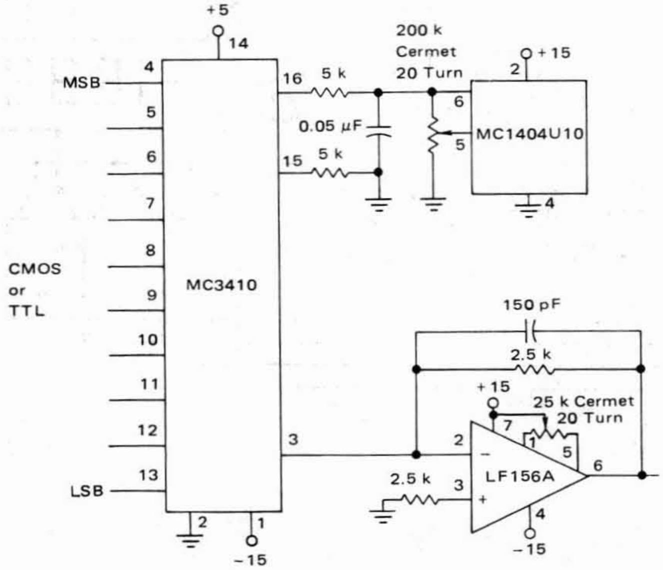
The MC1404 series of ICs is a family of temperature-compensated voltage references for precision data conversion applications, such as A/D, D/A, V/F, and F/V. Advances in laser-trimming and ion-implanted devices, as well as monolithic fabrication techniques, make these devices stable and accurate to 12 bits over both military and commercial temperature ranges. In addition to excellent temperature stability, these parts offer excellent long-term stability and low noise.

- Output Voltages: Standard, 5.0 V, 6.25 V, 10 V
- Trimmable Output: > ±6%
- Wide Input Voltage Range: $V_{ref}$ + 2.5 V to 40 V
- Low Quiescent Current: 1.25 mA Typical
- Temperature Coefficient: 10 ppm/°C Typical
- Low Output Noise: 12 μV p-p Typical
- Excellent Ripple Rejection: > 80 dB Typical

### TYPICAL APPLICATIONS

- Voltage Reference for 8 – 12 Bit D/A Converters
- Low $T_C$ Zener Replacement
- High Stability Current Reference
- MPU D/A and A/D Applications

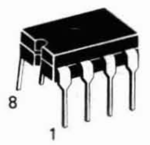
**FIGURE 1 — VOLTAGE OUTPUT 10-BIT DAC USING MC1404U10**


+5
14
MSB
4
5
6
7
8
9
10
11
12
13
LSB
CMOS
or
TTL
MC3410
2
1
−15
16
5 k
0.05 μF
15
5 k
200 k
Cermet
20 Turn
+15
2
6
5
MC1404U10
4
3
150 pF
2.5 k
+15
7
25 k Cermet
20 Turn
1
5
2
−
LF156A
+
3
2.5 k
6
4
−15

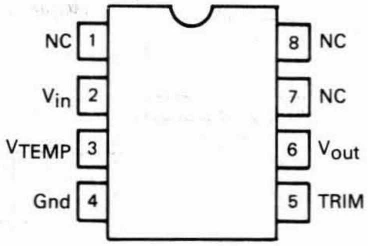
## PRECISION LOW-DRIFT VOLTAGE REFERENCES

5.0, 6.25, and 10-VOLT OUTPUT VOLTAGES

LASER TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT



**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02


NC 1
Vin 2
VTEMP 3
Gnd 4
8 NC
7 NC
6 Vout
5 TRIM

### ORDERING INFORMATION

**PACKAGE Ceramic DIP**

| Device | Temperature Range |
|---|---|
| **5.0 Volts** | |
| MC1504U5 | −55°C to +125°C |
| MC1404U5 | 0°C to +70°C |
| MC1404AU5 | 0°C to +70°C |
| **6.25 Volts** | |
| MC1504U6 | −55°C to +125°C |
| MC1404U6 | 0°C to +70°C |
| MC1404AU6 | 0°C to +70°C |
| **10 Volts** | |
| MC1504U10 | −55°C to +125°C |
| MC1404U10 | 0°C to +70°C |
| MC1404AU10 | 0°C to +70°C |

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage | $V_I$ | 40 | V |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature | $T_J$ | +175 | °C |
| Operating Ambient Temperature Range | $T_A$ | | |
| MC1504 | | −55 to +125 | °C |
| MC1404,A | | 0 to +70 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = 15 Volts, $T_A$ = 25°C and Trim Terminal not connected unless otherwise noted)

| Characteristic | Symbol | MC1404,A | | | MC1504 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage ($I_o$ = 0 mA) | $V_o$ | | | | | | | Volt |
| U5, AU5 | | 4.95 | 5.00 | 5.05 | 4.95 | 5.00 | 5.05 | |
| U6, AU6 | | 6.19 | 6.25 | 6.31 | 6.19 | 6.25 | 6.31 | |
| U10, AU10 | | 9.90 | 10 | 10.10 | 9.90 | 10 | 10.10 | |
| Output Voltage Tolerance | — | — | ±0.1 | ±1.0 | — | ±0.1 | ±1.0 | % |
| Output Trim Range (Figure 10) ($R_P$ = 100 kΩ) | $\Delta V_{TRIM}$ | ±6.0 | — | — | ±6.0 | — | — | % |
| Output Voltage Temperature Coefficient, Over Full Temperature Range | $\Delta V_o/\Delta T$ | | | | | | | ppm/°C |
| MC1404, MC1504 | | — | 10 | 40 | — | — | 55 | |
| MC1404A | | — | 10 | 25 | — | — | — | |
| Maximum Output Voltage Change Over Temperature Range | $\Delta V_o$ | | | | | | | mV |
| MC1404U5, MC1504U5 | | — | — | 14 | — | — | 50 | |
| MC1404AU5 | | — | — | 9.0 | — | — | — | |
| MC1404U6, MC1504U6 | | — | — | 17.5 | — | — | 62 | |
| MC1404AU6 | | — | — | 11 | — | — | — | |
| MC1404U10, MC1504U10 | | — | — | 28 | — | — | 99 | |
| MC1404AU10 | | — | — | 18 | — | — | — | |
| Line Regulation (1) ($V_{in}$ = $V_{out}$ + 2.5 V to 40 V, $I_{out}$ = 0 mA) | $Reg_{line}$ | — | 2.0 | 6.0 | — | 2.0 | 6.0 | mV |
| Load Regulation (1) ($0 \leqslant I_o \leqslant 10$ mA) | $Reg_{load}$ | — | — | 10 | — | — | 10 | mV |
| Quiescent Current ($I_o$ = 0 mA) | $I_I$ | — | 1.2 | 1.5 | — | 1.2 | 1.5 | mA |
| Short Circuit Current | $I_{sc}$ | — | 20 | 30 | — | — | 30 | mA |
| Long Term Stability | — | — | 25 | — | — | 25 | — | ppm/1000 hrs |

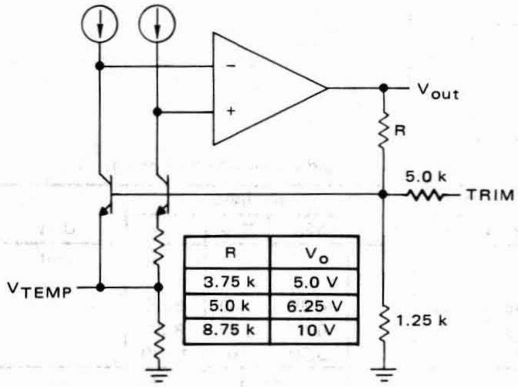
Note 1: Includes thermal effects.

**DYNAMIC CHARACTERISTICS** ($V_{in}$ = 15 V, $T_A$ = 25°C all voltage ranges unless otherwise noted)

| Characteristic | Symbol | MC1404,A | | | MC1504 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Turn-On Settling Time (to ±0.01%) | $t_S$ | — | 50 | — | — | 50 | — | μs |
| Output Noise Voltage — P to P (Bandwidth 0.1 to 10 Hz) | $V_n$ | — | 12 | — | — | 12 | — | μV |
| Small-Signal Output Impedance | $r_o$ | | | | | | | Ω |
| 120 Hz | | — | 0.15 | — | — | 0.15 | — | |
| 500 Hz | | — | 0.2 | — | — | 0.2 | — | |
| Power Supply Rejection Ratio | PSRR | 70 | 80 | — | 70 | 80 | — | dB |

## TYPICAL CHARACTERISTICS

FIGURE 2 – SIMPLIFIED DEVICE DIAGRAM



| R | Vo |
|---|---|
| 3.75 k | 5.0 V |
| 5.0 k | 6.25 V |
| 8.75 k | 10 V |

FIGURE 3 – LINE REGULATION versus TEMPERATURE

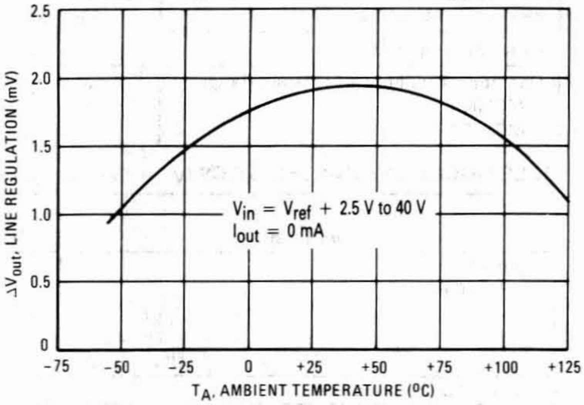


FIGURE 4 – OUTPUT VOLTAGE versus TEMPERATURE MC1404U10

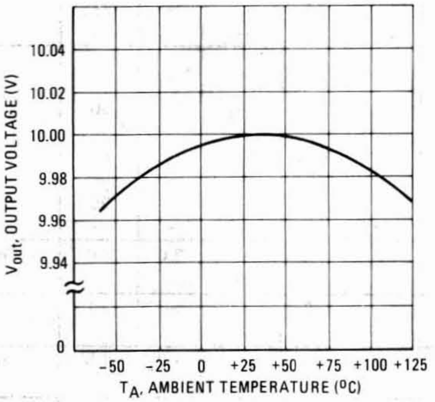


FIGURE 5 – LOAD REGULATION versus TEMPERATURE

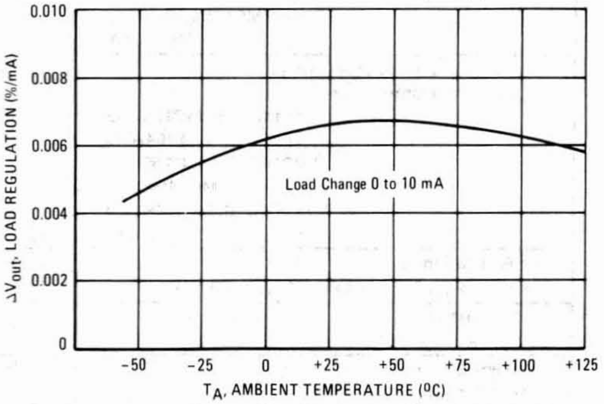


FIGURE 6 – POWER SUPPLY REJECTION RATIO versus FREQUENCY

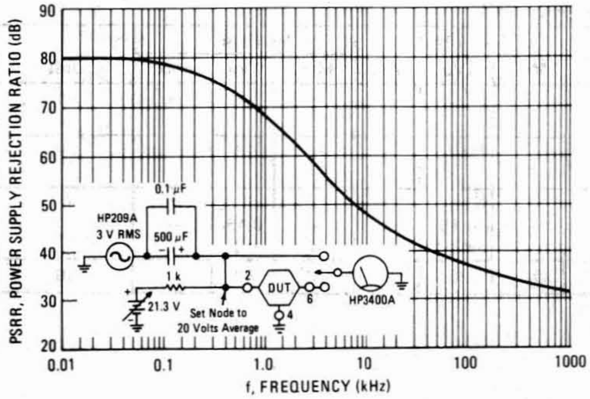


FIGURE 7 – QUIESCENT CURRENT versus TEMPERATURE

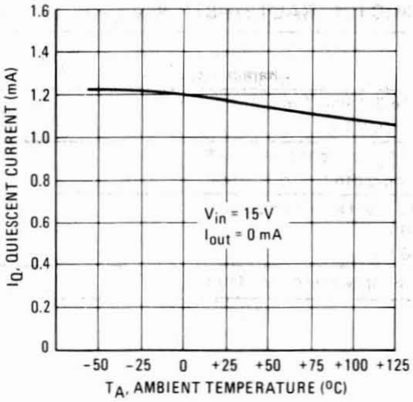


FIGURE 8 – SHORT CIRCUIT CURRENT versus TEMPERATURE

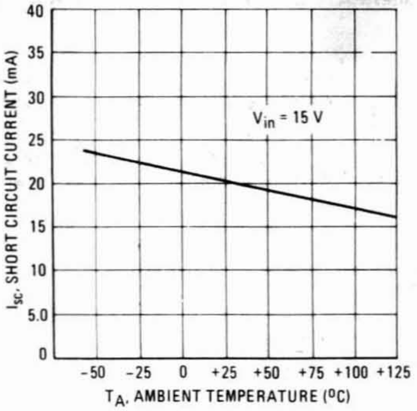


FIGURE 9 – $V_{TEMP}$ OUTPUT versus TEMPERATURE

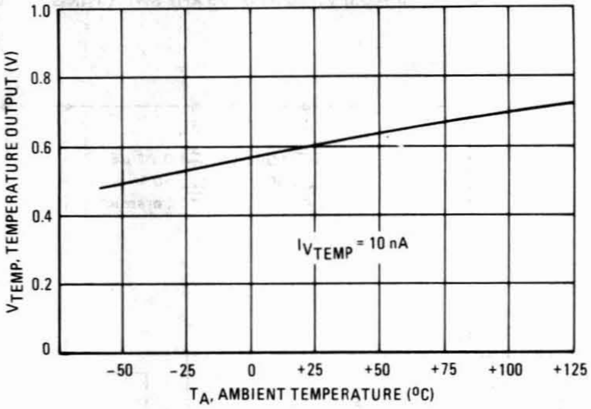
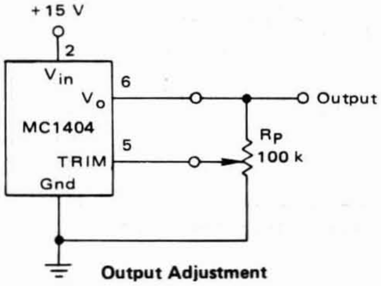


FIGURE 10 – OUTPUT TRIM CONFIGURATION

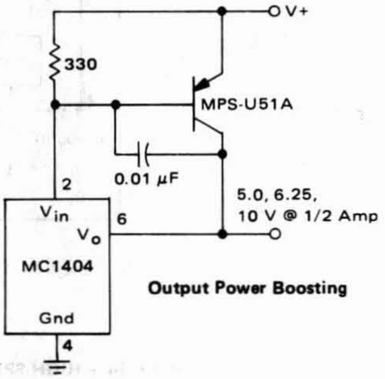

+15 V
2
$V_{in}$
6
$V_o$
Output
MC1404
5
$R_P$
100 k
TRIM
Gnd

**Output Adjustment**

The MC1404 trim terminal can be used to adjust the output voltage over a ±6% range. For example, the output can be set to 10.000 V or 10.240 V for binary applications. For trimming, Bourns type 3059, 100 kΩ or 200 kΩ trimpot is recommended.

Although Figure 10 illustrates a wide trim range, temperature coefficients may become unpredictable for trim > ±6.0%.

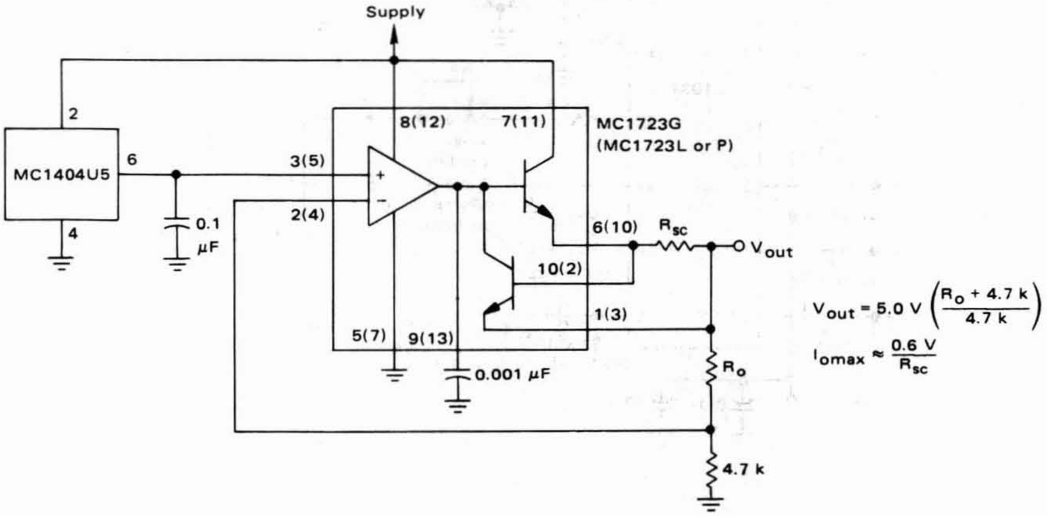
FIGURE 11 – PRECISION SUPPLY USING MC1404


V+
330
MPS-U51A
0.01 μF
2
$V_{in}$
6
$V_o$
5.0, 6.25,
10 V @ 1/2 Amp
MC1404
Gnd
4

**Output Power Boosting**

The addition of a power transistor, a resistor, and a capacitor converts the MC1404 into a precision supply with one ampere current capability. At V+ = 15 V, the MC1404 can carry in excess of 14 mA of load current with good regulation. If the power transistor current gain exceeds 75, a one ampere supply can be realized.

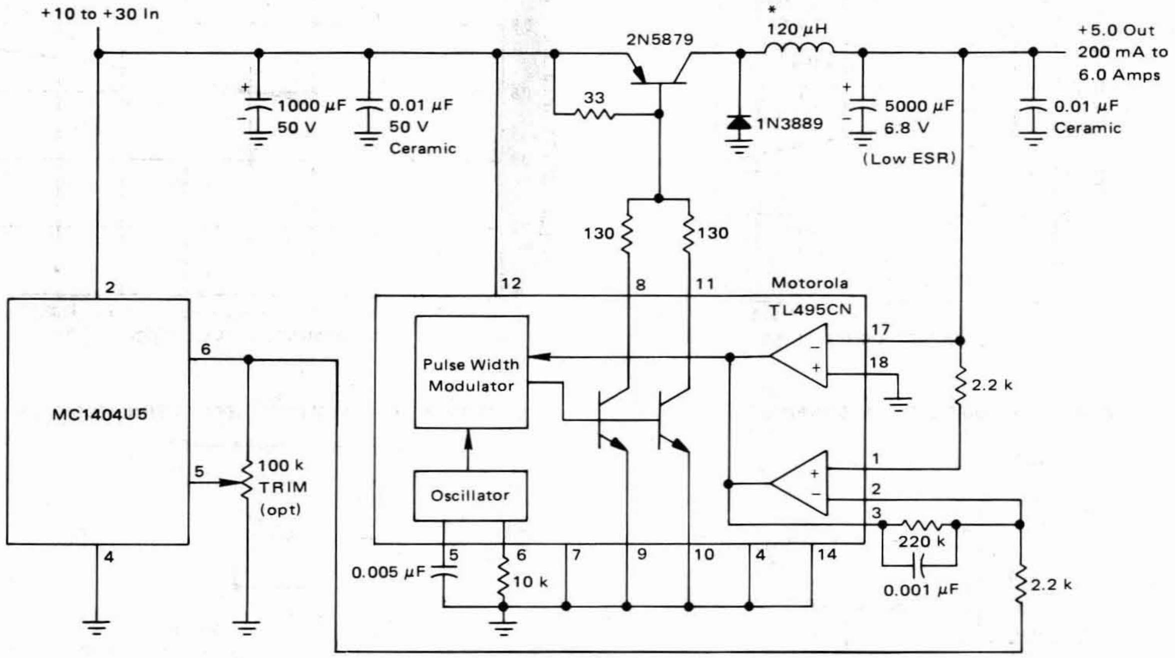
FIGURE 12 – ULTRA STABLE REFERENCE FOR MC1723 VOLTAGE REGULATOR


Supply
2
MC1404U5
6
4
0.1
μF
3(5)
2(4)
8(12)
7(11)
MC1723G
(MC1723L or P)
6(10)
$R_{sc}$
$V_{out}$
10(2)
1(3)
5(7)
9(13)
0.001 μF
$R_o$
4.7 k

$$V_{out} = 5.0\ \text{V}\left(\frac{R_o + 4.7\ \text{k}}{4.7\ \text{k}}\right)$$

$$I_{omax} \approx \frac{0.6\ \text{V}}{R_{sc}}$$

FIGURE 13 – 5.0 V, 6.0 AMP, 25 kHz SWITCHING REGULATOR WITH SEPARATE ULTRA-STABLE REFERENCE

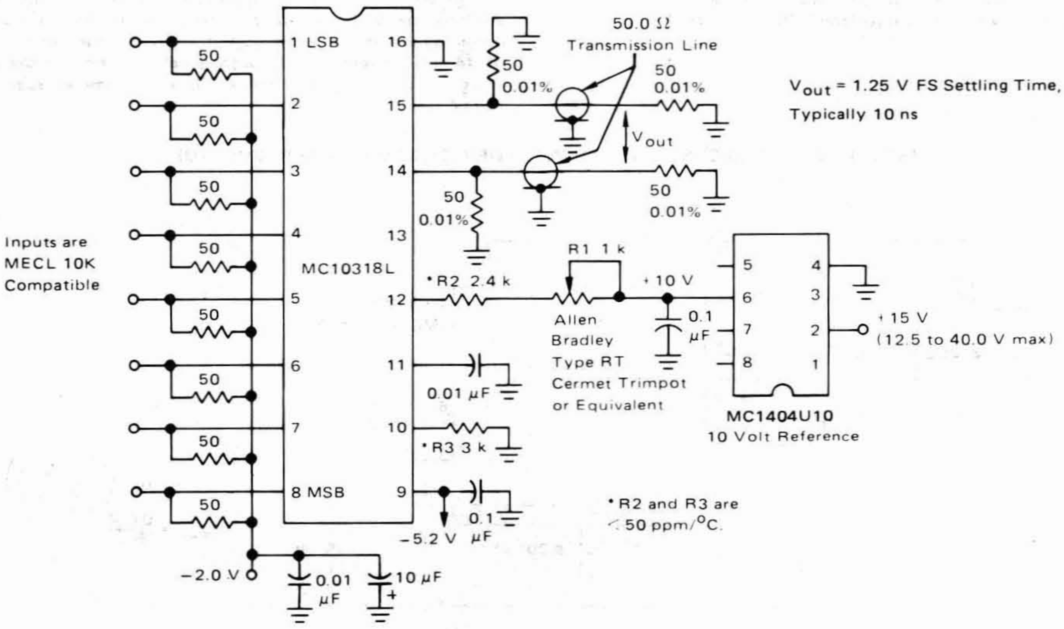

+10 to +30 In
1000 μF
50 V
0.01 μF
50 V
Ceramic
2N5879
33
*
120 μH
1N3889
5000 μF
6.8 V
(Low ESR)
+5.0 Out
200 mA to
6.0 Amps
0.01 μF
Ceramic
130
130
12
8
11
Motorola
TL495CN
17
18
2.2 k
Pulse Width
Modulator
Oscillator
1
2
3
220 k
0.001 μF
2.2 k
MC1404U5
2
6
5
4
100 k
TRIM
(opt)
0.005 μF
5
6
10 k
7
9
10
4
14

*40 Turns #16 Wire, CARBONYL E OR J

4

FIGURE 14 – HIGH SPEED 8-BIT D/A CONVERTER USING MC1404U10

$I_{FS}$ is set to 51.000 mA with R1


Inputs are
MECL 10K
Compatible
50
1 LSB
2
3
4
5
6
7
8 MSB
16
15
14
13
12
11
10
9
MC10318L
−2.0 V
0.01 μF
10 μF
50
0.01%
50.0 Ω
Transmission Line
50
0.01%
V_out
50
0.01%
50
0.01%
*R2 2.4 k
R1 1 k
Allen
Bradley
Type RT
Cermet Trimpot
or Equivalent
+10 V
0.1 μF
0.01 μF
*R3 3 k
0.1 μF
−5.2 V
5
6
7
8
4
3
2
1
+15 V
(12.5 to 40.0 V max)
MC1404U10
10 Volt Reference

$V_{out}$ = 1.25 V FS Settling Time, Typically 10 ns

*R2 and R3 are
< 50 ppm/°C.

**MOTOROLA**

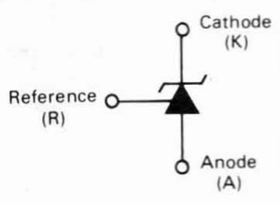
# TL431,A Series

## Specifications and Applications Information

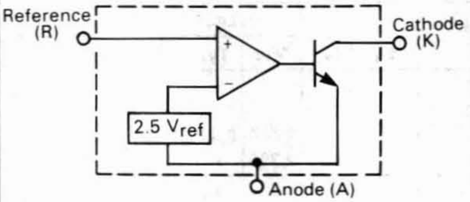
### PROGRAMMABLE PRECISION REFERENCES

The TL431,A integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from $V_{ref}$ to 36 volts with two external resistors. These devices exhibit a wide operating current range of 1.0 to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 volt reference makes it convenient to obtain a stable reference from 5.0 volt logic supplies, and since the TL431,A operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

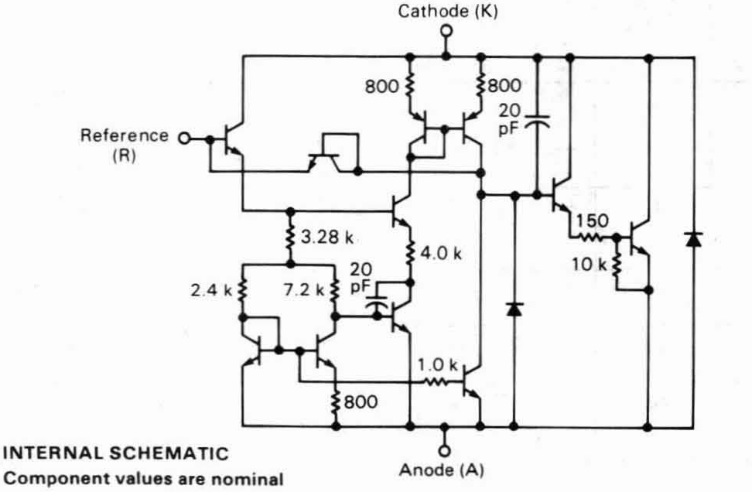
- Programmable Output Voltage to 36 Volts
- Voltage Reference Tolerance: ±1.0% (TL431,A)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage



SYMBOL



FUNCTIONAL BLOCK DIAGRAM



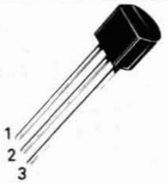
INTERNAL SCHEMATIC
Component values are nominal

### PROGRAMMABLE PRECISION REFERENCES

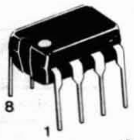
SILICON MONOLITHIC
INTEGRATED CIRCUITS

**LP SUFFIX**
CASE 29-02
TO-226AA
(TO-92)

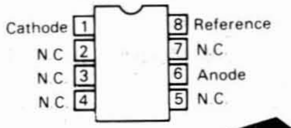
Pin 1. Reference
2. Anode
3. Cathode

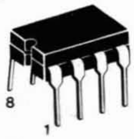


**P SUFFIX**
PLASTIC DUAL-IN-LINE PACKAGE
CASE 626



(Top View)





**JG SUFFIX**
CERAMIC DUAL-IN-LINE PACKAGE
CASE 693

**D SUFFIX***
PLASTIC PACKAGE
CASE 751-01
SO-8

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

***Surface Mount pin-out is different than standard package pin-out for this device. Please refer to Chapter 7 for details.**

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| TL431CLP,ACLP | 0 to +70°C | Plastic TO-92 |
| TL431CP,ACP | 0 to +70°C | Plastic DIP |
| TL431CD,ACD | 0 to +70°C | SOP-8 |
| TL431CJG | 0 to +70°C | Ceramic DIP |
| TL431ILP,AILP | −40 to +85°C | Plastic TO-92 |
| TL431IP,AIP | −40 to +85°C | Plastic DIP |
| TL431IJG | −40 to +85°C | Ceramic DIP |
| TL431MJG | −55 to +125°C | Ceramic DIP |

**MAXIMUM RATINGS** (Full operating ambient temperature range applies unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Cathode To Anode Voltage | $V_{KA}$ | 37 | V |
| Cathode Current Range, Continuous | $I_K$ | −100 to +150 | mA |
| Reference Input Current Range, Continuous | $I_{ref}$ | −0.05 to +10 | mA |
| Operating Junction Temperature | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | | °C |
| TL431M | | −55 to +125 | |
| TL431I, TL431AI | | −40 to +85 | |
| TL431C, TL431AC | | 0 to +70 | |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C Ambient Temperature | $P_D$ | | W |
| D, LP Suffix Plastic Package | | 0.70 | |
| P Suffix Plastic Package | | 1.10 | |
| JG Suffix Ceramic Package | | 1.25 | |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C Case Temperature | $P_D$ | | W |
| D, LP Suffix Plastic Package | | 1.5 | |
| P Suffix Plastic Package | | 3.0 | |
| JG Suffix Ceramic Package | | 3.3 | |

**THERMAL CHARACTERISTICS**

| Characteristics | Symbol | D, LP Suffix Package | P Suffix Package | JG Suffix package | Unit |
|---|---|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 178 | 114 | 100 | °C/W |
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 83 | 41 | 38 | °C/W |

**RECOMMENDED OPERATING CONDITIONS**

| Condition/Value | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Cathode To Anode Voltage | $V_{KA}$ | $V_{ref}$ | 36 | V |
| Cathode Current | $I_K$ | 1.0 | 100 | mA |

**ELECTRICAL CHARACTERISTICS** (Ambient temperature at 25°C unless otherwise noted)

| Characteristic | Symbol | TL431M | | | TL431I | | | TL431C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reference Input Voltage (Figure 1)<br>$V_{KA} = V_{ref}$, $I_K$ = 10 mA | $V_{ref}$ | | | | | | | | | | V |
| $T_A$ = +25°C | | 2.440 | 2.495 | 2.550 | 2.440 | 2.495 | 2.550 | 2.440 | 2.495 | 2.550 | |
| $T_A = T_{low}$ to $T_{high}$ (Note 1) | | 2.396 | — | 2.594 | 2.410 | — | 2.580 | 2.423 | — | 2.567 | |
| Reference Input Voltage Deviation Over Temperature Range (Figure 1, Note 1, 2, 4)<br>$V_{KA} = V_{ref}$, $I_K$ = 10 mA | $\Delta V_{ref}$ | — | 15 | 44 | — | 7.0 | 30 | — | 3.0 | 17 | mV |
| Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage | $\frac{\Delta V_{ref}}{\Delta V_{KA}}$ | | | | | | | | | | mV/V |
| $I_K$ = 10 mA (Figure 2), $\Delta V_{KA}$ = 10 V to $V_{ref}$ | | — | −1.4 | −2.7 | — | −1.4 | −2.7 | — | −1.4 | −2.7 | |
| $\Delta V_{KA}$ = 36 V to 10 V | | — | −1.0 | −2.0 | — | −1.0 | −2.0 | — | −1.0 | −2.0 | |
| Reference Input Current (Figure 2)<br>$I_K$ = 10 mA, R1 = 10 k, R2 = ∞ | $I_{ref}$ | | | | | | | | | | μA |
| $T_A$ = +25°C | | — | 1.8 | 4.0 | — | 1.8 | 4.0 | — | 1.8 | 4.0 | |
| $T_A = T_{low}$ to $T_{high}$ (Note 1) | | — | — | 7.0 | — | — | 6.5 | — | — | 5.2 | |
| Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4)<br>$I_K$ = 10 mA, R1 = 10 k, R2 = ∞ | $\Delta I_{ref}$ | — | 1.0 | 3.0 | — | 0.8 | 2.5 | — | 0.4 | 1.2 | μA |
| Minimum Cathode Current For Regulation<br>$V_{KA} = V_{ref}$ (Figure 1) | $I_{min}$ | — | 0.5 | 1.0 | — | 0.5 | 1.0 | — | 0.5 | 1.0 | mA |
| Off-State Cathode Current (Figure 3)<br>$V_{KA}$ = 36 V, $V_{ref}$ = 0 V | $I_{off}$ | — | 2.6 | 1000 | — | 2.6 | 1000 | — | 2.6 | 1000 | nA |
| Dynamic Impedance (Figure 1, Note 3)<br>$V_{KA} = V_{ref}$, $\Delta I_K$ = 1.0 mA to 100 mA<br>f ≤ 1.0 kHz | $\lvert Z_{ka} \rvert$ | — | 0.22 | 0.5 | — | 0.22 | 0.5 | — | 0.22 | 0.5 | Ω |

**ELECTRICAL CHARACTERISTICS** (Ambient temperature at 25°C unless otherwise noted)

| Characteristic | Symbol | TL431AI |  |  | TL431AC |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Reference Input Voltage (Figure 1)<br>$V_{KA} = V_{ref}, I_K = 10$ mA | $V_{ref}$ |  |  |  |  |  |  | V |
| $T_A = +25°C$ |  | 2.470 | 2.495 | 2.520 | 2.470 | 2.495 | 2.520 |  |
| $T_A = T_{low}$ to $T_{high}$ (Note 4) |  | 2.440 | — | 2.550 | 2.453 | — | 2.537 |  |
| Reference Input Voltage Deviation Over Temperature Range (Figure 1, Note 1, 2)<br>$V_{KA} = V_{ref}, I_K = 10$ mA | $\Delta V_{ref}$ | — | 7.0 | 30 | — | 3.0 | 17 | mV |
| Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage | $\frac{\Delta V_{ref}}{\Delta V_{KA}}$ |  |  |  |  |  |  | mV/V |
| $I_K = 10$ mA (Figure 2), $\Delta V_{KA} = 10$ V to $V_{ref}$ |  | — | −1.4 | −2.7 | — | −1.4 | −2.7 |  |
| $\Delta V_{KA} = 36$ V to 10 V |  | — | −1.0 | −2.0 | — | −1.0 | −2.0 |  |
| Reference Input Current (Figure 2)<br>$I_K = 10$ mA, R1 = 10 k, R2 = ∞ | $I_{ref}$ |  |  |  |  |  |  | μA |
| $T_A = +25°C$ |  | — | 1.8 | 4.0 | — | 1.8 | 4.0 |  |
| $T_A = T_{low}$ to $T_{high}$ (Note 1) |  | — | — | 6.5 | — | — | 5.2 |  |
| Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1)<br>$I_K = 10$ mA, R1 = 10 k, R2 = ∞ | $\Delta I_{ref}$ | — | 0.8 | 2.5 | — | 0.4 | 1.2 | μA |
| Minimum Cathode Current For Regulation<br>$V_{KA} = V_{ref}$ (Figure 1) | $I_{min}$ | — | 0.5 | 1.0 | — | 0.5 | 1.0 | mA |
| Off-State Cathode Current (Figure 3)<br>$V_{KA} = 36$ V, $V_{ref} = 0$ V | $I_{off}$ | — | 2.6 | 1000 | — | 2.6 | 1000 | nA |
| Dynamic Impedance (Figure 1, Note 3)<br>$V_{KA} = V_{ref}, \Delta I_K = 1.0$ mA to 100 mA<br>f ≤ 1.0 kHz | $\|Z_{ka}\|$ | — | 0.22 | 0.5 | — | 0.22 | 0.5 | Ω |

Note 1:

$T_{low}$ = −55°C for TL431MJG
= −40°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431IJG
= 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

$T_{high}$ = +125°C for TL431MJG
= +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431IJG
= +70°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

FIGURE 1 — TEST CIRCUIT FOR $V_{KA} = V_{ref}$

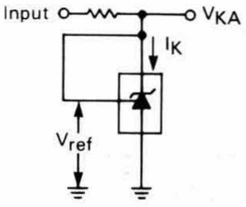
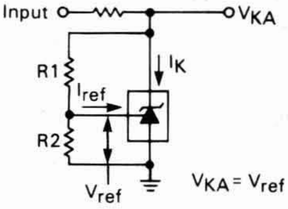
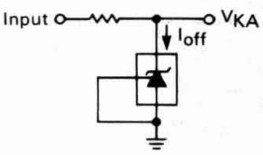


FIGURE 2 — TEST CIRCUIT FOR $V_{KA} > V_{ref}$



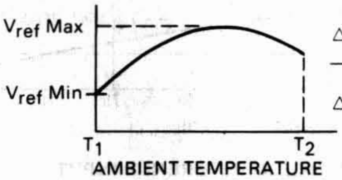
$$V_{KA} = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{ref} \cdot R1$$

FIGURE 3 — TEST CIRCUIT FOR $I_{off}$



Note 2:

The deviation parameter $\Delta V_{ref}$ is defined as the differences between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



$\Delta V_{ref} = V_{ref}$ Max
$- V_{ref}$ Min

$\Delta T_A = T_2 - T_1$

The average temperature coefficient of the reference input voltage, $\alpha V_{ref}$, is defined as:

$$\alpha V_{ref} \frac{ppm}{°C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref} @ 25°C}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25°C)}$$

$\alpha V_{ref}$ can be positive or negative depending on whether $V_{ref}$ Min or $V_{ref}$ Max occurs at the lower ambient temperature. (Refer to Figure 6)

Example: $\Delta V_{ref} = 8.0$ mV and slope is positive, $V_{ref}$ @ 25°C = 2.495 V, $\Delta T_A = 70°C$

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70\,(2.495)} = 45.8 \text{ ppm/°C}$$

**Note 3:**

**The dynamic impedance $Z_{ka}$ is defined as:**

$$|Z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$|Z_{ka}'| \approx |Z_{ka}| \left(1 + \frac{R1}{R2}\right)$$

**Note 4:**

**This test is not applicable to surface mount (D suffix) devices.**

**FIGURE 4 — CATHODE CURRENT versus CATHODE VOLTAGE**

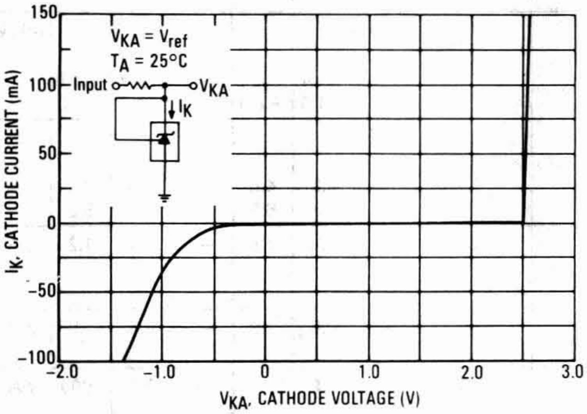


**FIGURE 5 — CATHODE CURRENT versus CATHODE VOLTAGE**

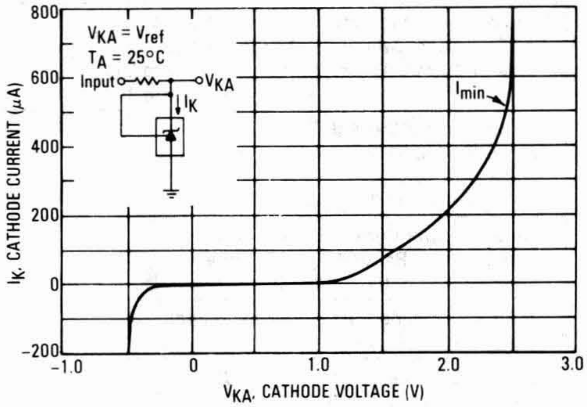


**FIGURE 6 — REFERENCE INPUT VOLTAGE versus AMBIENT TEMPERATURE**

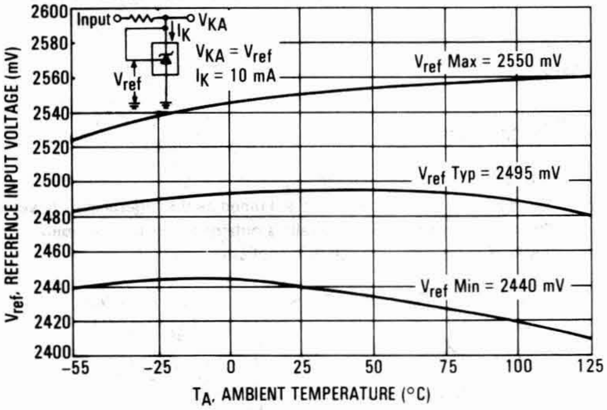


**FIGURE 7 — REFERENCE INPUT CURRENT versus AMBIENT TEMPERATURE**

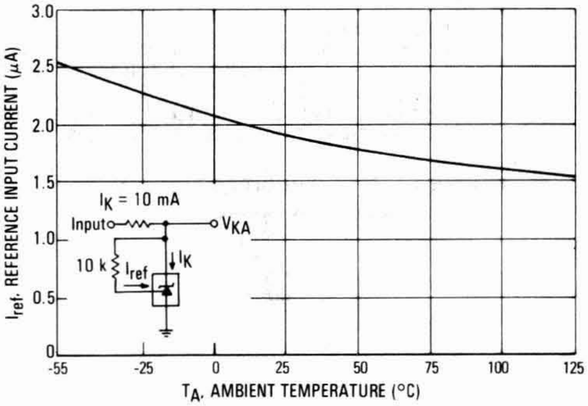


**FIGURE 8 — CHANGE IN REFERENCE INPUT VOLTAGE versus CATHODE VOLTAGE**

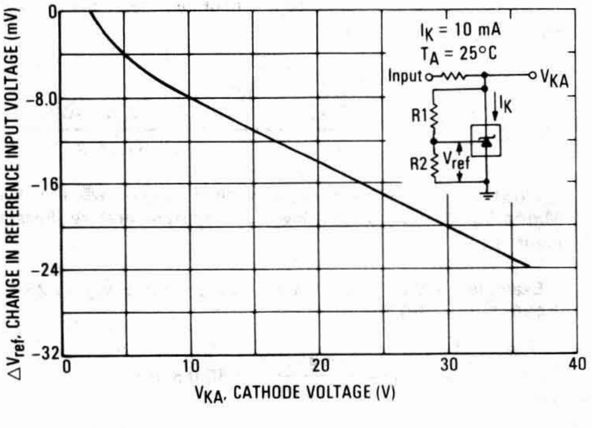
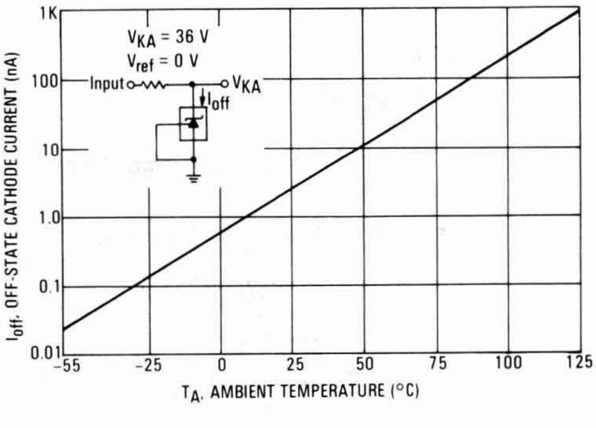
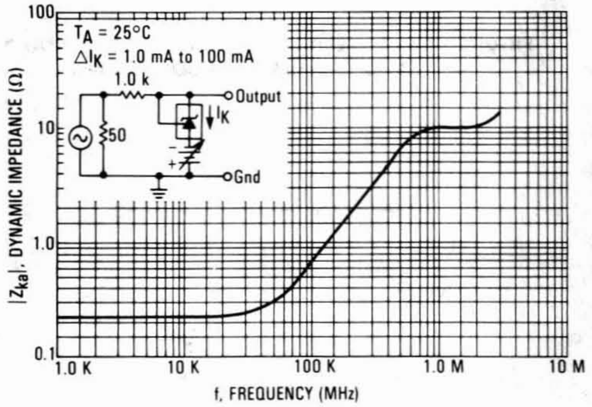


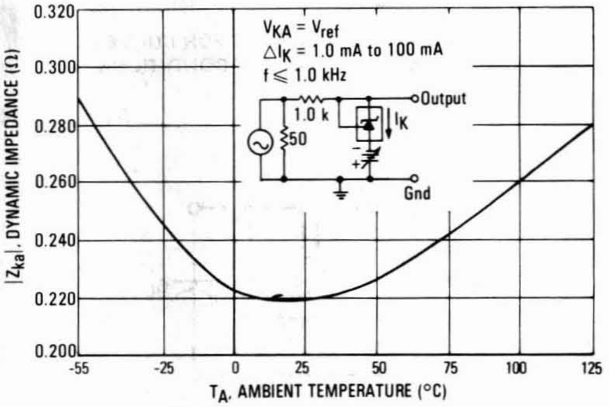
**FIGURE 9 — OFF-STATE CATHODE CURRENT versus AMBIENT TEMPERATURE**



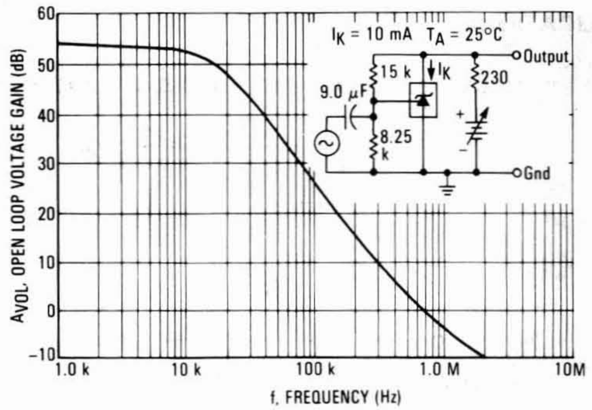
### FIGURE 10 — DYNAMIC IMPEDANCE versus FREQUENCY



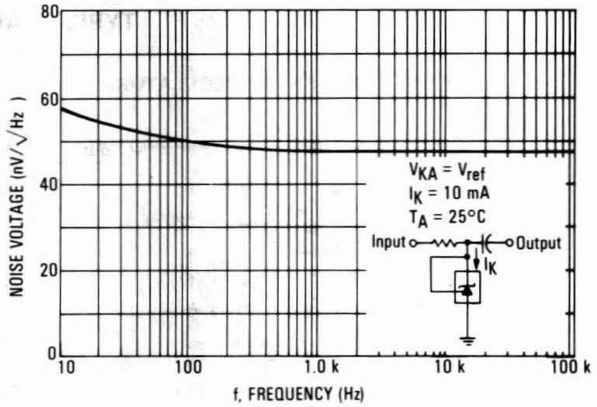
### FIGURE 11 — DYNAMIC IMPEDANCE versus AMBIENT TEMPERATURE



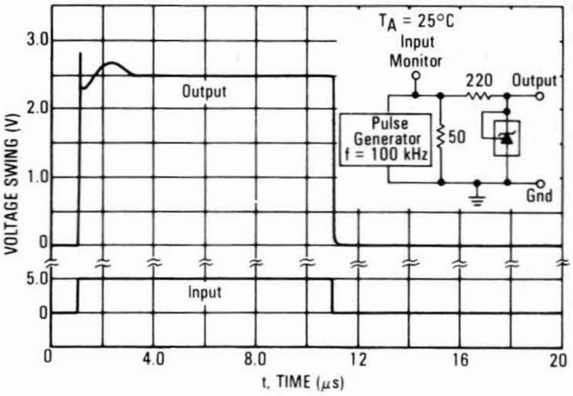
### FIGURE 12 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY



### FIGURE 13 — SPECTRAL NOISE DENSITY



### FIGURE 14 — PULSE RESPONSE



### FIGURE 15 — STABILITY BOUNDARY CONDITIONS

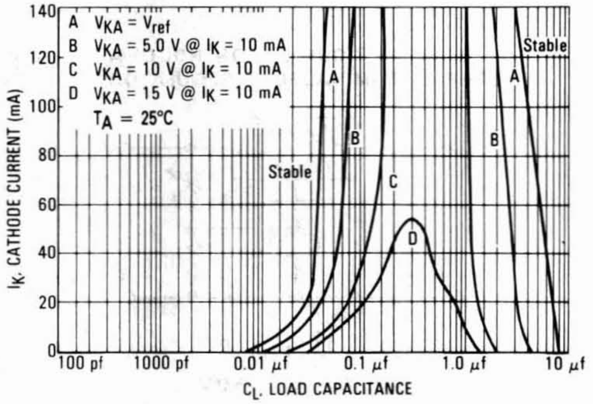


FIGURE 16 — TEST CIRCUIT FOR CURVE A OF STABILITY BOUNDARY CONDITIONS

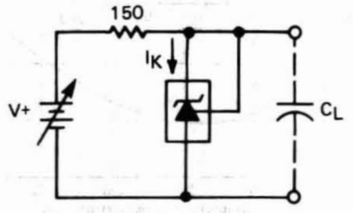
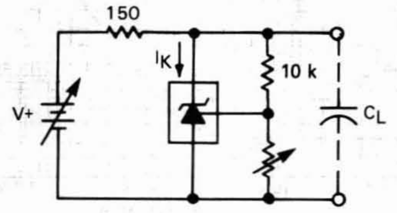
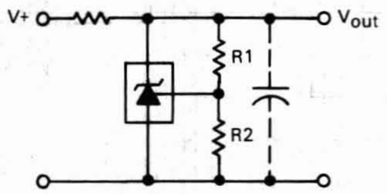


FIGURE 17 — TEST CIRCUIT FOR CURVES B, C, AND D OF STABILITY BOUNDARY CONDITIONS


150
$I_K$
10 k
V+
$C_L$

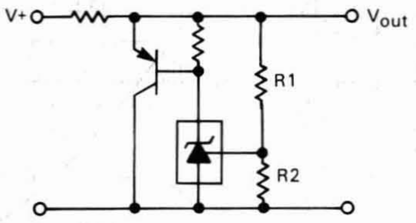
## TYPICAL APPLICATIONS

FIGURE 18 — SHUNT REGULATOR



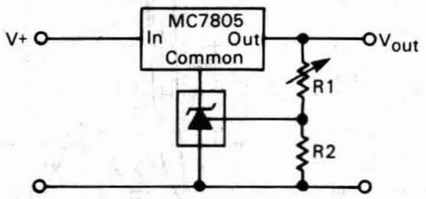
$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

FIGURE 19 — HIGH CURRENT SHUNT REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

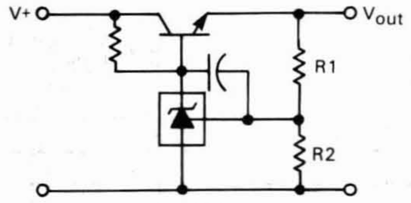
FIGURE 20 — OUTPUT CONTROL OF A THREE-TERMINAL FIXED REGULATOR


MC7805
In
Out
Common
V+
$V_{out}$
R1
R2

$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$V_{out}$ Min = $V_{ref}$ + 5.0 V

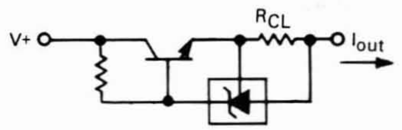
FIGURE 21 — SERIES PASS REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

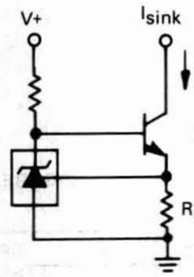
$V_{out}$ Min = $V_{ref}$ + $V_{be}$

FIGURE 22 — CONSTANT CURRENT SOURCE



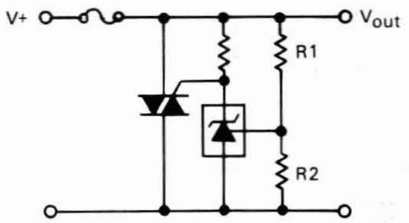
$$I_{out} = \frac{V_{ref}}{R_{CL}}$$

FIGURE 23 — CONSTANT CURRENT SINK



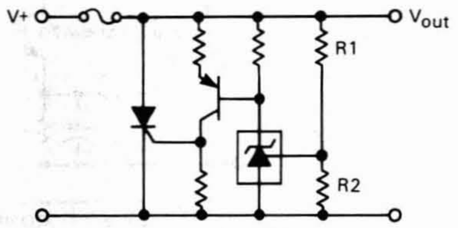
$$I_{sink} = \frac{V_{ref}}{R_S}$$

FIGURE 24 — TRIAC CROWBAR



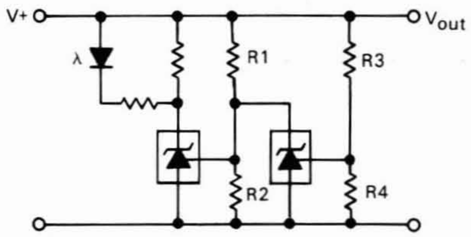
$$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

FIGURE 25 — SCR CROWBAR



$$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

FIGURE 26 — VOLTAGE MONITOR

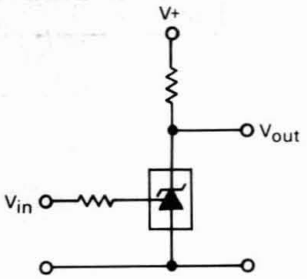

V+
$V_{out}$
λ
R1
R3
R2
R4

L.E.D. indicator is 'on' when V+ is between the upper and lower limits.

$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right)V_{ref}$$

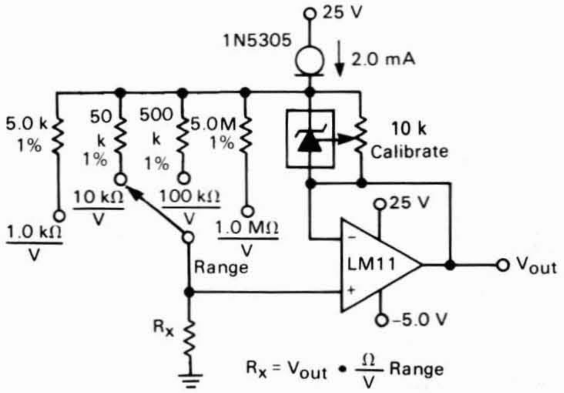
FIGURE 27 — SINGLE-SUPPLY COMPARATOR WITH TEMPERATURE-COMPENSATED THRESHOLD



$V_{th} = V_{ref}$

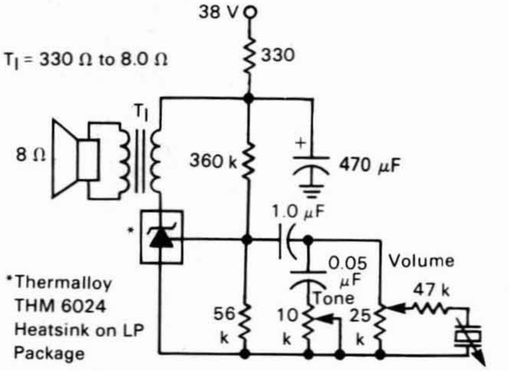
| $V_{in}$ | $V_{out}$ |
|---|---|
| $<V_{ref}$ | V+ |
| $>V_{ref}$ | ≈ 2.0 V |

FIGURE 28 — LINEAR OHMMETER


25 V
1N5305
2.0 mA
5.0 k 1%
50 k 1%
500 k 1%
5.0 M 1%
10 k Calibrate
10 kΩ/V
100 kΩ/V
1.0 kΩ/V
1.0 MΩ/V
Range
25 V
LM11
−5.0 V
$V_{out}$
$R_x$

$$R_x = V_{out} \bullet \frac{\Omega}{V} \text{ Range}$$

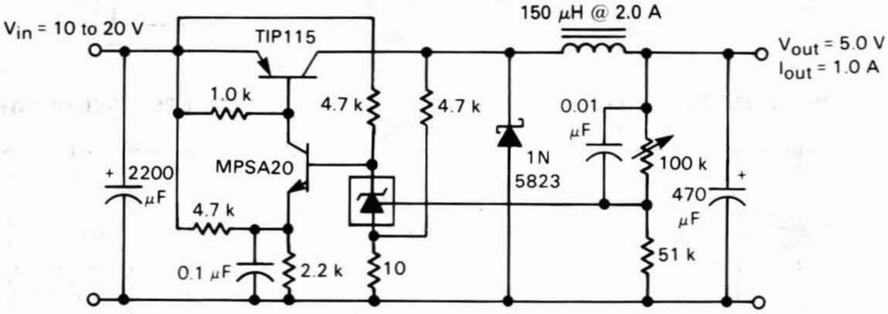
FIGURE 29 — SIMPLE 400 mW PHONO AMPLIFIER


38 V
330
$T_l$
8 Ω
360 k
470 μF
1.0 μF
*
0.05 μF
Tone
Volume
47 k
56 k
10 k
25 k

$T_l$ = 330 Ω to 8.0 Ω

*Thermalloy THM 6024 Heatsink on LP Package

FIGURE 30 — HIGH EFFICIENCY STEP-DOWN SWITCHING CONVERTER


$V_{in}$ = 10 to 20 V
TIP115
150 µH @ 2.0 A
$V_{out}$ = 5.0 V
$I_{out}$ = 1.0 A
1.0 k
4.7 k
4.7 k
0.01 µF
1N 5823
100 k
MPSA20
+
2200 µF
+
470 µF
4.7 k
51 k
0.1 µF
2.2 k
10

| TEST | CONDITIONS | RESULTS |
|---|---|---|
| Line Regulation | $V_{in}$ = 10 V to 20 V, $I_o$ = 1.0 A | 53 mV (1.1%) |
| Load Regulation | $V_{in}$ = 15 V, $I_o$ = 0A to 1.0 A | 25 mV (0.5%) |
| Output Ripple | $V_{in}$ = 10 V, $I_o$ = 1.0 A | 50 $mV_{p-p}$ P.A.R.D. |
| Output Ripple | $V_{in}$ = 20 V, $I_o$ = 1.0 A | 100 $mV_{p-p}$ P.A.R.D. |
| Efficiency | $V_{in}$ = 15 V, $I_o$ = 1.0 A | 82% |

**MOTOROLA**

# MC3423
# MC3523

## Specifications and Applications Information

## OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

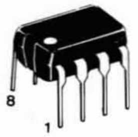
These overvoltage protection circuits (OVP) protect sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. They sense the overvoltage condition and quickly "crowbar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

The protection voltage threshold is adjustable and the MC3423/3523 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

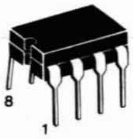
The MC3423/3523 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.

### OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04
(MC3423 only)



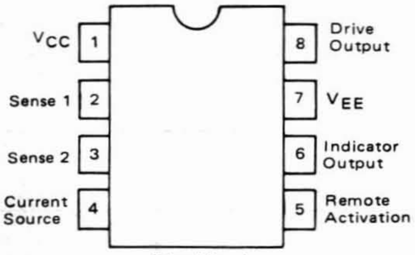
**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02

**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8

### MAXIMUM RATINGS

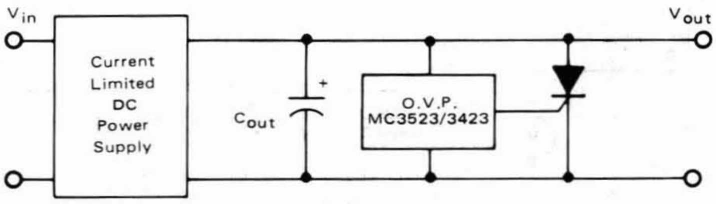
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Differential Power Supply Voltage | $V_{CC}$-$V_{EE}$ | 40 | Vdc |
| Sense Voltage (1) | $V_{Sense\ 1}$ | 6.5 | Vdc |
| Sense Voltage (2) | $V_{Sense\ 2}$ | 6.5 | Vdc |
| Remote Activation Input Voltage | $V_{act}$ | 7.0 | Vdc |
| Output Current | $I_O$ | 300 | mA |
| Operating Ambient Temperature Range<br>MC3423<br>MC3523 | $T_A$ | <br>0 to +70<br>−55 to +125 | °C |
| Operating Junction Temperature<br>Plastic Package<br>Ceramic Package | $T_J$ | <br>125<br>150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

### PIN CONNECTIONS



(Top View)

### TYPICAL APPLICATION



### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC3423D | 0 to +70°C | SO-8 |
| MC3423P1 | | Plastic DIP |
| MC3423U | | Ceramic DIP |
| MC3523U | −55 to +125°C | Ceramic DIP |

**ELECTRICAL CHARACTERISTICS** ($5\ V \leq V_{CC} - V_{EE} \leq 36\ V$, $T_{low} < T_A < T_{high}$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage Range | $V_{CC}$-$V_{EE}$ | 4.5 | – | 40 | Vdc |
| Output Voltage<br>($I_O$ = 100 mA) | $V_O$ | $V_{CC}$-2.2 | $V_{CC}$-1.8 | – | Vdc |
| Indicator Output Voltage<br>($I_{O(Ind)}$ = 1.6 mA) | $V_{OL}$(Ind) | – | 0.1 | 0.4 | Vdc |
| Sense Trip Voltage<br>($T_A$ = 25°C) | $V_{Sense\ 1}$,<br>$V_{Sense\ 2}$ | 2.45 | 2.6 | 2.75 | Vdc |
| Temperature Coefficient of $V_{Sense\ 1}$<br>(Figure 2) | $TCV_{S1}$ | – | 0.06 | – | %/°C |
| Remote Activation Input Current | | | | | µA |
| ($V_{IH}$ = 2.0 V, $V_{CC}$-$V_{EE}$ = 5.0 V) | $I_{IH}$ | – | 5.0 | 40 | |
| ($V_{IL}$ = 0.8 V, $V_{CC}$-$V_{EE}$ = 5.0 V) | $I_{IL}$ | – | -120 | -180 | |
| Source Current | $I_{Source}$ | 0.1 | 0.2 | 0.3 | mA |
| Output Current Risetime<br>($T_A$ = 25°C) | $t_r$ | – | 400 | – | mA/µs |
| Propagation Delay Time<br>($T_A$ = 25°C) | $t_{pd}$ | – | 0.5 | – | µs |
| Supply Current | $I_D$ | | | | mA |
| MC3423 | | – | 6.0 | 10 | |
| MC3523 | | – | 5.0 | 7.0 | |

$T_{low}$ = -55°C for MC3523
= 0°C for MC3423

$T_{high}$ = +125°C for MC3523
= +70°C for MC3423

FIGURE 1 – BLOCK DIAGRAM

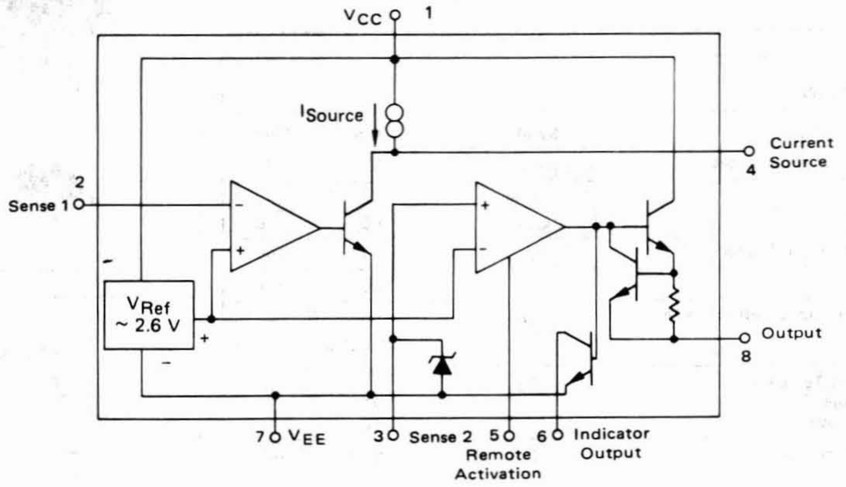
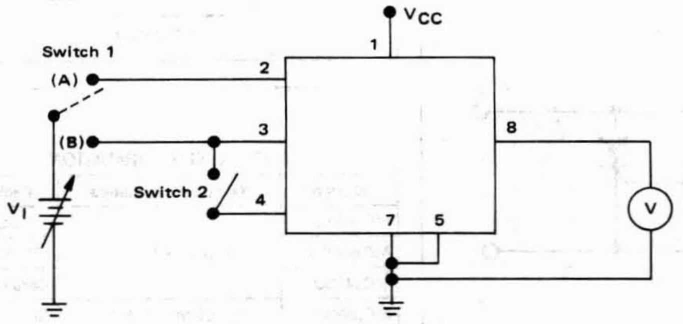

$V_{CC}$ 1
$I_{Source}$
Current Source 4
2 Sense 1
$V_{Ref}$ ~ 2.6 V
Output 8
7 $V_{EE}$
3 Sense 2
5 Remote Activation
6 Indicator Output

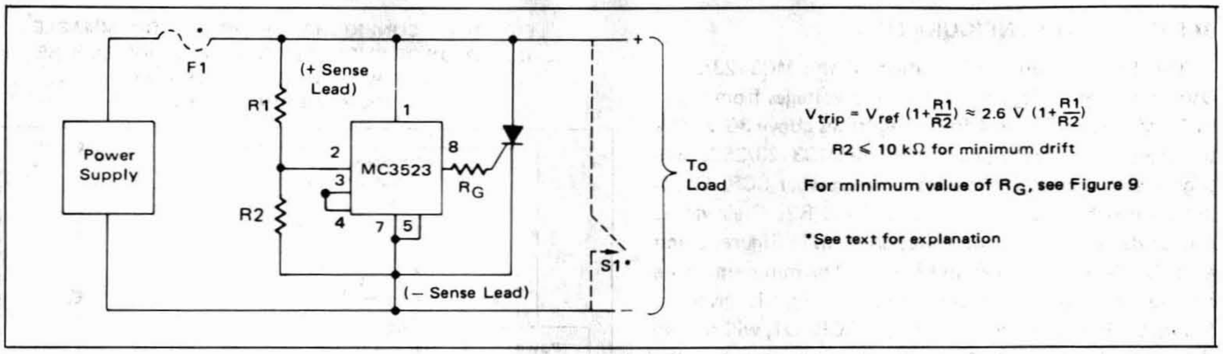
FIGURE 2 – SENSE VOLTAGE TEST CIRCUIT


$V_{CC}$
1
Switch 1
(A)
(B)
2
3
Switch 2
4
$V_I$
8
7
5
V

| | Switch 1 | Switch 2 |
|---|---|---|
| $V_{Sense\ 1}$ | Position A | Closed |
| $V_{Sense\ 2}$ | Position B | Open |

Ramp $V_I$ until output goes high; this is the $V_{Sense}$ threshold.

FIGURE 3 – BASIC CIRCUIT CONFIGURATION


F1
(+ Sense Lead)
R1
Power Supply
MC3523
1
2
3
4
7
5
8
R_G
R2
(– Sense Lead)
S1*
+
–
To Load

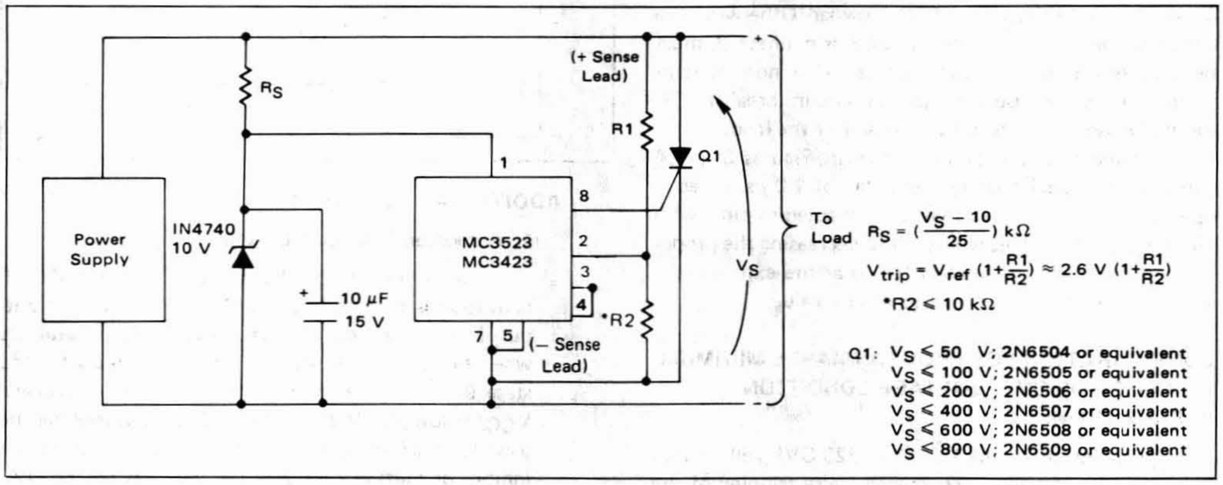
$V_{trip} = V_{ref}\,(1+\frac{R1}{R2}) \approx 2.6\ V\ (1+\frac{R1}{R2})$

R2 ≤ 10 kΩ for minimum drift

For minimum value of $R_G$, see Figure 9

*See text for explanation

FIGURE 4 – CIRCUIT CONFIGURATION FOR SUPPLY VOLTAGE ABOVE 36 V


R_S
Power Supply
IN4740
10 V
10 µF
15 V
MC3523
MC3423
1
8
2
3
4
7
5
(+ Sense Lead)
R1
Q1
*R2
(– Sense Lead)
V_S
+
–
To Load

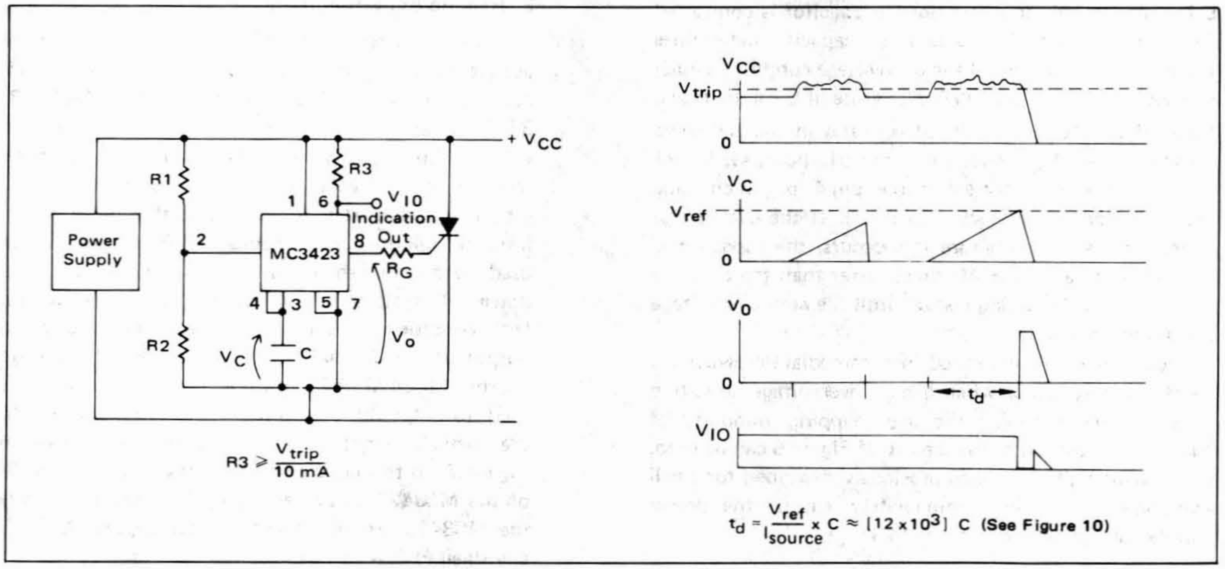
$R_S = (\frac{V_S - 10}{25})\ k\Omega$

$V_{trip} = V_{ref}\,(1+\frac{R1}{R2}) \approx 2.6\ V\ (1+\frac{R1}{R2})$

*R2 ≤ 10 kΩ

Q1: $V_S \leq 50$ V; 2N6504 or equivalent
$V_S \leq 100$ V; 2N6505 or equivalent
$V_S \leq 200$ V; 2N6506 or equivalent
$V_S \leq 400$ V; 2N6507 or equivalent
$V_S \leq 600$ V; 2N6508 or equivalent
$V_S \leq 800$ V; 2N6509 or equivalent

FIGURE 5 – BASIC CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP


+ V_CC
R1
R3
1
6
V_IO
Indication Out
Power Supply
2
MC3423
8
R_G
4
3
5
7
R2
V_C
C
V_o
V_CC
V_trip
0
V_C
V_ref
0
V_O
0
t_d
V_IO

$R3 \geq \frac{V_{trip}}{10\ mA}$

$t_d = \frac{V_{ref}}{I_{source}} \times C \approx [12 \times 10^3]\ C$ (See Figure 10)

## APPLICATIONS INFORMATION

### BASIC CIRCUIT CONFIGURATION

The basic circuit configuration of the MC3423/3523 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V, and in Figure 4 for trip voltages above 36 V. The threshold or trip voltage at which the MC3423/3523 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, $R_G$, is given in Figure 9. Using this value of $R_G$, the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423/3523. If lower output currents are required, $R_G$ can be increased in value. The switch, S1, shown in Figure 3 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

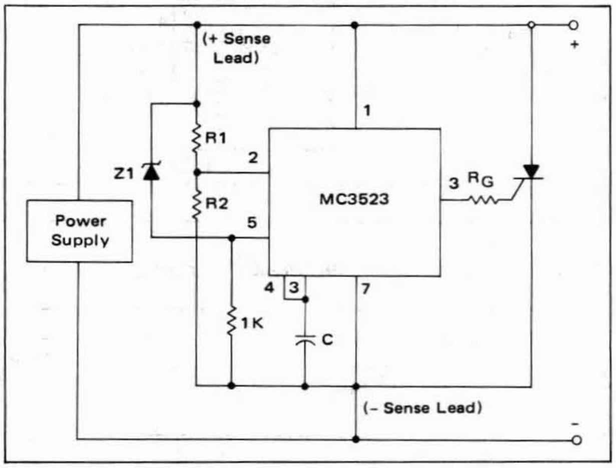
The circuit configurations shown in Figures 3 and 4 will have a typical propogation delay of 1.0 μs. If faster operation is desired, pin 3 may be connected to pin 2 with pin 4 left floating. This will result in decreasing the propogation delay to approximately 0.5 μs at the expense of a slightly increased TC for the trip voltage value.

### CONFIGURATION FOR PROGRAMMABLE MINIMUM DURATION OF OVERVOLTAGE CONDITION BEFORE TRIPPING

In many instances, the MC3423/3523 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423/3523 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from pin 3 to $V_{EE}$. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When $V_{CC}$ rises above the trip point set by R1 and R2, an internal current source (pin 4) begins charging the capacitor, C, connected to pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≅ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds $V_{Z1} + 1.4$ V.

FIGURE 6 – CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP/WITH IMMEDIATE TRIP AT HIGH OVERVOLTAGES



### ADDITIONAL FEATURES

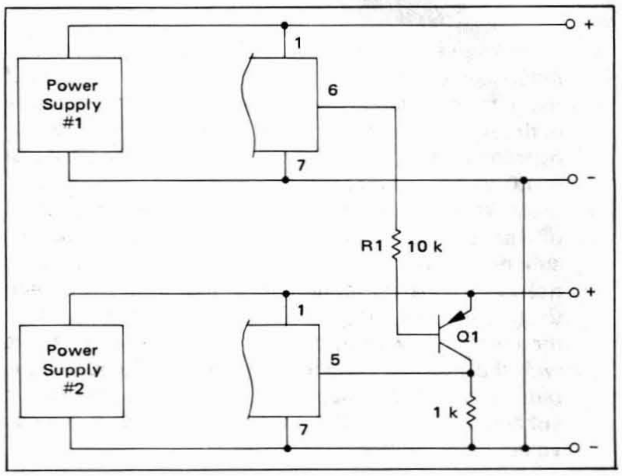
**1. Activation Indication Output**

An additional output for use as an indicator of OVP activation is provided by the MC3423/3523. This output is an open collector transistor which saturates when the OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, $V_{CC}$, below 4.5 V as in Figure 5. This output can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

**2. Remote Activation Input**

Another feature of the MC3423/3523 is its remote activation input, pin 5. If the volage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423/3523 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423/3523 can be used to activate another MC3423/3523 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

FIGURE 7 – CIRCUIT CONFIGURATION FOR ACTIVATING ONE MC3523 FROM ANOTHER



Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

## CROWBAR SCR CONSIDERATIONS

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, $C_{out}$. This capacitance consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps. This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or $I^2t$. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

### 1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities – depending on the severity of the occasion.

FIGURE 8 – R1 versus TRIP VOLTAGE

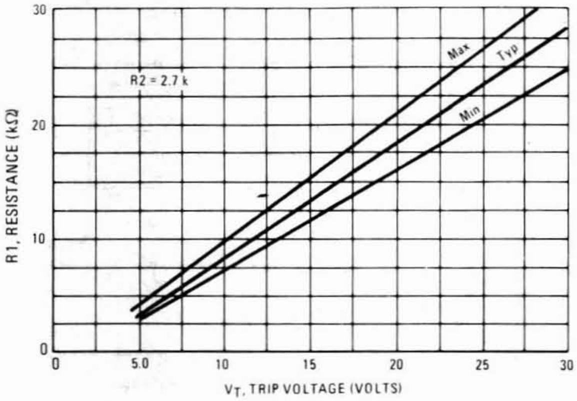


FIGURE 9 – MINIMUM $R_G$ versus SUPPLY VOLTAGE

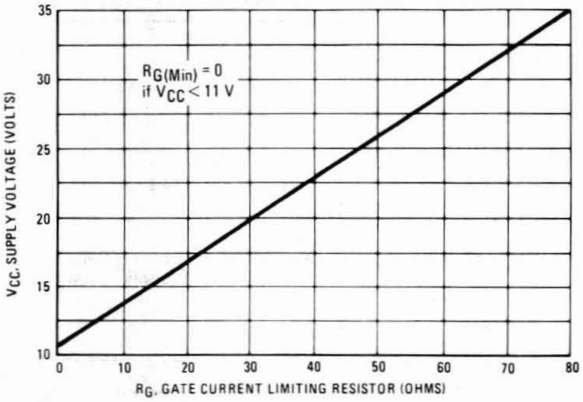


FIGURE 10 – CAPACITANCE versus MINIMUM OVERVOLTAGE DURATION

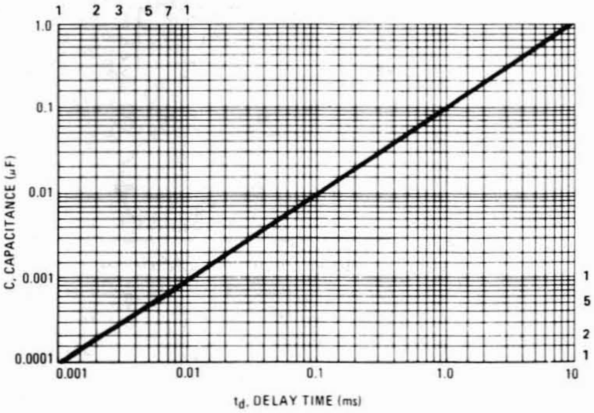


FIGURE 11 – TYPICAL CROWBAR OVP CIRCUIT CONFIGURATIONS

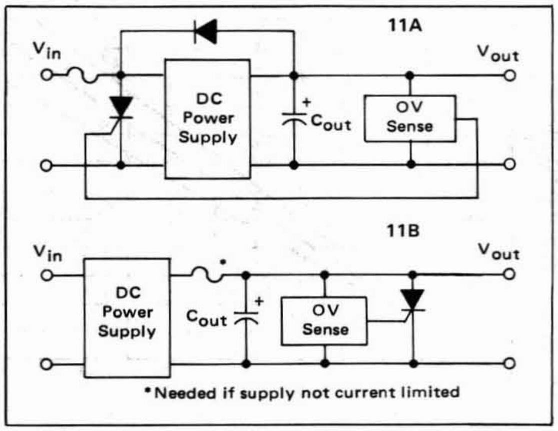


FIGURE 12 – CROWBAR SCR SURGE CURRENT WAVEFORM

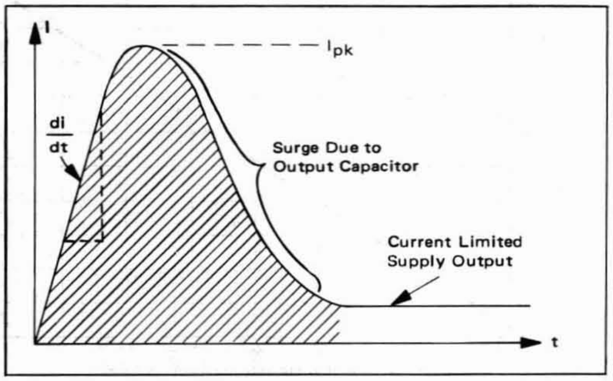
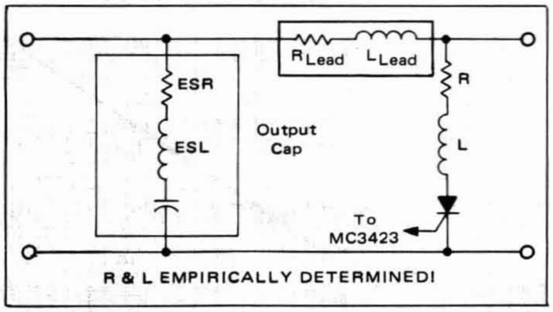


FIGURE 13 – CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times $I_{GT}$) the SCR gate with a fast $< 1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times $I_{GT}$ and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

### 2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 13) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

## A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 11A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an $I^2t$ rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

For a complete and detailed treatment of SCR and fuse selection, refer to Motorola Application Note AN-789.

### CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

| DEVICE | $I_{RMS}$ | $I_{FSM}$ | PACKAGE |
|---|---|---|---|
| 2N6400 Series | 16A | 160A | TO220 Plastic |
| 2N6504 Series | 25A | 160A | TO220 Plastic |
| 2N1842 Series | 16A | 125A | Metal Stud |
| 2N2573 Series | 25A | 260A | Metal TO-3 Type |
| 2N681 Series | 25A | 200A | Metal Stud |
| MCR3935-1 Series | 35A | 350A | Metal Stud |
| MCR81-5 Series | 80A | 1000A | Metal Stud |

**MOTOROLA**

# MC3424,A
# MC3524,A
# MC3324,A

## POWER SUPPLY SUPERVISORY CIRCUIT/DUAL VOLTAGE COMPARATOR

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

## POWER SUPPLY SUPERVISORY CIRCUIT/ DUAL-VOLTAGE COMPARATOR

The MC3424 series is a dual-channel supervisory circuit, consisting of two uncommitted input comparators, a reference, output comparators, with high current Drive and Indicator outputs for each channel. The input comparators feature programmable hysteresis, high common-mode rejection, and wide common-mode range, capable of comparing at ground potential with single-supply operation. Separate Delay pins are provided to increase noise immunity by delaying activation of the outputs. A 2.5 V bandgap voltage reference is pinned-out for referencing the input comparators, or other external functions. Independent high current Drive and Indicator outputs for each channel can source and sink up to 300 mA and 30 mA respectively. CMOS/TTL compatible digital inputs provide Remote Activation of each channel's outputs. An Input Enable pin allows control of the input comparators.

Although this device is intended for power supply supervision, the pinned-out reference, uncommitted input comparators, and many other features, enable the MC3424 series to be utilized for a wide range of applications.

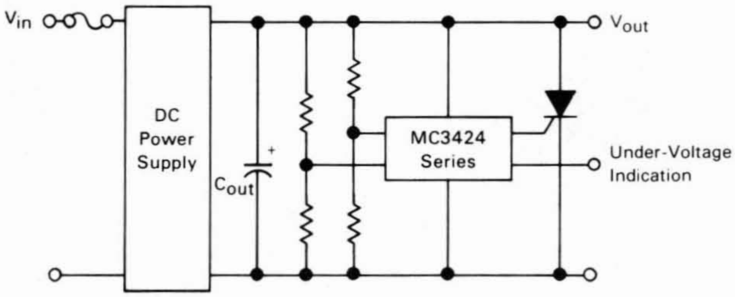
- Pinned-Out 2.5 V Reference
- Wide Common-Mode Range
- Programmable Hysteresis
- Programmable Time Delays
- Two 300 mA Drive Outputs
- Remote Activation Capability
- Wide Supply Range: $4.5\ V \leq V_{CC} \leq 40\ V$

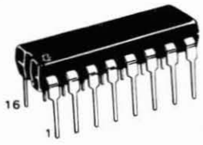
### APPLICATIONS

- Dual Over-Voltage "Crowbar" Protection
- Dual Under-Voltage Supervision
- Over/Under Voltage Protection
- Split-Supply Supervision
- Line-Loss Sensing
- Proportional Controller
- Programmable Frequency Switch
- Battery Charger

### TYPICAL APPLICATION

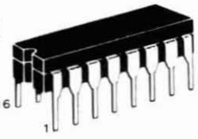
Over-Voltage Crowbar Protection, Under-Voltage Indication



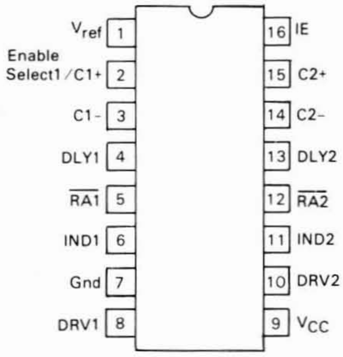


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02



### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC3524L, AL | -55 to +125°C | Ceramic DIP |
| MC3324L, AL | -40 to +85°C | Ceramic DIP |
| MC3324P, AP | | Plastic DIP |
| MC3424L, AL | 0 to +70°C | Ceramic DIP |
| MC3424P, AP | | Plastic DIP |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 40 | Vdc |
| Comparator Input Differential Voltage Range | $V_{IDR}$ | ±40 | Vdc |
| Comparator Input Voltage Range | $V_{IR}$ | -0.3 to +40 | Vdc |
| Input Enable Voltage Range | $V_{IE}$ | -0.3 to +40 | Vdc |
| Remote Activation Input Voltage Range | $V_{RA}$ | -0.3 to +40 | Vdc |
| Drive Output Short-Circuit Current | $I_{OS(DRV)}$ | Internally Limited | mA |
| Indicator Output Voltage | $V_{IND}$ | 0 to 40 | Vdc |
| Indicator Output Sink Current | $I_{IND}$ | 30 | mA |
| Reference Short-Circuit Current | $I_{OS(ref)}$ | Internally Limited | mA |
| Power Dissipation and Thermal Characteristics<br>Ceramic Package<br>Maximum Power Dissipation @ $T_A = 95°C$<br>Thermal Resistance Junction to Air<br>Plastic Package<br>Maximum Power Dissipation @ $T_A = 70°C$<br>Thermal Resistance Junction to Air | <br><br>$P_D$<br>$R_{\theta JA}$<br><br>$P_D$<br>$R_{\theta JA}$ | <br><br>1000<br>80<br><br>1000<br>80 | <br><br>mW<br>°C/W<br><br>mW<br>°C/W |
| Operating Junction Temperature<br>Ceramic Package<br>Plastic Package | $T_J$ | <br>+175<br>+150 | °C |
| Operating Ambient Temperature Range<br>MC3524, MC3524A<br>MC3324, MC3324A<br>MC3424, MC3424A | $T_A$ | <br>-55 to +125<br>-40 to +85<br>0 to +70 | °C |
| Storage Temperature Range<br>Ceramic Package<br>Plastic Package | $T_{stg}$ | <br>-65 to +175<br>-55 to +150 | °C |

## ELECTRICAL CHARACTERISTICS

(4.5 V $\leqslant V_{CC} \leqslant$ 40 V; $T_A = T_{low}$ to $T_{high}$ [see Note 1] unless otherwise specified.)

| Characteristic | Symbol | MC3524A/3424A/3324A | | | MC3524/3424/3324 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **REFERENCE SECTION** | | | | | | | | |
| Reference Output Voltage<br>$V_{CC} = 15V$; $I_L = 0$ mA<br>$T_A = 25°C$<br>$T_{low}$ to $T_{high}$ (Note 1) | $V_{ref}$ | <br><br>2.475<br>2.45 | <br><br>2.5<br>2.5 | <br><br>2.525<br>2.55 | <br><br>2.4<br>2.33 | <br><br>2.5<br>2.5 | <br><br>2.6<br>2.63 | Vdc |
| Line Regulation<br>4.5 V $\leqslant V_{CC} \leqslant$ 40 V; $I_L = 0$ mA; $T_J = 25°C$ | $Reg_{line}$ | — | 7.0 | 15 | — | 7.0 | 15 | mV |
| Load Regulation<br>0 mA $\leqslant I_L \leqslant$ 10 mA; $V_{CC} = 15$ V;<br>$T_J = 25°C$ | $Reg_{load}$ | — | 4.0 | 12 | — | 4.0 | 12 | mV |
| Output Short-Circuit Current ($T_A = 25°C$) | $I_{OS(ref)}$ | — | 23 | — | — | 23 | — | mA |
| Power Supply Voltage Operating Range | $V_{CC}$ | 4.5 | — | 40 | 4.5 | — | 40 | Vdc |
| Power Supply Current<br>$V_{CC} = 40$ V; $T_A = 25°C$; No Output Loads<br>$V_{C1-}$, $V_{C2-} = V_{CC}$;<br>$V_{C1+}$, $V_{C2+} = 0$ V | $I_{CC(off)}$ | — | 12 | 15 | — | 12 | 15 | mA |
| $V_{C1+}$, $V_{C2+} = V_{CC}$;<br>$V_{C1-}$, $V_{C2-} = 0$ V | $I_{CC(on)}$ | — | 27 | 32 | — | 27 | 32 | mA |

NOTES:

(1) $T_{low}$ = -55°C for MC3524, MC3524A
= -40°C for MC3324, MC3324A
= 0°C for MC3424, MC3424A

$T_{high}$ = +125°C for MC3524, MC3524A
= +85°C for MC3324, MC3324A
= +70°C for MC3424, MC3424A

(2) The input common-mode voltage or input signal voltage should not be allowed to go negative by more than 300 mV. The upper functional limit of the common-mode voltage range is typically $V_{CC}$ -1.4 volts, but either or both inputs can go to 40 volts, independent of $V_{CC}$, without device destruction.

(3) The $V_{th(ES1)}$ limits are approximately 0.9 times the $V_{ref}$ limits over the applicable temperature range.

(4) The $V_{th(OC)}$ limits are approximately the $V_{ref}$ limits over the applicable temperature range.

**ELECTRICAL CHARACTERISTICS** (4.5 V $\leqslant V_{CC} \leqslant$ 40 V; $T_A = T_{low}$ to $T_{high}$ [see Note 1] unless otherwise specified.)

| Characteristic | Symbol | MC3524A/3424A/3324A | | | MC3524/3424/3324 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **INPUT SECTION** | | | | | | | | |
| Input Offset Voltage<br>$T_A$ = 25°C<br>$T_{low}$ to $T_{high}$ (Note 1) | $V_{IO}$ | <br>—<br>— | <br>±3.0<br>±3.0 | <br>±8.0<br>±12 | <br>—<br>— | <br>±5.0<br>±5.0 | <br>±10<br>±15 | mV |
| Input Offset Current<br>$T_A$ = 25°C<br>$T_{low}$ to $T_{high}$ (Note 1) | $I_{IO}$ | <br>—<br>— | <br>±3.0<br>±3.0 | <br>±25<br>±250 | <br>—<br>— | <br>±3.0<br>±3.0 | <br>±25<br>±250 | nA |
| Input Bias Current<br>$T_A$ = 25°C<br>$T_{low}$ to $T_{high}$ (Note 1) | $I_{IB}$ | <br>—<br>— | <br>50<br>500 | <br>250<br>1000 | <br>—<br>— | <br>50<br>500 | <br>250<br>1000 | nA |
| Comparator Input Functional Common Mode Range ($T_A$ = 25°C, Note 2) | $V_{ICR}$ | -0.1 | $V_{CC}$-1.4 | — | -0.1 | $V_{CC}$-1.4 | — | V |
| Hysteresis Activation Voltage<br>$V_{CC}$ = 15 V; $V_{C1+}$, $V_{C2+}$ = $V_{CC}$; $T_A$ = 25°C<br>$I_H$ = 10%<br>$I_H$ = 90% | $V_{H(act)}$ | <br><br>—<br>— | <br><br>1.2<br>1.4 | <br><br>—<br>— | <br><br>—<br>— | <br><br>1.2<br>1.4 | <br><br>—<br>— | V |
| Hysteresis Current<br>$V_{CC}$ = 15 V; $V_{C1-}$, $V_{C2-}$ = 2.5 V;<br>$V_{C1+}$, $V_{C2+}$ = $V_{CC}$; $T_A$ = 25°C | $I_H$ | 10 | 12.5 | 15 | 9.0 | 12.5 | 16 | µA |
| Common Mode Rejection Ratio | CMRR | 60 | 72 | — | 60 | 72 | — | dB |
| Power Supply Rejection Ratio | PSRR | — | 95 | — | — | 95 | — | dB |
| Input Enable Threshold (Pin 16; Note 3) | $V_{th(IE)}$ | 0.9 | 1.4 | 1.9 | 0.9 | 1.4 | 1.9 | V |
| Input Enable Current (Pin 16)<br>$V_{IL(IE)}$ = 0 V<br>$V_{IH(IE)}$ = 40 V | <br>$I_{IL(IE)}$<br>$I_{IH(IE)}$ | <br>—<br>— | <br>-0.5<br>0.05 | <br>-2.5<br>1.0 | <br>—<br>— | <br>-0.5<br>0.05 | <br>-2.5<br>1.0 | µA |
| Enable Select 1 Threshold Voltage (Pin 2) | $V_{th(ES1)}$ | 2.2 | 2.25 | 2.3 | 2.1 | 2.25 | 2.4 | V |
| Delay Pin Voltage ($I_{DLY}$ = 0 mA)<br>Low State<br>High State | <br>$V_{OL(DLY)}$<br>$V_{OH(DLY)}$ | <br>—<br>$V_{CC}$-0.5 | <br>0.2<br>$V_{CC}$-0.15 | <br>0.5<br>— | <br>—<br>$V_{CC}$-0.5 | <br>0.2<br>$V_{CC}$-0.15 | <br>0.5<br>— | V |
| Delay Pin Source Current<br>$V_{CC}$ = 15 V; $V_{DLY1}$, $V_{DLY2}$ = 0 V | $I_{DLY(source)}$ | 150 | 200 | 250 | 140 | 200 | 260 | µA |
| Delay Pin Sink Current<br>$V_{CC}$ = 15 V; $V_{DLY1}$, $V_{DLY2}$ = 2.5 V | $I_{DLY(sink)}$ | 1.8 | 3.0 | — | 1.8 | 3.0 | — | mA |
| **OUTPUT SECTION** | | | | | | | | |
| Drive Output Peak Current ($T_A$ = 25°C) | $I_{DRV(peak)}$ | 200 | 300 | — | 200 | 300 | — | mA |
| Drive Output V ($I_{DRV}$ = 100 mA; $T_A$ = 25°C) | $V_{OH(DRV)}$ | $V_{CC}$-2.5 | $V_{CC}$-2.0 | — | $V_{CC}$-2.5 | $V_{CC}$-2.0 | — | V |
| Drive Output Leakage Current ($V_{DRV}$ = 0 V) | $I_{DRV(leak)}$ | — | 15 | 200 | — | 15 | 200 | nA |
| Drive Output Current Slew Rate ($T_A$ = 25°C) | di/dt | — | 2.0 | — | — | 2.0 | — | A/µS |
| Drive Output Transient Rejection ($T_A$ = 25°C)<br>$V_{CC}$ = 0 V to 15 V at dV/dt = 200 V/µs;<br>$V_{C1-}$, $V_{C2-}$ = $V_{ref}$; $V_{C1+}$, $V_{C2+}$ = 0 V | $I_{DRV(trans)}$ | — | 1.0 | — | — | 1.0 | — | mA (Peak) |
| Indicator Output Saturation Voltage<br>$I_{IND}$ = 30 mA; $T_A$ = 25°C | $V_{IND(sat)}$ | — | 560 | 800 | — | 560 | 800 | mV |
| Indicator Output Leakage Current<br>$V_{OH(IND)}$ = 40 V | $I_{IND(leak)}$ | — | 25 | 200 | — | 25 | 200 | nA |
| Output Comparator Threshold V (Note 4) | $V_{th(OC)}$ | 2.45 | 2.5 | 2.55 | 2.33 | 2.5 | 2.63 | V |
| Remote Activation Threshold Voltage | $V_{th(RA)}$ | 1.3 | 1.4 | 1.5 | 1.1 | 1.4 | 1.7 | V |
| Remote Activation Current<br>$V_{IL(RA)}$ = 0 V<br>$V_{IH(RA)}$ = 40 V | <br>$I_{IL(RA)}$<br>$I_{IH(RA)}$ | <br>—<br>— | <br>-100<br>70 | <br>-250<br>250 | <br>—<br>— | <br>-100<br>70 | <br>-250<br>250 | µA |
| Propagation Delay ($V_{CC}$ = 15 V; $T_A$ = 25°C)<br>Input to Drive Output<br>100 mV Overdrive, $C_{DLY}$ = 0 µF | $t_{PLH(IN/DRV)}$ | — | 1.0 | — | — | 1.0 | — | µs |
| Remote Activation to Drive Output<br>1.4 V Overdrive (2.5 V to 0 V Step) | $t_{PLH(RA/DRV)}$ | — | 600 | — | — | 600 | — | ns |

FIGURE 1 — HYSTERESIS CURRENT versus HYSTERESIS ACTIVATION VOLTAGE

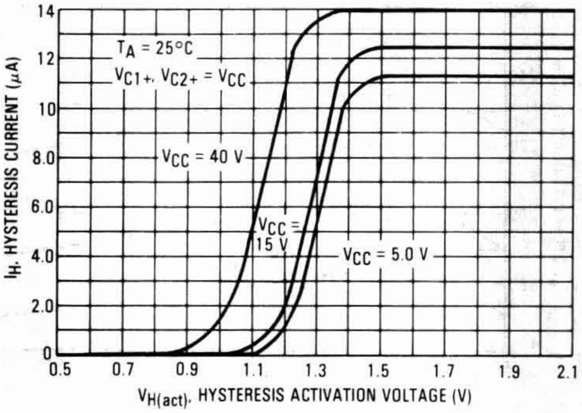


FIGURE 2 — HYSTERESIS ACTIVATION VOLTAGE versus TEMPERATURE

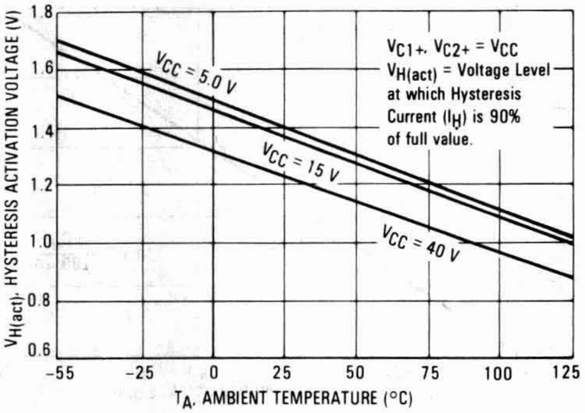


FIGURE 3 — HYSTERESIS CURRENT versus TEMPERATURE

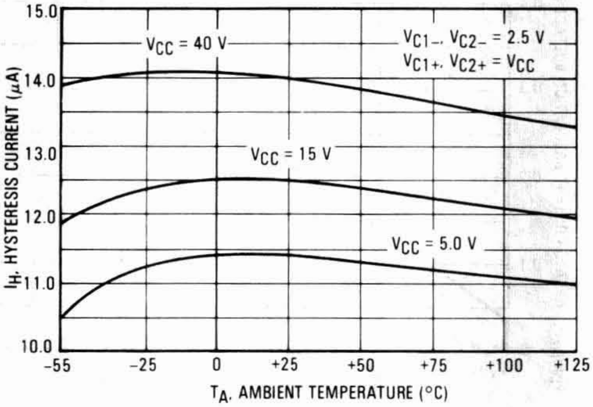


FIGURE 4 — REFERENCE VOLTAGE CHANGE versus OUTPUT CURRENT

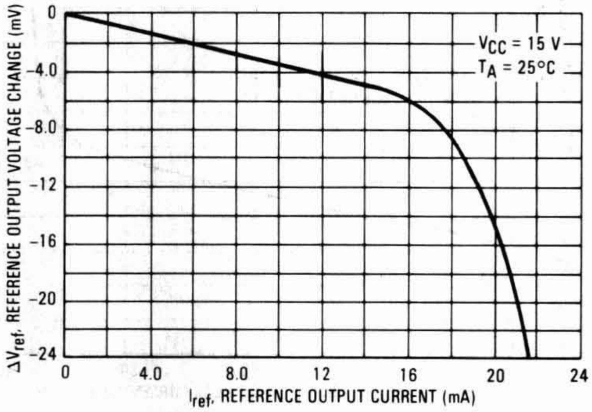


FIGURE 5 — REFERENCE VOLTAGE CHANGE versus TEMPERATURE

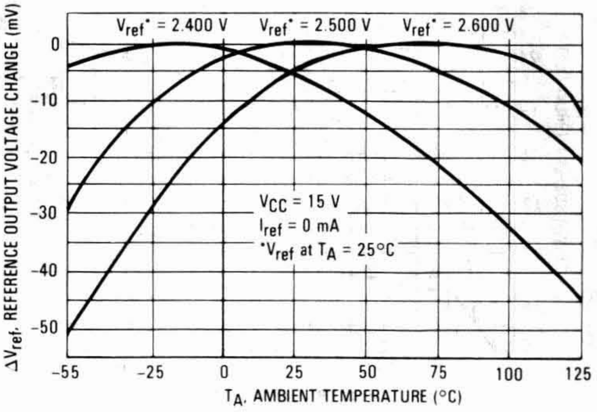
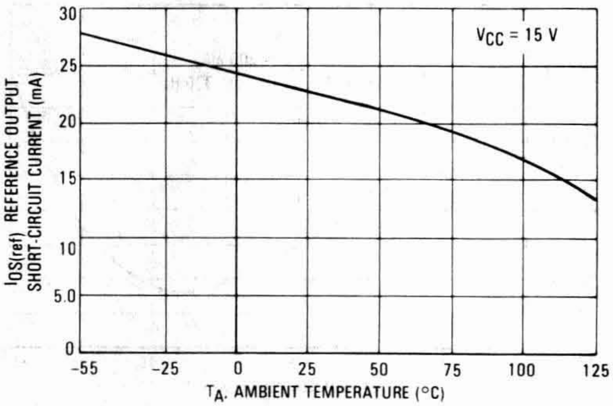
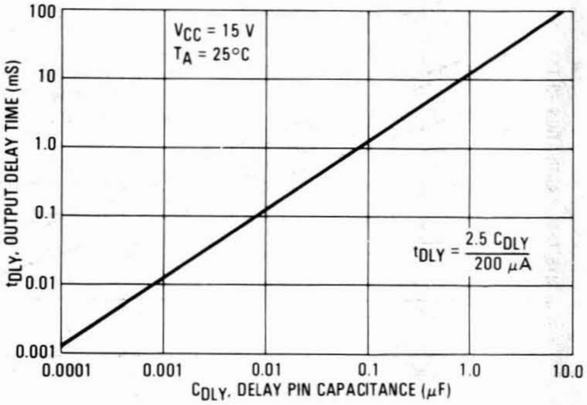


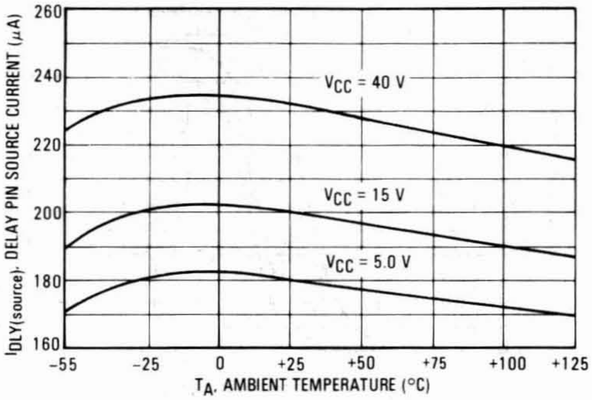
FIGURE 6 — REFERENCE SHORT-CIRCUIT CURRENT versus TEMPERATURE



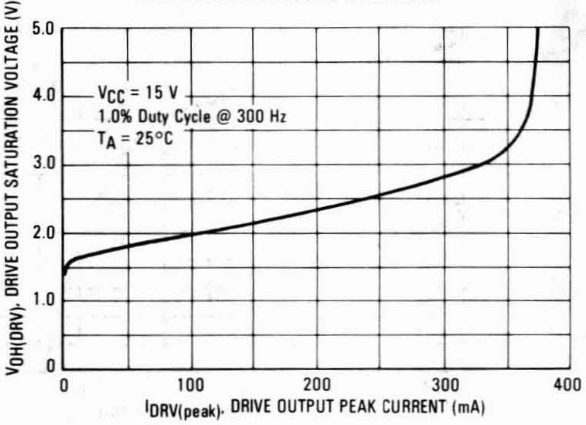
### FIGURE 7 — OUTPUT DELAY TIME versus DELAY CAPACITANCE



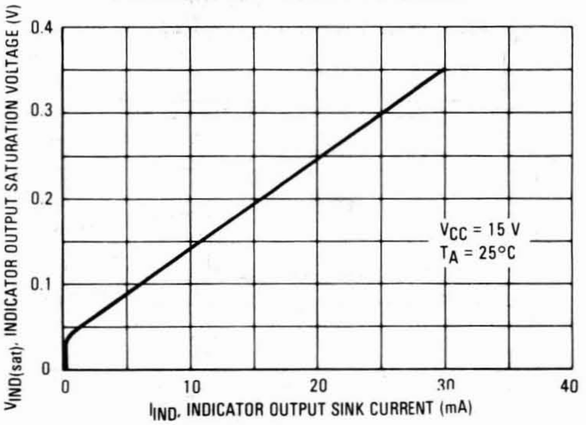
### FIGURE 8 — DELAY PIN SOURCE CURRENT versus TEMPERATURE



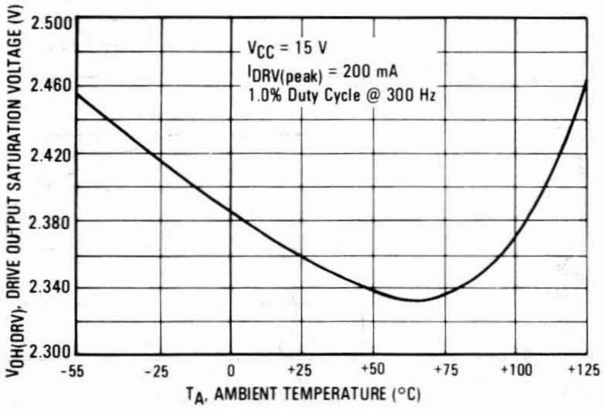
### FIGURE 9 — DRIVE OUTPUT SATURATION VOLTAGE versus OUTPUT PEAK CURRENT



### FIGURE 10 — INDICATOR OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT



### FIGURE 11 — DRIVE OUTPUT SATURATION VOLTAGE versus TEMPERATURE



### FIGURE 12 — POWER SUPPLY CURRENT versus VOLTAGE

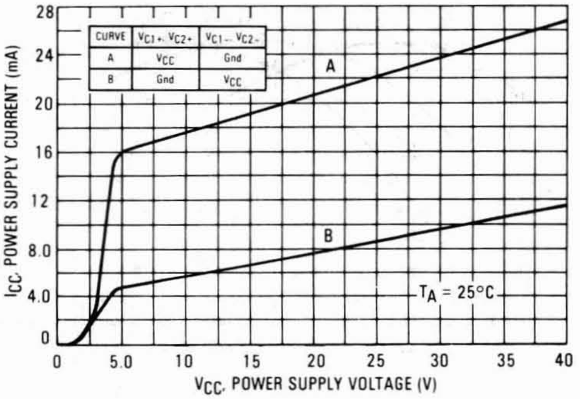
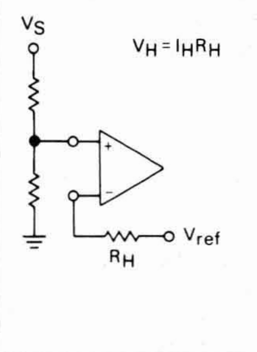
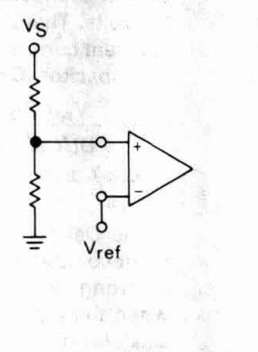
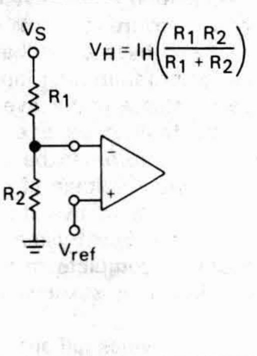
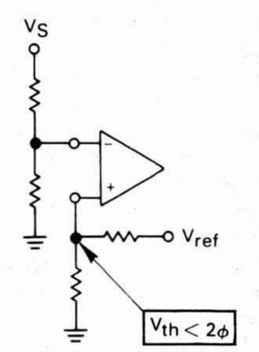
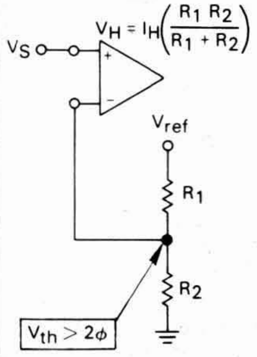
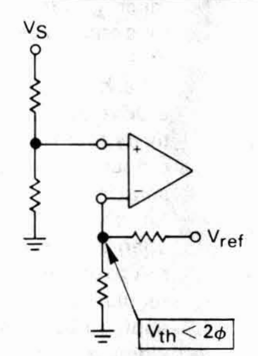
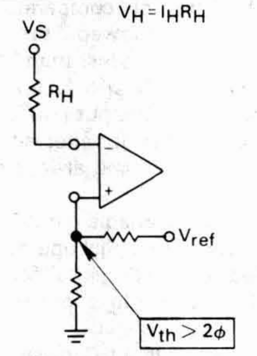
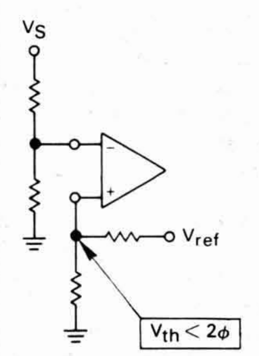
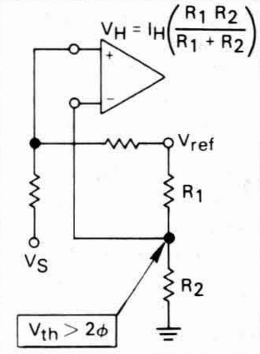
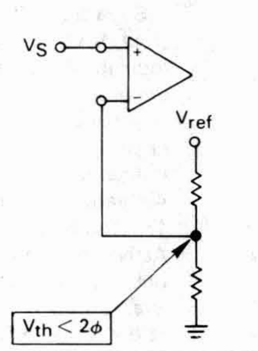
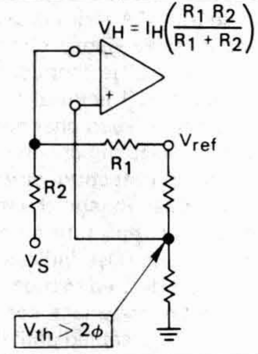
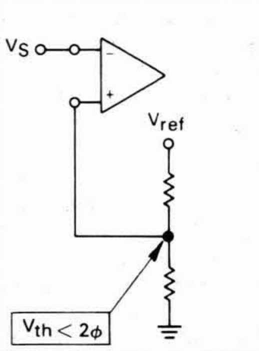
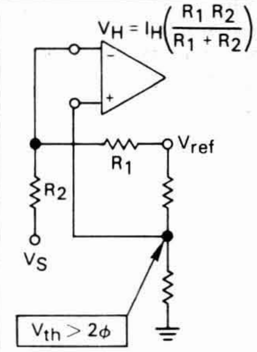
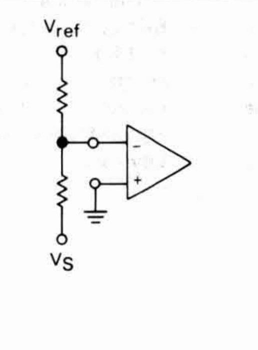
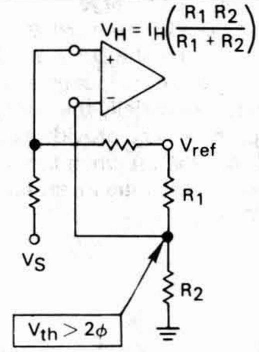
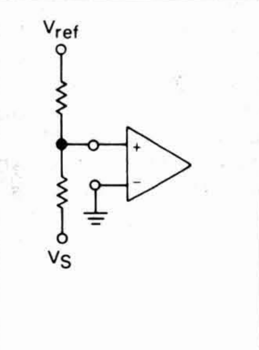


FIGURE 13 — THE COMPLETE VOLTAGE SENSE CAPABILITY OF THE INPUT COMPARATORS, WITH OR WITHOUT PROGRAMMABLE HYSTERESIS.

| | VOLTAGE SENSE ($V_S$) | | | |
|---|---|---|---|---|
| | OVER | | UNDER | |
| | WITH HYSTERESIS | WITHOUT HYSTERESIS | WITH HYSTERESIS | WITHOUT HYSTERESIS |
| $V_S > V_{ref}$ |   $V_S$<br>$V_H = I_HR_H$<br>+<br>−<br>$V_{ref}$<br>$R_H$ |  |   $V_S$<br>$V_H = I_H\left(\frac{R_1 R_2}{R_1 + R_2}\right)$<br>$R_1$<br>−<br>+<br>$R_2$<br>$V_{ref}$ |   $V_S$<br>−<br>+<br>$V_{ref}$<br>$V_{th} < 2\phi$ |
| $V_S \leq V_{ref}$<br>$V_S \geq 2\phi$* |   $V_H = I_H\left(\frac{R_1 R_2}{R_1 + R_2}\right)$<br>$V_S$<br>+<br>−<br>$V_{ref}$<br>$R_1$<br>$R_2$<br>$V_{th} > 2\phi$ |   $V_S$<br>+<br>−<br>$V_{ref}$<br>$V_{th} < 2\phi$ |   $V_H = I_HR_H$<br>$V_S$<br>$R_H$<br>−<br>+<br>$V_{ref}$<br>$V_{th} > 2\phi$ |   $V_S$<br>−<br>+<br>$V_{ref}$<br>$V_{th} < 2\phi$ |
| $V_S < 2\phi$*<br>$V_S \geq 0$ V |   $V_H = I_H\left(\frac{R_1 R_2}{R_1 + R_2}\right)$<br>+<br>−<br>$V_{ref}$<br>$R_1$<br>$V_S$<br>$R_2$<br>$V_{th} > 2\phi$ |   $V_S$<br>+<br>−<br>$V_{ref}$<br>$V_{th} < 2\phi$ |   $V_H = I_H\left(\frac{R_1 R_2}{R_1 + R_2}\right)$<br>−<br>+<br>$V_{ref}$<br>$R_1$<br>$R_2$<br>$V_S$<br>$V_{th} > 2\phi$ |   $V_S$<br>−<br>+<br>$V_{ref}$<br>$V_{th} < 2\phi$ |
| $V_S < 0$ V |   $V_H = I_H\left(\frac{R_1 R_2}{R_1 + R_2}\right)$<br>−<br>+<br>$V_{ref}$<br>$R_1$<br>$R_2$<br>$V_S$<br>$V_{th} > 2\phi$ |  |   $V_H = I_H\left(\frac{R_1 R_2}{R_1 + R_2}\right)$<br>+<br>−<br>$V_{ref}$<br>$R_1$<br>$V_S$<br>$R_2$<br>$V_{th} > 2\phi$ |  |

*$2\phi \simeq 1.1$ Volts at $T_J = 25$°C

## CIRCUIT DESCRIPTION

The MC3424 series is a high current output, dual channel power supply supervisory circuit. Basic circuit configuration is shown in Figure 29. Each channel features a true differential input comparator with a common-mode range from ground potential to $V_{CC} - 1.4$ volts, with single supply operation. The inverting inputs of each input comparator (C1 −, C2 −) have a feedback activated 12.5 µA current sink for programming input comparator hysteresis. Source resistance of the inverting inputs determines the amount of hysteresis for each input comparator. The hysteresis feature can be defeated by reducing the inverting input voltage of the respective input comparator to less than two diode drops ($2\ \phi \approx 1.1$ volts) above Gnd (See Hysteresis Activation Voltage specification). A complete matrix of various input comparator conditions is shown in Figure 13.

The digital Input Enable (IE) pin provides full enable/disable control of one or both of the input comparators. Input Comparator 1 enable control is allowed if the Enable Select1/Non-Inverting Input (Pin 2) is less than 90% of the internal 2.5 volts reference ($0.9\ V_{ref} \cong 2.25$ V). If the Input Enable Select1/Non-Inverting Input (Pin 2) is greater than $0.9\ V_{ref}$, Comparator 1 is not affected by the logic state of the Input Enable pin and always remains enabled.

The voltage threshold of the Input Enable pin is TTL compatible. A logic level "1" permits normal operation of input comparators, as stated above. A logic "0" forces the respective Delay pin (DLY1, DLY2) to a low state, independent of the input comparator's state.

The selective enabling feature of Input Comparator 1 is directly applicable when the MC3424 series is used as an over- and under-voltage supervisory circuit, where channel 2 (Input Comparator 2) is monitoring under-voltage conditions, and channel 1 is utilized for over-voltage protection. The ability to keep channel 1 (Input Comparator 1) active, while disabling channel 2, provides immediate over-voltage protection during power supply turn-on, while the under-voltage channel (2) can be disabled during the power supply turn-on rise time to the regulated level, preventing false indication of an under-voltage condition. If it is desired to monitor two independent voltages for an under-voltage condition, both channels can be selectively disabled until the slowest supply reaches its regulated voltage.

Separate Delay pins (DLY1, DLY2) are provided for each channel to independently delay the Drive and Indicator Outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source of typically 200 µA when the non-inverting input voltage is greater than the inverting input level ($V_{C1+} > V_{C1-}$; $V_{C2+} > V_{C2-}$).

A capacitor ($C_{DLY}$) tied to these Delay pins will establish a predictable delay time ($t_{DLY}$) of the Drive and Indicator outputs for the respective channel. The Delay pins are internally tied to the non-inverting input of Output Comparators 1 and 2, which are referenced to 2.5 volts. Therefore, delay time ($t_{DLY}$) is based on the constant current $I_{DLY(source)}$ charging the external delay capacitor ($C_{DLY}$) to 2.5 volts or;

$$t_{DLY} = \frac{V_{ref}\ C_{DLY}}{I_{DLY(source)}} = \frac{2.5\ C_{DLY}}{200\ \mu A} = 12500\ C_{DLY}.$$

Figure 7 provides $C_{DLY}$ values for a wide range of time delays.

The Delay pins are pulled low when the respective input comparator's non-inverting input is less than the inverting input ($V_{C1+} < V_{C1-}$; $V_{C2+} < V_{C2-}$), or when the Input Enable pin is at a low logic level. The sink current ($\geq 1.8$ mA) capability of the Delay pins is much greater than the typical 200 µA source current, thus enabling a relatively fast delay capacitor discharge time.

Each independent channel of the MC3424 series has a Drive (DRV) and Indicator output (IND) which respectively source and sink current simultaneously. The Drive outputs are current-limited emitter-followers capable of sourcing 300 mA at a turn-on slew rate of 2.0 A/µs, ideal for driving "Crowbar" SCR's. The Indicator outputs are open collector, NPN transistors, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or regular shut-down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

Separate TTL-compatible Remote Activation inputs ($\overline{RA1}$, $\overline{RA2}$) for each channel will activate the Drive and Indicator outputs of the respective channel, independent of the input comparator state, when a low logic level is applied. The active low for remote activation permits latching of the respective outputs by connecting the Indicator output, via a ≤ 5.0 k resistor to the Remote Activation input of the same channel, as shown in Figure 17. Latching will now occur by either of the Remote Activation inputs with a short duration low logic level, or by the input comparators. Unlatching of each channel is accomplished with a short duration, high logic level at the Remote Activation pin.

The MC3424 series has an internal 2.5 V bandgap reference capable of sourcing up to 10 mA of load current for external bias circuits. This reference has an accuracy of ±4.0% for the basic devices and ±1.0% for the A-suffix device types at 25°C. The reference has a typical temperature coefficient of 30 ppm/°C for A-suffix devices.

## CROWBAR SCR CONSIDERATIONS

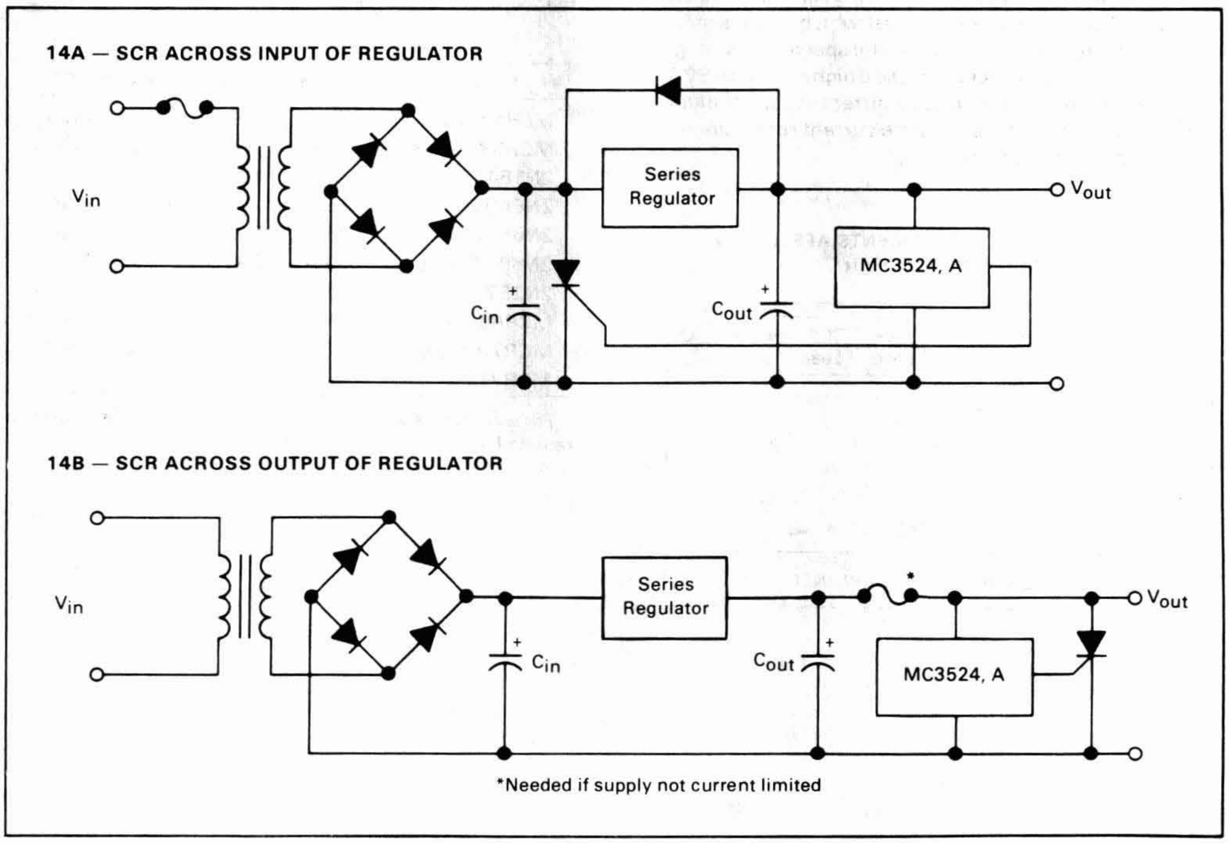
Referring to Figure 14, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, $C_{out}$. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 14A, the supply's input filter capacitors. This surge current is illustrated in Figure 15, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or $I^2t$. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

### 1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

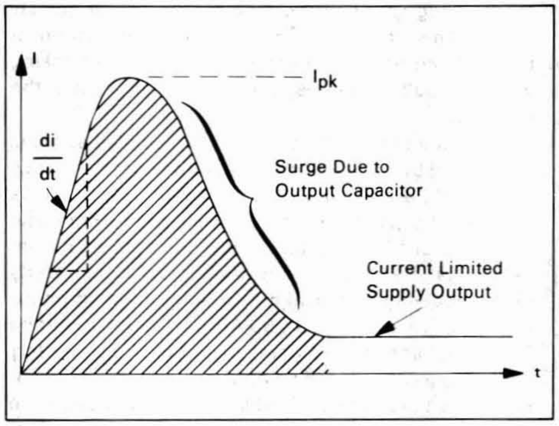
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times $I_{GT}$) the SCR gate with a fast <1.0 μs rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times $I_{GT}$ and < 1.0 μs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 16. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 14 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS



*Needed if supply not current limited

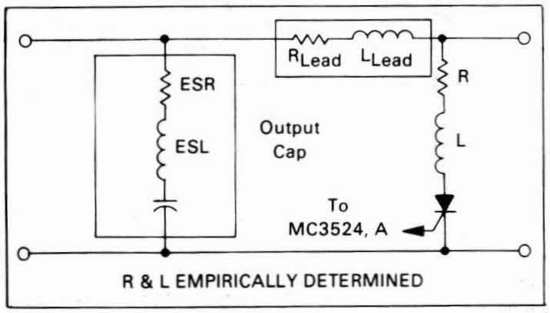
FIGURE 15 — CROWBAR SCR SURGE CURRENT WAVEFORM



**2. Surge Current**

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 16) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 16 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



## A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 14A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an $I^2t$ rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 14B.

## CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

| DEVICE | $I_{RMS}$ | $I_{FSM}$ | PACKAGE |
|---|---|---|---|
| MCR67 Series | 12 A | 100 A | Metal Stud |
| MCR68 Series | 12 A | 100 A | TO-220 Plastic |
| 2N1842 Series | 16 A | 125 A | Metal Stud |
| 2N6400 Series | 16 A | 160 A | TO-220 Plastic |
| 2N6504 Series | 25 A | 160 A | TO-220 Plastic |
| 2N681 Series | 25 A | 200 A | Metal Stud |
| 2N2573 Series | 25 A | 260 A | TO-3 Metal Can |
| MCR69 Series | 25 A | 300 A | TO-220 Plastic |
| MCR70 Series | 35 A | 350 A | Metal Stud |
| MCR71 Series | 55 A | 550 A | Metal Stud |

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

## APPLICATIONS INFORMATION

FIGURE 17 — OVERVOLTAGE PROTECTION OF SPLIT SUPPLIES WITH DELAY AND LATCHED-FAULT INDICATION.

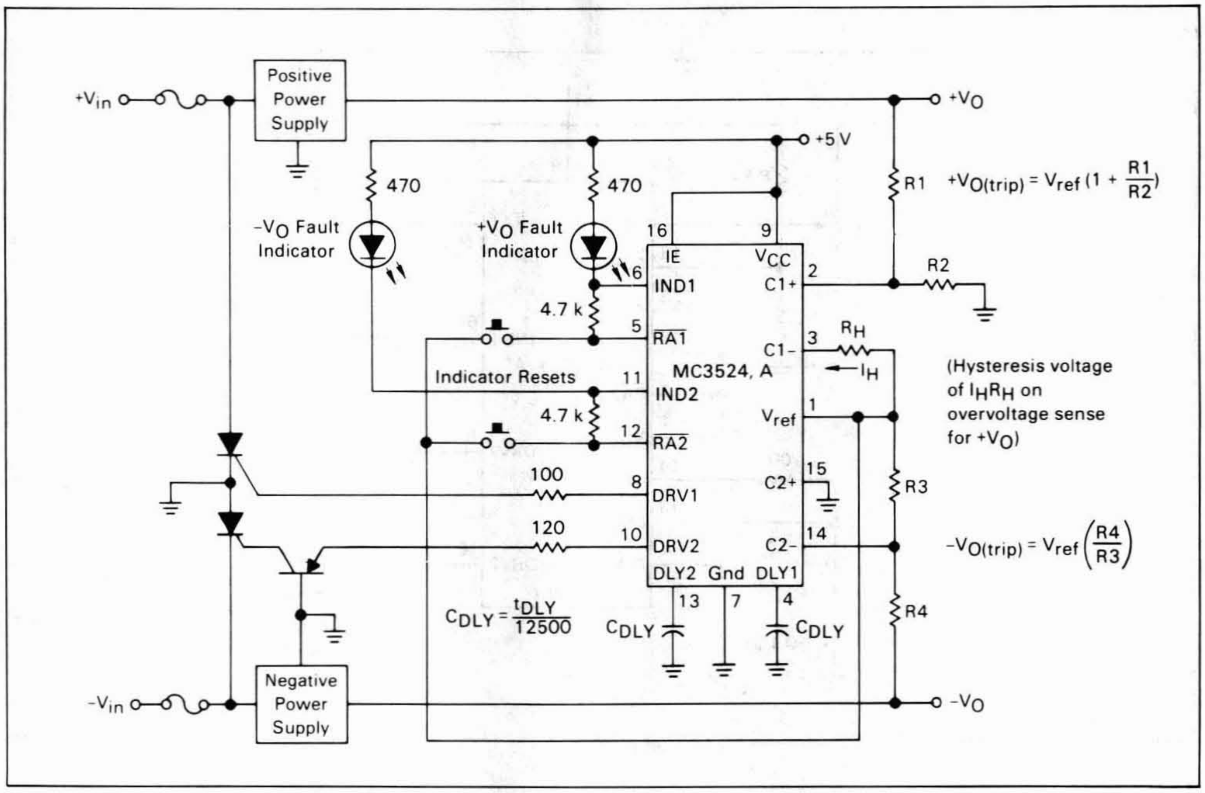

+Vin
Positive Power Supply
+VO
+5 V
470
470
R1
+VO(trip) = Vref (1 + R1/R2)
-VO Fault Indicator
+VO Fault Indicator
16
9
IE
VCC
6
IND1
2
C1+
R2
4.7 k
5
RA1
C1-
3
RH
IH
Indicator Resets
11
MC3524, A
IND2
(Hysteresis voltage of IHRH on overvoltage sense for +VO)
4.7 k
12
RA2
1
Vref
100
8
DRV1
15
C2+
R3
120
10
DRV2
14
C2-
-VO(trip) = Vref (R4/R3)
DLY2
Gnd
DLY1
13
7
4
CDLY = tDLY/12500
CDLY
CDLY
R4
Negative Power Supply
-Vin
-VO

FIGURE 18 — OVERVOLTAGE PROTECTION OF 5.0 V SUPPLY WITH LINE LOSS DETECTOR

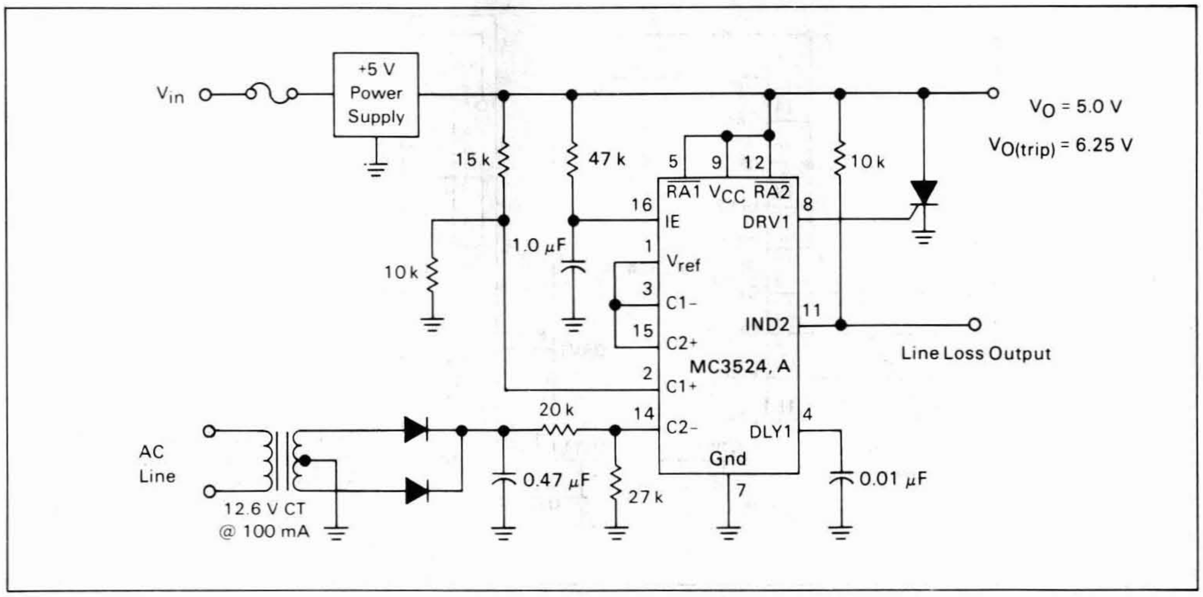

Vin
+5 V Power Supply
VO = 5.0 V
VO(trip) = 6.25 V
15 k
47 k
5
9
12
10 k
RA1
VCC
RA2
16
IE
DRV1
8
1.0 μF
1
Vref
10 k
3
C1-
15
C2+
IND2
11
Line Loss Output
2
C1+
MC3524, A
20 k
14
C2-
DLY1
4
Gnd
AC Line
12.6 V CT @ 100 mA
0.47 μF
27 k
7
0.01 μF

FIGURE 19 — LATCHING OVERVOLTAGE SENSING CIRCUIT WITH INTERMITTENT AUDIO ALARM

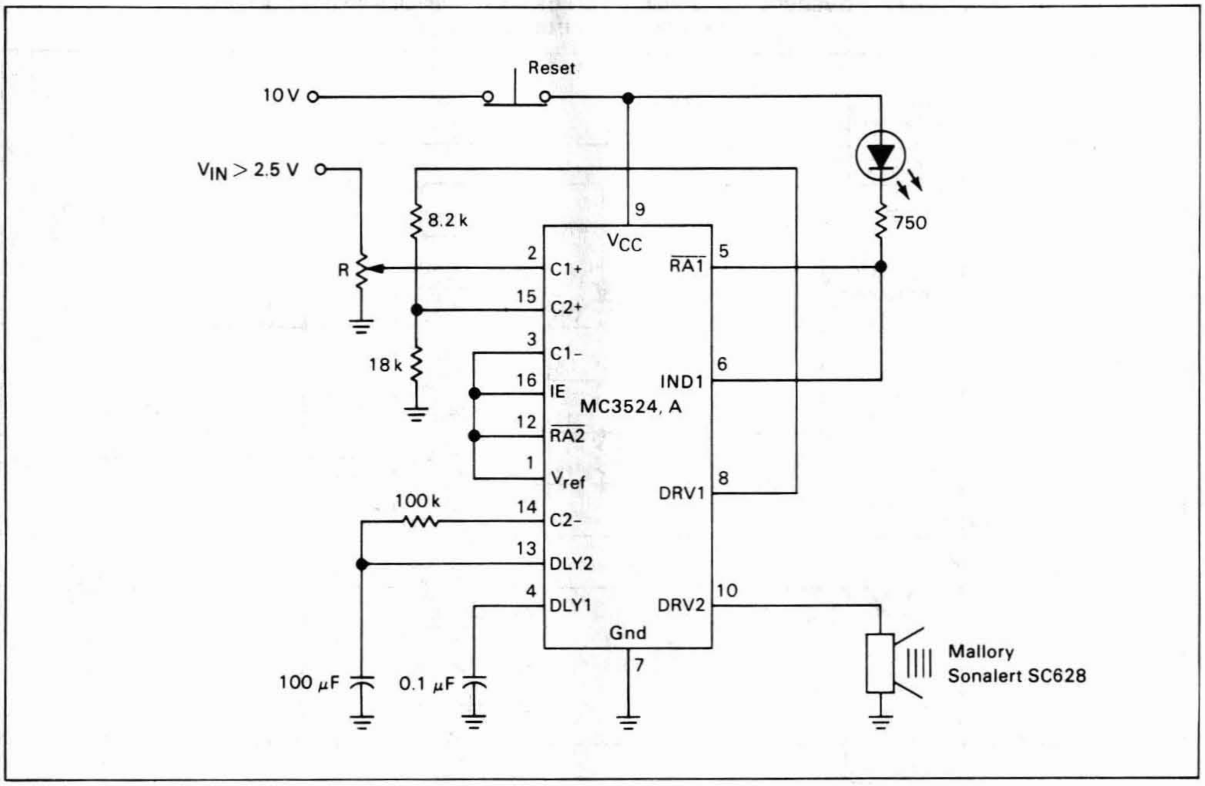
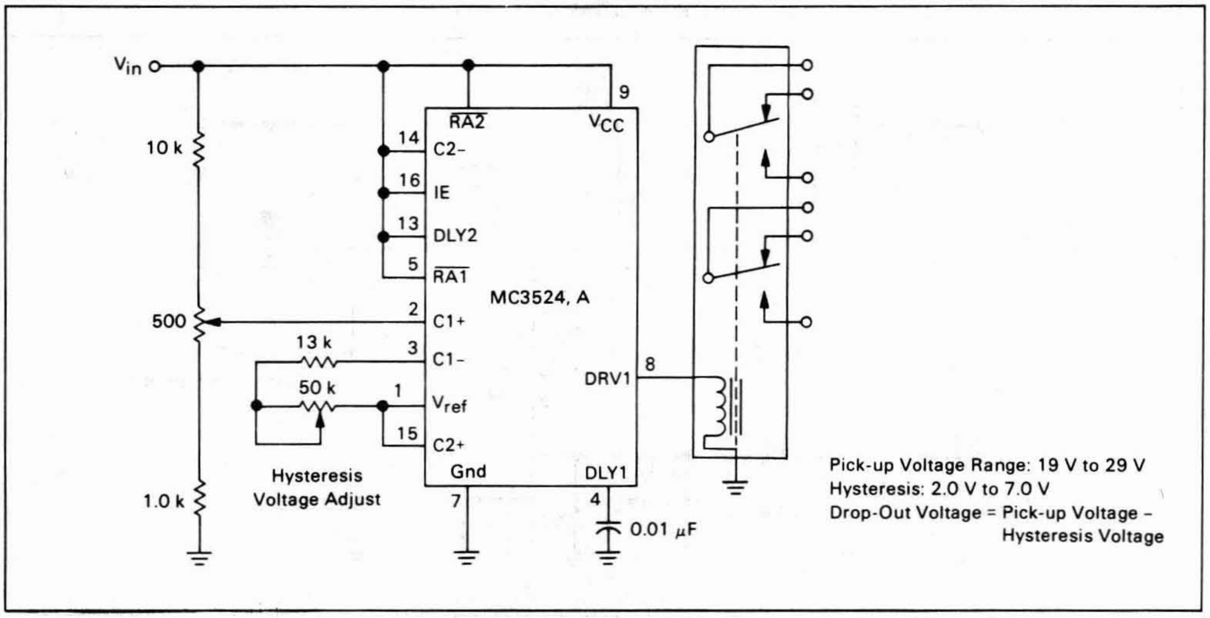
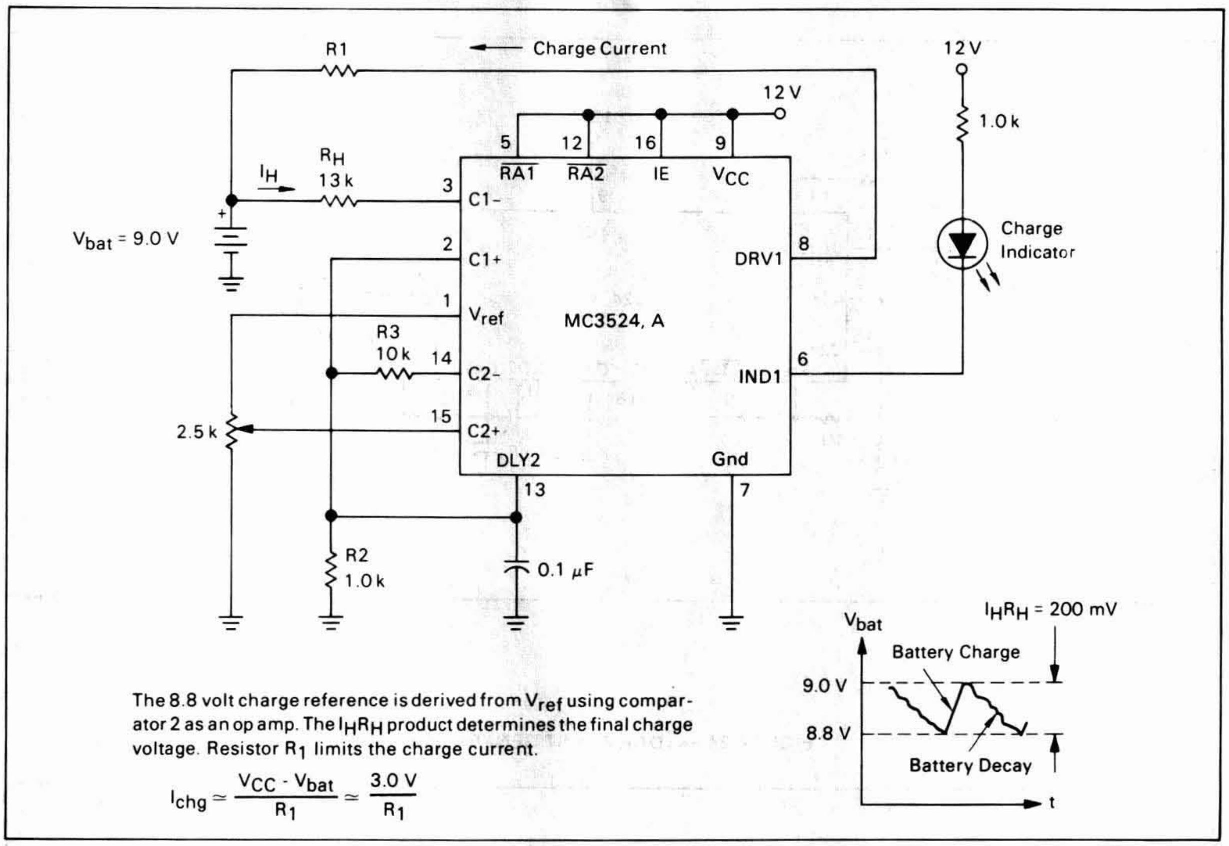

Reset
10 V
$V_{IN} > 2.5$ V
8.2 k
R
18 k
100 k
100 µF
0.1 µF
750
Mallory
Sonalert SC628
MC3524, A
9
$V_{CC}$
2 C1+
15 C2+
3 C1−
16 IE
12 $\overline{RA2}$
1 $V_{ref}$
14 C2−
13 DLY2
4 DLY1
5 $\overline{RA1}$
6 IND1
8 DRV1
10 DRV2
Gnd
7

FIGURE 20 — ADJUSTABLE D.C. PICK-UP/DROP-OUT RELAY CIRCUIT


$V_{in}$
10 k
500
1.0 k
13 k
50 k
Hysteresis
Voltage Adjust
MC3524, A
9
$\overline{RA2}$
$V_{CC}$
14 C2−
16 IE
13 DLY2
5 $\overline{RA1}$
2 C1+
3 C1−
1 $V_{ref}$
15 C2+
Gnd
7
DLY1
4
0.01 µF
8 DRV1

Pick-up Voltage Range: 19 V to 29 V
Hysteresis: 2.0 V to 7.0 V
Drop-Out Voltage = Pick-up Voltage − Hysteresis Voltage

FIGURE 21 — 9.0 V BATTERY CHARGER with ZERO SENSE LOAD CURRENT


R1
Charge Current
12 V
12 V
5
12
16
9
$\overline{RA1}$
$\overline{RA2}$
IE
$V_{CC}$
$I_H$
$R_H$
13 k
3
C1−
$V_{bat}$ = 9.0 V
+
2
C1+
DRV1
8
1.0 k
Charge Indicator
1
$V_{ref}$
MC3524, A
R3
10 k
14
C2−
IND1
6
2.5 k
15
C2+
DLY2
Gnd
13
7
R2
1.0 k
0.1 µF
$V_{bat}$
$I_HR_H$ = 200 mV
Battery Charge
9.0 V
8.8 V
Battery Decay
t

The 8.8 volt charge reference is derived from $V_{ref}$ using comparator 2 as an op amp. The $I_HR_H$ product determines the final charge voltage. Resistor $R_1$ limits the charge current.

$$I_{chg} \simeq \frac{V_{CC} - V_{bat}}{R_1} \simeq \frac{3.0\ V}{R_1}$$

FIGURE 22 — PROPORTIONAL CONTROL CIRCUIT

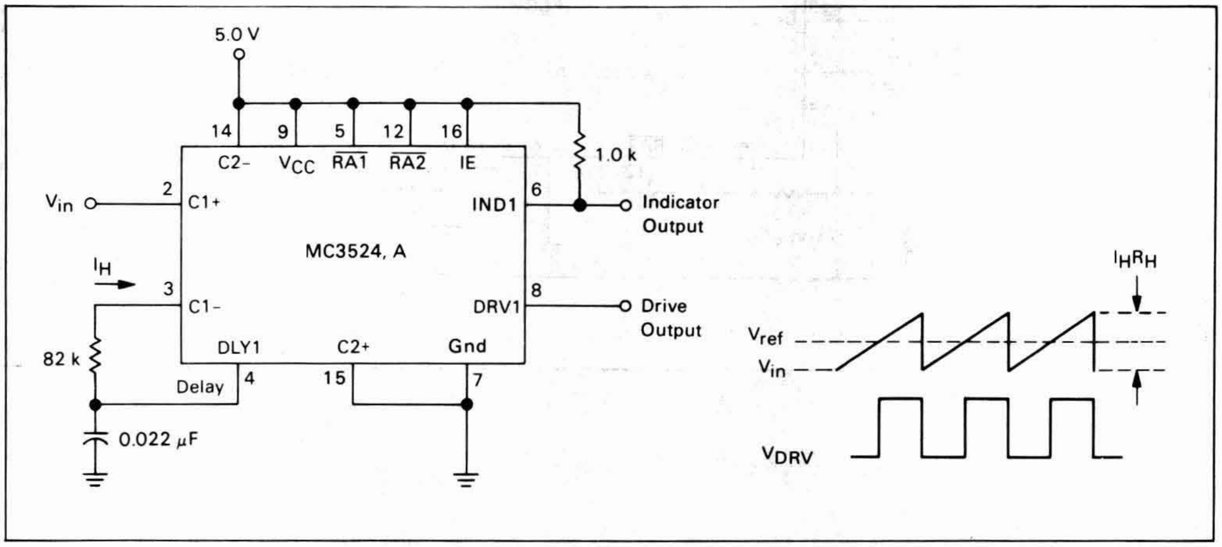

5.0 V
14
9
5
12
16
C2−
$V_{CC}$
$\overline{RA1}$
$\overline{RA2}$
IE
1.0 k
$V_{in}$
2
C1+
IND1
6
Indicator Output
MC3524, A
$I_H$
3
C1−
DRV1
8
Drive Output
82 k
DLY1
C2+
Gnd
Delay
4
15
7
0.022 µF
$I_HR_H$
$V_{ref}$
$V_{in}$
$V_{DRV}$

FIGURE 23 — ALTERNATING TWO TONE GENERATOR (EUROPEAN SIREN)

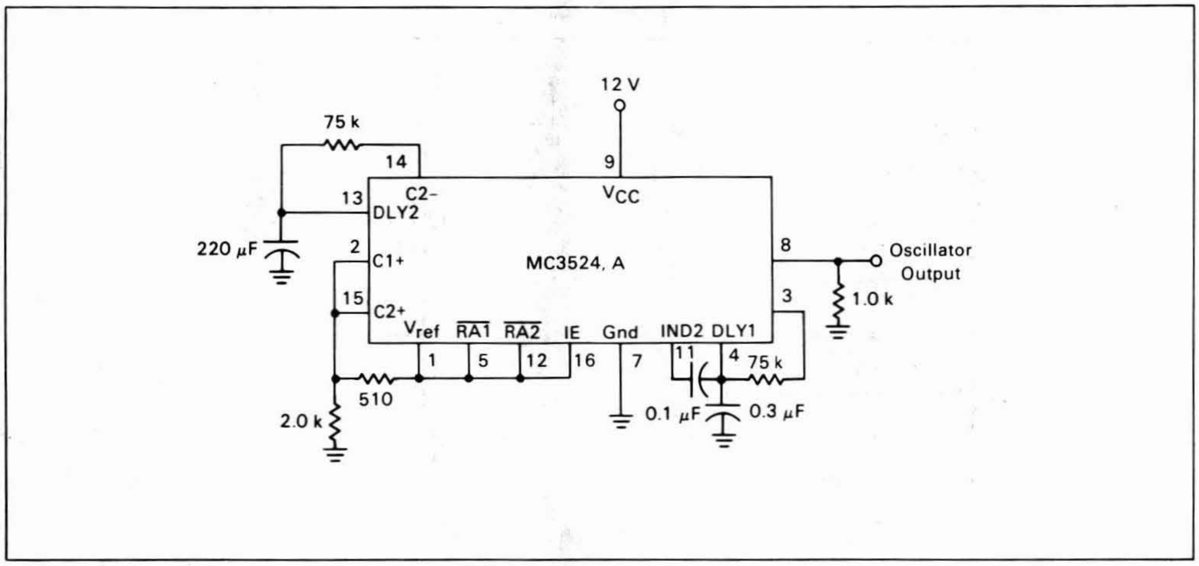

12 V
75 k
14
9
13
C2-
DLY2
VCC
220 μF
2
C1+
MC3524, A
8
Oscillator Output
15
C2+
3
1.0 k
Vref
RA1
RA2
IE
Gnd
IND2
DLY1
1
5
12
16
7
11
4
75 k
510
0.1 μF
0.3 μF
2.0 k

FIGURE 24 — TONE BURST GENERATOR

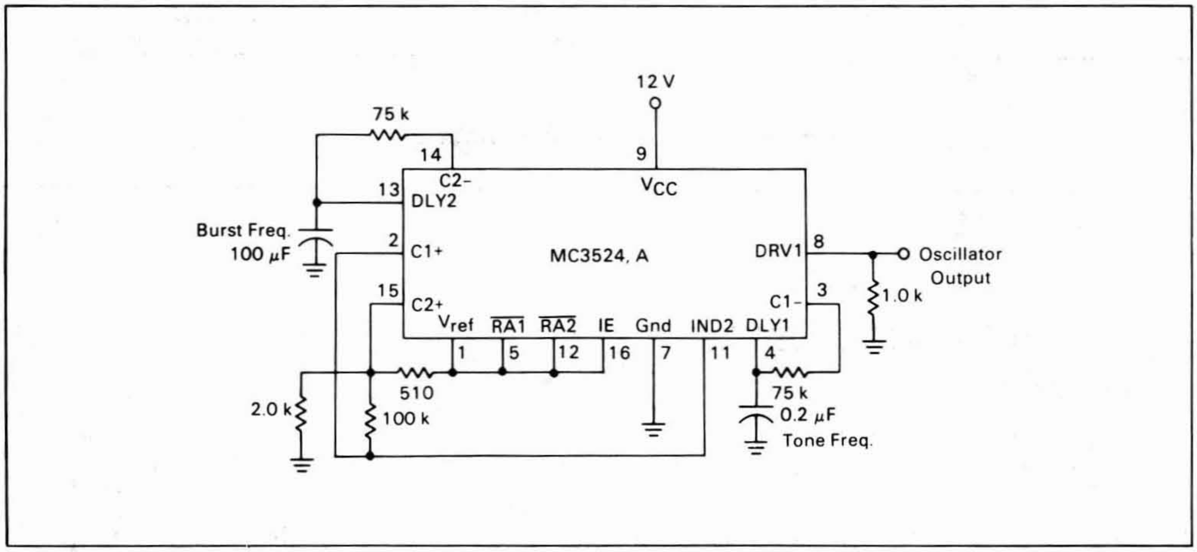

12 V
75 k
14
9
13
C2-
DLY2
VCC
Burst Freq.
100 μF
2
C1+
MC3524, A
DRV1
8
Oscillator Output
15
C2+
C1-
3
1.0 k
Vref
RA1
RA2
IE
Gnd
IND2
DLY1
1
5
12
16
7
11
4
510
75 k
2.0 k
100 k
0.2 μF
Tone Freq.

FIGURE 25 — PHOTOFLASH CONVERTER

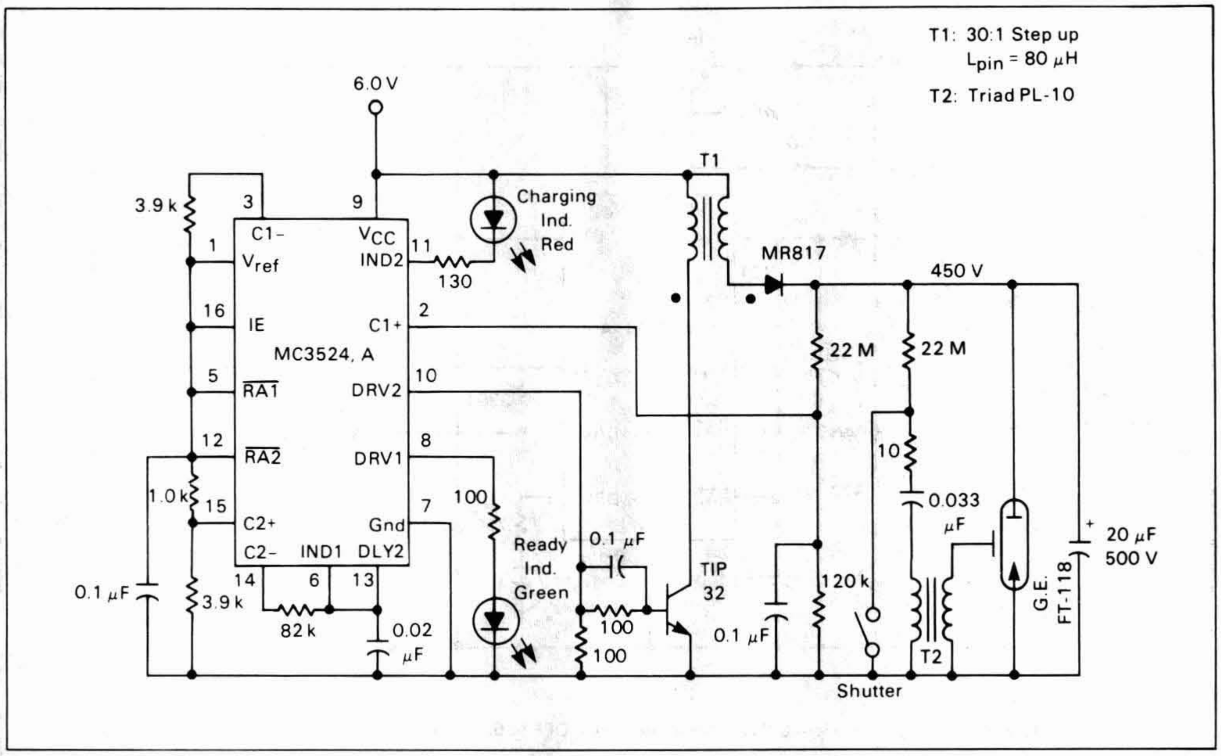
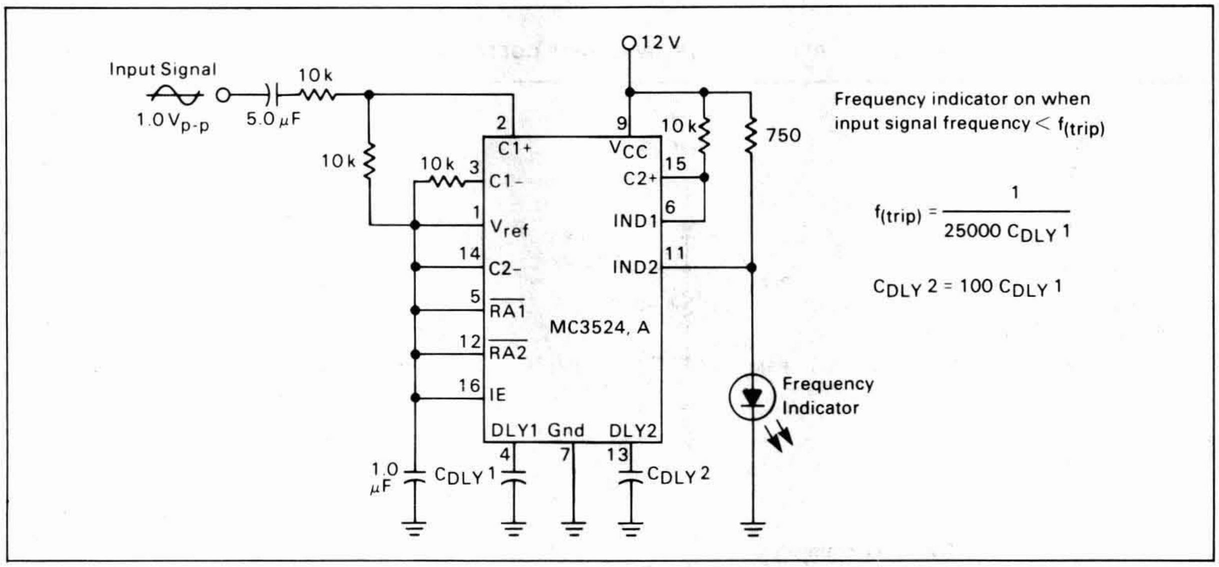

T1: 30:1 Step up
Lpin = 80 μH
T2: Triad PL-10
6.0 V
T1
3.9 k
3
9
C1−
VCC
1
Vref
11
IND2
130
Charging
Ind.
Red
MR817
450 V
16
IE
C1+
2
MC3524, A
5
RA1
DRV2
10
22 M
22 M
12
RA2
DRV1
8
10
1.0 k
15
C2+
Gnd
7
100
0.033
μF
C2−
IND1
DLY2
Ready
Ind.
Green
0.1 μF
14
6
13
TIP
32
120 k
0.1 μF
3.9 k
82 k
0.02
μF
100
100
0.1 μF
T2
Shutter
G.E.
FT-118
20 μF
500 V

FIGURE 26 — PROGRAMMABLE FREQUENCY SWITCH

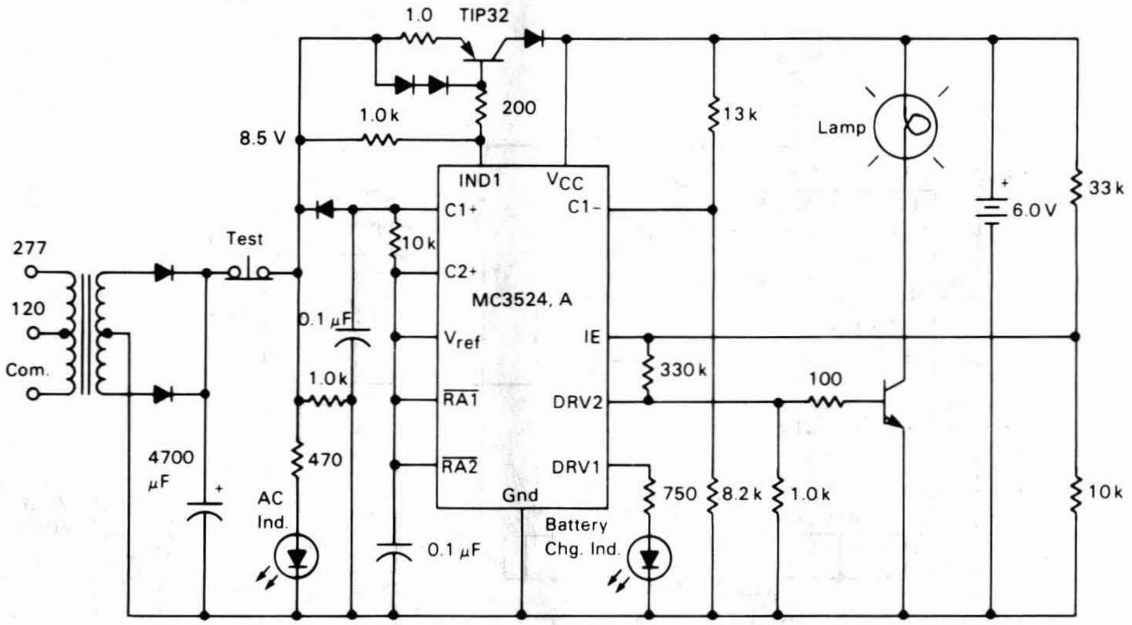

12 V
Input Signal
1.0 Vp-p
5.0 μF
10 k
10 k
10 k
3
C1+
2
9
VCC
10 k
750
15
C2+
C1−
1
Vref
IND1
6
14
C2−
IND2
11
5
RA1
MC3524, A
12
RA2
16
IE
Frequency
Indicator
DLY1
Gnd
DLY2
4
7
13
1.0
μF
CDLY 1
CDLY 2

Frequency indicator on when input signal frequency $< f_{(trip)}$

$$f_{(trip)} = \frac{1}{25000\ C_{DLY\ 1}}$$

$$C_{DLY\ 2} = 100\ C_{DLY\ 1}$$

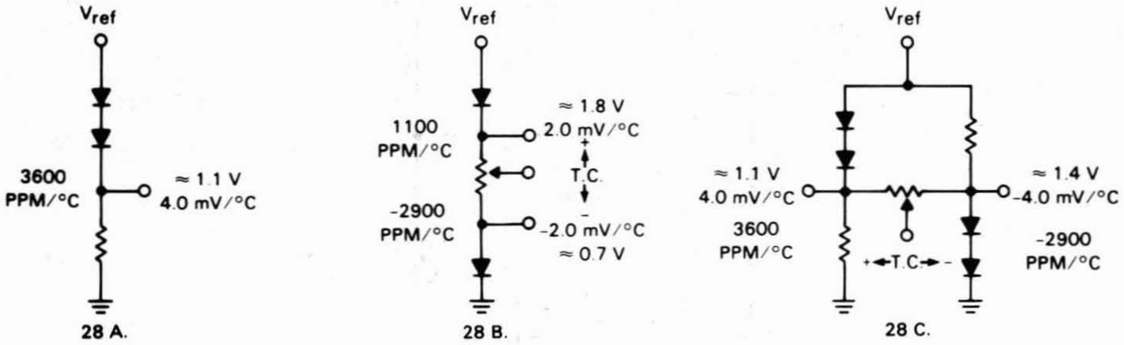
FIGURE 27 — EMERGENCY LIGHTING SYSTEM


1.0
TIP32
1.0 k
200
8.5 V
13 k
Lamp
IND1
VCC
C1+
C1−
33 k
6.0 V
277
Test
10 k
C2+
120
MC3524, A
0.1 µF
Vref
IE
Com.
1.0 k
330 k
100
RA1
DRV2
4700 µF
470
RA2
DRV1
AC Ind.
Gnd
750
8.2 k
1.0 k
10 k
Battery Chg. Ind.
0.1 µF

All diodes are 1N4001.

1. Battery charge current ≈ 0.6 A. Charger will cycle OFF at 6.6 V, ON at 6.4 V.
2. Lamp is ON with loss of ac and battery voltage ≥ 5.7 V. As battery discharges to < 5.3 V, lamp will turn OFF.

FIGURE 28 — REFERENCE TEMPERATURE COEFFICIENT MODIFICATIONS


Vref
3600 PPM/°C
≈ 1.1 V
4.0 mV/°C
Vref
≈ 1.8 V
1100 PPM/°C
2.0 mV/°C
+
T.C.
−
-2900 PPM/°C
-2.0 mV/°C
≈ 0.7 V
Vref
≈ 1.1 V
4.0 mV/°C
3600 PPM/°C
+ T.C. −
≈ 1.4 V
-4.0 mV/°C
-2900 PPM/°C

28 A.

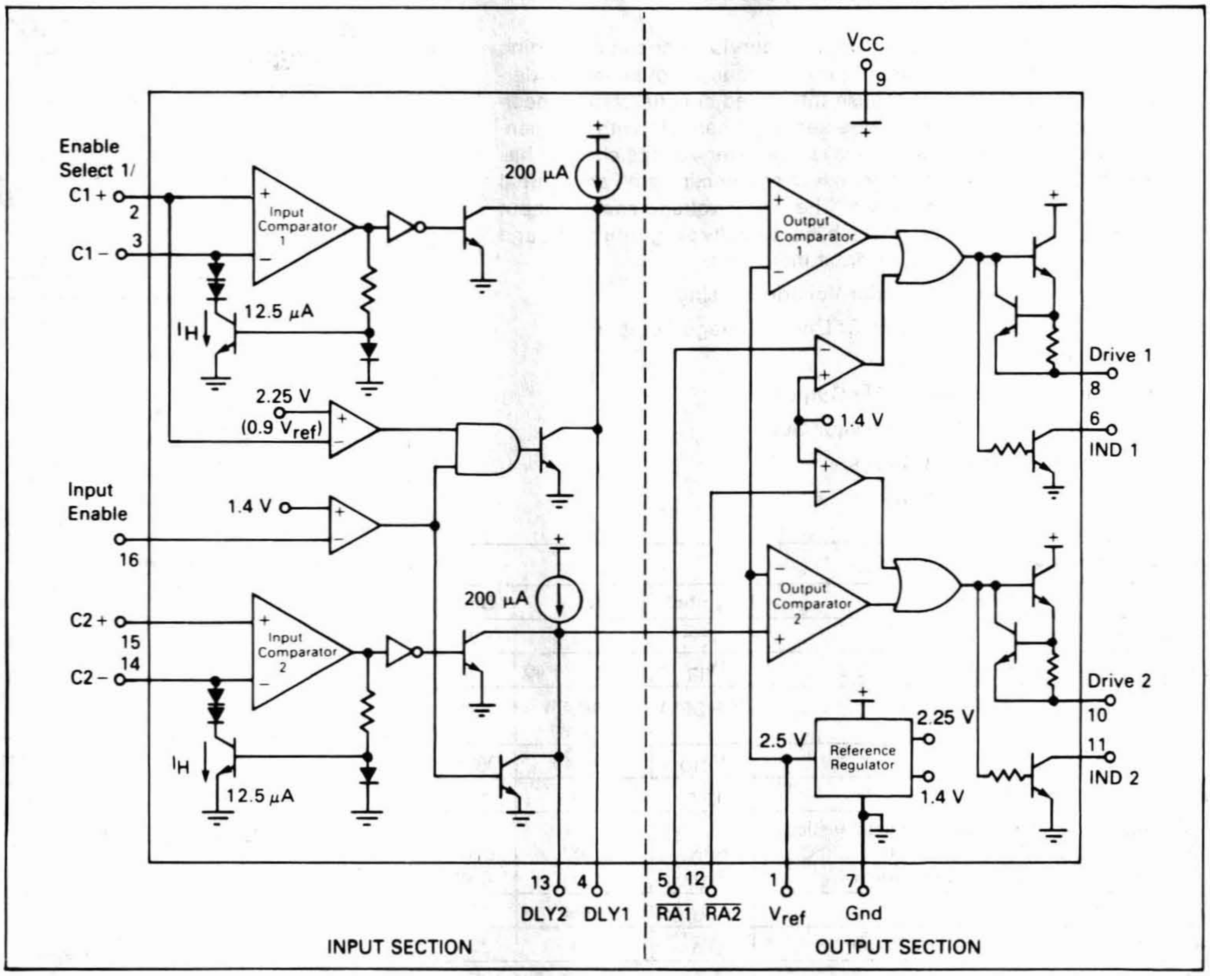
28 B.

28 C.

All diodes are 1N4001.

**28 A.** Fixed positive T.C.
**28 B.** Variable positive or negative T.C.
**28 C.** Variable positive or negative T.C. with almost constant voltage.

FIGURE 29 — MC3524/3424/3324 BLOCK DIAGRAM


VCC
9
Enable
Select 1/
C1 +
2
C1 −
3
Input Comparator 1
200 μA
12.5 μA
IH
2.25 V
(0.9 Vref)
Input
Enable
16
1.4 V
C2 +
15
14
C2 −
Input Comparator 2
200 μA
IH
12.5 μA
Output Comparator 1
1.4 V
Drive 1
8
6
IND 1
Output Comparator 2
Drive 2
10
2.25 V
2.5 V
Reference Regulator
1.4 V
11
IND 2
13
4
5
12
1
7
DLY2
DLY1
RA1
RA2
Vref
Gnd
INPUT SECTION
OUTPUT SECTION

Note: All voltages and currents are nominal.

**MOTOROLA**

# MC3425
# MC3425A

## POWER SUPPLY SUPERVISORY/OVER-UNDER-VOLTAGE PROTECTION CIRCUIT

The MC3425A is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. These integrated circuits contain dedicated over- and under-voltage sensing channels with independently programmable time delays. The over-voltage channel has a high current Drive Output for use in conjunction with an external SCR "Crowbar" for shutdown. The under-voltage channel input comparator has hysteresis which is externally programmable, and an open-collector output for fault indication.

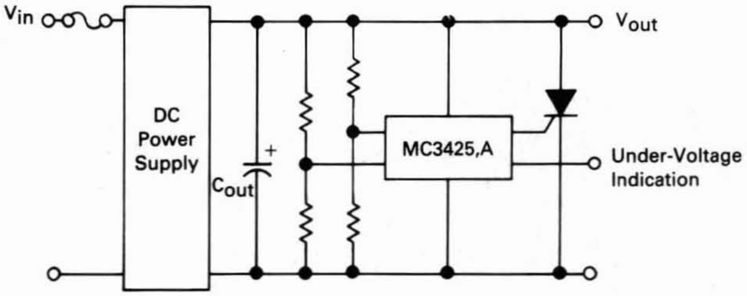
- Dedicated Over- And Under-Voltage Sensing
- Programmable Hysteresis Of Under-Voltage Comparator
- Internal 2.5 V Reference
- 300 mA Over-Voltage Drive Output
- 30 mA Under-Voltage Indicator Output
- Programmable Time Delays
- 4.5 V to 40 V Operation

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 40 | Vdc |
| Comparator Input Voltage Range (Note 2) | $V_{IR}$ | −0.3 to +40 | Vdc |
| Drive Output Short-Circuit Current | $I_{OS(DRV)}$ | Internally Limited | mA |
| Indicator Output Voltage | $V_{IND}$ | 0 to 40 | Vdc |
| Indicator Output Sink Current | $I_{IND}$ | 30 | mA |
| Power Dissipation and Thermal Characteristics | | | |
| Maximum Power Dissipation @ $T_A = 70°C$ | $P_D$ | 1000 | mW |
| Thermal Resistance Junction to Air | $R_{\theta JA}$ | 80 | °C/W |
| Operating Junction Temperature | $T_J$ | +150 | °C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

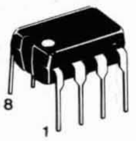
### TYPICAL APPLICATION

Over-Voltage Crowbar Protection, Under-Voltage Indication



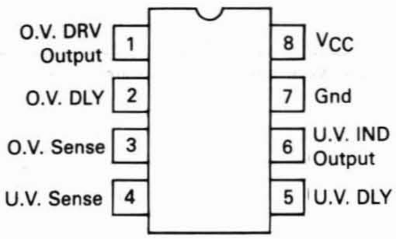
## POWER SUPPLY SUPERVISORY/ OVER-UNDER-VOLTAGE PROTECTION CIRCUIT

### SILICON MONOLITHIC INTEGRATED CIRCUIT



**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC3425P1,AP1 | 0 to +70°C | Plastic DIP |

**ELECTRICAL CHARACTERISTICS** (4.5 V≤$V_{CC}$≤40 V; $T_A$ = $T_{low}$ to $T_{high}$ [see Note 1] unless otherwise specified.)

| Characteristic | Symbol | MC3425A Min | MC3425A Typ | MC3425A Max | MC3425 Min | MC3425 Typ | MC3425 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| **REFERENCE SECTION** | | | | | | | | |
| Sense Trip Voltage (Reference Voltage)<br>$V_{CC}$ = 15 V | $V_{Sense}$ | | | | | | | Vdc |
| $T_A$ = 25°C | | 2.475 | 2.5 | 2.525 | 2.4 | 2.5 | 2.6 | |
| $T_{low}$ to $T_{high}$ (Note 1) | | 2.45 | 2.5 | 2.55 | 2.33 | 2.5 | 2.63 | |
| Line Regulation of $V_{Sense}$<br>4.5 V ≤ $V_{CC}$ ≤ 40 V; $T_J$ = 25°C | $Reg_{line}$ | — | 7.0 | 15 | — | 7.0 | 15 | mV |
| Power Supply Voltage Operating Range | $V_{CC}$ | 4.5 | — | 40 | 4.5 | — | 40 | Vdc |
| Power Supply Current<br>$V_{CC}$ = 40 V; $T_A$ = 25°C; No Output Loads<br>O.V. Sense (Pin 3) = 0 V;<br>U.V. Sense (Pin 4) = $V_{CC}$ | $I_{CC(off)}$ | — | 8.5 | 10 | — | 8.5 | 10 | mA |
| O.V. Sense (Pin 3) = $V_{CC}$;<br>U.V. Sense (Pin 4) = 0 V | $I_{CC(on)}$ | — | 16.5 | 19 | — | 16.5 | 19 | mA |
| **INPUT SECTION** | | | | | | | | |
| Input Bias Current, O.V. and U.V. Sense | $I_{IB}$ | — | 1.0 | 2.0 | — | 1.0 | 2.0 | μA |
| Hysteresis Activation Voltage, U.V. Sense<br>$V_{CC}$ = 15 V; $T_A$ = 25°C; | $V_{H(act)}$ | | | | | | | V |
| $I_H$ = 10% | | — | 0.6 | — | — | 0.6 | — | |
| $I_H$ = 90% | | — | 0.8 | — | — | 0.8 | — | |
| Hysteresis Current, U.V. Sense<br>$V_{CC}$ = 15 V; $T_A$ = 25°C;<br>U.V. Sense (Pin 4) = 2.5 V | $I_H$ | 10 | 12.5 | 15 | 9.0 | 12.5 | 16 | μA |
| Delay Pin Voltage ($I_{DLY}$ = 0 mA) | | | | | | | | V |
| Low State | $V_{OL(DLY)}$ | — | 0.2 | 0.5 | — | 0.2 | 0.5 | |
| High State | $V_{OH(DLY)}$ | $V_{CC}$−0.5 | $V_{CC}$−0.15 | — | $V_{CC}$−0.5 | $V_{CC}$−0.15 | — | |
| Delay Pin Source Current<br>$V_{CC}$ = 15 V; $V_{DLY}$ = 0 V | $I_{DLY(source)}$ | 150 | 200 | 250 | 140 | 200 | 260 | μA |
| Delay Pin Sink Current<br>$V_{CC}$ = 15 V; $V_{DLY}$ = 2.5 V | $I_{DLY(sink)}$ | 1.8 | 3.0 | — | 1.8 | 3.0 | — | mA |
| **OUTPUT SECTION** | | | | | | | | |
| Drive Output Peak Current ($T_A$ = 25°C) | $I_{DRV(peak)}$ | 200 | 300 | — | 200 | 300 | — | mA |
| Drive Output Voltage<br>$I_{DRV}$ = 100 mA; $T_A$ = 25°C | $V_{OH(DRV)}$ | $V_{CC}$−2.5 | $V_{CC}$−2.0 | — | $V_{CC}$−2.5 | $V_{CC}$−2.0 | — | V |
| Drive Output Leakage Current<br>$V_{DRV}$ = 0 V | $I_{DRV(leak)}$ | — | 15 | 200 | — | 15 | 200 | nA |
| Drive Output Current Slew Rate ($T_A$ = 25°C) | di/dt | — | 2.0 | — | — | 2.0 | — | A/μs |
| Drive Output $V_{CC}$ Transient Rejection<br>$V_{CC}$ = 0 V to 15 V at dV/dt = 200 V/μs;<br>O.V. Sense (Pin 3) = 0 V; $T_A$ = 25°C | $I_{DRV(trans)}$ | — | 1.0 | — | — | 1.0 | — | mA<br>(Peak) |
| Indicator Output Saturation Voltage<br>$I_{IND}$ = 30 mA; $T_A$ = 25°C | $V_{IND(sat)}$ | — | 560 | 800 | — | 560 | 800 | mV |
| Indicator Output Leakage Current<br>$V_{OH(IND)}$ = 40 V | $I_{IND(leak)}$ | — | 25 | 200 | — | 25 | 200 | nA |
| Output Comparator Threshold Voltage<br>(Note 3) | $V_{th(OC)}$ | 2.45 | 2.5 | 2.55 | 2.33 | 2.5 | 2.63 | V |
| Propagation Delay Time<br>($V_{CC}$ = 15 V; $T_A$ = 25°C)<br>Input to Drive Output or Indicator Output<br>100 mV Overdrive, $C_{DLY}$ = 0 μF | $t_{PLH(IN/OUT)}$ | — | 1.7 | — | — | 1.7 | — | μs |
| Input to Delay<br>2.5 V Overdrive (0 V to 5.0 V Step) | $t_{PLH(IN/DLY)}$ | — | 700 | — | — | 700 | — | ns |

NOTES:
(1) $T_{low}$ = 0°C  $T_{high}$ = +70°C
(2) The input signal voltage should nto be allowed to go negative by more than 300 mV or positive by more than 40 V, independent of $V_{CC}$, without device destruction.
(3) The $V_{th(OC)}$ limits are approximately the $V_{Sense}$ limits over the applicable temperature range.

FIGURE 1 — HYSTERESIS CURRENT versus HYSTERESIS ACTIVATION VOLTAGE

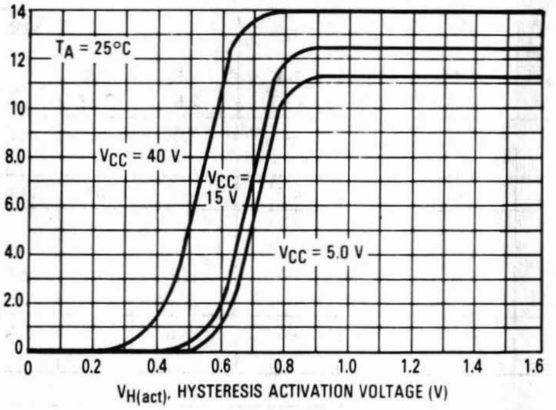


FIGURE 2 — HYSTERESIS ACTIVATION VOLTAGE versus TEMPERATURE

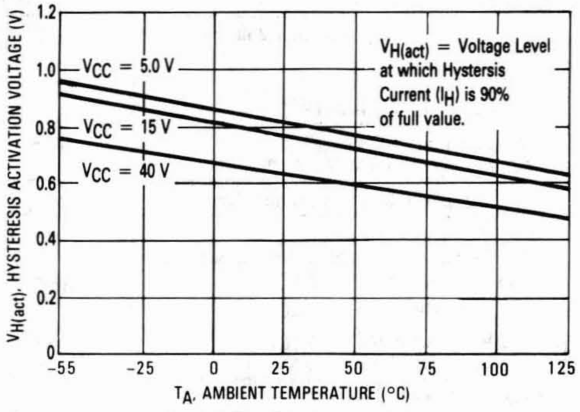


FIGURE 3 — HYSTERESIS CURRENT versus TEMPERATURE

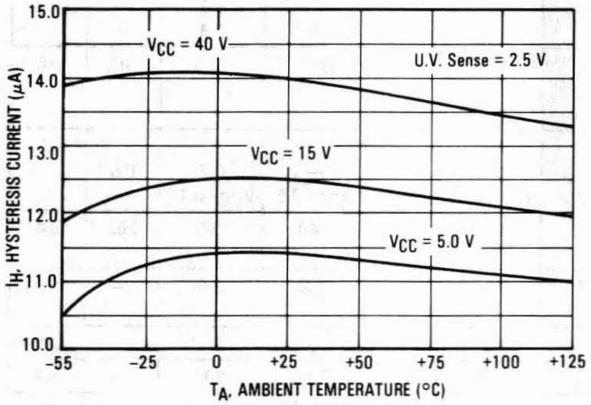


FIGURE 4 — SENSE TRIP VOLTAGE CHANGE versus TEMPERATURE

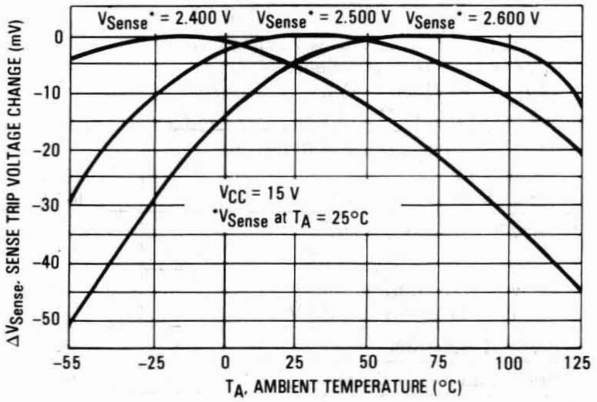


FIGURE 5 — OUTPUT DELAY TIME versus DELAY CAPACITANCE

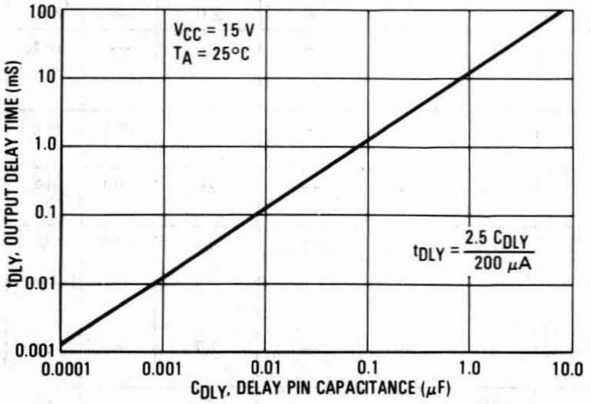


FIGURE 6 — DELAY PIN SOURCE CURRENT versus TEMPERATURE

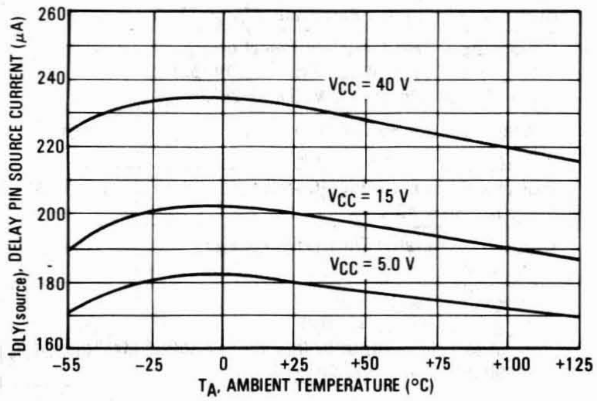


FIGURE 7 — DRIVE OUTPUT SATURATION VOLTAGE versus OUTPUT PEAK CURRENT

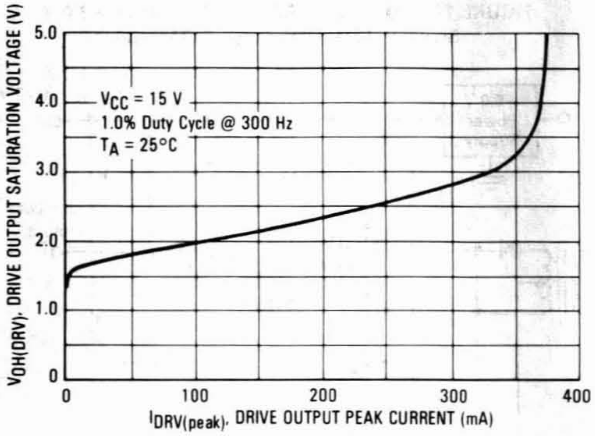


FIGURE 8 — INDICATOR OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

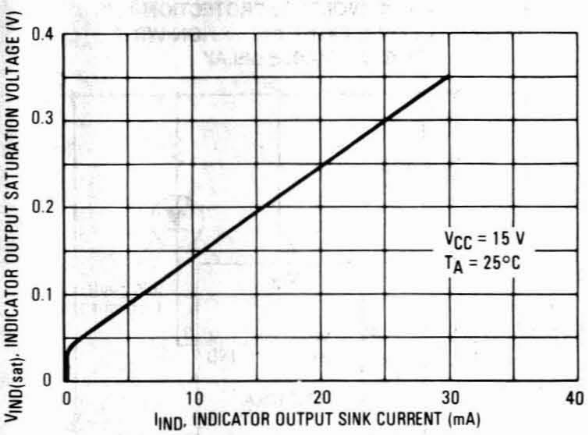


FIGURE 9 — DRIVE OUTPUT SATURATION VOLTAGE versus TEMPERATURE

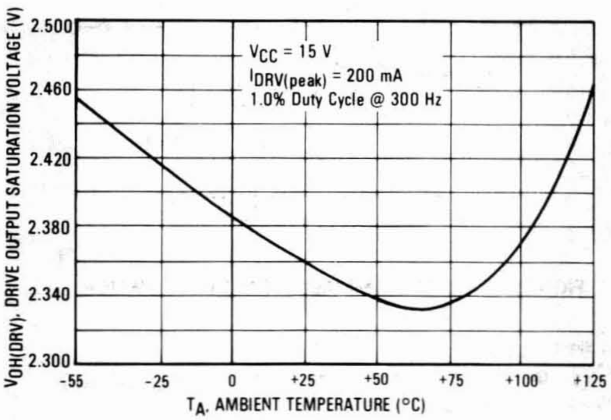
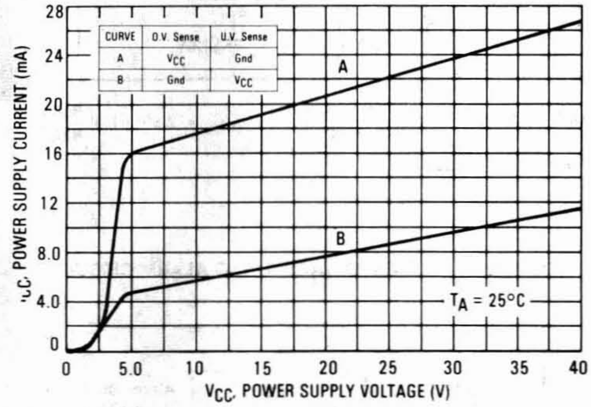
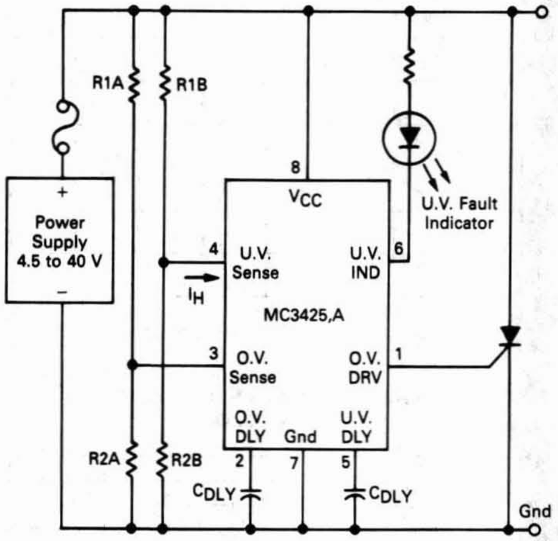


FIGURE 10 — POWER SUPPLY CURRENT versus VOLTAGE



## APPLICATIONS INFORMATION

FIGURE 11 — OVERVOLTAGE PROTECTION AND UNDER VOLTAGE FAULT INDICATION WITH PROGRAMMABLE DELAY

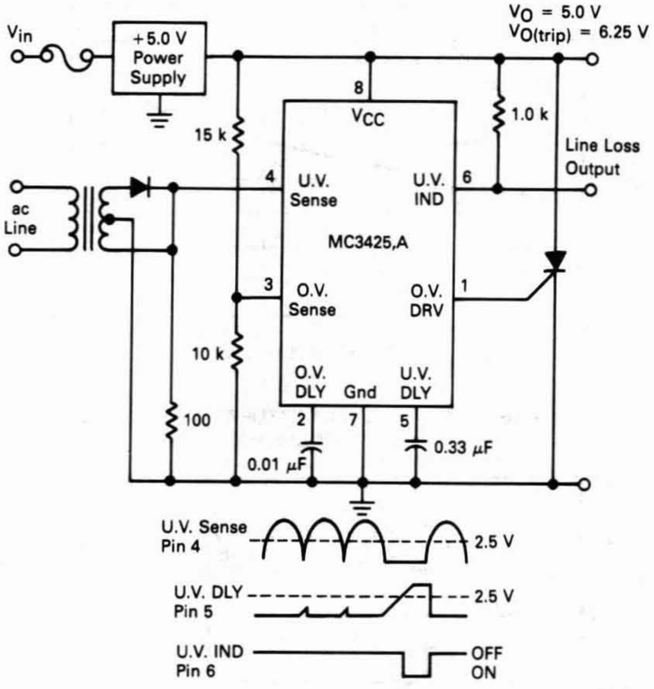


+Vo
R1A
R1B
+
Power Supply 4.5 to 40 V
−
8
VCC
U.V. Fault Indicator
4
U.V. Sense
U.V. IND
6
IH
MC3425,A
3
O.V. Sense
O.V. DRV
1
O.V. DLY
Gnd
U.V. DLY
R2A
R2B
2
7
5
CDLY
CDLY
Gnd

$$\text{U.V. Hysteresis} = I_H\left(\frac{R1B\ R2B}{R1B + R2B}\right) \qquad V_{O(trip)} = 2.5\ V\left(1 + \frac{R1A}{R2A}\right)$$

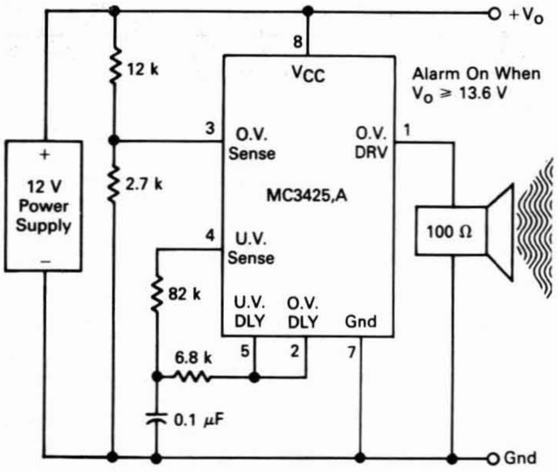
$$t_{DLY} = 12500\ C_{DLY}$$

FIGURE 12 — OVERVOLTAGE PROTECTION OF 5.0 V SUPPLY WITH LINE LOSS DETECTOR



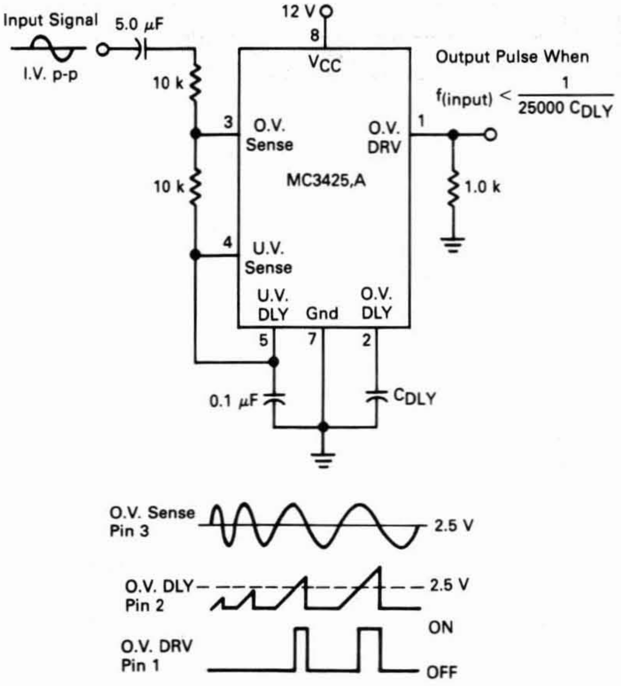
Vin
+5.0 V Power Supply
VO = 5.0 V
VO(trip) = 6.25 V
8
VCC
1.0 k
15 k
Line Loss Output
4
U.V. Sense
U.V. IND
6
ac Line
MC3425,A
3
O.V. Sense
O.V. DRV
1
10 k
O.V. DLY
Gnd
U.V. DLY
100
2
7
5
0.33 μF
0.01 μF
U.V. Sense Pin 4
2.5 V
U.V. DLY Pin 5
2.5 V
U.V. IND Pin 6
OFF
ON

FIGURE 13 — OVERVOLTAGE AUDIO ALARM CIRCUIT



+Vo
8
12 k
VCC
Alarm On When Vo ≥ 13.6 V
3
O.V. Sense
O.V. DRV
1
+
12 V Power Supply
−
2.7 k
MC3425,A
100 Ω
4
U.V. Sense
82 k
U.V. DLY
O.V. DLY
Gnd
6.8 k
5
2
7
0.1 μF
Gnd

FIGURE 14 — PROGRAMMABLE FREQUENCY SWITCH



Input Signal
1.V. p-p
5.0 μF
12 V
8
VCC
Output Pulse When
f(input) < 1/(25000 CDLY)
10 k
3
O.V. Sense
O.V. DRV
1
10 k
MC3425,A
1.0 k
4
U.V. Sense
U.V. DLY
Gnd
O.V. DLY
5
7
2
0.1 μF
CDLY
O.V. Sense Pin 3
2.5 V
O.V. DLY Pin 2
2.5 V
O.V. DRV Pin 1
ON
OFF

## CIRCUIT DESCRIPTION

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. The block diagram is shown below in Figure 15. The Over-Voltage (O.V.) and Under-Voltage (U.V.) Input Comparators are both referenced to an internal 2.5 V regulator. The U.V. Input Comparator has a feedback activated 12.5 μA current sink ($I_H$) which is used for programming the input hysteresis voltage ($V_H$). The source resistance feeding this input ($R_H$) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6} R_H$.

Separate Delay pins (O.V. DLY, U.V. DLY) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 μA when the non-inverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time ($t_{DLY}$) for the Drive and Indicator outputs. The Delay pins are internally connected to the non-inverting inputs of the O.V. and U.V. Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time ($t_{DLY}$) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor ($C_{DLY}$) to 2.5 volts.

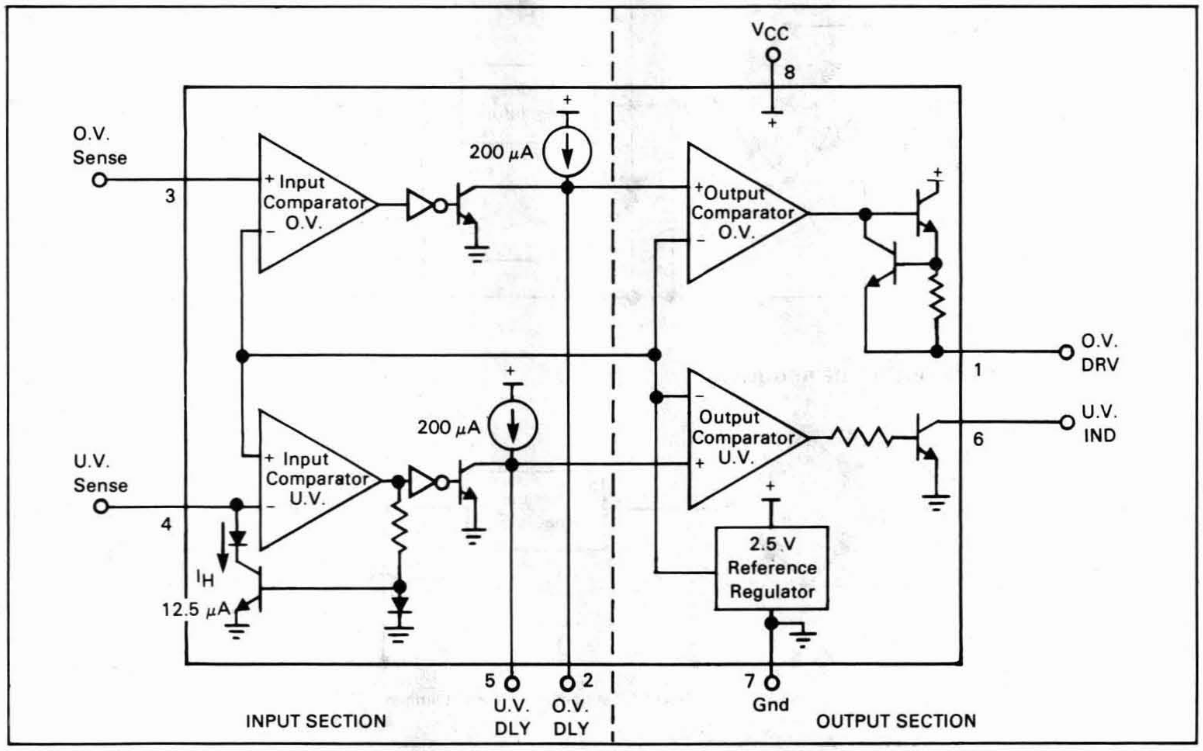
$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{2.5\, C_{DLY}}{200\ \mu A} = 12500\, C_{DLY}$$

Figure 5 provides $C_{DLY}$ values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's non-inverting input is less than the inverting input. The sink current, $I_{DLY(sink)}$, capability of the Delay pins is ≥ 1.8 mA and is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

The Over-Voltage Drive Output is a current-limited emitter-follower capable of sourcing 300 mA at a turn-on slew rate of 2.0 A/μs, ideal for driving "Crowbar" SCR's. The Under-Voltage Indicator Output is an open-collector, NPN transistor, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or shut-down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of ±4.0% for the basic devices and ±1.0% for the A-suffix device types at 25°C. The reference has a typical temperature coefficient of 30 ppm/°C for A-suffix devices.

**FIGURE 15 — BLOCK DIAGRAM**


$V_{CC}$
8
O.V. Sense
3
+ Input Comparator − O.V.
200 μA
+ Output Comparator − O.V.
O.V. DRV
1
− Output Comparator + U.V.
U.V. IND
6
U.V. Sense
4
+ Input Comparator − U.V.
200 μA
$I_H$
12.5 μA
2.5 V Reference Regulator
5
U.V. DLY
2
O.V. DLY
7
Gnd
INPUT SECTION
OUTPUT SECTION

Note: All voltages and currents are nominal.

## CROWBAR SCR CONSIDERATIONS

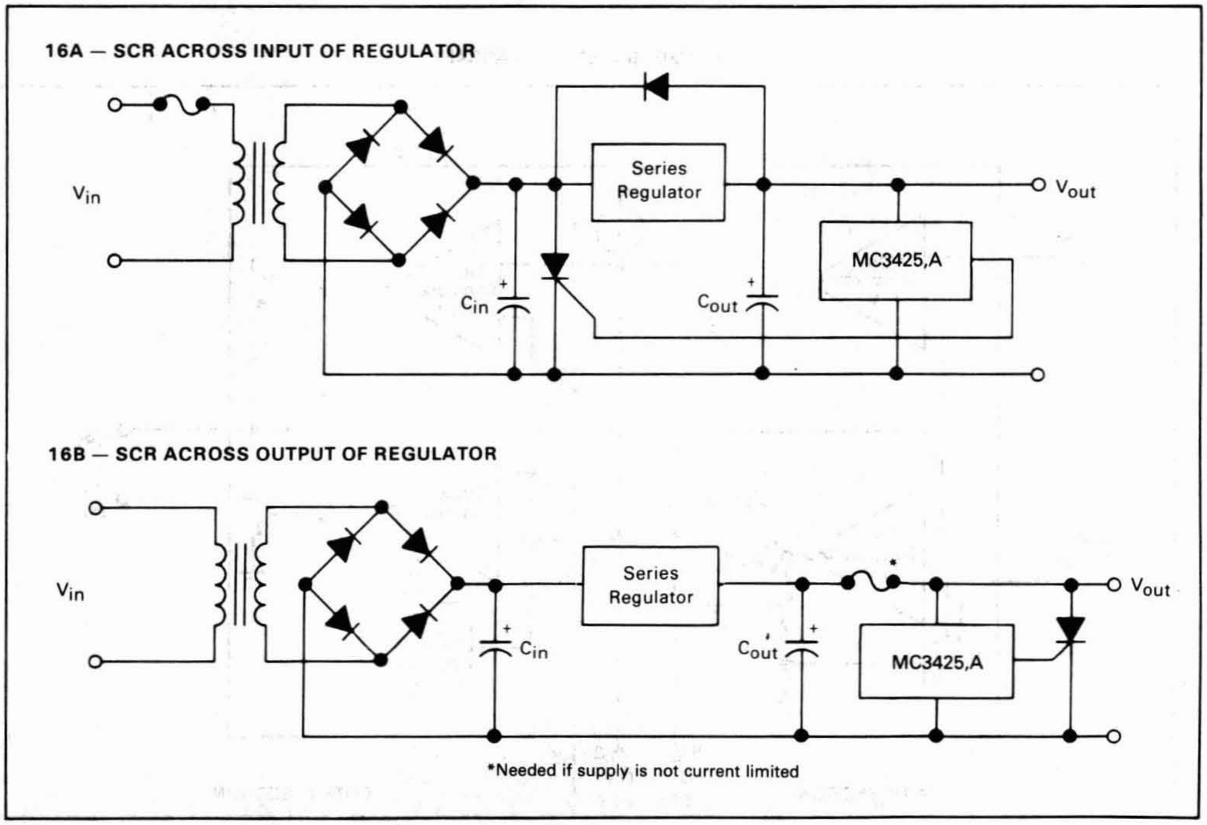
Referring to Figure 16, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, $C_{out}$. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 16A, the supply's input filter capacitors. This surge current is illustrated in Figure 17, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or $I^2t$. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

### 1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

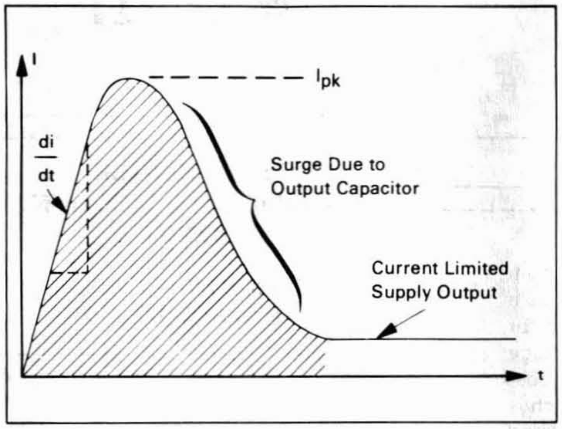
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times $I_{GT}$) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times $I_{GT}$ and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 18. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 16 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS



*Needed if supply is not current limited

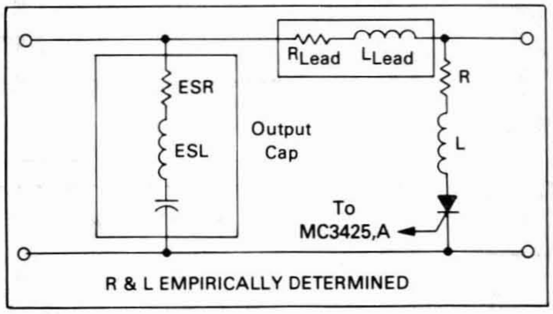
FIGURE 17 — CROWBAR SCR SURGE CURRENT WAVEFORM



**2. Surge Current**

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 18) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 18 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



## A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 16A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an $I^2t$ rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 16B.

## CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

| DEVICE | $I_{RMS}$ | $I_{FSM}$ | PACKAGE |
|---|---|---|---|
| MCR67 Series | 12 A | 100 A | Metal Stud |
| MCR68 Series | 12 A | 100 A | TO-220 Plastic |
| 2N1842 Series | 16 A | 125 A | Metal Stud |
| 2N6400 Series | 16 A | 160 A | TO-220 Plastic |
| 2N6504 Series | 25 A | 160 A | TO-220 Plastic |
| 2N681 Series | 25 A | 200 A | Metal Stud |
| 2N2573 Series | 25 A | 260 A | TO-3 Metal Can |
| MCR69 Series | 25 A | 300 A | TO-220 Plastic |
| MCR70 Series | 35 A | 350 A | Metal Stud |
| MCR71 Series | 55 A | 550 A | Metal Stud |

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

**MOTOROLA**

# MC33031T

## SERIES SWITCH TRANSIENT PROTECTION CIRCUIT

### SILICON MONOLITHIC INTEGRATED CIRCUIT

## Product Preview

The MC33031 is a Series Switch Transient Protection Circuit. Under normal operating voltage conditions, the device acts as a saturated series pass element with a very low voltage drop for load currents in excess of 750 mA. In the event of an over voltage condition (≥31 V typically) or high voltage transient of either positive or negative polarity, the MC33031 instantaneously switches to an open circuit (OFF) state, interrupting power to the load and protecting the load during this potentially destructive condition. The device will immediately recover to an ON state when supply voltages fall within the normal operating range.

The MC33031 is fabricated on a power BIMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.

The device operates in its ON state over a wide power supply voltage range of 4.5 V to 31 V and can withstand voltage transients (positive or negative) of ± 100 V. A rugged PNP output stage along with active clamp circuitry, current limit and thermal shutdown permits driving of all types of loads including inductive. The MC33031 is specified over a wide junction temperature of − 40°C to + 125°C and is ideally suited for industrial and automotive applications where harsh environments exist.

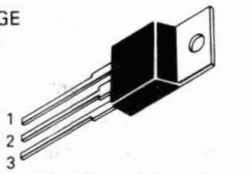
- Transient Protection Up to ± 100 V
- Load Currents in Excess of 750 mA
- Low Switch Voltage Drop
- Low Quiescent Current
- Fast Shutdown and Recovery Response to Transients
- On-Chip Current Limit and Thermal Shutdown Circuitry
- Capacitor May Be Used to Support Load During Transient

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage — Continuous | $V_{in}$ | + 55<br>− 12 | Vdc |
| Input Voltage — Transient<br>t = 100 ms<br>t = 1.0 ms | $V_{in(t)}$ | <br>± 60<br>± 100 | V |
| Output Current | $I_O$ | Internally Limited | A |
| Power Dissipation and Thermal Characteristics<br>$T_A$ = + 25°C<br>Derate above $T_A$ = + 25°C<br>Thermal Resistance Junction to Ambient<br>$T_C$ = + 25°C<br>Derate above $T_C$ = + 25°C<br>Thermal Resistance Junction to Case | <br>$P_D$<br>$1/\theta_{JA}$<br>$\theta_{JA}$<br>$P_D$<br>$1/\theta_{JA}$<br>$\theta_{JA}$ | <br>2.0<br>16<br>62.5<br>25<br>200<br>5.0 | <br>Watts<br>mW/°C<br>°C/W<br>Watts<br>mW/°C<br>°C/W |
| Operating Junction Temperature Range | $T_J$ | − 40 to + 125 | °C |
| Storage Temperature Range | $T_{stg}$ | − 65 to + 150 | °C |

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

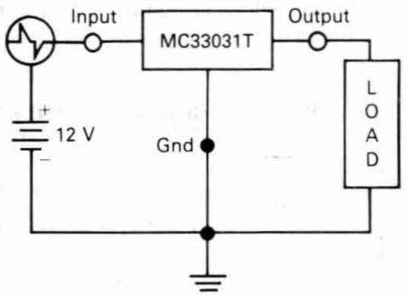
**T SUFFIX**
PLASTIC PACKAGE
CASE 221A-03
TO-220AB



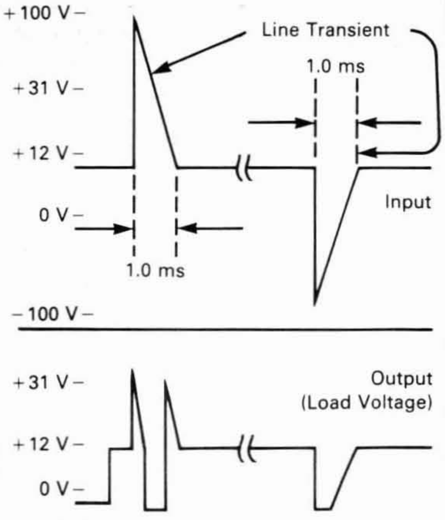
Pin 1. Input
2. Ground
3. Output

(Heatsink surface connected to Pin 2)

**BLOCK DIAGRAM**



**TIMING DIAGRAM**

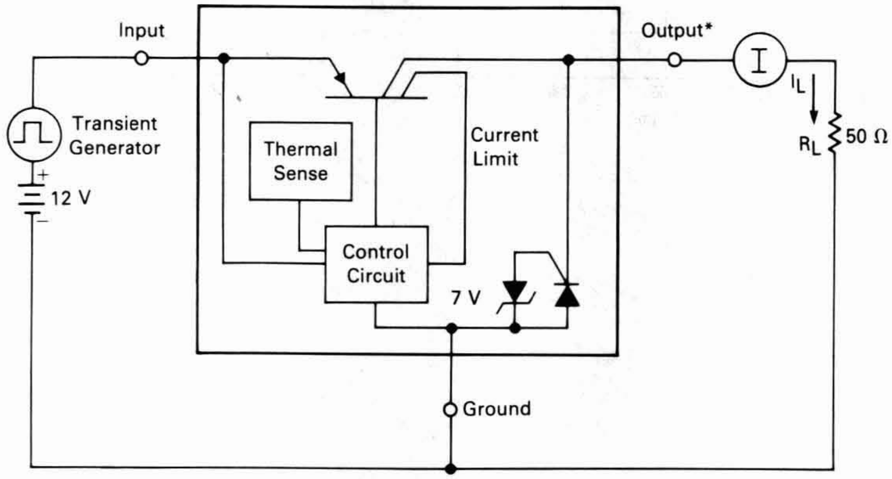


**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = +12 V, $I_L$ = 150 mA, −40°C ≤ $T_J$ ≤ +125°C unless noted)*

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Minimum Operating Voltage | $V_{in(min)}$ | — | 2.5 | 4.5 | V |
| Quiescent Current<br>$I_L$ = 150 mA, $V_{in}$ = +4.5 V<br>$I_L$ = 500 mA, $V_{in}$ = +12 V<br>$I_L$ = 750 mA, $V_{in}$ = +24 V | $I_B$ | <br>—<br>—<br>— | <br>3.0<br>8.0<br>15 | <br>10<br>15<br>75 | mA |
| Switch Voltage Drop<br>$I_L$ = 150 mA, $V_{in}$ = +4.5 V<br>$I_L$ = 500 mA, $V_{in}$ = +12 V<br>$I_L$ = 750 mA, $V_{in}$ = +24 V | $V_{in}-V_O$ | <br>—<br>—<br>— | <br>125<br>300<br>425 | <br>200<br>500<br>750 | mV |
| Output Current Limit<br>$V_O$ = 0 V | $I_{SC}$ | 0.8 | 1.5 | 2.5 | A |
| Output Leakage Current<br>36 V < $V_{in}$ ≤ 55 V, $V_O$ = 0 V | $I_{Leak}$ | — | 10 | — | mA |
| Over Voltage Shutdown Threshold<br>$I_L$ ≤ 100 μA | $V_{in(OV)}$ | 26 | 31 | 36 | V |
| Output Turn-Off Delay Time<br>($T_J$ = +25°C) to Over Voltage Condition, $V_{in}$ stepped from 12 V to 40 V<br>V ≤ 0.9 $V_O$ (Figures 3 and 4) | $t_{DLY(OV)}$ | — | 2.0 | — | μs |
| Output Recovery Delay Time ($T_J$ = +25°C)<br>$V_{in}$ stepped from 40 V to 12 V, V ≥ 0.9 $V_O$ (Figures 3 and 4) | $t_{RCVY}$ | — | 5.0 | — | μs |

NOTES:
*Typical Values Represent Characteristics of Operation at $T_J$ = +25°C.

**FIGURE 3 — TRANSIENT RESPONSE TEST CIRCUIT**



NOTE:
*Depending on Load Current and Transient Duration, an Output Capacitor ($C_O$) of sufficient value may be used to hold up Output Voltage during the Transient, and absorb Turn-off Delay Voltage Overshoot.

FIGURE 4 — RESPONSE TIME DIAGRAM

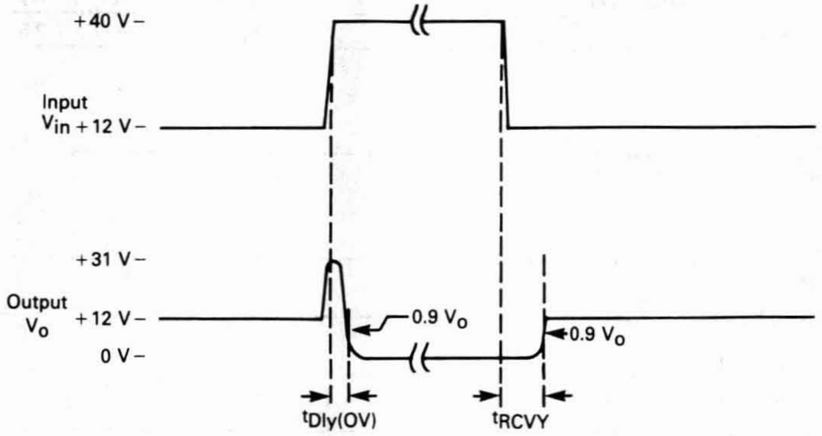

+40 V
Input
$V_{in}$ +12 V
+31 V
Output
$V_o$
+12 V
0 V
0.9 $V_o$
0.9 $V_o$
$t_{Dly(OV)}$
$t_{RCVY}$

FIGURE 5 — SWITCH VOLTAGE DROP versus LOAD CURRENT

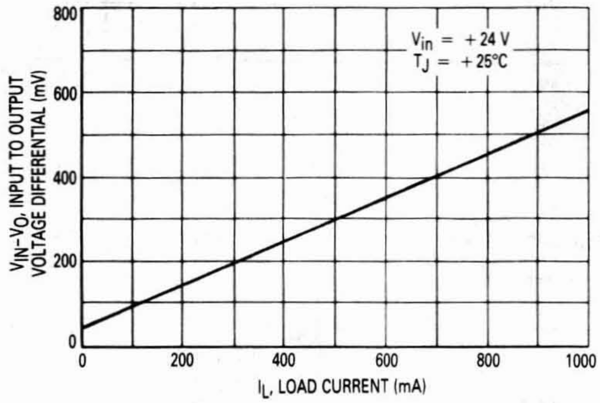
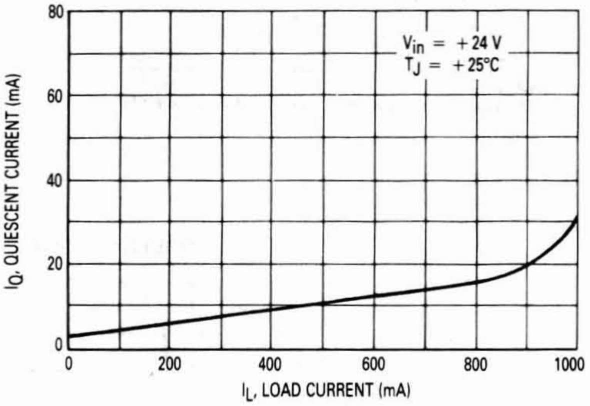


FIGURE 6 — QUIESCENT CURRENT versus LOAD CURRENT



**MOTOROLA**

# MC34061
# MC34061A

## THREE-TERMINAL PROGRAMMABLE OVERVOLTAGE SENSING CIRCUIT

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

## Advance Information

### THREE-TERMINAL OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

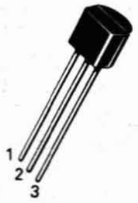
The MC34061 overvoltage protection (OVP) circuit, in combination with two external programming resistors and a "crowbar" SCR, protects sensitive electronic circuitry from overvoltage damage. It senses an overvoltage condition and quickly "crowbars", or short circuits, the supply. An external capacitor may be used to program a minimum overvoltage duration before tripping, thus providing noise immunity.

This three-terminal circuit provides a cost-effective means of protecting either positive or negative power supplies. The unique design of the MC34061 eliminates trip voltage and temperature drift errors due to SCR gate variations.

The basic MC34061 device offers a ±2% tolerance on the sense trip voltage. The A-suffix device has a ±1% sense trip voltage specification and other key parameters have tightened limits. The device is available in a low-cost plastic TO-92 package and features:

- Unique Three-Terminal Design
- SCR Gate Drive Output of 200 mA
- Sense Voltage of 2.5 V ±1% or ±2%
- Hysteresis of 250 mV
- Wide Supply Range: 4.0 V ≤ $V_{CC}$ ≤ 41 V

**P SUFFIX**
PLASTIC PACKAGE
CASE 29-02
TO-226AA
(TO-92)



Pin 1. $V_{CC}$
2. Drive Output
3. Sense

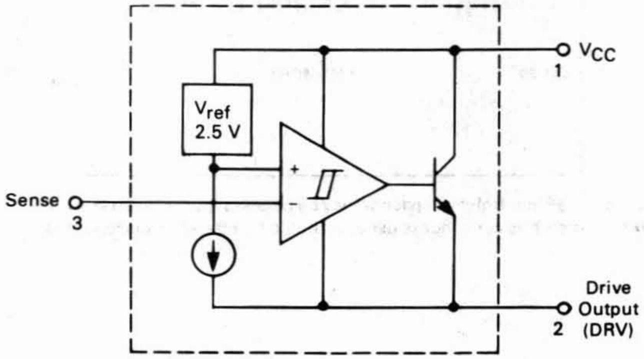
### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Operating Voltage | $V_{CC}-V_{DRV}$ | 40 | Vdc |
| Sense Voltage | $V_{Sense}$ | 40 | Vdc |
| Drive Output Current | $I_{DRV}$ | Internally Limited | mA |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Operating Junction Temperature | $T_J$ | 150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC34061P,AP | 0 to +70° C | Plastic TO-92 |

### FUNCTIONAL BLOCK DIAGRAM



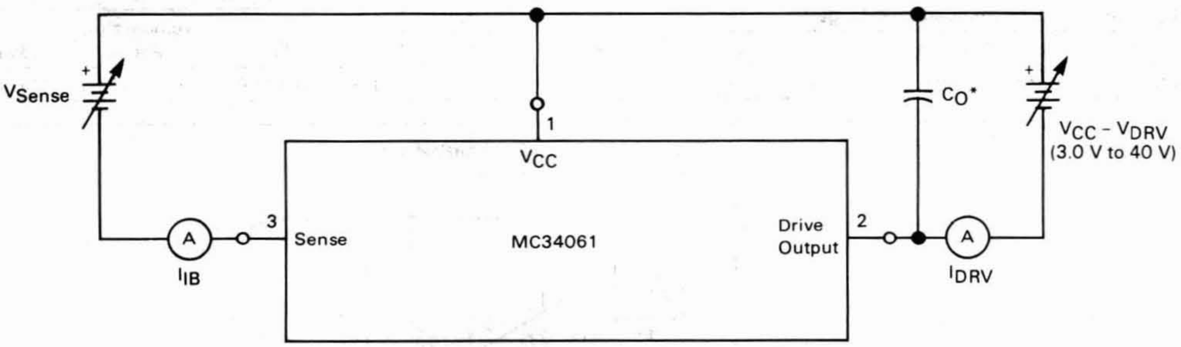
This document contains information on a new product. Specifications and information herein are subject to change without notice.

**ELECTRICAL CHARACTERISTICS** ($V_{CC} - V_{DRV}$ = 5.0 V; $T_A = T_{low}$ to $T_{high}$ [see Note 1] unless otherwise specified)

| Characteristic | Symbol | MC34061A | | | MC34061 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Operating Voltage Range | $V_{CC} - V_{DRV}$ | 3.0 | — | 40 | 3.0 | — | 40 | Vdc |
| Sense Trip Voltage | $V_{Sense}$ | | | | | | | Vdc |
| $T_A$ = 25°C | | 2.475 | 2.5 | 2.525 | 2.45 | 2.5 | 2.55 | |
| $T_{low}$ to $T_{high}$ (Note 1) | | 2.45 | 2.5 | 2.55 | 2.4 | 2.5 | 2.6 | |
| Line Regulation, $V_{Sense}$ ($3.0 \leq V_{CC} - V_{DRV} \leq 40$ V) | $Reg_{line}$ | | | | | | | %/V |
| $T_A$ = 25°C | | — | 0.001 | 0.005 | — | 0.001 | 0.01 | |
| $T_{low}$ to $T_{high}$ (Note 1) | | — | 0.001 | 0.01 | — | 0.001 | 0.02 | |
| Input Bias Current, Sense Pin | $I_{IB}$ | | | | | | | μA |
| At Trip Point (Note 2) | | — | 0.3 | 1.0 | — | 0.3 | 2.0 | |
| After Trip ($V_{Sense}$ = 3.0 V) | | — | 0.9 | 3.0 | — | 0.9 | 6.0 | |
| Hysteresis Voltage, Sense Pin | $V_H$ | — | 250 | — | — | 250 | — | mV |
| Drive Output Current, ON State | $I_{DRV(on)}$ | | | | | | | mA |
| $T_J$ = 25°C | | 130 | 200 | 300 | 130 | 200 | 300 | |
| $T_{low}$ to $T_{high}$ (Note 1) | | 90 | — | 350 | 90 | — | 350 | |
| Drive Output Current, OFF State | $I_{DRV(off)}$ | | | | | | | mA |
| $V_{CC} - V_{DRV}$ = 5.0 V | | 0.2 | 0.6 | 1.0 | 0.2 | 0.6 | 1.0 | |
| $3.0 \text{ V} \leq V_{CC} - V_{DRV} \leq 40$ V | | 0.2 | 0.6 | 1.5 | 0.2 | 0.6 | 1.5 | |
| Drive Output Current Slew Rate $T_A$ = 25°C | di/dt | — | 2.0 | — | — | 2.0 | — | A/μs |
| Drive Output $V_{CC}$ Transient Rejection $V_{CC} - V_{DRV}$ = 0 V to 15 V at dV/dt = 200 V/μs; $V_{Sense}$ = 0 V; $T_A$ = 25°C | $\Delta I_{DRV(trans)}$ | — | 1.0 | — | — | 1.0 | — | mA (Peak) |
| Propagation Delay Time ($T_A$ = 25°C) 500 mV Overdrive | $t_{PLH}$ | — | 500 | — | — | 500 | — | ns |

NOTES:
(1) $T_{low}$ to $T_{high}$ = 0°C to 70°C
(2) This specification is an engineering estimate based on design parameters, and is not tested.

**FIGURE 1 — STANDARD TEST CIRCUIT**



*A 1.0 μF tantalum or 10 μF electrolytic capacitor may be necessary to compensate for lead inductance when measuring Hysteresis Voltage. When this capacitor is used, it should be placed as close as possible to the device package.

## TYPICAL CHARACTERISTICS

FIGURE 2 — DRIVE CURRENT versus SENSE VOLTAGE

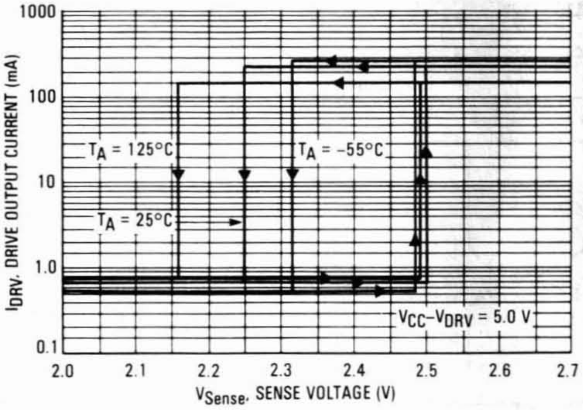


FIGURE 3 — SENSE TRIP VOLTAGE versus TEMPERATURE

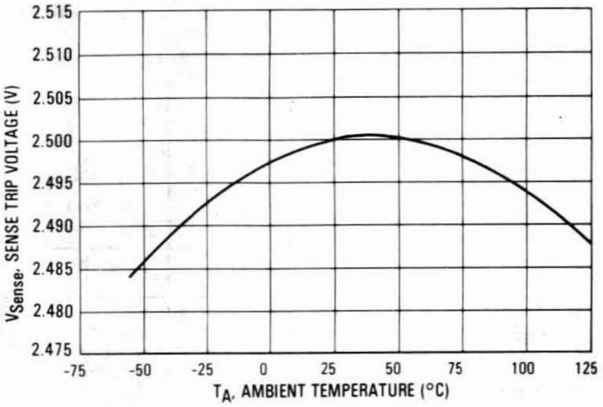


FIGURE 4 — OFF STATE DRIVE CURRENT versus SUPPLY VOLTAGE

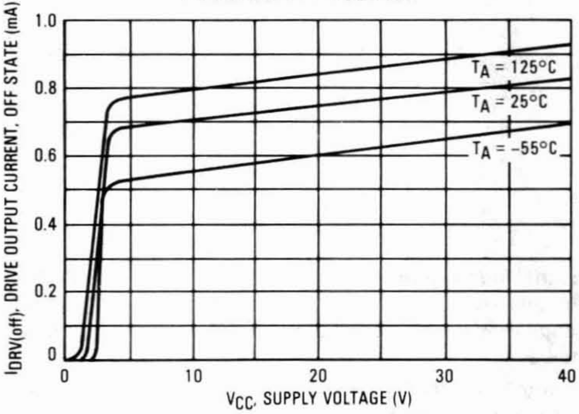


FIGURE 5 — INPUT BIAS CURRENT versus SENSE VOLTAGE

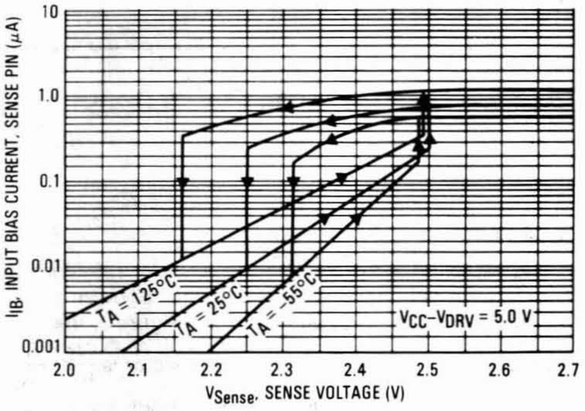


FIGURE 6 — DELAY CAPACITANCE versus DELAY TIME

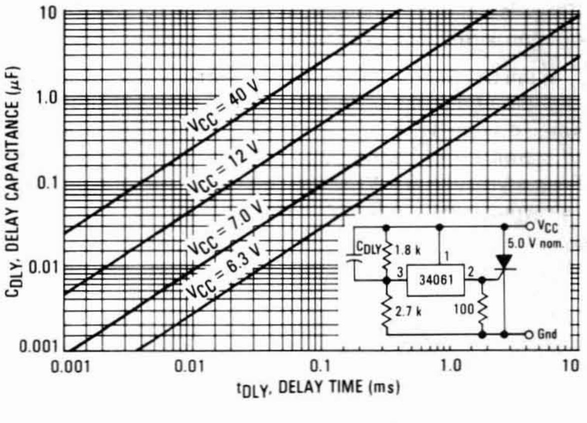
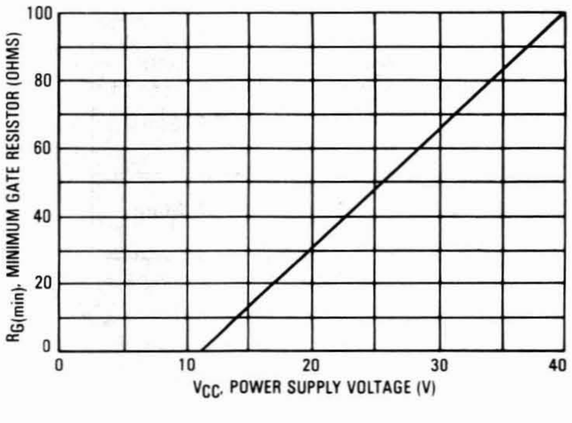
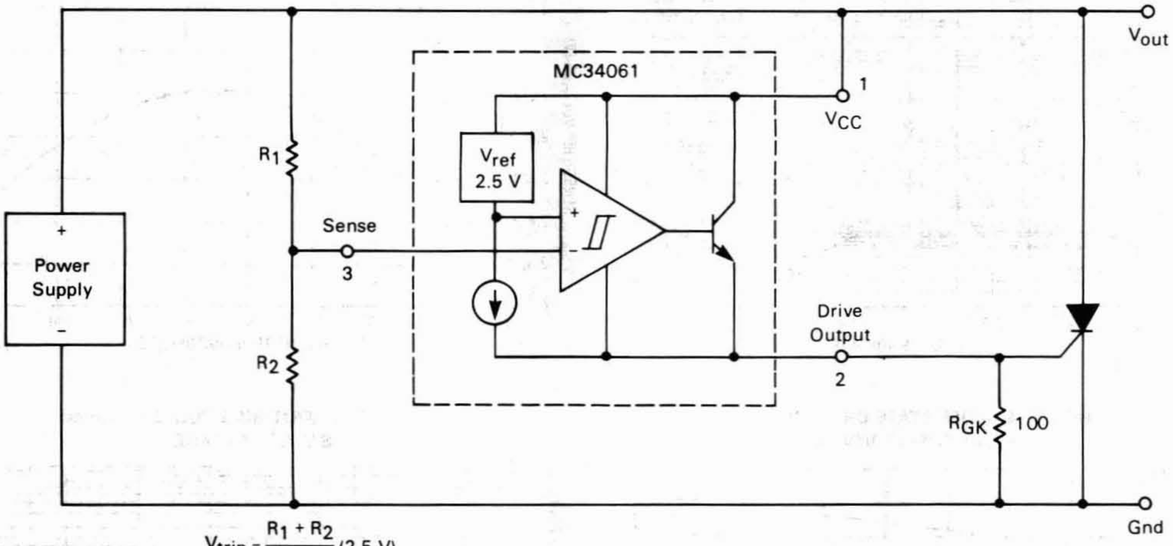


FIGURE 7 — MINIMUM $R_G$ versus SUPPLY VOLTAGE



## APPLICATIONS INFORMATION

FIGURE 8 — BLOCK DIAGRAM AND TYPICAL APPLICATION



$$V_{trip} = \frac{R_1 + R_2}{R_1}(2.5\ V)$$

### BASIC CIRCUIT CONFIGURATION

The MC34061 consists of a 2.5 V shunt reference, a comparator with 250 mV hysteresis and a power output transistor. In the typical application of Figure 8, the voltage at the inverting input of the comparator is $\frac{V_{CC} R_2}{R_1 + R_2}$, while the voltage at the non-inverting input is $V_{CC} - 2.5$ V. Thus, given ($R_1$, $R_2$) voltage divider, the comparator's output state is a function of $V_{CC}$. The following table applies:

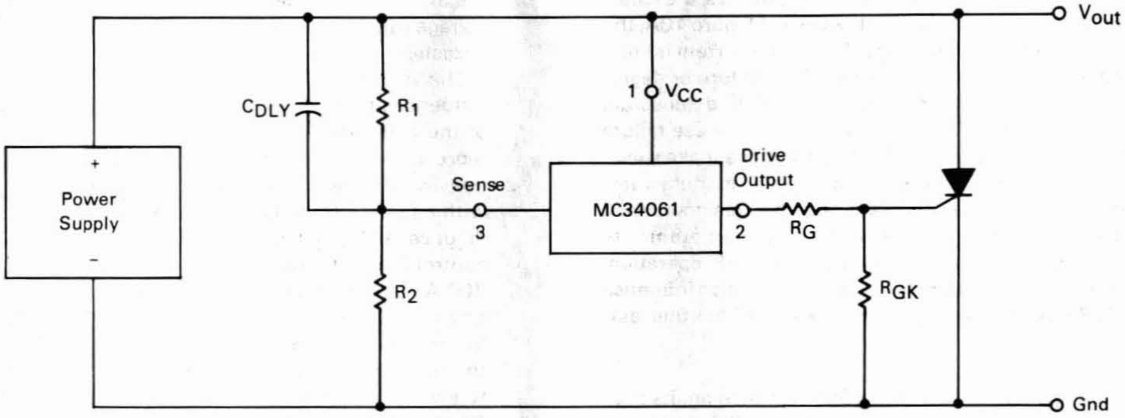
| $V_{CC}$ | Drive Output |
|---|---|
| $< \frac{R_1 + R_2}{R_1}(2.5\ V)$ | OFF State |
| $> \frac{R_1 + R_2}{R_1}(2.5\ V)$ | ON State |

By making the proper choice of $R_1$ and $R_2$, a level detector for any voltage within the device's operating voltage range may be realized. A few precautions are necessary, however.

Note that even in the OFF State, a minimum drive output current, equal to the sum of the reference and comparator supply currents, is available. Therefore, a means of shunting this current away from the driven circuit is necessary. In the example of Figure 8, a 100 Ω resistor ($R_{GK}$) is used, producing a voltage at the Drive Output of approximately 60 mV in the OFF State.

In the ON State the MC34061 becomes a current source capable of saturating to within 2.0 V of $V_{CC}$. Therefore, when driving a high impedance load, it may be desirable to clamp the drive output to at least 3.0 V below $V_{CC}$ ($V_{CC} - V_{DRV} \geq 3.0$ V) if it is important that the voltage reference continue to regulate.

FIGURE 9 — OVERVOLTAGE PROTECTION WITH TIME DELAY



### PROGRAMMING A MINIMUM OVERVOLTAGE DURATION BEFORE TRIPPING

A time delay may be programmed into the operation of the MC34061 to provide noise immunity. This time delay is implemented by adding a capacitor ($C_{DLY}$) between the $V_{CC}$ and Sense leads as shown in Figure 9. The time delay obtained by this technique is a function of $R_1$, $R_2$ and $C_{DLY}$ as well as the nominal supply voltage, $V_{CC(nom)}$, and the overvoltage supply voltage, $V_{CC}$. The nominal supply voltage determines the initial charge on $C_{DLY}$, while the magnitude of the overvoltage condition determines the rate at which $C_{DLY}$ charges to the reference voltage, $V_{ref} = 2.5$ V. Thus, for a given $R_1$, $R_2$ and $C_{DLY}$, the time delay is reduced as the overvoltage is increased. The expression for the time delay, $T_{DLY}$, is:

$$t_{DLY} = \frac{R_1 R_2 C_{DLY}}{R_1 + R_2} \ln \left[\frac{V_{CC} - V_{CC(nom)}}{V_{CC} - V_{trip}}\right]$$

where:

$$V_{trip} = \frac{R_1 + R_2}{R_1} (2.5\ V)$$

Figure 6 shows the $C_{DLY}$ values versus delay time ($t_{DLY}$) for a typical 5.0 V power supply protection circuit. The figure also shows the change in $t_{DLY}$ with variations in the overvoltage supply, $V_{CC}$. In this example $R_1 = 1.8$ k, $R_2 = 2.7$ k, $V_{CC(nom)} = 5.0$ V, and $V_{trip} = 6.25$ V.

### THE NEED FOR A GATE RESISTOR

For power supplies above 11 V, a gate resistor, $R_G$, in series with the SCR gate is recommended to limit the power dissipated by the IC to approximately 2.0 W. This resistor will protect the MC34061 in the event of a defective or missing SCR, while allowing the maximum drive output current to the gate of the SCR. Figure 7 shows the minimum recommended gate resistor, $R_{G(min)}$, versus the power supply voltage, $V_{CC}$. A larger value of $R_G$ may be used if less drive current is needed.

## CROWBAR SCR CONSIDERATIONS

Referring to Figure 10, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, $C_{out}$. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 10A, the supply's input filter capacitors. This surge current is illustrated in Figure 11, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or $I^2t$. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

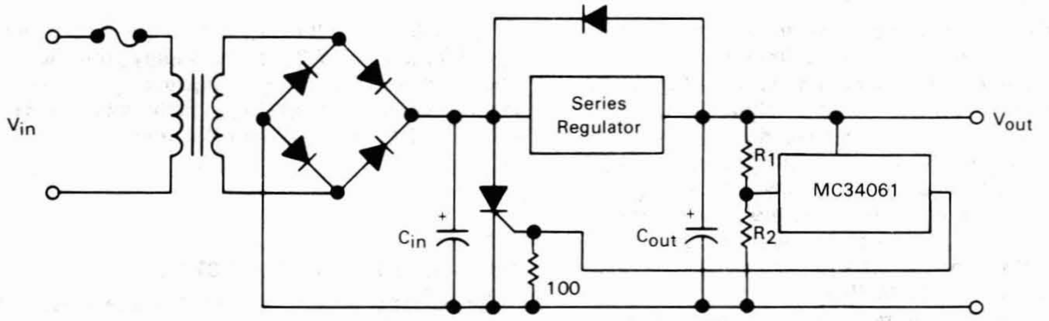
### 1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

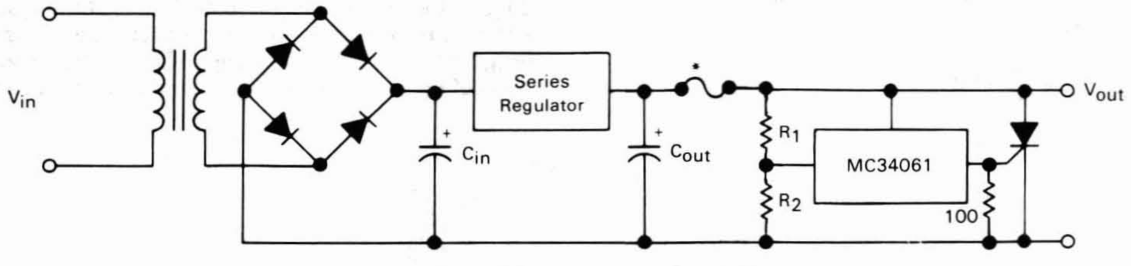
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times $I_{GT}$) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/µs, assuming a gate current of five times $I_{GT}$ and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 12. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 10 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS

10A — SCR ACROSS INPUT OF REGULATOR

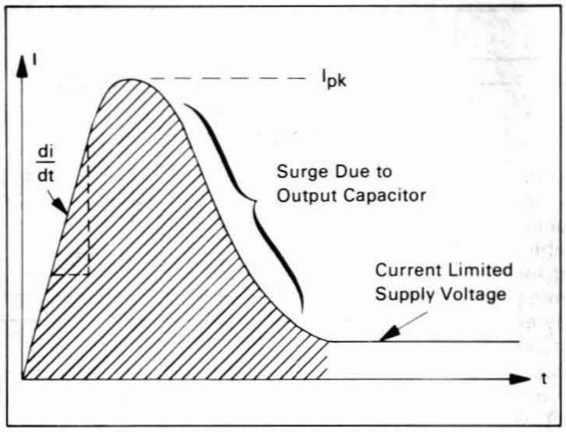


10B — SCR ACROSS OUTPUT OF REGULATOR



*Needed if supply is not current limited

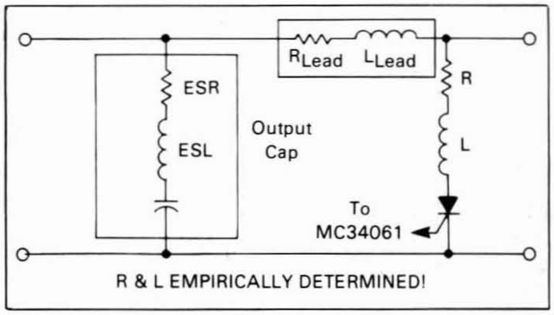
FIGURE 11 — CROWBAR SCR SURGE CURRENT WAVEFORM



**2. Surge Current**

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 12) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 12 — CIRCUIT ELEMENTS AFFECTING SCR SURGE AND di/dt



## A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 10A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an $I^2t$ rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 10B.

## CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

| DEVICE | $I_{RMS}$ | $I_{FSM}$ | PACKAGE |
|---|---|---|---|
| MCR67 Series | 12 A | 100 A | Metal Stud |
| MCR68 Series | 12 A | 100 A | TO-220 Plastic |
| 2N1842 Series | 16 A | 125 A | Metal Stud |
| 2N6400 Series | 16 A | 160 A | TO-220 Plastic |
| 2N6504 Series | 25 A | 160 A | TO-220 Plastic |
| 2N681 Series | 25 A | 200 A | Metal Stud |
| 2N2573 Series | 25 A | 260 A | TO-3 Metal Can |
| MCR69 Series | 25 A | 300 A | TO-220 Plastic |
| MCR70 Series | 35 A | 350 A | Metal Stud |
| MCR71 Series | 55 A | 550 A | Metal Stud |

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

**MOTOROLA**

# MC34062
# MC35062

## Advance Information

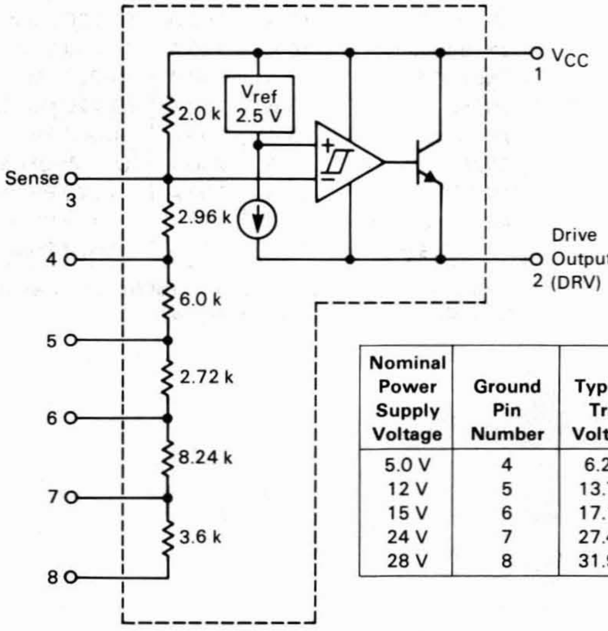
## PIN-PROGRAMMABLE OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

The MC34062/35062 overvoltage protection (OVP) circuits require only an external "crowbar" SCR to protect sensitive electronic circuitry from overvoltage damage. They sense an overvoltage condition and quickly "crowbar", or short circuit, the supply. An on-chip, tapped resistor network allows the device to be programmed for trip voltages ranging from 3.5 to 40 V. Each of the five programming pins provides one standard overvoltage trip point for nominal power supply voltages of 5.0, 12, 15, 24 or 28 V. Many other trip voltages may be programmed by interconnecting and grounding various combinations of these programming pins. Tables are provided in the Applications Information which show connection schemes for 120 trip voltages.

These circuits provide a cost-effective means of protecting either positive or negative power supplies. In addition, an external capacitor may be used to program a minimum overvoltage duration before tripping, thus providing noise immunity. The unique design of the MC34062/35062 eliminates voltage and temperature drift errors due to SCR gate variations.

- Unique Pin-Programmable Trip Voltage from 3.5 to 40 V
- One-Pin Programming for 5.0, 12, 15, 24 and 28 V Power Supplies
- SCR Gate Drive Output of 200 mA
- Built-In Hysteresis Voltage
- Wide Supply Range: 4.0 V $\leq V_{CC} \leq$ 40 V

### FUNCTIONAL BLOCK DIAGRAM



| Nominal Power Supply Voltage | Ground Pin Number | Typical Trip Voltage |
|---|---|---|
| 5.0 V | 4 | 6.2 V |
| 12 V | 5 | 13.7 V |
| 15 V | 6 | 17.1 V |
| 24 V | 7 | 27.4 V |
| 28 V | 8 | 31.9 V |

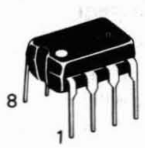
Pins 4 through 8 are used to program the Trip Voltage, $V_{trip}$

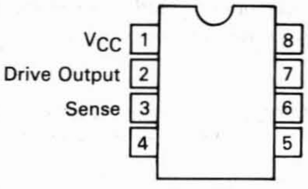
## PIN-PROGRAMMABLE OVERVOLTAGE SENSING CIRCUIT

### SILICON MONOLITHIC INTEGRATED CIRCUIT

**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04

(MC34062 only)

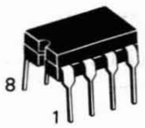




(Top View)

Note:
Pins 4 thru 8 are used to program the Trip Voltage, $V_{trip}$

**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02



### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC35062U | -55 to +125°C | Ceramic DIP |
| MC34062P1 | 0 to +70°C | Plastic DIP |
| MC34062U | | Ceramic DIP |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

## MAXIMUM RATINGS

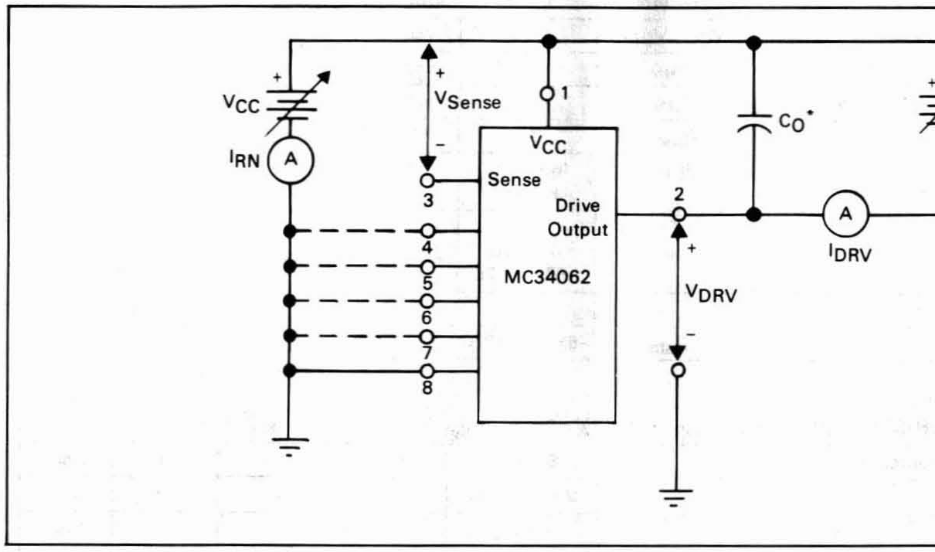
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Operating Voltage | $V_{CC} - V_{DRV}$ | 40 | Vdc |
| Voltage Across Any Internal Resistor In Network | $V_{RN}$ | 40 | Vdc |
| Current Through Any Resistor In Network | $I_{RN}$ | 10 | mA |
| Sense Voltage | $V_{Sense}$ | 40 | Vdc |
| Drive Output Current | $I_{DRV}$ | Internally Limited | mA |
| Operating Ambient Temperature | $T_A$ | | °C |
| MC34062 | | 0 to +70 | |
| MC35062 | | −55 to +125 | |
| Operating Junction Temperature | $T_J$ | 150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150°C | °C |

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0 V; $V_{DRV}$ = 0 V; $T_A = T_{low}$ to $T_{high}$ unless otherwise specified.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Voltage Range | $V_{CC} - V_{DRV}$ | 3.0 | — | 40 | Vdc |
| Sense Trip Voltage | $V_{Sense}$ | | | | Vdc |
| $T_A$ = 25°C | | 2.425 | 2.5 | 2.575 | |
| $T_{low}$ to $T_{high}$ | | 2.375 | 2.5 | 2.625 | |
| Line Regulation, $V_{Sense}$ (3.0 V ≤ $V_{CC} - V_{DRV}$ ≤ 40 V) | $Reg_{line}$ | | | | %/V |
| $T_A$ = 25°C | | — | 0.001 | 0.01 | |
| $T_{low}$ to $T_{high}$ | | — | 0.001 | 0.02 | |
| Trip Voltage (Pin 4 = Gnd; $V_{DRV}$ = 0 V) | $V_{trip(4)}$ | | | | V |
| $T_A$ = 25°C | | 6.01 | 6.2 | 6.39 | |
| $T_{low}$ to $T_{high}$ | | 5.89 | 6.2 | 6.51 | |
| Hysteresis Voltage (Pin 4 = Gnd; $V_{DRV}$ = 0 V) | $V_{H(4)}$ | — | 0.62 | — | V |
| Trip Voltage (Pin 5 = Gnd; $V_{DRV}$ = 0 V) | $V_{trip(5)}$ | | | | V |
| $T_A$ = 25°C | | 13.3 | 13.7 | 14.1 | |
| $T_{low}$ to $T_{high}$ | | 13.0 | 13.7 | 14.4 | |
| Hysteresis Voltage (Pin 5 = Gnd; $V_{DRV}$ = 0 V) | $V_{H(5)}$ | — | 1.37 | — | V |
| Trip Voltage (Pin 6 = Gnd; $V_{DRV}$ = 0 V) | $V_{trip(6)}$ | | | | V |
| $T_A$ = 25°C | | 16.6 | 17.1 | 17.6 | |
| $T_{low}$ to $T_{high}$ | | 16.2 | 17.1 | 18.0 | |
| Hysteresis Voltage (Pin 6 = Gnd; $V_{DRV}$ = 0 V) | $V_{H(6)}$ | — | 1.71 | — | V |
| Trip Voltage (Pin 7 = Gnd; $V_{DRV}$ = 0 V) | $V_{trip(7)}$ | | | | V |
| $T_A$ = 25°C | | 26.6 | 27.4 | 28.2 | |
| $T_{low}$ to $T_{high}$ | | 26.0 | 27.4 | 28.8 | |
| Hysteresis Voltage (Pin 7 = Gnd; $V_{DRV}$ = 0 V) | $V_{H(7)}$ | — | 2.74 | — | V |
| Trip Voltage (Pin 8 = Gnd; $V_{DRV}$ = 0 V) | $V_{trip(8)}$ | | | | V |
| $T_A$ = 25°C | | 30.9 | 31.9 | 32.9 | |
| $T_{low}$ to $T_{high}$ | | 30.3 | 31.9 | 33.5 | |
| Hysteresis Voltage (Pin 8 = Gnd; $V_{DRV}$ = 0 V) | $V_{H(8)}$ | — | 3.19 | — | V |
| Resistor Network Current at Nominal Power Supply Voltage<br>$V_{CC}$ = 28 V; $V_{DRV}$ = 0 V; Pin 8 = Gnd | $I_{RN}$ | 0.5 | 1.1 | 2.0 | mA |
| Drive Output Current, ON State | $I_{DRV(on)}$ | | | | mA |
| $T_J$ = 25°C | | 130 | 200 | 300 | |
| $T_{low}$ to $T_{high}$ | | 90 | — | 350 | |
| Drive Output Current, OFF State | $I_{DRV(off)}$ | | | | mA |
| $V_{CC}$ = 5.0 V; $V_{DRV}$ = 0 V | | 0.2 | 0.6 | 1.0 | |
| 3.0 V ≤ $V_{CC} - V_{DRV}$ ≤ 40 V | | 0.2 | 0.6 | 1.5 | |
| Drive Output Current Slew Rate ($T_A$ = 25°C) | di/dt | — | 2.0 | — | A/μs |
| Drive Output $V_{CC}$ Transient Rejection<br>$V_{CC}$ = 0 V to 15 V at dV/dt = 200 V/μs;<br>$V_{DRV}$ = 0 V; $V_{Sense}$ = 0 V; $T_A$ = 25°C | $\Delta I_{DRV(trans)}$ | — | 1.0 | — | mA (Peak) |
| Propagation Delay Time ($T_A$ = 25°C; 500 mV Overdrive) | $t_{PLH}$ | — | 500 | — | ns |

$T_{low}$ = −55°C for MC35062 $T_{high}$ = +125°C for MC35062
= 0°C for MC34062 = + 70°C for MC34062

FIGURE 1 — STANDARD TEST CIRCUIT


VCC
IRN
A
VSense
+
-
1
VCC
Sense
3
Drive
Output
2
4
5
6
7
8
MC34062
+
VDRV
-
CO*
A
IDRV
VCC - VDRV
(3.0 V to 40 V)

*A 1.0 µF tantalum or 10 µF electrolytic capacitor may be necessary to compensate for lead inductance when measuring Hysteresis Voltage. When this capacitor is used, it should be placed as close as possible to the device package.

FIGURE 2 — DRIVE CURRENT versus NORMALIZED RESISTOR DIVIDER VOLTAGE (Normalized to $V_{trip}$ at $T_A$ = 25°C)

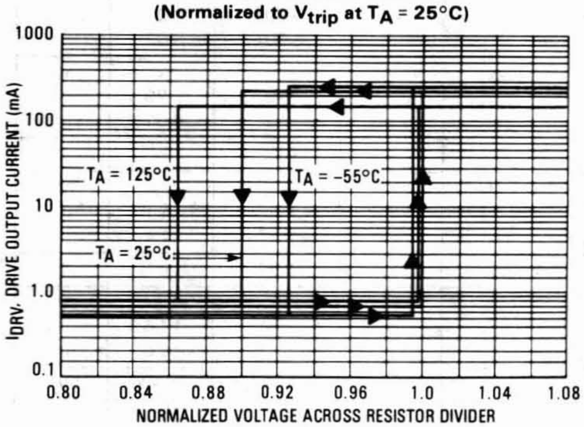


FIGURE 3 — NORMALIZED TRIP VOLTAGE versus TEMPERATURE (Normalized to $T_A$ = 25°C)

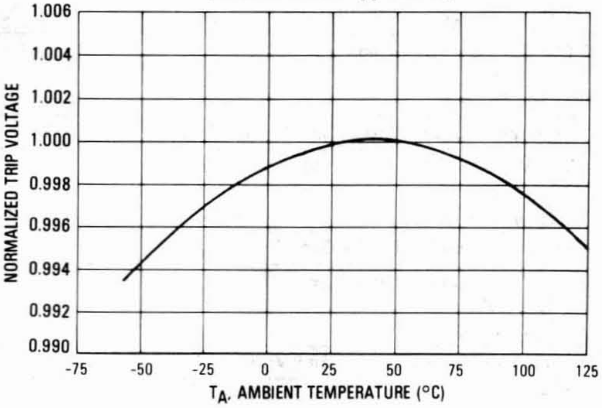


FIGURE 4 — OFF STATE DRIVE CURRENT versus SUPPLY VOLTAGE

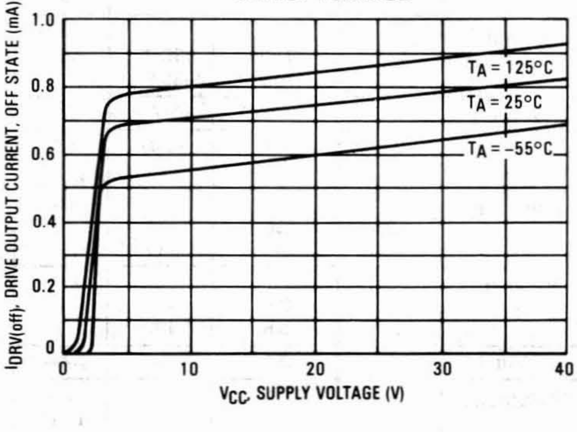


FIGURE 5 — MINIMUM $R_G$ versus SUPPLY VOLTAGE

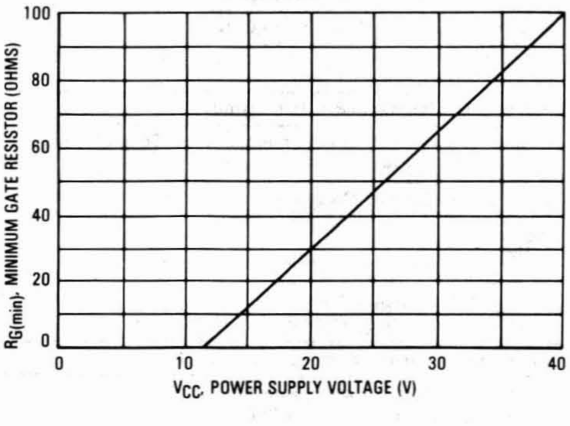


FIGURE 6 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 5.0 V POWER SUPPLY

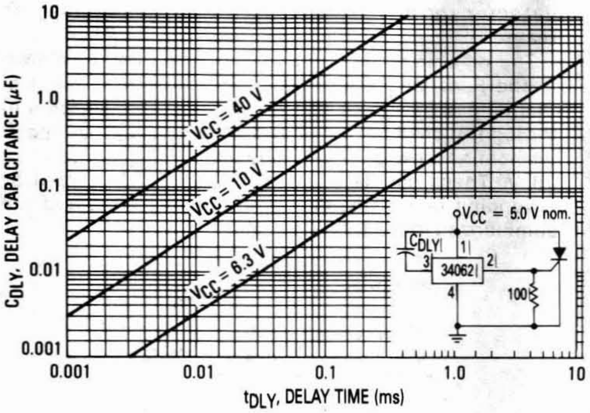


FIGURE 7 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 12 V POWER SUPPLY

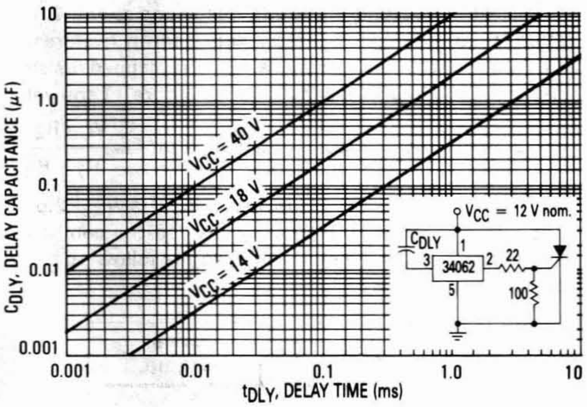


FIGURE 8 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 15 V POWER SUPPLY

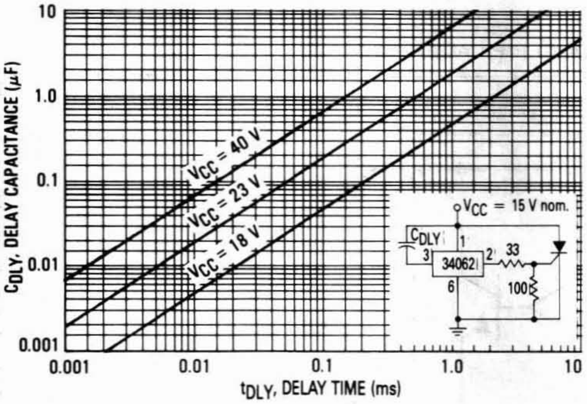


FIGURE 9 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 24 V POWER SUPPLY

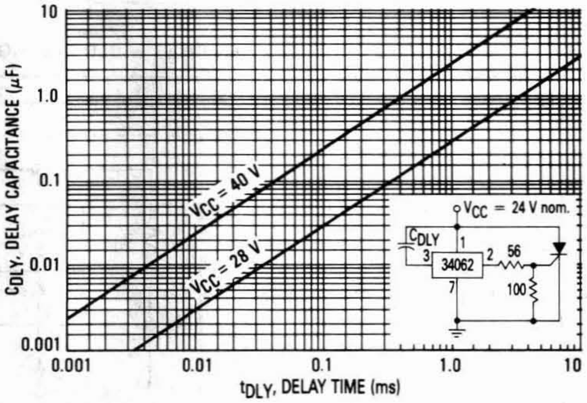


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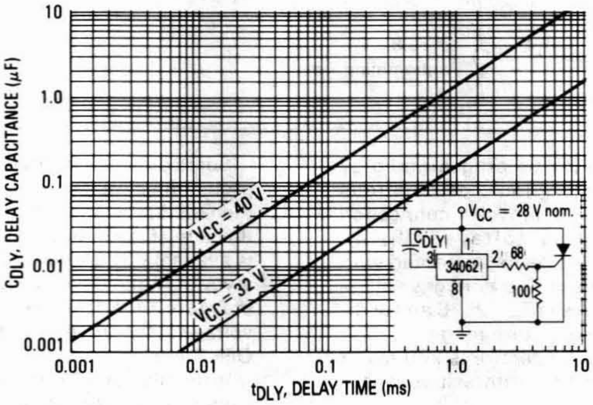
FIGURE 10 — DELAY CAPACITANCE versus DELAY TIME FOR NOMINAL 28 V POWER SUPPLY



## APPLICATIONS INFORMATION

### BASIC CIRCUIT CONFIGURATION

The MC34062 and MC35062 each consist of a 2.5 V shunt reference, a comparator with built-in hysteresis, a power output transistor, and an on-chip, tapped resistor network. In the typical application of Figure 11 the voltage at the inverting input of the comparator is $\frac{V_{CC} R_2}{R_1 + R_2}$, while the voltage at the non-inverting input is $V_{CC} - 2.5$ V. Thus, for a given ($R_1$, $R_2$) voltage divider, the comparator's output state is a function of $V_{CC}$. The following table applies:

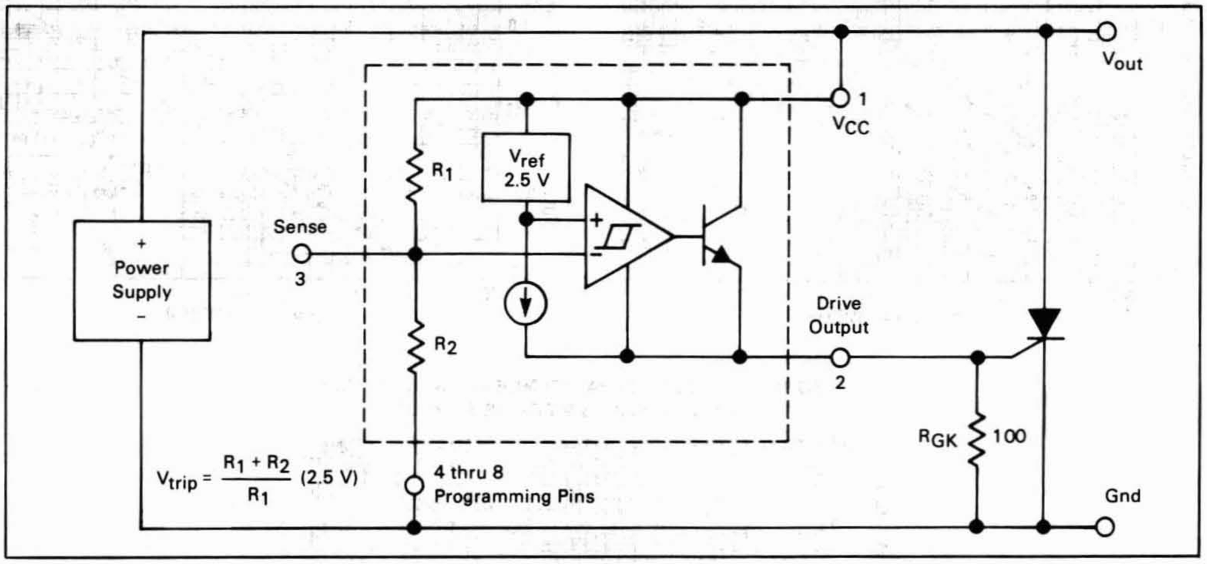
| $V_{CC}$ | Drive Output |
|---|---|
| $< \frac{R_1 + R_2}{R_1}$ (2.5 V) | OFF State |
| $> \frac{R_1 + R_2}{R_1}$ (2.5 V) | ON State |

By making the proper choice of $R_1$ and $R_2$, a level detector for any voltage from 3.5 to 40 V may be realized.

The on-chip resistor network is configured as shown in the Functional Block Diagram on the front page of this data sheet. Each of the five programming pins (4 through 8) provides one standard overvoltage trip point for nominal power supply voltages of 5.0, 12, 15, 24 or 28 V. These standard trip points are implemented by grounding one of the five programming pins, and are summarized in the following table:

| Nominal Power Supply Voltage | Ground Pin Number | Typical Trip Voltage |
|---|---|---|
| 5.0 V | 4 | 6.2 V |
| 12 V | 5 | 13.7 V |
| 15 V | 6 | 17.1 V |
| 24 V | 7 | 27.4 V |
| 28 V | 8 | 31.9 V |

FIGURE 11 — BLOCK DIAGRAM AND TYPICAL APPLICATION



Many other trip voltages may be programmed by interconnecting and grounding various combinations of the programming pins. Table 1 provides connection schemes for 120 nominal Trip Voltages ($V_{trip}$). Additional Trip Voltages may also be implemented with other pin connections. All of these Trip Voltages will be within ±3.0% of the nominal value at $T_A = 25°C$ and within ±5.0% over the operating temperature range.

The hysteresis built into the comparator is 250 mV at the inverting input. This comparator hysteresis voltage is multiplied by the ratio $\frac{R_1 + R_2}{R_1}$, just as the 2.5 V Sense Trip Voltage ($V_{Sense}$) is multiplied by the same ratio to define the Trip Voltage ($V_{trip}$). Thus, the Hysteresis Voltage ($V_H$) is approximately 10% of the Trip Voltage for any Trip Voltage.

Some precautions are necessary in the operation of the protection circuit shown in Figure 11. Note that even in the OFF State, a minimum drive output current, equal to the sum of the reference and comparator supply currents, is available. Therefore, a means of shunting this current away from the driven circuit is necessary. In the example of Figure 11; a 100 Ω resistor ($R_{GK}$) is used, producing a voltage at the Drive Output of approximately 60 mV in the OFF State.

In the ON State the MC34062 becomes a current source capable of saturating to within 2.0 V of $V_{CC}$. Therefore, when driving a high impedance load, it may be desirable to clamp the drive output to at least 3.0 V below $V_{CC}$ ($V_{CC} - V_{DRV} \geq 3.0$ V) if it is important that the reference continue to regulate.

### PROGRAMMING A MINIMUM OVERVOLTAGE DURATION BEFORE TRIPPING

A time delay may be programmed into the operation of the MC34062/35062 to provide noise immunity. This time delay is implemented by adding a capacitor ($C_{DLY}$) between the $V_{CC}$ and Sense leads as shown in Figure 12. The time delay obtained by this technique is a function of the internal resistors ($R_1$, $R_2$) and $C_{DLY}$, as well as the nominal supply voltage, $V_{CC(nom)}$, and the overvoltaged supply voltage $V_{CC}$. The nominal supply voltage determines the initial charge on $C_{DLY}$, while the magnitude of the overvoltage condition determines the rate at which $C_{DLY}$ charges to the reference voltage, $V_{ref} = 2.5$ V. Thus, for a given $R_1$, $R_2$ and $C_{DLY}$, the time delay is reduced as the overvoltage is increased. The expression for the time delay, $t_{DLY}$ is:

$$t_{DLY} = \frac{R_1 R_2 C_{DLY}}{R_1 + R_2} \ln \left[\frac{V_{CC} - V_{CC(nom)}}{V_{CC} - V_{trip}}\right]$$

$$\text{where: } V_{trip} = \frac{R_1 + R_2}{R_1}(2.5\text{ V})$$

Figures 6 through 10 show the $C_{DLY}$ values versus delay time ($t_{DLY}$) for nominal 5.0, 12, 15, 24 and 28 V power supply protection circuits, each using a one-pin MC34062/35062 programming scheme. These figures also show the change in $t_{DLY}$ with variations in the overvoltaged supply, $V_{CC}$.

### THE NEED FOR A GATE RESISTOR

For power supplies above 11 V, a gate resistor, $R_G$, in series with the SCR gate is recommended to limit the power dissipated by the IC to approximately 2.0 W. This resistor will protect the MC34062/35062 in the event of a defective or missing SCR, while allowing the maximum drive output current to the gate of the SCR. Figure 5 shows the minimum recommended gate resistor, $R_{G(min)}$, versus the power supply voltage, $V_{CC}$. A larger value of $R_G$ may be used if less drive current is needed.

FIGURE 12 — OVERVOLTAGE PROTECTION WITH TIME DELAY

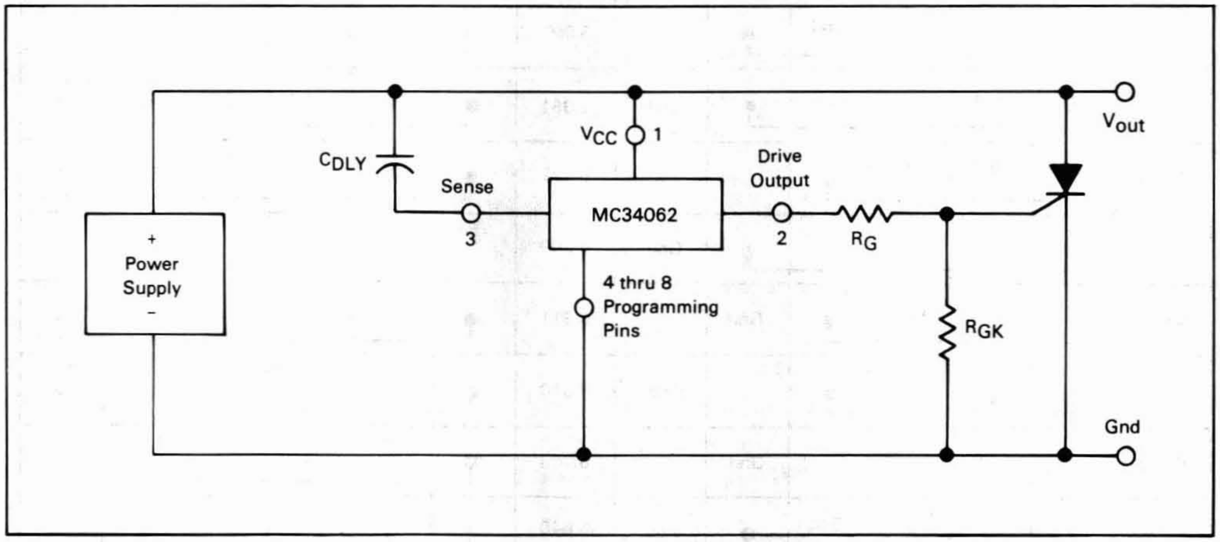
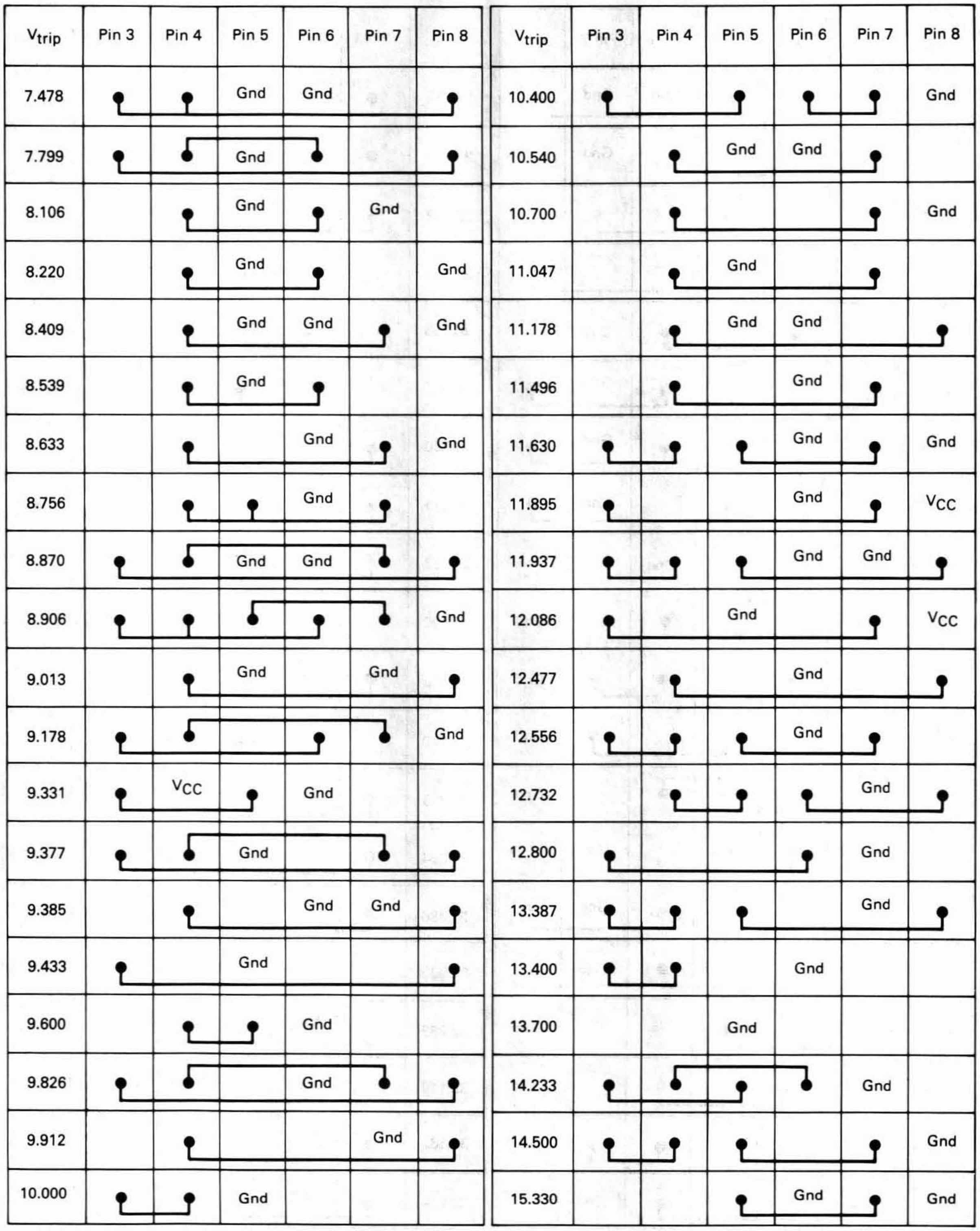


TABLE 1 — PIN-PROGRAMMING OF RESISTOR NETWORK FOR NOMINAL TRIP VOLTAGES

| $V_{trip}$ | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 | $V_{trip}$ | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.483 | ● | Gnd | ● | Gnd | ● | Gnd | 5.101 | ● |  | Gnd |  | ● | Gnd |
| 3.632 | ● | Gnd | Gnd | ● | Gnd | ● | 5.222 | ● | Gnd |  | Gnd | ● |  |
| 3.758 | ● | Gnd | ● | Gnd | ● |  | 5.328 | ● | Gnd | ● |  | ● | ● |
| 3.807 | ● | Gnd | ● | Gnd |  | ● | 5.413 | ● | Gnd | Gnd |  | ● |  |
| 3.883 | ● | Gnd | ● | ● | Gnd | ● | 5.563 | ● | Gnd | ● | ● | ● |  |
| 3.923 | ● |  | Gnd | ● | Gnd | ● | 5.673 | ● | Gnd | ● | ● |  | ● |
| 4.012 | ● | Gnd | Gnd | ● | Gnd |  | 5.734 | ● | Gnd |  |  |  | ● |
| 4.098 | ● | Gnd | ● |  | ● | Gnd | 5.887 | ● |  | ● |  | Gnd | ● |
| 4.130 | ● |  | ● | Gnd | ● | Gnd | 5.900 | ● |  | ● | Gnd |  |  |
| 4.196 | ● | Gnd |  | Gnd | ● | Gnd | 5.991 | ● | ● | Gnd | ● | ● | ● |
| 4.272 | ● | Gnd | Gnd | ● |  |  | 6.092 | ● | ● | ● | ● | Gnd | ● |
| 4.353 | ● | Gnd |  |  | ● | Gnd | 6.200 |  | Gnd |  |  |  |  |
| 4.407 | ● | ● | Gnd | ● | Gnd |  | 6.311 | ● |  |  |  | Gnd | ● |
| 4.520 | ● | ● | Gnd | ● |  | Gnd | 6.610 | ● | ● | ● | ● | Gnd | ● |
| 4.598 | ● | Gnd | ● |  | Gnd |  | 6.703 | ● | ● | ● | Gnd | ● |  |
| 4.673 | ● | ● | ● | Gnd | ● | Gnd | 6.840 | ● | ● | Gnd | Gnd | ● |  |
| 4.709 | ● | ● | Gnd | Gnd | ● | Gnd | 7.000 | ● |  |  |  | ● | Gnd |
| 4.845 | ● | Gnd | ● | Gnd | ● | ● | 7.132 | ● |  | Gnd | ● | ● | ● |
| 4.947 | ● |  | Gnd | Gnd | ● | Gnd | 7.298 | ● | ● | ● | Gnd |  | ● |
| 4.996 | ● | ● | Gnd | ● | Gnd | ● | 7.347 | ● | ● | Gnd |  | ● |  |

TABLE 1 — (Continued)



| $V_{trip}$ | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 |
|---|---|---|---|---|---|---|
| 7.478 | ● | ● | Gnd | Gnd | | ● |
| 7.799 | ● | ● | Gnd | ● | | ● |
| 8.106 | | ● | Gnd | ● | Gnd | |
| 8.220 | | ● | Gnd | ● | | Gnd |
| 8.409 | | ● | Gnd | Gnd | ● | Gnd |
| 8.539 | | ● | Gnd | ● | | |
| 8.633 | | ● | | Gnd | ● | Gnd |
| 8.756 | | ● | ● | Gnd | ● | |
| 8.870 | ● | ● | Gnd | Gnd | ● | ● |
| 8.906 | ● | ● | ● | ● | ● | Gnd |
| 9.013 | | ● | Gnd | | Gnd | ● |
| 9.178 | ● | ● | | ● | ● | Gnd |
| 9.331 | ● | $V_{CC}$ | ● | Gnd | | |
| 9.377 | ● | ● | Gnd | | ● | ● |
| 9.385 | | ● | | Gnd | Gnd | ● |
| 9.433 | ● | | Gnd | | | ● |
| 9.600 | | ● | ● | Gnd | | |
| 9.826 | ● | ● | | Gnd | ● | ● |
| 9.912 | | ● | | | Gnd | ● |
| 10.000 | ● | ● | Gnd | | | |
| 10.400 | ● | | ● | ● | ● | Gnd |
| 10.540 | | ● | Gnd | Gnd | ● | |
| 10.700 | | ● | | | ● | Gnd |
| 11.047 | | ● | Gnd | | ● | |
| 11.178 | | ● | Gnd | Gnd | | ● |
| 11.496 | | ● | | Gnd | ● | |
| 11.630 | ● | ● | ● | Gnd | ● | Gnd |
| 11.895 | ● | | | Gnd | ● | $V_{CC}$ |
| 11.937 | ● | ● | ● | Gnd | Gnd | ● |
| 12.086 | ● | | Gnd | | ● | $V_{CC}$ |
| 12.477 | | ● | | Gnd | | ● |
| 12.556 | ● | ● | ● | Gnd | ● | |
| 12.732 | | ● | ● | ● | Gnd | ● |
| 12.800 | ● | | | ● | Gnd | |
| 13.387 | ● | ● | ● | | Gnd | ● |
| 13.400 | ● | ● | | Gnd | | |
| 13.700 | | | Gnd | | | |
| 14.233 | ● | ● | ● | ● | Gnd | |
| 14.500 | ● | ● | ● | | ● | Gnd |
| 15.330 | | | ● | Gnd | ● | Gnd |

**TABLE 1 — (Continued)**

| $V_{trip}$ | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 |
|---|---|---|---|---|---|---|
| 15.637 | | | ● | Gnd | Gnd | ● |
| 16.200 | ● | | ● | | Gnd | |
| 16.256 | | | ● | Gnd | ● | |
| 16.465 | | | ● | Gnd | | ● |
| 16.500 | | ● | | ● | Gnd | |
| 16.532 | ● | ● | | ● | Gnd | ● |
| 16.832 | | | ● | ● | Gnd | ● |
| 17.087 | | | ● | | Gnd | ● |
| 17.100 | | | | Gnd | | |
| 17.300 | ● | | | ● | | Gnd |
| 17.900 | ● | ● | | ● | ● | Gnd |
| 18.200 | | | ● | | ● | Gnd |
| 18.733 | ● | ● | ● | ● | | Gnd |
| 19.900 | | ● | ● | | Gnd | |
| 20.232 | | | | ● | Gnd | ● |
| 20.300 | ● | ● | ● | ● | Gnd | |
| 20.700 | ● | | ● | | | Gnd |
| 21.000 | | ● | | ● | | Gnd |
| 21.600 | | | | ● | ● | Gnd |
| 22.122 | ● | $V_{CC}$ | | ● | Gnd | |
| 22.673 | ● | | $V_{CC}$ | ● | Gnd | |
| 23.700 | ● | ● | | | Gnd | |
| 23.807 | ● | ● | $V_{CC}$ | ● | Gnd | |
| 24.000 | | | ● | ● | Gnd | |
| 24.283 | | ● | $V_{CC}$ | ● | | Gnd |
| 24.400 | | ● | ● | | | Gnd |
| 24.800 | ● | ● | ● | ● | | Gnd |
| 25.211 | ● | | | Gnd | $V_{CC}$ | ● |
| 27.333 | ● | $V_{CC}$ | $V_{CC}$ | ● | Gnd | |
| 27.400 | | | | | Gnd | |
| 28.200 | ● | ● | | | | Gnd |
| 28.500 | | | ● | ● | | Gnd |
| 30.023 | ● | $V_{CC}$ | ● | | Gnd | |
| 30.694 | ● | $V_{CC}$ | | ● | | Gnd |
| 31.486 | ● | | $V_{CC}$ | ● | | Gnd |
| 31.900 | | | | | | Gnd |
| 32.233 | ● | $V_{CC}$ | ● | ● | | Gnd |
| 33.116 | ● | ● | $V_{CC}$ | ● | | Gnd |
| 38.182 | ● | $V_{CC}$ | $V_{CC}$ | ● | | Gnd |
| 39.064 | ● | $V_{CC}$ | ● | | | Gnd |

## CROWBAR SCR CONSIDERATIONS

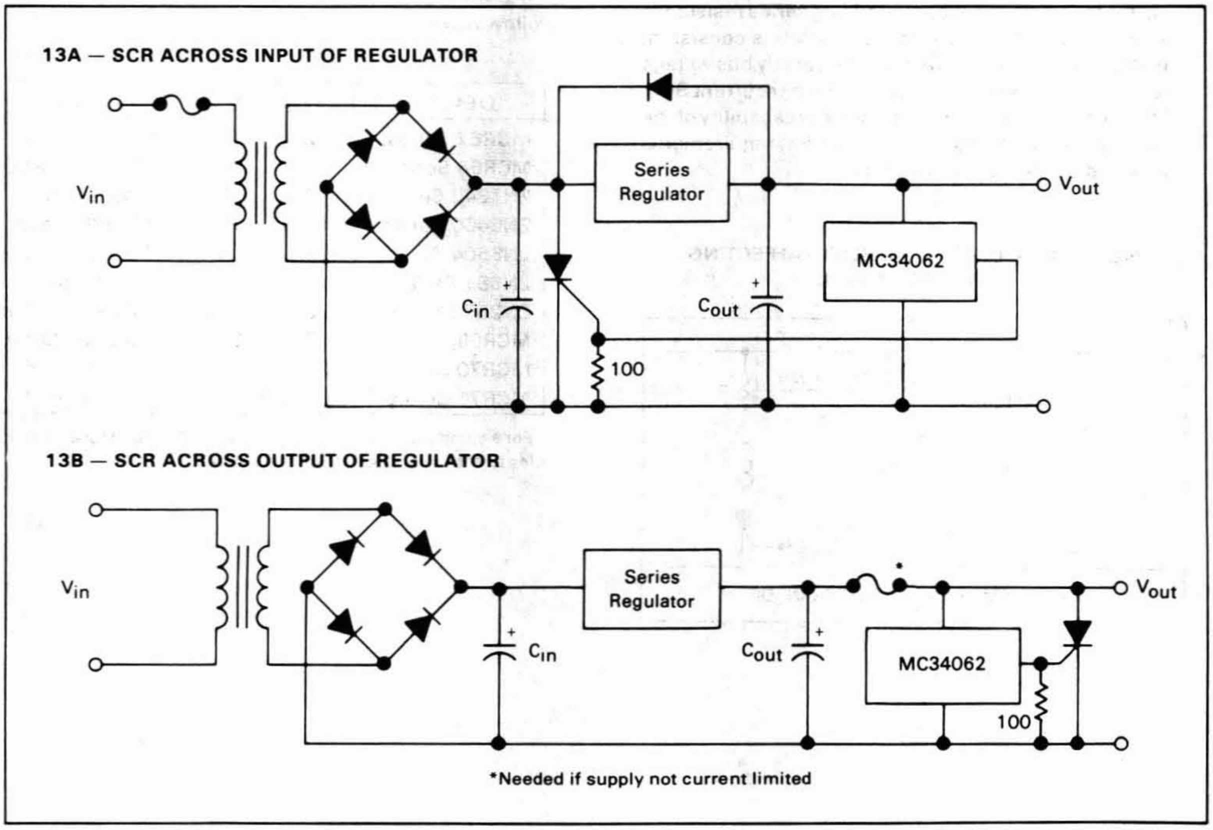
Referring to Figure 13, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, $C_{out}$. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 13A, the supply's input filter capacitors. This surge current is illustrated in Figure 14, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or $I^2t$. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

### 1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

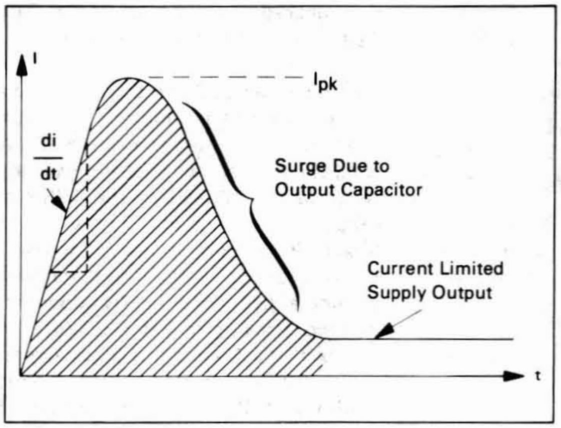
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times $I_{GT}$) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/μs, assuming a gate current of five times $I_{GT}$ and $<1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 15. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 13 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS



*Needed if supply not current limited

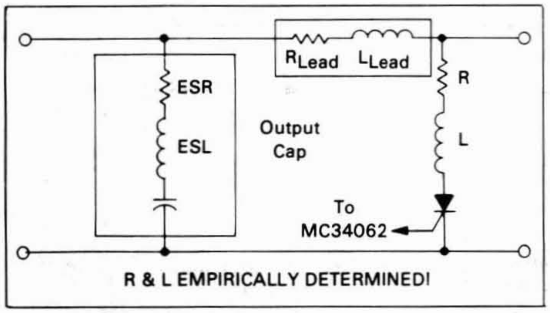
FIGURE 14 — CROWBAR SCR SURGE CURRENT WAVEFORM



### 2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 15) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 15 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



## A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 13A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an $I^2t$ rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 13B.

## CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

| DEVICE | $I_{RMS}$ | $I_{FSM}$ | PACKAGE |
|---|---|---|---|
| MCR67 Series | 12 A | 100 A | Metal Stud |
| MCR68 Series | 12 A | 100 A | TO-220 Plastic |
| 2N1842 Series | 16 A | 125 A | Metal Stud |
| 2N6400 Series | 16 A | 160 A | TO-220 Plastic |
| 2N6504 Series | 25 A | 160 A | TO-220 Plastic |
| 2N681 Series | 25 A | 200 A | Metal Stud |
| 2N2573 Series | 25 A | 260 A | TO-3 Metal Can |
| MCR69 Series | 25 A | 300 A | TO-220 Plastic |
| MCR70 Series | 35 A | 350 A | Metal Stud |
| MCR71 Series | 55 A | 550 A | Metal Stud |

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

**MOTOROLA**

# CA3059
# CA3079

## ZERO VOLTAGE SWITCHES

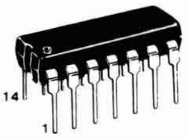
. . . designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V @ 50/60 Hz.

**Applications:**

- Relay Control
- Heater Control
- Valve Control
- Lamp Control
- Synchronous Switching of Flashing Lights
- On-Off Motor Switching
- Differential Comparator With Self-Contained Power Supply for Industrial Applications
- Photosensitive Control
- Power One-Shot Control

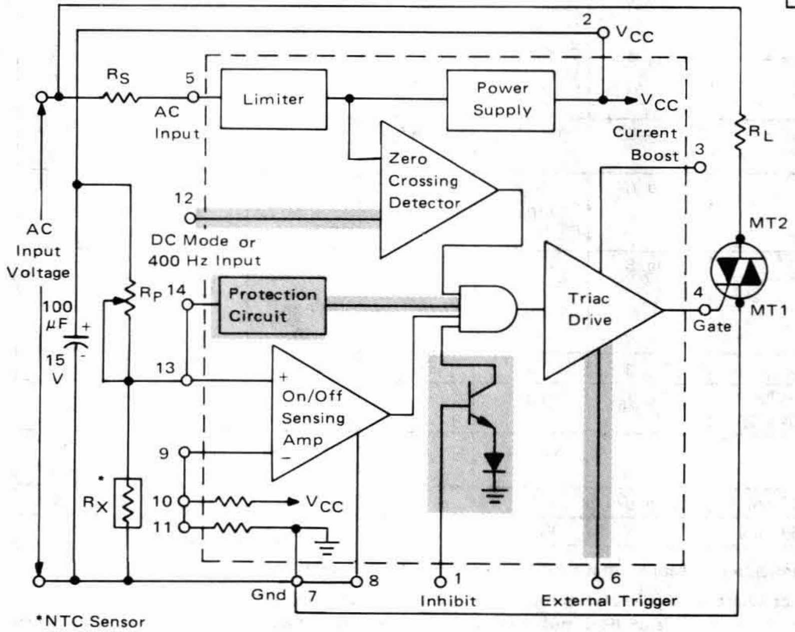
## ZERO VOLTAGE SWITCHES

### SILICON MONOLITHIC INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 646-05

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



2
$V_{CC}$
$R_S$
5
AC Input
Limiter
Power Supply
$V_{CC}$
Current Boost
3
$R_L$
Zero Crossing Detector
12
DC Mode or 400 Hz Input
MT2
AC Input Voltage
$R_P$
14
Protection Circuit
Triac Drive
4
Gate
MT1
100 µF
15 V
13
On/Off Sensing Amp
9
$R_X$
10
$V_{CC}$
11
8
Gnd
7
1
Inhibit
6
External Trigger

*NTC Sensor

NOTE: Shaded Area Not Included With CA3079.

TABLE A

| AC Input Voltage (50/60 Hz) vac | Input Series Resistor ($R_S$) kΩ | Dissipation Rating for $R_S$ W |
|---|---|---|
| 24 | 2.0 | 0.5 |
| 120 | 10 | 2.0 |
| 208/230 | 20 | 4.0 |
| 277 | 25 | 5.0 |

### FUNCTIONAL BLOCK DESCRIPTION

1. **Limiter-Power Supply** — Allows operation of the CA3059/79 directly from an ac line. Suggested dropping resistor ($R_S$) values are given in Table A.

2. **Differential On/Off Sensing Amplifier** — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented using this block.

3. **Zero-Crossing Detector** — Synchronizes the output pulses to the zero voltage point of the ac cycle. This synchronization eliminates RFI when used with resistive loads.

4. **Triac Drive** — Supplies high-current pulses to the external power controlling thyristor.

5. **Protection Circuit (CA3059 only)** — A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive current from the external triac.

6. **Inhibit Capability (CA3059 only)** — Thyristor firing may be inhibited by the action of an internal diode gate at Pin 1.

7. **High Power DC Comparator Operation (CA3059 only)** — Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector). When Pin 13 is positive with respect to Pin 9, current to the thyristor is continuous.

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| DC Supply Voltage<br>(Between Pins 2 and 7 | <br>CA3059<br>CA3079 | $V_{CC}$ | <br>12<br>10 | Vdc |
| DC Supply Voltage<br>(Between Pins 2 and 8) | <br>CA3059<br>CA3079 | $V_{CC}$ | <br>12<br>10 | Vdc |
| Peak Supply Current (Pins 5 and 7) | | $I_{5,7}$ | ±50 | mA |
| Fail-Safe Input Current (Pin 14) | | $I_{14}$ | 2.0 | mA |
| Output Pulse Current (Pin 4) | | $I_{out}$ | 150 | mA |
| Junction Temperature | | $T_J$ | 150 | °C |
| Operating Temperature Range | | $T_A$ | -40 to +85 | °C |
| Storage Temperature Range | | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** (Operation @ 120 Vrms, 50-60 Hz, $T_A$ = 25°C)**

| Characteristic | | Test Circuits | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| DC Supply Voltage | | Fig. 2 | $V_S$ | | | | Vdc |
| Inhibit Mode | | | | | | | |
| $R_S$ = 10 k, $I_L$ = 0 | | | | 6.1 | 6.5 | 7.0 | |
| $R_S$ = 5.0 k, $I_L$ = 2.0 mA | | | | – | 6.1 | – | |
| Pulse Mode | | | | | | | |
| $R_S$ = 10 k, $I_L$ = 0 | | | | 6.0 | 6.4 | 7.0 | |
| $R_S$ = 5.0 k, $R_L$ = 2.0 mA | | | | – | 6.2 | – | |
| Gate Trigger Current<br>($V_{GT}$ = 1.0 V, Pins 3 and 2 connected) | | Fig. 3 | $I_{GT}$ | – | 160 | – | mA |
| Peak Output Current, Pulsed | | Fig. 3 | $I_{OM}$ | | | | mA |
| With Internal Power Supply, $V_{GT}$ = 0 | | | | | | | |
| Pin 3 Open | | | | 50 | 125 | – | |
| Pins 3 and 2 Connected | | | | 90 | 190 | – | |
| With External Power Supply, $V_{CC}$ = 12 V, $V_{GT}$ = 0 | | Fig. 4 | | | | | |
| Pin 3 Open | | | | – | 230 | – | |
| Pins 3 and 2 Connected | | | | – | 300 | – | |
| Inhibit Input Ratio<br>(Ratio of Voltage @ Pin 9 to Pin 2) | | Fig. 5 | $V_9/V_2$ | 0.465 | 0.485 | 0.520 | – |
| Total Gate Pulse Duration ($C_{Ext}$ = 0) | | Fig. 6 | | | | | μs |
| Positive dv/dt | | | tp | 70 | 100 | 140 | |
| Negative dv/dt | | | tn | 70 | 100 | 140 | |
| Pulse Duration After Zero Crossing<br>($C_{Ext}$ = 0, $R_{Ext}$ = ∞) | | Fig. 6 | | | | | μs |
| Positive dv/dt | | | $tp_1$ | – | 50 | – | |
| Negative dv/dt | | | $tn_1$ | – | 60 | – | |
| Output Leakage Current Inhibit Mode*** | | Fig. 3 | $I_4$ | – | 0.001 | 10 | μA |
| Input Bias Current | CA3059 | Fig. 7 | $I_{IB}$ | – | 0.15 | 1.0 | μA |
| | CA3079 | | | – | 0.15 | 2.0 | |
| Common Mode Input Voltage Range<br>(Pins 9 and 13 Connected) | | – | $V_{CMR}$ | – | 1.4 to 5.0 | – | Vdc |
| Inhibit Input Voltage | CA3059 only | Fig. 8 | $V_1$ | – | 1.4 | 1.6 | Vdc |
| External Trigger Voltage | CA3059 only | – | $V_6$-$V_4$ | – | 1.4 | – | Vdc |

*Care must be taken, especially when using an external power supply, that total package dissipation is not exceeded.

**The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration test. However, the series resistor ($R_S$) must have the indicated value, shown in Table A for the specified input voltage.

***$I_4$ out of Pin 4
2 V on Pin 1
S1 position 2

## TEST CIRCUITS

(All resistor values are in ohms)

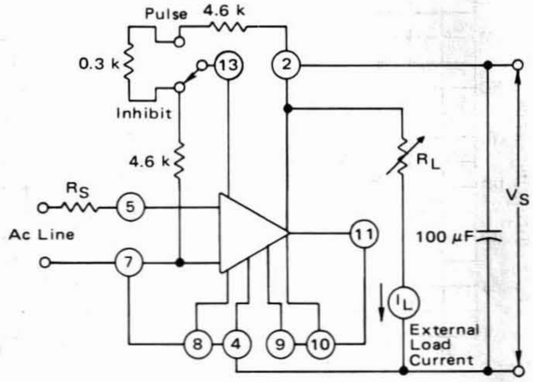


FIGURE 2 – DC SUPPLY VOLTAGE

Pulse
4.6 k
0.3 k
Inhibit
13
2
4.6 k
RL
VS
RS
5
Ac Line
7
11
100 μF
IL
External Load Current
8
4
9
10

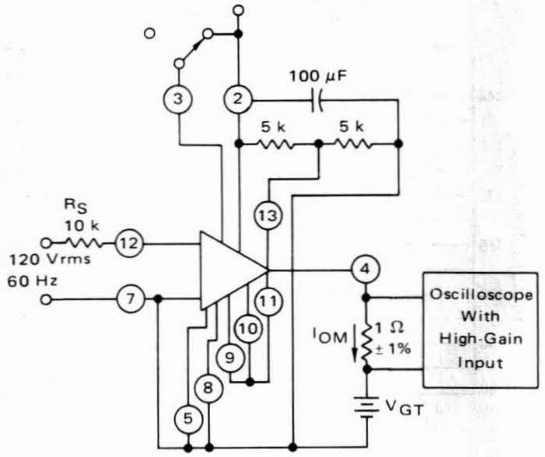


FIGURE 4 – PEAK OUTPUT CURRENT (PULSED) WITH EXTERNAL POWER SUPPLY

3
2
100 μF
5 k
5 k
13
RS
10 k
12
120 Vrms
60 Hz
7
11
10
9
8
5
4
IOM
1 Ω
± 1%
Oscilloscope With High-Gain Input
VGT

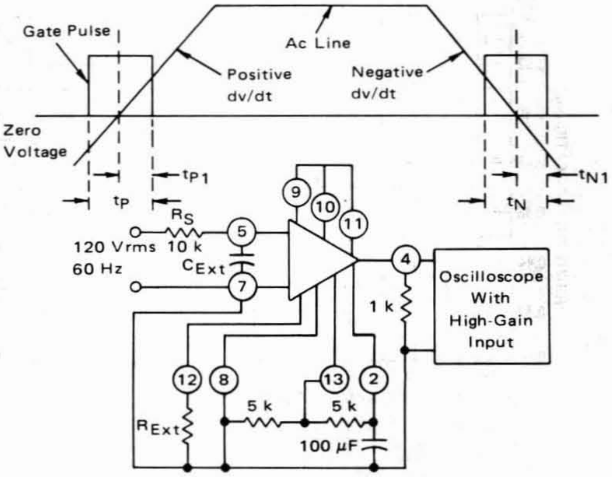


FIGURE 6 – GATE PULSE DURATION TEST CIRCUIT WITH ASSOCIATED WAVEFORM

Gate Pulse
Ac Line
Positive dv/dt
Negative dv/dt
Zero Voltage
tP1
tP
tN
tN1
9
10
11
RS
5
120 Vrms
10 k
60 Hz
CExt
7
4
1 k
Oscilloscope With High-Gain Input
12
8
13
2
RExt
5 k
5 k
100 μF

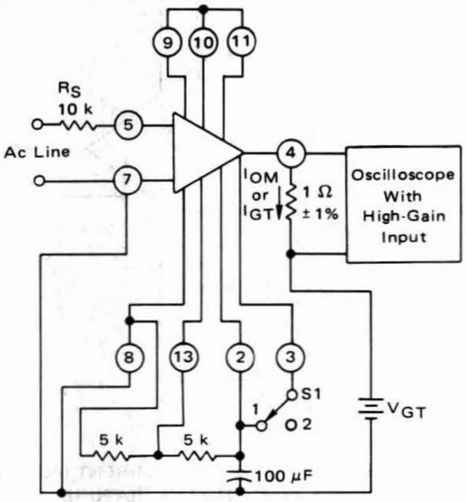


FIGURE 3 – PEAK OUTPUT (PULSED) AND GATE TRIGGER CURRENT WITH INTERNAL POWER SUPPLY

9
10
11
RS
10 k
5
Ac Line
7
4
IOM or IGT
1 Ω
± 1%
Oscilloscope With High-Gain Input
8
13
2
3
S1
1
2
VGT
5 k
5 k
100 μF

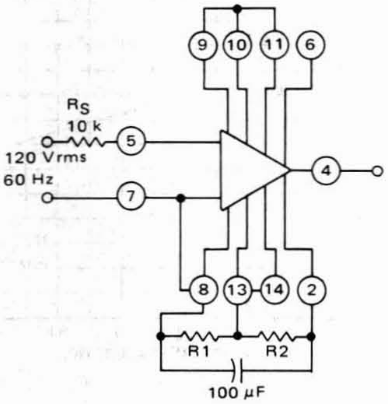
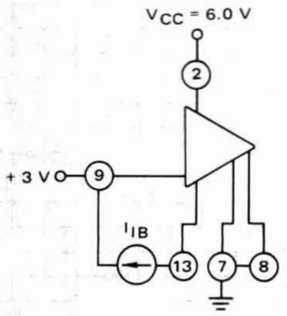


FIGURE 5 – INPUT INHIBIT RATIO

9
10
11
6
RS
10 k
5
120 Vrms
60 Hz
7
4
8
13
14
2
R1
R2
100 μF

FIGURE 7 – INPUT BIAS CURRENT TEST CIRCUIT



VCC = 6.0 V
2
+ 3 V
9
IIB
13
7
8

## TYPICAL CHARACTERISTICS

FIGURE 8 – INHIBIT INPUT VOLTAGE TEST

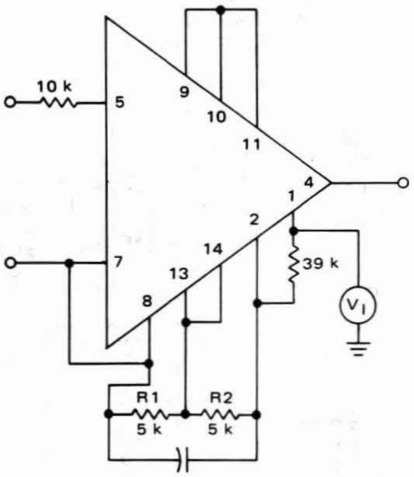


FIGURE 9 – PEAK OUTPUT CURRENT (PULSED) versus EXTERNAL POWER SUPPLY VOLTAGE

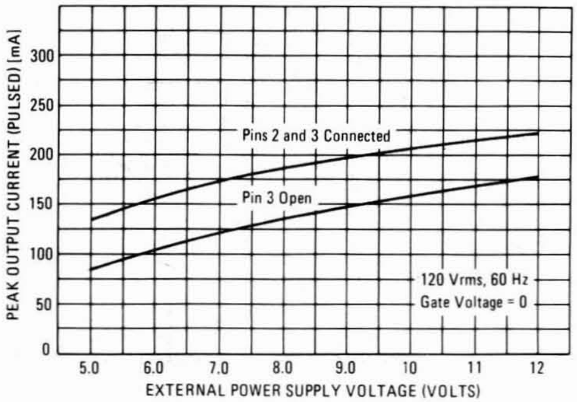


FIGURE 10 – PEAK OUTPUT CURRENT (PULSED) versus AMBIENT TEMPERATURE

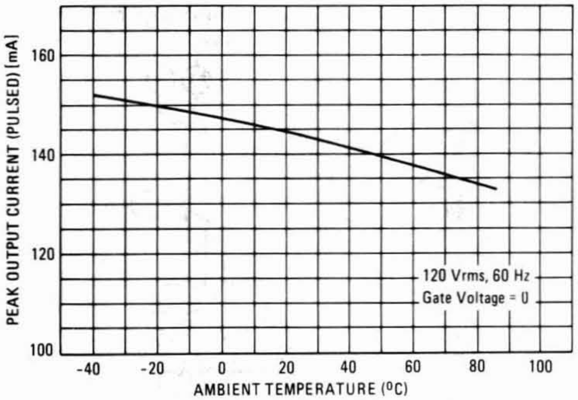


FIGURE 11 – TOTAL PULSE WIDTH versus AMBIENT TEMPERATURE

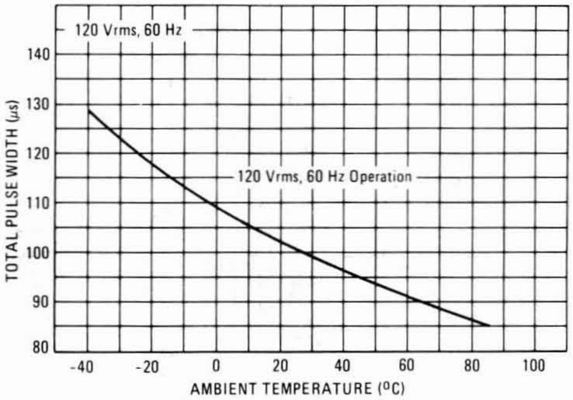


FIGURE 12 – INTERNAL SUPPLY versus AMBIENT TEMPERATURE

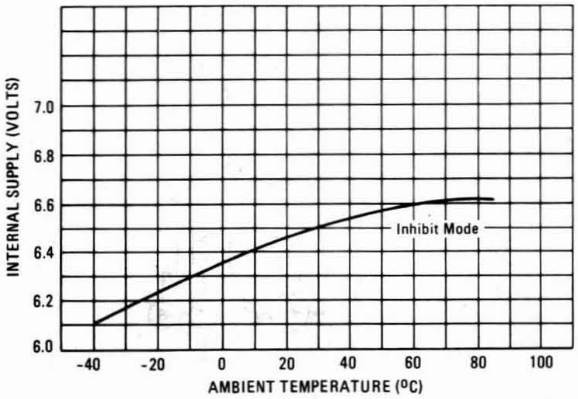


FIGURE 13 – INHIBIT VOLTAGE RATIO versus AMBIENT TEMPERATURE

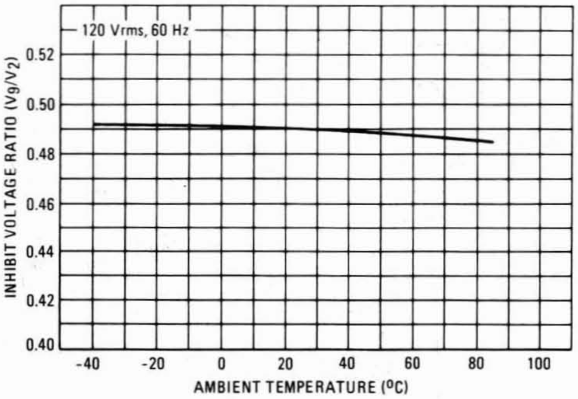
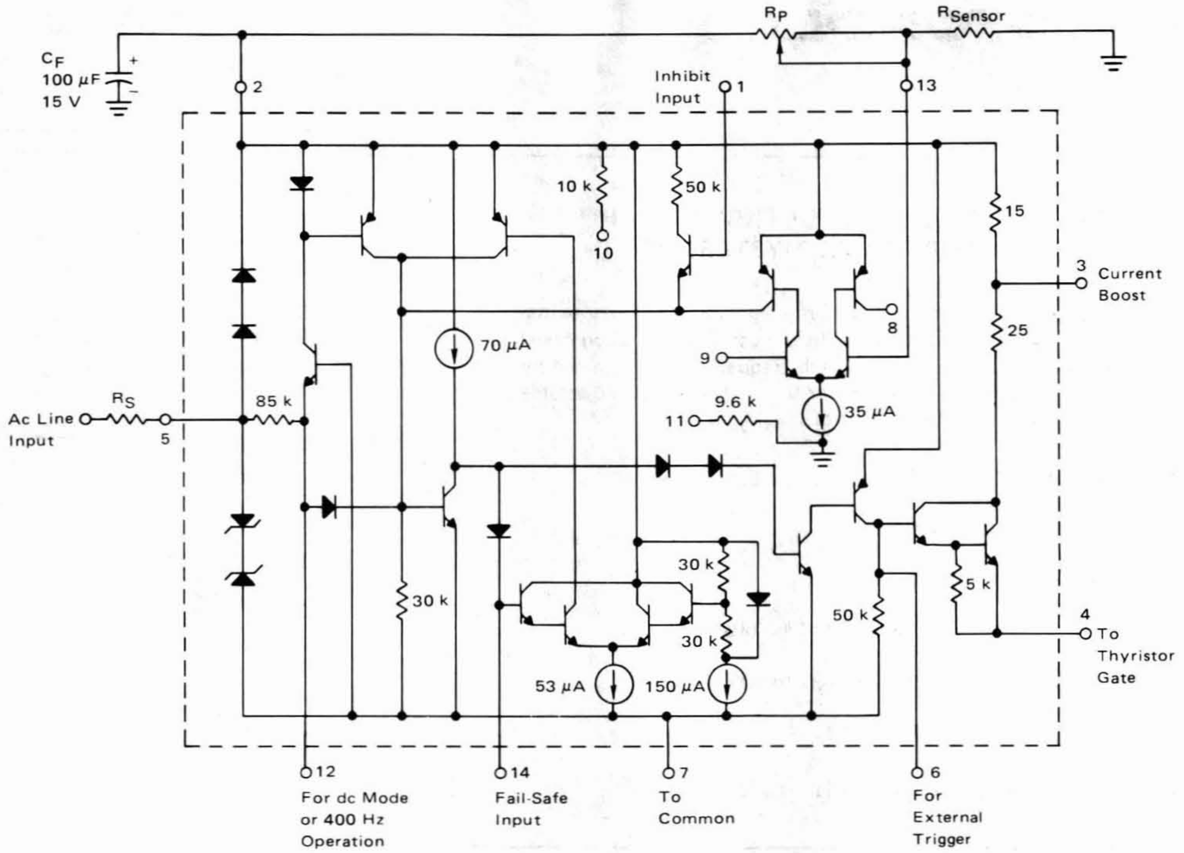


FIGURE 14 – CIRCUIT SCHEMATIC


$R_P$
$R_{Sensor}$
$C_F$
100 µF
15 V
+
2
Inhibit Input
1
13
10 k
50 k
15
10
3
Current Boost
70 µA
8
25
9
$R_S$
Ac Line Input
5
85 k
9.6 k
11
35 µA
30 k
5 k
50 k
4
To Thyristor Gate
30 k
30 k
53 µA
150 µA
12
For dc Mode or 400 Hz Operation
14
Fail-Safe Input
7
To Common
6
For External Trigger

NOTE: Current sources are established by an internal reference.
Pins 1, 6, 12, and 14 are not used with CA3079.

## APPLICATION INFORMATION

### Power Supply

The CA3059 and CA3079 are self-powered circuits, powered from the ac line through an appropriate dropping resistor (see Table A). The internal supply is designed to power the auxiliary power circuits.

In applications where more output current from the internal supply is required, an external power supply of higher voltage should be used. To use an external power supply, connect pin 5 and pin 7 together and apply the synchronizing voltage to pin 12 and the dc supply voltage to pin 2 as shown in Figure 4.

### Operation of Protection Circuit (CA3059 Only)

The protection circuit, when connected, will remove current drive from the triac if an open or shorted sensor is detected. This circuit is activated by connecting pin 13 to pin 14 (see Figure 1).

The following conditions should be observed when the protection circuit is utilized:

A. The internal supply should be used and the external load current must be limited to 2 mA with a 5 kΩ dropping resistor.

B. Sensor Resistance $(R_X)$ and $R_P$ values should be between 2 kΩ and 100 kΩ.

C. The relationship $0.33 < R_X/R_P < 3$ must be met over the anticipated temperature range to prevent undesired activation of the circuit. A shunt or series resistor may have to be added.

### External Inhibit Function (CA3059 Only)

A priority inihibit command applied to pin 1 will remove current drive from the thyristor. A command of at least +1.2 V @ 10 µA is required. A DTL or $T^2L$ logic 1 applied to pin 1 will activate the inhibit function.

### DC Gate Current Mode (CA3059 Only)

When comparator operation is desired or inductive loads are being switched, pins 7 and 12 should be connected. This connection disables the zero-crossing detector to permit the flow of gate current from the differential sensing amplifier on demand. Care should be exercised to avoid possible overloading of the internal power supply when operating the device in this mode. A resistor should be inserted between pin 4 and the thyristor gate in order to limit the current.

**MOTOROLA**

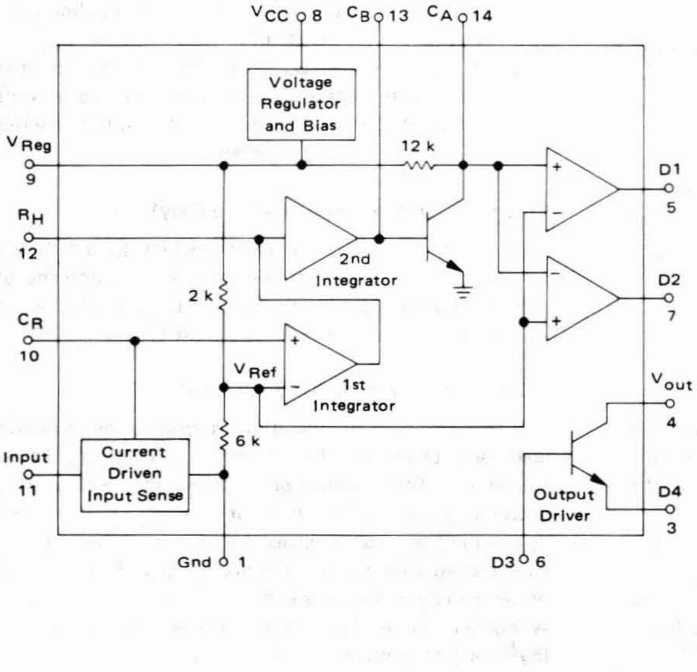
# MC3344

## PROGRAMMABLE FREQUENCY SWITCH WITH ADJUSTABLE HYSTERESIS

The MC3344 is a general purpose programmable frequency switch designed for use in systems where a load must be switched on or off at a predetermined frequency. Switch frequency is determined by an external resistor ($R_R$) and capacitor ($C_R$). Hysteresis is adjustable and determined by an external resistor ($R_H$).

- Isolated Driver Transistor
- Complementary Outputs
- Adjustable Hysteresis
- Wide Supply Operating Range (7 to 24 Volts)
- Wide Input Frequency Range (10 Hz to 100 kHz)
- Internal Regulator
- Ideal for Automotive and Industrial Applications

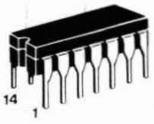
FIGURE 1 – CIRCUIT BLOCK DIAGRAM



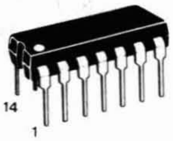
$V_{CC}$ 8
$C_B$ 13
$C_A$ 14
Voltage Regulator and Bias
$V_{Reg}$ 9
12 k
$R_H$ 12
2nd Integrator
D1 5
D2 7
2 k
$C_R$ 10
$V_{Ref}$
1st Integrator
$V_{out}$ 4
6 k
Input 11
Current Driven Input Sense
Output Driver
D4 3
Gnd 1
D3 6

## PROGRAMMABLE FREQUENCY SWITCH

### SILICON MONOLITHIC INTEGRATED CIRCUIT

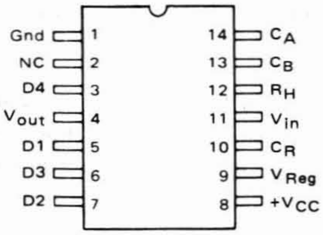


**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

PIN CONNECTIONS



Gnd 1
NC 2
D4 3
$V_{out}$ 4
D1 5
D3 6
D2 7
14 $C_A$
13 $C_B$
12 $R_H$
11 $V_{in}$
10 $C_R$
9 $V_{Reg}$
8 $+V_{CC}$

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC3344L | −40°C to +85°C | Ceramic DIP |
| MC3344P | −40°C to +85°C | Plastic DIP |

**MAXIMUM RATINGS** ($T_A = 25^oC$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply | $V_{CC}$ | 24 | Vdc |
| Peak Input Current | $I_I$ | 10 | mA |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | -40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A = 25^oC$, $V_{CC}$ = +15 Vdc unless otherwise specified)

| Characteristic | Test Ckts | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Current | 2 | $I_D$ | – | 2.5 | 4.0 | mA |
| Trigger Reset Voltage | 3 | | | | | Vdc |
| $I_{in}$ = 200 µA | | $V_{CR1}$ | 0.25 | – | – | |
| $I_{in}$ = 600 µA | | $V_{CR2}$ | – | – | 0.125 | |
| Regulator Output Voltage | 4 | $V_{Reg}$ | 4.0 | 5.1 | 5.8 | Vdc |
| Threshold Output Voltage $V_{TCR} = V_{CR}/V_{Reg}$ | 5 | $V_{TCR}$ | 0.739 | 0.750 | 0.761 | V/V |
| Hysteresis Sink Current | 6 | $I_H$ | 100 | 400 | – | µA |
| Second Comparator Output | 7 | | | | | |
| D1 Leakage | | $I_{D1L}$ | – | – | 100 | nA |
| D2 Source | | $I_{D2S}$ | 100 | 250 | – | µA |
| D1 Source | | $I_{D1S}$ | 100 | 200 | – | µA |
| D2 Leakage | | $I_{D2L}$ | – | – | 100 | nA |
| Output Driver Gain $I_C$ = 5.0 mA | 8 | $h_{FE1}$ | 50 | 100 | – | – |
| Output Driver Voltage Standoff $I_D$ = 5.0 mA | 9 | $V_{(BR)CEO}$ | 25 | 30 | – | Vdc |
| Integrator Transistor Gain $h_{FE2} = \Delta I_C/\Delta I_B$, $I_{C1}$ = 0.4 mA, $I_{C2}$ = 0.6 mA | 10 | $h_{FE2}$ | 50 | 200 | 300 | – |

## TEST CIRCUITS

FIGURE 2 – SUPPLY CURRENT

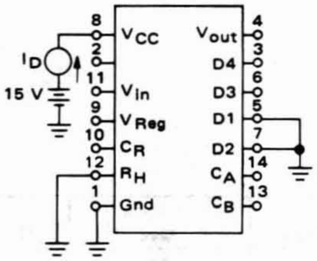
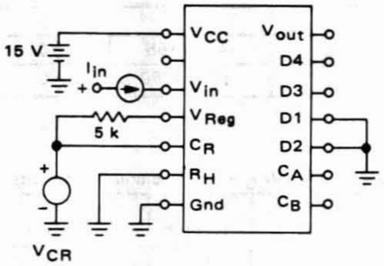

8
VCC
2
11
Vin
9
VReg
10
CR
12
RH
1
Gnd
ID
15 V
4
Vout
3
D4
6
D3
5
D1
7
D2
14
CA
13
CB

FIGURE 3 – TRIGGER RESET VOLTAGE


15 V
Iin
+
5 k
+
–
VCR
VCC
Vin
VReg
CR
RH
Gnd
Vout
D4
D3
D1
D2
CA
CB

$I_{in}$ = 200 µA, $V_{CR} \geq 0.125$ V

$I_{in}$ = 600 µA, $V_{CR} \leq 0.125$ V

FIGURE 4 – REGULATOR OUTPUT VOLTAGE

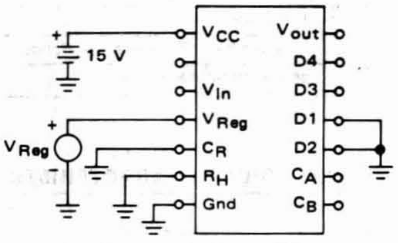
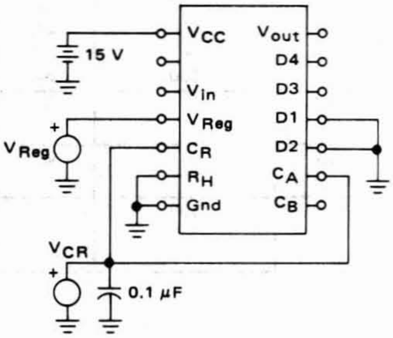

+
15 V
+
VReg
VCC
Vin
VReg
CR
RH
Gnd
Vout
D4
D3
D1
D2
CA
CB

FIGURE 5 – THRESHOLD VOLTAGE RATIO


15 V
+
VReg
VCR
+
0.1 µF
VCC
Vin
VReg
CR
RH
Gnd
Vout
D4
D3
D1
D2
CA
CB

$V_{TCR} = V_{CR}/V_{Reg}$

FIGURE 6 – HYSTERESIS SINK CURRENT

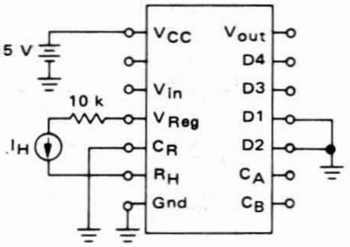
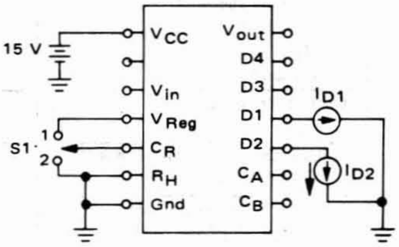

15 V
10 k
IH
VCC
Vin
VReg
CR
RH
Gnd
Vout
D4
D3
D1
D2
CA
CB

FIGURE 7 – $I_{D1L}/I_{D2S}$, $I_{D2L}/I_{D1S}$


15 V
S1
1
2
ID1
ID2
VCC
Vin
VReg
CR
RH
Gnd
Vout
D4
D3
D1
D2
CA
CB

$I_{D1L}/I_{D2S}$ – S1 in position 1

$I_{D2L}/I_{D1S}$ – S1 in position 2

FIGURE 8 – OUTPUT DRIVER GAIN

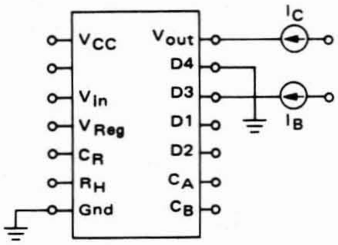

IC
IB
VCC
Vin
VReg
CR
RH
Gnd
Vout
D4
D3
D1
D2
CA
CB

FIGURE 9 – $BV_{CEO}$ OF OUTPUT TRANSISTOR

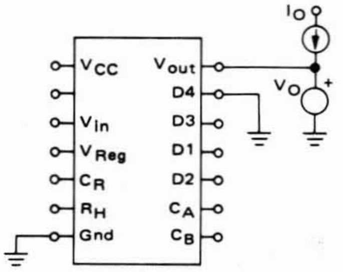
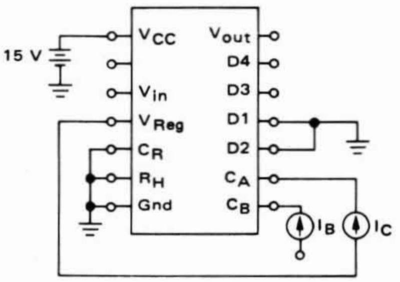

IO
VO
+
VCC
Vin
VReg
CR
RH
Gnd
Vout
D4
D3
D1
D2
CA
CB

FIGURE 10 – INTEGRATOR TRANSISTOR GAIN


15 V
IB
IC
VCC
Vin
VReg
CR
RH
Gnd
Vout
D4
D3
D1
D2
CA
CB

## APPLICATIONS INFORMATION

The voltage regulator and bias section provides the proper biasing and regulated supply voltage to the integrated circuit.

A square wave, when applied to the RC differentiator, provides input current pulses to the IC. The input circuit discharges and clamps, for a predetermined time, the voltage across capacitor $C_R$. This establishes the initial ramp voltage ($V_{sat}$) and allows initiation of a new voltage ramp after each positive transition of the input waveform.

The voltage, $V_{CR}$, ramps from $V_{sat}$ to the final value, $V_{Reg}$, charging through $R_R$.

If $V_{CR}$ is never allowed to reach $V_{Ref}$ due to quick reset pulses, the second integrator amplifier will not be activated, and capacitor $C_{AB}$ is allowed to charge through the 12 kΩ resistor until $V_{CA}$ is greater than $V_{Ref}$. At this point, D1 will switch ON and D2 will switch OFF. By connecting either D1 or D2 to the D3 drive pin, the output drive transistor may be either switched ON or OFF at the switch point.

If $V_{CR}$ is allowed to ramp above $V_{Ref}$ before being reset, the second integrator amplifier is driven ON which discharges and resets capacitor $C_{AB}$ keeping $V_{CA}$ low with respect to $V_{Ref}$.

$V_{CA}$ will always be low with respect to $V_{Ref}$ if the time from reset $C_R$ to $V_{CR} = V_{Ref}$ is less than the time from reset $C_{AB}$ to $V_{CA} = V_{Ref}$.

Resistor $R_H$ provides hysteresis around the switch point (i.e., frequency to switch the output driver ON, when connected to the D1 terminal, is higher than the frequency required to switch the output driver OFF). If no hysteresis is desired then the $R_H$ resistor should be omitted and pin 12 grounded.

Circuit Equations:

The first integrator time constant is $T1 = R_H \parallel R_R\ C_R$. If $R_H$ is omitted then $T1 = R_R\ C_R$.

The second integrator time constant is $T2 = (12\ k)\ (h_{FE2})\ (C_{AB})$.

$$f1 = \text{Switch Point frequency} \cong \frac{1}{1.39\ R_R\ C_R}$$

$$f2 = \text{Hysteresis Switch Point frequency} \approx \frac{1}{R_R \parallel R_H\ C_R\ \ln\left[\dfrac{R_H}{0.25\ R_H - 0.75\ R_R}\right]}$$

FIGURE 11 – TYPICAL APPLICATION

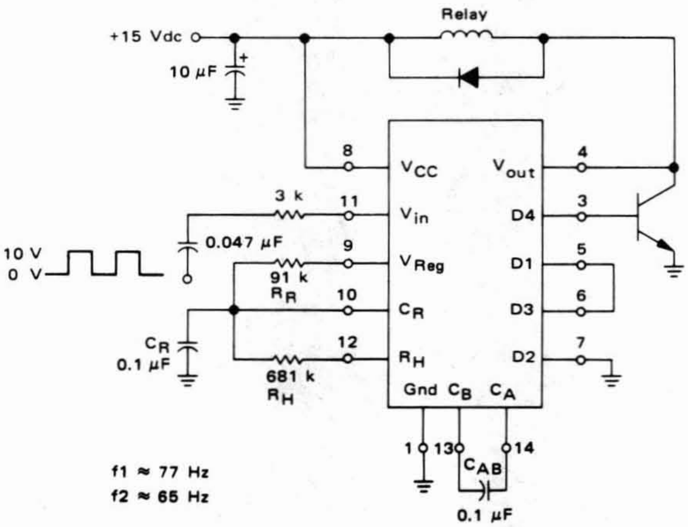
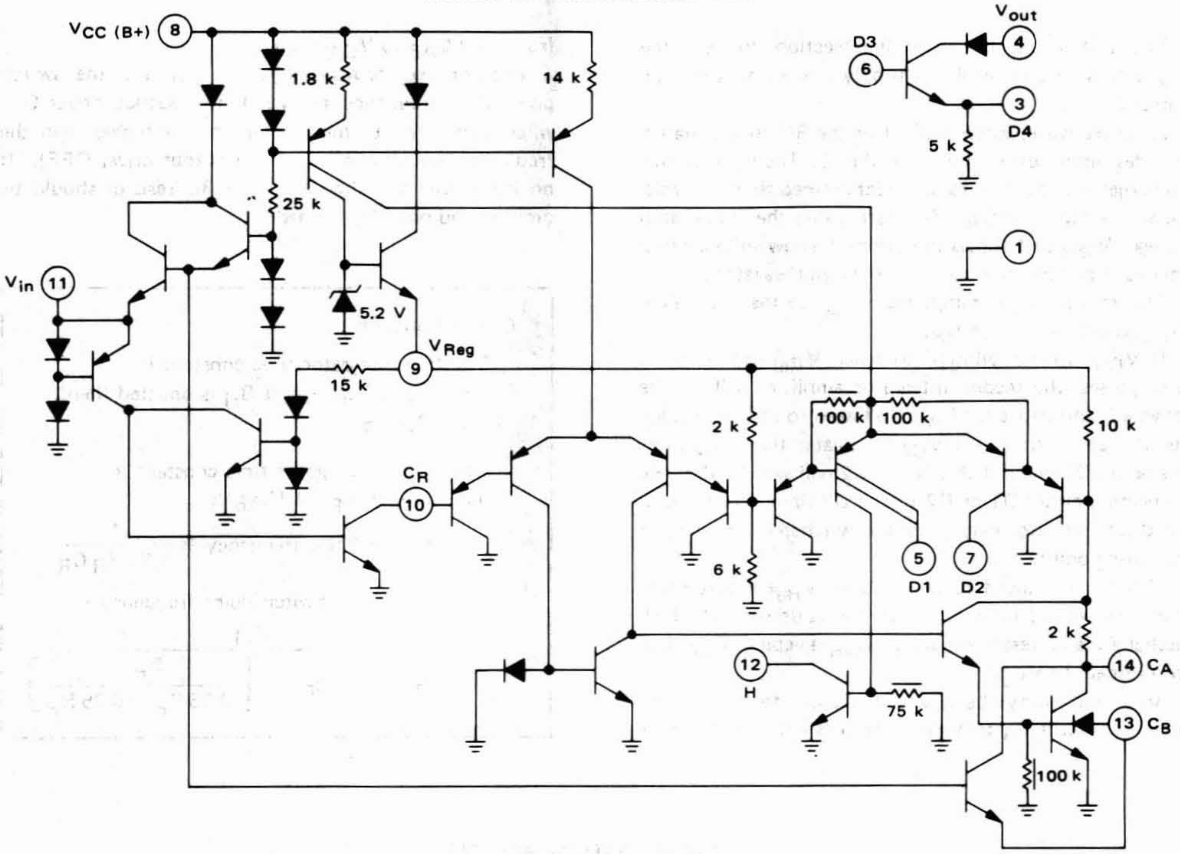


FIGURE 12 — CIRCUIT SCHEMATIC


VCC (B+)
8
1.8 k
14 k
Vout
D3
6
4
3
D4
5 k
1
25 k
Vin
11
5.2 V
VReg
9
15 k
2 k
100 k
100 k
10 k
CR
10
6 k
5
7
D1
D2
2 k
14
CA
12
H
75 k
13
CB
100 k

**MOTOROLA**

# MC3479P

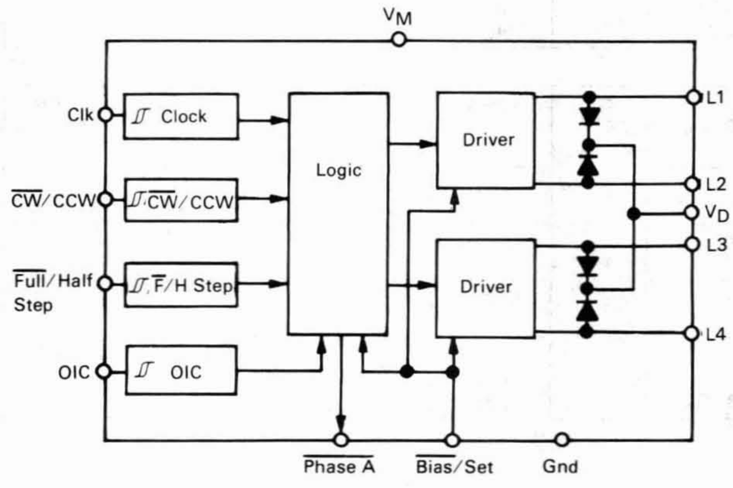
## Advance Information

### STEPPER MOTOR DRIVER

The MC3479P is designed to drive a two-phase stepper motor in the bipolar mode. The circuit consists of four input sections, a logic decoding/sequencing section, two driver-stages for the motor coils, and an output to indicate the Phase A drive state.

- Single Supply Operation — +7.2 to +16.5 Volts
- 350 mA/Coil Drive Capability
- Clamp Diodes Provided for Back-EMF Suppression
- Selectable $\overline{\text{CW}}$/CCW and $\overline{\text{Full}}$/Half Step Operation
- Selectable High/Low Output Impedance (Half Step Mode)
- TTL/CMOS Compatible Inputs
- Input Hysteresis — 400 mV Minimum
- Phase Logic Can Be Initialized to $\overline{\text{Phase A}}$
- $\overline{\text{Phase A}}$ Output Drive State Indication (Open-Collector)

FIGURE 1 — BLOCK DIAGRAM

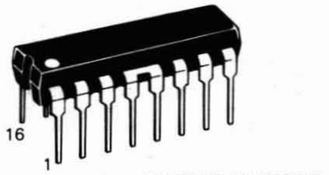


VM
Clk
Clock
CW/CCW
CW/CCW
Full/Half Step
F/H Step
OIC
OIC
Logic
Driver
Driver
L1
L2
VD
L3
L4
Phase A
Bias/Set
Gnd

This document contains information on a new product. Specifications and information herein are subject to change without notice.

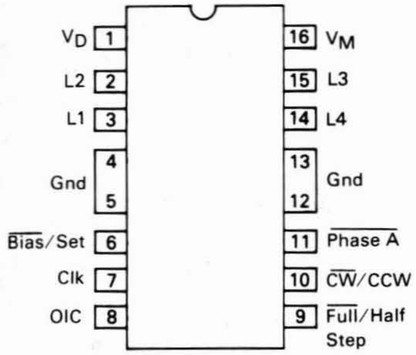
### STEPPER MOTOR DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
**CASE 648C**

### PIN ASSIGNMENT



VD 1
L2 2
L1 3
Gnd 4
5
Bias/Set 6
Clk 7
OIC 8
16 VM
15 L3
14 L4
13 Gnd
12
11 Phase A
10 CW/CCW
9 Full/Half Step

### INPUT TRUTH TABLE

| | Input Low | Input High |
|---|---|---|
| $\overline{\text{CW}}$/CCW | CW | CCW |
| $\overline{\text{Full}}$/Half Step | Full Step | Half Step |
| OIC | Hi Z | Low Z |
| Clk | Positive Edge Triggered | |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_M$ | +18 | Vdc |
| Clamp Diode Cathode Voltage (Pin 1) | $V_D$ | $V_M + 5.0$ | Vdc |
| Driver Output Voltage (Pins 2, 3, 14, 15) | $V_{OD}$ | $V_M + 6.0$ | Vdc |
| Driver Output Current/Coil | $I_{OD}$ | ±500 | mA |
| Input Voltage (Pins 7, 8, 9, 10) | $V_{in}$ | −0.5 to +7.0 | Vdc |
| $\overline{\text{Bias}}$/Set Current (Pin 6) | $I_{BS}$ | −10 | mA |
| $\overline{\text{Phase A}}$ Output Voltage (Pin 11) | $V_{OA}$ | +18 | Vdc |
| $\overline{\text{Phase A}}$ Sink Current (Pin 11) | $I_{OA}$ | 20 | mA |
| Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

*"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Electrical Characteristics" tables provide conditions for actual device operation.

## RECOMMENDED OPERATING CONDITIONS

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_M$ | +7.2 | +16.5 | Vdc |
| Clamp Diode Cathode Voltage | $V_D$ | $V_M$ | $V_M + 4.5$ | Vdc |
| Driver Output Current (Per Coil) (Note 5) | $I_{OD}$ | — | 350 | mA |
| Input Voltage (Pins 7, 8, 9, 10) | $V_{in}$ | 0 | +5.5 | Vdc |
| $\overline{\text{Bias}}$/Set Current (Outputs Active) | $I_{BS}$ | −300 | −75 | µA |
| $\overline{\text{Phase A}}$ Output Voltage | $V_{OA}$ | — | $V_M$ | Vdc |
| $\overline{\text{Phase A}}$ Sink Current | $I_{OA}$ | 0 | 8.0 | mA |
| Operating Ambient Temperature | $T_A$ | 0 | +70 | °C |

## DC ELECTRICAL CHARACTERISTICS

(Specifications apply over the recommended supply voltage and temperature ranges unless otherwise noted.) (See Notes 1, 2)

| Characteristic | Pins | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT LOGIC LEVELS** | | | | | | |
| Threshold Voltage (Low-to-High) | 7, 8, 9, 10 | $V_{TLH}$ | — | — | 2.0 | Vdc |
| Threshold Voltage (High-to-Low) | | $V_{THL}$ | 0.8 | — | — | Vdc |
| Hysteresis | | $V_{HYS}$ | 0.4 | — | — | Vdc |
| Current ($V_I = 0.4$ V) | | $I_{IL}$ | −100 | — | — | µA |
| ($V_I = 5.5$ V) | | $I_{IH1}$ | — | — | +100 | |
| ($V_I = 2.7$ V) | | $I_{IH2}$ | — | — | +20 | |
| **DRIVER OUTPUT LEVELS** | | | | | | |
| Output High Voltage ($I_{BS} = -300$ µA) ($I_{OD} = -350$ mA) | 2, 3, 14, 15 | $V_{OHD}$ | $V_M - 2.0$ | — | — | Vdc |
| ($I_{OD} = -0.1$ mA) | | | $V_M - 1.2$ | — | — | |
| Output Low Voltage ($I_{BS} = -300$ µA, $I_{OD} = 350$ mA) | | $V_{OLD}$ | — | — | 0.8 | Vdc |
| Differential Mode Output Voltage Difference (Note 3) ($I_{BS} = -300$ µA, $I_{OD} = 350$ mA) | | $DV_{OD}$ | — | — | 0.15 | Vdc |
| Common Mode Output Voltage Difference (Note 4) ($I_{BS} = -300$ µA, $I_{OD} = -0.1$ mA) | | $CV_{OD}$ | — | — | 0.15 | Vdc |
| Output Leakage — Hi Z State ($0 \leqslant V_{OD} \leqslant V_M$, $I_{BS} = -5.0$ µA) | | $I_{OZ1}$ | −100 | — | +100 | µA |
| ($0 \leqslant V_{OD} \leqslant V_M$, $I_{BS} = -300$ µA, Pin 9 = 2.0 V, Pin 8 = 0.8 V) | | $I_{OZ2}$ | −100 | — | +100 | |

### DC ELECTRICAL CHARACTERISTICS (continued)

(Specifications apply over the recommended supply voltage and temperature ranges unless otherwise noted.) (See Notes 1, 2)

| Characteristic | Pins | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CLAMP DIODES** | | | | | | |
| Forward Voltage<br>($I_D$ = 350 mA) | 1, 2, 3,<br>14, 15 | $V_{DF}$ | — | 2.5 | 3.0 | Vdc |
| Leakage Current (Per Diode)<br>(Pin 1 = 21 V; Pins 2, 3, 14, 15 = 0 V; $I_{BS}$ = 0 μA) | | $I_{DR}$ | — | — | 100 | μA |
| **$\overline{\text{PHASE A}}$ OUTPUT** | | | | | | |
| Output Low Voltage<br>($I_{OA}$ = 8.0 mA) | 11 | $V_{OLA}$ | — | — | 0.4 | Vdc |
| Off State Leakage Current<br>($V_{OHA}$ = 16.5 V) | | $I_{OHA}$ | — | — | 100 | μA |
| **POWER SUPPLY** | | | | | | |
| Power Supply Current<br>($I_{OD}$ = 0 μA, $I_{BS}$ = −300 μA) | 16 | | | | | mA |
| (L1 = $V_{OHD}$, L2 = $V_{OLD}$, L3 = $V_{OHD}$, L4 = $V_{OLD}$) | | $I_{MW}$ | — | — | 70 | |
| (L1 = $V_{OHD}$, L2 = $V_{OLD}$, L3 = Hi Z, L4 = Hi Z) | | $I_{MZ}$ | — | — | 40 | |
| (L1 = $V_{OHD}$, L2 = $V_{OLD}$, L3 = $V_{OHD}$, L4 = $V_{OHD}$) | | $I_{MN}$ | — | — | 75 | |
| **$\overline{\text{BIAS}}$/SET CURRENT** | | | | | | |
| To Set $\overline{\text{Phase A}}$ | 6 | $I_{BS}$ | -5.0 | — | — | μA |

NOTES:

1. Algebraic convention rather than absolute values is used to designate limit values.
2. Current into a pin is designated as positive. Current out of a pin is designated as negative.
3. $DV_{OD} = |V_{OD1,2} - V_{OD3,4}|$ where
   $V_{OD1,2} = (V_{OHD1} - V_{OLD2})$ or $(V_{OHD2} - V_{OLD1})$, and
   $V_{OD3,4} = (V_{OHD3} - V_{OLD4})$ or $(V_{OHD4} - V_{OLD3})$.
4. $CV_{OD} = |V_{OHD1} - V_{OHD2}|$ or $|V_{OHD3} - V_{OHD4}|$.
5. See section on Power Dissipation in Application Information.

### PACKAGE THERMAL CHARACTERISTICS

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Thermal Resistance, Junction to Ambient — No Heat Sink | $R_{\theta JA}$ | — | 45 | — | °C/W |

### AC SWITCHING CHARACTERISTICS ($T_A$ = +25°C, $V_M$ = 12 V) (See Figures 2, 3, 4)

| Characteristic | Pins | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Clock Frequency | 7 | $f_{CK}$ | 0 | — | 50 | kHz |
| Clock Pulse Width — High | 7 | $PW_{CKH}$ | 10 | — | — | μs |
| Clock Pulse Width — Low | 7 | $PW_{CKL}$ | 10 | — | — | μs |
| $\overline{\text{Bias}}$/Set Pulse Width | 6 | $PW_{BS}$ | 10 | — | — | μs |
| Setup Time — $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS | 10–7<br>9–7 | $t_{su}$ | 5.0 | — | — | μs |
| Hold Time — $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS | 10–7<br>9–7 | $t_h$ | 10 | — | — | μs |
| Propagation Delay — Clk-to-Driver Output | | $t_{PCD}$ | — | 8.0 | — | μs |
| Propagation Delay — $\overline{\text{Bias}}$/Set-to-Driver Output | | $t_{PBSD}$ | — | 1.0 | — | μs |
| Propagation Delay — Clk-to-$\overline{\text{Phase A}}$ Low | 7–11 | $t_{PHLA}$ | — | 12 | — | μs |
| Propagation Delay — Clk-to-$\overline{\text{Phase A}}$ High | 7–11 | $t_{PLHA}$ | — | 5.0 | — | μs |

FIGURE 2 — AC TEST CIRCUIT

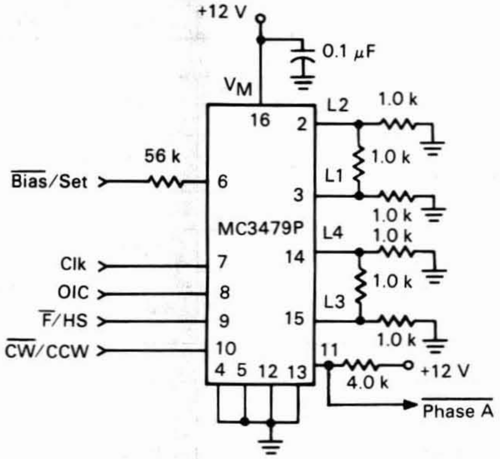
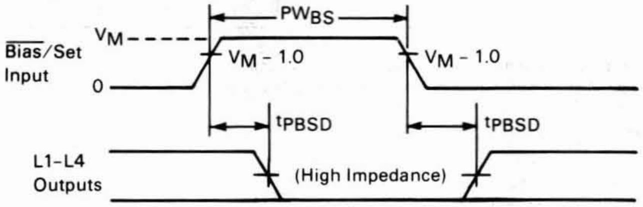

+12 V
0.1 μF
$V_M$
16
2
L2
1.0 k
1.0 k
56 k
$\overline{\text{Bias}}$/Set
6
3
L1
1.0 k
MC3479P
L4
1.0 k
Clk
7
14
1.0 k
OIC
8
L3
$\overline{\text{F}}$/HS
9
15
1.0 k
$\overline{\text{CW}}$/CCW
10
11
4 5 12 13
4.0 k
+12 V
$\overline{\text{Phase A}}$

FIGURE 3 — $\overline{\text{BIAS}}$/SET TIMING (Refer to Figure 2)

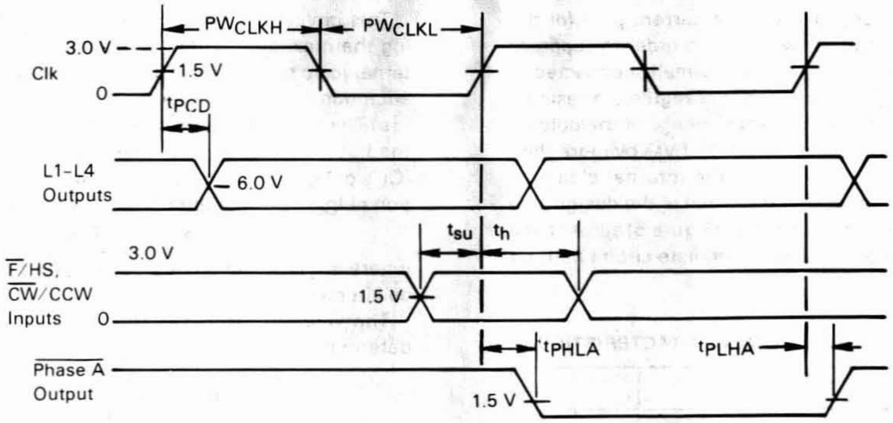

$PW_{BS}$
$\overline{\text{Bias}}$/Set Input
$V_M$
0
$V_M$ - 1.0
$V_M$ - 1.0
$t_{PBSD}$
$t_{PBSD}$
L1-L4 Outputs
(High Impedance)

Note: $t_r$, $t_f$ (10%–90%) for input signals are ⩽ 25 ns.

## PIN DESCRIPTION

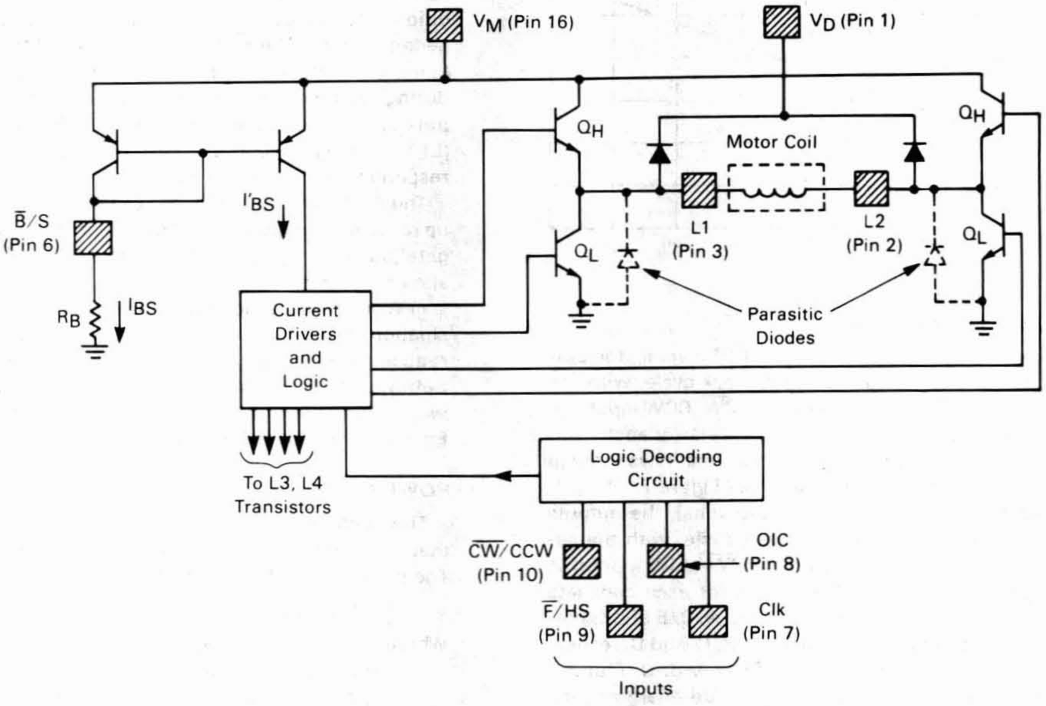
| Name | Symbol | Pin # | Description |
|---|---|---|---|
| Power Supply | $V_M$ | 16 | Power supply pin for both the logic circuit and the motor coil current. Voltage range is +7.2 to +16.5 volts. |
| Ground | Gnd | 4, 5<br>12, 13 | Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins aids in dissipating heat from within the IC package. |
| Clamp Diode Voltage | $V_D$ | 1 | This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and Pin 16. See Figure 11. |
| Driver Outputs | L1, L2<br>L3, L4 | 2, 3<br>14, 15 | High current outputs for the motor coils. L1 and L2 are connected to one coil, and L3 and L4 to the other coil. |
| $\overline{\text{Bias}}$/Set | $\overline{\text{B}}$/S | 6 | This pin is typically 0.7 volts below $V_M$. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened ($I_{BS} < 5.0\ \mu A$) the outputs assume a high impedance condition, while the internal logic presets to a Phase A condition. |
| Clock | Clk | 7 | The positive edge of the clock input switches the outputs to the next position. This input has no effect if Pin 6 is open. |
| $\overline{\text{Full}}$/Half Step | $\overline{\text{F}}$/HS | 9 | When low (Logic "0"), each clock pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one-half step. See Figure 7 for sequence. |
| $\overline{\text{Clockwise}}$/ Counterclockwise | $\overline{\text{CW}}$/CCW | 10 | This input allows reversing the rotation of the motor. See Figure 7 for sequence. |
| Output Impedance Control | OIC | 8 | This input is relevant only in the half step mode (Pin 9 > 2.0 V). When low (Logic "0") the two driver outputs of the non-energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance referenced to $V_M$. See Figure 7. |
| $\overline{\text{Phase A}}$ | $\overline{\text{Ph A}}$ | 11 | This open-collector output indicates (when low) that the driver outputs are in the Phase A condition (L1 = L3 = $V_{OHD}$, L2 = L4 = $V_{OLD}$). |

FIGURE 4 — CLOCK TIMING (Refer to Figure 2)


PWCLKH
PWCLKL
3.0 V
Clk
0
1.5 V
tPCD
L1-L4
Outputs
6.0 V
tsu
th
3.0 V
F/HS,
CW/CCW
Inputs
0
1.5 V
tPHLA
tPLHA
Phase A
Output
1.5 V

Note: $t_r$, $t_f$ (10–90%) for input signals are ≤ 10 ns.

FIGURE 5 — OUTPUT STAGES


VM (Pin 16)
VD (Pin 1)
QH
Motor Coil
QH
B/S
(Pin 6)
I'BS
L1
(Pin 3)
L2
(Pin 2)
QL
QL
RB
IBS
Current
Drivers
and
Logic
Parasitic
Diodes
To L3, L4
Transistors
Logic Decoding
Circuit
CW/CCW
(Pin 10)
OIC
(Pin 8)
F/HS
(Pin 9)
Clk
(Pin 7)
Inputs

## APPLICATION INFORMATION

### GENERAL

The MC3479P integrated circuit is designed to drive a stepper positioning motor in applications such as disk drives and robotics. The outputs can provide up to 350 mA to each of two coils of a two-phase motor. The outputs change state with each low-to-high transition of the clock input, with the new output state depending on the previous state, as well as the input conditions on Pins 8, 9, and 10.

### OUTPUTS (Pins 2, 3, 14, 15)

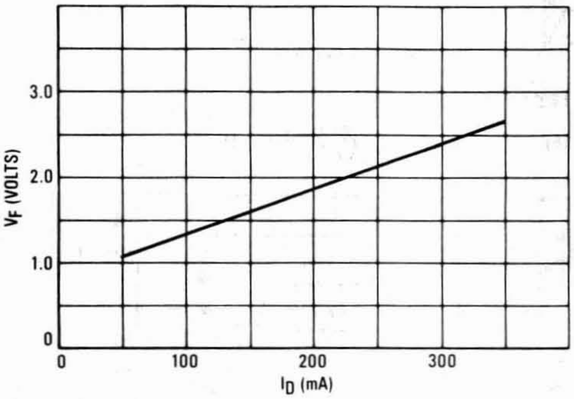
The outputs (L1–L4) are high current outputs (see Figure 5), which when connected to a two-phase motor, provide two full-bridge configurations (L3 and L4 are not shown in Figure 5). The polarities applied to the motor coils depend on which transistor ($Q_H$ or $Q_L$) of each output is on, which in turn depends on the inputs and the decoding circuitry.

The maximum sink current available at the outputs is a function of the resistor connected between Pin 6 and ground (see section on $\overline{\text{Bias}}$/Set operation). Whenever the outputs are to be in a high impedance state, both transistors ($Q_H$ and $Q_L$ of Figure 5) of each output are off.

### $V_D$ (Pin 1)

This pin allows for provision of a current path for the motor coil current during switching, in order to suppress back-EMF voltage spikes. Pin 1 is normally connected to $V_M$ (Pin 16) through a diode (zener or regular), a resistor, or directly. The peak instantaneous voltage at the outputs (Pins 2, 3, 14, and 15) must not exceed $V_M$ by more than 6 volts. The voltage drop across the internal clamping diodes must be included in this portion of the design (see Figure 6). Note the parasitic diodes (Figure 5) across each $Q_L$ of each output provide for a complete circuit path for the switched current.

FIGURE 6 — CLAMP DIODE CHARACTERISTICS



### $\overline{\text{FULL}}$/HALF STEP (Pin 9)

When this input is at a Logic "0" (<0.8 volts), the outputs change a full step with each clock cycle, with the sequence direction depending on the $\overline{\text{CW}}$/CCW input (Pin 10). There are four steps (Phase A, B, C, D) for each complete cycle of the sequencing logic. Current flows through both motor coils during each step. See Figure 7.

When taken to a Logic "1" (>2.0 volts), the outputs change a half step with each clock cycle, with the sequence direction depending on the $\overline{\text{CW}}$/CCW input (Pin 10). Eight steps (Phases A–H) result for each complete cycle of the sequencing logic. Phases A, C, E and G correspond (in polarity) to the phases A, B, C, and D, respectively, of the full step sequence. Phases B, D, F and H provide current to one motor coil, while de-energizing the other coil. The condition of the outputs of the de-energized coil depends on the OIC input (Pin 8). See Figure 7 for timing diagram.

### OIC (Pin 8)

The output impedance control input determines the output impedance to the de-energized coil when operating in the half-step mode. When the outputs are in Phase B, D, F or H (Figure 7) and this input is at a Logic "0" (<0.8 V), the two outputs to the de-energized coil are in a high-impedance condition — $Q_L$ and $Q_H$ of both outputs (Figure 5) are off. When this input is at a Logic "1" (>2.0 V), a low impedance output is provided to the de-energized coil as both outputs have $Q_H$ on ($Q_L$ off). To complete the low impedance path requires connecting Pin 1 ($V_D$) to Pin 16 ($V_M$) as described elsewhere in this data sheet.

### $\overline{\text{BIAS}}$/SET (Pin 6)

This pin can be used for three functions: a) determining the maximum output sink current; b) setting the internal logic to a known state; and c) reducing power consumption.

a) The maximum output sink current is determined by the base drive current supplied to the lower transistors ($Q_L$'s of Figure 5) of each output, which in turn, is a function of $I_{BS}$. The appropriate value of $I_{BS}$ is determined by:

$$I_{BS} = I_{OD} \times 0.86$$

where $I_{BS}$ is in microamps, and $I_{OD}$ is the motor current/coil in milliamps.

The value of $R_B$ (between Pin 6 and ground) is then determined by:

$$R_B = \frac{V_M - 0.7\ \text{V}}{I_{BS}}$$

b) When Pin 6 is opened (raised to $V_M$) such that $I_{BS}$ is <5.0 μA, the internal logic is set to the Phase A condition, and the four driver outputs are put into a high impedance state. The $\overline{\text{Phase A}}$ output (Pin 11) goes active (low), and input signals at Pins 7, 8, 9 and 10 are ignored during this time. Upon re-establishing $I_{BS}$, the driver outputs become active, and will be in the Phase A position ($L1 = L3 = V_{OHD}$, $L2 = L4 = V_{OLD}$). The circuit will then respond to the inputs at Pins 7, 8, 9 and 10.

The Set function (opening Pin 6) can be used as a power-up reset while supply voltages are settling. A CMOS logic gate (powered by $V_M$) can be used to control this pin as shown in Figure 11.

c) Whenever the motor is not being stepped, power dissipation in the IC and in the motor may be lowered by reducing $I_{BS}$, so as to reduce the output (motor) current. Setting $I_{BS}$ to 75 μA will reduce the motor current, but will not reset the internal logic as described above. See Figure 12 for a suggested circuit.

### POWER DISSIPATION

The power dissipated by the MC3479P must be such that the junction temperature ($T_J$) does not exceed 150°C. The power dissipated can be expressed as:

$$P = (V_M \times I_M) + (2 \times I_{OD})\,[(V_M - V_{OHD}) + V_{OLD}]$$

where $V_M$ = Supply voltage;
$I_M$ = Supply current other than $I_{OD}$;
$I_{OD}$ = Output current to each motor coil;
$V_{OHD}$ = Driver output high voltage;
$V_{OLD}$ = Driver output low voltage.

The power supply current ($I_M$) is obtained from Figure 8. After the power dissipation is calculated, the junction temperature can be calculated using:

$$T_J = (P \times R_{\theta JA}) + T_A$$

where $R_{\theta JA}$ = Junction to ambient thermal resistance;
$T_A$ = Ambient temperature.

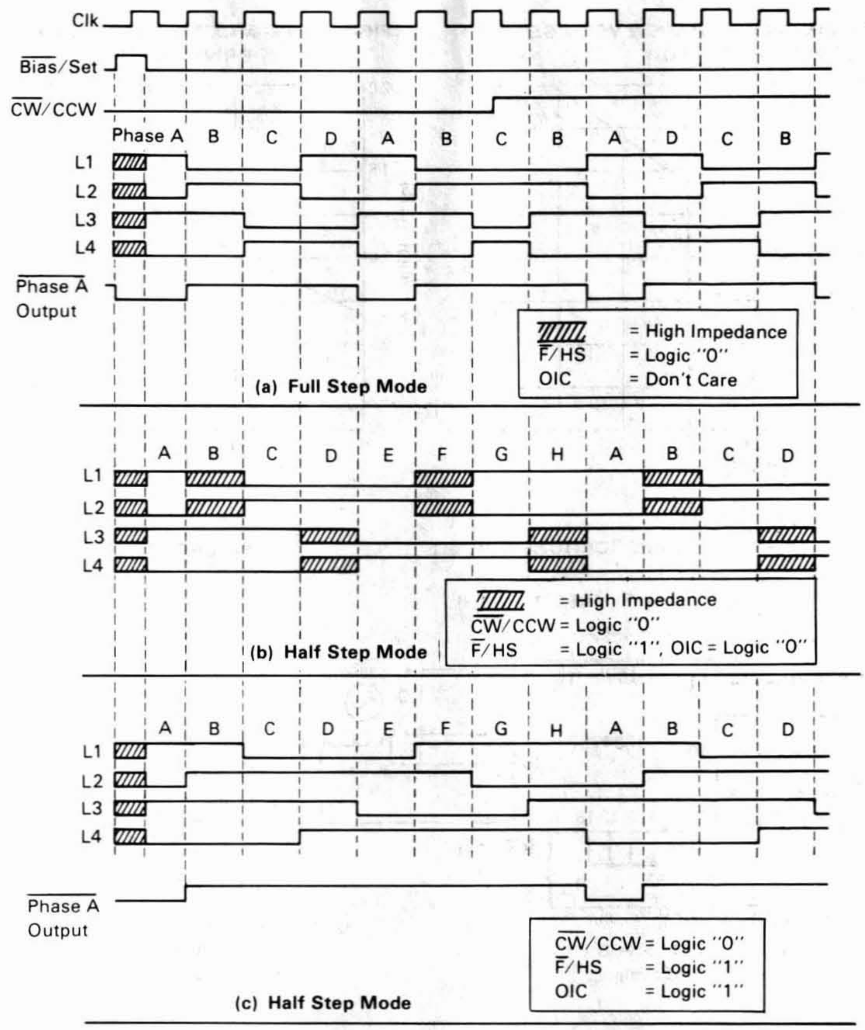
For example, assume an application where $V_M = 12$ V, the motor requires 200 mA/coil, operating at room temperature with no heat sink on the IC. $I_{BS}$ is calculated:

$$I_{BS} = 200 \times 0.86$$
$$I_{BS} = 172\ \mu\text{A}$$

$R_B$ is calculated:

$$R_B = (12 - 0.7)\ \text{V}/172\ \mu\text{A}$$
$$R_B = 65.7\ \text{k}\Omega$$

**FIGURE 7 — OUTPUT SEQUENCE**


Clk
$\overline{\text{Bias}}$/Set
$\overline{\text{CW}}$/CCW
Phase A B C D A B C B A D C B
L1
L2
L3
L4
$\overline{\text{Phase A}}$ Output
▨ = High Impedance
$\overline{\text{F}}$/HS = Logic "0"
OIC = Don't Care
A B C D E F G H A B C D
▨ = High Impedance
$\overline{\text{CW}}$/CCW = Logic "0"
$\overline{\text{F}}$/HS = Logic "1", OIC = Logic "0"
A B C D E F G H A B C D
$\overline{\text{Phase A}}$ Output
$\overline{\text{CW}}$/CCW = Logic "0"
$\overline{\text{F}}$/HS = Logic "1"
OIC = Logic "1"

(a) **Full Step Mode**

(b) **Half Step Mode**

(c) **Half Step Mode**

From Figure 8, $I_M$ (max) is determined to be 40 mA. From Figure 9, $V_{OLD}$ is 0.46 volts, and from Figure 10, ($V_M - V_{OHD}$) is 1.4 volts.

$$P = (12 \times 0.040) + (2 \times 0.2)(1.4 + 0.46)$$
$$P = 1.22 \text{ W}$$

$$T_J = (1.22 \text{ W} \times 45°\text{C/W}) + 25°\text{C}$$
$$T_J = 80°\text{C}$$

This temperature is well below the maximum limit. If the calculated $T_J$ had been higher than 150°C, a heat sink such as the Staver Co. V-7 series, Aavid #5802, or Thermalloy #6012 could be used to reduce $R_{\theta JA}$. In extreme cases forced air cooling should be considered.

The above calculation, and $R_{\theta JA}$, assumes that a ground plane is provided under the MC3479P (either or both sides of the PC board) to aid in the heat dissipation. Single nominal width traces leading from the four ground pins should be avoided as this will increase $T_J$, as well as provide potentially disruptive ground noise and $I_R$ drops when switching the motor current.

**FIGURE 8 — POWER SUPPLY CURRENT**

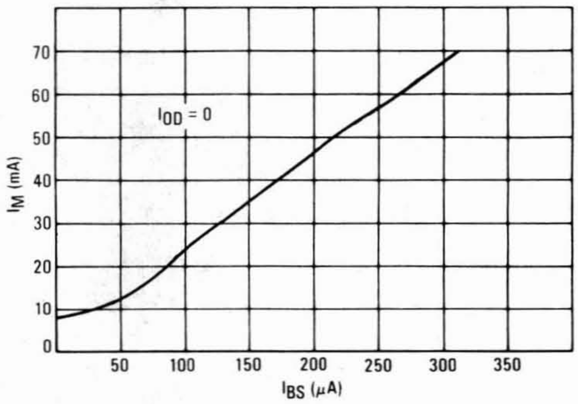


FIGURE 9 — MAXIMUM SATURATION VOLTAGE — DRIVER OUTPUT LOW

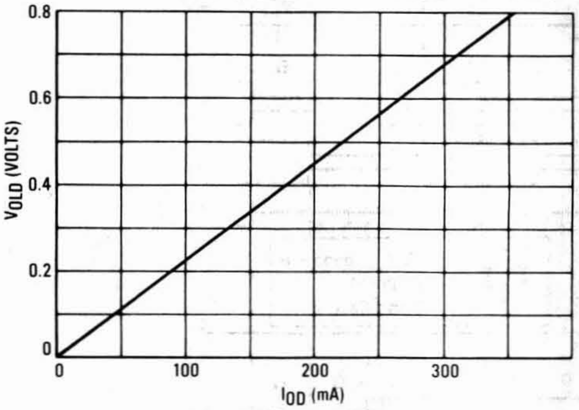


FIGURE 10 — MAXIMUM SATURATION VOLTAGE — DRIVER OUTPUT HIGH

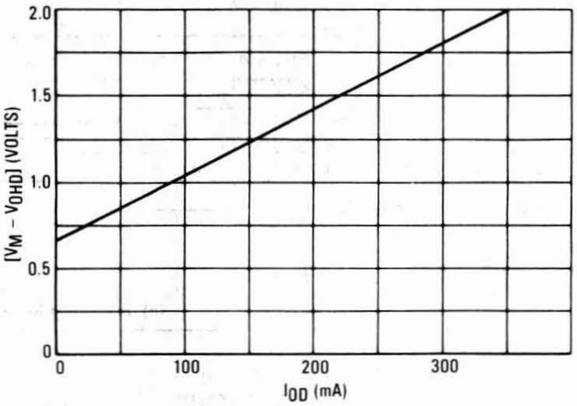


FIGURE 11 — TYPICAL APPLICATIONS CIRCUIT

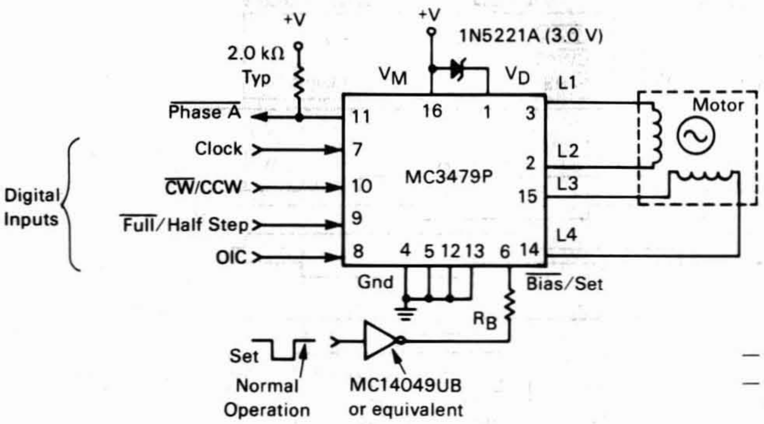
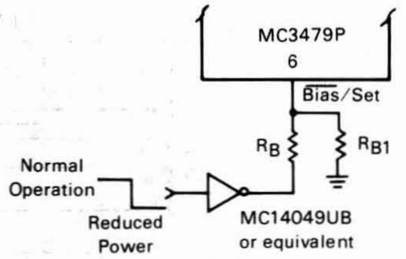

+V
+V
2.0 kΩ
Typ
1N5221A (3.0 V)
$V_M$
$V_D$
L1
Phase A
11
16
1
3
Motor
Clock
7
2
L2
Digital Inputs
CW/CCW
10
MC3479P
15
L3
Full/Half Step
9
L4
OIC
8
4 5 12 13 6 14
Gnd
Bias/Set
$R_B$
Set
Normal Operation
MC14049UB
or equivalent

FIGURE 12 — POWER REDUCTION


MC3479P
6
Bias/Set
$R_B$
$R_{B1}$
Normal Operation
Reduced Power
MC14049UB
or equivalent

— Suggested value for $R_{B1}$ ($V_M$ = 12 V) is 150 kΩ.

— $R_B$ calculation (see text) must take into account the current through $R_{B1}$.

**MOTOROLA**

# MC3484V2
# MC3484V4

## Advance Information

### INTEGRATED SOLENOID DRIVER

The MC3484 is an integrated monolithic solenoid driver. Its typical function is to apply full battery voltage to fuel injector(s) for rapid current rise, in order to produce positive injector opening. When load current reaches a preset level (4.0 A in MC3484V4 or 2.4 A in MC3484V2) the injector driver reduces the load current by a 4-to-1 ratio and operates as a constant current supply. This condition holds the injector open and reduces system dissipation. Other solenoid or relay applications could be served by the MC3484. Two high impedance inputs are provided which permit a variety of control options and can be driven by TTL or CMOS logic:

- Microprocessor Compatible Inputs
- On-Chip Power Device

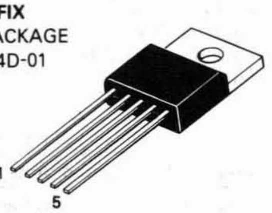
| | | |
|---|---|---|
| MC3484V2 | 2.4 A Peak | 0.6 A Sustain |
| MC3484V4 | 4.0 A Peak | 1.0 A Sustain |

- Low Thermal Resistance to Grounded Tab
  $R_{\theta JC} = 2.5°C/W$
- Internal Thermal Protection
  Controls die temperature to 160°C
- Low Saturation Voltage
  $V_{CE(sat)} = 1.6$ V Typ @ 4.0 A
- Uncompromised Performance −40°C to +125°C Junction Temperature
- Fully Functional from $V_{bat} = 4.0$ V to 24 V
- High $V_{(BR)CEO(sus)} = 42$ V min @ $I_{SUSTAIN}$

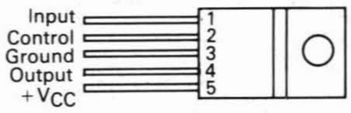
**SOLENOID DRIVER**
**2.4 A — V2**
**4.0 A — V4**

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

**V SUFFIX**
PLASTIC PACKAGE
CASE 314D-01



**PIN CONNECTIONS UNFORMED PACKAGE**

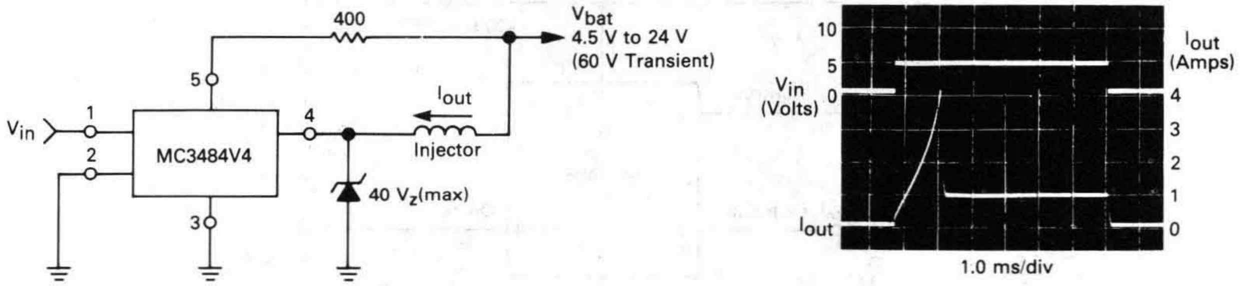


**ORDERING INFORMATION**

| Device | Temperature Range | Peak Current |
|---|---|---|
| MC3484V2 | −40 to + 125°C | 2.4 A |
| MC3484V4 | −40 to +125°C | 4.0 A |

**FIGURE 1 — TYPICAL APPLICATION**

Single Injector — No Control Option



This document contains information on a new product. Specifications and information herein are subject to change without notice.

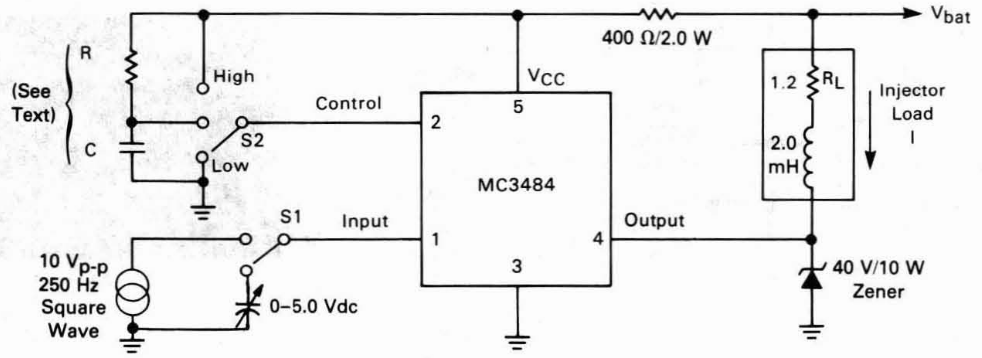
## MAXIMUM RATINGS

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage ($V_{bat}$) | 24 | Volts |
| Input (Pin 1) | -6.0 to +24 | V |
| Control (Pin 2) | -6.0 to +24 | V |
| Internal Regulator (Pin 5) | 50 | mA |
| Junction Temperature | 150 | °C |
| Operating Temperature Range (Tab Temperature) | -40 to +125 | °C |
| Storage Temperature Range | -65 to +150 | °C |
| Thermal Resistance, Junction to Case | 2.5 | °C/W |

**ELECTRICAL CHARACTERISTICS** ($V_{bat}$ = 12 Vdc, $T_C$ = 25°C, test circuit of Figure 2, unless noted)

| Characteristic | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Peak Current ($I_{pk[sense]}$) | V4<br>V2 | 3.6<br>1.7 | 4.0<br>2.4 | 5.2<br>2.9 | A |
| Output Sustaining Current ($I_{sus}$) | V4<br>V2 | 0.95<br>0.50 | 1.0<br>0.6 | 1.3<br>0.7 | A |
| $V_{(BR)CEO(sus)}$ @ 2.0 A | | 42 | 50 | — | V |
| Output Voltage in Saturated Mode | | | | | V |
| V2 or V4 @ 2.0 A | | — | 1.2 | — | |
| V2 or V4 @ 2.4 A | | — | 1.3 | — | |
| V4 @ 4.0 A | | — | 1.6 | — | |
| Internal Regulated Voltage ($V_{CC}$, Figure 2) | | — | 7.1 | — | V |
| Input "on" Threshold Voltage | | — | 1.4 | 2.0 | V |
| Input "off" Threshold Voltage | | 0.7 | 1.3 | — | V |
| Input "on" Current | | | | | μA |
| @ $V_I$ = 1.4 Vdc | | — | 35 | — | |
| @ $V_I$ = 5.0 Vdc | | — | 220 | — | |
| Control "on" Threshold Voltage | | — | 1.9 | — | V |
| Control "on" Current | | | | | μA |
| @ $V_Z$ = 1.9 Vdc ($V_I$ High) | | — | −10 | — | |
| @ $V_Z$ = 5.0 Vdc ($V_I$ High) | | — | 140 | — | |
| Control Pin Discharge Impedance ($V_I$ Low) | | — | 10 | — | kΩ |
| Input Turn On Delay ($t_i$) | | — | 0.5 | 1.0 | μs |
| $I_{pk}$ sense to $I_{sus}$ delay (tp) | | — | 60 | — | μs |
| Control Signal Delay ($t_t$) | | — | 15 | — | μs |
| Input Turn Off from Saturated Mode Delay ($t_s$) | | — | 1.0 | — | μs |
| Input Turn Off from Sustain Mode Delay ($t_d$) | | — | 0.2 | — | μs |
| Output Voltage Rise Time ($t_V$) | | — | 0.4 | — | μs |
| Output Current Fall Time ($t_f$) | 2.0 A<br>4.0 A | —<br>— | 0.3<br>0.6 | 1.0<br>1.0 | μs |
| Internal Thermal Regulation | | — | 160 | — | °C |

FIGURE 2 — TEST CIRCUIT


R
(See Text)
C
High
Low
S2
Control
$V_{CC}$
5
2
MC3484
S1
Input
1
3
4
Output
10 $V_{p-p}$ 250 Hz Square Wave
0–5.0 Vdc
400 Ω/2.0 W
$V_{bat}$
1.2
$R_L$
2.0 mH
Injector Load
I
40 V/10 W Zener

## GENERAL INFORMATION

Inductive actuators such as automotive electronic fuel injectors, relays, solenoids and hammer drivers can be powered more efficiently by providing a high current drive until actuation (pull-in) occurs and then decreasing the drive current to a level which will sustain actuation. Pull-in and especially drop-out times of the actuators are also improved.

The fundamental output characteristic of the MC3484 provides a low impedance saturated power switch until the load current reaches a predetermined high-current level and then changes to a current source of lower magnitude until the device is turned off. This output characteristic allows the inductive load to control its actuation time during turn-on while minimizing power and stored energy during the sustain period, thereby promoting a fast turn-off time.

Automotive injectors at present come in two types. The large throttle body injectors have an impedance of about 2.0 mH and 1.2 Ω and require the MC3484 V4 driver. The smaller type, popular world-wide, has an impedance of 4.0 mH and 2.4 Ω and needs about a 2.0 A pulse for good results. Some designs are planned which employ two of the smaller types in parallel. The inductance of the injectors are much larger at low current, decreasing due to armature movement and core saturation to the values above at rated current.

Operating frequencies range from 5.0 Hz to 250 Hz depending on the injector location and engine type. Duty cycle in some designs reaches 80%.

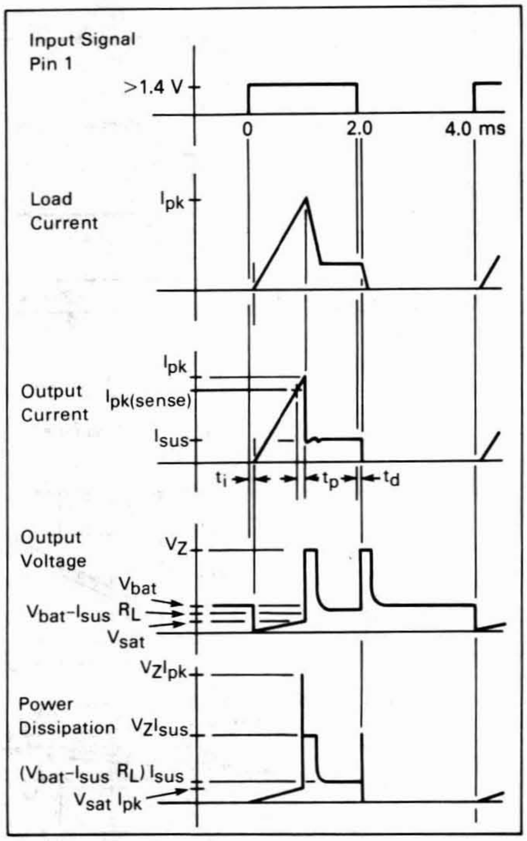
## APPLICATIONS INFORMATION

The MC3484 is provided with an input pin (Pin 1) which turns the injector driver "on" and "off". This pin has a nominal trip level of 1.4 V and an input impedance of 20 kΩ. It is internally protected against negative voltages and is compatible with TTL and most other logic.

There is also a control pin (Pin 2) which if held low or grounded, permits the device to operate in saturation to $I_{pk(sense)}$, where it will switch to $I_{sus}$ automatically. If Pin 2 is brought high (>1.9 V), the MC3484 will switch to $I_{sus}$ mode, whether or not $I_{pk(sense)}$ has been reached. (More on this later.)

Figure 3 shows the operating waveforms for the simplest mode; i.e., with control Pin 2 grounded. When the driver is turned on, the current ramps up to the peak current sense level, where some overshoot occurs because of internal delay. The MC3484 then reduces its output to $I_{sus}$. The fall time of the device is very rapid (≤1.0 μs), but the decay of the load current takes 150 to 220 μs, while dumping the load energy into the protection zener clamp.

**FIGURE 3 — OPERATING WAVEFORMS**
**(Max Frequency 250 Hz, Pin 2 Grounded)**



It is essential that the zener voltage be lower than the $V_{(BR)CEO(sus)}$, but not so low as to greatly stretch the load current decay time. Without the zener, the discharge of the load energy would be totally into the MC3484, which, for the high current applications, could cause the device to fail. (See SOA, Figure 12.)

Also in Figure 3 is the graphically derived instantaneous power dissipation of the MC3484. It shows that, for practical purposes, the worst case dissipation is less than $(I_{sus})(V_{bat})$ (duty cycle).

If the combined effects of dissipation, ambient temperature and poor heat sinking causes the die temperature to reach 160°C, an internal protection circuit will reduce the output current to prevent device failure. The output pulses will remain controlled by the input, but may not operate the fuel injectors.

FIGURE 4 — SWITCHING WAVEFORMS
(Expanded Time Scale)

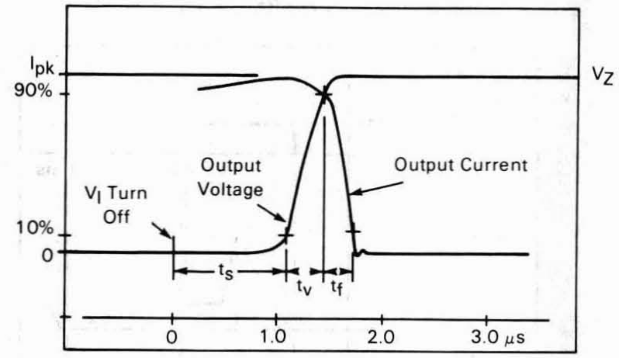
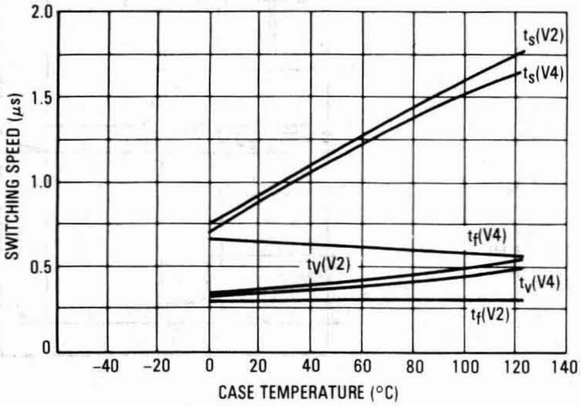


FIGURE 5 — SWITCHING SPEED versus TEMPERATURE



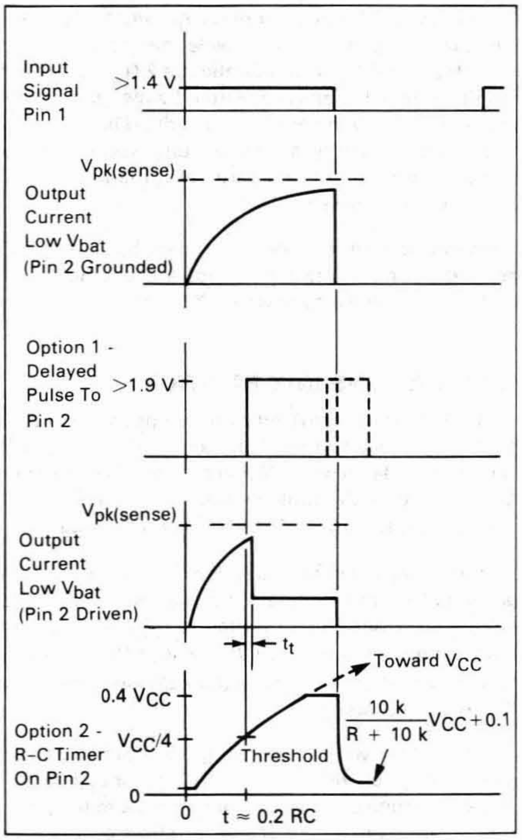
Provided in Figures 3, 4, and 6 are definitions of the switching intervals specified in the Electrical Characteristics. Figure 5 shows that the critical switching parameters stay under control at elevated temperatures.

In the case where $V_{bat}$ is too low, or the input Pin 1 "on" signal is too narrow for the output current to reach $I_{pk(sense)}$, it may still be desirable to cause the MC3484 to switch to the $I_{sus}$ mode. This can be accomplished either by driving Pin 2 with a properly delayed pulse, or by using an R-C charging circuit on Pin 2. If a pulse source is used, only the leading edge and 2.0 volts amplitude are important. The pulse duration is not critical, because once the MC3484 has changed to $I_{sus}$ mode, it will stay there until Pin 1 has been recycled. A minimum pulse width of 15 μs will assure state change.

If the R-C circuit is used (circuit of Figure 2, switch S2 in middle position), the charging voltage will be toward $V_{CC}$, but will reach the Pin 2 threshold at $V_{CC}/4$. This maintains the timing of the $I_{sus}$ transition even when $V_{CC}$ is below regulation. When Pin 1 is turned off, the capacitor on Pin 2 is discharged through an internal 10 kΩ resistor to about 0.1 V above ground. It is important to use a high value for R, so that the capacitor will be almost fully discharged. With a recommended R = 470 kΩ and C = 0.02 μF, Pin 2 threshold will be reached in approximately 2.0 ms.

In another application option, Pin 2 can be enabled in paralleled with Pin 1, or connected to $V_{CC}$, so that the MC3484 always turns on in the $I_{sus}$ mode. The MC3484 thus provides a logic compatible, constant current power switch.

FIGURE 6 — APPLICATION OF CONTROL (PIN 2)
(Test Circuit of Figure 2)


Input Signal Pin 1
>1.4 V
$V_{pk(sense)}$
Output Current Low $V_{bat}$ (Pin 2 Grounded)
Option 1 - Delayed Pulse To Pin 2
>1.9 V
$V_{pk(sense)}$
Output Current Low $V_{bat}$ (Pin 2 Driven)
$t_t$
Toward $V_{CC}$
0.4 $V_{CC}$
$\frac{10\ k}{R + 10\ k} V_{CC} + 0.1$
Option 2 - R-C Timer On Pin 2
$V_{CC}/4$
Threshold
0
0
t ≈ 0.2 RC

## TYPICAL CHARACTERISTICS

(Unless otherwise noted: Test circuit of Figure 2, $V_{bat}$ = 12 Vdc, $T_C$ = 25°C, 250 Hz square wave input)

FIGURE 7 — OUTPUT CURRENT versus TEMPERATURE

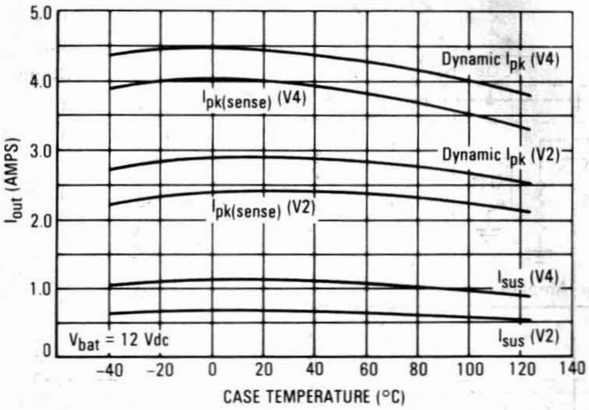


FIGURE 8 — SATURATION VOLTAGE

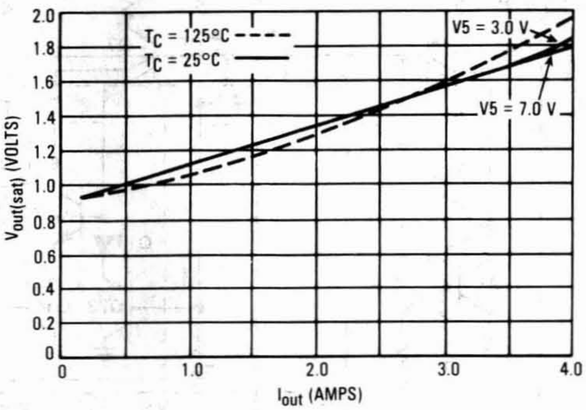


FIGURE 9 — OUTPUT CURRENT versus SUPPLY VOLTAGE

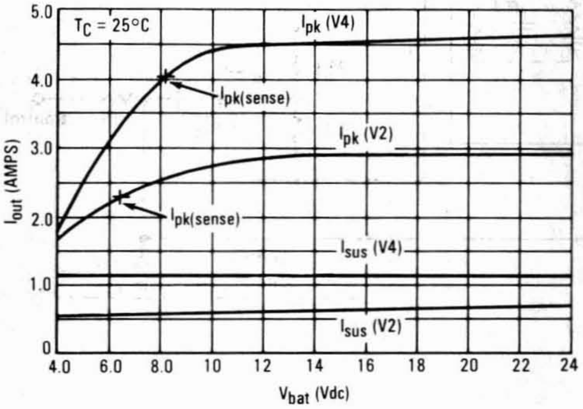


FIGURE 10 — OPERATING VOLTAGES

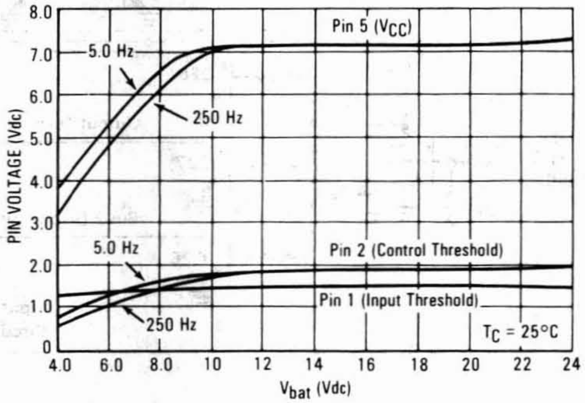


FIGURE 11 — BREAKDOWN VOLTAGE versus TEMPERATURE

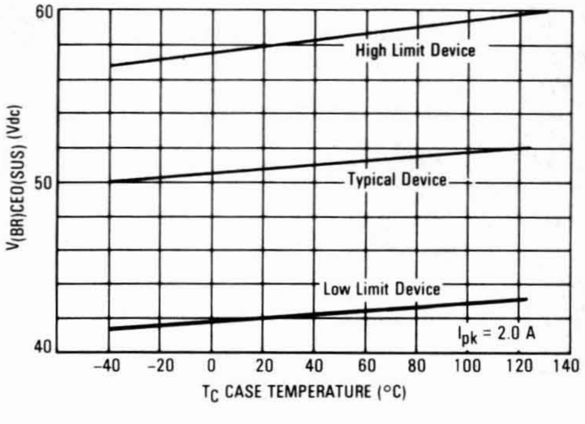


FIGURE 12 — SAFE OPERATING AREA

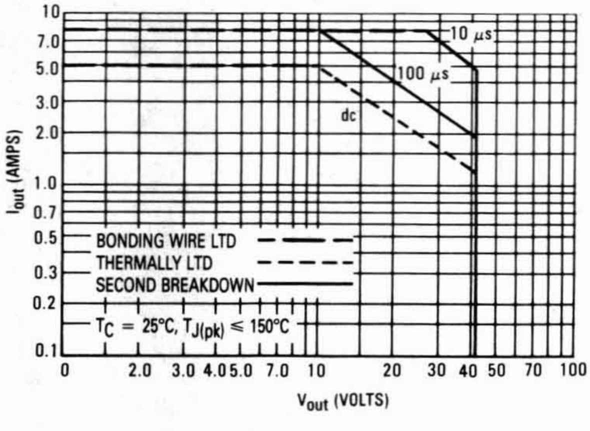
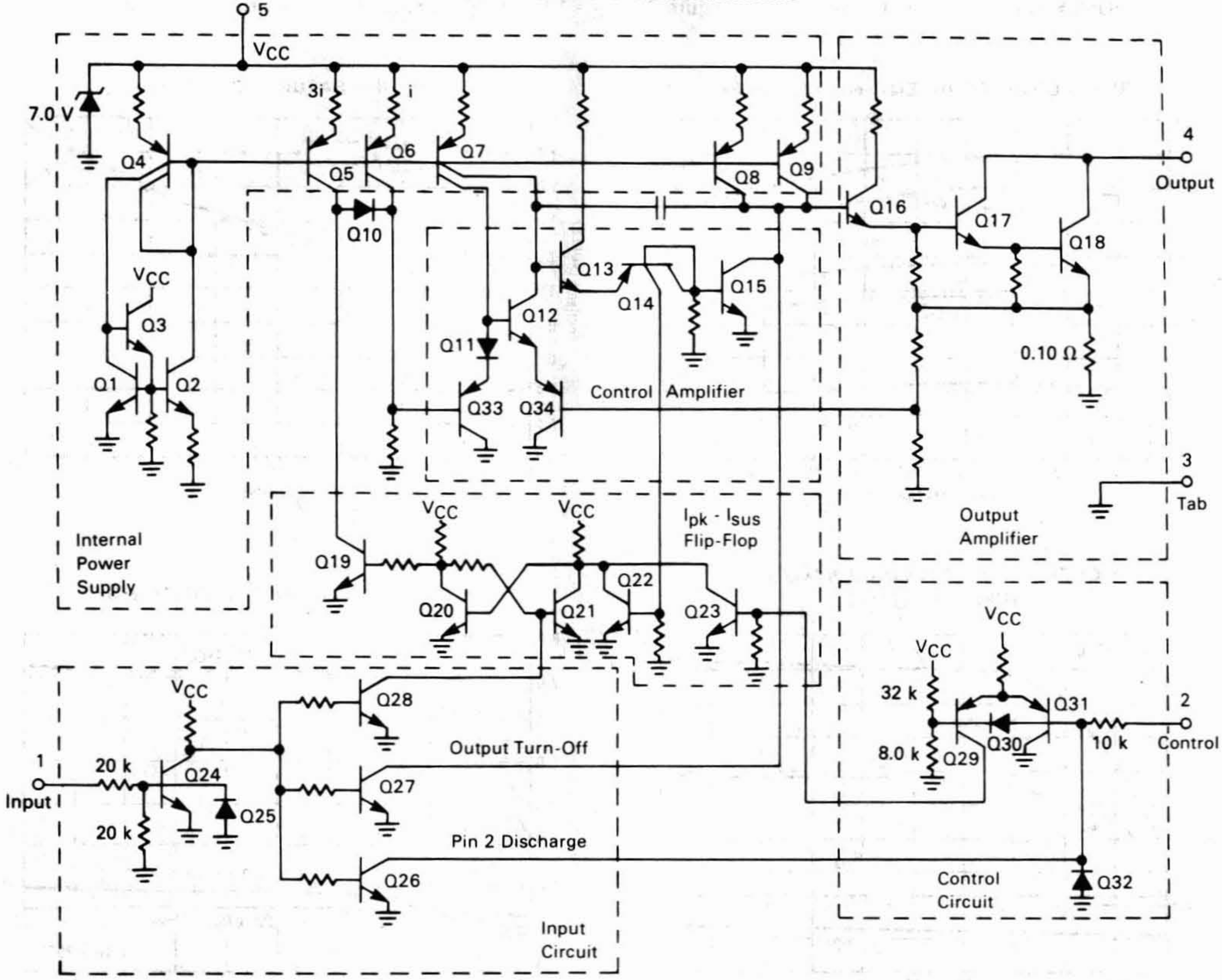


FIGURE 13 — INTERNAL SCHEMATIC


5
VCC
7.0 V
Q4
3i
i
Q5
Q6
Q7
Q8
Q9
Q10
Q16
Q17
Q18
4
Output
VCC
Q3
Q1
Q2
Q13
Q14
Q15
Q11
Q12
Q33
Q34
Control Amplifier
0.10 Ω
3
Tab
Output Amplifier
Internal Power Supply
VCC
VCC
Ipk - Isus Flip-Flop
Q19
Q20
Q21
Q22
Q23
VCC
VCC
32 k
Q31
2
Control
8.0 k
Q29
Q30
10 k
VCC
Q28
Output Turn-Off
1
Input
20 k
Q24
Q25
20 k
Q27
Pin 2 Discharge
Q26
Input Circuit
Control Circuit
Q32

**MOTOROLA**

# MC33030

## Advance Information

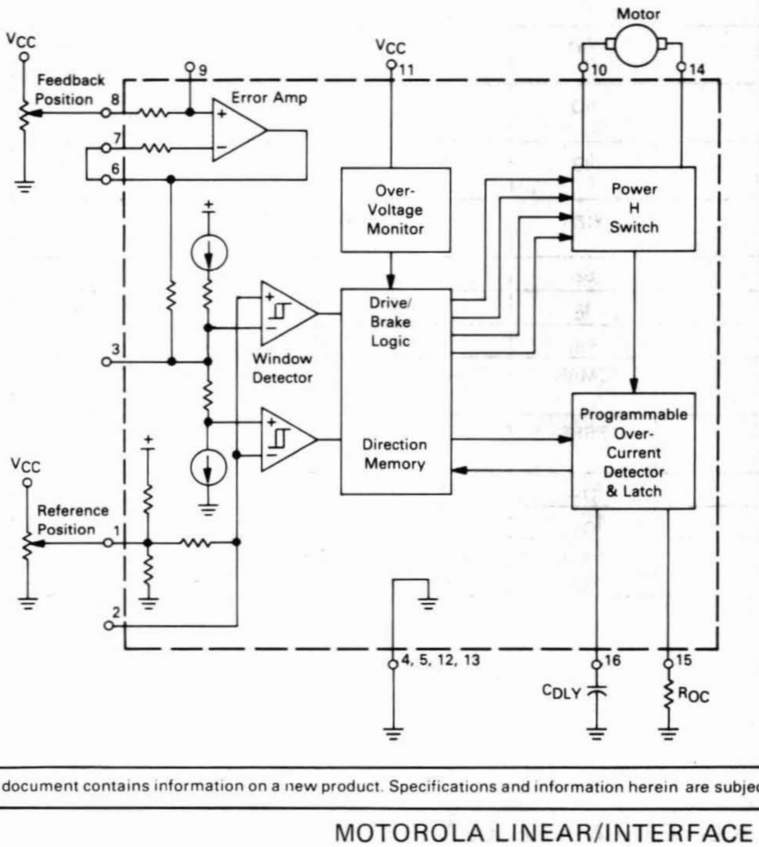
### DC SERVO MOTOR CONTROLLER/DRIVER

The MC33030 is a monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on-chip op amp and window comparator with wide input common-mode range, drive and brake logic with direction memory, power H switch driver capable of 1.0 A, independently programmable over-current monitor and shutdown delay, and over-voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.

Although this device is primarily intended for servo applications, it can be used as a switchmode motor controller.

- On-Chip Error Amp for Feedback Monitoring
- Window Detector with Deadband and Self Centering Reference Input
- Drive/Brake Logic with Direction Memory
- 1.0 A Power H Switch
- Programmable Over-Current Detector
- Programmable Over-Current Shutdown Delay
- Over-Voltage Shutdown

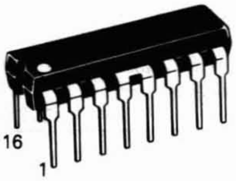
### SIMPLIFIED BLOCK DIAGRAM



$V_{CC}$
Feedback Position
8
9
7
6
Error Amp
$V_{CC}$
11
Motor
10
14
Over-Voltage Monitor
Power H Switch
Drive/Brake Logic
Window Detector
3
Direction Memory
Programmable Over-Current Detector & Latch
$V_{CC}$
Reference Position
1
2
4, 5, 12, 13
16
15
$C_{DLY}$
$R_{OC}$

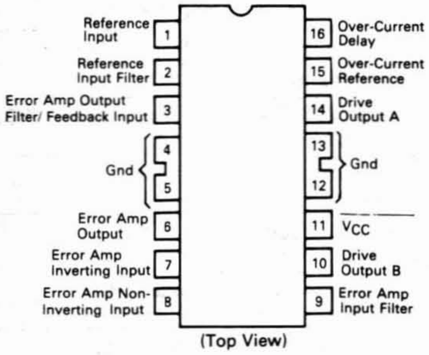
### DC SERVO MOTOR CONTROLLER/DRIVER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



PLASTIC PACKAGE
**CASE 648C**

### PIN CONNECTIONS



Reference Input 1
Reference Input Filter 2
Error Amp Output Filter/ Feedback Input 3
Gnd 4
5
Error Amp Output 6
Error Amp Inverting Input 7
Error Amp Non-Inverting Input 8
16 Over-Current Delay
15 Over-Current Reference
14 Drive Output A
13 Gnd
12
11 $V_{CC}$
10 Drive Output B
9 Error Amp Input Filter
(Top View)

Pins 4, 5, 12 and 13 are electrical ground and heat sink pins for IC

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC33030P | −40°C to +85°C | Plastic DIP |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 36 | V |
| Input Voltage Range<br>Op Amp, Comparator, Current Limit.<br>Pins 1, 2, 3, 6, 7, 8, 9, 15. | $V_{IR}$ | $-0.3$ to $V_{CC}$ | V |
| Input Differential Voltage Range<br>Op Amp, Comparator.<br>Pins 1, 2, 3, 6, 7, 8, 9. | $V_{IDR}$ | $-0.3$ to $V_{CC}$ | V |
| Delay Pin Sink Current (Pin 16) | $I_{DLY(sink)}$ | 20 | mA |
| Output Source Current (Op Amp) | $I_{source}$ | 10 | mA |
| Drive Output Voltage Range (Note 1) | $V_{DRV}$ | $-0.3$ to $(V_{CC}+V_F)$ | V |
| Drive Output Source Current (Note 2) | $I_{DRV(source)}$ | 1.0 | A |
| Drive Output Sink Current (Note 2) | $I_{DRV(sink)}$ | 1.0 | A |
| Brake Diode Forward Current (Note 2) | $I_F$ | 1.0 | A |
| Power Dissipation and Thermal Characteristics<br>Maximum Power Dissipation @ $T_A = 70°C$<br>Thermal Resistance Junction to Air<br>Thermal Resistance Junction to Case.<br>Pins 4, 5, 12, 13. | <br>$P_D$<br>$R_{\theta JA}$<br>$R_{\theta JC}$ | <br>1000<br>80<br>15 | <br>mW<br>°C/W<br>°C/W |
| Operating Junction Temperature | $T_J$ | +150 | °C |
| Operating Ambient Temperature Range | $T_A$ | $-40$ to $+85$ | °C |
| Storage Temperature Range | $T_{stg}$ | $-65$ to $+150$ | °C |

Notes:
1. The upper voltage level is clamped by the forward drop, $V_F$, of the brake diode.
2. These values are for continuous dc current. Maximum package power dissipation limits must be observed.

**ELECTRICAL CHARACTERISTICS** ($V_{CC} = 14$ V, $T_A = 25°C$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **ERROR AMP** | | | | | |
| Input Offset Voltage ($-40°C \leq T_A \leq +85°C$)<br>$V_{Pin\ 6} = 7.0$ V, $R_L = 100$ k | $V_{IO}$ | — | 1.5 | 10 | mV |
| Input Offset Current<br>$V_{Pin\ 6} = 1.0$ V, $R_L = 100$ k | $I_{IO}$ | — | 0.7 | — | nA |
| Input Bias Current<br>$V_{Pin\ 6} = 7.0$ V, $R_L = 100$ k | $I_{IB}$ | — | 7.0 | — | nA |
| Input Common-Mode Voltage Range<br>$\Delta V_{IO} = 20$ mV, $R_L = 100$ k | $V_{ICR}$ | — | 0 to $(V_{CC}-1.2)$ | — | V |
| Slew Rate, Open Loop ($V_{ID} = 0.5$ V, $C_L = 15$ pF) | SR | — | 0.40 | — | V/μs |
| Unity-Gain Crossover Frequency | $f_c$ | — | 550 | — | kHz |
| Unity-Gain Phase Margin | $\phi_m$ | — | 63 | — | deg. |
| Common-Mode Rejection Ratio<br>$V_{Pin\ 6} = 7.0$ V, $R_L = 100$ k | CMRR | 50 | 82 | — | dB |
| Power Supply Rejection Ratio<br>$V_{CC} = 9.0$ to 16 V, $V_{Pin\ 6} = 7.0$ V, $R_L = 100$ k | PSRR | — | 89 | — | dB |
| Output Source Current ($V_{Pin\ 6} = 12$ V) | $I_{O+}$ | — | 1.8 | — | mA |
| Output Sink Current ($V_{Pin\ 6} = 1.0$ V) | $I_{O-}$ | — | 250 | — | μA |
| Output Voltage Swing ($R_L = 17$ k to Ground) | $V_{OH}$<br>$V_{OL}$ | 12.5<br>— | 13.1<br>0.02 | —<br>— | V<br>V |

(Continued)

**ELECTRICAL CHARACTERISTICS** (Continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **WINDOW DETECTOR** | | | | | |
| Input Hysteresis Voltage ($V_1 - V_4$, $V_2 - V_3$, Figure 17) | $V_H$ | 20 | 28 | 36 | mV |
| Input Dead Zone Range ($V_2 - V_4$, Figure 17) | $V_{IDZ}$ | 166 | 210 | 254 | mV |
| Input Offset Voltage ($\|[V_2 - V_{Pin\,2}] - [V_{Pin\,2} - V_4]\|$, Figure 17) | $V_{IO}$ | — | 25 | — | mV |
| Input Functional Common-Mode Range (Note 4)<br>Upper Threshold<br>Lower Threshold | <br>$V_{IH}$<br>$V_{IL}$ | <br>—<br>— | <br>($V_{CC} - 1.05$)<br>0.24 | <br>—<br>— | V |
| Reference Input Self Centering Voltage<br>Pins 1 and 2 Open | $V_{RSC}$ | — | (1/2 $V_{CC}$) | — | V |
| Window Detector Propagation Delay<br>Comparator Input, Pin 3, to Drive Outputs<br>$V_{ID}$ = 0.5 V, $R_{L(DRV)}$ = 390 Ω | $t_{p(IN/DRV)}$ | — | 2.0 | — | μs |
| **OVER-CURRENT MONITOR** | | | | | |
| Over-Current Reference Resistor Voltage (Pin 15) | $R_{OC}$ | 3.9 | 4.3 | 4.7 | V |
| Delay Pin Source Current<br>$V_{DLY}$ = 0 V, $R_{OC}$ = 27 k, $I_{DRV}$ = 0 mA | $I_{DLY(source)}$ | — | 4.5 | 5.9 | μA |
| Delay Pin Sink Current ($R_{OC}$ = 27 k, $I_{DRV}$ = 0 mA)<br>$V_{DLY}$ = 5.0 V<br>$V_{DLY}$ = 8.3 V<br>$V_{DLY}$ = 14 V | $I_{DLY(sink)}$ | <br>—<br>—<br>— | <br>0.1<br>0.7<br>16.5 | <br>—<br>—<br>— | mA |
| Delay Pin Voltage, Low State ($I_{DLY}$ = 0 mA) | $V_{OL(DLY)}$ | — | 0.3 | 0.4 | V |
| Over-Current Shutdown Threshold<br>$V_{CC}$ = 14 V<br>$V_{CC}$ = 8.0 V | $V_{th(OC)}$ | <br>6.8<br>5.8 | <br>7.5<br>6.4 | <br>8.2<br>7.0 | V |
| Over-Current Shutdown Propagation Delay<br>Delay Capacitor Input, Pin 16, to Drive Outputs<br>$V_{ID}$ = 0.5 V | $t_{p(DLY/DRV)}$ | — | 1.8 | — | μs |
| **POWER H-SWITCH** | | | | | |
| Drive-Output Saturation (−40°C ≤ $T_A$ ≤ +85°C, Note 3)<br>High State ($I_{source}$ = 100 mA)<br>Low State ($I_{sink}$ = 100 mA) | <br>$V_{OH(DRV)}$<br>$V_{OL(DRV)}$ | <br>($V_{CC} - 2$)<br>— | <br>($V_{CC} - 0.85$)<br>0.12 | <br>—<br>1.0 | V |
| Drive-Output Voltage Switching Time ($C_L$ = 15 pF)<br>Rise Time<br>Fall Time | <br>$t_r$<br>$t_f$ | <br>—<br>— | <br>200<br>200 | <br>—<br>— | ns |
| Brake Diode Forward Voltage Drop ($I_F$ = 200 mA, Note 3) | $V_F$ | — | 1.04 | 2.5 | V |
| **TOTAL DEVICE** | | | | | |
| Standby Supply Current | $I_{CC}$ | — | 14 | 25 | mA |
| Over-Voltage Shutdown Threshold<br>(−40°C ≤ $T_A$ ≤ +85°C) | $V_{th(OV)}$ | 16.5 | 19.5 | 22 | V |
| Over-Voltage Shutdown Hysteresis (Device off to on)<br>(−40°C ≤ $T_A$ ≤ +85°C) | $V_{H(OV)}$ | 0.3 | 0.6 | 1.0 | V |
| Operating Voltage Lower Threshold<br>(−40°C ≤ $T_A$ ≤ +85°C) | $V_{CC}$ | — | 7.5 | 8.0 | V |

NOTES:

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.
4. The upper or lower hysteresis will be lost when operating the Input, Pin 3, close to the respective rail. Refer to Figure 4.

FIGURE 1 — ERROR AMP INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

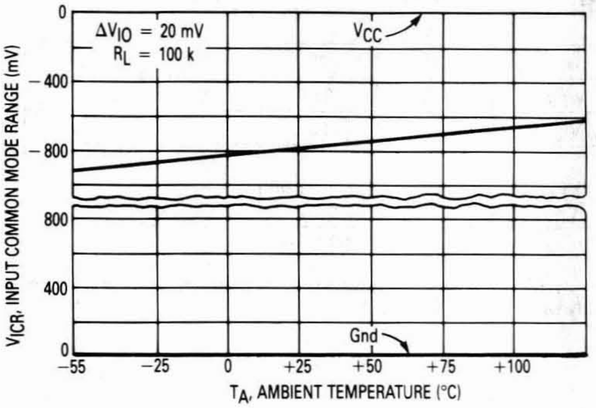


FIGURE 2 — ERROR AMP OUTPUT SATURATION versus LOAD CURRENT

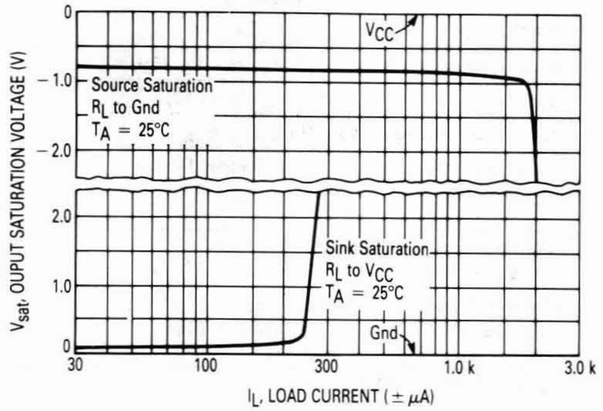


FIGURE 3 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

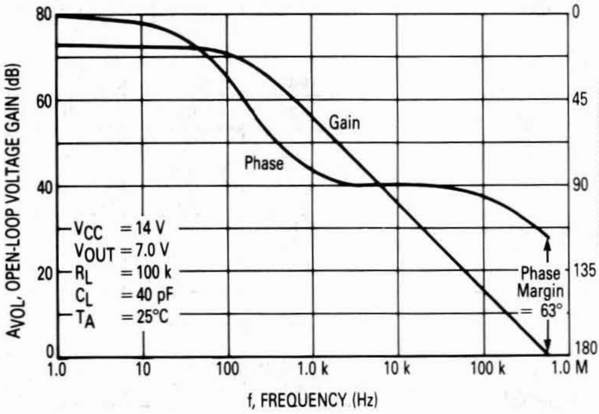


FIGURE 4 — WINDOW DETECTOR REFERENCE-INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

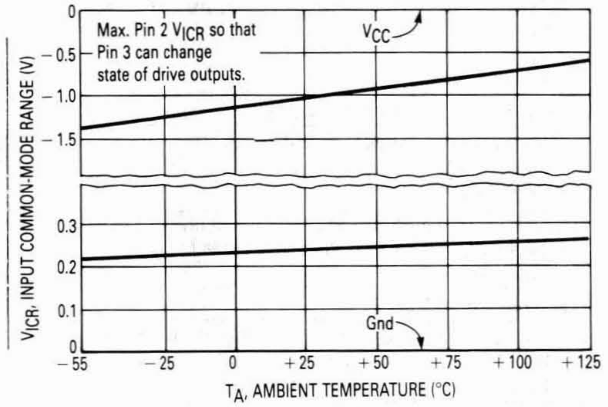


FIGURE 5 — WINDOW DETECTOR FEEDBACK-INPUT THRESHOLDS versus TEMPERATURE

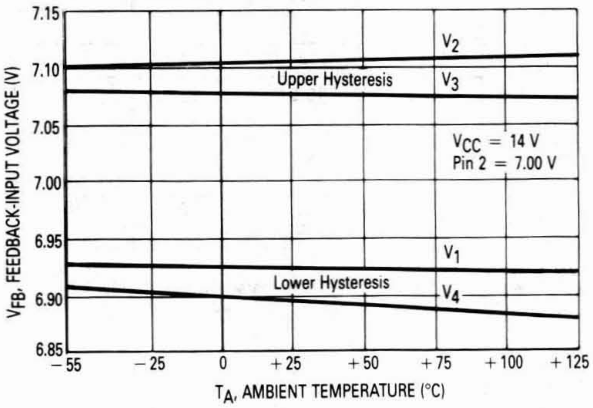


FIGURE 6 — OUTPUT DRIVE SATURATION versus LOAD CURRENT

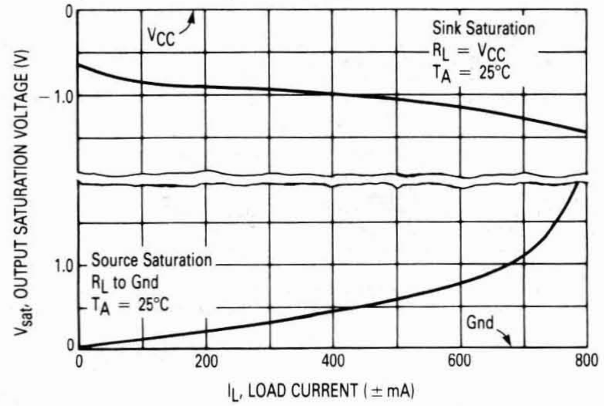


FIGURE 7 — BRAKE DIODE FORWARD CURRENT versus FORWARD VOLTAGE

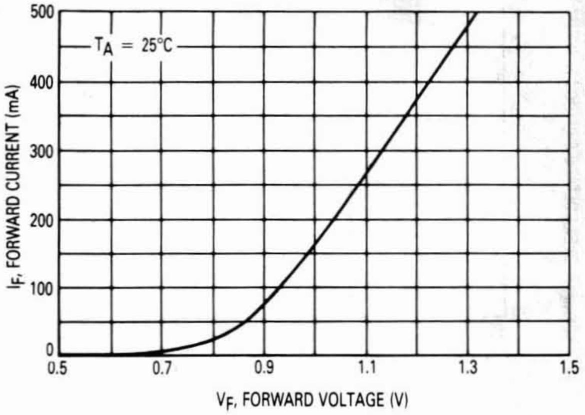


FIGURE 8 — OUTPUT SOURCE CURRENT-LIMIT versus OVER-CURRENT REFERENCE RESISTANCE

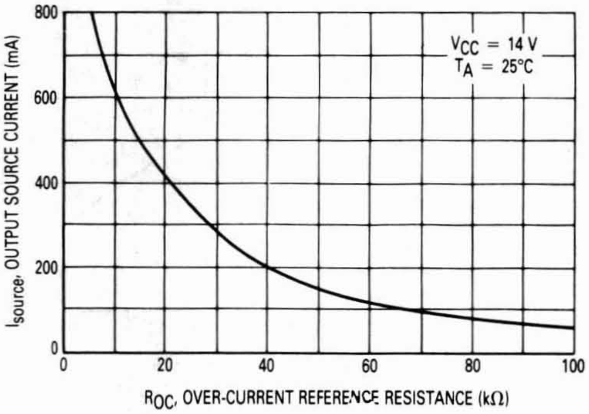


FIGURE 9 — OUTPUT SOURCE CURRENT-LIMIT versus TEMPERATURE

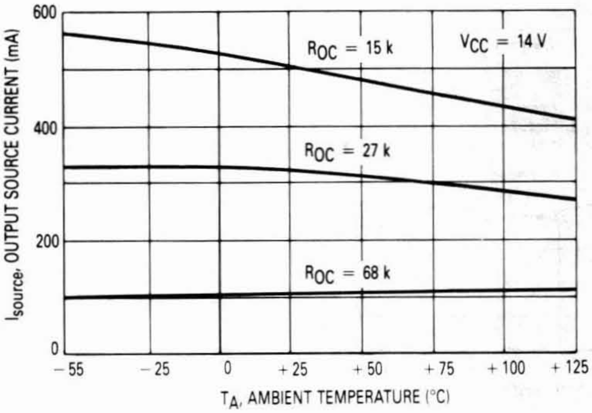


FIGURE 10 — NORMALIZED DELAY PIN SOURCE CURRENT versus TEMPERATURE

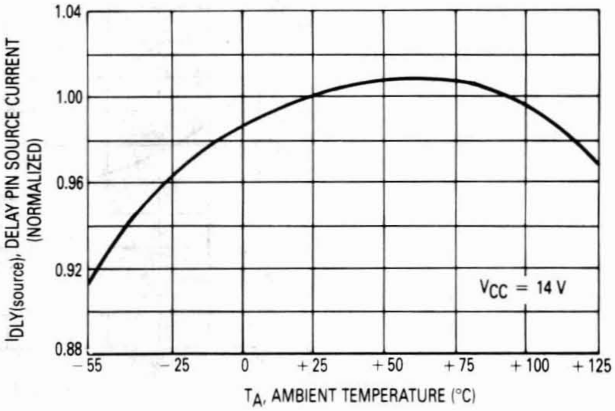


FIGURE 11 — NORMALIZED OVER-CURRENT DELAY THRESHOLD VOLTAGE versus TEMPERATURE

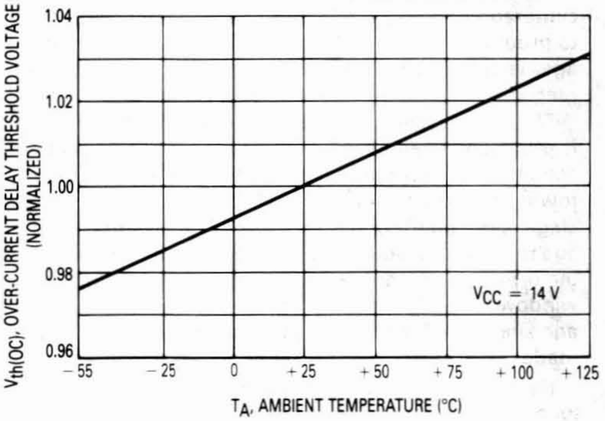


FIGURE 12 — SUPPLY CURRENT versus SUPPLY VOLTAGE

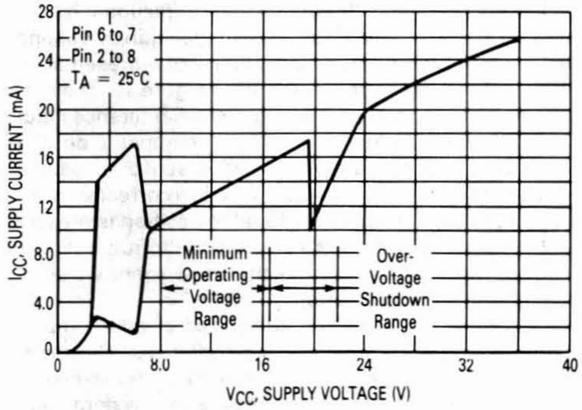


**FIGURE 13 — NORMALIZED OVER-VOLTAGE SHUTDOWN THRESHOLD versus TEMPERATURE**

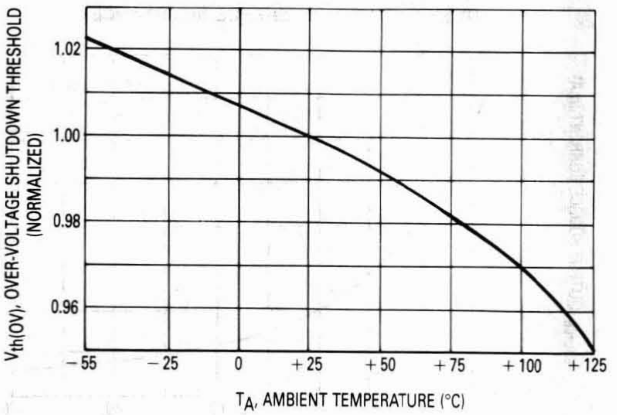


**FIGURE 14 — NORMALIZED OVER-VOLTAGE SHUTDOWN HYSTERESIS versus TEMPERATURE**

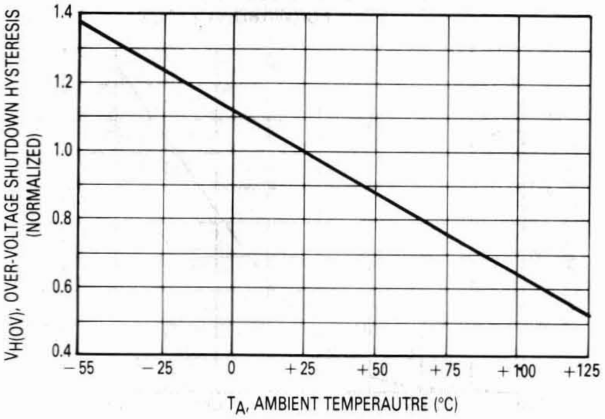
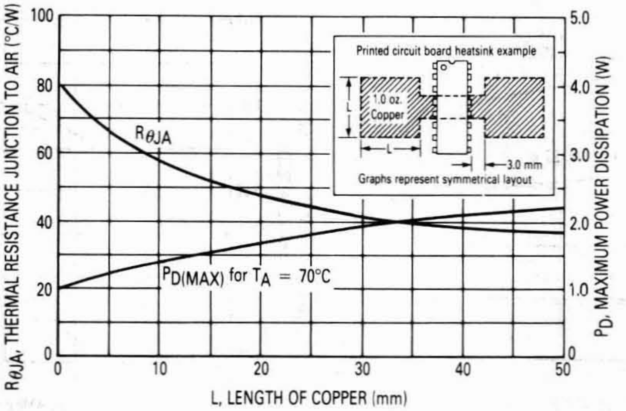


**FIGURE 15 — THERMAL RESISTANCE AND MAXIMUM POWER DISSIPATION versus P.C.B. COPPER LENGTH**



## OPERATING DESCRIPTION

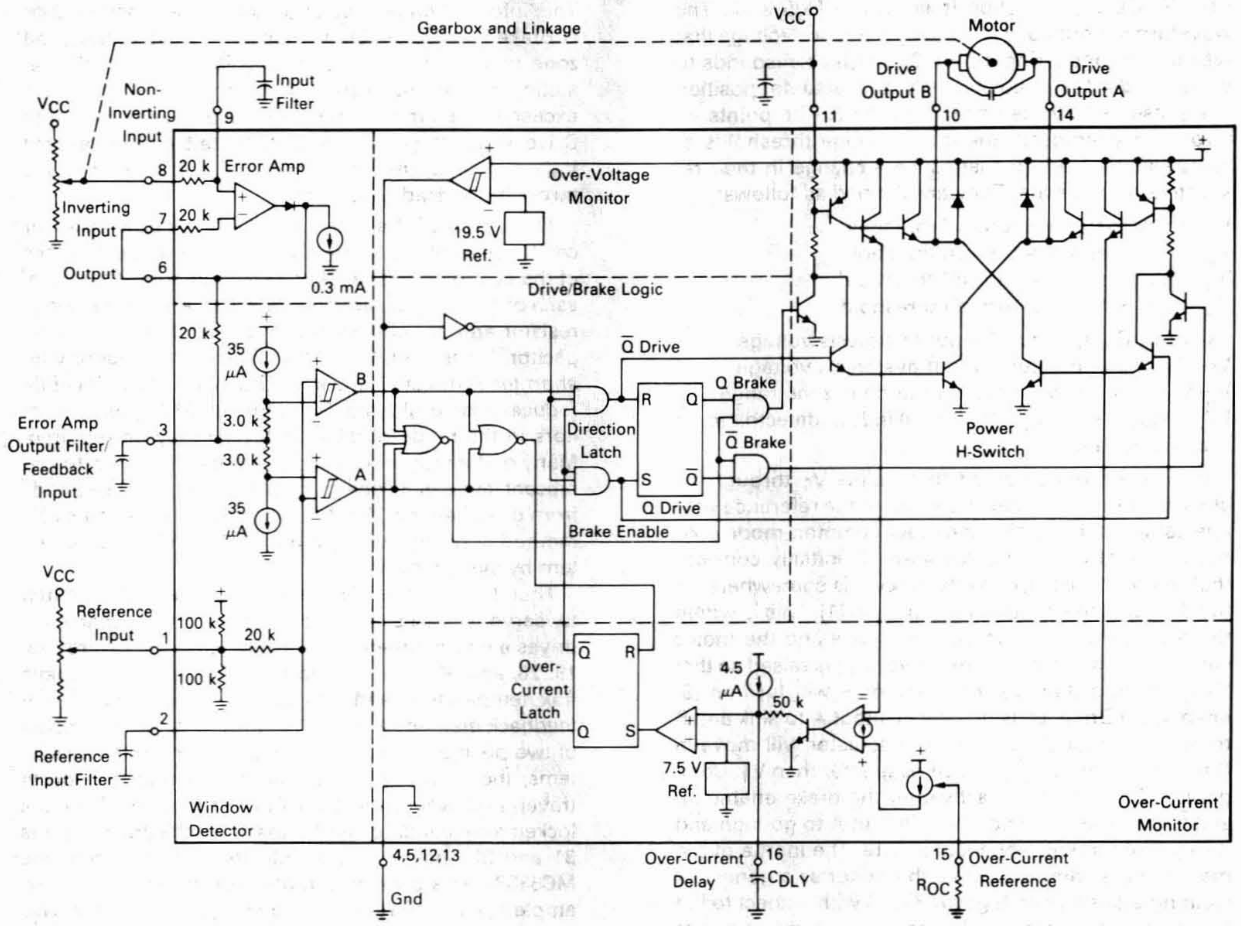
The MC33030 was designed to drive fractional horsepower dc motors and sense actuator position by voltage feedback. A typical servo application and representative internal block diagram are shown in Figure 16. The system operates by setting a voltage on the reference input of the Window Detector (Pin 1) which appears on (Pin 2). A dc motor then drives a position sensor, usually a potentiometer driven by a gear box, in a corrective fashion so that a voltage proportional to position is present at Pin 3. The servo motor will continue to run until the voltage at Pin 3 falls within the dead zone, which is centered about the reference voltage.

The Window Detector is composed of two comparators, A and B, each containing hysteresis. The reference input, common to both comparators, is pre-biased at 1/2 $V_{CC}$ for simple two position servo systems and can easily be overriden by an external voltage divider. The feedback voltage present at Pin 3 is connected to the center of two resistors that are driven by an equal magnitude current source and sink. This generates an offset voltage at the input of each comparator which is centered about Pin 3 that can float virtually from $V_{CC}$ to ground. The sum of the upper and lower offset voltages is defined as the window detector input dead zone range.

To increase system flexibility, an on-chip Error Amp is provided. It can be used to buffer and/or gain-up the actuator position voltage which has the effect of narrowing the dead zone range. A PNP differential input stage is provided so that the input common-mode voltage range will include ground. The main design goal of the error amp output stage was to be able to drive the window detector input. It typically can source 1.8 mA and sink 250 μA. Special design considerations must be made if it is to be used for other applications.

The Power H-Switch provides a direct means for motor drive and braking with a maximum source, sink, and brake current of 1.0 A continuous. Maximum package power dissipation limits must be observed. Refer to Figure 15 for thermal information. For greater drive current requirements, a method for buffering that maintains all the system features is shown in Figure 29.

FIGURE 16 — REPRESENTATIVE BLOCK DIAGRAM AND TYPICAL SERVO APPLICATION



Gearbox and Linkage
VCC
Motor
Drive Output B
Drive Output A
11
10
14
VCC
Non-Inverting Input
Input Filter
9
8
20 k
Error Amp
Inverting Input
7
20 k
Output
6
0.3 mA
Over-Voltage Monitor
19.5 V Ref.
Drive/Brake Logic
20 k
35 μA
B
Q̄ Drive
Q Brake
R
Q
Error Amp Output Filter/ Feedback Input
3
3.0 k
3.0 k
Direction Latch
Q̄ Brake
A
S
Q̄
35 μA
Q Drive
Brake Enable
Power H-Switch
VCC
Reference Input
1
100 k
20 k
100 k
2
Reference Input Filter
Q̄
R
Over-Current Latch
Q
S
4.5 μA
50 k
7.5 V Ref.
Window Detector
4,5,12,13
Gnd
Over-Current Delay
16
CDLY
15
Over-Current Reference
ROC
Over-Current Monitor

The Over-Current Monitor is designed to distinguish between motor start-up or locked rotor conditions that can occur when the actuator has reached its travel limit. A fraction of the Power H-Switch source current is internally fed into one of the two inverting inputs of the current comparator, while the non-inverting input is driven by a programmable current reference. This reference level is controlled by the resistance value selected for $R_{OC}$, and must be greater than the required motor run-current with its mechanical load over temperature; refer to Figure 8. During an over-current condition, the comparator will turn off and allow the current source to charge the delay capacitor, $C_{DLY}$. When $C_{DLY}$ charges to a level of 7.5 V, the set input of the over-current latch will go high, disabling the drive and brake functions of the Power H-Switch. The programmable time delay is determined by the capacitance value selected for $C_{DLY}$.

$$t_{DLY} = \frac{V_{ref}\,C_{DLY}}{I_{DLY(source)}} = \frac{7.5\,C_{DLY}}{4.5\,\mu A} = 1.67\,C_{DLY} \text{ in } \mu F$$

This system allows the Power H-Switch to supply motor start-up current for a predetermined amount of time. If the rotor is locked, the system will time-out and shutdown. This feature eliminates the need for servo end-of-travel or limit switches. Care must be taken so as not to select too large of a capacitance value for $C_{DLY}$. An over-current condition for an excessively long time-out period can cause the integrated circuit to overheat and eventually fail. Again, the maximum package power dissipation limits must be observed. The over-current latch is reset upon power-up or by readjusting $V_{pin\ 2}$ as to cause $V_{pin\ 3}$ to enter or pass through the dead zone. This can be achieved by requesting the motor to reverse direction.

An Over-Voltage Monitor circuit provides protection for the integrated circuit and motor by disabling the Power H-Switch functions if $V_{CC}$ should exceed 19.5 V. Resumption of normal operation will commence when $V_{CC}$ falls below 18.9 V.

A timing diagram that depicts the operation of the Drive/Brake Logic section is shown in Figure 17. The waveforms grouped in [1] show a reference voltage that was preset, appearing on Pin 2, which corresponds to the desired actuator position. The true actuator position is represented by the voltage on Pin 3. The points $V_1$ through $V_4$ represent the input voltage thresholds of comparators A and B that cause a change in their respective output state. They are defined as follows:

$V_1$ = Comparator B turn-off threshold
$V_2$ = Comparator A turn-on threshold
$V_3$ = Comparator A turn-off threshold
$V_4$ = Comparator B turn-on threshold

$V_1$–$V_4$ = Comparator B input hysteresis voltage
$V_2$–$V_3$ = Comparator A input hysteresis voltage
$V_2$–$V_4$ = Window detector input dead zone range
$|(V_2 - V_{pin2}) - (V_{pin2} - V_4)|$ = Window detector input offset voltage

It must be remembered that points $V_1$ through $V_4$ always try to follow and center about the reference voltage setting if it is within the input common-mode voltage range of Pin 3; Figures 4 and 5. Initially consider that the feedback input voltage level is somewhere on the dashed line between $V_2$ and $V_4$ in [1]. This is within the dead zone range as defined above and the motor will be off. Now if the reference voltage is raised so that $V_{pin\ 3}$ is less than $V_4$, comparator B will turn-on [3] enabling $\overline{Q}$ Drive, causing Drive Output A to sink and B to source motor current [8]. The actuator will move in Direction B until $V_{pin\ 3}$ becomes greater than $V_1$. Comparator B will turn-off, activating the brake enable [4] and $\overline{Q}$ Brake [6] causing Drive Output A to go high and B to go into a high impedance state. The inertia of the mechanical system will drive the motor as a generator creating a positive voltage on Pin 10 with respect to Pin 14. The servo system can be stopped quickly, so as not to over-shoot through the dead zone range, by braking. This is accomplished by shorting the motor/generator terminals together. Brake current will flow into the diode at Drive Output B, through the internal $V_{CC}$ rail, and out the emitter of the sourcing transistor at Drive Output A. The end of the solid line and beginning of the dashed for $V_{pin\ 3}$ [1] indicates the possible resting position of the actuator after braking.

If $V_{pin\ 3}$ should continue to rise and become greater than $V_2$, the actuator will have over shot the dead zone range and cause the motor to run in Direction A until $V_{pin\ 3}$ is equal to $V_3$. The Drive/Brake behavior for Direction A is identical to that of B. Overshooting the dead zone range in both directions can cause the servo system to continuously hunt or oscillate. Notice that the last motor run-direction is stored in the direction latch. This information is needed to determine whether Q or $\overline{Q}$ Brake is to be enabled when $V_{pin\ 3}$ enters the dead zone range. The dashed lines in [8,9] indicate the resulting waveforms of an over-current condition that has exceeded the programmed time delay. Notice that both Drive Outputs go into a high impedance state until $V_{pin\ 2}$ is readjusted so that $V_{pin\ 3}$ enters or crosses through the dead zone [7,4].

The inputs of the Error Amp and Window Detector can be susceptible to the noise created by the brushes of the dc motor and cause the servo to hunt. Therefore, each of these inputs are provided with an internal series resistor and are pinned out for an external bypass capacitor. It has been found that placing a capacitor with *short leads* directly across the brushes will significantly reduce noise problems. Good quality RF bypass capacitors in the range of 0.001 to 0.1 $\mu$F may be required. Many of the more economical motors will generate significant levels of RF energy over a spectrum that extends from dc to beyond 200 MHz. The capacitance value and method of noise filtering must be determined on a system by system basis.

Thus far, the operating description has been limited to servo systems in which the motor mechanically drives a potentiometer for position sensing. Figures 18, 19, 26, and 30 show examples that use light, magnetic flux, temperature, and pressure as a means to drive the feedback element. Figures 20, 21 and 22 are examples of two position, open-loop servo systems. In these systems, the motor runs the actuator to each end of its travel limit where the Over-Current Monitor detects a locked rotor condition and shuts down the drive. Figures 31 and 32 show two possible methods of using the MC33030 as a switching motor controller. In each example a fixed reference voltage is applied to Pin 2. This causes $V_{pin\ 3}$ to be less than $V_4$ and Drive Output A, Pin 14, to be in a low state saturating the TIP42 transistor. In Figure 31, the motor drives a tachometer that generates an ac voltage proportional to RPM. This voltage is rectified, filtered, divided down by the speed set potentiometer, and applied to Pin 8. The motor will accelerate until $V_{pin\ 3}$ is equal to $V_1$ at which time Pin 14 will go to a high state and terminate the motor drive. The motor will now coast until $V_{pin\ 3}$ is less than $V_4$ where upon drive is then reapplied. The system operation of Figure 32 identical to that of 31 except the signal at Pin 3 is an amplified average of the motors drive and back EMF voltages. Both systems exhibit excellent control of RPM with variations of $V_{CC}$; however, Figure 31 has somewhat better torque characteristics at low RPM.

**FIGURE 17 — TIMING DIAGRAM**

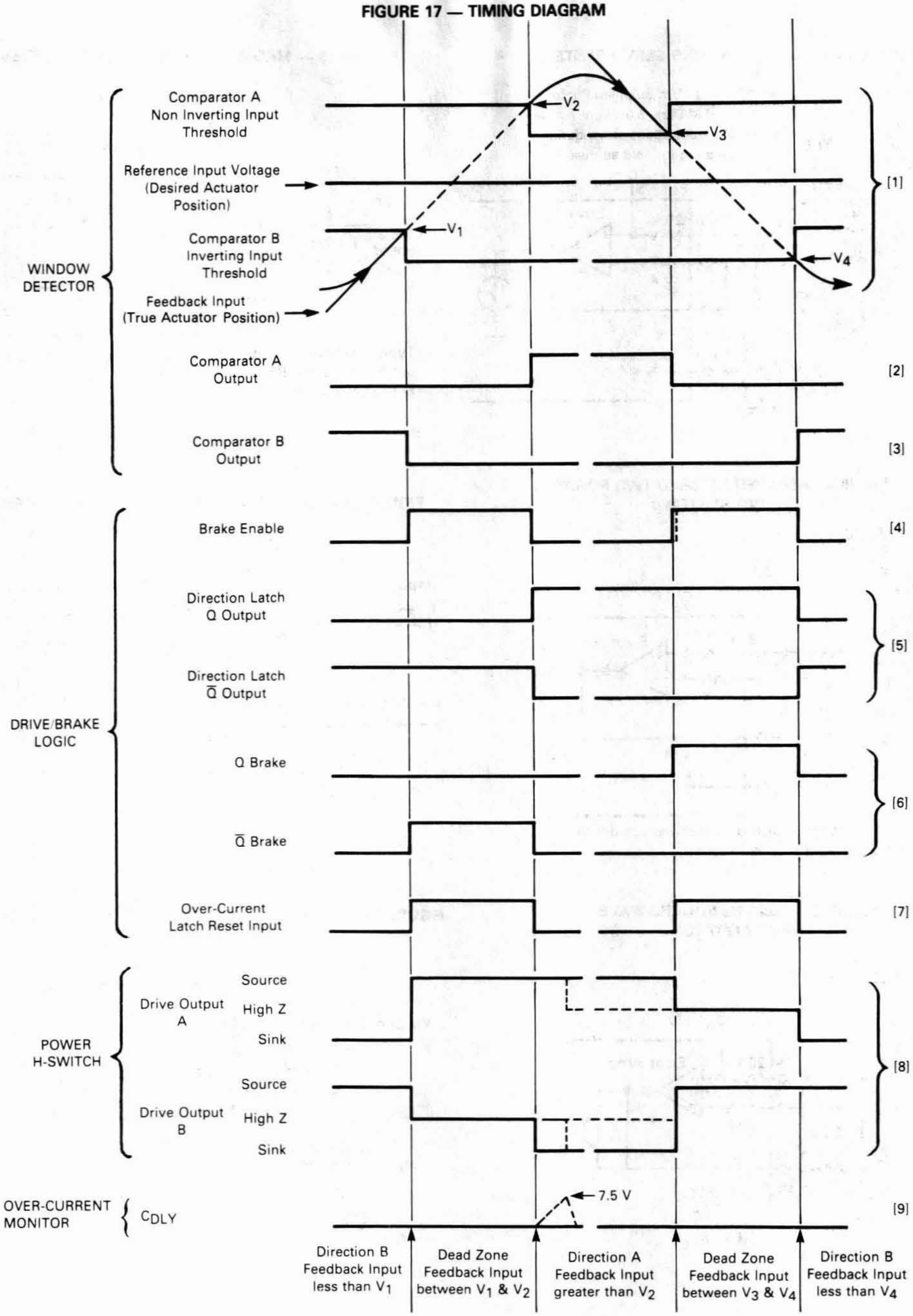
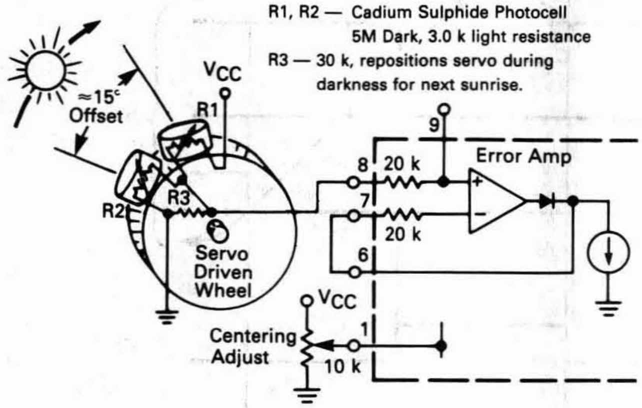

WINDOW DETECTOR
Comparator A Non Inverting Input Threshold
Reference Input Voltage (Desired Actuator Position)
Comparator B Inverting Input Threshold
Feedback Input (True Actuator Position)
V1
V2
V3
V4
[1]
Comparator A Output
[2]
Comparator B Output
[3]
DRIVE/BRAKE LOGIC
Brake Enable
[4]
Direction Latch Q Output
Direction Latch Q̄ Output
[5]
Q Brake
Q̄ Brake
[6]
Over-Current Latch Reset Input
[7]
POWER H-SWITCH
Drive Output A
Drive Output B
Source
High Z
Sink
[8]
OVER-CURRENT MONITOR
CDLY
7.5 V
[9]
Direction B Feedback Input less than V1
Dead Zone Feedback Input between V1 & V2
Direction A Feedback Input greater than V2
Dead Zone Feedback Input between V3 & V4
Direction B Feedback Input less than V4

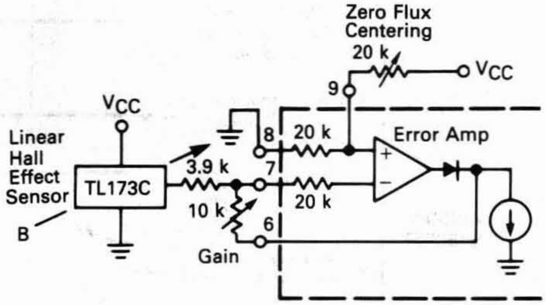
FIGURE 18 — SOLAR TRACKING SERVO SYSTEM


≈15° Offset
R1
R2
R3
VCC
Servo Driven Wheel
9
8
7
6
1
20 k
20 k
Error Amp
VCC
Centering Adjust
10 k

R1, R2 — Cadium Sulphide Photocell 5M Dark, 3.0 k light resistance

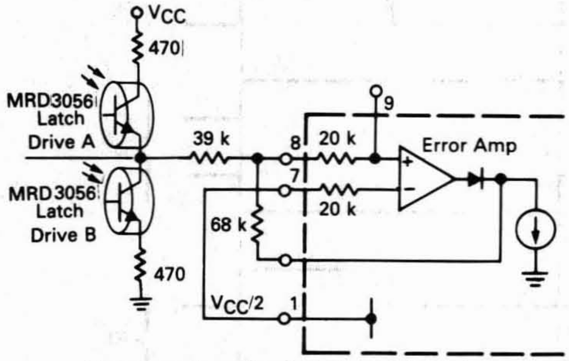
R3 — 30 k, repositions servo during darkness for next sunrise.

FIGURE 19 — MAGNETIC SENSING SERVO SYSTEM


Zero Flux Centering
20 k
VCC
9
VCC
Linear Hall Effect Sensor
B
TL173C
3.9 k
10 k
Gain
8
7
6
20 k
20 k
Error Amp

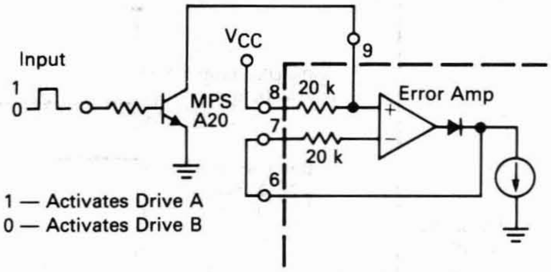
Typical sensitivity with gain set at 3.9 k is 1.5 mV/gauss. Servo motor controls magnetic field about sensor.

FIGURE 20 — INFRARED LATCHED TWO POSITION SERVO SYSTEM


VCC
470
MRD3056 Latch Drive A
MRD3056 Latch Drive B
470
39 k
68 k
VCC/2
9
8
7
1
20 k
20 k
Error Amp

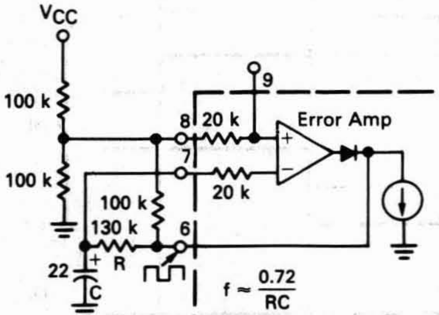
Over-current monitor (not shown) shuts down servo when end stop is reached.

FIGURE 21 — DIGITAL TWO POSITION SERVO SYSTEM


Input
1
0
MPS A20
VCC
9
8
7
6
20 k
20 k
Error Amp
1 — Activates Drive A
0 — Activates Drive B

Over-Current monitor (not shown) shuts down servo when end stop is reached.

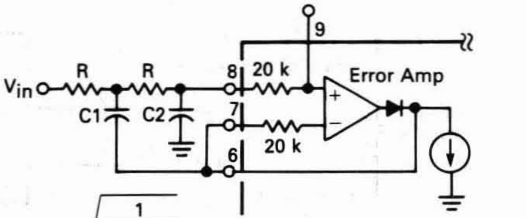
FIGURE 22 — 0.25 Hz SQUARE-WAVE SERVO AGITATOR


VCC
100 k
100 k
100 k
130 k
22
C
R
9
8
7
6
20 k
20 k
Error Amp

$f \approx \frac{0.72}{RC}$

$R \geq 20\ k$

FIGURE 23 — SECOND ORDER LOW-PASS ACTIVE FILTER

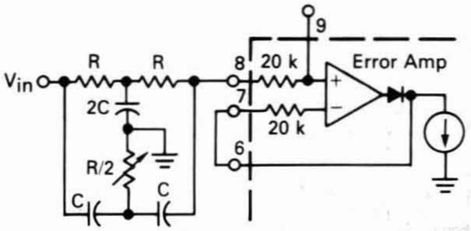

Vin
R
R
C1
C2
9
8
7
6
20 k
20 k
Error Amp

$$f_o = \frac{\sqrt{\frac{1}{R^2\ C1C2}}}{2\pi}$$

$$Q = \frac{\sqrt{\frac{C1}{C2}}}{2}$$

For 500 Hz: R = 1.0 M
C1 = 1000 pF
C2 = 100 pF

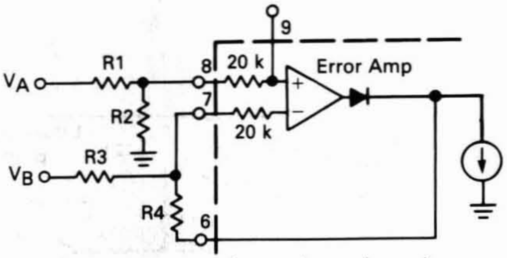
FIGURE 24 — NOTCH FILTER


Vin
R
R
2C
R/2
C
C
8
7
6
9
20 k
20 k
Error Amp
+
−

$$f_{notch} = \frac{1}{2\pi RC}$$

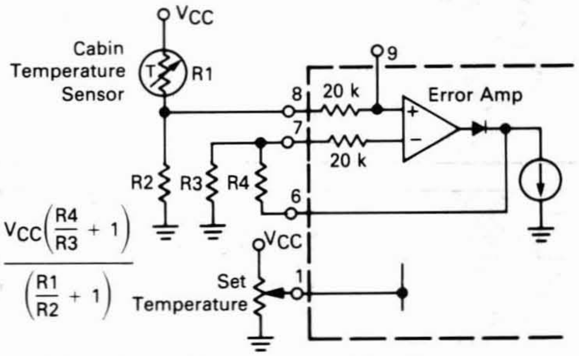
For 60 Hz R = 53.6 k, C = 0.05

FIGURE 25 — DIFFERENTIAL INPUT AMPLIFIER


VA
VB
R1
R2
R3
R4
8
7
6
9
20 k
20 k
Error Amp
+
−

$$V_{pin6} = V_A\left(\frac{R3+R4}{R1+R2}\right)\frac{R2}{R3} - \left(\frac{R4}{R3}V_B\right)$$

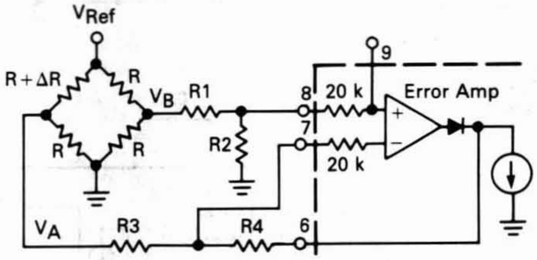
FIGURE 26 — TEMPERATURE SENSING SERVO SYSTEM


VCC
Cabin Temperature Sensor
T
R1
R2
R3
R4
8
7
6
9
1
20 k
20 k
Error Amp
+
−
VCC
Set Temperature

$$V_{pin\,6} = \frac{V_{CC}\left(\frac{R4}{R3}+1\right)}{\left(\frac{R1}{R2}+1\right)}$$

In this application the servo motor drives the heat/air conditioner modulator door in a duct system.

FIGURE 27 — BRIDGE AMPLIFIER

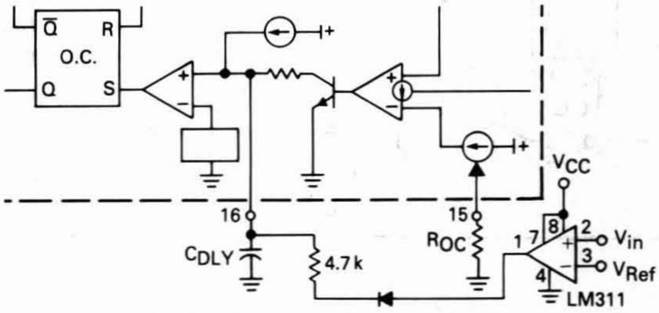

VRef
R + ΔR
R
R
R
VB
R1
R2
VA
R3
R4
8
7
6
9
20 k
20 k
Error Amp
+
−

$$V_A - V_B = V_{Ref}\left(\frac{\Delta R}{4R+2\Delta R}\right)$$

R1 = R3, R2 = R4, R1 >> R

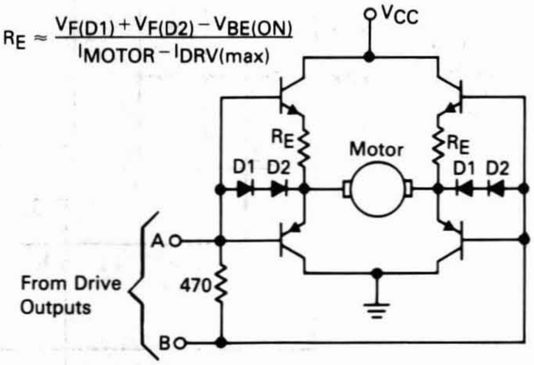
$$V_{pin6} = \frac{R4}{R3}(V_A - V_B)$$

FIGURE 28 — REMOTE LATCHED SHUTDOWN


Q̄
R
O.C.
Q
S
+
−
+
−
+
+
VCC
16
15
CDLY
4.7 k
ROC
1
7
8
2
3
4
Vin
VRef
LM311

A direction change signal is required at Pins 2 or 3 to reset the over-current latch.

FIGURE 29 — POWER H-SWITCH BUFFER


VCC
RE
RE
Motor
D1
D2
D1
D2
A
470
B
From Drive Outputs

$$R_E \approx \frac{V_{F(D1)} + V_{F(D2)} - V_{BE(ON)}}{I_{MOTOR} - I_{DRV(max)}}$$

This circuit maintains the brake and over-current features of the MC33030. Set $R_{OC}$ to 15 k for $I_{DRV(max)} \approx 0.5$ A.

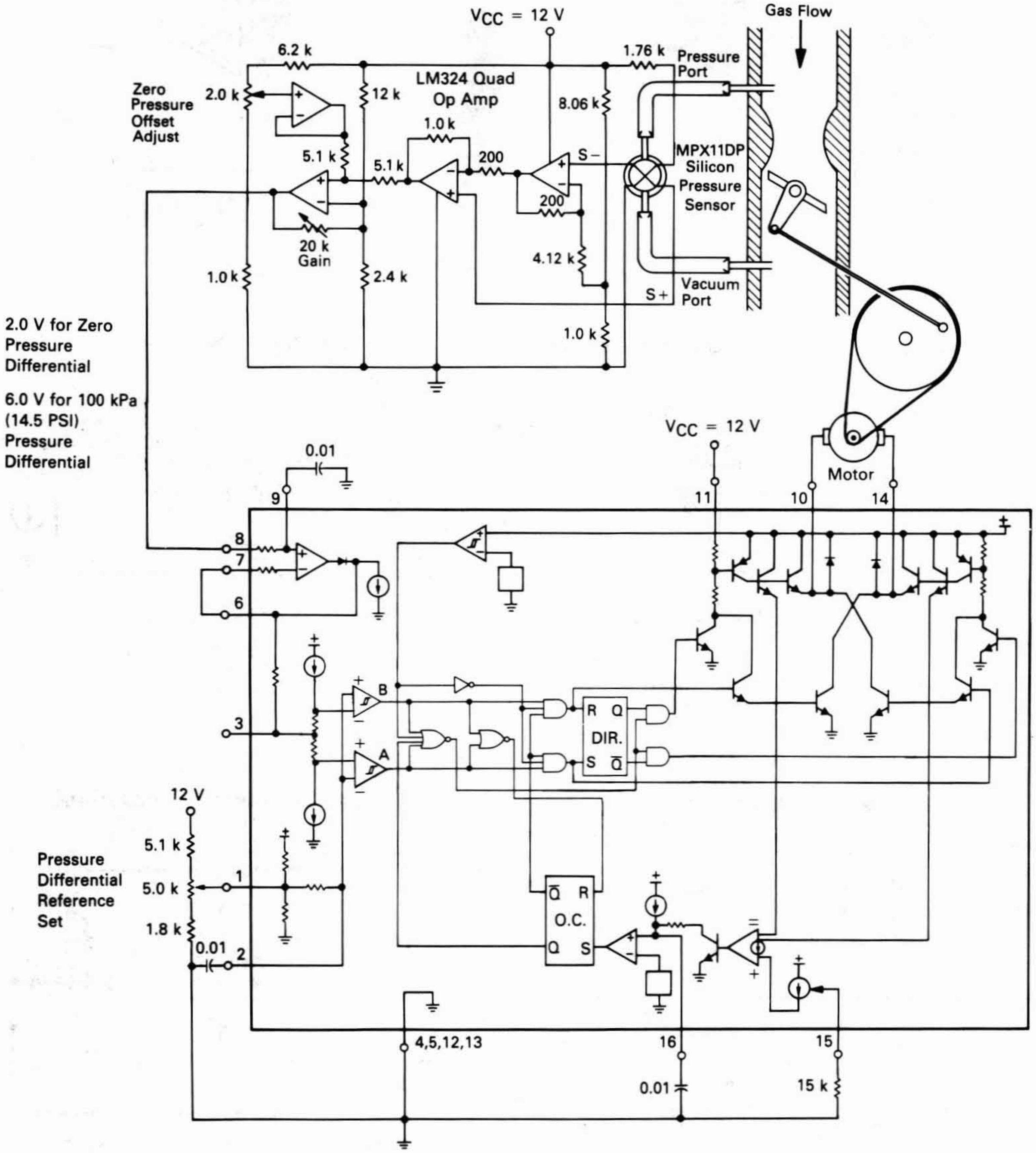


FIGURE 30 — ADJUSTABLE PRESSURE DIFFERENTIAL REGULATOR

VCC = 12 V
Gas Flow
6.2 k
1.76 k
Pressure Port
LM324 Quad Op Amp
Zero Pressure Offset Adjust
2.0 k
12 k
8.06 k
1.0 k
5.1 k
5.1 k
200
S−
MPX11DP Silicon Pressure Sensor
200
20 k Gain
4.12 k
1.0 k
2.4 k
S+
Vacuum Port
1.0 k
2.0 V for Zero Pressure Differential
6.0 V for 100 kPa (14.5 PSI) Pressure Differential
VCC = 12 V
Motor
0.01
9
11
10
14
8
7
6
B
A
3
R Q
DIR.
S Q̄
12 V
5.1 k
Pressure Differential Reference Set
5.0 k
1
1.8 k
0.01
2
Q̄ R
O.C.
Q S
4,5,12,13
16
15
0.01
15 k

FIGURE 31 — SWITCHING MOTOR CONTROLLER WITH BUFFERED OUTPUT AND TACH FEEDBACK

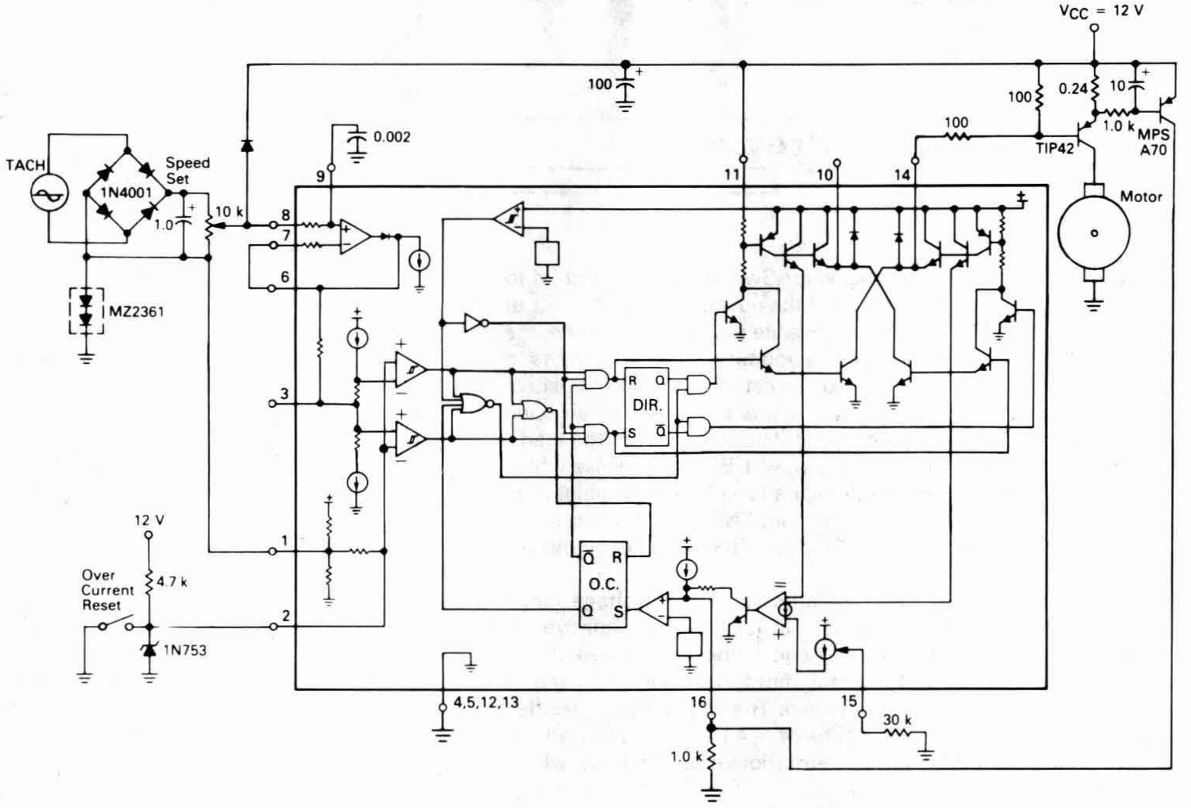
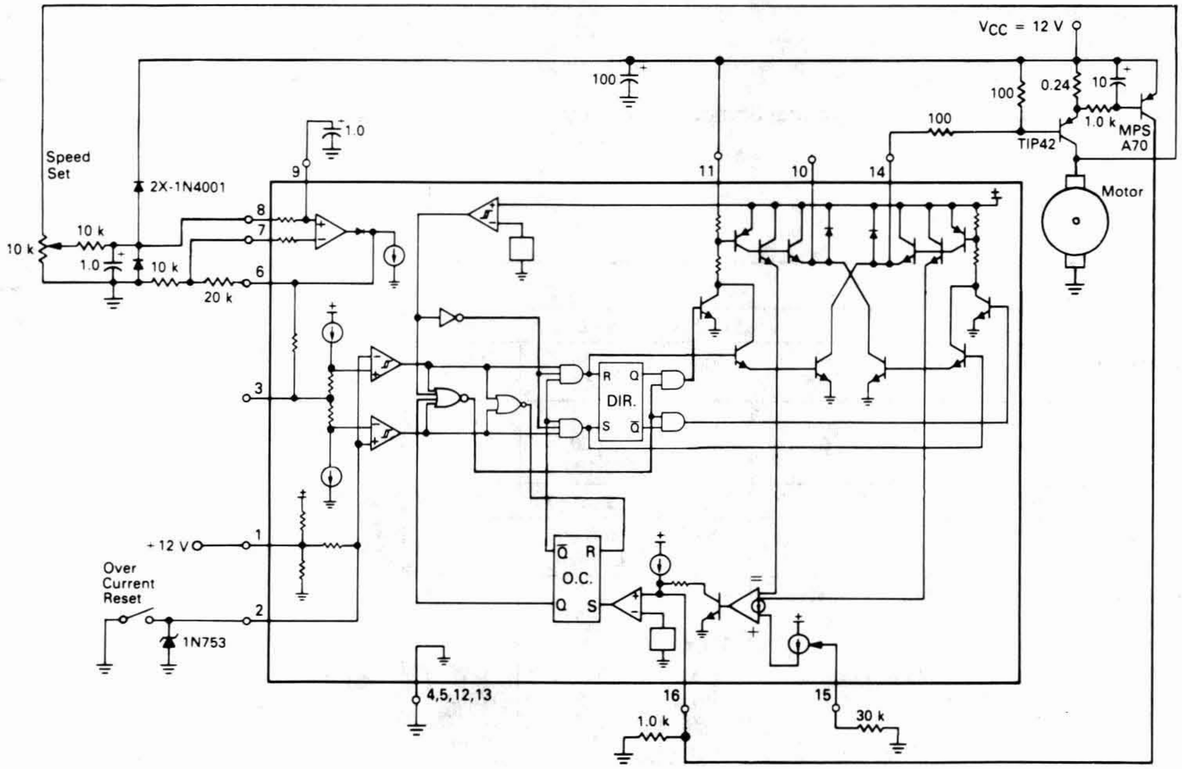

VCC = 12 V
100
0.24
10
1.0 k
MPS A70
100
TIP42
Motor
100
0.002
TACH
Speed Set
1N4001
10 k
1.0
MZ2361
9
11
10
14
8
7
6
3
12 V
Over Current Reset
4.7 k
1N753
1
2
R
Q
DIR.
S
Q̄
Q̄
R
O.C.
Q
S
4,5,12,13
16
15
30 k
1.0 k

FIGURE 32 — SWITCHING MOTOR CONTROLLER WITH BUFFERED OUTPUT AND BACK EMF SENSING


VCC = 12 V
100
0.24
10
100
1.0 k
MPS A70
100
TIP42
Motor
1.0
Speed Set
2X-1N4001
10 k
10 k
1.0
10 k
20 k
9
11
10
14
8
7
6
3
+12 V
1
Over Current Reset
2
1N753
R
Q
DIR.
S
Q̄
Q̄
R
O.C.
Q
S
4,5,12,13
16
1.0 k
15
30 k

**MOTOROLA**

# MC33038

## Product Preview

## HIGH-SIDE DRIVER SWITCH

### SILICON MONOLITHIC INTEGRATED CIRCUIT

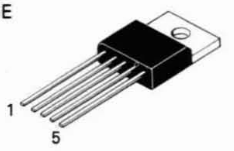
The MC33038 is a High-Side Driver Switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive or negative going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC33038 is fabricated on a power BIMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.

The device operates over a wide power supply voltage range and can withstand voltage transients (positive or negative) of ±100 V. A rugged PNP output stage along with active clamp circuitry, current limit and thermal shutdown permits driving of all types of loads including inductive. The MC33038 is specified over a wide junction temperature of −40°C to +125°C and is ideally suited for industrial and automotive applications where harsh environments exist.

- Low Switch Voltage Drop
- Load Currents in Excess of 750 mA
- Low Quiescent Current
- Transient Protection Up to ±100 V
- TTL Compatible Enable Input
- On-Chip Current Limit and Thermal Shutdown Circuitry

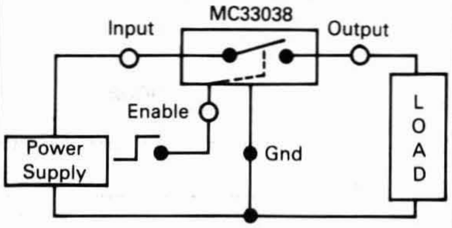
**T SUFFIX**
PLASTIC PACKAGE
CASE 314D-01
TO-220AB



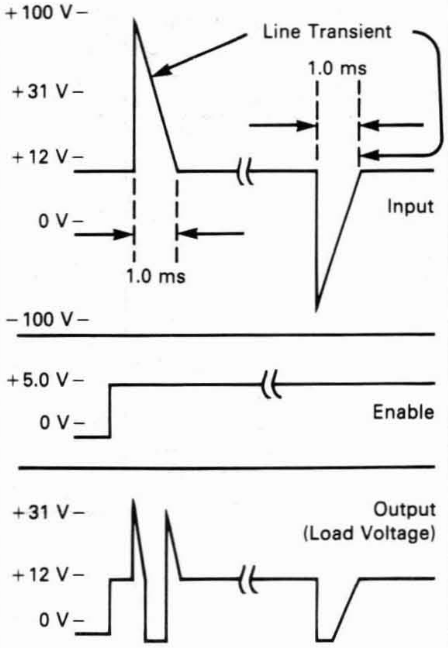
Pin 1. Input
2. N.C.
3. Output
4. Ground
5. Enable

(Heatsink surface connected to Pin 2)

**BLOCK DIAGRAM**



**TIMING DIAGRAM**



## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage — Continuous | $V_{in}$ | +55<br>−12 | Vdc |
| Input Voltage — Transient<br>t = 100 ms<br>t = 1.0 ms | $V_{in(t)}$ | <br>±60<br>±100 | V |
| Enable Input Voltage | $V_{en}$ | −0.3 to +7.0 | V |
| Output Current | $I_O$ | Internally Limited | A |
| Power Dissipation and Thermal Characteristics | | | |
| $T_A = +25°C$ | $P_D$ | 2.0 | Watts |
| Derate above $T_A = +25°C$ | $1/\theta_{JA}$ | 16 | mW/°C |
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | 62.5 | °C/W |
| $T_C = +25°C$ | $P_D$ | 25 | Watts |
| Derate above $T_C = +25°C$ | $1/\theta_{JA}$ | 200 | mW/°C |
| Thermal Resistance Junction to Case | $\theta_{JA}$ | 5.0 | °C/W |
| Operating Junction Temperature Range | $T_J$ | −40 to +150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

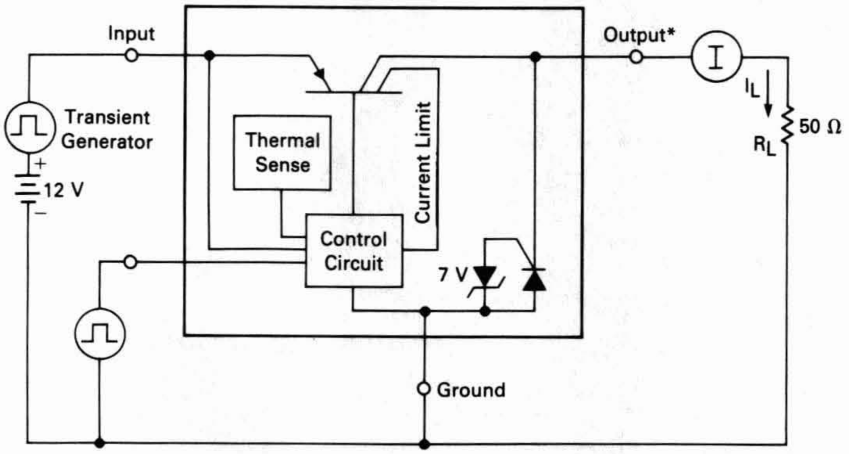
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = +12 V, $I_L$ = 150 mA, −40°C ≤ $T_J$ = +125°C, Enable = "1" unless noted)*

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Voltage | $V_{in(min)}$ | 4.5 | — | — | V |
| Quiescent Current | $I_B$ | | | | mA |
| $I_L$ = 150 mA, $V_{in}$ = +4.5 V | | — | 3.0 | 10 | |
| $I_L$ = 500 mA, $V_{in}$ = +12 V | | — | 8.0 | 15 | |
| $I_L$ = 750 mA, $V_{in}$ = +24 V | | — | 15 | 75 | |
| $I_L$ = 0 mA, $V_{in}$ = +12 V, Enable = "0" | | — | — | 0.08 | |
| Switch Voltage Drop | $V_{in}–V_O$ | | | | mV |
| $I_L$ = 150 mA, $V_{in}$ = +4.5 V | | — | 125 | 200 | |
| $I_L$ = 500 mA, $V_{in}$ = +12 V | | — | 300 | 500 | |
| $I_L$ = 750 mA, $V_{in}$ = +24 V | | — | 425 | 750 | |
| Output Current Limit<br>$V_O$ = 0 V | $I_{SC}$ | 0.8 | 1.5 | 2.5 | A |
| Output Leakage Current<br>$V_{in}$ = 24 V, Enable = "0" | $I_{Leak}$ | — | 10 | 150 | µA |
| Enable Input Voltage | | | | | V |
| High Logic State | $V_{IH}$ | 2.0 | — | — | |
| Low Logic State | $V_{IH}$ | — | — | 0.8 | |
| Enable Input Current | | | | | µA |
| High Logic State ($V_{IH}$ = 5.5 V) | $I_{IH}$ | — | 120 | — | |
| Low Logic State ($V_{IL}$ = 0.4 V) | $I_{IL}$ | — | 20 | — | |
| Output Turn-On Delay Time<br>Enable = "0" → "1", $T_J$ = +25°C (Figures 3 and 4) | $t_{DLY(on)}$ | — | 5.0 | — | µs |
| Output Turn-Off Delay Time<br>Enable = "1" → "0", $T_J$ = +25°C (Figures 3 and 4) | $t_{DLY(off)}$ | — | 50 | — | µs |
| Over Voltage Shutdown Threshold | $V_{in(OV)}$ | 26 | 31 | 36 | V |
| Output Turn-Off Delay Time<br>($T_J$ = +25°C) to Over Voltage Condition, $V_{in}$ stepped from 12 V to 40 V<br>V ≤ 0.9 $V_O$ (Figures 3 and 4) | $t_{DLY(OV)}$ | — | 2.0 | — | µs |
| Output Recovery Delay Time<br>($T_J$ = +25°C) $V_{in}$ stepped from 40 V to 12 V, V ≥ 0.9 $V_O$ (Figures 3 and 4) | $t_{RCVY}$ | — | 5.0 | — | µs |

NOTES:
*Typical Values Represent Characteristics of Operation at $T_J$ = +25°C.

**FIGURE 3 — TRANSIENT RESPONSE TEST CIRCUIT**



NOTE:
*Depending on Load Current and Transient Duration, an Output Capacitor ($C_O$) of sufficient value may be used to hold up Output Voltage during the Transient, and absorb Turn-off Delay Voltage Overshoot.

**FIGURE 4 — RESPONSE TIME DIAGRAM**

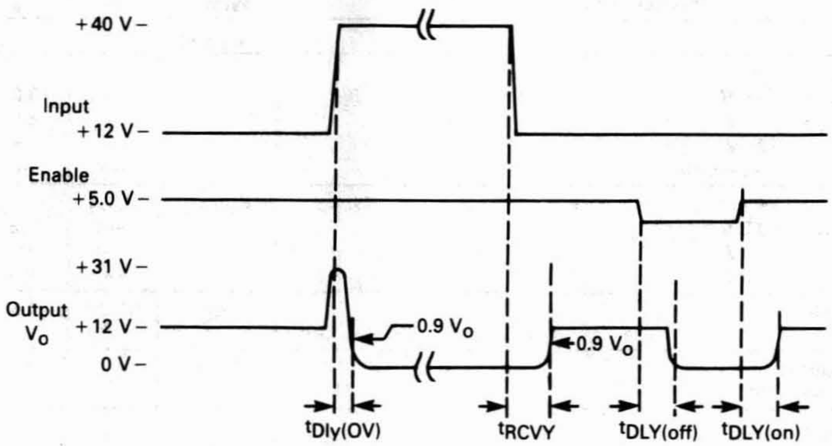

+40 V –
Input
+12 V –
Enable
+5.0 V –
+31 V –
Output
$V_O$
+12 V –
0 V –
0.9 $V_O$
0.9 $V_O$
$t_{Dly(OV)}$
$t_{RCVY}$
$t_{DLY(off)}$
$t_{DLY(on)}$

**FIGURE 5 — SWITCH VOLTAGE DROP versus LOAD CURRENT**

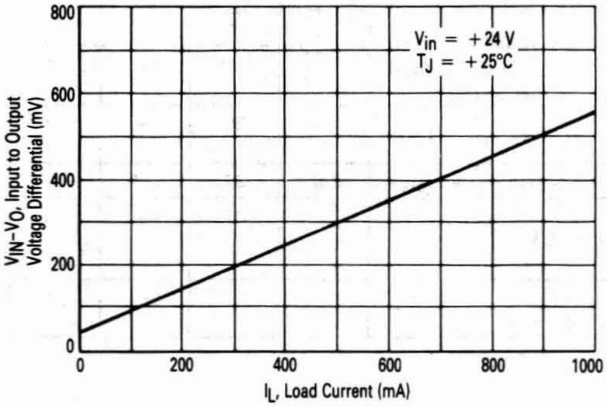
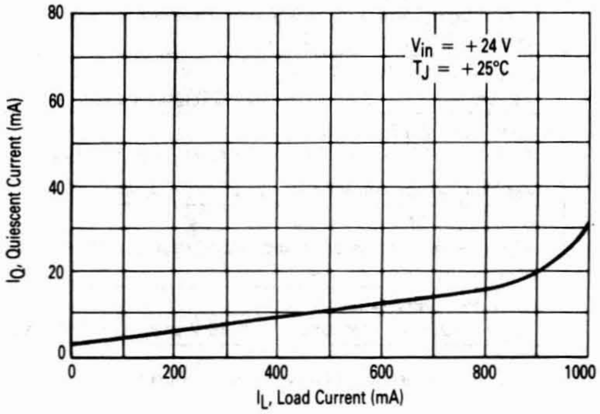


**FIGURE 6 — QUIESCENT CURRENT versus LOAD CURRENT**



**MOTOROLA**

# SAA1042
# SAA1042A

## Specifications and Applications Information

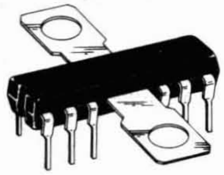
### STEPPER MOTOR DRIVER

The SAA1042 drives a two-phase stepper motor in the bipolar mode. The device contains: three input stages, a logic section and two output stages.

- Drive Stages Designed for Motors: 6.0 V and 12 V: SAA1042
  24 V: SAA1042A
- 500 mA/Coil Drive Capability
- Built-In Clamp Diodes for Overvoltage Suppression
- Wide Logic Supply Voltage Range
- Accepts Commands for CW/CCW and Half/Full Step Operation
- Inputs Compatible with Popular Logic Families: MOS, TTL, DTL
- Set Input Defined Output State
- Drive Stage Bias Adaptable to Motor Power Dissipation for Optimum Efficiency

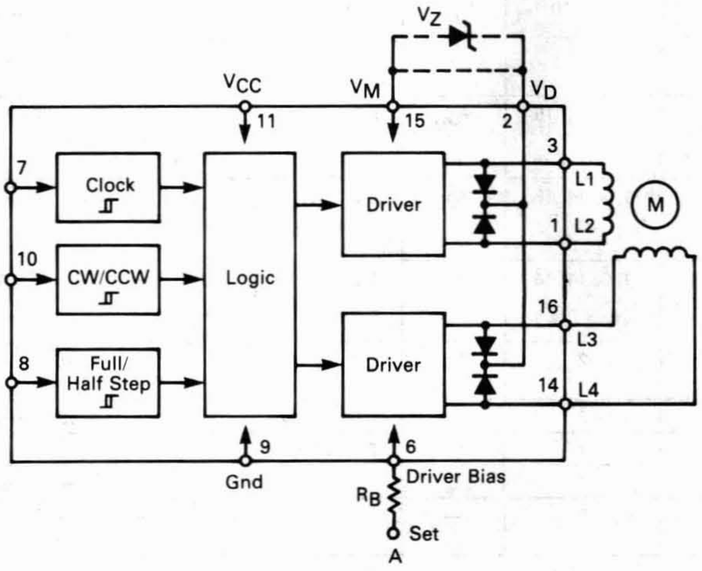
### STEPPER MOTOR DRIVER

**SILICON MONOLITHIC**
**INTEGRATED CIRCUIT**

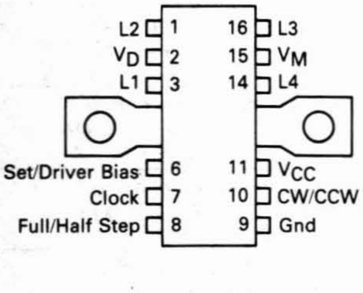


PLASTIC PACKAGE
CASE 721-02

**FIGURE 1 — SAA1042 BLOCK DIAGRAM**


$V_Z$
$V_{CC}$
$V_M$
$V_D$
11
15
2
3
7
Clock
Logic
Driver
L1
1
L2
M
10
CW/CCW
16
L3
8
Full/
Half Step
Driver
14
L4
9
6
Gnd
Driver Bias
$R_B$
Set
A

**PIN ASSIGNMENT**


L2 1
$V_D$ 2
L1 3
Set/Driver Bias 6
Clock 7
Full/Half Step 8
16 L3
15 $V_M$
14 L4
11 $V_{CC}$
10 CW/CCW
9 Gnd

(Top View)

Note: Case heat sink is electrically connected to ground (Pin 9) through the die substrate.

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise stated)

| Rating | Symbol | SAA1042 | SAA1042A | Unit |
|---|---|---|---|---|
| Clamping Voltage (Pins 1, 3, 14 & 16) | $V_{clamp}$ | 20 | 30 | V |
| Over Voltage ($V_{OV} = V_{clamp} - V_M$) | $V_{OV}$ | 6.0 | | V |
| Supply Voltage | $V_{CC}$ | 20 | 30 | V |
| Switching or Motor Current/Coil | $I_M$ | 500 | | mA |
| Input Voltage (Pins 7, 8 & 10) | $V_{in}$ clock<br>$V_{in}$ Full/Half<br>$V_{in}$ CW/CCW | $V_{CC}$ | | V |
| Power Dissipation | $P_D$* | 2.0 | | W |
| Derate above $T_A$ = 25°C | $1/\theta_{JA}$ | 20 | | mW/°C |
| Thermal Resistance, Junction to Air | $\theta_{JA}$ | 50 | | °C/W |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | 8.0 | | °C/W |
| Operating Junction Temperature Range | $T_J$ | −30 to +125 | | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | | °C |

*The power dissipation, $P_D$, of the circuit is given by the supply voltage, $V_M$ and $V_{CC}$, and the motor current, $I_M$, and can be determined from Figures 3 and 5. $P_D = P_{drive} + P_{logic}$.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = +25°C)

| Characteristic | Pin | Symbol | $V_{CC}$ | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply Current | 11 | $I_{CC}$ | 5.0 V | — | — | 3.5 | mA |
| | | | 20 V | — | — | 8.5 | |
| Motor Supply Current<br>(I Pin 6 = −400 μA, Pins 1, 3, 14, 16 Open) | 15 | $I_M$ | | | | | mA |
| $V_M$ = 6.0 V | | | 5.0 V | — | 25 | — | |
| $V_M$ = 12 V | | | 5.0 V | — | 30 | — | |
| $V_M$ = 24 V | | | 5.0 V | — | 40 | — | |
| Input Voltage — High State | 7, 8, 10 | $V_{IH}$ | 5.0 V | 2.0 | — | — | V |
| | | | 10 V | 7.0 | — | — | |
| | | | 15 V | 10 | — | — | |
| | | | 20 V | 14 | — | — | |
| Input Voltage — Low State | 7, 8, 10 | $V_{IL}$ | 5.0 V | — | — | 0.8 | V |
| | | | 10 V | — | — | 1.5 | |
| | | | 15 V | — | — | 2.5 | |
| | | | 20 V | — | — | 3.5 | |
| Input Reverse Current — High State<br>($V_{in} = V_{CC}$) | 7, 8, 10 | $I_{IR}$ | 5.0 V | — | — | 2.0 | μA |
| | | | 10 V | — | — | 2.0 | |
| | | | 15 V | — | — | 3.0 | |
| | | | 20 V | — | — | 5.0 | |
| Input Forward Current — Low State<br>($V_{in}$ = Gnd) | 7, 8, 10 | $I_{IF}$ | 5.0 V | −10 | — | — | μA |
| | | | 10 V | −25 | — | — | |
| | | | 15 V | −40 | — | — | |
| | | | 20 V | −55 | — | — | |
| Output Voltage — High State | 1, 3, 14, 16 | $V_{OH}$ | 5.0 to 20 V | | | | V |
| ($V_M$ = 12 V) $I_{out}$ = −500 mA | | | | — | $V_M - 2.0$ | — | |
| $I_{out}$ = − 50 mA | | | | — | $V_M - 1.2$ | — | |
| Output Voltage — Low State | 1, 3, 14, 16 | $V_{OL}$ | 5.0 to 20 V | | | | V |
| $I_{out}$ = 500 mA | | | | — | 0.7 | — | |
| $I_{out}$ = 50 mA | | | | — | 0.2 | — | |
| Output Leakage Current<br>($V_M = V_D = V_{clamp\ max.}$)<br>Pin 6: Open | 1, 3, 14, 16 | $I_{DR}$ | 5.0 to 20 V | −100 | — | — | μA |
| Clamp Diode Forward Voltage<br>(Drop at $I_M$ = 500 mA) | 2 | $V_F$ | — | — | 2.5 | 3.5 | V |
| Clock Frequency | 7 | $f_c$ | 5.0 to 20 V | 0 | — | 50 | kHz |
| Clock Pulse Width | 7 | $t_w$ | 5.0 to 20 V | 10 | — | — | μs |
| Set Pulse Width | 6 | $t_s$ | — | 10 | — | — | μs |
| Set Control Voltage — High State | 6 | — | — | $V_M$ | — | — | V |
| Low State | | | | — | — | 0.5 | |

## INPUT/OUTPUT FUNCTIONS

**Clock — (Pin 7)** This input is active on the positive edge of the clock pulse and accepts Logic '1' input levels dependant on the supply voltage and includes hysteresis for noise immunity.

**CW/CCW — (Pin 10)** This input determines the motor's rotational direction. When the input is held low, (OV, see the electrical characteristics) the motor's direction is nominally clockwise (CW). When the input is in the high state, Logic '1,' the motor direction will be nominally counter clockwise (CCW), depending on the motor connections.

**Full/Half Step — (Pin 8)** This input determines the angular rotation of the motor for each clock pulse. In the low state the motor will make a full step for each applied clock pulse, while in the high state, the motor will make half a step.

**$V_D$ — (Pin 2)** This pin is used to protect the outputs (1, 3, 14, 16) where large positive spikes occur due to switching the motor coils. The maximum allowable voltage on these pins is the clamp voltage ($V_{clamp}$). Motor performance is improved if a zener diode is connected between Pin 2 and Pin 15 as shown in Figure 1.

The following conditions have to be considered when selecting the zener diode:

$V_{clamp} = V_M + 6.0\text{ V}$

$V_Z = V_{clamp} - V_M - V_F{}^*$

where: $V_F$ = clamp diodes forward voltage drop (see Figure 4)

$V_{clamp}$:
$\leq 20$ V for SAA1042
$\leq 30$ V for SAA1042A

Pins 2 and 15 can be linked, in this case $V_Z = 0$ V.

**Set/Bias Input — (Pin 6)** This input has two functions:

The resistor $R_B$ adapts the drivers to the motor current.

A pulse via the resistor $R_B$ sets the outputs (1, 3, 14, 16) to a defined state.

The resistor $R_B$ can be determined from the graph of Figure 2 according to the motor current and voltage. Smaller values of $R_B$ will increase the power dissipation of the circuit and larger values of $R_B$ may increase the saturation voltage of the driver transistors.

When the "set" function is not used, terminal A of the resistor $R_B$ must be grounded. When the set function is used, terminal A has to be connected to an open-collector (buffer) circuit. Figure 7 shows this configuration. The buffer circuit (off-state) has to sustain the motor voltage $V_M$. When a pulse is applied via the buffer and the bias resistor $R_B$:

During the pulse duration, the motor driver transistors are turned off.

After elapsing the pulse, the outputs will have defined states.

Figure 6 shows the timing diagram.

Figure 7 illustrates a typical application in which the SAA1042 drives a 12 V stepper motor with a current consumption of 200 mA/coil.

A bias resistor ($R_B$) of 56 kΩ is chosen according to Figure 2.

The maximum voltage permitted at the output pin is $V_M + 6.0$ V (see the Maximum Ratings), in this application $V_M = 12$ V, therefore the maximum voltage is 18 V. The outputs are protected by the internal diodes and an external zener connected between Pins 2 and 15.

From Figure 4, it can be seen that the voltage drop across the internal diodes is about 1.7 V at 200 mA. This results in a zener voltage between Pins 2 and 15 of:

$$V_Z = 6.0\text{ V} - 1.7\text{ V} = 4.3\text{ V}.$$

To allow for production tolerances and a safety margin, a 3.9 V zener has been chosen for this example.

The clock is derived from the line frequency which is phase locked by the MC14046B and the MC14024.

The voltage on the clock input, is normally low (Logic '0'). The motor steps on the positive going transition of the clock pulse.

A Logic '0' applied to the Full/Half input, Pin 8, operates the motor in the Full Step mode. A Logic '1' at this input will result in the Half Step mode. The logic level state on the CW/CCW input, Pin 10, and the connection of the motor coils to the outputs determines the rotational direction of the motor.

These two inputs should be biased to a Logic '0' or '1' and not left floating. In the event of non-use, they should be tied to ground or the logic supply line, $V_{CC}$.

The output drivers can be set to a fixed operating point by use of the Set input and a bias resistor $R_B$. A positive pulse to this input turns the drivers off and sets the logic state of the outputs.

After the negative going transition of the Set pulse, and until the first positive going transition of the clock, the outputs will be:

$$L1 = L3 = \text{high and } L2 = L4 = \text{low}.$$

(See Figure 6, the timing diagram).

The Set input can be driven by a MC14007B or a transistor whose collector resistor is $R_B$. If the input is not used, the 'bottom' of $R_B$ must be grounded.

The total power dissipation of the circuit can be determined from Figures 3 and 5.

$$P_D = 0.9\text{ W} + 0.08\text{ W} = 0.98\text{ W}.$$

This results in a junction to ambient temperature, without a heatsink of:

$$T_J - T_A = 50°\text{C/W} \times 0.98\text{ W} = 49°\text{C}.$$

or a maximum ambient temperature of 76°C. For operation at elevated temperatures a heatsink is required.

FIGURE 2 — BIAS RESISTOR $R_B$ versus MOTOR CURRENT

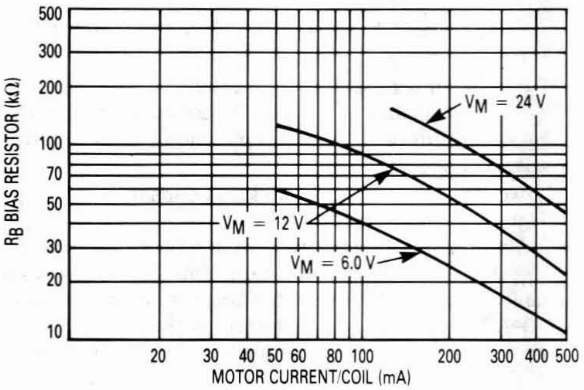


FIGURE 3 — DRIVE STAGE POWER DISSIPATION

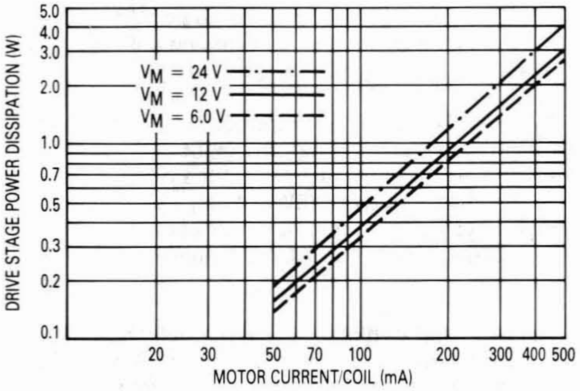


FIGURE 4 — CLAMP DIODE FORWARD CURRENT versus FORWARD VOLTAGE

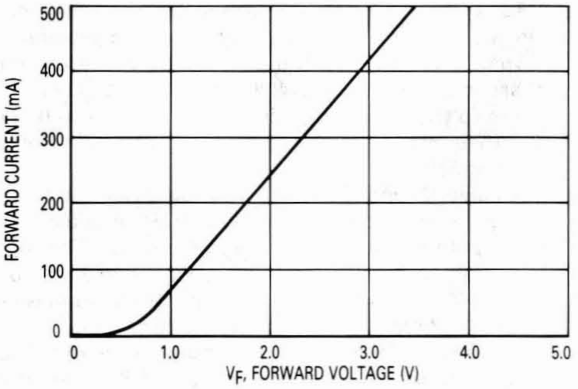


FIGURE 5 — POWER DISSIPATION versus LOGIC SUPPLY VOLTAGE

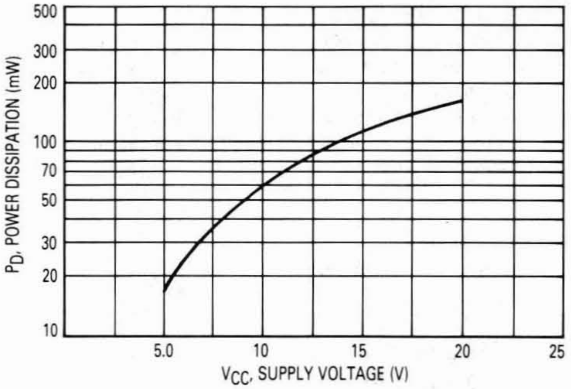


FIGURE 6 — TIMING DIAGRAM

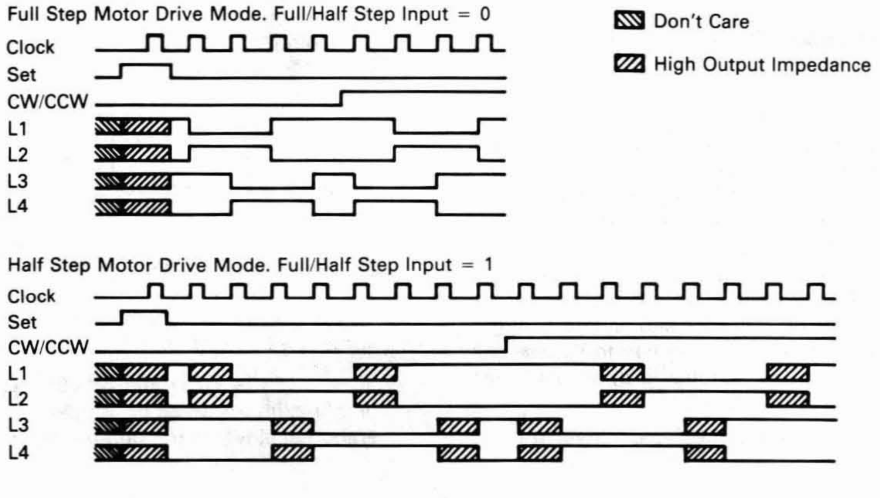
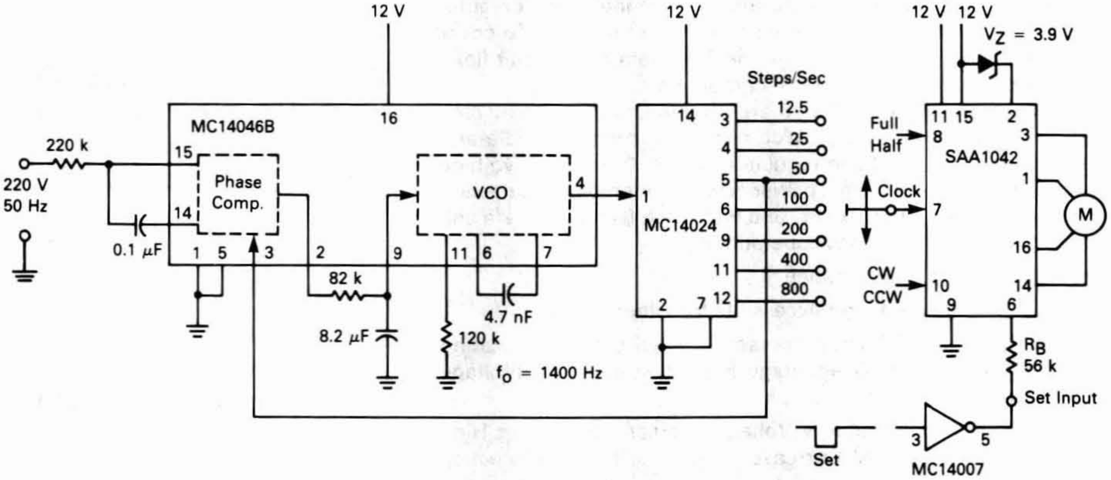

Full Step Motor Drive Mode. Full/Half Step Input = 0
Clock
Set
CW/CCW
L1
L2
L3
L4
Don't Care
High Output Impedance
Half Step Motor Drive Mode. Full/Half Step Input = 1
Clock
Set
CW/CCW
L1
L2
L3
L4

FIGURE 7 — TYPICAL APPLICATION
SELECTABLE STEP RATES WITH THE TIME BASE DERIVED FROM THE LINE FREQUENCY


12 V
12 V
12 V
12 V
$V_Z$ = 3.9 V
Steps/Sec
MC14046B
16
220 k
220 V
50 Hz
15
14
0.1 µF
Phase
Comp.
1
5
3
2
9
11
6
7
VCO
4
82 k
8.2 µF
120 k
4.7 nF
$f_o$ = 1400 Hz
14
MC14024
1
3
4
5
6
9
11
12
2
7
12.5
25
50
100
200
400
800
Full
Half
8
Clock
7
CW
CCW
10
11
15
2
SAA1042
3
1
16
14
9
6
M
$R_B$
56 k
Set Input
Set
3
5
MC14007

# TCA5600
# TCF5600

## Product Preview

### UNIVERSAL MICROPROCESSOR POWER SUPPLY/ CONTROLLER

The TCA5600 is a versatile power supply control circuit for microprocessor based systems and mainly intended for automotive applications and battery powered instruments. To cover a wide range of applications, the device offers high circuit flexibility with minimum of external components.

Functions included in this IC are a temperature compensated voltage reference, on chip dc/dc converter, programmable and remote controlled voltage regulator, fixed 5.0 V supply voltage regulator with external PNP power device, undervoltage detection circuit, power-on RESET delay and watchdog feature for safe and hazard free microprocessor operations.

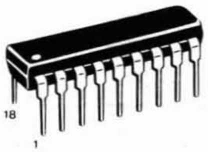
- 6.0 to 30 V Operation Range
- 2.5 V Reference Voltage Accessible for Other Tasks
- Fixed 5.0 V ± 4% Microprocessor Supply Regulator Including Current Limitation, Overvoltage Protection and Undervoltage Monitor
- Programmable 6.0 to 30 V Voltage Regulator Exhibiting High Peak Current (150 mA), Current Limiting and Thermal Protection
- Two Remote Inputs to Select the Regulator's Operation Mode: OFF, 5.0 V, 5.0 V Standby and Programmable Output Voltage
- Self Contained dc/dc Converter Fully Controlled By the Programmable Regulator to Guarantee Safe Operation Under All Working Conditions
- Programmable Power-On RESET Delay
- Watchdog Select Input
- Negative Edge Triggered Watchdog Input
- Low Current Consumption in the $V_{CC1}$ Standby Mode
- All Digital Control Ports are TTL- and MOS-Compatible

APPLICATIONS INCLUDE

- Microprocessor Systems with $E^2$PROMs
- High Voltage Crystal and Plasma Displays
- Decentralized Power Supplies in Computer and Telecommunication Systems

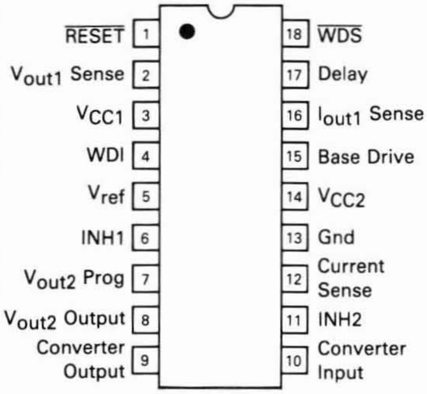
### UNIVERSAL MICROPROCESSOR POWER SUPPLY CONTROLLER

SILICON MONOLITHIC
INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 707-02

### PIN CONNECTIONS



(Top View)

### RECOMMENDED OPERATION CONDITIONS

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC1}$<br>$V_{CC2}$ | 5.0<br>5.5 | 30<br>30 | V |
| Collector Current | $I_C$ | — | 800 | mA |
| Output Voltage | $V_{out2}$ | 6.0 | 30 | V |
| Reference Source Current | $I_{ref}$ | 0 | 2.0 | mA |

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

### ORDERING INFORMATION

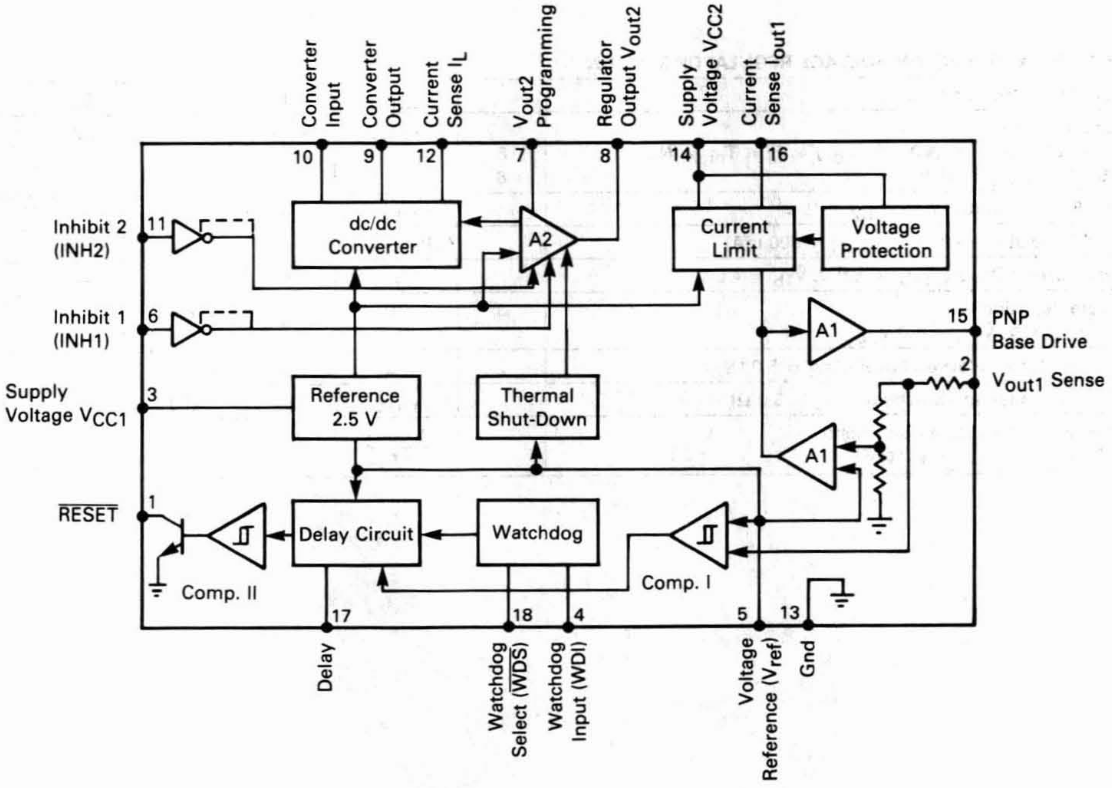
| Device | Operating Junction Temperature Range | Package |
|---|---|---|
| TCA5600 | 0 to +125°C | Plastic DIP |
| TCF5600 | −40 to +150°C | Plastic DIP |

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted, Note 1)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage (Pin 3, 14) | $V_{CC1}$, $V_{CC2}$ | 35 | Vdc |
| Base Drive Current (Pin 15) | $I_B$ | 20 | mA |
| Collector Current (Pin 10) | $I_C$ | 1.0 | A |
| Forward Rectifier Current (Pin 10–Pin 9) | $I_F$ | 1.0 | A |
| Logic Inputs INH1, INH2, $\overline{\text{WDS}}$ (Pin 6, 11, 18) | $V_{INP}$ | −0.3 V to $V_{CC1}$ | Vdc |
| Logic Input Current WDI (Pin 4) | $I_{WDI}$ | ±0.5 | mA |
| Output Sink Current $\overline{\text{RESET}}$ (Pin 1) | $I_{\overline{RES}}$ | 10 | mA |
| Analog Inputs (Pin 2)<br>(Pin 7) | —<br>— | −0.3 to 10<br>−0.3 to 5.0 | V |
| Reference Source Current (Pin 5) | $I_{ref}$ | 5.0 | mA |
| Power Dissipation (Note 2)<br>$T_A$ = +75°C TCA5600<br>$T_A$ = +85°C TCF5600 | $P_D$ | <br>500<br>650 | mW |
| Thermal Resistance (Junction to Air) | $R_{\theta JA}$ | 100 | °C/W |
| Operating Temperature Range<br>TCA5600<br>TCF5600 | $T_A$ | <br>0 to +75<br>−40 to +85 | °C |
| Operating Junction Temperature<br>TCA5600<br>TCF5600 | $T_J$ | <br>+125<br>+150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

NOTES:
1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for junction temperature above +75°C (TCA5600).
Derate at 10 mW/°C for junction temperature above +85°C (TCF5600).

**FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM**


Converter Input
Converter Output
Current Sense $I_L$
$V_{out2}$ Programming
Regulator Output $V_{out2}$
Supply Voltage $V_{CC2}$
Current Sense $I_{out1}$
10
9
12
7
8
14
16
dc/dc Converter
A2
Current Limit
Voltage Protection
Inhibit 2 (INH2)
11
Inhibit 1 (INH1)
6
A1
15
PNP Base Drive
2
$V_{out1}$ Sense
Supply Voltage $V_{CC1}$
3
Reference 2.5 V
Thermal Shut-Down
A1
$\overline{\text{RESET}}$
1
Delay Circuit
Watchdog
Comp. II
Comp. I
17
18
4
5
13
Delay
Watchdog Select ($\overline{\text{WDS}}$)
Watchdog Input (WDI)
Voltage Reference ($V_{ref}$)
Gnd

**ELECTRICAL CHARACTERISTICS** ($V_{CC1}$ = $V_{CC2}$ = 12 V; $T_J$ = 25°C; $I_{ref}$ = 0; $I_{out1}$ = 0 (Note 3); $R_{SC}$ = 0.5 Ω; INH1 = "High"; INH2 = "High"; $\overline{WDS}$ = "High"; $I_{out2}$ = 0 (Note 4); if not otherwise specified)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **REFERENCE SECTION** | | | | | | |
| Nominal Reference Voltage | 1 | $V_{ref\ nom}$ | 2.42 | 2.5 | 2.58 | V |
| Reference Voltage<br>$I_{ref}$ = 0.5 mA, $T_{low} \le T_J \le T_{high}$ (Note 5),<br>6.0 V ≤ $V_{CC1}$ ≤ 18 V | | $V_{ref}$ | 2.4 | — | 2.6 | V |
| Line Regulation (6.0 V ≤ $V_{CC2}$ ≤ 18 V) | | $Reg_{line}$ | — | 2.0 | 15 | mV |
| Average Temperature Coefficient<br>$T_{low} \le T_J \le T_{high}$ (Note 5) | 2 | $\frac{\Delta V_{ref}}{\Delta T_J}$ | — | — | +/−0.5 | mV/°C |
| Ripple Rejection Ratio<br>f = 1.0 kHz, $V_{sin}$ = 1.0 $V_{pp}$ | 3 | RR | 60 | 70 | — | dB |
| Output Impedance<br>0 ≤ $I_{ref}$ ≤ 2.0 mA | | $Z_O$ | — | 1.0 | — | Ohm |
| Standby Current Consumption<br>$V_{CC2}$ = Open | 4 | $I_{CC1}$ | — | 3.0 | — | mA |

NOTES:

3. The external PNP power transistor satisfies the following minimum specifications:
   $h_{FE} \ge 60$ at $I_C$ = 500 mA and $V_{CE}$ = 5.0 V; $V_{CE(sat)} \le 300$ mV at $I_B$ = 10 mA and $I_C$ = 300 mA
4. Regulator $V_{out2}$ programmed for nominal 24 V output by means of R4, R5 (see Figure 1)
5. $T_{low}$ = 0°C for TCA5600; $T_{low}$ = −40°C for TCF5600.
   $T_{high}$ = 125°C for TCA5600; $T_{high}$ = 150°C for TCF5600.

**5.0 V MICROPROCESSOR VOLTAGE REGULATOR SECTION**

| | | | | | | |
|---|---|---|---|---|---|---|
| Nominal Output Voltage | | $V_{out1(nom)}$ | 4.8 | 5.0 | 5.2 | V |
| Output Voltage<br>5.0 mA ≤ $I_{out1}$ ≤ 300 mA, $T_{low} \le T_J \le T_{high}$ (Note 5)<br>6.0 V ≤ $V_{CC2}$ ≤ 18 V | <br>5<br>6 | $V_{out1}$ | 4.75 | — | 5.25 | V |
| Line Regulation (6.0 V ≤ $V_{CC2}$ ≤ 18 V) | | $Reg_{line}$ | — | 10 | 50 | mV |
| Load Regulation (5.0 mA ≤ $I_{out1}$ ≤ 300 mA) | | $Reg_{load}$ | — | 20 | 100 | mV |
| Base Current Drive ($V_{CC2}$ = 6.0 V, $V_{15}$ = 4.0 V) | | $I_B$ | 10 | 15 | — | mA |
| Ripple Rejection Ratio<br>f = 1.0 kHz, $V_{sin}$ = 1.0 $V_{pp}$ | 3 | RR | 50 | 65 | — | dB |
| Undervoltage Detection Level ($R_{SC}$ = 5.0 Ω) | 7 | $V_{low}$ | 4.5 | 0.93 x $V_{out1}$ | — | V |
| Current Limitation Threshold ($R_{SC}$ = 5.0 Ω) | | $V_{RSC}$ | 210 | 250 | 290 | mV |
| Average Temperature Coefficient<br>$T_{low} \le T_J \le T_{high}$ (Note 5) | | $\frac{\Delta V_{out1}}{\Delta T_J}$ | — | — | ±1.0 | mV/°C |

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PROGRAMMABLE VOLTAGE REGULATOR SECTION** (Note 6) | | | | | | |
| Nominal Output Voltage | | $V_{out2(nom)}$ | 23 | 24 | 25 | V |
| Output Voltage<br>1.0 mA $\le I_{out2} \le$ 100 mA, $T_{low} \le T_J \le T_{high}$ (Notes 5, 7) | 8 | $V_{out2}$ | 22.8 | — | 25.2 | V |
| Load Regulation 1.0 mA $\le I_{out2} \le$ 100 mA (Note 7) | | $Reg_{load}$ | — | 40 | 200 | mV |
| DC Output Current | | $I_{out2}$ | 100 | — | — | mA |
| Peak Output Current (Internally Limited) | | $I_{out2\ p}$ | 150 | 200 | — | mA |
| Ripple Rejection Ratio<br>f = 20 kHz, V = 0.4 $V_{pp}$ | | RR | 45 | 55 | — | dB |
| Output Voltage (Fixed 5.0 V)<br>1.0 mA $\le I_{out2} \le$ 20 mA, $T_{low} \le T_J \le T_{high}$,<br>INH1 = "High" (Note 5) | | $V_{out2(5.0\ V)}$ | 4.75 | — | 5.25 | V |
| OFF State Output Impedance (INH2 = "Low") | | $R_{out1}$ | — | 10 | — | kΩ |
| Average Temperature Coefficient<br>$T_{low} \le T_J \le T_{high}$ (Note 5) | | $\frac{\Delta V_{out2}}{\Delta T_J V_{out2}}$ | — | — | ±0.25 | mV/°C V |

NOTES:

6. $V_g$ = 28 V, INH1 = "Low" for this Electrical Characteristic section unless otherwise specified.
7. Pulse tested $t_p \le 300\ \mu s$

**DC/DC CONVERTER SECTION**

| | | | | | | |
|---|---|---|---|---|---|---|
| Collector Current Detection Level "High"<br>$R_C$ = 10 k "Low" | 9 | $V_{12}(H)$<br>$V_{12}(L)$ | 350<br>— | 400<br>50 | 450<br>— | mV |
| Collector Saturation Voltage<br>$I_C$ = 600 mA (Note 7) | 10 | $V_{CE(sat)}$ | — | — | 1.6 | V |
| Rectifier Forward Voltage Drop<br>$I_F$ = 600 mA (Note 7) | 11 | $V_F$ | — | — | 1.4 | V |

**WATCHDOG AND $\overline{\text{RESET}}$ CIRCUIT SECTION**

| | | | | | | |
|---|---|---|---|---|---|---|
| Threshold Voltage "High"<br>(static) "Low" | | $V_{C5(H)}$<br>$V_{C5(L)}$ | —<br>— | 2.5<br>1.0 | —<br>— | V |
| Current Source $T_{low} \le T_J \le T_{high}$ (Note 5)<br>Power-Up $\overline{\text{RESET}}$<br>Watchdog Time Out<br>Watchdog $\overline{\text{RESET}}$ | | $I_{C5}$ | <br>−1.8<br>—<br>— | <br>−2.5<br>$5xI_{C5}$<br>$-50xI_{C5}$ | <br>−3.2<br>—<br>— | µA |
| Watchdog Input Voltage Swing | | $V_{WDI}$ | — | — | ±5.5 | V |
| Watchdog Input Impedance | | $r_i$ | 12 | 15 | — | kΩ |
| Watchdog Reset Pulse Width (C8 = 1.0 nF) (Note 9) | | $t_p$ | — | — | 10 | µs |

**DIGITAL PORTS: $\overline{\text{WDS}}$, INH 1, INH 2, $\overline{\text{RESET}}$** (Note 8)

| | | | | | | |
|---|---|---|---|---|---|---|
| Input Voltage Range | | $V_{INP}$ | — | — | −0.3 to $V_{CC1}$ | V |
| Input HIGH Current<br>2.0 V $\le V_{IH} \le$ 5.5 V<br>5.5 V $\le V_{IH} \le V_{CC1}$ | | $I_{IH}$ | <br>—<br>— | <br>—<br>— | <br>100<br>150 | µA |
| Input LOW Current<br>−0.3 V $\le V_{IL} \le$ 0.8 V for INH1, INH2,<br>−0.3 V $\le V_{IL} \le$ 0.4 V for $\overline{\text{WDS}}$ | | $I_{IL}$ | — | — | −100 | µA |
| Leakage Current Immunity (INH2, High "Z" State) | 12 | $I_Z$ | ±20 | — | — | µA |
| Output LOW Voltage $\overline{\text{RESET}}$ ($I_{OL}$ = 6.0 mA) | | $V_{OL}$ | — | — | 0.4 | V |
| Output HIGH Current $\overline{\text{RESET}}$ ($V_{OH}$ = 5.5 V) | | $V_{OH}$ | — | — | 20 | µA |

NOTES:

8. Temperature range $T_{low} \le T_J \le T_{high}$ applies to this Electrical Characteristics section.
9. For test purposes, a negative pulse is applied to Pin 4 ($-2.5\ V \ge V_4 \ge -5.5\ V$).

## TYPICAL CHARACTERISTICS

FIGURE 1 — REFERENCE VOLTAGE versus SUPPLY VOLTAGE

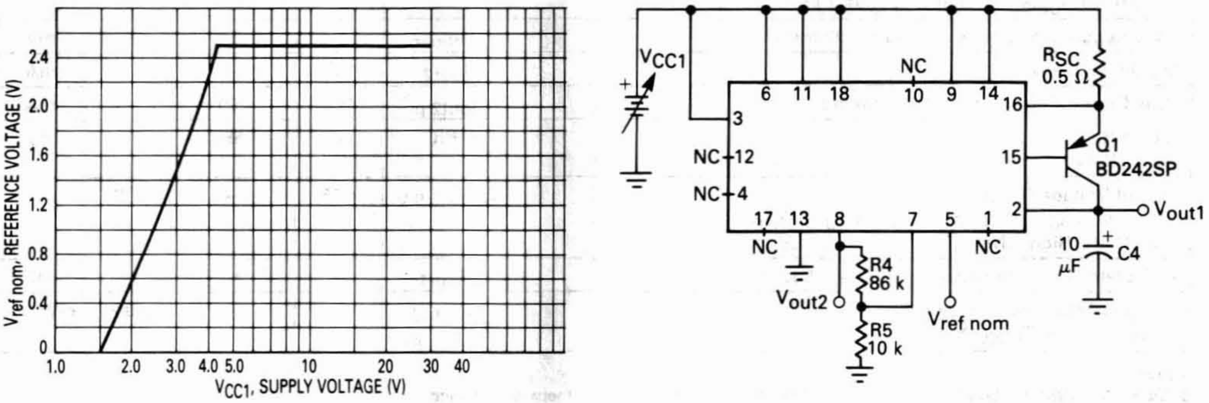


FIGURE 2 — REFERENCE STABILITY versus TEMPERATURE

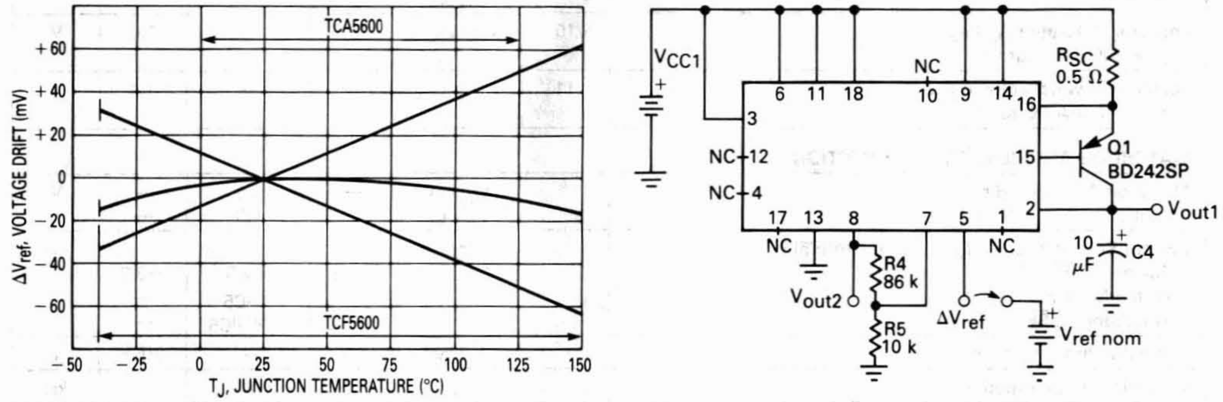


FIGURE 3 — RIPPLE REJECTION versus FREQUENCY

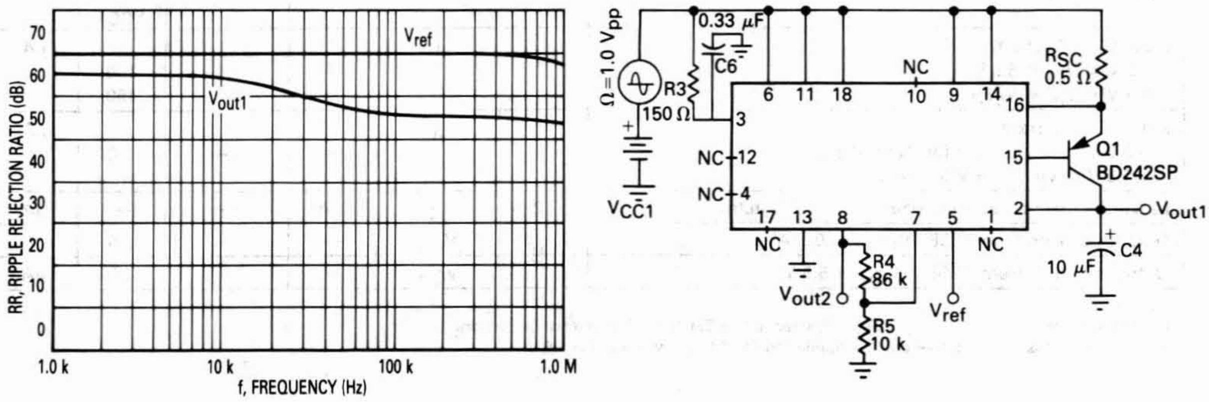


FIGURE 4 — STAND-BY CURRENT versus SUPPLY VOLTAGE

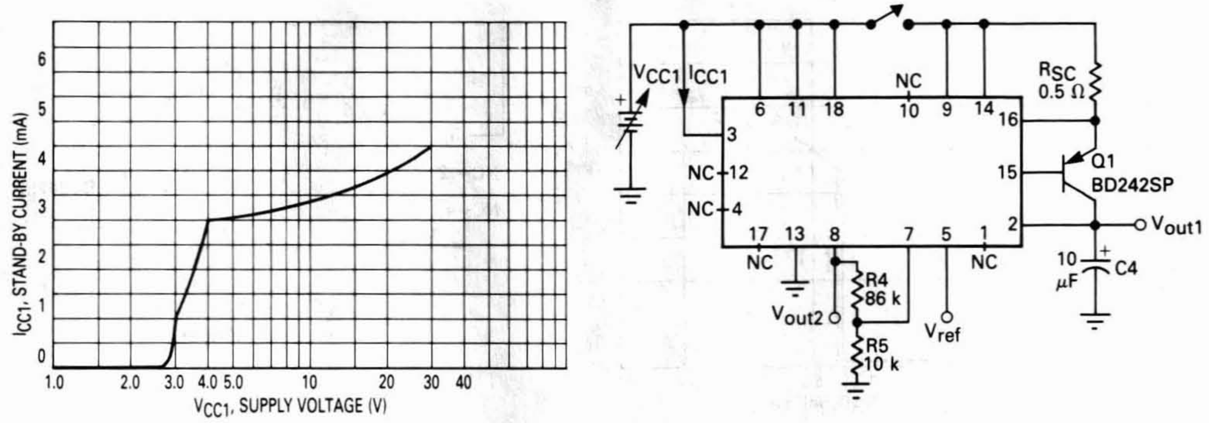


FIGURE 5 — POWER-UP BEHAVIOR OF THE 5.0 V REGULATOR

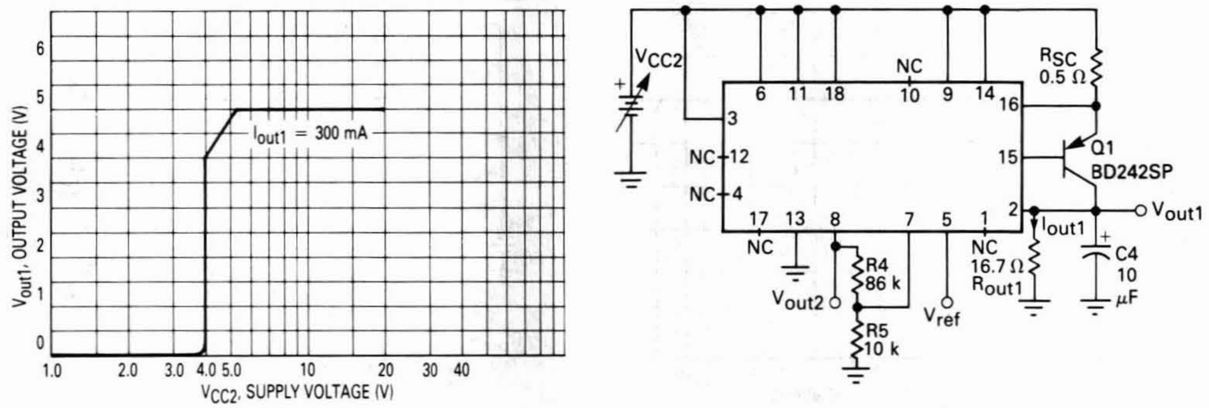


FIGURE 6 — FOLDBACK CHARACTERISTICS OF THE 5.0 V REGULATOR

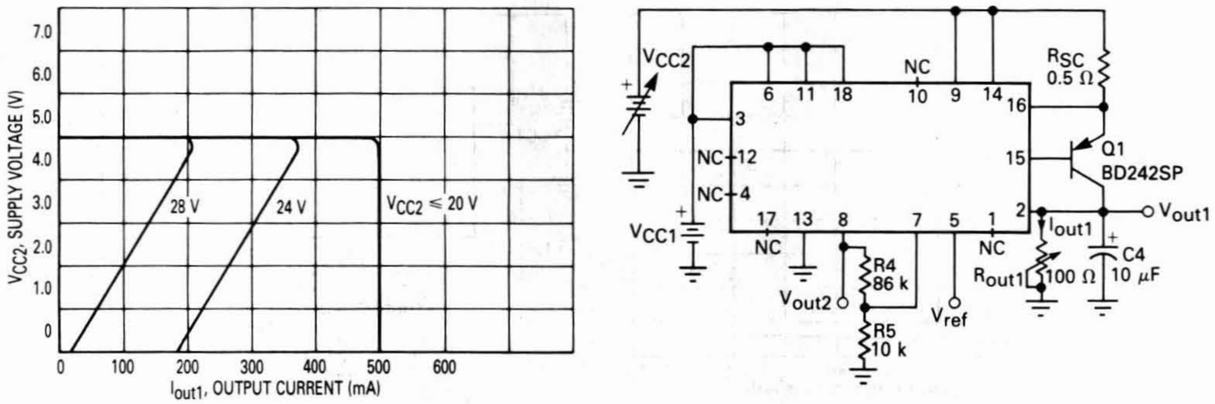


FIGURE 7 — UNDERVOLTAGE LOCKOUT CHARACTERISTICS

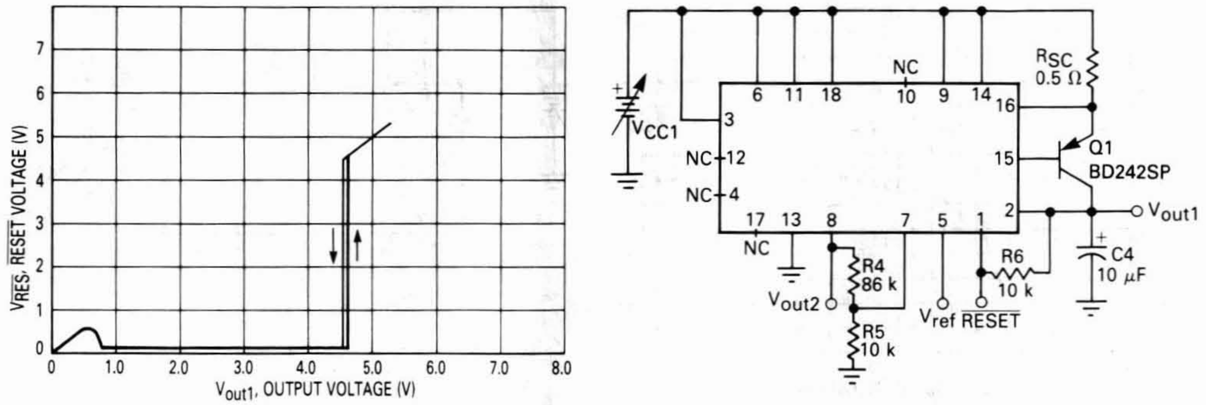


FIGURE 8 — OUTPUT CURRENT CAPABILITY OF THE PROGRAMMING REGULATOR

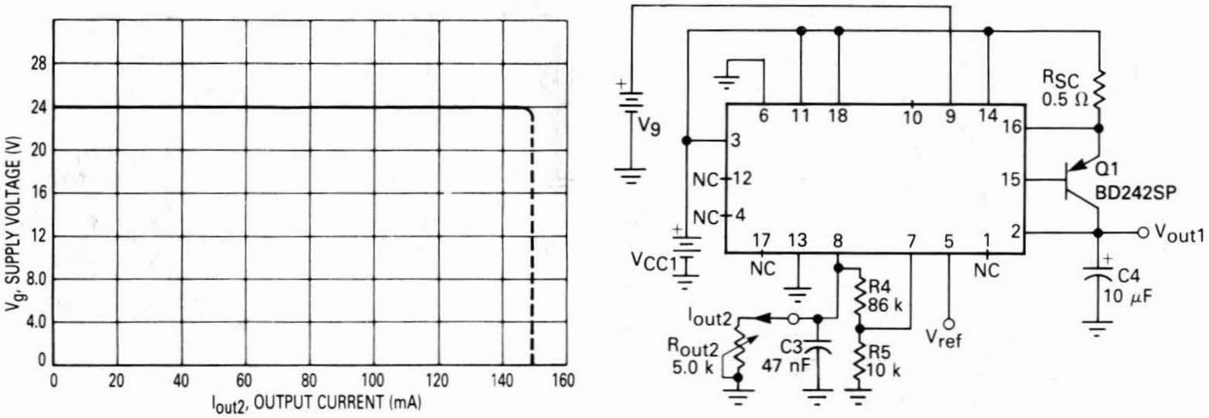


FIGURE 9 — COLLECTOR CURRENT DETECTION LEVEL

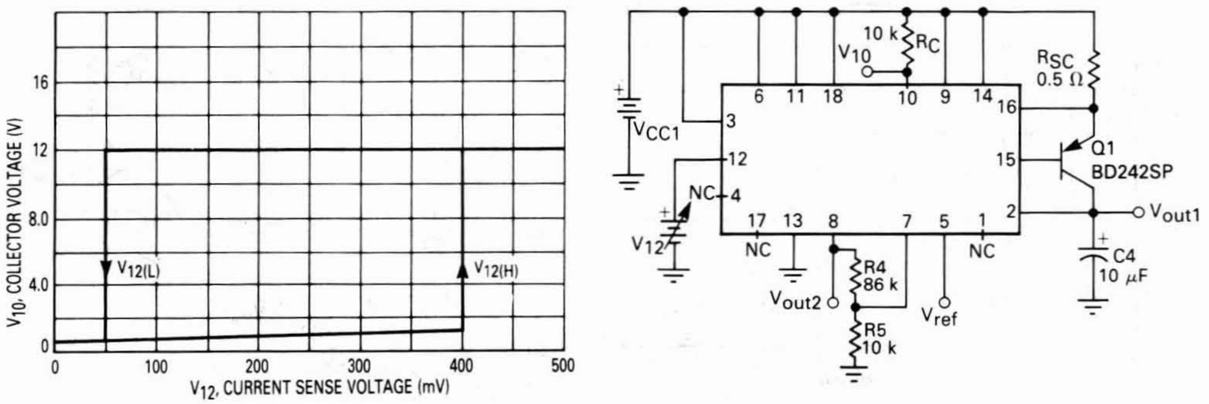


FIGURE 10 — POWER SWITCH CHARACTERISTICS

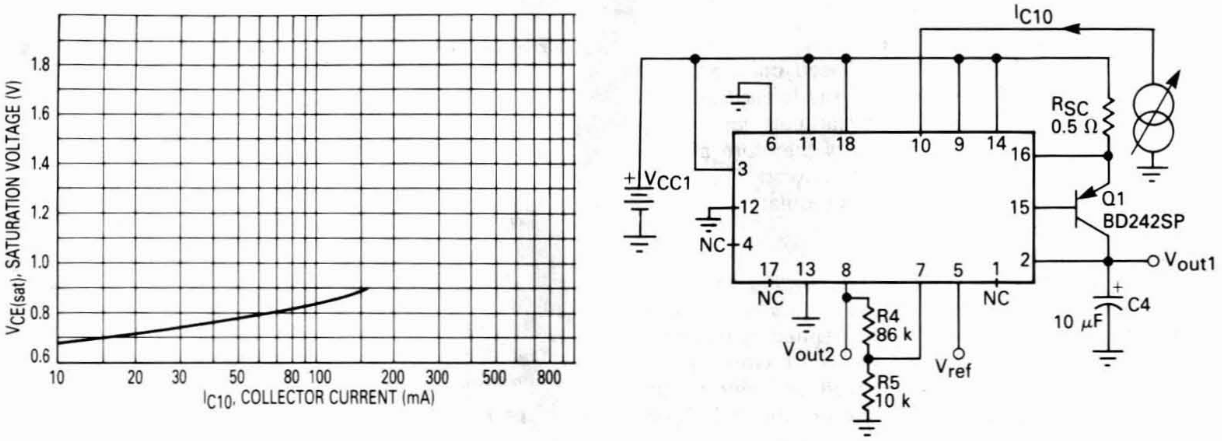


FIGURE 11 — RECTIFIER CHARACTERISTICS

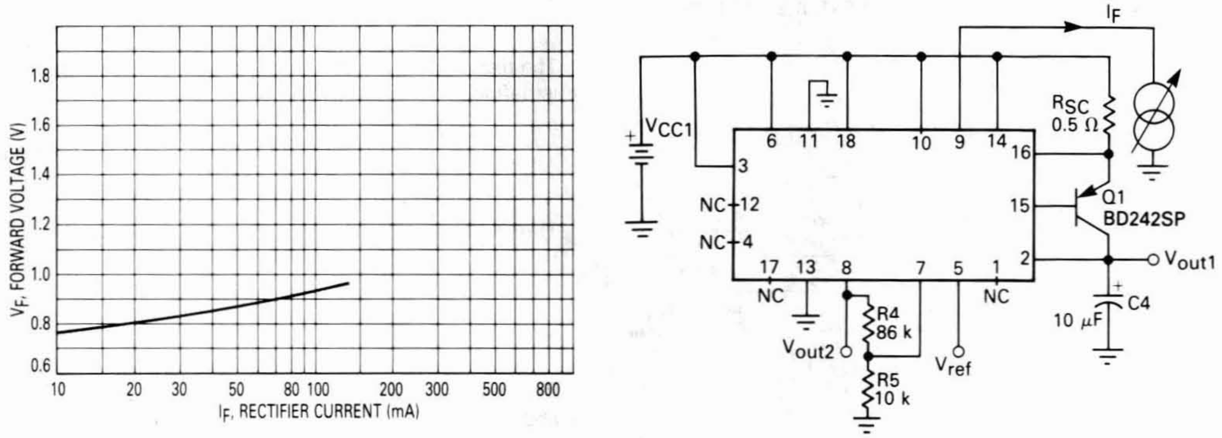
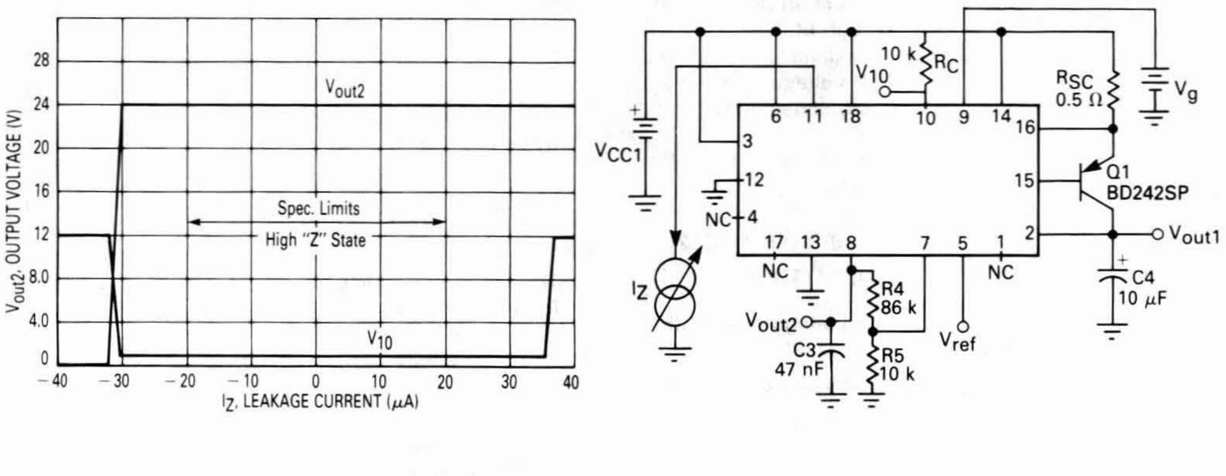


FIGURE 12 — INH 2 LEAKAGE CURRENT IMMUNITY



## APPLICATIONS INFORMATION
(See Figure 18)

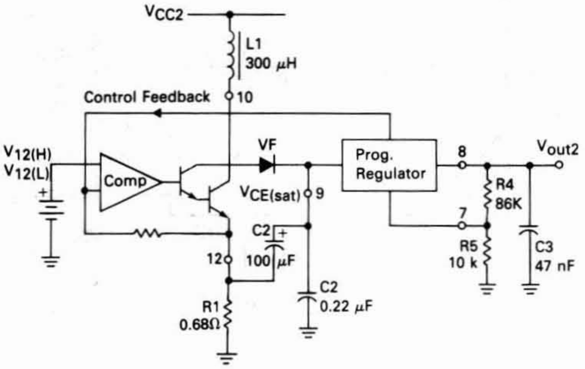
### 1. VOLTAGE REFERENCE $V_{ref}$

The voltage reference $V_{ref}$ is based upon a highly stable bandgap voltage reference and is accessible on Pin 5 for additional tasks. This circuit part has its own supply connection on Pin 3 and is therefore able to operate in standby mode. The RC network R3, C6 improves the ripple rejection on both regulators.

### 2. DC/DC CONVERTER

The dc/dc converter performs according to the fly back principle and does not need a time base circuit. The maximum coil current is well defined by means of the current sensing resistor R1 under all working conditions (start-up phase, circuit overload, wide supply voltage range and extreme load current change). Figure 13 shows the simplified converter schematic:

FIGURE 13 — SIMPLIFIED CONVERTER SCHEMATIC



A simplified method on "how to calculate the coil inductance" is given below. The operation point at min. supply voltage ($V_{CC2}$) and max. output current ($I_{out2}$) for a fixed output voltage ($V_{out2}$) determines the coil data. Figure 14 shows the typical voltage and current wave forms on the coil L1 (coil losses neglected).

The equations (1) and (2) yield the respective coil voltage $V_L-$ and $V_L+$ (see Figure 14):

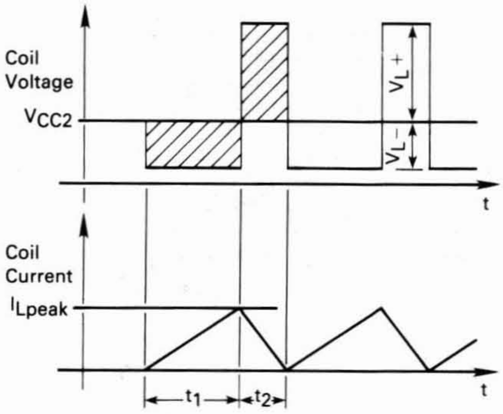
$$V_L+ = V_{out2} + \Delta V_{(Pin\ 9\ -\ Pin\ 8)} + V_F - V_{CC2} \quad (1)$$

$$V_L- = V_{CC2} - V_{CE(sat)} - V_{12(H)} \quad (2)$$

($\Delta V_{(Pin\ 9\ -\ Pin\ 8)}$: input/output voltage drop of the regulator, 2.5 V typical)

($V_F$, $V_{CE(sat)}$, $V_{12(H)}$: see electrical characteristics)

FIGURE 14 — VOLTAGE AND CURRENT WAVEFORM ON THE COIL (not to scale)



The time ratio α for the charging time to dumping time is defined by equation (3):

$$\alpha = \frac{t_1}{t_2} = \frac{V_L+}{V_L-} \quad (3)$$

The coil charging time $t_1$ is found using equation (4):

$$t_1 = \frac{1}{(1 + \frac{1}{\alpha}) \cdot f} \quad (4)$$

(f : min. oscillation frequency which should be chosen above the audio frequency band (e.g. 20 kHz))

Knowing the dc output current $I_{out2}$ of the programmable regulator, the peak coil current $I_{L(peak)}$ can now be calculated:

$$I_{L(peak)} = 2 \cdot I_{out2} \cdot (1 + \alpha) \quad (5)$$

The coil inductance L1 of the nonsaturated coil is given by equation (6):

$$L1 = \frac{t_1}{I_{L(peak)}} \cdot V_L- \quad (6)$$

The formula (6a) yields the current sensing resister R1 for a defined peak coil current $I_{L(peak)}$:

$$R1 = \frac{V_{12(H)}}{I_{L(peak)}} \quad (6a)$$

In order to limit the by-pass current through capacitor C7 during the energy dumping phase the value C2>>C7 should be implemented.

For all other operation conditions, the feedback signal from the programmable voltage regulator controls the activity of the converter.

### 3. PROGRAMMABLE VOLTAGE REGULATOR

This series voltage regulator is programmable by the voltage divider R4, R5 for a nominal output voltage $6.0\ V \leq V_{out2} \leq 30\ V$.

$$R4 = \frac{(V_{out2} - V_{ref\ nom}) \cdot R5}{V_{ref\ nom}} \qquad (7)$$

$$(R5 = 10\ k,\ V_{ref\ nom} = 2.5\ V)$$

Current limitation and thermal shutdown capability are standard features of this regulator. The voltage drop $\Delta V_{(Pin\ 9\ -\ Pin\ 8)}$ across the series pass transistor generates the feedback signal to control the dc/dc converter (see Figure 13).

### 4. CONTROL INPUTS INH1, INH2

The dc/dc converter and/or the regulator $V_{out2}$ are remote controllable through the TTL, MOS compatible inhibit inputs INH1 and INH2 where the latter is a 3-level detector (Logic "0", high impedance "Z", Logic "1"). Both inputs are setup to provide the following truth table:

**FIGURE 15 — INH1, INH2 TRUTH TABLE**

| Mode | INH1 | INH2 | $V_{out2}$ | dc/dc |
|---|---|---|---|---|
| 1 | 0 | 0 | OFF | INT |
| 2 | 0 | High "Z" | $V_{out2}$ | ON |
| 3 | 0 | 1 | $V_{out2}$ | INT |
| 4 | 1 | 0 | OFF | INT |
| 5 | 1 | High "Z" | 5.0 V | ON |
| 6 | 1 | 1 | 5.0 V | INT |

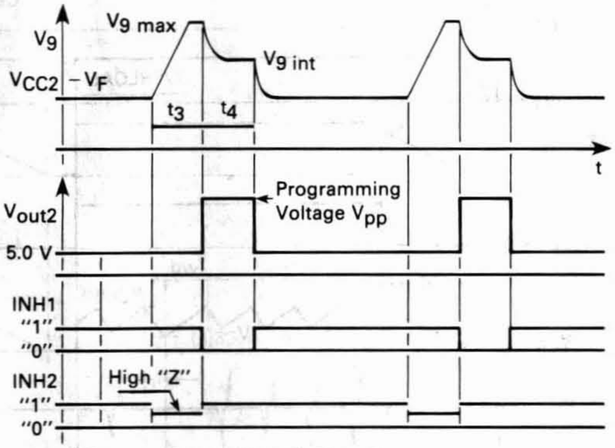
| | |
|---|---|
| INT: | Intermittent operation of the converter means that the converter operates only if $V_{CC2}<V_{out2}$. |
| ON: | The converter loads the storage capacitor C2 to its full charge ($V_9$ = 33 V), allowing fast response time of the regulator $V_{out2}$ when addressed by the control software. |
| OFF: | High impedance (internal resistor 10 k to ground) |

Figure 16 represents a typical timing diagram for an E²PROM programming sequence in a microprocessor based system. The high "Z" state enables the dc/dc converter to ramp during $t_3$ to the voltage $V_9$ at Pin 9 to a high level before the write cycle takes place in the memory.

### 5. MICROPROCESSOR SUPLY REGULATOR

Together with an external PNP power transistor (Q1), a 5.0 V supply exhibiting low voltage drop is obtained to power microprocessor systems and auxilliary circuits. Using a power Darlington with adequate heat sink in the output stage boosts the output current $I_{out1}$ above 1 amp.

**FIGURE 16 — TYPICAL E²PROM PROGRAMMING SEQUENCE (not to scale)**



The current limitation circuit measures the emitter current of Q1 by means of the sensing resistor $R_{SC}$.

$$R_{SC} = \frac{V_{RSC}}{I_E} \qquad (8)$$

($I_E$: emitter current of Q1)

($V_{RSC}$: threshold voltage (see electrical characteristics))

The voltage protection circuit performs a fold-back characteristic above a nominal operating voltage $V_{CC2} \geq 18\ V$.

### 6. DELAY AND WATCHDOG CIRCUIT

The under voltage monitor supervises the power supply $V_{out1}$ and releases the delay circuit $\overline{RESET}$ as soon as the regulator output reaches the microprocessor operating range (e.g. $V_{LOW} \geq 0.93 \cdot V_{out1(nom)}$). The $\overline{RESET}$ output has an open-collector and may be connected in a "wired-OR" configuration.

The watchdog circuit consists of a retriggerable monostable with a negative edge sensitive control input WDI. The watchdog feature may be disabled by means of the watchdog select input $\overline{WDS}$ driven to a "1". Figure 17 displays the typical $\overline{RESET}$ timing diagram.

The commuted current source $I_{C5}$ on Pin 17, threshold voltage $V_{C5(L)}$, $V_{C5(H)}$ and an external capacitor C5 define the $\overline{RESET}$ delay and the watchdog timing. The relationship of the timing signals are indicated by the equations (9) to (11).

$\overline{RESET}$ delay:
$$t_d = \frac{C5 \cdot V_{C5(H)}}{|I_{C5}|} \qquad (9)$$

Watchdog time-out:
$$t_{wd} = \frac{C5 \cdot (V_{C5(H)} - V_{C5(L)})}{5 \cdot I_{C5}} \qquad (10)$$

Watchdog $\overline{RESET}$:
$$t_r = \frac{C5 \cdot (V_{C5(H)} - V_{C5(L)})}{50 \cdot |I_{C5}|} \qquad (11)$$

($I_{C5}$, $V_{C5(H)}$, $V_{C5(L)}$: see electrical characteristics.)

FIGURE 17 — TYPICAL $\overline{\text{RESET}}$ TIMING DIAGRAM
(not to scale)

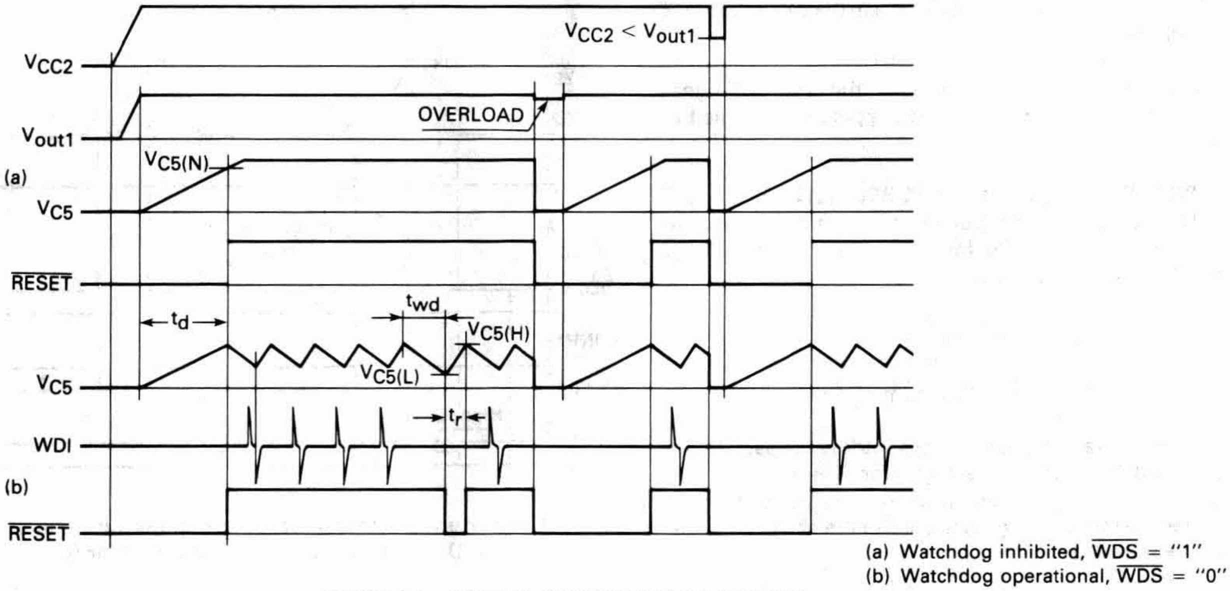
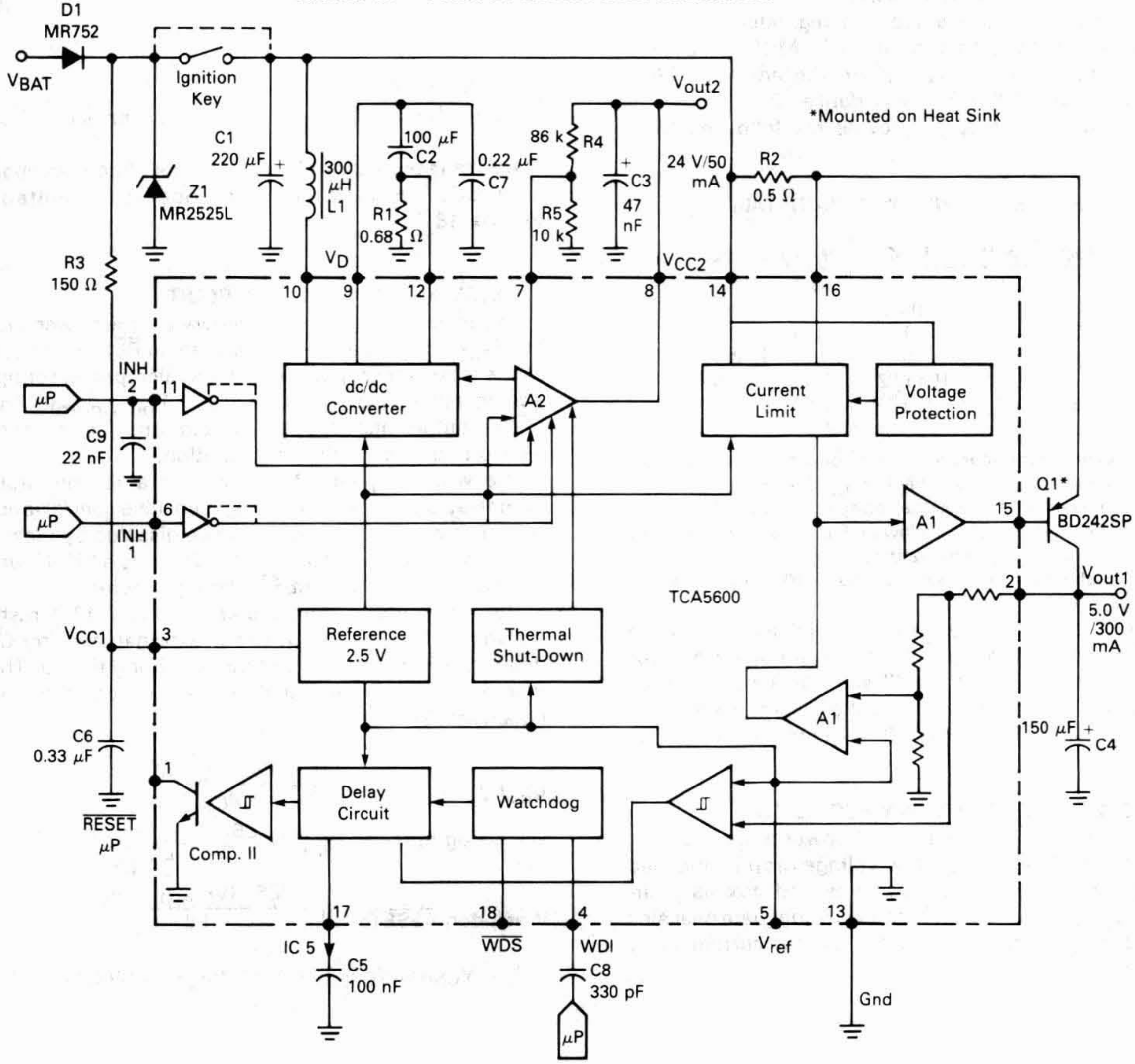


FIGURE 18 — TYPICAL AUTOMOTIVE APPLICATION



D1
MR752
$V_{BAT}$
Ignition Key
$V_{out2}$
*Mounted on Heat Sink
C1
220 μF
300 μH
L1
100 μF
C2
0.22 μF
C7
86 k
R4
24 V/50 mA
R2
0.5 Ω
Z1
MR2525L
R1
0.68 Ω
R5
10 k
C3
47 nF
R3
150 Ω
$V_D$
$V_{CC2}$
10
9
12
7
8
14
16
INH 2
11
μP
dc/dc Converter
A2
Current Limit
Voltage Protection
C9
22 nF
μP
6
INH 1
Q1*
15
A1
BD242SP
$V_{out1}$
2
5.0 V /300 mA
TCA5600
$V_{CC1}$
3
Reference 2.5 V
Thermal Shut-Down
C6
0.33 μF
A1
150 μF
C4
1
$\overline{\text{RESET}}$
μP
Comp. II
Delay Circuit
Watchdog
17
18
4
5
13
IC 5
C5
100 nF
$\overline{\text{WDS}}$
WDI
C8
330 pF
$V_{ref}$
Gnd
μP

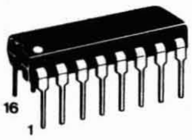
**MOTOROLA**

# TDA1085A

## Specification and Applications Information

## UNIVERSAL MOTOR SPEED CONTROLLER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



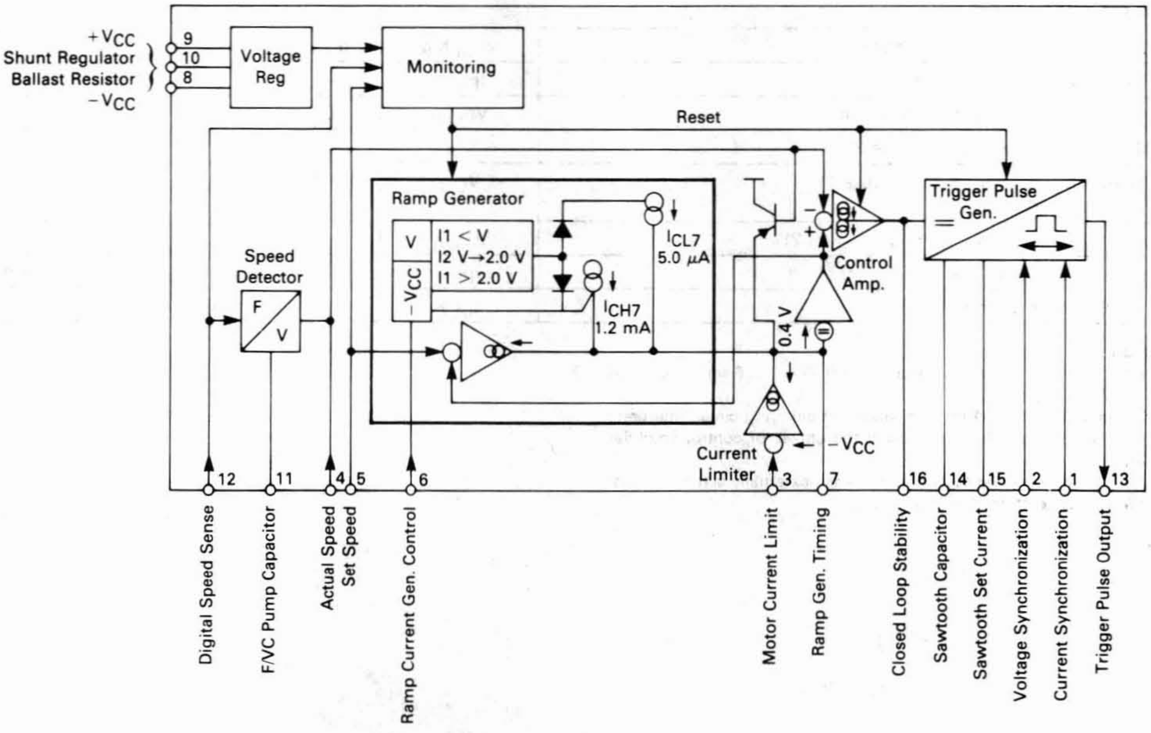
**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### UNIVERSAL MOTOR SPEED CONTROLLER

The TDA1085A has all the necessary functions for the speed control of universal (ac/dc) motors in an open or closed loop configuration. Additionally it has the facility for defining the initial speed/time characteristic. The circuit provides a phase angle varied trigger pulse to the motor control triac.

- Guaranteed Full Wave Triac Drive
- Soft Start from Powerup
- On-Chip Frequency/Voltage Convertor and Ramp Generator
- Current Limiting Incorporated
- Direct Drive from ac Line

**FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT**


+VCC
Shunt Regulator
Ballast Resistor
−VCC
9
10
8
Voltage Reg
Monitoring
Reset
Ramp Generator
V
−VCC
I1 < V
I2 V→2.0 V
I1 > 2.0 V
ICL7
5.0 μA
ICH7
1.2 mA
Speed Detector
F
V
Trigger Pulse Gen.
Control Amp.
0.4 V
−VCC
Current Limiter
12
11
4
5
6
3
7
16
14
15
2
1
13
Digital Speed Sense
F/VC Pump Capacitor
Actual Speed
Set Speed
Ramp Current Gen. Control
Motor Current Limit
Ramp Gen. Timing
Closed Loop Stability
Sawtooth Capacitor
Sawtooth Set Current
Voltage Synchronization
Current Synchronization
Trigger Pulse Output

## MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{Pin\ 9\text{-}8}$ | 17 | V |
| Power Supply Current (Pin 10 Open) | $I_{Pin\ 9}$ | 15 | mA |
| Peak Power Supply Regulation Current | $I_{Pin\ 9} + I_{Pin\ 10}$ | 35 | mA |
| Peak ac Synchronization Input Current | $I_{Pin\ 1}$<br>$I_{Pin\ 2}$ | ±1.0 | mA |
| Peak Output Triggering Current (Pulse Width 300 μs; Duty Cycle ≤ 3%) | $I_{Pin\ 13}$ | 200 | mA |
| Current Drain per Listed Pin | $I_{15}$<br>$I_3$<br>$I_{12}$ | 1.0<br>−5.0<br>−3.0, +0.1 | mA |
| Power Dissipation ($T_A$ = 25°C)<br>Derate above 25°C | $P_D$<br>$1/R_{\theta JA}$ | 625<br>6.8 | mW<br>mW/°C |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +125 | °C |

## ELECTRICAL CHARACTERISTICS ($T_A$ = +25°C unless otherwise stated)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **VOLTAGE REGULATOR** | | | | | |
| Regulated Voltage* ($I_9 + I_{10}$ = 10 mA) | $V_{CC}$ | — | 15.5 | — | V |
| Monitoring Enable Level* | $V_{ME}$ | — | 15.1 | — | V |
| Monitoring Disable Level* | $V_{MD}$ | — | 14.5 | — | V |
| Internal Current Consumption[1] | $I_{Pin\ 9}$ | — | 4.2 | — | mA |
| **RAMP GENERATOR** | | | | | |
| Reference Input Voltage Range[2] | $V_{Pin\ 5\text{-}8}$ | 0.08 | — | 13.5 | V |
| Reference Input Bias Current | $I_{Pin\ 5}$ | — | — | −20 | μA |
| Distribute Low Level Voltage Range | $V_{Pin\ 6}$ | 0 | — | 2.0 | V |
| Distribute — Low Level (Figure 2) | $V_{DL}$ | — | $V_{Pin\ 6}$ | — | V |
| Distribute — Upper Level* (Figure 2) ($V_{Pin\ 6}$ = 950 mV) | $V_{DU}$ | 1.9 $V_6$ | 2.0 $V_6$ | 2.1 $V_6$ | V |
| Low–High Acceleration Range (Figure 2) | $\Delta V_{DA}$ | — | 400 | — | mV |
| High Acceleration Charging Current | $I_{CH7}$ | — | 1.2 | — | mA |
| Low Charging Current[3] | $I_{CL7}$ | — | 5.0 | — | μA |

**NOTES:**

1. Pins 1, 2, 11, 12, 14 and 15 not connected; Pins 4, 5, 6 and 7 grounded to Pin 8: $V_{CC}$ = 15.5 V
2. When $V_{Pin\ 5}$ is ≤ 80 mV, the internal monitoring circuit interprets it as a true zero, thus minimizing the effects of control amplifier offsets.
3. This value should be accounted for when externally setting the distribute acceleration charging current.

**ELECTRICAL CHARACTERISTICS** (Continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CURRENT LIMITER** | | | | | |
| Stage Current Gain | $\frac{I_{DL7}}{\Delta I_3}$ | — | 170 | — | — |
| Output Discharge Current Swing | $I_{DL7}$ | — | 35 | — | mA |
| **CONTROL AMPLIFIER** | | | | | |
| Actual Speed Voltage Range | $V_{Pin\ 4\text{-}8}$ | 0 | — | 13.5 | V |
| Actual Speed Input Bias Current | $I_{Pin\ 4}$ | — | — | −350 | nA |
| Total Input Offset Voltage[4] | $V_{off}$ | −60 | — | 20 | mV |
| Transconductance $\left(\frac{\Delta I_{Pin\ 16}}{V_{Pin\ 4} - V_{Pin\ 7}}\right)$ | $g_m$ | — | 300 | — | μA/V |
| Output Current Swing | $I_{Pin\ 16}$ | — | ±100 | — | μA |
| **FREQUENCY/VOLTAGE CONVERTER** | | | | | |
| Input Signal Low Voltage[5] | $V_{L12}$ | −0.1 | — | — | V |
| Input Signal High Voltage | $V_{H12}$ | 0.1 | — | 5.0 | V |
| Polarization Current | $I_{Pin\ 12}$ | — | −25 | — | μA |
| Conversion Rate[6]* | $K_C$ | — | 15 | — | mV/Hz |
| Linearity* (Figure 3) | $K_L$ | — | ±4.0 | — | % |
| **TRIGGER PULSE GENERATOR** | | | | | |
| Voltage Synchronization Levels | $I_{Pin\ 2}$ | — | ±50 | — | μA |
| Current Synchronization Levels | $I_{Pin\ 1}$ | — | ±50 | — | μA |
| Input Voltage Swing (for full angle swing) | V | — | 11.7 | — | V |
| Trigger Pulse Width[7] | $t_p$ | — | 55 | — | μs |
| Trigger Pulse Repetition Period | t | — | 215 | — | μs |
| Trigger Pulse High Level ($I_{Pin\ 13}$ = 150 mA) | $V_{Pin\ 13}$ | $V_{CC} - 4$ | — | — | V |
| Output Leakage Current ($V_{Pin\ 13}$ = 0 V) | $I_{oPin\ 13}$ | — | — | 30 | μA |

[4] $V_{off}$ is defined as being the voltage difference between Pin 5 and 4 with no current flow on Pin 16.

[5] The negative swing is clamped to −0.3 V.

[6] $V_{Pin\ 4} = k \cdot C_{Pin\ 11} \cdot (V_{CC} - V_a) \cdot R_{Pin\ 4} \cdot \left(1 + \frac{180 \times 10^3}{R_{Pin\ 11}}\right)^{-1} \cdot \text{freq in.}$
Where: $9 < K < 13$ & $V_a = 1.3$ V.

[7] The timing given is when $C_{Pin\ 14}$ = 47 nF.

* These figures apply for the application shown in Figure 4.

## INPUT/OUTPUT FUNCTIONS

**VOLTAGE REGULATOR** — (Pins 8, 9, 10). This is a parallel type voltage regulator able to sink a large amount of current while offering good regulation characteristics.

A resistor between Pins 9 and 10 reduces the internal power dissipation. Under minimal current sink conditions (min. current from the unregulated supply, max. consumption by the circuitry), at least 1.0 mA should flow through this resistor. Under max. sink conditions (max. current from the unregulated supply, min. consumption by the circuitry), the maximum resistor value is chosen so that the voltage at Pin 10 falls towards 3.0 V, but not lower. The above, fixed dynamic range of the regulator must not be exceeded within one line cycle.

A power supply failure causes shutdown.

For operation from an externally regulated voltage, Pin 10 is not connected.

**SPEED SENSING** — (Pins 4, 11, 12). Speed sensing can be achieved either digitally (tachogenerator frequency) or analogically (tachogenerator amplitude).

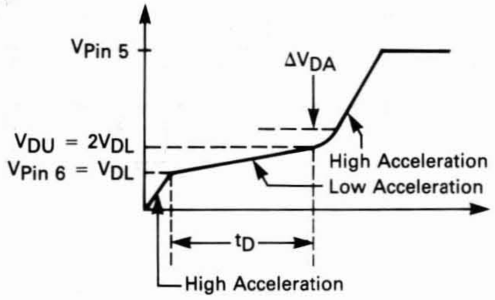
For digital sensing, a bipolar signal with respect to ground is applied to Pin 12. During positive excursions $C_{Pin\ 11}$ is charged. An internal mirror delivers ten times the charge on $C_{Pin\ 11}$ via Pin 4. However, due to internal circuitry, the charge on Pin 4 can vary in the region of 9 to 13 times the charge on $C_{Pin\ 11}$. For that reason it is necessary to calibrate the Frequency/Voltage Convertor (F/VC) with a variable resistor on Pin 4. Thus the relationship between speed and $V_{Pin\ 4}$ is defined by $R_{Pin\ 4}$ and $C_{Pin\ 11}$.

To maintain linearity in the high speed ranges it is important that $C_{Pin\ 11}$ is fully charged across an equivalent resistor of about 180 kΩ. It should be borne in mind that the impedance on Pin 11 should be kept as low as possible as $C_{Pin\ 11}$ has a large influence on the temperature coefficient of the FV/C. The time constant on Pin 4 should also be kept as low as possible.

Pin 12 is also an impedance monitoring input; at high impedances $V_{Pin\ 12}$ increases. Should $V_{Pin\ 12}$ exceed 5.0 V the triac trigger pulses are inhibited and the circuit resets.

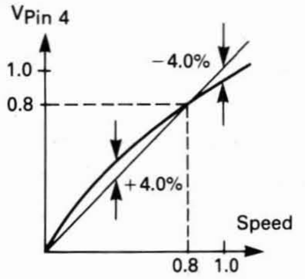
A 470 kΩ resistor from Pin 11 to $+V_{CC}$ significantly reduces the leakage current and reduces the device temperature coefficient to almost zero.

FIGURE 2 — RAMP GENERATOR TRANSFER CHARACTERISTIC



The shape of the curve is determined by $CR_{Pin\ 7}$; where $C_{Pin\ 7}$ defines the high acceleration slope and $R_{Pin\ 7}$ defines that of the low acceleration.

FIGURE 3 — FREQUENCY/VOLTAGE CONVERTER OUTPUT CHARACTERISTIC



## INPUT/OUTPUT FUNCTIONS (continued)

For analog sensing input 12 should be grounded and a positive signal, with respect to ground, Pin 8, applied to Pin 4.

**RAMP GENERATOR** — (Pins 5, 6, 7) (refer to Figure 2). A preset voltage applied to Pin 5 will initiate the generation of a ramp whose final value is determined by the voltage applied to Pin 5. The voltage applied to Pin 6 will determine how much of the full ramp, shown in Figure 2, is used. The charging current passing through Pin 7 to the ramp generator timing capacitor determines the ramp slope.

When Pin 6 is held at $-V_{CC}$ a charging current of 1.2 mA is delivered to Pin 7, regardless of the voltage of Pin 5. This represents the high acceleration period shown in Figure 2.

If the preset voltage applied to Pin 5 is equal to or less than the voltage on Pin 6 the charging current will be 1.2 mA, or high acceleration.

If the preset voltage applied to Pin 5 is between $V_{Pin\ 6}$ and 2 $V_{Pin\ 6}$ the charging current is 1.2 mA (high acceleration) until the voltage at the reference input of the control amplifier equals $V_{Pin\ 6}$. At this point the charging current will switch to 5.0 μA; i.e. low acceleration.

If the preset voltage applied to Pin 5 is greater than 2 $V_{Pin\ 6}$ the charging current will be 1.2 mA (high acceleration) until the control amplifier's reference input reaches $V_{Pin\ 6}$ when it will switch to 5.0 μA (low acceleration) until 2 $V_{Pin\ 6}$ is reached. At this point the charging current will revert to 1.2 mA, high acceleration, until the final value of $V_{Pin\ 5}$ is reached.

Should the preset voltage at Pin 5 fall below 80 mV, the triac trigger pulses are inhibited and the circuit resets. This fact should be borne in mind when switching from one preset value to another.

As long as the voltages applied at Pins 5 and 6 are derived from the internal voltage regulator, they and the voltage on Pin 4 are ratioed and thus independent of the voltage regulator spread and temperature coefficient.

**CURRENT LIMITER** — (Pin 3). Safe operation of the motor and triac under all conditions is ensured by reducing the motor speed if a preset current limit is exceeded.

This is achieved as follows: The motor current will set up an alternating current, consisting of positive and negative peaks through the shunt resistor (0.05 Ω in Figure 4).

The negative peaks of this current are fed through a resistor to Pin 3 where they are compared with a preset current defined by a resistor between Pin 3 and $+V_{CC}$. An excessive shunt current will try to pull Pin 3 below $-V_{CC}$, but the current limiter becomes active at this point and reduces the charge on $C_{Pin\ 7}$, consequently reducing the motor speed.

Thus the value of the shunt and the ratio of the two resistors to Pin 3 fix the level at which the limiter becomes active, while the parallel equivalent of the two resistors determines the magnitude of the discharge current and thus how rapidly the circuit responds to an overcurrent condition.

**CONTROL AMPLIFIER** — (Pin 16). Connected to this pin is a network which compensates electrically for the mechanical characteristics of the motor and its load to give the circuit optimum closed loop stability and transient response.

The component values are best determined empirically by connecting R and C substitution boxes and looking for the best results.

**TRIGGER PULSE GENERATOR** — (Pins 1, 2, 13, 14, 15). This circuit performs four functions:

1. The conversion of the control amplifier's dc output level to a proportional firing angle positioned to within half a line cycle.
2. The calibration of the pulse width.
3. The repetition of the firing pulse if the triac fails to latch, or if the current is interrupted by brush bounce.
4. To delay the firing pulse until the current crosses zero at wide firing angles.

$R_{Pin\ 15}$ and $C_{Pin\ 14}$ fix the sawtooth while $C_{Pin\ 14}$ also determines the pulse width.

Pin 13 is the trigger pulse output. A current limiting resistor is essential on this pin. This configuration will drive two thyristors controlling a bridge if the supply for the speed controller is isolated.

## TYPICAL APPLICATIONS

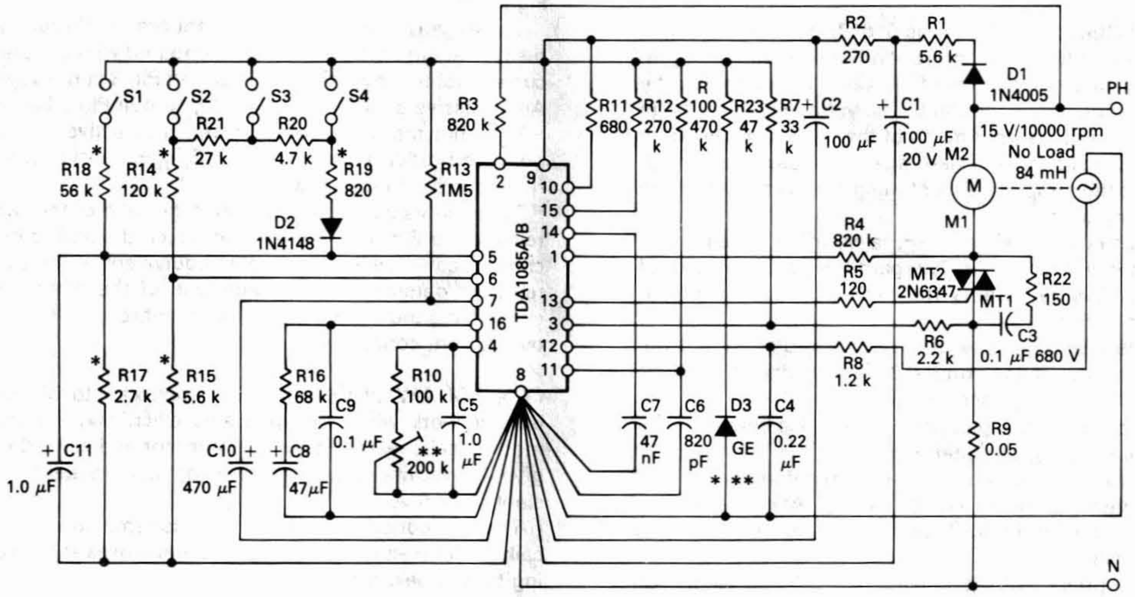

R2
270
R1
5.6 k
D1
1N4005
PH
S1
S2
S3
S4
R21
27 k
R20
4.7 k
R3
820 k
R11
680
R12
270 k
R
100
470 k
R23
47 k
R7
33 k
C2
100 µF
C1
100 µF
20 V
15 V/10000 rpm
No Load
84 mH
M2
M
M1
R18
56 k
R14
120 k
R19
820
R13
1M5
D2
1N4148
TDA1085A/B
2
9
10
15
14
1
5
6
7
16
4
13
3
12
11
8
R4
820 k
R5
120
MT2
2N6347
MT1
R22
150
R6
2.2 k
C3
0.1 µF 680 V
R8
1.2 k
R17
2.7 k
R15
5.6 k
R16
68 k
C9
0.1 µF
R10
100 k
200 k
C5
1.0 µF
C7
47 nF
C6
820 pF
D3
GE
C4
0.22 µF
R9
0.05
C11
1.0 µF
C10
470 µF
C8
47 µF
N
*
**
***

FIGURE 4 — CLOSED LOOP, FULLY PROGRAMMED, MULTI-SPEED SYSTEM WITH CURRENT LIMITING

* Chosen to suit the speeds required
** Adjust for the highest speed
*** Required only with 'A' suffix device

**Speed Control Resistor Network Equations**

| | | |
|---|---|---|
| R17 | = | given |
| R18 | = | $R17\,(\frac{15.5\ V}{V_W} - 1)$ |
| R19 | = | $R17\,(\frac{14.8\ V}{V_{spin\ 2}} - 1)$ |
| R20 | = | $R17\,(\frac{14.8\ V}{V_{spin\ 1}} - 1) - R19$ |
| R21 | = | $R17\,(\frac{14.8\ V}{k.V_W} - 1) - R19 - R20$ |
| R15 | = | $R21\,(\frac{K.V_W}{15.5\ V\ (2-K)})$ |
| R14 | = | $R15\,(\frac{15.5\ V}{V_W} - 1)$ |

The ratio distribute speed to wash speed can be chosen as:

$$\frac{V_{DIST}}{V_{WASH}} \leqslant 2 = K$$

| | S1 | S2 | S3 | S4 | $V_{Pin\ 5}$ | $V_{Pin\ 6}$ |
|---|---|---|---|---|---|---|
| Wash | sc | oc | oc | oc | $V_W$ | 0 |
| Distribute | oc | sc | oc | oc | $KV_W$ | $V_W$ |
| Spin 1 | oc | oc | sc | oc | $>KV_W$ | $\frac{K}{2}V_W$ |
| Spin 2 | oc | oc | oc | sc | $>>KV_W$ | $\simeq\frac{K}{2}V_W$ |

sc = switch closed
oc = switch open

**Note:**
When changing from one speed to another $V_{Pin\ 5}$ must not be allowed to fall below 80 mV — otherwise the circuit will reset and restart from zero.

The component values given in Figure 4 correspond to:

$V_W$ = 0.7 V
$V_D$ = 1.13 V
$V_{spin\ 1}$ = 5.0 V
$V_{spin\ 2}$ = 11 V
K = 1.6

**FIGURE 5 — OPEN LOOP, SOFT START — WITH PROGRAMMED TIME TO MAX. SPEED**
**($t = C_{Pin\ 7} \cdot 65 \times 10^5$)**

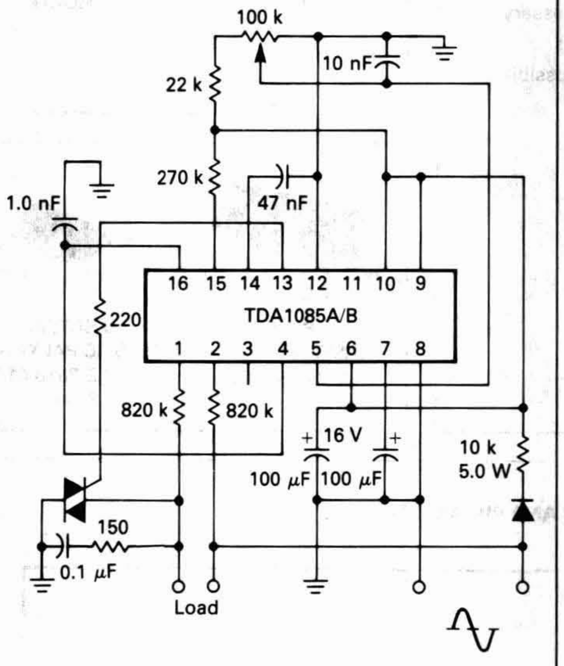
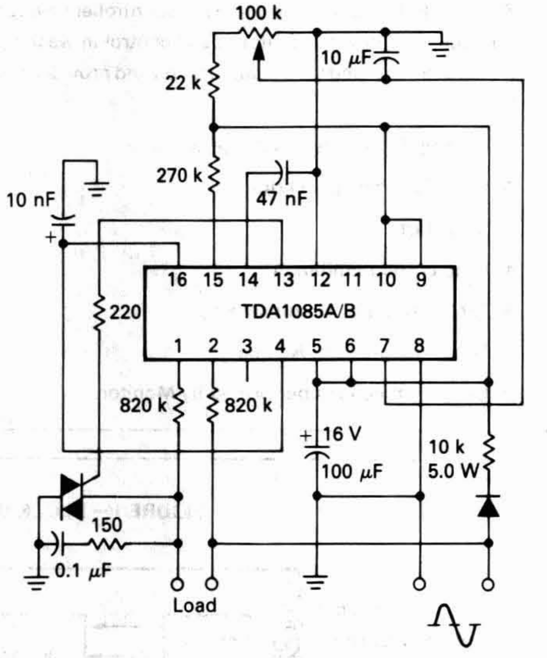

100 k
10 nF
22 k
270 k
47 nF
1.0 nF
16 15 14 13 12 11 10 9
TDA1085A/B
1 2 3 4 5 6 7 8
220
820 k
820 k
16 V
100 μF
100 μF
10 k
5.0 W
150
0.1 μF
Load

**FIGURE 6 — OPEN LOOP, SOFT-START/SOFT-STOP, LIGHTING/INDUCTIVE LOAD CONTROLLER**


100 k
10 μF
22 k
270 k
47 nF
10 nF
16 15 14 13 12 11 10 9
TDA1085A/B
1 2 3 4 5 6 7 8
220
820 k
820 k
16 V
100 μF
10 k
5.0 W
150
0.1 μF
Load

**MOTOROLA**

# TDA1085C

## Designer's Data Sheet

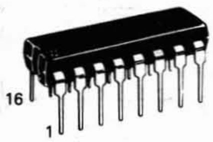
### UNIVERSAL MOTOR SPEED CONTROLLER

The TDA 1085C is a phase angle triac controller having all the necessary functions for universal motor speed control in washing machines.
It operates in closed loop configuration and provides two ramps possibilities.

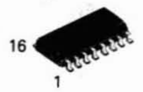
- On-chip frequency to voltage converter
- On-chip ramps generator
- Soft start
- Load current limitation
- Tachogenerator circuit sensing
- Direct supply from AC line
- Security functions performed by Monitor.

## UNIVERSAL MOTOR SPEED CONTROLLER

**LINEAR INTEGRATED CIRCUIT**

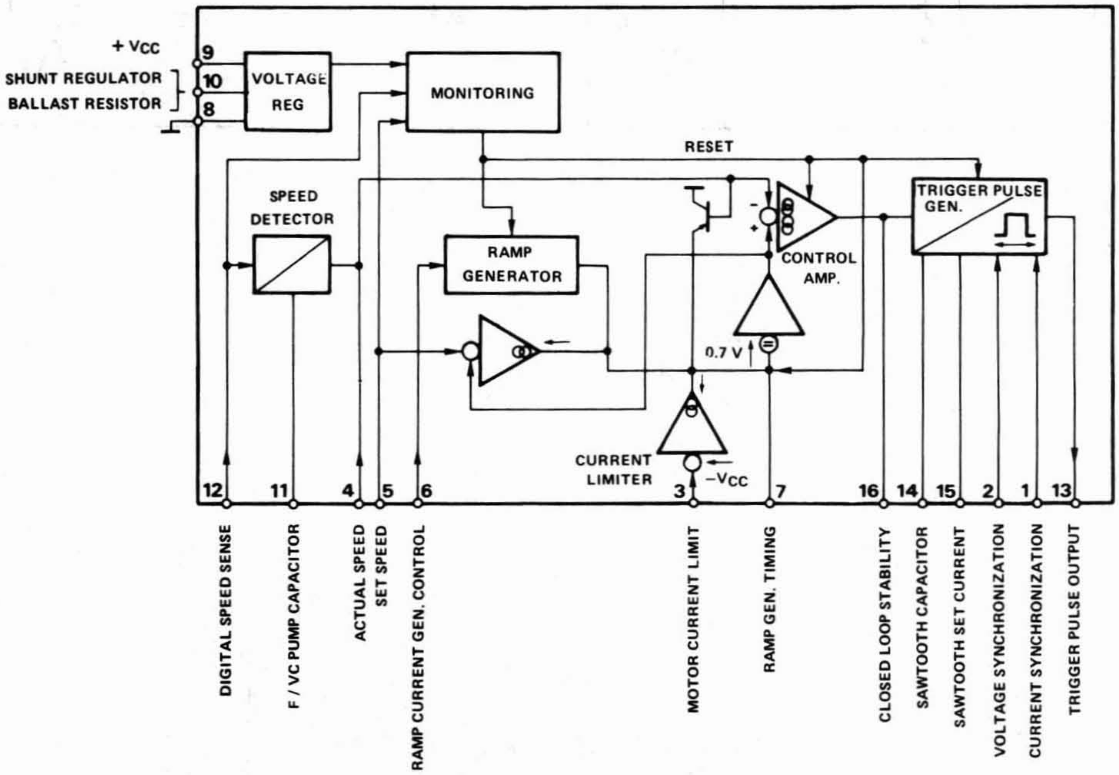


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05



**D SUFFIX**
PLASTIC PACKAGE
CASE 751B-01
SO-16

**FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT**


+ Vcc
SHUNT REGULATOR
BALLAST RESISTOR
9
10
8
VOLTAGE REG
MONITORING
RESET
SPEED DETECTOR
RAMP GENERATOR
TRIGGER PULSE GEN.
CONTROL AMP.
0.7 V
CURRENT LIMITER
−Vcc
12
11
4
5
6
3
7
16
14
15
2
1
13
DIGITAL SPEED SENSE
F / VC PUMP CAPACITOR
ACTUAL SPEED
SET SPEED
RAMP CURRENT GEN. CONTROL
MOTOR CURRENT LIMIT
RAMP GEN. TIMING
CLOSED LOOP STABILITY
SAWTOOTH CAPACITOR
SAWTOOTH SET CURRENT
VOLTAGE SYNCHRONIZATION
CURRENT SYNCHRONIZATION
TRIGGER PULSE OUTPUT

## MAXIMUM RATINGS ($T_A$ = 25 °C, Voltages are referred to pin 8 [Ground])

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply, when externally regulated, $V_{pin9}$ | $V_{CC}$ | 15 | V |
| Maximum Voltage per listed pin | $V_{pin}$ | | V |
| pin 3 | | +5 | |
| pin 4-5-6-7-13-14-16 | | 0 to $+V_{CC}$ | |
| pin 10 | | 0 to +17 | |
| Maximum Current per listed pin | $I_{pin}$ | | mA |
| pin 1 and 2 | | −3 to +3 | |
| pin 3 | | −1 to +0 | |
| pin 9 ($V_{CC}$) | | 15 | |
| pin 10 shunt regulator | | 35 | |
| pin 12 | | −1 to +1 | |
| pin 13 | | −200 | |
| Maximum Power Dissipation | $P_D$ | 1 | W |
| Junction to Air Thermal Resistance | $R_{\theta JA}$ | 65 | °C/W |
| Operating Junction Temperature | $T_A$ | −10 to +120 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C)

| Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **VOLTAGE REGULATOR** | | | | | |
| Internally Regulated Voltage ($V_{pin9}$)<br>($I_{pin7}$ = 0, $I_{pin9} + I_{pin10}$ = 15 mA, $I_{pin13}$ = 0) | $V_{CC}$ | 15.0 | 15.3 | 15.6 | V |
| $V_{CC}$ Temperature Factor | TF | | −100 | | ppm/°C |
| Current Consumption ($I_{pin9}$)<br>($V_9$ = 15 v, $V_{12} = V_8 = 0$, $I_1 = I_2$ = 100 µA, all other pins not connected) | $I_{CC}$ | | 4.5 | 6.0 | mA |
| $V_{CC}$ Monitoring Enable Level | $V_{CC}$ EN | | $V_{CC}$ − 04 | | V |
| Disable Level | $V_{CC}$ DIS | | $V_{CC}$ − 1 | | |
| **RAMP GENERATOR** | | | | | |
| Reference Speed Input Voltage Range | $V_{pin5}$ | .08 | | 13,5 | V |
| Reference Input Bias Current | $-I_{pin5}$ | 0 | .8 | 1 | µA |
| Ramp Selection Input Bias Current | $-I_{pin6}$ | 0 | | 1 | µA |
| Distribution Starting Level Range ($V_{DS}$) | $V_{pin6}$ | 0 | | 2 | V |
| Distribution Final Level ($V_{DF}$)<br>$V_{pin6}$ = 0,75 V | $V_{DS}/V_{pin6}$ | 2.0 | 2.09 | 2,20 | |
| High Acceleration Charging Current,<br>$V_{pin7}$ = 0 V | $-I_{pin7}$ | 1,0 | | 1,7 | mA |
| $V_{pin7}$ = 10 V | | 1,0 | 1,2 | 1,4 | |
| Distribution Charging Current,<br>$V_{pin7}$ = 2 volts | $-I_{pin7}$ | 4 | 5 | 6 | µA |

**ELECTRICAL CHARACTERISTICS** (continued)

| Characteristic | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **CURRENT LIMITER** | | | | | |
| Limiter Current Gain, $-I_{pin7}/I_{pin3}$ ($I_{pin3} = -300\ \mu A$) | Cg | 130 | 180 | 250 | |
| Detection Threshold Voltage, $I_{pin3} = -10\ \mu A$ | $V_{pin3\ TH}$ | 50 | 65 | 80 | mV |
| **FREQUENCY TO VOLTAGE CONVERTER** | | | | | |
| Input Signal "Low Voltage" | $V_{12\ L}$ | − 100 | | | mV |
| Input Signal "High Voltage" | $V_{12\ H}$ | + 100 | | | mV |
| Monitoring Reset Voltage | $V_{12\ R}$ | 5 | | | V |
| Negative Clamping Voltage, $I_{pin12} = -200\ \mu A$ | $-V_{12\ CL}$ | | .6 | | V |
| Input Bias Current | $-I_{pin12}$ | | 25 | | µA |
| Internal Current Source Gain $G = \frac{I_{pin4}}{I_{pin11}}$, $V_{pin4} = V_{pin11} = 0$ | G.0 | 10.0 | 10.3 | 10.5 | |
| Gain Linearity versus Voltage on pin4 ($G_{8.6}$ = Gain for $V_{pin4}$ = 8.6 Volts) | $G/G_{8.6}$ | | | | |
| $V_4 = 0\ V$ | | 1.040 | 1.050 | 1.060 | |
| $V_4 = 4.3\ V$ | | 1.015 | 1.025 | 1.035 | |
| $V_4 = 12\ V$ | | .965 | .975 | .985 | |
| Gain Temperature Effect ($V_{pin4} = 0$) | TF | | 350 | | ppm/°C |
| Output Leakage Current ($I_{pin11} = 0$) | $-I_{pin4}$ | 0 | | 100 | nA |
| **CONTROL AMPLIFIER** | | | | | |
| Actual Speed Input Voltage Range | $V_{pin4}$ | 0 | | 13.5 | V |
| Input Offset Voltage $V_{pin5} - V_{pin4}$ ($I_{pin16} = 0$, $V_{pin16}$ = 3 and 8 Volts) | $V_{off}$ | 0 | | 50 | mV |
| Amplifier Transconductance $I_{pin16}/\Delta\ (V_5 - V_4)$ ($I_{pin16}$ = + and − 50 µA, $V_{pin16}$ = 3 Volt) | T | 270 | 340 | 400 | µA/V |
| Output Current Swing Capability | $I_{pin16}$ | | | | |
| Source | | − 200 | − 100 | − 50 | µA |
| Sink | | 50 | 100 | 200 | µA |
| Output Saturation Voltage | $V_{16\ sat}$ | | | .80 | V |
| **TRIGGER PULSE GENERATOR** | | | | | |
| Synchronization Level Currents | | | | | |
| Voltage Line Sensing | $I_{pin2}$ | | ± 50 | ± 100 | µA |
| Triac Sensing | $I_{pin1}$ | | ± 50 | ± 100 | µA |
| Trigger Pulse Duration ($C_{pin14}$ = 47 nF, $R_{pin15}$ = 270 kΩ) | $T_p$ | | 55 | | µS |
| Trigger Pulse Repetition Period, conditions as a.m. | $T_R$ | | 220 | | µS |
| Output Pulse Current $V_{pin13} = V_{cc} - 4$ Volts | $-I_{pin13}$ | 180 | 192 | | mA |
| Output Leakage Current $V_{pin13} = -3$ Volts | $I_{13\ L}$ | | | 30 | µA |
| Full Angle Conduction Input Voltage | $V_{14}$ | | 11.7 | | V |
| Saw Toth "High" Level Voltage | $V_{14\ H}$ | 12 | | 12.7 | V |
| Saw Tooth Discharge Current, $I_{pin15} = 100\ \mu A$ | $I_{pin14}$ | 95 | | 105 | µA |

## GENERAL DESCRIPTION

The TDA 1085C triggers a triac accordingly to the speed regulation requirements. Motor speed is digitally sensed by a tachogenerator and then converted into an analog voltage.

The speed set is externally fixed and is applied to the internal linear regulation input after having been submitted to programmable acceleration ramps. The overall result consists in a full motor speed range with two acceleration ramps which allow efficient washing machine control (Distribute function).

Additionnally, the TDA 1085C protects the whole system against AC line stop or variations, overcurrent in the motor and tachogenerator failure.

## INPUT/OUTPUT FUNCTIONS

(referred to figure 1 and 8)

**VOLTAGE REGULATOR – (pins 9 and 10)** This is a parallel type regulator able to sink a large amount of current and offering good characteristics. Current flow is provided from AC line by external dropping resistors R1, R2, and rectifier: This half wave current is used to feed a smoothering capacitor, the voltage of which is checked by the IC.

When $V_{CC}$ is reached, the excess of current is derived by another dropping resistor R10 and by pin 10. These three resistors must be determined in order:

- to let 1mA flow through pin 10 when AC line is minimum and $V_{CC}$ consumption is maximum (fast ramps and pulses present).
- to let $V_{10}$ reach 3V when AC line provides maximum current and $V_{CC}$ consumption is minimum (no ramps and no pulses).
- all along the main line cycle, the pin 10 dynamic range must not be exceeded unless loss of regulation.

An AC line supply failure would cause shut down.

The double capacitive filter built with $R_1$ and $R_2$ gives an efficient $V_{CC}$ smoothing and helps to remove noise from set speeds.

**SPEED SENSING – (pins 4-11-12)** The IC is compatible with an external analog speed sensing: its output must be applied to pin 4, and pin 12 connected to pin 8.

In most of the applications it is more convenient to use a digital speed sensing with an unexpensive tachogenerator which doesn't need any tuning. During every positive cycle at pin 12, the capacitor $C_{pin\ 11}$ is charged to almost $V_{CC}$ and during this time, pin 4 delivers a current which is 10 time the one charging $C_{pin\ 11}$. The current source gain is called G and is tightly specified, but nevertheless requires an adjustment on $R_{pin\ 4}$. The current into this resistor is proportional to $C_{pin\ 11}$ and to the motor speed; being filtered by a capacitor, $V_{pin\ 4}$ becomes smoothered and represents the "true actual motor speed".

To maintain linearity into the high speed range, it is important to verify that $C_{pin\ 11}$ is fully charged: the internal source on pin 11 has 100 KΩ impedance. Nevertheless $C_{pin\ 11}$ has to be as high as possible as it has a large influence on FV/C temperature factor. A 470 KΩ resistor between pins 11 and 9 reduces leakage currents and temperature factor as well, down to neglectable effects.

Pin 12 has also a monitoring function: when its voltage is above 5V, the trigger pulses are inhibited and the IC is reset. It also senses the tachogenerator continuity and in case of any circuit aperture, it inhibits pulse, avoiding the motor to run out of control. In the TDA 1085C, pin 12 is negatively clamped by an internal diode which removes the necessity of the external one used in the former circuit.

**RAMP GENERATOR – (pins 5-6-7)** The true Set Speed value taken in consideration by the regulation is the output of the ramp generator (pin 7). With a given value of speed set input (pin 5), the ramp generator charges an external capacitor $C_{pin\ 7}$ up to the moment $V_{pin\ 5}$ (set speed) equals $V_{pin\ 4}$ (true speed), see fig. 2. The IC has an internal charging current source of 1.2mA and delivers it from 0 to 12 V at pin 7. It is the high acceleration ramp (5 seconds typ.) which allows rapid motor speed changes without excessive strains on the mechanics. The TDA 1085C offers in addition the possibility to break this high acceleration with the introduction of a low acceleration ramp (called Distribution) by reducing the pin 7 source current down to 5 μA under pin 6 full control, as shown by following conditions:

- Presence of high acceleration ramp $V_{pin\ 5} > V_{pin\ 4}$
- Distribution occurs in the $V_{pin\ 4}$ range (true motor speed) defined by $V_{pin\ 6} \leqq V_{pin\ 4} \leqq 2V_{pin\ 6}$

For two fixed values of $V_{pin\ 5}$ and $V_{pin\ 6}$, the motor speed will have high acceleration, excluding the time for $V_{pin\ 4}$ to go from $V_{pin\ 6}$ to two times this value, high acceleration again, up to the moment the motor has reached the set speed value, at which it will stay, see fig. 3.

Should a reset happen (whatever the cause would be), the above mentionned successive ramps will be fully reprocessed from 0 to the max. speed. If $V_{pin\ 6} = 0$, only the high acceleration ramp occurs.

To get a real zero speed position, pin 5 has been designed in such a way that its voltage from 0 to 80 mV is interpreted as a true zero. As a consequence, when changing the speed set position, the designer must be sure that any transient zero would not occur: if any, the entire circuit will be reset.

As the voltages applied by pins 5 and 6, are derived from the internal voltage regulator supply and pin 4 voltage is also derived from the same source, motor speed, which is determined by the ratios between above mentioned voltages, is totally independent from $V_{CC}$ variations and temperature factor.

**CONTROL AMPLIFIER – (pin 16)** It amplifies the difference between true speed (pin 4) and set speed (pin 5), through the ramp generator. Its output available at pin 16 is a double sense current source with a max. capability of ± 100 μA and a specified transconductance (340 μA/v.typ.). Pin 16 drives directly the trigger pulse generator, and must be loaded by an electrical network which compensates the mechanical characteristics of the motor and its load, in order to provide stability in any condition and shortest transient response, see fig. 4.

This network must be adjusted experimentally.

In case of a periodic torque variations, pin 16 provides directly the phase angle oscillations.

**TRIGGER PULSE GENERATOR – (pins 5 1-2-13-14-15)** This circuit performs four functions:

- The conversion of the control amplifier DC output level to a proportionnal firing angle at every main line half cycle.
- The calibration of pulse duration.
- The repetition of the pulse if the triac fails to latch on if the current has been interrupted by brush bounce.
- The delay of firing pulse until the current crosses zero at wide firing angles and inductive loads.

$R_{pin\ 15}$ programs the pin 14 discharging current. Saw-tooth signal is then fully determined by R15 and C14 (usually 47 nF). Firing pulse duration and repetition period are in inverse ratio to the saw-tooth slope.

Pin 13 is the pulse output and an external limiting resistor is mandatory. Max current capability is 200 mA.

**CURRENT LIMITER – (pin 3)** Safe operation of the motor and triac under all conditions is ensured by limiting the peak current. The motor current develops an alternative voltage in the shunt resistor (0.05 ohm in fig. 4). The negative half waves are transferred to pin 3 which is positively preset at a voltage determined by resistors $R_3$ and $R_4$. As motor current increases, the dynamical voltage range of pin 3 increases and when pin 3 becomes slightly negative in respect of pin 8 a current starts to circulate in it. This current, amplified typically 180 times, is then used to discharge pin 7 capacitor and, as a result, reduces firing angle down to a value where an equilibrium is reached. The choice of resistors $R_3$, $R_4$ and shunt determines the magnitude of the discharge current signals on $C_{pin7}$.

Notice that the current limiter acts only on peak Triac current.

## APPLICATION NOTES

(referred to fig. 4)

### PRINTED CIRCUIT LAYOUT RULES

In the common applications, where TDA1085C is used, there is on the same board, presence of high voltage, high currents as well as low voltage signals where millivolts count. It is of first magnitude importance to separate them each other and to respect following rules:

- Capacitors decoupling pins which are the inputs of the same comparator, must be physically close to the IC, close to each other and grounded in the same point.
- Ground connexion for tachogenerator must be directly connected to pin 8 and should ground only the tacho. In effect the latter is a first magnitude noise generator due to its proximity of the motor which induces high dØ/dt signals.
- The ground pattern must be in the "star style", in order to fully eliminate power currents flowing in the ground network devoted to capacitors decoupling sensitive pins: (4-5-7-11-12-14-16).

As an example, fig. 5 presents a PC board pattern which concerns the group of sensitive pins and their associated capacitors into which the a.m. rules have been implemented. Notice the full separation of "Signal World" from "Power" one by line AB and their communication by a unique strip.

These rules will lead to much satisfactory volume production in the sense that speed adjustment will stay valid in the entire speed range.

### POWER SUPPPLY

As dropping resistor dissipates noticeable power, it is necessary to reduce the $I_{CC}$ needs down to a minimum. Triggering pulses, if a certain number of repetition is in reserve to cope with motor brush wearing at end of its life, are the largest $I_{CC}$ user. Classical worst case configuration have to be considered to select dropping resistor. In addition the parallel regulator must be always into its dynamic range, i.e. $I_{pin\ 10}$ over 1 mA and $V_{pin\ 10}$ over 3 volt in any extreme configuraton. The double filtering cell is mandatory.

### TACHOGENERATOR CIRCUIT

The tacho signal voltage is proportional to the motor speed. Stability considerations, in addition, require a RC filter the pole of which must be looked at. The combination of both elements yield a constant amplitude signal on pin 12 in most of the speed range. It is recommended to verify this maximum amplitude to be within 1 volt peak in order to have the largest signal/noise ratio without resetting the integrated circuit (which occurs if $V_{pin\ 12}$ reaches 5.5 V). It must be also verified that the pin 12 signal is approximately balanced between "High" (over 300 mV) and "Low". A 8 poles tacho is a minimum for low speed stability and a 16 poles is even better.

The RC pole of the tacho circuit should be chosen within 30 Hz in order to be as far as possible from the 150 Hz which corresponds to the AC line 3rd harmonic generated by the motor during starting procedure. In addition, a high value resistor coming from $V_{CC}$ introduces a positive offset at pin 12, removes noise to be interpreted as a tacho signal. This offset should be designed in order to let pin 12 to reach at least – 200 mV (negative voltage) at the lowest motor speed. We remember the necessity of an individual tacho ground connection.

### FREQUENCY TO VOLTAGE CONVERTER – F V/C

$C_{pin\ 11}$ has a recommended value of 820 pF for 8 poles tachos and max. motor rpm of 15000, and $R_{pin\ 11}$ must be always 470 K.

$R_{pin\ 4}$ should be choosen to deliver within 12 volts at maximum motor speed in order to maximize signal/noise ratio. As the FV/C ratio as well as the $C_{pin\ 11}$ value are dispersed, $R_{pin\ 4}$ must be adjustable and should be made of a fixed resistor in serie with a trimmer representing 25% of the total. Adjustment would become easier.

Once adjusted, for instance at maximum motor speed, the F V/C presents a residual non linearity; the conversion factor (mV per R.P.M.) increases by within 7.7% as speed tends to zero. The guaranteed dispersion of the latter being very narrow, a maximum 1% speed error is guaranteed if during pin 5 network design the small set values are modified, once for ever, according this increase.

The following formulae gives $V_{pin\ 4}$:

$$V_{pin4} = 140 \cdot C_{pin11} \cdot R_4 \cdot f \cdot \frac{1}{\left(1 + \frac{180\ k}{R_{pin11}}\right)} \text{ in volt per Hertz.}$$

**SPEED SET – (pin 5)** Upon designer choice, a set of external resistors apply a serie of various voltages corresponding to the various motor speeds. When switching external resistors, verify that a voltage below 80 mV in never applied to pin 5, if no, a full circuit reset will occur.

**RAMPS GENERATOR — (pin 6)** If only a high acceleration ramp is needed, connect pin 6 to ground.

When a Distribute ramp should occur, pre-set a voltage on pin 6 to which corresponds the motor speed starting ramp point. Distribution (or low ramp) will continue up to the moment the motor speed would have reached twice the starting value.

The ratio of two is imposed by the IC. Nevertheless it could be externally changed downwards (fig. 6) or upwards (fig. 7).

The distribution ramp can be shortened by an external resistor from $V_{CC}$ charging $C_{pin\ 7}$, adding its current to the internal 5 μA generator.

**POWER CIRCUITS**

Triac Triggering pulse amplitude must be determined by Pin 13 resistor according the needs in Quadrant IV. Trigger pulses duration can be disturbed by noise signals, generated by the triac itself, which interfere within pins 14 and 16, precisely those which determine it. While easily visible this effect is harmless.

Triac must be protected from high AC line dV/dt during external disturbances by 100 nF × 100 Ω network.

Shunt resistor must be as non selfic as possible. It can be made locally by Constantan alloy wiring.

When the load is a DC fed universal motor through a rectifier bridge, the triac must be protected from commutating dV/dt by a 1 to 2 mH coil in serie with $MT_2$.

Synchronisation functions are performed by resistors sensing AC line and triac conduction. 820 K values are usual but could be reduced down to 330 K in order to detect the Zeros with accuracy and to reduce the residual DC line component below 20 mA.

**CURRENT LIMITATION**

The current limiter starts to discharge pin 7 capacitor (reference speed) as Motor current reaches the designed threshold level. The loop gain is determined by the resistor connecting pin 3 to the serie shunt. Experience has shown that its optimal value for a 10 A rms limitation is within 2 KΩ. Pin 3 input has a sensitivity in current which is limited to reasonable values and should not react to spikes.

If not used, pin 3 must be connected to a max. positive voltage of 5 V rather to be left open.

**LOOP STABILITY**

The pin 16 network is predominant and must be adjusted experimentally during module development. The values indicated in fig. 4 are typical for washing machines applications but accept large modifications from one model to another. R16, it is the sole restriction, should not be below 33 k otherwise slew rate limitation will cause large transient errors for load steps.

FIGURE 2 — ACCELERATION RAMP

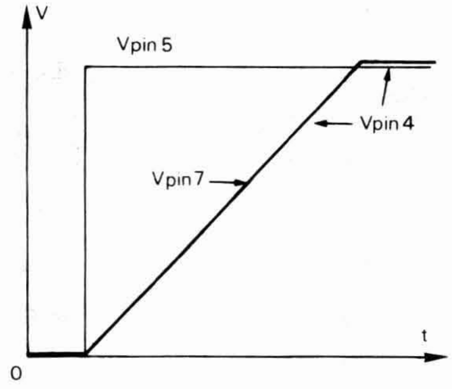


FIGURE 3 — PROGRAMMABLE DOUBLE ACCELERATION RAMP

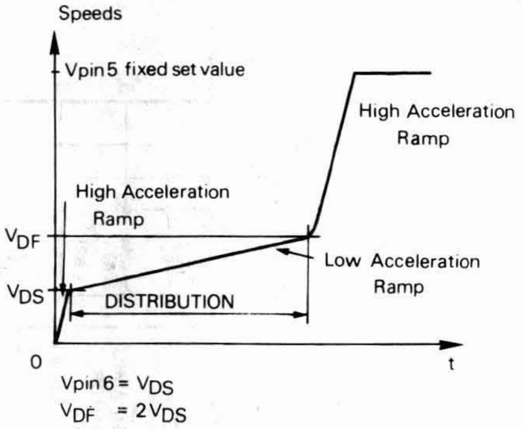
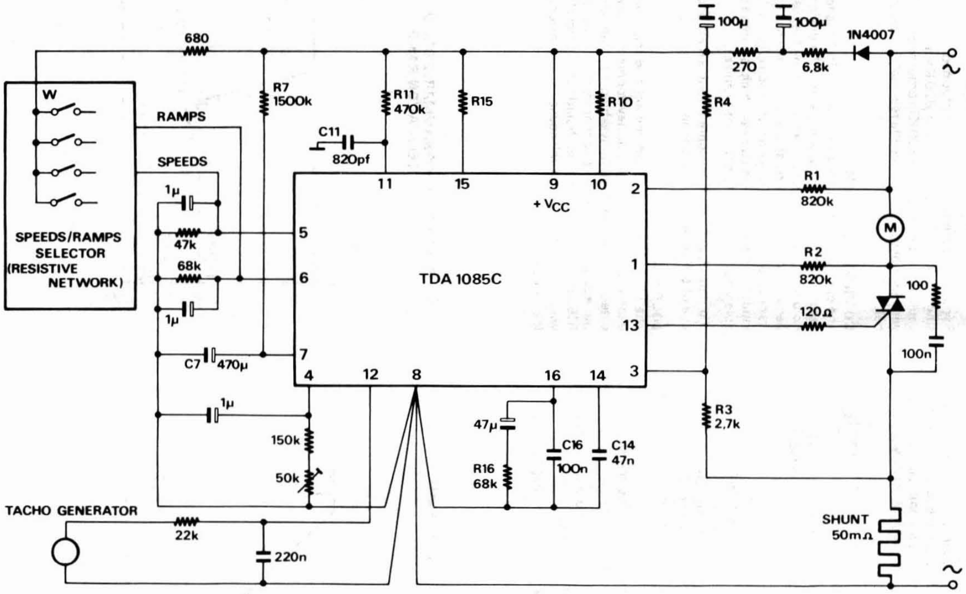


FIGURE 4 — BASIC APPLICATION CIRCUIT


680
W
RAMPS
SPEEDS
SPEEDS/RAMPS SELECTOR (RESISTIVE NETWORK)
R7
1500k
R11
470k
C11
820pf
R15
R10
R4
100μ
100μ
270
6,8k
1N4007
1μ
47k
68k
1μ
C7
470μ
1μ
150k
50k
11
15
9
10
2
+ $V_{CC}$
5
6
TDA 1085C
7
4
12
8
16
14
1
13
3
R1
820k
M
R2
820k
100
120Ω
100n
47μ
R16
68k
C16
100n
C14
47n
R3
2,7k
TACHO GENERATOR
22k
220n
SHUNT
50mΩ
~
~

Current limitation: 10 A adjusted by $R_4$ experimentally

Ramps High acceleration: 3200 rpm per second

Distribution ramp: 10 s from 850 to 1300 rpm

| **Speeds:** | **Pin 5 voltage Set:** | |
|---|---|---|
| Wash 800 rpm | 609 mV | Including non linearity corrections |
| Distribution 1300 | 996 mV | Including non linearity corrections |
| Spin 1 : 7500 | 5,912 V | Including non linearity corrections |
| Spin 2 : 15 000 | 12,000V | Adjustment point |

Motor Speed Range: 0 to 15 000 rpm

Tachogenerator 8 poles
delivering 30 v peak to peak at 6000 rpm, in open circuit

FV/C Factor: · 8 mV per rpm (12 v full speed) $C_{pin11}$ = 680 pF $V_{CC}$ = 15.3 v

Triac MAC 15 A-8 15 A 600 v
Igt min = 90 mA to cover Quad. IV at − 10 °C

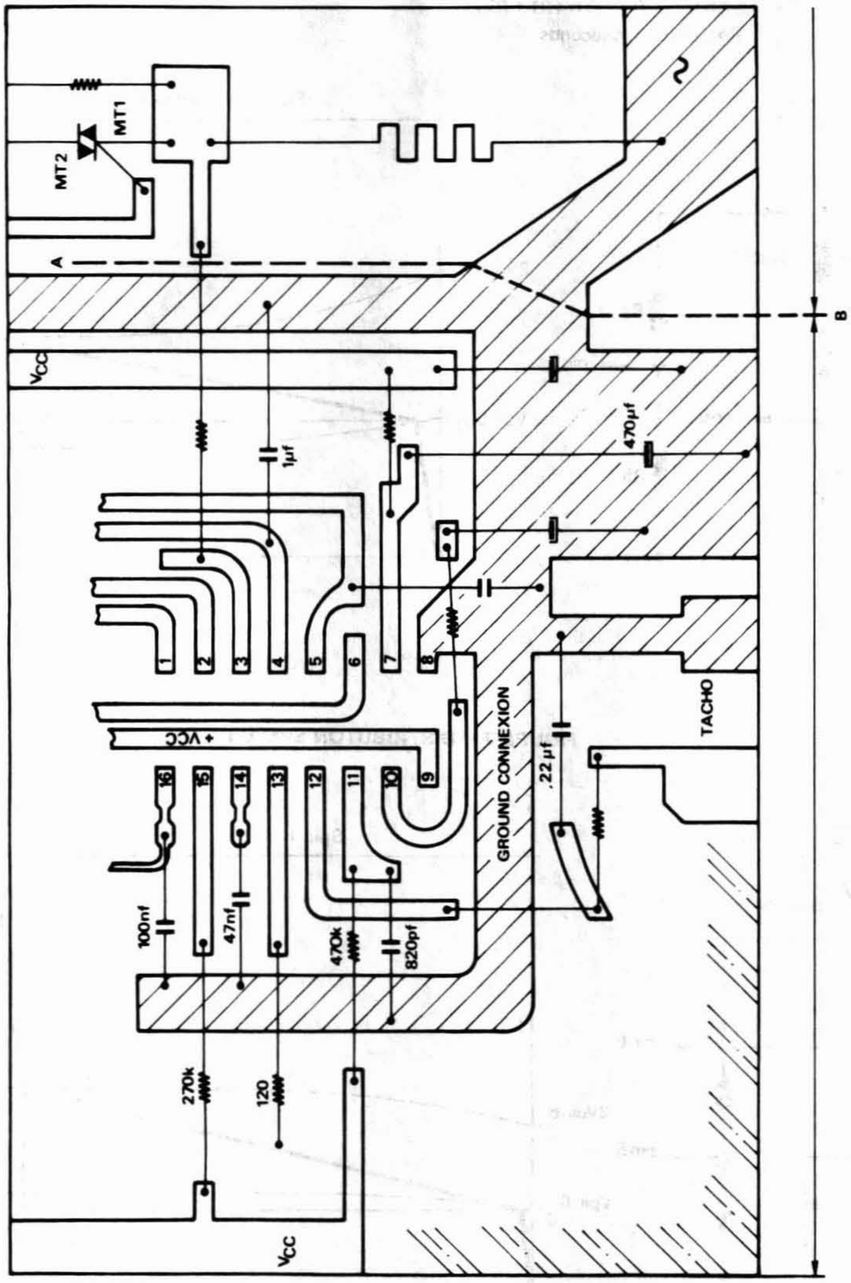
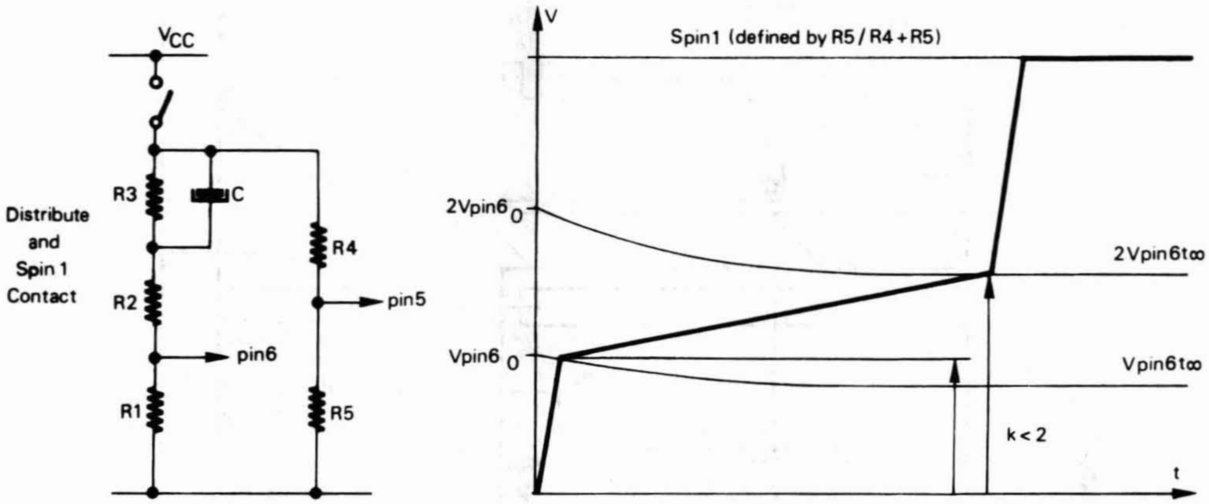

MT1
MT2
~
A
B
VCC
1µf
470µf
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
+VCC
GROUND CONNEXION
.22 µf
TACHO
100nf
47nf
470k
820pf
270k
120
VCC

FIGURE 5 — PC BOARD PATERN

FIGURE 6 — DISTRIBUTION SPEED k < 2

For k = 1.6, $R_3 = 0.6\ (R1 + R2)$,
$R_3C$ within 4seconds


V
Spin1 (defined by R5 / R4 + R5)
$V_{CC}$
R3
C
Distribute and Spin 1 Contact
R4
R2
pin5
pin6
R1
R5
2Vpin6 0
2Vpin6t∞
Vpin6 0
Vpin6t∞
k < 2
t

4

FIGURE 7 — DISTRIBUTON SPEED k > 2

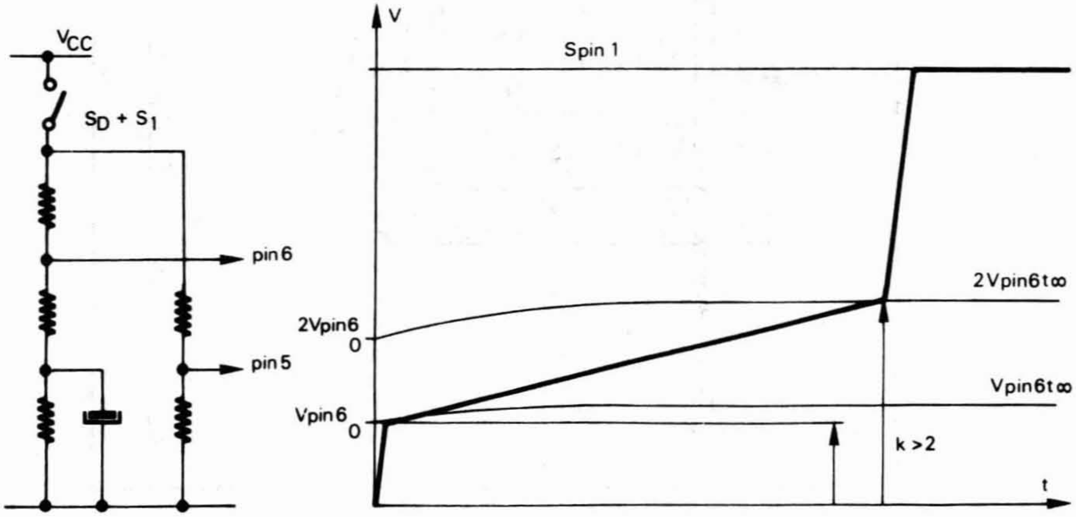
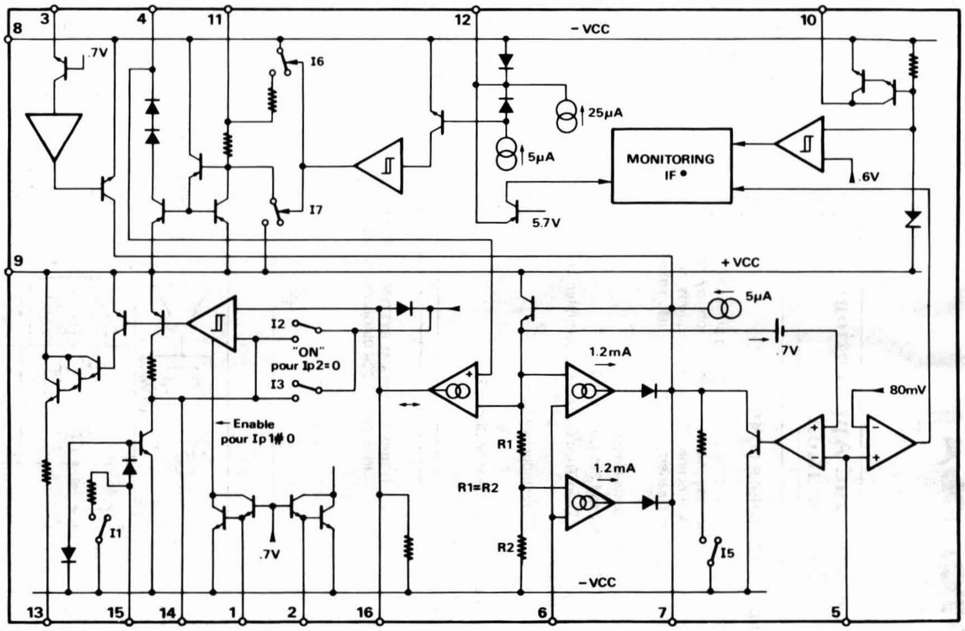

V
$V_{CC}$
Spin 1
$S_D + S_1$
pin 6
2Vpin6t∞
2Vpin6 0
pin 5
Vpin6t∞
Vpin6 0
k > 2
t

FIGURE 8 — INTERNAL CONFIGURATION


8
3
4
11
12
10
– VCC
.7V
I6
I7
25μA
5μA
MONITORING
IF •
.6V
5.7V
9
+ VCC
5μA
.7V
I2
"ON"
pour Ip2 = 0
I3
← Enable
pour Ip1 # 0
1.2mA
1.2mA
80mV
R1
R1 = R2
R2
I1
.7V
I5
– VCC
13
15
14
1
2
16
6
7
5

• (P12 connected) AND (VCC OK) AND (VP5>80mV)
THEN
(I1 OFF), (I2 OFF), (I4 OFF) AND (I5 OFF)

**MOTOROLA**

# TDA1185A

## Specifications and Applications Information

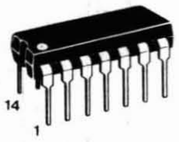
### TRIAC PHASE ANGLE CONTROLLER

The TDA1185A generates controlled triac triggering pulses and allows tacholess speed stabilization of universal motors by an integrated positive feedback function. Typical applications are power hand tools, vacuum cleaners, mixers and other small appliances.

- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses When Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 1.0 mA

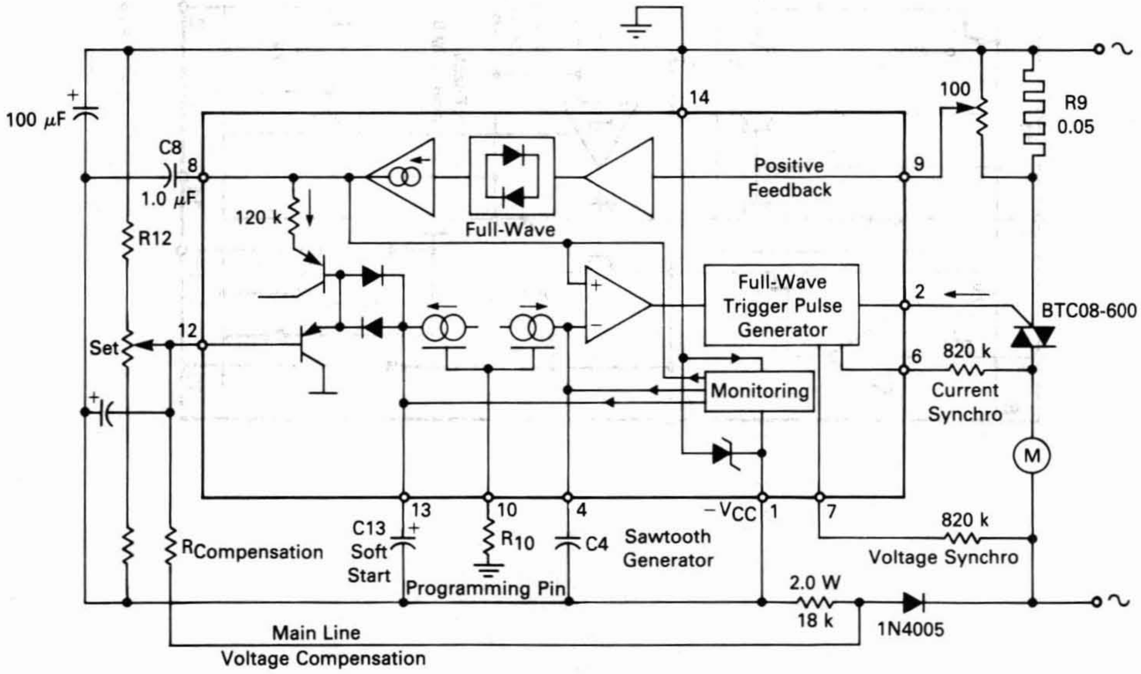
**TRIAC PHASE ANGLE CONTROLLER**

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



PLASTIC PACKAGE
CASE 646-05

FIGURE 1 — TYPICAL SYSTEM CONFIGURATION
— INTERNAL BLOCK DIAGRAM/PIN ASSIGNMENT


100 μF
C8
8
1.0 μF
R12
120 k
Full-Wave
Positive
Feedback
14
9
100
R9
0.05
Set
12
Full-Wave
Trigger Pulse
Generator
2
BTC08-600
6
820 k
Current
Synchro
Monitoring
M
13
10
4
−VCC
1
7
C13
Soft
Start
R10
C4
Sawtooth
Generator
820 k
Voltage Synchro
RCompensation
Programming Pin
2.0 W
18 k
1N4005
Main Line
Voltage Compensation

**MAXIMUM RATINGS** (Voltages are referred to Pin 14 (ground) unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Maximum Voltage Range per Listed Pin | $V_{Pin}$ | | Volt |
| Pins 3-5-11 (not connected) | | −20 to +20 | |
| Pins 4-8-13 | | $-V_{CC}$ to 0 | |
| Pin 2 | | −3.0 to +3.0 | |
| Maximum Positive Voltage (No minimum value allowed; see current ratings) | $V_{Pin\ 12}$<br>$V_{Pin\ 1}$ | +0<br>+0.5 | |
| Maximum Current per Listed Pin | $I_{Pin}$ | | |
| Pin 1 | | ±20 | mA |
| Pins 6 and 7 | | ±2.0 | mA |
| Pin 9 | | ±0.5 | mA |
| Pin 10 | | ±300 | μA |
| Pin 12 | | −500 | μA |
| Maximum Power Dissipation (at $T_A$ = 25°C) | $P_D$ | 250 | mW |
| Maximum Junction to Ambient Thermal Resistance | $R_{\theta JA}$ | 100 | °C/W |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +125 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C) Voltages are related to Pin 14 (ground)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply | | | | | |
| Zener Regulated Voltage, ($V_{Pin\ 1}$) $I_{Pin\ 1}$ = 2.0 mA | $-V_{CC}$ | −9.6 | −8.6 | −7.6 | Volt |
| Circuit Current Consumption, $I_{Pin\ 1}$ $V_{Pin\ 1}$ = −6.0 V, $I_{Pin\ 2}$ = 0 V | $-I_{CC}$ | −2.0 | −1.0 | — | mA |
| Monitoring Enable Supply Voltage ($V_{EN}$) | $V_{Pin\ 1EN}$ | $V_{CC}$ + 0.2 | — | $V_{CC}$ + 0.5 | Volt |
| Monitoring Disable Supply Voltage ($V_{DIS}$) | $V_{Pin\ 1DIS}$ | $V_{EN}$ + 0.12 | — | $V_{EN}$ + 0.3 | |
| Phase Set | | | | | |
| Control Voltage Static Offset $V_{Pin\ 8}$ − $V_{Pin\ 12}$ | $V_{off}$ | 1.2 | — | 1.8 | Volt |
| Pin 12 Input Bias Current | $I_{Pin\ 12}$ | −200 | — | 0 | nA |
| $V_{Pin\ 4}$ − $V_{Pin\ 12}$ Residual Offset | | — | 180 | — | mV |
| Soft Start | $I_{Pin\ 13}$ | −17 | −14 | −11 | μA |
| Capacitor Charging Current $R_{Pin\ 10}$ = 100 kΩ, $V_{Pin\ 13}$ from $-V_{CC}$ to −3.0 Volts | | | | | |
| Sawtooth Generator | | | | | |
| Sawtooth Capacitor Discharge Current $R_{10}$ = 100 kΩ $V_{Pin\ 4}$ from −2.0 to −6.0 Volts | $I_{Pin\ 4}$ | 67 | 70 | 73 | μA |
| Capacitor Charging Current | $I_{Pin\ 4}$ | −10 | — | −1.5 | mA |
| Sawtooth "High" Voltage ($V_{Pin\ 4}$) | $V_{HTH}$ | −2.5 | −1.6 | −1.0 | Volt |
| Sawtooth Minimum "Low" Voltage ($V_{Pin\ 4}$) referred to Pin 1 | $V_{LTH}$ | — | +1.5 | — | Volt |
| Positive Feedback | | | | | |
| Pin 9 Input Bias Current, $V_{Pin\ 9}$ = 0 | $I_{Pin\ 9}$ | — | 2 x $I_{Pin\ 10}$ | — | |
| Programming Pin Voltage Related to Pin 1 | $V_{Pin\ 10}$ | 1 | 1.25 | 1.5 | Volt |
| Transfer Function Gain $\Delta V_{Pin\ 8}/\Delta V_{Pin\ 9}$ | | | | | |
| $R_{10}$ = 100 kΩ, $\Delta V_{Pin\ 9}$ = 50 mV | A | — | 75 | — | |
| $R_{10}$ = 270 kΩ, $\Delta V_{Pin\ 9}$ = 50 mV | A | — | 36 | — | |
| Pin 8 Output Internal Impedance | $Z_{Pin\ 8}$ | — | 120 | — | kΩ |
| Trigger Pulse Generator | | | | | |
| Output Current (Sink) $V_{Pin\ 2}$ = 0 V | $I_{Pin\ 2}$ | 60 | — | 80 | mA |
| Output Leakage Current $V_{Pin\ 2}$ = +2.0 V | | — | — | 4.0 | μA |
| Output Pulse Width $C_1$ = 47 nF $R_{10}$ = 270 kΩ | tp | — | 55 | — | μs |
| Output Pulse Repetition Period $C_1$ = 47 nF $R_{10}$ = 270 kΩ | t | — | 420 | — | μs |
| Current Synchronization Threshold Levels $I_{Pin\ 6}$, $I_{Pin\ 7}$ | $I_{SYNC}$ | −40 | — | +40 | μA |

## CIRCUIT DESCRIPTION

The TDA1185A generates trigger pulses for triac control of power into an ac load. The firing angle is determined by generating a ramp voltage synchronized to the ac line half cycle and compared to an external set voltage representing the conduction angle.

Gate pulses are negative (sink current) and thus the triac is driven in its most effective quadrants (Q2–Q3).

If the load is a Universal motor (the speed of which is decreasing as torque increases), the TDA1185A allows to increase the firing angle proportionally to the motor current, sensed by a low value series resistor.

**Notice:** Perfect motor speed compensation cannot be provided by open-loop systems, since no negative feedback is used. Due to the low cost of tacholess systems, the TDA1185A is the optimum solution for applications tolerating 5% motor speed variations.

Nevertheless by accurate circuit design, these variations can be reduced down to 2% from no load to full load conditions.

## CIRCUIT FUNCTIONS

**DC POWER SUPPLY** — DC power is directly derived from the ac line through a 2.0 watt, 18 kΩ resistor, rectifier and filtering capacitor circuit. The latter being directly connected to the dropping resistor protects the whole IC from any ac line overvoltage. The $-V_{CC}$ voltage is internally regulated by an integrated zener. Referred to Pin 14 (ground) the power supply voltage is negative (−8.6 volts). The TDA1185A internal consumption is 1.0 mA.

**TRIGGER PULSE GENERATOR** — It delivers a 60 mA minimum pulse current (sink) through an internally short-circuit protected output. Pulse width is roughly proportional to $R_{10} \cdot C_4$ and is repeated every 420 μs if triac fails to latch or is switched off by brush bounce. With inductive loads, the current lags in respect of the voltage: Pin 6 delays the triggering pulse up to the moment the triac is off, in order to prevent erratic power control (see Figure 2). The logic structure guarantees full-wave triac operation.

**SAWTOOTH GENERATOR** — A constant current generator discharges the capacitor $C_4$, the voltage of which is the sawtooth signal synchronized with main line. Pin 4 voltage is reset to −1.6 volt at every ac line zero crossing (see Figure 3). The constant current generator is externally programmable by an external resistor connected to Pin 10:

$$I_{Pin\ 4} = I_{Pin\ 10}\ 10 \pm 5\%$$

$$I_{Pin\ 10} = \frac{-V_{CC} \pm 1.25}{R_{10}}$$

**MAIN COMPARATOR** — Its role is to determine the trigger pulse time which occurs as the sawtooth voltage equals set voltage. Fixed set values lead to a constant triac conduction angle unless positive current feedback is connected or soft start capacitor is not charged.

**SOFT START** — The TDA1185A allows the user to avoid any abrupt inrush current in the load, for various purposes: motor soft start, protection of high performance bulbs or ac line minimum disturbances.

The firing angle is established from zero to the set value according to a voltage ramp generated by a constant current delivered to capacitor $C_{13}$. The constant current value is:

$$I_{Pin\ 13} = 0.2 \times I_{Pin\ 10} \pm 10\%$$

The voltage ramp lasts as long as $V_{Pin\ 13}$ is lower than $V_{Pin\ 12}$. $V_{Pin\ 13}$ reset voltage is $-V_{CC}$. See Figure 4.

**Notice.** Universal motors do not have any motion effect as long as a minimum conduction angle is not reached. The time the voltage ramp reaches this threshold value is considered as "dead" time and can be eliminated by a series resistor at Pin 13. The voltage drop developed by $I_{Pin\ 13}$ makes the firing angle immediately reach the threshold value and have the soft start function without dead time. See Figure 5.

**POSITIVE CURRENT FEEDBACK** — The Universal motor speed drops as load increases. To maintain it as stable as possible, the triac firing angle must be increased. For this purpose the Pin 9 input senses the motor current as a voltage developed in a low resistor value, $R_g$, amplifies, rectifies and adds it to Pin 12 set voltage. The transfer function $\Delta V_{Pin\ 8} = f\ (\Delta V_{Pin\ 9})$ and is represented on Figure 6.

The gain in the linear region is dependent on $R_{10}$. The voltage transferred to Pin 8 is proportional to the average value of the motor current and is very close to its RMS value (as motor current is not far from a sine wave). This averaging effect is represented in Figure 7.

For large amplitude Pin 9 signals, the am function presents a saturation effect which limits the maximum firing angle increase. Figure 8 presents this aspect as well as the total Pin 8 voltage which is:

$$V_{Pin\ 8} = V_{Pin\ 12} + f(|V_{Pin\ 9}|\ R_{10}) + \text{offset}$$

The offset is the addition of two PN Junctions and is compensated with respect to $V_{Pin\ 4}$ (sawtooth) by additional diodes within the main comparator (See Figure 10).

The effect of positive feedback is described per Figure 9.

**MONITORING** — A central logic block performs the following functions: — ENABLE/DISABLE of the IC with respect to power supply voltage. Under DISABLE conditions, Pins 4, 8, 12, and 13 are forced to appropriate voltages to prepare for the next reset (See Figure 10).

## APPLICATION CONSIDERATIONS

**PINS CHARACTERISTICS** — Figure 10 describes more details in the internal IC layout and defines the pin characteristics. Pin 9 has a low internal impedance and requires a maximum 100 Ω trimmer on $R_g$ to adjust reaction ratio. Pin 8 must always be connected to $-V_{CC}$ through a filtering capacitor.

**TEMPERATURE EFFECTS** — The TDA1185A has very efficient internal temperature compensation. If positive current feedback is not connected, the RMS power delivered to the load is stabilized within ±0.2% over a temperature range of +20 to +70°C. The positive feedback introduces in the same temperature range, a drift of 250 mV on $V_{Pin\ 8}$; this slight firing angle increase may be successfully used to compensate a motor ohmic resistance increase with temperature as well.

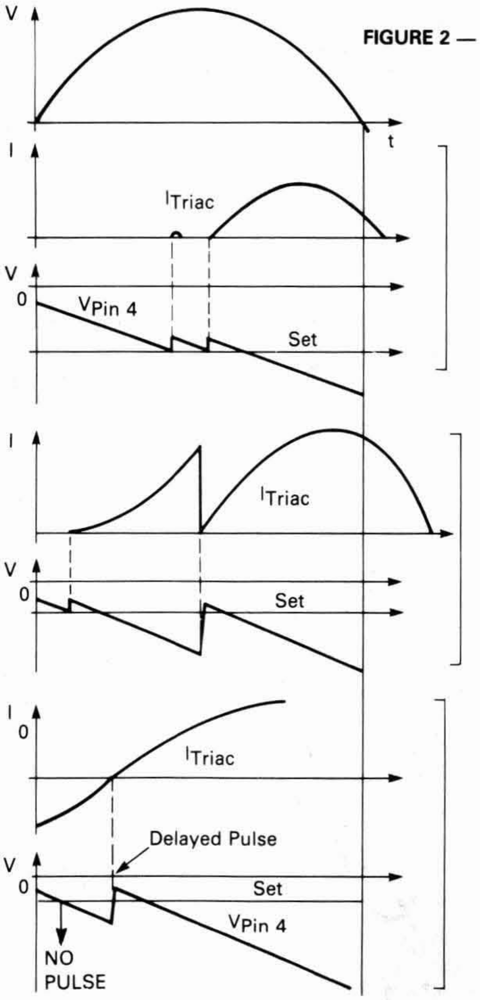
**MAIN LINE VOLTAGE COMPENSATION** — As the firing angle is independent of main line voltage, any change in the latter (usually ±15%) induces a very large power variation to the load. An external compensation must be used, introducing a $V_{Pin\ 12}$ decrease as $V_{mains}$ increases. An inexpensive resistor $R_{COMP}$, connected to the rectifier anode and to Pin 12 performs this role and its value depends on $V_{Pin\ 12}$, $R_{10}C_4$, $R_{12}$. $R_{COMP}$ can be empirically determined without difficulty under no load conditions.

**FIRING ANGLE DYNAMIC** — With purely resistive loads, the effective RMS applied power to the load is an increasing function of the firing angle (per Figure 11). We notice the fact that a firing angle of 150° provides 97% of the full power corresponding to 180°.

With inductive loads, as currents lag with respect to Voltage, 100% power corresponds to a firing angle which is smaller than 180°.

These considerations will simplify positive feedback design if maximum firing angle is accepted to be within 150–160°.

FIGURE 2 — MULTIPULSE GENERATION DELAYED PULSE



The triac failed to latch at the first pulse. Successive pulses are generated up to the moment latching oocurs.

The triac turned off due to brush bounce, a new pulse is immediately delivered.

Approaching full conduction, a pulse would occur when the triac still carries current; the pulse is delayed until the triac turns off.

FIGURE 3 — TRIGGERING PULSE TIMING

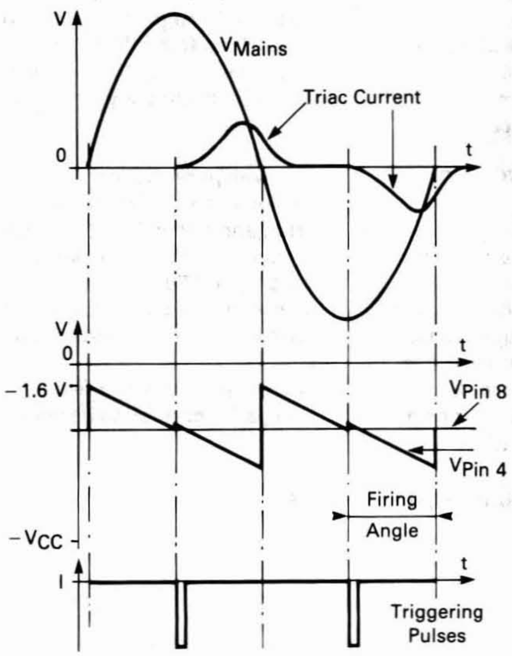

V
$V_{Mains}$
Triac Current
0
t
V
0
t
− 1.6 V
$V_{Pin\ 8}$
$V_{Pin\ 4}$
Firing
Angle
$-V_{CC}$
I
t
Triggering
Pulses

FIGURE 4 — SOFT START

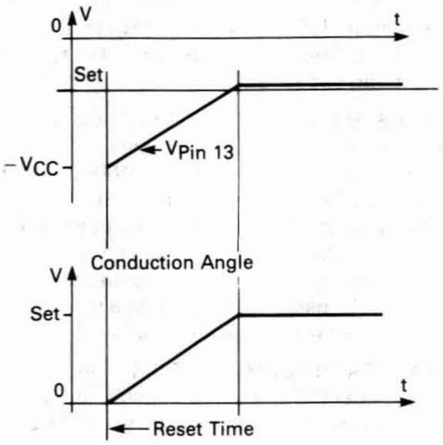

0
V
t
Set
$-V_{CC}$
$V_{Pin\ 13}$
V
Conduction Angle
Set
0
t
Reset Time

FIGURE 5 — SOFT START WITHOUT DEAD TIME

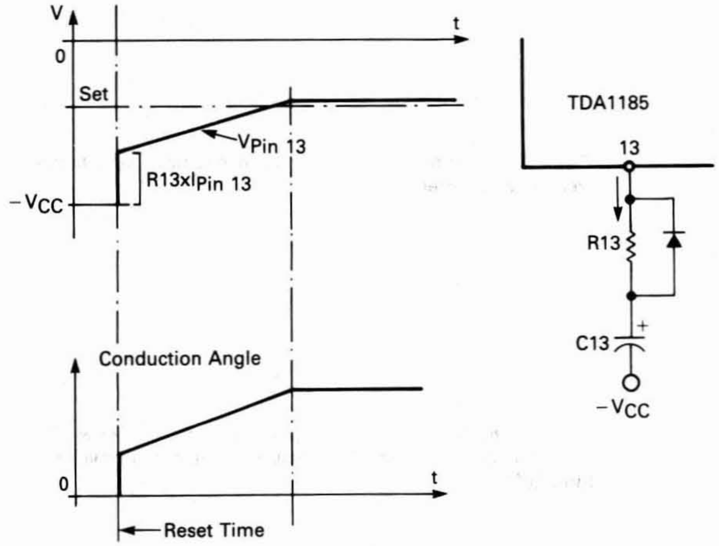

V
0
t
Set
$V_{Pin\ 13}$
$R13xI_{Pin\ 13}$
$-V_{CC}$
Conduction Angle
0
t
Reset Time
TDA1185
13
R13
C13
+
$-V_{CC}$

FIGURE 6 — TRANSFER FUNCTION

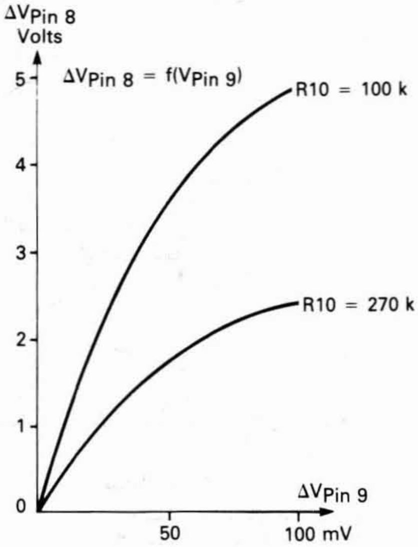


FIGURE 7 — AVERAGING EFFECT OF TRANSFER FUNCTION

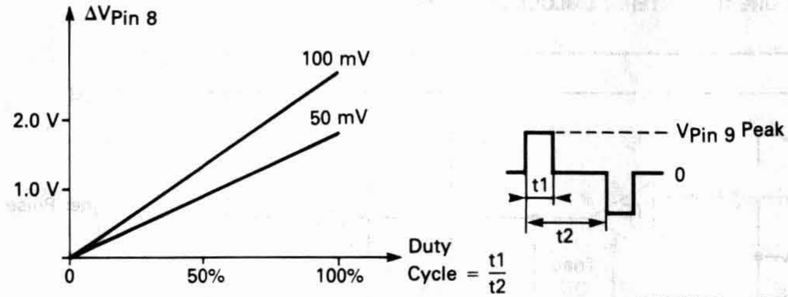


FIGURE 8 — TRANSFER FUNCTION (Pin 8/Pin 9)

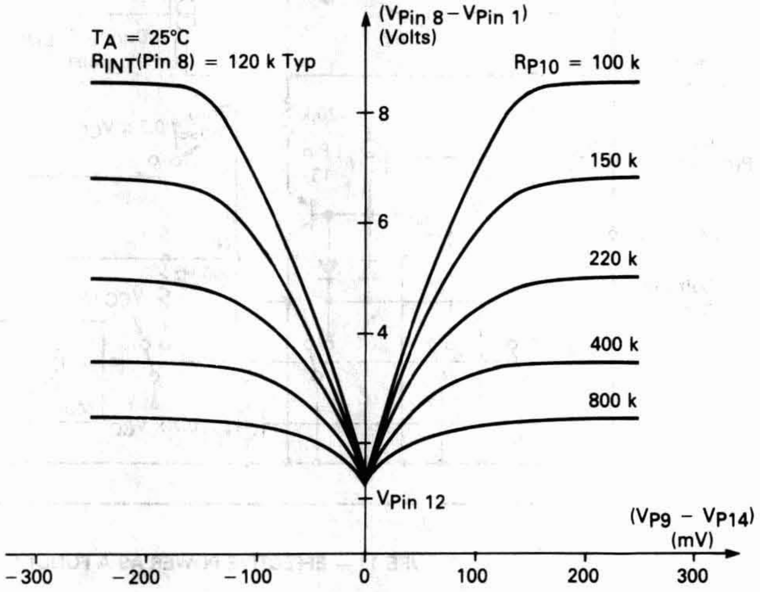
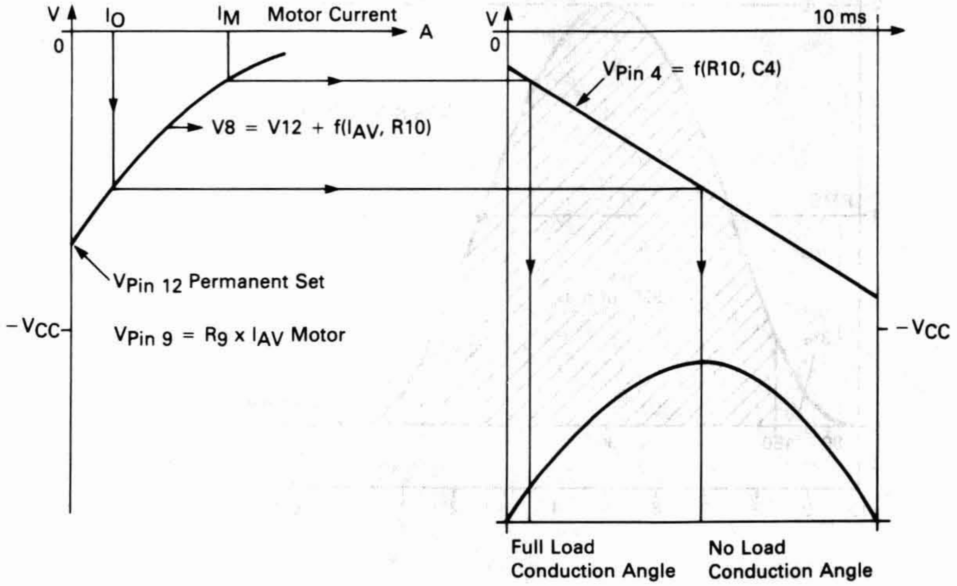


FIGURE 9 — POSITIVE FEEDBACK EFFECT
offset Voltages have been neglected



V
0
$I_O$
$I_M$
Motor Current
A
V8 = V12 + f($I_{AV}$, R10)
$V_{Pin\ 12}$ Permanent Set
$-V_{CC}$
$V_{Pin\ 9}$ = $R_9$ x $I_{AV}$ Motor
V
0
10 ms
$V_{Pin\ 4}$ = f(R10, C4)
$-V_{CC}$
Full Load Conduction Angle
No Load Conduction Angle

FIGURE 10 — INTERNAL BLOCK DIAGRAM

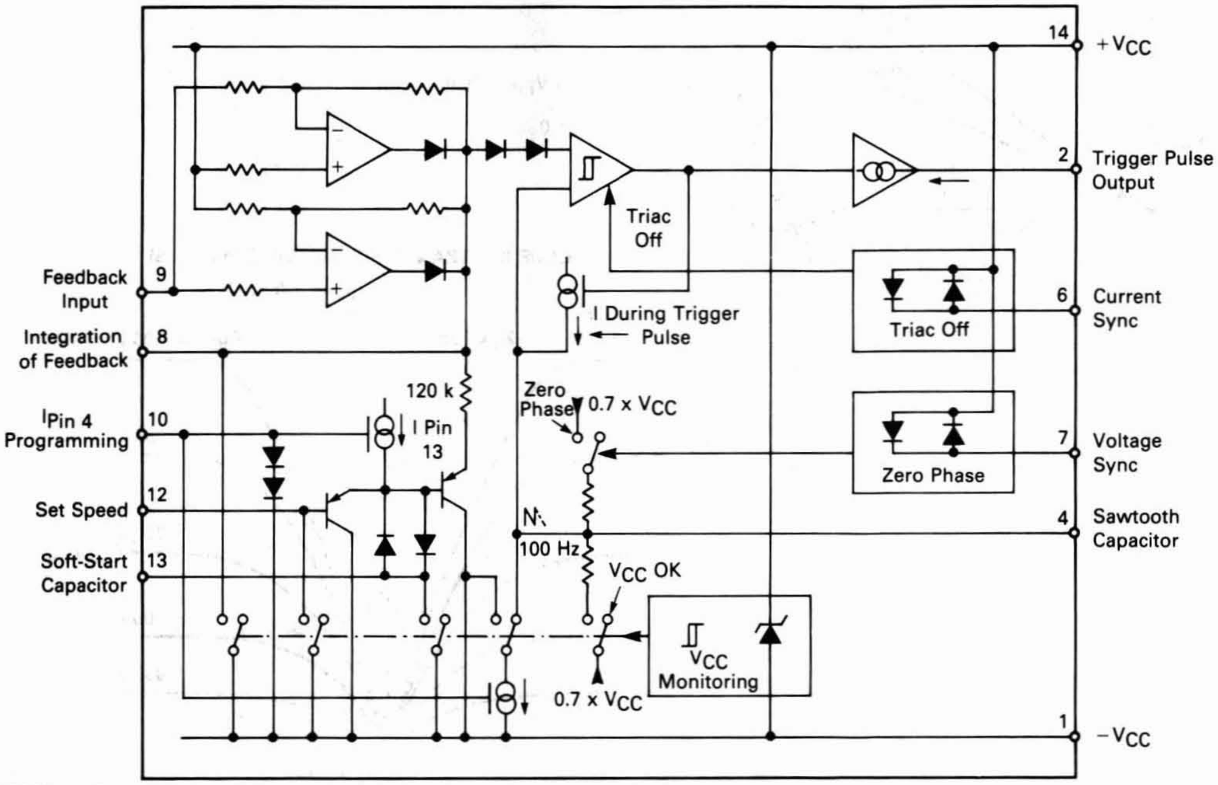
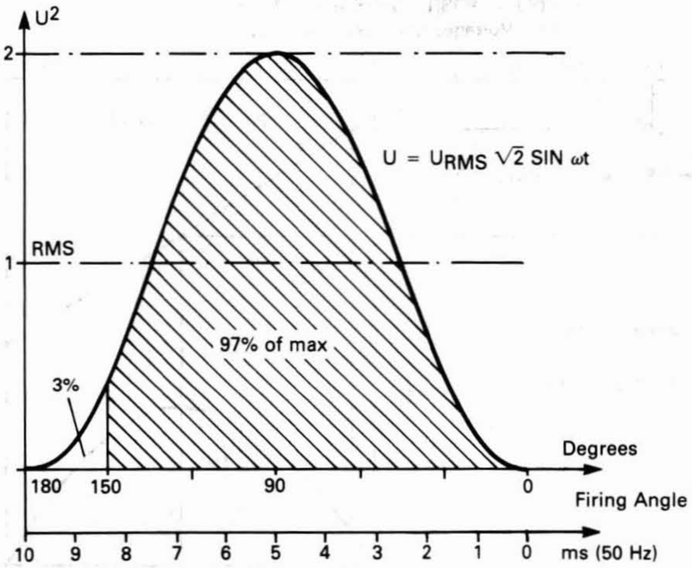

14
+VCC
2
Trigger Pulse Output
6
Current Sync
7
Voltage Sync
4
Sawtooth Capacitor
1
−VCC
Feedback Input
9
Integration of Feedback
8
IPin 4 Programming
10
Set Speed
12
Soft-Start Capacitor
13
Triac Off
I During Trigger Pulse
120 k
I Pin 13
Zero Phase
0.7 x VCC
Triac Off
Zero Phase
100 Hz
VCC OK
VCC Monitoring
0.7 x VCC

FIGURE 11 — EFFECTIVE POWER AS A FUNCTION OF FIRING ANGLE



**MOTOROLA**

# TDA1285A

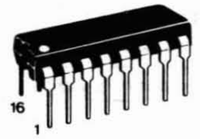
## MOTOR SPEED CONTROLLER

The TDA1285A has all the necessary functions for the speed control of universal motors in a closed loop configuration. Directly driven from the ac line, the circuits generate a phase angle varied trigger pulse to the control triac. In addition it provides the following features:

- Full Wave Triac Drive
- Repeated Trigger Pulse if Triac Fails to Latch
- Over 65 mA Output Pulse Current
- Automatic Adaptation to Inductive or Hall Effect Sensors
- Sensor Circuit Continuity Detection
- Motor Current Limitation
- Controlled Motor Starting Acceleration
- Typical 1–2% Motor Speed Variation Within All Temperature and Load Ranges

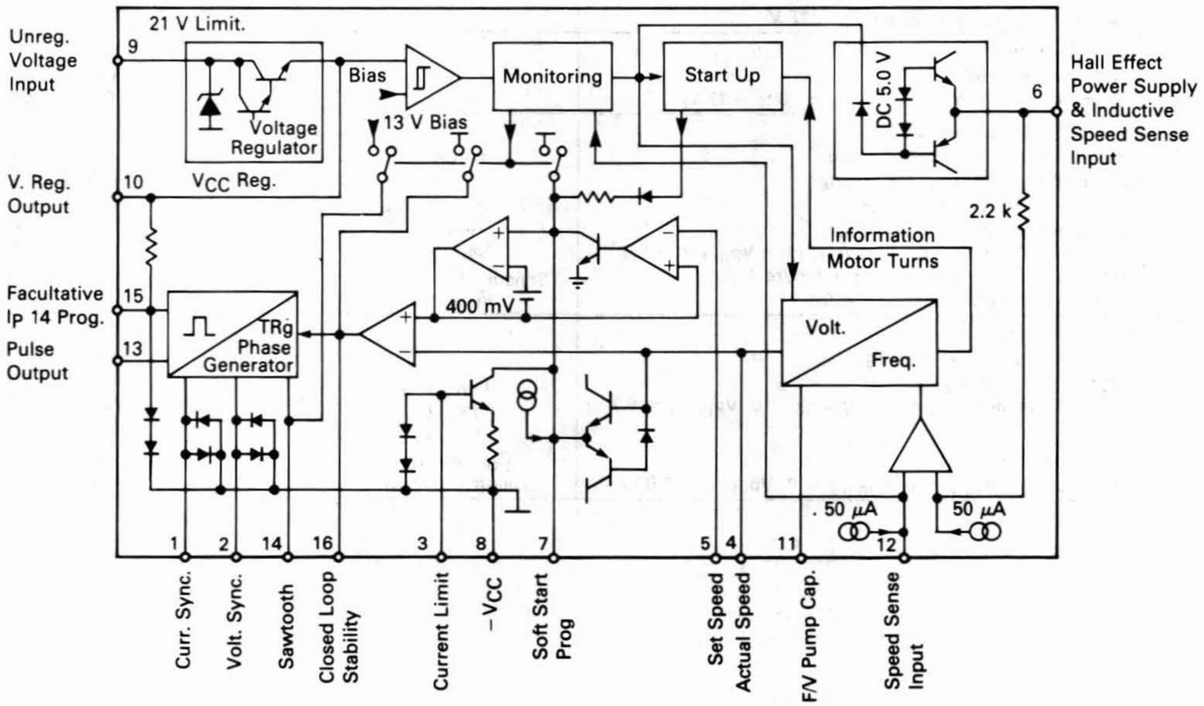
## UNIVERSAL MOTOR SPEED CONTROLLER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

**FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT**


Unreg. Voltage Input
9
21 V Limit.
Voltage Regulator
V. Reg. Output
10
VCC Reg.
Bias
13 V Bias
Monitoring
Start Up
DC 5.0 V
Hall Effect Power Supply & Inductive Speed Sense Input
6
2.2 k
Information Motor Turns
Facultative Ip 14 Prog.
15
Pulse Output
13
TRg Phase Generator
400 mV
Volt.
Freq.
50 μA
50 μA
1
2
14
16
3
8
7
5
4
11
12
Curr. Sync.
Volt. Sync.
Sawtooth
Closed Loop Stability
Current Limit
−VCC
Soft Start Prog
Set Speed
Actual Speed
F/V Pump Cap.
Speed Sense Input

## MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Current | $I_{Pin\ 9\ RMS}$ | 20 | mA |
| Peak Supply Current, t < 250 μs | $I_{Pin\ 9\ PEAK}$ | 200 | mA |
| Regulated Supply Current Drain | $I_{Pin\ 10}$ | 10 | mA |
| Peak ac Synchronization Input Currents | $I_{Pin\ 1}$<br>$I_{Pin\ 2}$ | ±2.0<br>±2.0 | mA<br>mA |
| Current Drain per Listed Pin | $I_3$ | −1.0<br>+2.0 | mA |
| | $I_{12}$ | +500<br>−4.0 | μA<br>mA |
| | $I_6$ | −7.0<br>+1.0 | mA |
| | $I_{15}$ | +1.0 | mA |
| Pin 3 Reverse Voltage | $V_{Pin\ 3}$ | −5.0 | V |
| Power Dissipation ($T_A$ = 25°C)<br>Derate above 25°C | $P_D$<br>$1/R_{\theta JA}$ | 625<br>6.8 | mW<br>mW/°C |
| Operating Temperature Range | $T_A$ | 0 to 70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +125 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Power Supply** | | | | | |
| Zener Regulated Voltage, $I_{Pin\ 9}$ = 20 mA | $V_{Pin\ 9}$ | 19 | 20.5 | 23 | V |
| Regulated Supply Voltage (Pin 10)<br>$I_{Pin\ 10}$ = 0; $I_{Pin\ 13}$ = 0; $I_{Pin\ 15}$ = 0<br>$I_{Pin\ 7}$ = 0; $V_{Pin\ 9}$ = 18 V | $V_{CC}$ | 13.6 | 14.6 | 15.6 | V |
| Current Consumption ($I_{Pin\ 9}$)<br>$I_{Pin\ 6}$ = 0; $I_{Pin\ 13}$ = 0; $I_{Pin\ 10}$ = 0<br>$I_{Pin\ 15}$ = 0; $I_{Pin\ 7}$ = 0; $V_{Pin\ 9}$ = 18 V | $I_{CC}$ | — | 4.5 | 7.0 | mA |
| **Speed Reference** | | | | | |
| Reference Input Voltage Range | $V_{Pin\ 5}$ | 0 | — | 12 | V |
| Reference Input Bias Current ($V_{Pin\ 5}$ : 0 to +12 V) | $I_{Pin\ 5}$ | −2.0 | — | 0 | μA |
| **Frequency to Voltage Converter** | | | | | |
| Inductive Sensor Application Range | $I_{Pin\ 6}$ | −2.5 | — | 0 | mA |
| Hall-Effect Sensor Application Range | $I_{Pin\ 6}$ | −8.0 | — | −3.5 | mA |
| Maximum Input Signal Voltage | $V_{Pin\ 12} - V_{Pin\ 6}$ | −5.0 | — | +5.0 | V |
| Common-Mode Reference Voltage | $V_{Pin\ 6}$ | — | 5.0 | — | V |
| Polarization Current ($-5.0\ V < V_{Pin\ 12} - V_{Pin\ 6} < +5.0\ V$) | $I_{Pin\ 12}$ | — | −50 | — | μA |
| Threshold Hysteresis Voltage (See Figure 4) | $(V_{Sensor} - V_{Pin\ 6})_{THRS}$ | — | ±60 | — | mV |
| Floating Input Voltage ($I_{Pin\ 12}$ = 0) | $V_{Pin\ 12}$ | 12 | — | — | V |
| **Main Comparator** | | | | | |
| Output Voltage Range ($I_{Pin\ 16}$ = 0) | $V_{Pin\ 16}$ | — | 0; +12 | — | V |
| Output Current Swing | $I_{Pin\ 16}$ | — | ±100 | — | μA |
| Transconductance ($I_{Pin\ 7}$ = 0; $I_{Pin\ 10}$ = 0; $V_{Pin\ 16}$ = 5.2 V) | $\frac{\Delta I_{Pin\ 16}}{\Delta V_{Pin\ 4}}$ | 140 | 205 | 265 | μA/V |
| Output Resistance | $R_{out\ Pin\ 16}$ | — | $10^6$ | — | Ω |
| Offset Voltage ($I_{Pin\ 7}$ = 0; $I_{Pin\ 16}$ = 0; $V_{Pin\ 16}$ = 5.0 V) | $V_{Pin\ 5} - V_{Pin\ 4}$ | −20 | 0 | +20 | mV |

**ELECTRICAL CHARACTERISTICS** (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Current Limitation | | | | | |
| Detection Level | $V_{Pin\ 3\ Min.}$ | — | 0.65 | — | V |
| Clamping Voltage Level | $V_{Pin\ 3\ CLAMP}$ | — | 1.3 | — | V |
| Output Discharge Current | $I_{DL7}$ | — | 0.5 | — | mA |
| Saturation Resistance | $R_{sat\ Pin\ 7}$ | — | 1.6 | — | kΩ |
| Start-up | | | | | |
| Maximum Start-up Voltage ($I_{Pin\ 7}$ = 0) | $V_{Pin\ 7}$ | — | 4.5 | — | V |
| Start-up Current (until motor turns) ($_{Pin\ 7}$ = 0) | $I_{Pin\ 7}$ | — | −1.0 | — | mA |
| Soft-Start | | — | | — | μA |
| Acceleration Charging Current | $I_{Pin\ 7}$ | | −8.0 | | |
| Trigger Pulse Generator | | | | | |
| Trigger Pulse Width* | tp | — | 100 | — | μs |
| Trigger Pulse Repetition Period* | t | — | 600 | — | μs |
| Output Pulse Current ($V_{Pin\ 13}$ = 1.0 V) | $I_{Pin\ 13}$ | −70 | — | −65 | mA |
| Output Leakage Current ($V_{Pin\ 13}$ = −2.0 V) | $I_{o\ Pin\ 13}$ | — | — | 10 | μA |
| Current Synchronization Threshold Levels (Pin 1 and Pin 2) | $I_{Thrs}$ | — | ±80 | — | μA |
| Sawtooth Current Generator | $I_{Pin\ 14}$ | — | −65 | — | μA |
| Pin 15 Voltage ($I_{Pin\ 15}$ = 0) | $V_{Pin\ 15}$ | — | 1.3 | — | Volt |

* These figures apply for the application shown in this data sheet.

## CIRCUIT DESCRIPTION

The TDA1285A generates trigger pulses for a triac controlling the power into an ac motor connected to mains. The firing angle of the triac is determined by comparison between a sawtooth signal (mains synchronized) and the main internal comparator signal. The latter is the difference between a set voltage (externally adjustable) representing the reference speed and the actual motor speed issued from an external sensor and converted by an internal frequency to voltage converter. This sensor may be inductive (tachometer) or Hall-effect. Other functions are also provided by the TDA1285A.

## KEY CIRCUIT FUNCTIONS

### DC POWER SUPPLY

DC Power is directly derived from the ac line by a low cost resistor-rectifier-capacitor circuit. The voltage on Pin 9 is Zener protected. The voltage on Pin 10 is fully regulated by a series ballast regulator, but is not self-limiting. Special provisions for Hall-effect sensor power are included.

### TACHOMETER INPUT (Pins 6 and 12)

The maximum allowable voltage swing is −5.0 to +5.0 V. Circuit continuity is permanently checked by the monitor.

### HALL-EFFECT INPUT (Pins 6 and 12)

When $I_{Pin\ 6}$ exceeds 3.0 mA, the circuit detects the use of a Hall-effect sensor and thus sensor circuit continuity is not checked (an open circuit would provide full triac conduction angle).

### FREQUENCY TO VOLTAGE CONVERTER

This circuit converts the tachometer input frequency into a proportional voltage on Pin 4 (eventually usable for any feedback). Particular care must be devoted to the conversion ratio of the F/V converter which is under the user control. In effect, it depends on the values of the $C_{11}$ capacitor and on tachometer frequency f(Hz).

$$V_{Pin\ 4} = 1.410 \times 10^{-10} \times C_{11}\,(\mathrm{pF}) \times R_4 \times F(\mathrm{Hz}) \times (1 \pm 0.15)$$

$V_{Pin\ 4}$ corresponding to maximum allowed motor speed must be chosen as close as possible to 12 V in order to minimize noise disturbance down to a negligible level.

### MAIN COMPARATOR

Its role is to amplify the signal error. Negative feedback from the output (Pin 16) to the input may be used to reduce the closed loop gain of the system and increase stability.

### SOFT START (Pin 7)

Set speed input (Pin 5) is overruled by similar data from Pin 7 as long as $V_{Pin\ 7}$ is smaller than $V_{Pin\ 5}$ + 400 mV (Typ). An internal 8.0 µA current source allows an external capacitor, $C_7$ to be charged slowly and thus lets the ac motor soft start (Figure 2). Pin 4 offset may be set appropriately by an external resistor ($R_1$ = 1 MΩ). Notice that $R_1$ may affect F/V conversion ratio. An external 10 nF capacitor on Pin 5 reduces noise sensitivity.

### START-UP CIRCUIT

From the moment power is applied to the circuit (or the circuit is enabled by Monitoring) to the moment a speed input signal is detected, $C_7$ is charged at a high current level (typically 1.0 mA). Detection of the first tachometer input resets the Pin 7 current to its nominal value (8.0 µA). The result of such a circuit is to start the acceleration ramp at the moment the motor starts to turn, avoiding any dead time (see Figure 2). When the motor is cycled on and off in close succession, the acceleration ramp is started immediately without waiting for the motor to stop.

### MOTOR CURRENT LIMITATION (Pin 3)

The motor current is sensed as a voltage developed across a resistor ($R_3$) in series with the triac. The limiter acts on positive peak values of $R_3$ x I filtered by a 22 k and 0.1 µF, RC network (Figure 7). The motor current is reduced, decreasing its speed reference by discharging $C_7$ until current limit equilibrium is reached (see Figure 3).

### TRIGGER PULSE GENERATOR

It delivers a 65 mA min. current pulse to the triac gate and repeats it if the triac fails to latch or if brush bounce has switched it off (Figure 6). Current and voltage detection through the triac are performed by Pins 1 and 2, delaying the trigger pulse until the triac current collapses. The pulse time is determined by the comparison of a sawtooth signal (available at Pin 14 and synchronous with line voltage) and the error signal directly supplied by the comparator.

Sawtooth slope is determined by the external capacitor $C_{14}$. Under these conditions pulse width is typically 100 µs (Figure 5).

### MONITORING

This is an internal function, disabling the circuit when

— $V_{CC}$ is insufficient

— Tachometer circuit is open and $I_{Pin\ 6} < |-3.0\ \mathrm{mA}|$

FIGURE 2 — START-UP AND SOFT-START CIRCUIT ACTIONS

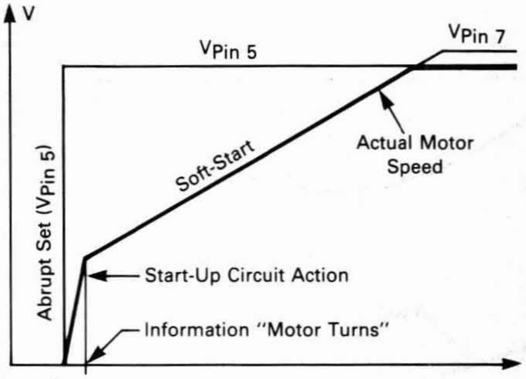


FIGURE 3 — CURRENT LIMITATION

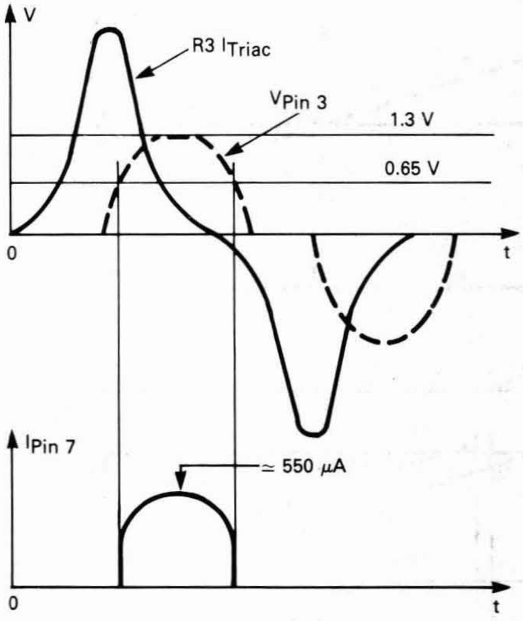
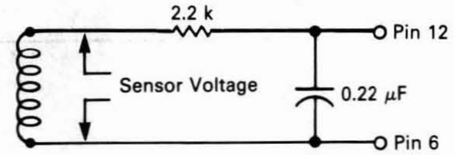


FIGURE 4 — SENSOR VOLTAGE DEFINITION


2.2 k
Pin 12
Sensor Voltage
0.22 μF
Pin 6

2.2 k is a recommended value to balance the voltage offset caused by sensor continuity detection circuit.

FIGURE 5 — FIRING PULSE GENERATION

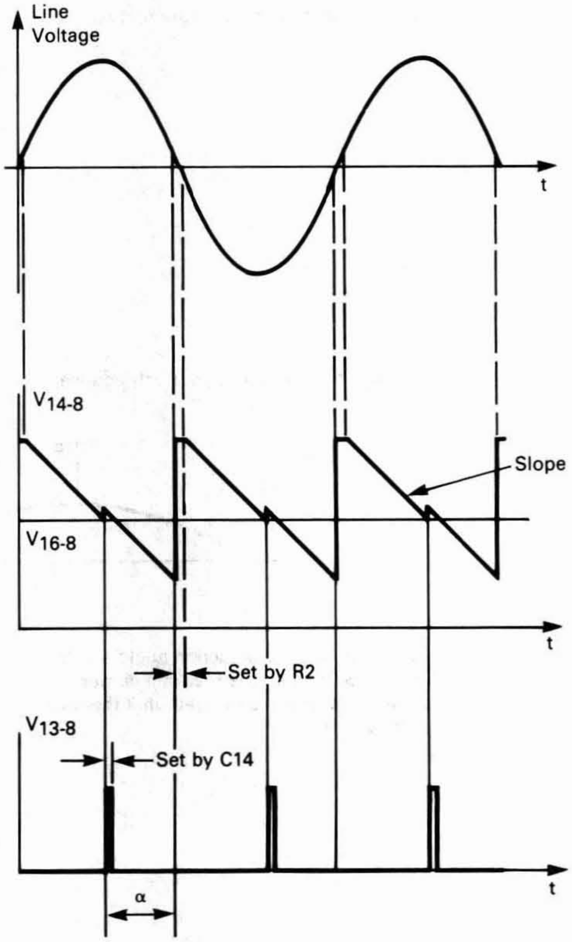
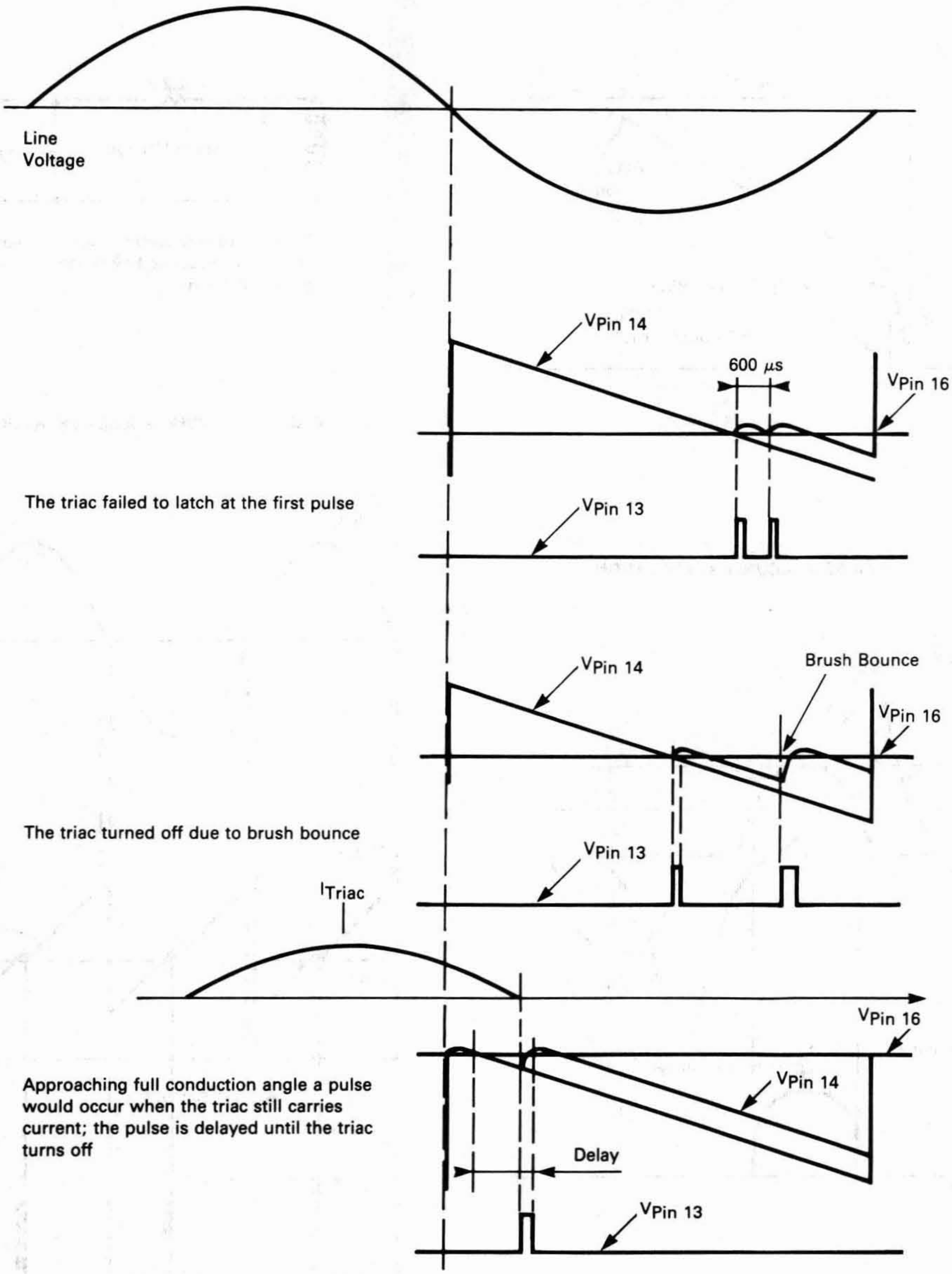


**FIGURE 6 — MULTIPLE FIRING PULSE AND FIRING PULSE DELAY**


Line
Voltage
$V_{Pin\ 14}$
600 μs
$V_{Pin\ 16}$
$V_{Pin\ 13}$
$V_{Pin\ 14}$
Brush Bounce
$V_{Pin\ 16}$
$V_{Pin\ 13}$
$I_{Triac}$
$V_{Pin\ 16}$
$V_{Pin\ 14}$
Delay
$V_{Pin\ 13}$

The triac failed to latch at the first pulse

The triac turned off due to brush bounce

Approaching full conduction angle a pulse would occur when the triac still carries current; the pulse is delayed until the triac turns off

## TYPICAL APPLICATION CIRCUITS

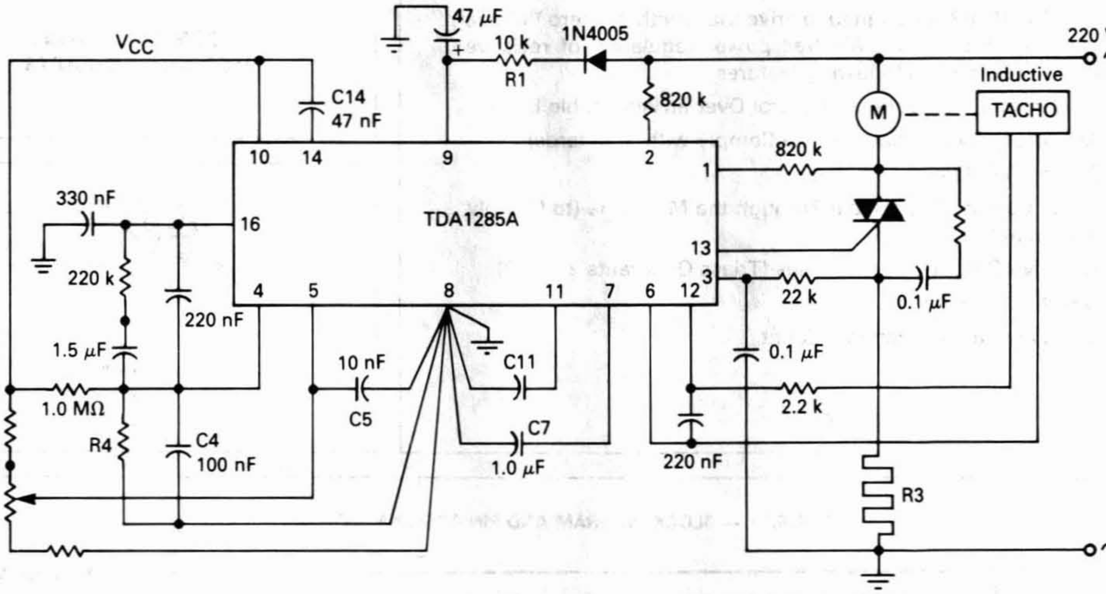
A motor control circuit using tachometer as speed sensor. It provides speed regulation as follows:

- ±1.0% from 20 to 70°C
- 1.0% in full load range.

It is strictly recommended to design the PC board in order to plug every connection to ground (Pin 8) directly and individually; otherwise, violent erratic currents may induce high level noise in the circuitry.

Motor will run full speed in case of tacho open circuit if a 47 k resistor is connncted permanently between Pins 6 and 12.

FIGURE 7 — MOTOR CONTROL CIRCUIT



47 µF
+
10 k
R1
1N4005
220 V
~
VCC
C14
47 nF
820 k
Inductive
TACHO
M
820 k
10
14
9
2
1
330 nF
16
TDA1285A
13
220 k
4
5
8
11
7
6
12
3
22 k
0.1 µF
220 nF
1.5 µF
10 nF
C11
0.1 µF
1.0 MΩ
C5
2.2 k
R4
C4
100 nF
C7
1.0 µF
220 nF
R3
~

**NOTES:**

Frequency to Voltage converter

— Max. motor speed 30,000 rpm

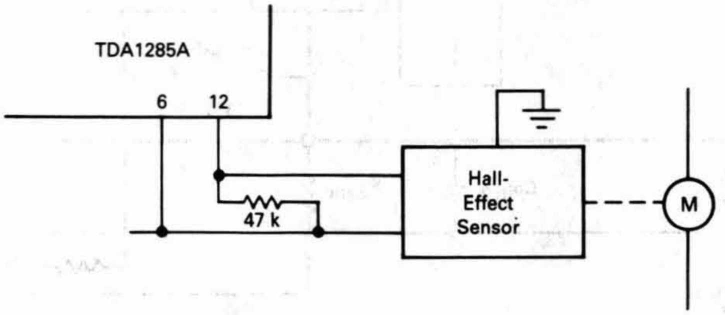
— Tachogenerator 4 pairs of poles: max. frequency $= \frac{30,000}{60} \times 4 = 2$ kHz

— C11 = 680 pF. R4 adjusted to obtain $V_{Pin\ 4} = 12$ V at max. speed: 68 kΩ

— Power Supply

with $V_{mains} = 120$ Vac, $R_1 = 4.7$ kΩ. Perfect operation will occur down to 80 Vac.

FIGURE 8 — CIRCUIT MODIFICATIONS TO CONNECT A HALL-EFFECT SENSOR



TDA1285A
6
12
47 k
Hall-Effect Sensor
M

**MOTOROLA**

# UAA1016B

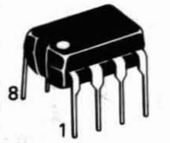
## ZERO VOLTAGE CONTROLLER

The UAA1016B is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. It provides the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail-Safe
- No dc Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triacs Quadrants 2 and 3)
- Direct ac Line Operation
- Low External Components Count

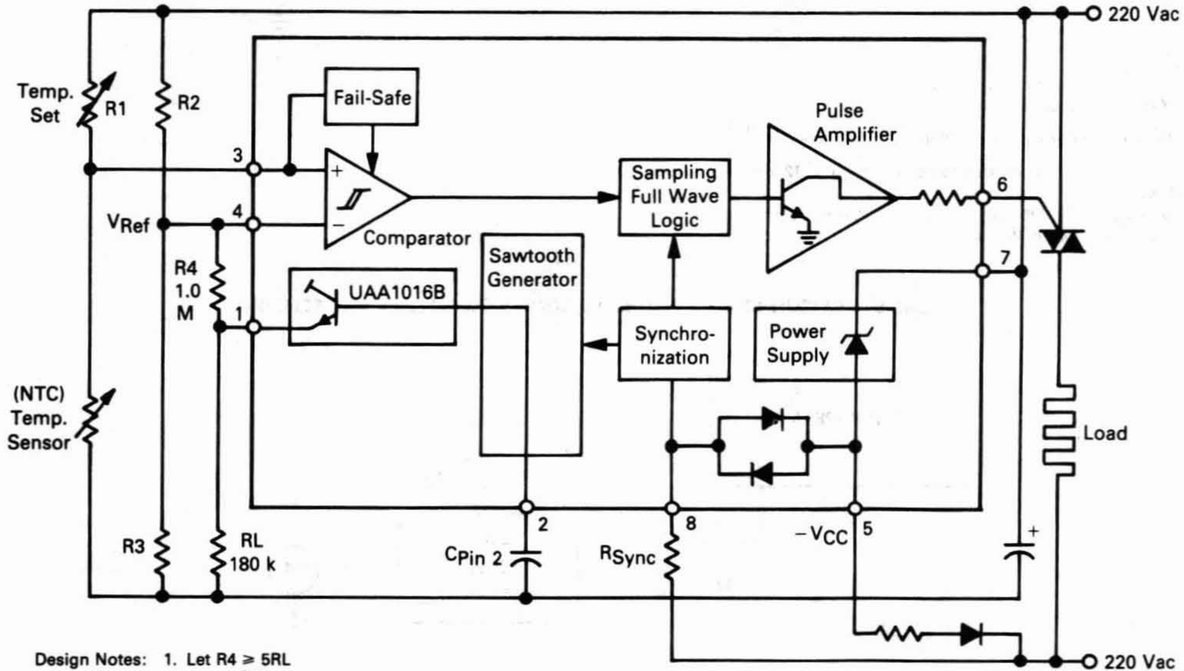
## ZERO VOLTAGE SWITCH PROPORTIONAL BAND TEMPERATURE CONTROLLER

### SILICON MONOLITHIC INTEGRATED CIRCUITS



**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04

**FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT**



220 Vac
Temp. Set
R1
R2
Fail-Safe
Pulse Amplifier
3
Sampling Full Wave Logic
6
VRef
4
Comparator
R4 1.0 M
Sawtooth Generator
7
UAA1016B
1
Synchro-nization
Power Supply
(NTC) Temp. Sensor
Load
2
8
−VCC
5
R3
RL 180 k
CPin 2
RSync
220 Vac

**Design Notes:** 1. Let R4 ≥ 5RL

2. Select $\frac{R2}{R3}$ Ratio for a symmetrical reference deviation centered about Pin 1 output swing, R2 will be slightly greater than R3.

3. Select R2 and R3 values for the desired reference deviation where $\Delta V_{REF} = \frac{\Delta V_{Pin\ 1}}{\frac{R4}{R2 \,||\, R3} + 1}$

**MAXIMUM RATINGS** (Voltages referred to Pin 7)

| Parameter | Symbol | Max. Rating | Unit |
|---|---|---|---|
| Supply Current ($I_{Pin\ 5}$) | $I_{CC}$ | 15 | mA |
| Nonrepetitive Supply Current ($I_{Pin\ 5}$) | $I_{CCP}$ | 200 | mA |
| AC Synchronization Current (Pin 8) | $I_{syn}$ | 3.0 | mA (RMS) |
| Maximum Pin Voltages | $V_{Pin\ 1}$<br>$V_{Pin\ 2}$<br>$V_{Pin\ 3}$<br>$V_{Pin\ 4}$<br>$V_{Pin\ 6}$ | 0; $-V_{CC}$<br>0; $-V_{CC}$<br>0; $-V_{CC}$<br>0; $-V_{CC}$<br>+2.0; $-V_{CC}$ | Volt |
| Maximum Current Drain | $I_{Pin\ 1}$ | 1.0 | mA |
| Power Dissipation<br>$T_A$ = 25°C | $P_D$ | 625 | mW |
| Maximum Thermal Resistance | $R_{\theta JA}$ | 100 | °C/W |
| Operating Temperature Range | $T_A$ | −20 to +100 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, Voltages referred to Pin 7 unless otherwise noted)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Current Consumption (Pins 6 and 8 not connected) | $I_{CC}$ | — | 0.8 | 1.5 | mA |
| Stabilized Supply Voltage ($V_{Pin\ 5}$)<br>$I_{CC}$ = 2.0 mA max | $-V_{CC}$ | −9.6 | −8.6 | −7.6 | V |
| Output Pulse Current ($V_{Pin\ 6}$ from −1.0 to +1.0 Volt) | $I_{out}$ | 60 | 90 | 120 | mA |
| Output Pulse Width<br>$R_{Pin\ 8}$ = 220 kΩ, $V_{mains}$ = 220 Vac/50 Hz, (Figures 4 and 5) | $t_{p1}$<br>$t_{p2}$ | 58<br>160 | 60<br>220 | 120<br>320 | μs |
| Comparator Input Offset Voltage ($V_{Pin\ 3} - V_{Pin\ 4}$) | $V_{off}$ | −10 | — | +10 | mV |
| Comparator Common Mode Voltage Range | $V_{CM}$ | $-V_{CC}+1$ | — | −1.5 | V |
| Input Bias Current (Pins 3 and 4) | $I_{IB}$ | — | — | 1.0 | μA |
| Output Leakage Current ($I_{Pin\ 6}$)<br>$V_{Pin\ 6}$ = +2.0 V | $I_{outL}$ | — | — | 10 | μA |
| Fail-safe Threshold Voltage ($V_{Pin\ 3}$) | $V_{FSTH}$ | — | −0.7 | — | V |
| Capacitor Charging Current (Source) | $I_{Pin\ 2}$ | −20 | −16 | −12 | μA |
| Capacitor Discharge Current (Sink) | $I'_{Pin\ 2}$ | — | 6.4 | — | mA |
| Sawtooth Pulse Length ($C_{Pin\ 2}$ = 1.0 μF) | $t_{saw}$ | — | 0.85 | — | S |
| Output Threshold Sawtooth Levels ($V_{Pin\ 2}$) | $V_{TH1}$<br>$V_{TH2}$ | —<br>— | −1.0<br>$-V_{CC}+1.25$ | —<br>— | V |
| Output Voltage Pin 1 | $V_{Pin\ 1}$ | — | $V_{Pin\ 2}-0.75$ | — | V |

## CIRCUIT DESCRIPTION

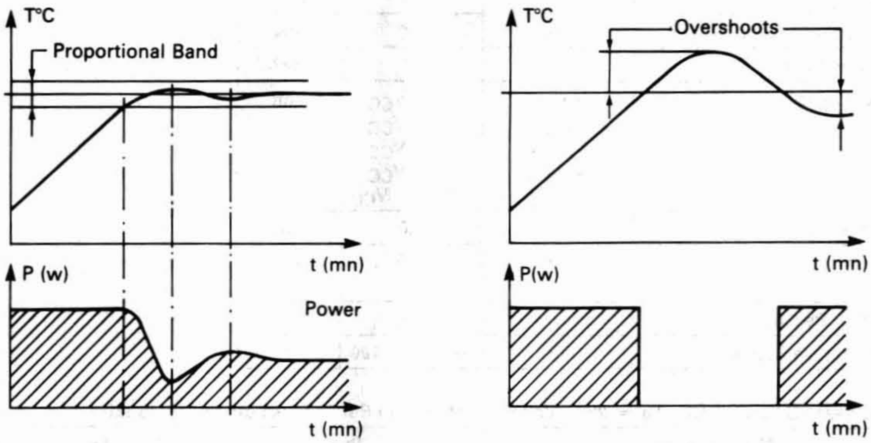
The circuit delivers current pulses to the triac at zero crossings of the main line sensed by Pin 8 through $R_{sync}$. An internal full wave logic allows the triac to latch during full wave periods in order to avoid any dc component in the main line, in compliance with European regulations. Trigger pulses are generated when the comparator detects $V_{Pin\ 3}$ is above $V_{Pin\ 4}$ (or $V_{reference}$) as sensed temperature through the NTC is then lower than the set value ($V_{REF}$ corresponding to the external Wheatstone bridge equilibrium).

In order to comply with norms limiting the frequency at which a kW sized load, or above, may be connected to the main line (fluorescent tubes "flickering"), the UAA1016B has an internal time base providing (power is delivered by bursts to the load) a proportional temperature band control. In fact, most of the heating regulation systems require low temperature overshoot for more precision and stability which cannot be accomplished by direct on/off regulation (see Figure 2). An internal low frequency sawtooth generator whose output is available at Pin 1, allows the designer to introduce a periodic linear change of $V_{Ref}$. This deviation defines the temperature band allowing proportional power control (see Figure 3).

A fail-safe circuit inhibits output pulses when the sensor circuit has a fault (open or short circuit).

The IC is directly powered from the mains by a dropping resistor, a diode and a filter capacitor.

FIGURE 2 — PROPORTIONAL TEMPERATURE CONTROL versus ON/OFF CONTROL



PROPORTIONAL TEMPERATURE CONTROL

Reduced Overshoot

Stability

ON/OFF CONTROL

Large Overshoot

Marginal Stability

## KEY CIRCUIT FUNCTIONS DESCRIPTION

**POWER SUPPLY** — The rectified supply current is Zener regulated to 8.6 V. Current consumption of the UAA1016B is typically less than 1.0 mA. The major part of the current fed by the dropping resistor is used for the sensor bridge and triac gate pulses. Any excess of supply current is excess power dissipation into the integrated Zener. Current consumption of the triac pulses may be derived from Figure 4 and 5 (Igt max. and pulse duration). Usually an 18 kΩ, 2.0 W dropping resistor is convenient to feed the UAA1016.

**COMPARATOR** — When $V_{Pin\ 3}$ is higher than $V_{Pin\ 4}$ ($V_{Ref}$), the comparator allows the triggering logic to deliver pulses to the triac (Figure 3). The offset hysteresis input voltage has been designed to be as low as possible (±10 mV max) in order to minimize the uncontrollable temperature band (proportional to the hysteresis) as per Figure 6. Noise rejection is performed by a synchronous sampling of the comparator output during very short times (typ. less than 100 ns).

**SAWTOOTH GENERATOR** — A sawtooth voltage signal is generated by a constant current source (typ. 7.5 μA), charging an external capacitor $C_{Pin\ 2}$ between two threshold levels, $V_{TH1}$ and $V_{TH2}$, which are respectively:

$V_{TH1} = -1.0$ V

$V_{TH2} = -V_{CC} + 1.25$ V.

Charging and discharging currents occur only with negative halfcycles of the line.

In the UAA1016B, the sawtooth signal is available at Pin 1 as a voltage source $V_{Pin\ 1} = V_{Pin\ 2} - 0.75$ V. Maximum source current is 1.0 mA, but to keep good linearity of sawtooth signal, a source current of 40 μA is recommended (see Figure 7).

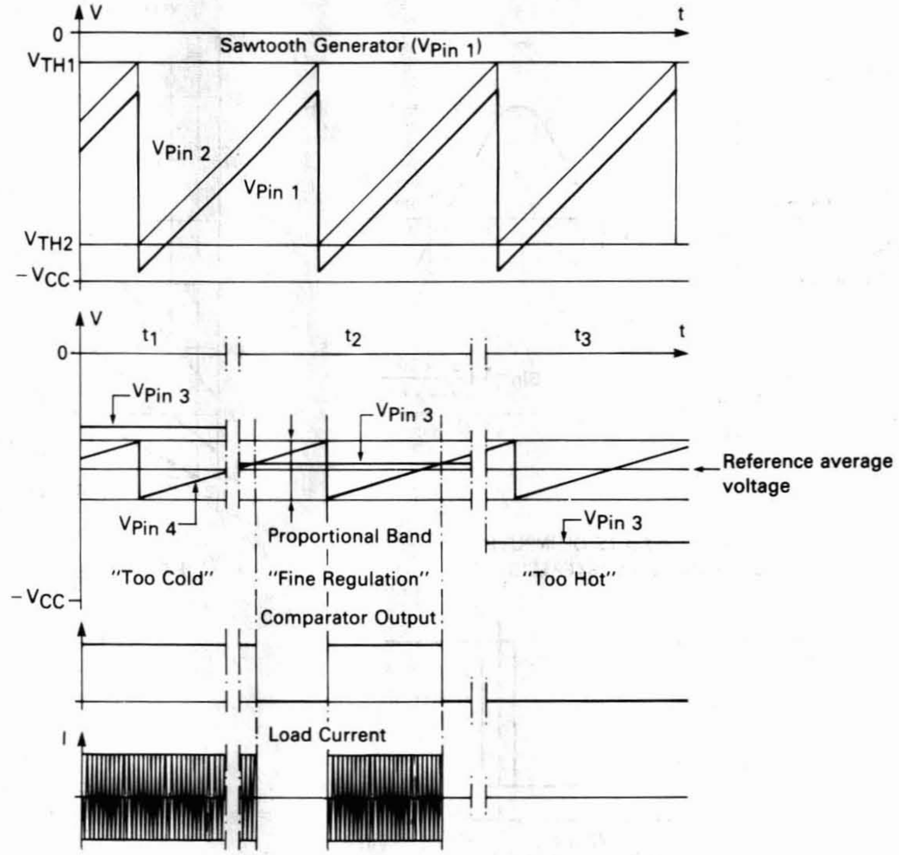
**FAIL-SAFE** — Output pulses are inhibited by the "fail-safe" circuit if the comparator input voltage exceeds the specified threshold voltage. This would occur if the temperature sensor circuit had a fault.

**SAMPLING FULL WAVE LOGIC** — Two consecutive zero-crossing trigger pulses are generated at every positive mains half-cycle of the line to minimize generation of noise (as per Figure 8). Within every zero-crossing the pulses are positioned as per Figure 4. Pulse length is also adjustable by $R_{sync}$ on Pin 8 to allow positive triggering of the triac at this critical moment (firing with low voltage between main terminals requires long pulses).

**PULSE AMPLIFIER** — The pulse amplifier circuit delivers minimum current pulses of 60 mA (sink). The triac is triggered in quadrants II and III.

**SYNCHRONIZATION CIRCUIT** — This circuit detects mains zero-crossings through $R_{sync}$ and the value selected determines the trigger pulse length. A zero crossing current detector is employed with typical thresholds of ∓27 μA to ±98 μA (see Figures 4 and 5).

FIGURE 3 — SAWTOOTH GENERATOR AND PROPORTIONAL BAND


V
t
0
Sawtooth Generator ($V_{Pin\ 1}$)
$V_{TH1}$
$V_{Pin\ 2}$
$V_{Pin\ 1}$
$V_{TH2}$
$-V_{CC}$
V
$t_1$
$t_2$
$t_3$
t
0
$V_{Pin\ 3}$
$V_{Pin\ 3}$
Reference average voltage
$V_{Pin\ 4}$
Proportional Band
$V_{Pin\ 3}$
"Too Cold"
"Fine Regulation"
"Too Hot"
$-V_{CC}$
Comparator Output
I
Load Current

COMMENTS TO FIGURE 3

Referring to Figure 1, the average value of $V_{Ref}$ is set by $R_2$ and $R_3$. $R_4$ defines the amplitude of the sawtooth signal superimposed on $V_{Ref}$, defining the Proportional Band.

Figure 3 shows three conditions:

1) During time $t_1$ we always have $V_{Pin\ 3} > V_{Ref}$, and as a result, the comparator is always "on" and the triac fired (100% max. power)
2) During time $t_2$, $V_{Pin\ 3}$ is in the proportional band, and the average power delivered to the load is a fraction of maximum power.
3) During time $t_3$, $V_{Pin\ 3} < V_{Ref}$, and the triac is always "off."

When the sensor temperature is above the set value and is slowly decreasing as no heating occurs, $V_{Pin\ 3} - V_{Pin\ 4}$ must exceed half the hysteresis value before power is applied again (1). A similar effect occurs in the opposite direction when temperature sensor is below the set value and can remain stable as position (2). This defines the "uncontrollable temperature band" which will be very small if hysteresis is also very small.

## SUGGESTIONS FOR USE

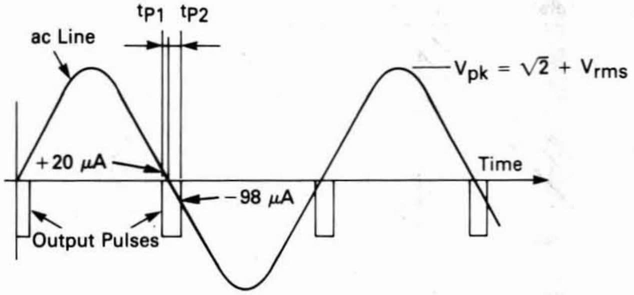
The temperature sensor circuit is a Wheatstone bridge including the sensor element. Comparator inputs may be free from power line noise only if the sensor element is purely resistive (NTC resistor). Usage of any P-N junction sensor would drastically reduce noise rejection.

Fixed phase sensing of the internal comparator output eliminates parasitic signals.

Some loads, even designed to be resistive, have in fact a slight inductive component. A phase shift at Pin 8 can be achieved with external capacitor $C_3$ connected to Pin 8 network (see Figure 9).

Suggested maximum source current at Pin 1 is 40 $\mu$A, in order to have acceptable sawtooth signal linearity.

**FIGURE 4 — OUTPUT PULSE WIDTH DEFINITIONS**


tP1 tP2
ac Line
Vpk = √2 + Vrms
+20 μA
Time
−98 μA
Output Pulses

$$t_{P1} = \frac{\sin^{-1}\left(\frac{27 \times 10^{-6}}{V_{rms} + \sqrt{2}}\right)}{360 f_{ac}} \qquad t_{P2} = \frac{\sin^{-1}\left(\frac{98 \times 10^{-6}}{V_{rms} + \sqrt{2}}\right)}{360 f_{ac}}$$

**FIGURE 5 — TYPICAL OUTPUT PULSE LENGTH versus SYNCHRONIZATION RESISTOR**

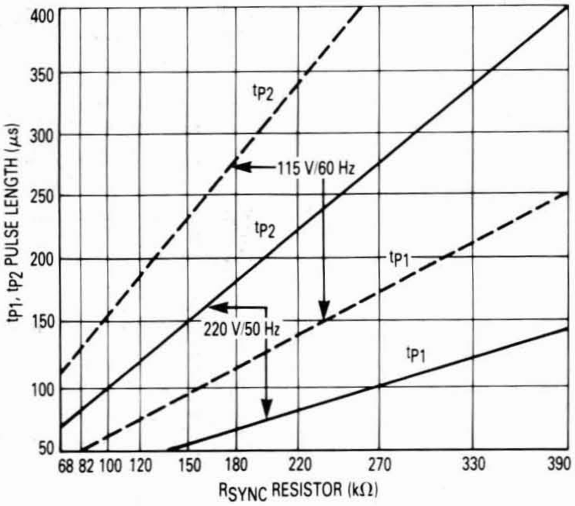


**FIGURE 6 — EFFECTS OF INPUTS COMPARATOR HYSTERESIS**

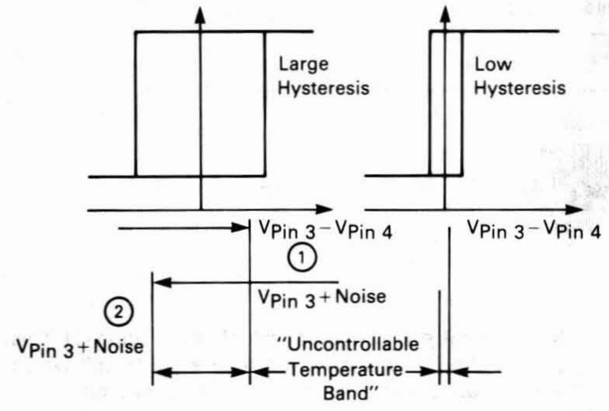

Large Hysteresis
Low Hysteresis
VPin 3 − VPin 4
VPin 3 − VPin 4
①
VPin 3 + Noise
②
VPin 3 + Noise
"Uncontrollable Temperature Band"

**FIGURE 7 — PIN 1 INTERNAL NETWORK**

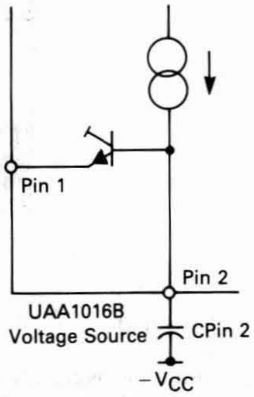
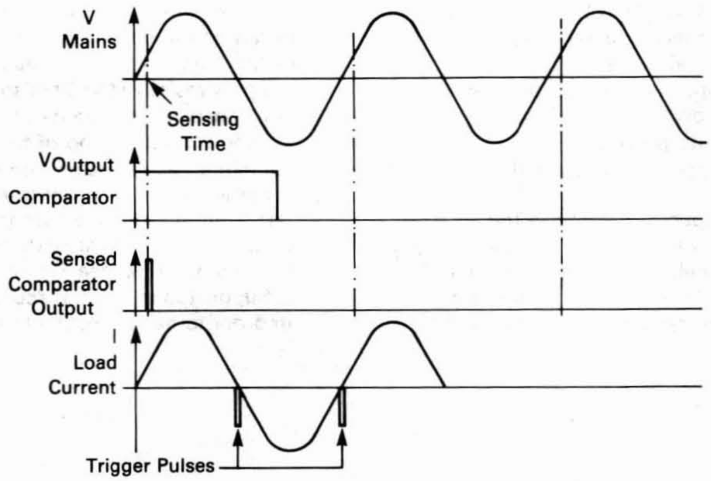

Pin 1
Pin 2
UAA1016B Voltage Source
CPin 2
−VCC

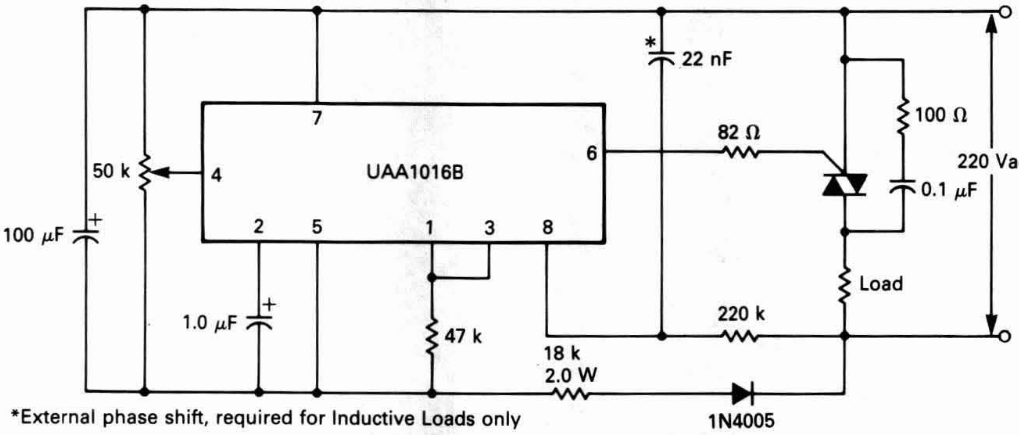
**FIGURE 8 — TRIGGER PULSE GENERATION**


V Mains
Sensing Time
VOutput Comparator
Sensed Comparator Output
I Load Current
Trigger Pulses

## APPLICATION CIRCUITS

Figure 9 shows a very simple application of the UAA1016B as an electronic rheostat having 100% efficiency. $C_3$ is required only if load has an inductive component. Figure 10 shows a typical application as a panel heater thermostat with a proportional temperature band of 1°C at 25°C.

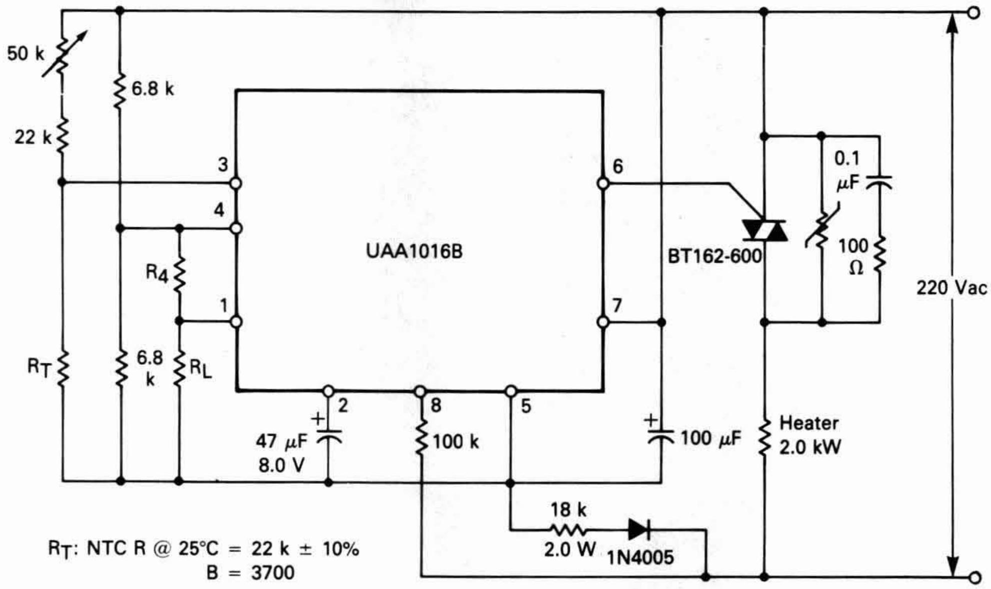
FIGURE 9 — APPLICATION CIRCUIT — ELECTRONIC RHEOSTAT



*
22 nF
7
UAA1016B
6
82 Ω
100 Ω
220 Vac
0.1 μF
50 k
4
100 μF
2
5
1
3
8
Load
1.0 μF
47 k
220 k
18 k
2.0 W
1N4005

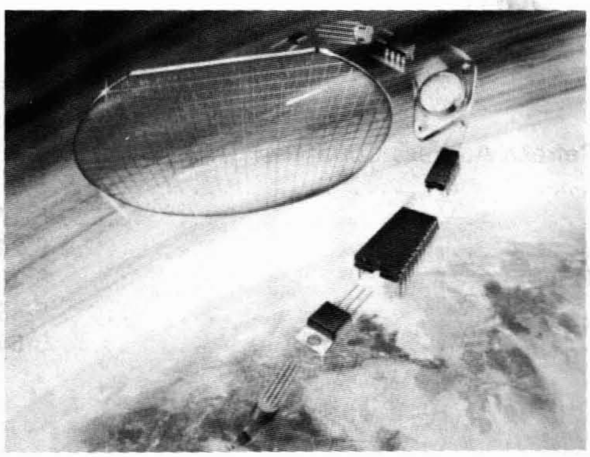
*External phase shift, required for Inductive Loads only

FIGURE 10 — APPLICATION CIRCUIT — ELECTRIC RADIATOR WITH PROPORTIONAL BAND THERMOSTAT, PROPORTIONAL BAND 1°C AT 25°C



50 k
6.8 k
22 k
3
4
1
6
7
UAA1016B
0.1 μF
BT162-600
100 Ω
220 Vac
R4
RT
6.8 k
RL
2
8
5
47 μF
8.0 V
100 k
100 μF
Heater
2.0 kW
18 k
2.0 W
1N4005

$R_T$: NTC R @ 25°C = 22 k ± 10%
B = 3700



# Interface Circuits

Memory Interface and Control
Bus Interface
Line Drivers and Receivers

# INTERFACE CIRCUITS

## Memory Interface and Control

| **Device** | **Function** | **Page** |
|---|---|---|
| MC3242A | Memory Address Multiplexer and Refresh Address Counter | 5-4 |
| MC3467 | Triple Preamplifier | 5-9 |
| MC3469P | Floppy Disk Write Controller | 5-14 |
| MC3470,A | Floppy Disk Read Amplifier System | 5-24 |
| MC3471P | Floppy Disk Write Controller/Head Driver | 5-38 |
| MC3480 | Memory Controller Circuit | 5-49 |
| TCF6000 | Peripheral Clamping Array | 5-64 |

## Bus Interface

| **Device** | **Function** | **Page** |
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| MC8T96 | Hex Three-State Buffer/Inverter | 5-68 |
| MC8T97 | Hex Three-State Buffer/Inverter | 5-68 |
| MC8T98 | Hex Three-State Buffer/Inverter | 5-68 |
| MC6875,A | MC6800 Clock Generator/Driver | 5-72 |
| MC6885 | Hex Three-State Buffer/Inverter | 5-68 |
| MC6886 | Hex Three-State Buffer/Inverter | 5-68 |
| MC6887 | Hex Three-State Buffer/Inverter | 5-68 |
| MC6888 | Hex Three-State Buffer/Inverter | 5-68 |

## Line Drivers and Receivers

| **Device** | **Function** | **Page** |
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| AM26LS32 | Quad RS-422/3 Line Receiver with Three-State Outputs | 5-86 |
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| MC8T28 | Noninverting Bus Transceiver | 5-94 |
| MC26S10 | Quad Open-Collector Bus Transceiver | 5-99 |
| MC75S110 | Dual Line Driver | 5-102 |
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| MC1412 | Peripheral Driver Array | 5-107 |
| MC1413 | Peripheral Driver Array | 5-107 |

## Line Drivers and Receivers (con't)

| Device | Function | Page |
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| MC1488 | Quad MDTL Line Driver | 5-114 |
| MC1489,A | Quad MDTL Line Receiver | 5-120 |
| MC3437 | Hex Unified Bus Receiver | 5-125 |
| MC3440A | Quad Interface Bus Transceiver | 5-128 |
| MC3441A | Quad Interface Bus Transceiver | 5-128 |
| MC3446A | Quad Interface Bus Transceiver | 5-132 |
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| MC3485 | Quad Single-Ended Line Driver | 5-157 |
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| MC6889 | Noninverting Bus Transceiver | 5-94 |
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| MC75108 | Dual Line Receiver | 5-173 |
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| MC75129 | Eight-Channel Line Receivers | 5-182 |
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| SN75174 | Quad RS-485 Line Driver with Three-State Output | 5-186 |
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| ULN2074B | Quad 1.5 A Darlington Switch | 5-197 |
| ULN2801 | Octal Peripheral Driver Array | 5-201 |
| ULN2802 | Octal Peripheral Driver Array | 5-201 |
| ULN2803 | Octal Peripheral Driver Array | 5-201 |
| ULN2804 | Octal Peripheral Driver Array | 5-201 |

**MOTOROLA**

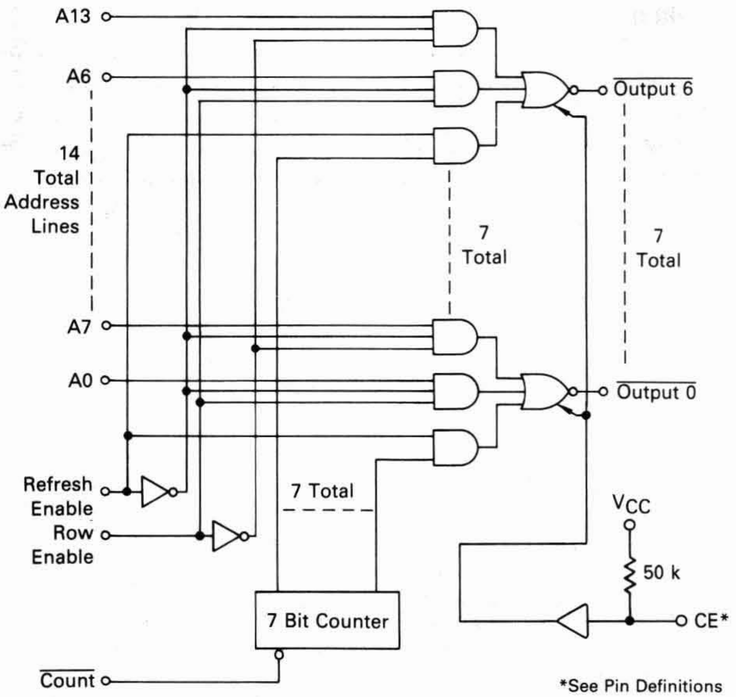
# MC3242A

## MEMORY ADDRESS MULTIPLEXER FOR 16K RAMs

The MC3242A is an address multiplexer/refresh counter for 16-pin 16K dynamic RAMs that require a 128-cycle refresh and multiplexes fourteen system address bits to the seven address pins of the memory device. It also contains a 7-bit refresh counter that is clocked externally to generate the 128 sequential addresses required for refresh. The high performance of the MC3242A will enhance the high speed of the N-channel RAMs such as the MCM4116.

- Simplifies 16-Pin 16K Dynamic Memory Design
- Reduces Package Count
- 7-Bit Binary Counter for 128 Refresh Address
- Multiplexing: Row Address/Column Address/Refresh Address
- High Input Impedance for Minimum Loading of Bus: $I_F = 0.25$ mA Max
- Schottky TTL for High Performance Address Input to Output Delay — $t_{AO} = 25$ ns @ $C_L = 250$ pF
- Second Source to Intel 3242 (Detect Zero Function Not Included and Additional Chip Enable Feature Added at Pin 15)

### LOGIC DIAGRAM

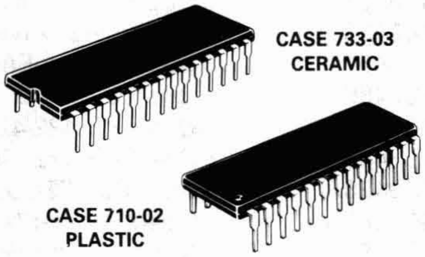


A13
A6
14 Total Address Lines
A7
A0
Refresh Enable
Row Enable
$\overline{\text{Count}}$
7 Bit Counter
7 Total
7 Total
7 Total
$\overline{\text{Output 6}}$
$\overline{\text{Output 0}}$
$V_{CC}$
50 k
CE*

*See Pin Definitions

## MEMORY ADDRESS MULTIPLEXER AND REFRESH ADDRESS COUNTER

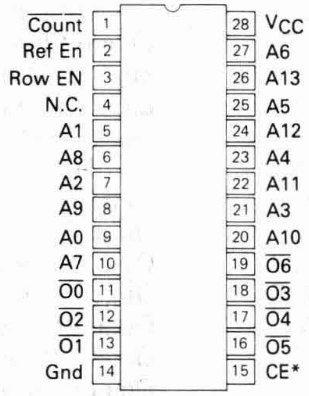
**SCHOTTKY SILICON MONOLITHIC INTEGRATED CIRCUITS**



CASE 733-03 CERAMIC

CASE 710-02 PLASTIC

### PIN ASSIGNMENT



$\overline{\text{Count}}$ 1
Ref En 2
Row EN 3
N.C. 4
A1 5
A8 6
A2 7
A9 8
A0 9
A7 10
$\overline{\text{O0}}$ 11
$\overline{\text{O2}}$ 12
$\overline{\text{O1}}$ 13
Gnd 14
28 $V_{CC}$
27 A6
26 A13
25 A5
24 A12
23 A4
22 A11
21 A3
20 A10
19 $\overline{\text{O6}}$
18 $\overline{\text{O3}}$
17 $\overline{\text{O4}}$
16 $\overline{\text{O5}}$
15 CE*

Note: A0 Through A6 Are Row Addresses
A7 Through A13 Are Column Addresses
*See Pin Definitions

### TRUTH TABLE AND DEFINITIONS

| Refresh Enable | Row Enable | Output |
|---|---|---|
| H | X | Refresh Address (From Internal Counter) |
| L | H | Row Address (A0 through A6) |
| L | L | Column Address (A7 through A13) |

$\overline{\text{Count}}$ — Advances Internal Refresh Counter

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC3242AL | 0 to +75°C | Ceramic DIP |
| MC3242AP | 0 to +75°C | Plastic DIP |

**ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | −0.5 to +7.0 | V |
| Input Voltage | $V_I$ | −0.5 to +7.0 | V |
| Output Voltage | $V_O$ | −0.5 to +7.0 | V |
| Output Current | $I_O$ | 100 | mA |
| Operating Ambient Temperature | $T_A$ | 0 to +75 | °C |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature<br>Ceramic Package<br>Plastic Package | $T_J$ | <br>+175<br>+150 | °C |

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

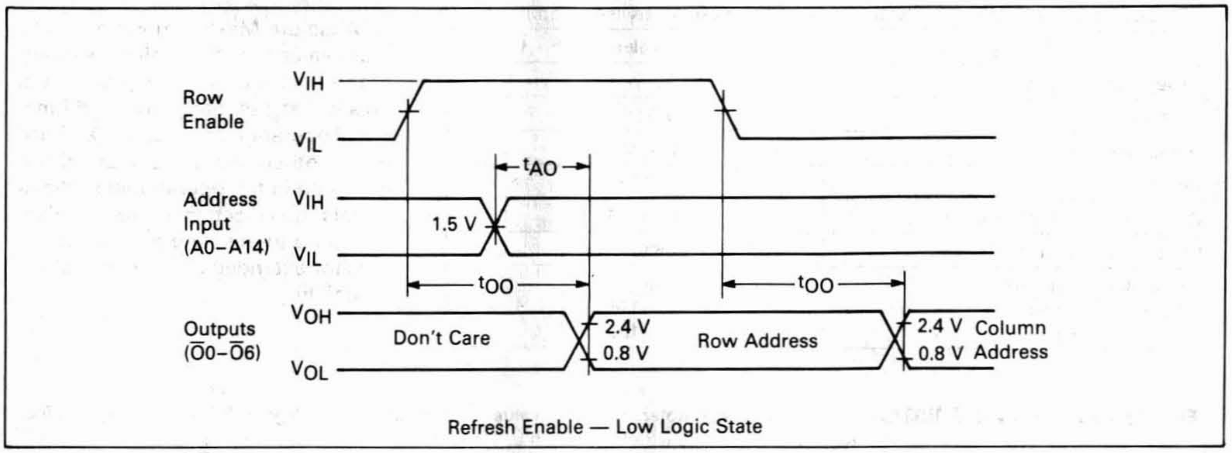
**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ $V_{CC}$ ≤ 5.5 V, 0°C ≤ $T_A$ ≤ 75°C; typical values apply with $V_{CC}$ = 5.0 V, $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Current, Low Logic State<br>($V_{IL}$ = 0.45 V) | $I_{IL}$ | — | −0.25 | −0.4 | mA |
| Input Current, High Logic State<br>($V_{IH}$ = 5.5 V) | $I_{IH}$ | — | — | 10 | μA |
| Input Voltage, Low Logic State | $V_{IL}$ | — | — | 0.8 | V |
| Input Voltage, High Logic State | $V_{IH}$ | 2.0 | — | — | V |
| Output Voltage, Low Logic State<br>($I_{OL}$ = 5.0 mA) | $V_{OL}$ | — | 0.25 | 0.4 | V |
| Output Voltage, High Logic State<br>($I_{OH}$ = −1.0 mA) | $V_{OH}$ | 3.0 | 4.0 | — | V |
| Input Clamp Voltage<br>($I_{IK}$ = −12 mA) | $V_{IK}$ | — | −0.8 | −1.5 | V |
| Power Supply Current<br>($V_{CC}$ = 5.5 V) | $I_{CC}$ | — | 80 | 125 | mA |

**SWITCHING CHARACTERISTICS** (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ $V_{CC}$ ≤ 5.5 V, 0°C ≤ $T_A$ ≤ 75°C; typical values apply with $V_{CC}$ = 5.0 V, $T_A$ = 25°C.)

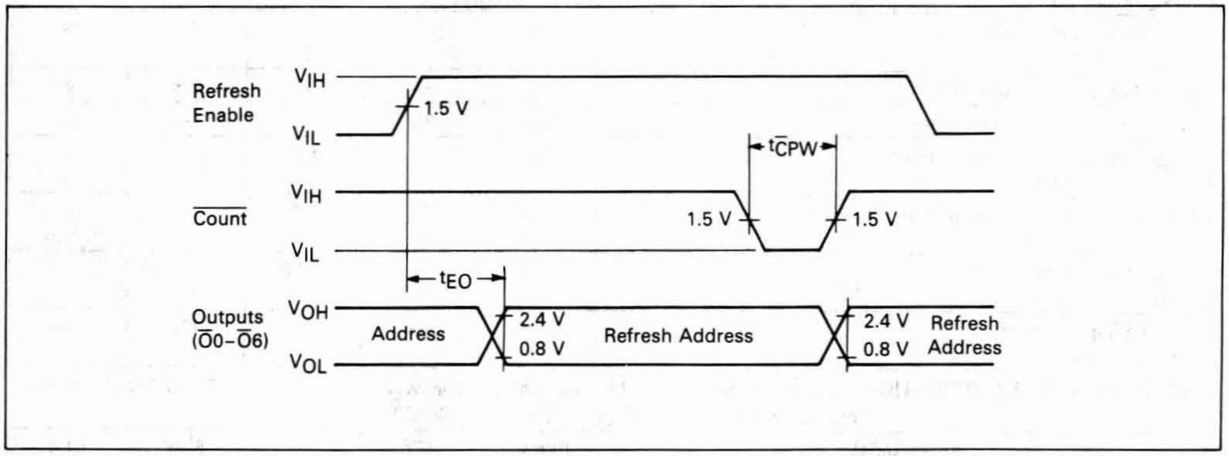
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Times | | | | | |
| Address Input to Output | $t_{AO}$ | | | | ns |
| (Load = 1 TTL, $C_L$ = 250 pF) | | — | 12 | 25 | |
| (Load = 1 TTL, $C_L$ = 15 pF, $V_{CC}$ = 5.0 V, $T_A$ = 25°C) | | — | 6.0 | 9.0 | |
| Row Enable to Output | $t_{OO}$ | | | | ns |
| (Load = 1 TTL, $C_L$ = 250 pF) | | 12 | 27 | 41 | |
| (Load = 1 TTL, $C_L$ = 15 pF, $V_{CC}$ = 5.0 V, $T_A$ = 25°C) | | 7.0 | 12 | 27 | |
| Refresh Enable to Output | $t_{EO}$ | | | | ns |
| (Load = 1 TTL, $C_L$ = 250 pF) | | 12 | 30 | 45 | |
| (Load = 1 TTL, $C_L$ = 15 pF, $V_{CC}$ = 5.0 V, $T_A$ = 25°C) | | 7.0 | 14 | 27 | |
| $\overline{\text{Count}}$ Pulse Width | $t_{W\overline{C}}$ | 30 | — | — | ns |
| Counting Frequency | $f_{\overline{C}}$ | 5.0 | 10 | — | MHz |

FIGURE 1 — AC WAVEFORMS WITH MCM4116 NORMAL CYCLE


Row Enable
$V_{IH}$
$V_{IL}$
$t_{AO}$
Address Input (A0–A14)
$V_{IH}$
1.5 V
$V_{IL}$
$t_{OO}$
$t_{OO}$
Outputs ($\overline{O}0$–$\overline{O}6$)
$V_{OH}$
$V_{OL}$
Don't Care
2.4 V
0.8 V
Row Address
2.4 V
0.8 V
Column Address

Refresh Enable — Low Logic State

FIGURE 2 — REFRESH CYCLE


Refresh Enable
$V_{IH}$
$V_{IL}$
1.5 V
$t_{\overline{C}PW}$
$\overline{\text{Count}}$
$V_{IH}$
$V_{IL}$
1.5 V
1.5 V
$t_{EO}$
Outputs ($\overline{O}0$–$\overline{O}6$)
$V_{OH}$
$V_{OL}$
Address
2.4 V
0.8 V
Refresh Address
2.4 V
0.8 V
Refresh Address

## TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CURRENT versus OUTPUT LOW VOLTAGE

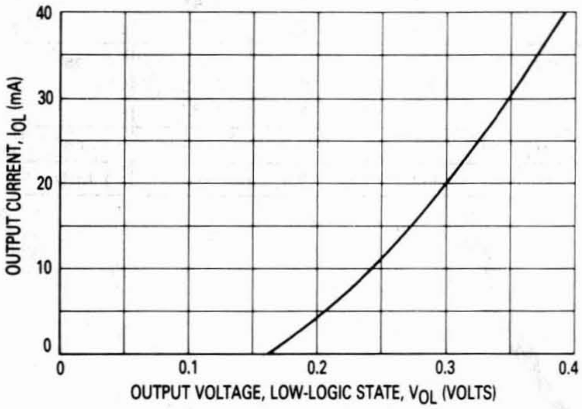
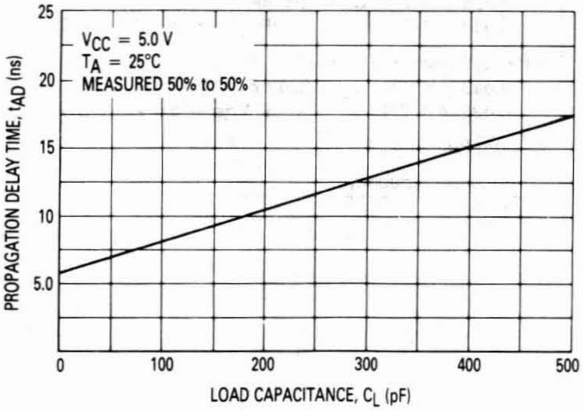


FIGURE 4 — PROPAGATION DELAY versus LOAD CAPACITANCE
Row or Column Address to Output



## PIN DEFINITIONS

**$\overline{\text{Count}}$ Inout — Pin 1**
Active low input increments internal 6-bit counter by one for each count pulse in.

**Refresh Enable Input — Pin 2**
Active high input which determines whether the MC3242A is in refresh mode (H) or address enable (L).

**A0–A6 Inputs — Pins 9, 5, 7, 21, 23, 27**
Row address inputs.

**A7–A13 Inputs — Pins 10, 6, 8, 20, 22, 24, 26**
Column address inputs.

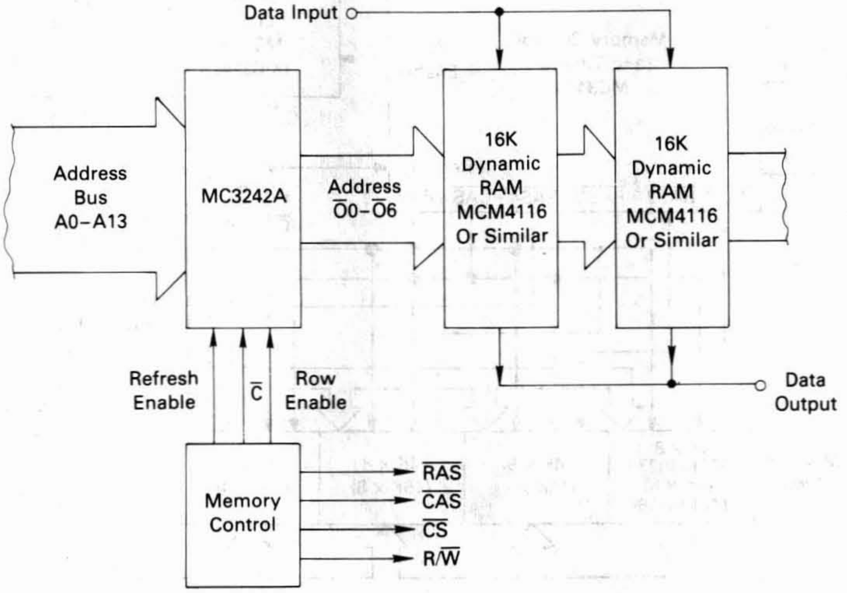
**$\overline{\text{O}}$0–$\overline{\text{O}}$6 Outputs — Pins 11, 12, 13, 18, 17, 16, 19**
Address outputs to memories. Inverted with respect to address inputs. Good high capacitance load driving techniques usually include a 10 Ω or greater clamping resistor in series with $\overline{\text{O}}$0–$\overline{\text{O}}$6 outputs.

**Gnd — Pin 14**
Power supply ground.

**CE Input — Pin 15**
Optional use, chip enable control pin. Left open, an internal 50 kΩ pullup resistor keeps this pin high and the MC3242A is a functional replacement for the Intel 3242 (without detect zero function). As an active input, when pulled low, all 3242A outputs go three-state.

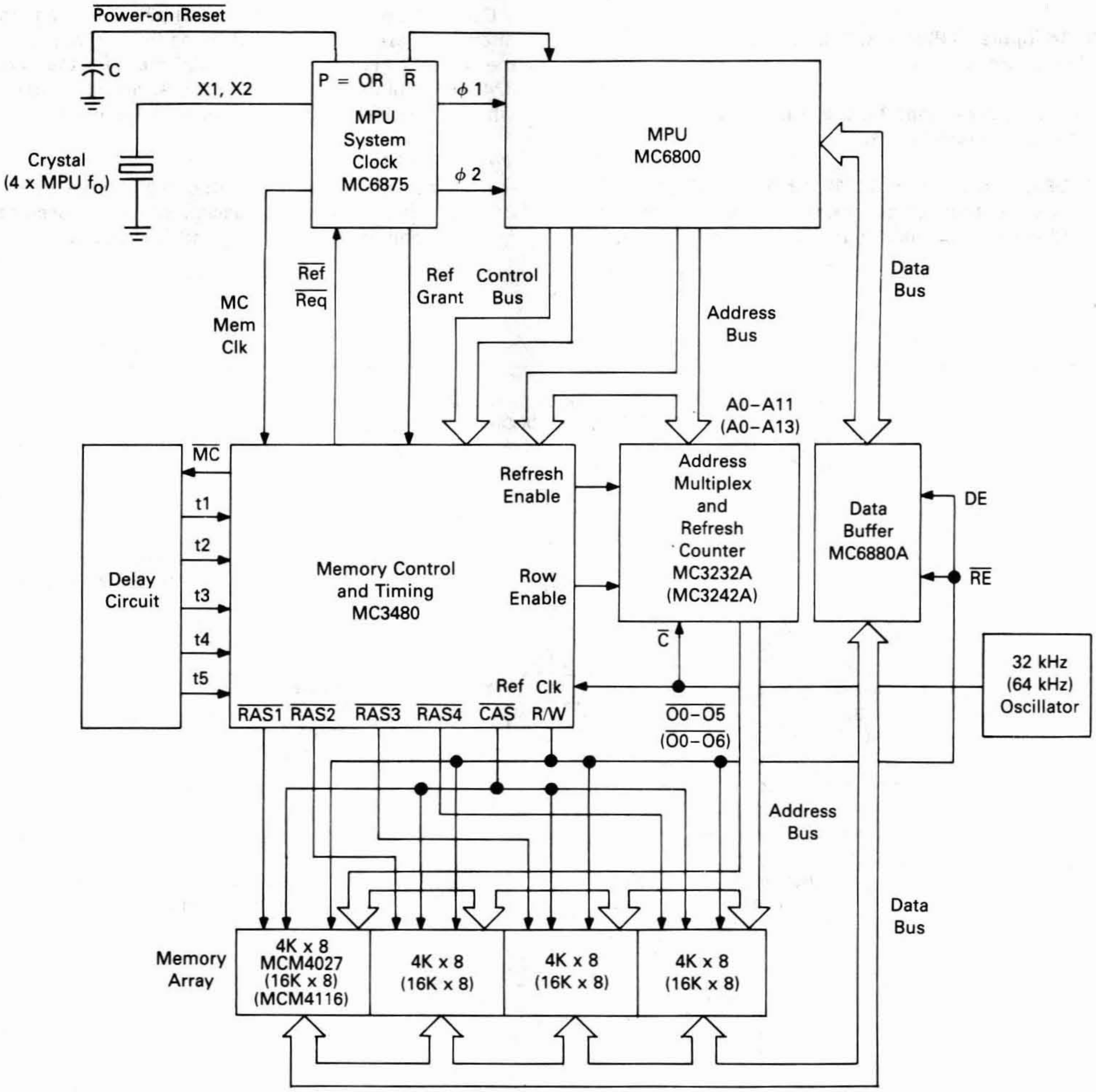
**$V_{CC}$ — Pin 28**
+5.0 V power supply input. Due to high capacitance drive capability, a 0.1 μF capacitor should be used to ground along with careful $V_{CC}$ and Gnd Bus layout.

**GENERAL 16K DYNAMIC RAM SIMPLIFIED BLOCK DIAGRAM**


Data Input
Address Bus A0–A13
MC3242A
Address $\overline{\text{O}}$0–$\overline{\text{O}}$6
16K Dynamic RAM MCM4116 Or Similar
16K Dynamic RAM MCM4116 Or Similar
Refresh Enable
$\overline{\text{C}}$
Row Enable
Data Output
Memory Control
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
$\overline{\text{CS}}$
R/$\overline{\text{W}}$

## TYPICAL APPLICATION
## 16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate part types or values for 16K x 1.0 RAMs


Power-on Reset
C
X1, X2
Crystal (4 x MPU $f_o$)
P = OR $\overline{R}$
MPU System Clock MC6875
$\phi$ 1
$\phi$ 2
MPU MC6800
Data Bus
MC Mem Clk
$\overline{Ref}$ $\overline{Req}$
Ref Grant
Control Bus
Address Bus
A0–A11 (A0–A13)
Delay Circuit
$\overline{MC}$
t1
t2
t3
t4
t5
Memory Control and Timing MC3480
Refresh Enable
Row Enable
Ref Clk
$\overline{RAS1}$ $\overline{RAS2}$ $\overline{RAS3}$ $\overline{RAS4}$ $\overline{CAS}$ R/W
Address Multiplex and Refresh Counter MC3232A (MC3242A)
$\overline{C}$
$\overline{O0-O5}$ ($\overline{O0-O6}$)
Data Buffer MC6880A
DE
$\overline{RE}$
32 kHz (64 kHz) Oscillator
Address Bus
Data Bus
Memory Array
4K x 8 MCM4027 (16K x 8) (MCM4116)
4K x 8 (16K x 8)
4K x 8 (16K x 8)
4K x 8 (16K x 8)

**MOTOROLA**

# MC3467

## TRIPLE MAGNETIC TAPE MEMORY PREAMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

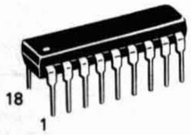
## TRIPLE WIDEBAND PREAMPLIFIER WITH ELECTRONIC GAIN CONTROL (EGC)

The MC3467 provides three independent preamplifiers with individual electronic gain control in a single 18-pin package. Each preamplifier has differential inputs and outputs allowing operation in completely balanced systems. The device is optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

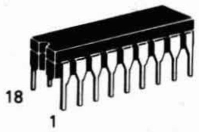
The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V.

- Wide Bandwidth – 15 MHz (Typ)
- Individual Electronic Gain Control
- Differential Input/Output

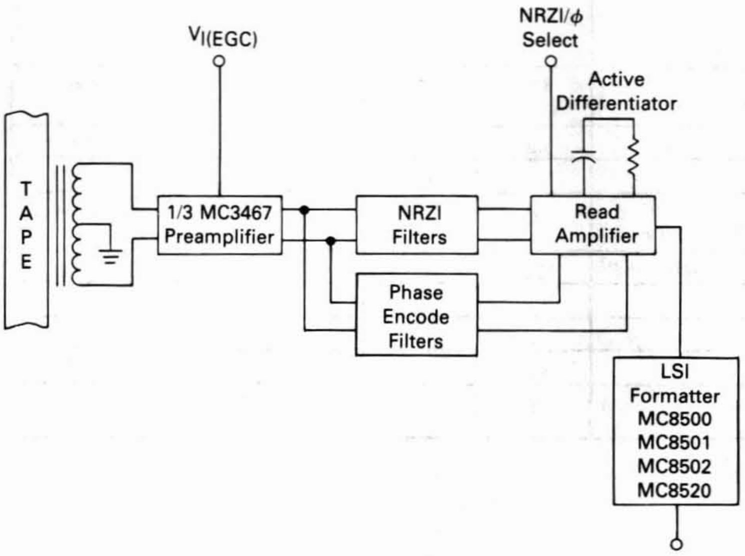
**P SUFFIX**
PLASTIC PACKAGE
707-02

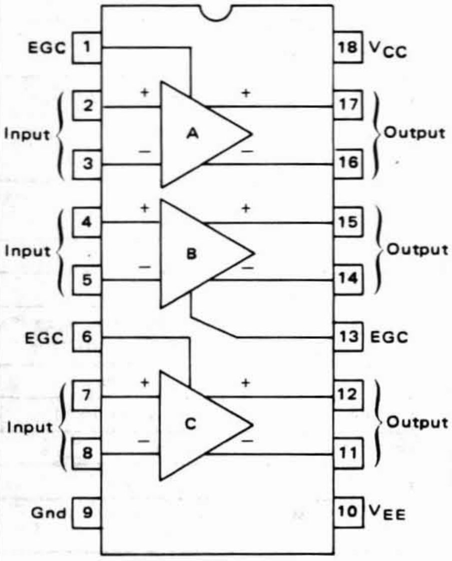


**L SUFFIX**
CERAMIC PACKAGE
CASE 726-01



### TYPICAL APPLICATION HIGH PERFORMANCE 9-TRACK OPEN REEL TAPE SYSTEM


V_I(EGC)
NRZI/φ Select
Active Differentiator
T A P E
1/3 MC3467 Preamplifier
NRZI Filters
Read Amplifier
Phase Encode Filters
LSI Formatter MC8500 MC8501 MC8502 MC8520


EGC 1
Input 2
Input 3
Input 4
Input 5
EGC 6
Input 7
Input 8
Gnd 9
18 VCC
17 Output
16 Output
15 Output
14 Output
13 EGC
12 Output
11 Output
10 VEE
A
B
C
+
–

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltages<br>Positive Supply Voltage<br>Negative Supply Voltage | <br>$V_{CC}$<br>$V_{EE}$ | <br>6.0<br>−9.0 | V |
| EGC Voltages (Pins 1, 6 and 13) | $V_{I(EGC)}$ | −5.0 to $V_{CC}$ | V |
| Input Differential Voltage | $V_{ID}$ | ±5.0 | V |
| Input Common-Mode Voltage | $V_{IC}$ | ±5.0 | V |
| Amplifier Output Short Circuit Duration (to Ground) | $t_{sc}$ | 10 | s |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature | $T_J$ | +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = −6.0 V, f = 100 kHz, $T_A$ = 0 to +70°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage Range<br>Positive Supply Voltage<br>Negative Supply Voltage<br>Operating EGC Voltage | <br>$V_{CCR}$<br>$V_{EER}$<br>$V_{I(EGC)}$ | <br>4.75<br>−5.5<br>0 | <br>5.0<br>−6.0<br>– | <br>5.25<br>−7.0<br>$V_{CC}$ | <br>V<br>V<br>V |
| Differential Voltage Gain (Balanced) ($V_{I(EGC)}$ = 0, $e_i$ = 25 mVp-p) (See Figure 1) | $A_{VD}$ | 85 | 100 | 120 | V/V |
| Differential Voltage Gain ($V_{I(EGC)}$ = $V_{CC}$) | $A_{VD}$ | – | 0.5 | 2.0 | V/V |
| Maximum Input Differential Voltage (Balanced) ($T_A$ = 25°C) | $V_{IDR}$ | 0.2 | – | – | $V_{pp}$ |
| Output Voltage Swing (Balanced) (Figure 1) ($e_i$ = 200 mVp-p) | $V_{OR}$ | 6.0 | 8.0 | – | $V_{pp}$ |
| Input Common-Mode Range | $V_{ICR}$ | ±1.5 | ±2.0 | – | V |
| Differential Output Offset Voltage ($T_A$ = 25°C) | $V_{OOD}$ | – | 500 | – | mV |
| Common-Mode Output Offset Voltage ($T_A$ = 25°C) | $V_{OOC}$ | – | 500 | – | mV |
| Common Mode Rejection Ratio (Figure 2)<br>$V_{I(EGC)}$ = 0, $V_{CM}$ = 1.0 $V_{pp}$<br>(f = 100 kHz)<br>(f = 1.0 MHz) | CMRR | <br><br>60<br>40 | <br><br>100<br>100 | <br><br>–<br>– | dB |
| Small-Signal Bandwidth (Figure 1) (−3.0 dB, $e_i$ = 1.0 mVp-p, $T_A$ = 25°C) | BW | 10 | 15 | – | MHz |
| Input Bias Current | $I_{IB}$ | – | 5.0 | 15 | μA |
| Output Sink Current (Figure 5) | $I_{OS}$ | 1.0 | 1.4 | – | mA |
| Differential Noise Voltage Referred to Input (Figure 3) ($V_{I(EGC)}$ = 0, $R_S$ = 50 Ω, BW = 10 Hz to 1.0 MHz, $T_A$ = 25°C) | $e_n$ | – | 3.5 | – | $\mu V_{RMS}$ |
| Positive Power Supply Current (Figure 4) | $I_{CC}$ | – | 30 | 40 | mA |
| Negative Power Supply Current (Figure 4) | $I_{EE}$ | – | −30 | −40 | mA |
| Input Resistance ($T_A$ = 25°C) | $r_i$ | 12 | 25 | – | kΩ |
| Input Capacitance ($T_A$ = 25°C) | $C_i$ | – | 2.0 | – | pF |
| Output Resistance (Unbalanced) ($T_A$ = 25°C) | $r_o$ | – | 30 | – | Ohms |

**FIGURE 1 – DIFFERENTIAL VOLTAGE GAIN, BANDWIDTH AND OUTPUT VOLTAGE SWING TEST CIRCUIT**
**(Channel A under test, other channels tested similarly)**

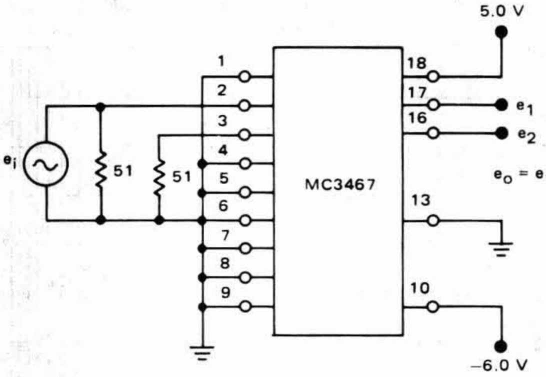

5.0 V
1
2
3
4
5
6
7
8
9
18
17
16
13
10
$e_1$
$e_2$
$e_i$
51
51
MC3467
$e_o = e_1 - e_2$
−6.0 V

**FIGURE 2 – COMMON-MODE REJECTION RATIO**
**(Channel A under test, other amplifiers tested similarly)**

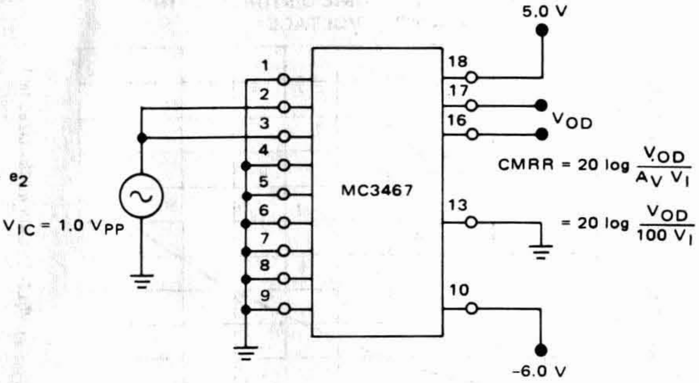
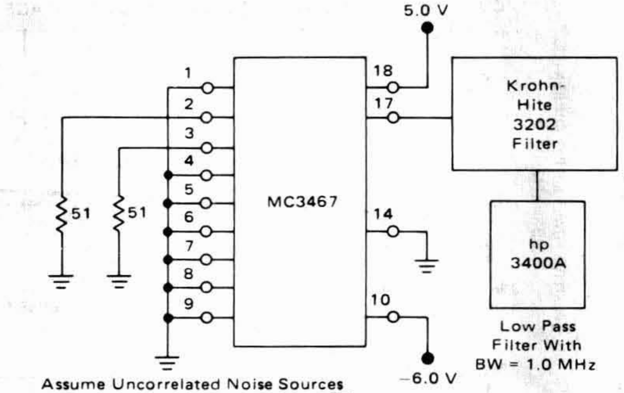

5.0 V
1
2
3
4
5
6
7
8
9
18
17
16
13
10
$V_{OD}$
$V_{IC} = 1.0\ V_{PP}$
MC3467
$\text{CMRR} = 20 \log \frac{V_{OD}}{A_V V_I}$
$= 20 \log \frac{V_{OD}}{100\ V_I}$
−6.0 V

**FIGURE 3 – DIFFERENTIAL NOISE VOLTAGE REFERRED TO THE INPUT**


5.0 V
1
2
3
4
5
6
7
8
9
18
17
14
10
51
51
MC3467
Krohn-Hite 3202 Filter
hp 3400A
Low Pass Filter With BW = 1.0 MHz
−6.0 V

Assume Uncorrelated Noise Sources
$e_n$ (Differential Noise at Input) = $e_o \sqrt{2}/100$

**FIGURE 4 – POWER SUPPLY CURRENT TEST CIRCUIT**

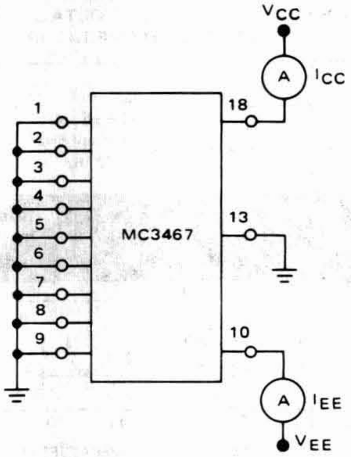

$V_{CC}$
A
$I_{CC}$
1
2
3
4
5
6
7
8
9
18
13
10
MC3467
A
$I_{EE}$
$V_{EE}$

**FIGURE 5 – OUTPUT SINK CURRENT TEST CIRCUIT**
**(Channel A under test, other channels tested similarly)**

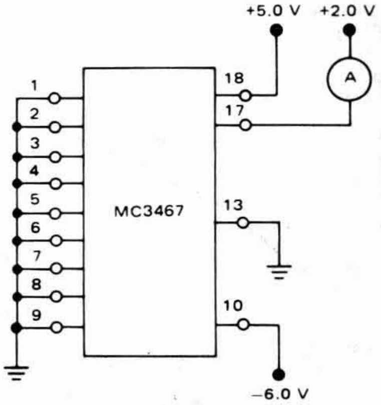
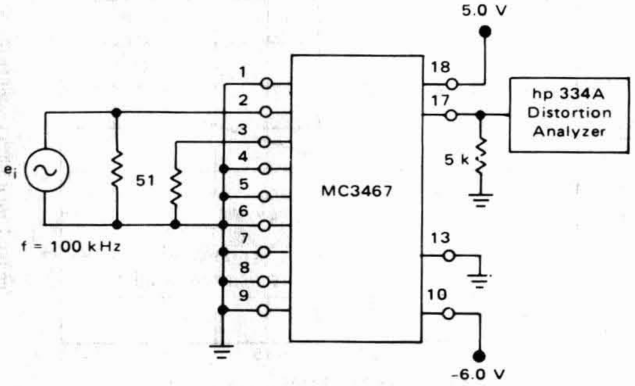

+5.0 V
+2.0 V
A
1
2
3
4
5
6
7
8
9
18
17
13
10
MC3467
−6.0 V

**FIGURE 6 – TOTAL HARMONIC DISTORTION TEST CIRCUIT**
**(Channel A under test, other channels tested similarly)**


5.0 V
1
2
3
4
5
6
7
8
9
18
17
13
10
$e_i$
51
f = 100 kHz
MC3467
hp 334A Distortion Analyzer
5 k
−6.0 V

## TYPICAL CHARACTERISTICS
## ($V_{CC}$ = 5.0 V, $V_{EE}$ = -6.0 V, $T_A$ = 25° unless otherwise noted)

**FIGURE 7 – TOTAL HARMONIC DISTORTION (THD) versus INPUT VOLTAGE**

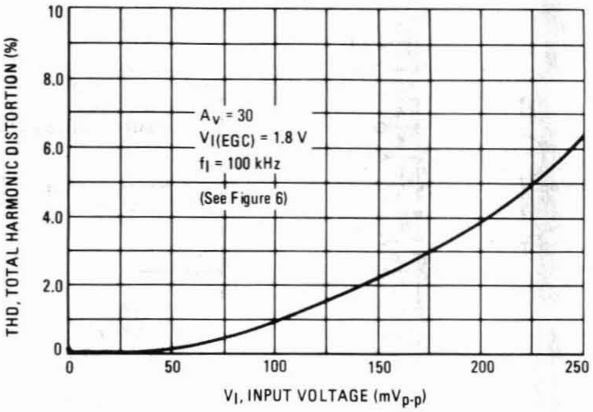


**FIGURE 8 – NORMALIZED VOLTAGE GAIN versus FREQUENCY**

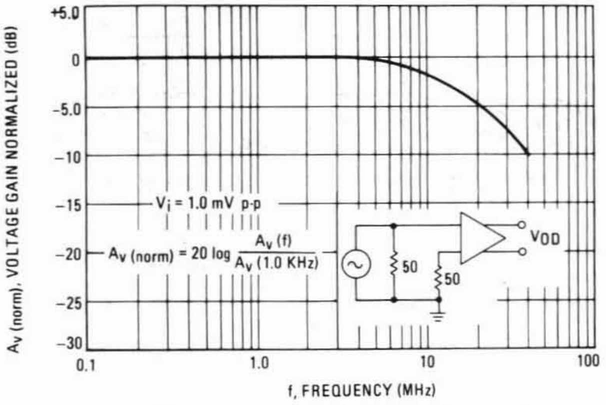


**FIGURE 9 – NORMALIZED VOLTAGE GAIN versus AMBIENT TEMPERATURE**

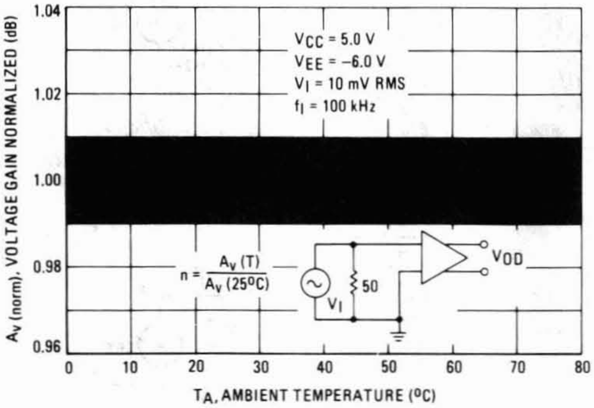


**FIGURE 10 – NORMALIZED POSITIVE POWER SUPPLY CURRENT versus POSITIVE POWER SUPPLY VOLTAGE**

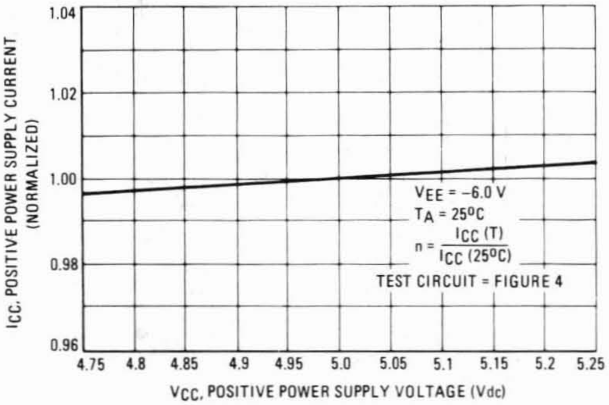


**FIGURE 11 – NORMALIZED NEGATIVE POWER SUPPLY CURRENT versus NEGATIVE POWER SUPPLY VOLTAGE**

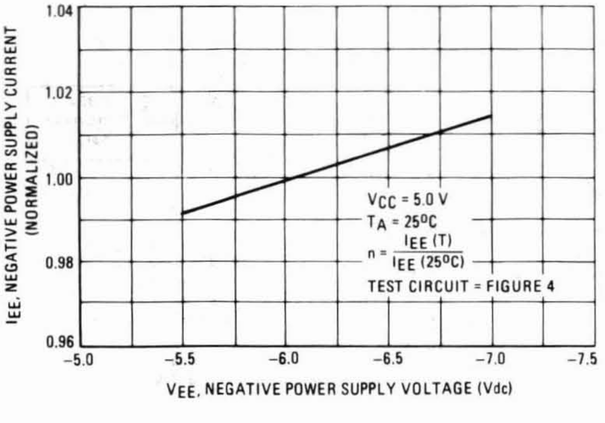


**FIGURE 12 – NORMALIZED POWER SUPPLY CURRENTS versus AMBIENT TEMPERATURE**

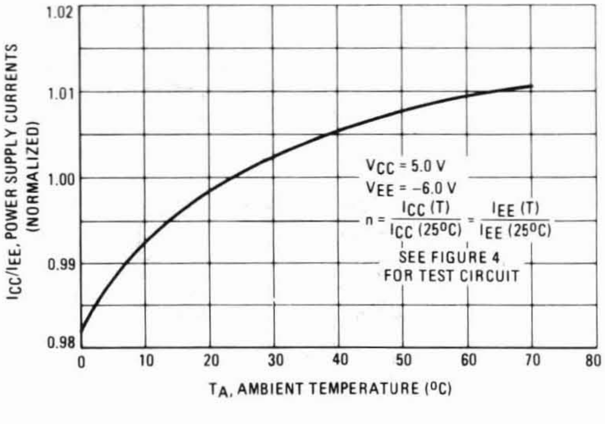


**FIGURE 13 – DIFFERENTIAL VOLTAGE GAIN versus ELECTRONIC GAIN CONTROL VOLTAGE ($V_{I(EGC)}$)**

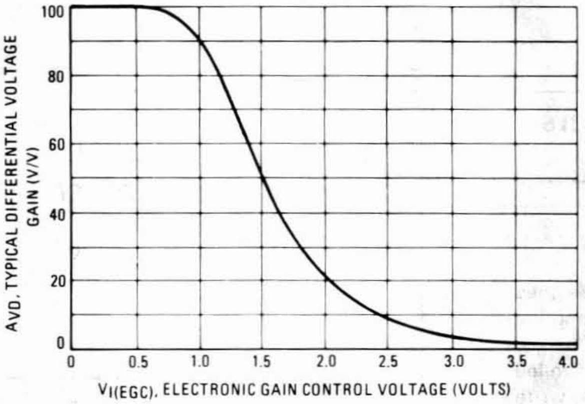


**FIGURE 14 – COMMON-MODE REJECTION RATIO (CMRR) versus FREQUENCY**

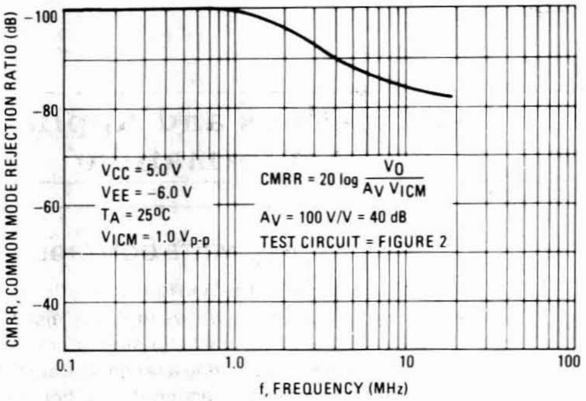


**FIGURE 15 – PHASE SHIFT versus FREQUENCY**

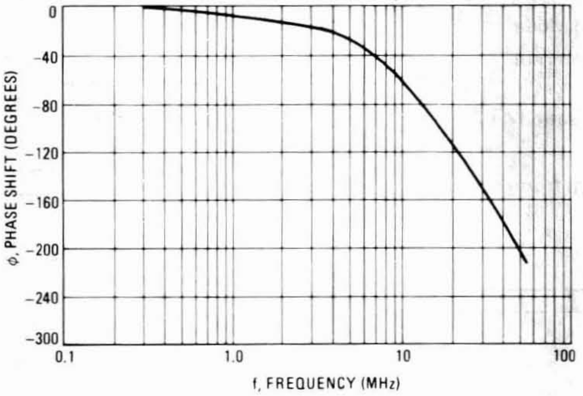
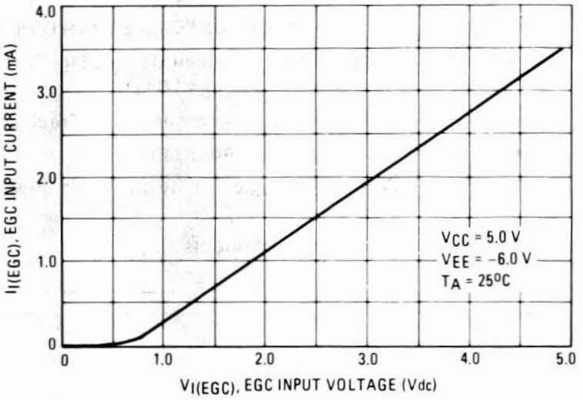
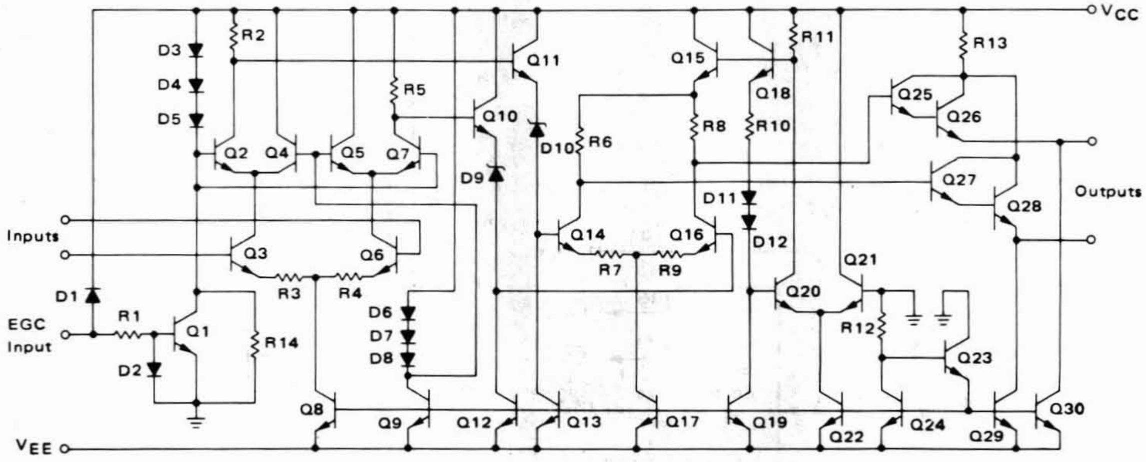


**FIGURE 16 – TYPICAL EGC INPUT CURRENT versus EGC INPUT VOLTAGE**



## REPRESENTATIVE CIRCUIT SCHEMATIC

1/3 MC3467



$V_{CC}$
D3
D4
D5
R2
R5
Q2
Q4
Q5
Q7
Q11
Q10
D10
D9
R6
Q15
Q18
R8
R10
R11
R13
Q25
Q26
Q27
Q28
Outputs
D11
D12
Inputs
Q3
Q6
R3
R4
Q14
Q16
R7
R9
Q21
Q20
R12
Q23
D1
R1
EGC Input
Q1
R14
D2
D6
D7
D8
Q8
Q9
Q12
Q13
Q17
Q19
Q22
Q24
Q29
Q30
$V_{EE}$

**MOTOROLA**

# MC3469P

## Specifications and Applications Information

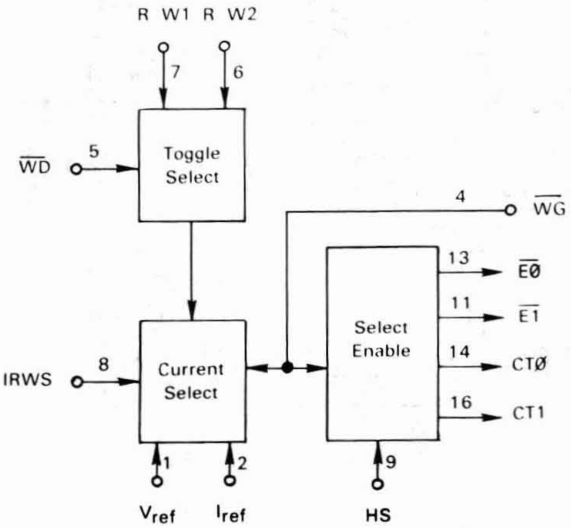
### FLOPPY DISK WRITE CONTROLLER

The MC3469 is a monolithic WRITE Current Controller designed to provide the entire interface between floppy disk heads and the head control and write data signals for stradle-erase heads.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer track compensation.

- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Provides High Impedance (Read Data Enable) During Read Mode
- Head Current (Write) Guaranteed Using Laser Trimmed Internal Resistor (3.0 mA using $R_{ext} = 10\ k\Omega$)
- IRW Select Input Provides for Inner/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified With ±10% Logic Supply and Head Supply ($V_{BB}$) from 10.8 V to 26.4 V
- Minimizes External Components

BLOCK DIAGRAM

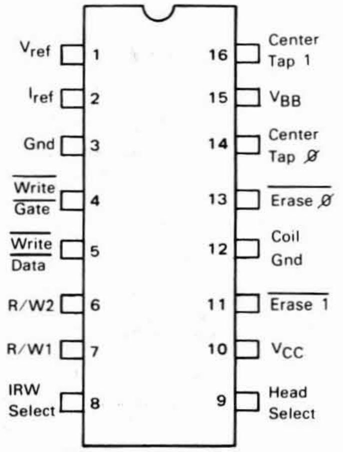

R W1
R W2
7
6
WD
5
Toggle Select
4
WG
13
E0
11
E1
Select Enable
14
CT0
16
CT1
IRWS
8
Current Select
1
2
9
Vref
Iref
HS

FLOPPY DISK
WRITE CONTROLLER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

PIN CONNECTIONS


Vref 1
Iref 2
Gnd 3
Write Gate 4
Write Data 5
R/W2 6
R/W1 7
IRW Select 8
16 Center Tap 1
15 VBB
14 Center Tap 0
13 Erase 0
12 Coil Gnd
11 Erase 1
10 VCC
9 Head Select

## ABSOLUTE MAXIMUM RATINGS (Note 1) ($T_A$ = 25°C)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage (Pin 10) | $V_{CC}$ | 7.0 | Vdc |
| Power Supply Voltage (Pin 15) | $V_{BB}$ | 30 | Vdc |
| Input Voltage (Pins 4, 5, 8, 9) | $V_I$ | 5.75 | Vdc |
| Storage Temperature | $T_{stg}$ | -55 to +150 | °C |
| Operating Junction Temperature | $T_J$ | 150 | °C |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## RECOMMENDED OPERATING CONDITIONS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage (Pin 10) | $V_{CC}$ | +4.5 to +5.5 | Vdc |
| Power Supply Voltage (Pin 15) | $V_{BB}$ | +10.8 to +26.4 | Vdc |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |

## ELECTRICAL CHARACTERISTICS ($T_A$ = 0 to +70°C, $V_{CC}$ = 4.5 to 5.5 V, $V_{BB}$ = 10.8 to 26.4 V unless otherwise noted. Typicals given for $V_{CC}$ = 5.0 V, $V_{BB}$ = 12 V and $T_A$ = 25°C unless otherwise noted.)

| Characteristics | Pins | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DIGITAL INPUT VOLTAGES** | | | | | | |
| Power Supply Current — $V_{CC}$<br>$V_{BB}$ | | $I_{CC}$<br>$I_{BB}$ | —<br>— | 22<br>15 | 50<br>30 | mA |
| High Level Input Voltage ($V_{CC}$ = 4.5 V) | 4, 8, 9 | $V_{IH}$ | 2.0 | — | — | V |
| Low Level Input Voltage ($V_{CC}$ = 5.5 V) | 4, 8, 9 | $V_{IL}$ | — | — | 0.8 | V |
| Input Clamp Voltage ($I_{IK}$ = −12 mA) | 4, 5, 8, 9 | $V_{IK}$ | — | -0.87 | -1.5 | V |
| Positive Threshold ($V_{CC}$ = 5.0) | 5 | $V_{T(+)}$ | 1.5 | 1.75 | 2.0 | V |
| Negative Threshold ($V_{CC}$ = 5.0) | 5 | $V_{T(-)}$ | 0.7 | 0.98 | 1.3 | V |
| Hysteresis ($V_{T(+)} - V_{T(-)}$)<br>$T_A$ = 0°C to +70°C<br>$T_A$ = 25°C | | $V_{HTS}$ | <br>0.2<br>0.4 | <br>—<br>0.76 | <br>—<br>— | V |
| **DIGITAL INPUT CURRENTS** | | | | | | |
| High Level Input Current ($V_{CC}$ = 5.5 V, $V_{BB}$ = 26.4 V, $V_I$ = 2.4 V) | 4, 5, 8, 9 | $I_{IH}$ | — | 0.1 | 40 | μA |
| Low Level Input Current ($V_{CC}$ = 5.5 V, $V_{BB}$ = 26.4 V, $T_A$ = 25°C unless noted below) | 4, 5, 8, 9 | $I_{IL}$ | — | — | -1.6 | mA |
| $V_{BB}$ = 12 V | 4 | | — | 0.36 | — | |
| $V_{BB}$ = 24 V | 4 | | — | 0.76 | — | |
| $V_{CC}$ = 5.0 V | 5 | | — | 0.46 | — | |
| $V_{CC}$ = 5.0 V | 8, 9 | | — | 0.39 | — | |

**ELECTRICAL CHARACTERISTICS (continued)** ($T_A = 0$ to $+70°C$, $V_{CC} = 4.5$ to $5.5$ V, $V_{BB} = 10.8$ to $26.4$ V unless otherwise noted. Typicals given for $V_{CC} = 5.0$ V, $V_{BB} = 12$ V and $T_A = 25°C$ unless otherwise noted.)

| Characteristics | Pins | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CENTER-TAP and ERASE OUTPUTS** | | | | | | |
| Output High Voltage (See Figure 9)<br>($I_{OH} = -100$ mA, $V_{CC} = 4.5$ V)<br>$V_{BB} = 10.8$ to $26.4$ V | 14, 16 | $V_{OH}$ | $V_{BB}$-1.5 | $V_{BB}$-1.0 | — | V |
| Output Low Voltage (See Figure 9)<br>($I_{OL} = 1.0$ mA) | 14, 16 | $V_{OL}$ | | | | mV |
| $V_{BB} = 12$ V | | | — | 70 | 150 | |
| $V_{BB} = 24$ V | | | — | 70 | 150 | |
| Output High Leakage<br>($V_{OH} = 24$ V, $V_{CC} = 4.5$ V, $V_{BB} = 24$ V) | 11, 13 | $I_{OH}$ | — | 0.01 | 100 | μA |
| Output Low Voltage (See Figure 10)<br>($I_{OL} = 90$ mA, $V_{CC} = 4.5$ V) | 11, 13 | $V_{OL}$ | | | | V |
| $V_{BB} = 12$ V | | | — | 0.27 | 0.60 | |
| $V_{BB} = 24$ V | | | — | 0.27 | 0.60 | |
| **CURRENT SOURCE** | | | | | | |
| Reference Voltage | 1 | $V_{ref}$ | — | 5.7 | — | V |
| Degauss Voltage (See Text)<br>(Voltage Pin 1 – Voltage Pin 2) | 1 | $V_{DEG}$ | — | 1.0 | — | V |
| Bias Voltage | 2 | $V_F$ | — | 0.7 | — | V |
| Write Current Off Leakage<br>($V_{OH} = 35$ V) | 6, 7 | $I_{OH}$ | — | 0.03 | 15 | μA |
| Saturation Voltage<br>($V_{BB} = 12$ V) | 6, 7 | $V_{sat}$ | — | 0.85 | 2.7 | V |
| Current Sink Compliance<br>(For $V_{6,\,7} = 4.0$ V to 24 V, $V_{\overline{WG}} = 0.8$ V) | 6, 7 | $\Delta I/RW2, 1$ | — | 15 | 40 | μA |
| Average Value Write Current<br>$\left(\frac{(I_{Pin\,6} + I_{Pin\,7})}{2}\right.$ for $V_{BB} = 10.8$ to $26.4$ V) | 6, 7 | | | | | |
| @ $I_{R/W} = I_{LOW}$, R = 10 k | | $\overline{I_{R/W(L)}}$ | | | | mA |
| $T_A = 25°C$ | | | 2.91 | 3.0 | 3.09 | |
| $T_A = 0$ to $+70°C$ | | | 2.84 | — | 3.16 | |
| @ $I_{R/W} = I_{LOW}$, R = 5.0 k | | | | | | |
| $T_A = 25°C$ | | | 5.64 | 5.89 | 6.14 | |
| $T_A = 0$ to $+70°C$ | | | 5.51 | — | 6.28 | |
| @ $I_{R/W} = I_{HI}$, R = 10 k ($I_{HI} = I_{LOW} + \%\ I_{LOW}$) | | $\overline{\Delta I_{R/W(H)}}$ | | | | % |
| $T_A = 25°C$ | | | 31.3 | 33.3 | 35.5 | |
| $T_A = 0$ to $+70°C$ | | | 30.3 | 33.3 | 36.6 | |
| Difference in Write Current<br>($\lvert I_{Pin\,6} - I_{Pin\,7} \rvert$<br>@ $I_{R/W} = I_{LOW}$, $V_{BB} = 10.8$ V to $26.4$ V) | 6, 7 | $I_{R/W\Delta}$ | | | | mA |
| R = 10 k | | | | | | |
| $T_A = 25°C$ | | | — | 0.003 | 0.015 | |
| $T_A = 0$ to $+70°C$ | | | — | — | 0.023 | |
| R = 5.0 k | | | | | | |
| $T_A = 25°C$ | | | — | — | 0.030 | |
| $T_A = 0$ to $+70°C$ | | | — | — | 0.046 | |

**AC SWITCHING CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $T_A$ = 25°C, $V_{BB}$ = 24 V, $I_{RWS}$ = 0.4 and $I_{R/W}$ = 3.0 mA unless otherwise noted — refer to Figure 2 and Figure 11.)

| **Characteristics** (Note 2) | $f_{in}$ (Note 3) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 1. Delay from Head Select going low through 0.8 V to CT0 going high through 20 V. | HS, Pin 9 | — | 1.6 | 4.0 | μs |
| 2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V. | HS, Pin 9 | — | 2.1 | 4.0 | μs |
| 3. Delay from Head Select going high through 2.4 V to CT0 going low through 1.0 V. | HS, Pin 9 | — | 1.7 | 4.0 | μs |
| 4. Delay from Head Select going high through 2.4 V to CT1 going high through 20 V. | HS, Pin 9 | — | 1.4 | 4.0 | μs |
| 5. Delay from $\overline{\mathrm{WG}}$ going low through 0.8 V to CT0 going low through 1.0 V. | $\overline{\mathrm{WG}}$, Pin 4 | — | 1.3 | 4.0 | μs |
| 6. Delay from $\overline{\mathrm{WG}}$ going low through 0.8 V to CT1 going high through 20 V. | $\overline{\mathrm{WG}}$, Pin 4 | — | 0.8 | 4.0 | μs |
| 7. Delay from $\overline{\mathrm{WG}}$ going low through 0.8 V to CT0 going high through 20 V. | $\overline{\mathrm{WG}}$, Pin 4 | — | 0.75 | 4.0 | μs |
| 8. Delay from $\overline{\mathrm{WG}}$ going low through 0.8 V to CT1 going low through 1.0 V. | $\overline{\mathrm{WG}}$, Pin 4 | — | 1.2 | 4.0 | μs |
| 9. After $\overline{\mathrm{WG}}$ goes high, delay from R/W1 turning off through 10% to CT0 going high through 20 V. | $\overline{\mathrm{WG}}$, Pin 4 | 20 | 750 | — | ns |
| 10. After $\overline{\mathrm{WG}}$ goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V. | $\overline{\mathrm{WG}}$, Pin 4 | 20 | 1200 | — | ns |
| 11. After $\overline{\mathrm{WG}}$ goes high, delay from R/W2 turning off through 10% to CT0 going low through 1.0 V. | $\overline{\mathrm{WG}}$, Pin 4 | 20 | 1200 | — | ns |
| 12. After $\overline{\mathrm{WG}}$ goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V. | $\overline{\mathrm{WG}}$, Pin 4 | 20 | 600 | — | ns |
| 13. Delay from $\overline{\mathrm{WG}}$ going low through 0.8 V to $\overline{\mathrm{E0}}$ going low through 1.0 V. | $\overline{\mathrm{WG}}$, Pin 4 | — | 0.085 | 4.0 | μs |
| 14. Delay from $\overline{\mathrm{WG}}$ going low through 0.8 V to $\overline{\mathrm{E1}}$ going low through 1.0 V. | $\overline{\mathrm{WG}}$, Pin 4 | — | 0.085 | 4.0 | μs |
| 15. Delay from $\overline{\mathrm{WG}}$ going high through 2.0 V to $\overline{\mathrm{E0}}$ going high through 23 V. | $\overline{\mathrm{WG}}$, Pin 4 | — | 0.7 | 4.0 | μs |
| 16. Delay from $\overline{\mathrm{WG}}$ going high through 2.0 V to $\overline{\mathrm{E1}}$ going high through 23 V. | $\overline{\mathrm{WG}}$, Pin 4 | — | 0.7 | 4.0 | μs |
| 17. After $\overline{\mathrm{WG}}$ goes low, delay from CT0 going low through 1.0 V to R/W1 turning on through 10%. | $\overline{\mathrm{WG}}$, Pin 4 | 20 | 750 | — | ns |
| 18. After $\overline{\mathrm{WG}}$ goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%. | $\overline{\mathrm{WG}}$, Pin 4 | 20 | 750 | — | ns |
| 19. After $\overline{\mathrm{WG}}$ goes low, fall time (10% to 90%) of R/W1. | $\overline{\mathrm{WG}}$, Pin 4 | — | 5.0 | 200 | ns |
| 20. After $\overline{\mathrm{WG}}$ goes low, fall time (10% to 90%) of R/W2. | $\overline{\mathrm{WG}}$, Pin 4 | — | 5.0 | 200 | ns |
| 21. Setup time, Head Select going low before $\overline{\mathrm{WG}}$ going low. | $\overline{\mathrm{WG}}$, Pin 4 | 4.0 | — | — | μs |
| 22. $\overline{\text{Write Data}}$ low Hold Time | $\overline{\mathrm{WD}}$, Pin 5 | 200 | — | — | ns |
| 23. $\overline{\text{Write Data}}$ high Hold Time | $\overline{\mathrm{WD}}$, Pin 5 | 500 | — | — | ns |
| 24. Delay from $\overline{\mathrm{WG}}$ going high through 2.0 V to R/W 1 turning off through 10% of on value. | $\overline{\mathrm{WG}}$, Pin 4 | — | 3.9 | — | μs |

Note 2: Test numbers refer to encircled numbers in Figure 2.

Note 3: AC test waveforms applied to the designated pins as follows:

| Pin | $f_{in}$ | Amplitude | Duty Cycle |
|---|---|---|---|
| HS, Pin 9 | 50 KHz | 0.4 to 2.4 V | 50% |
| $\overline{\mathrm{WG}}$, Pin 4 | 50 KHz | 0.4 to 2.4 V | 50% |
| $\overline{\mathrm{WD}}$, Pin 5 | 1.0 MHz | 0.2 to 2.4 V | 50% |

## AC SWITCHING CHARACTERISTICS (continued)

($V_{CC}$ = 5.0 V, $T_A$ = 25°C, $V_{BB}$ = 24 V, $\overline{WG}$ = 0.4 unless otherwise noted — refer to Figure 3 and Figure 11.)

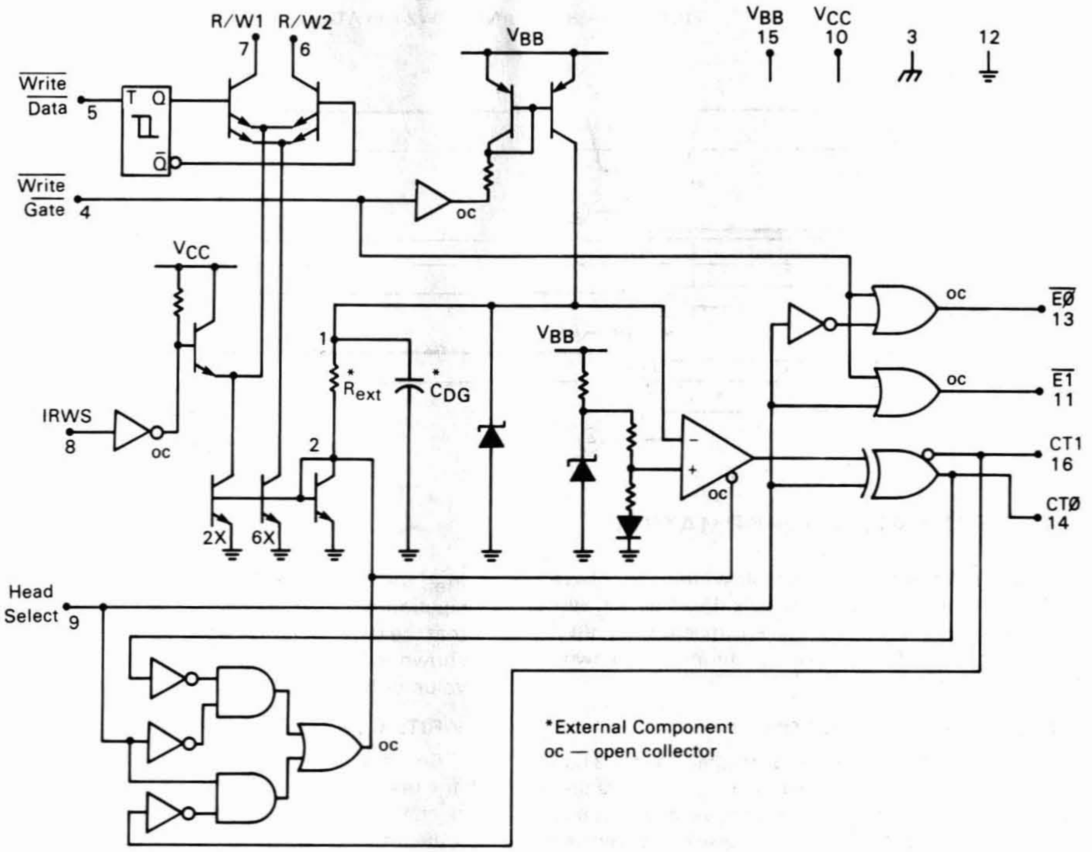
| **Characteristics** (Note 4) | Min | Typ | Max | Unit |
|---|---|---|---|---|
| 1. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning on through 50%. | — | 85 | — | ns |
| 2. Delay skew, difference of R/W1 turning off and R/W2 turning on through 50% after $\overline{\text{Write Data}}$ going low through 0.9 V. | — | 1.0 | ±40 | ns |
| 3. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning off through 50%. | — | 80 | — | ns |
| 4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after $\overline{\text{Write Data}}$ going low through 0.9 V. | — | 1.0 | ±40 | ns |
| 5. Rise time, 10% to 90%, of R/W1 | — | 1.7 | 200 | ns |
| 6. Rise time, 10% to 90%, of R/W2 | — | 1.7 | 200 | ns |
| 7. Fall time, 90% to 10%, of R/W1 | — | 12 | 200 | ns |
| 8. Fall time, 90% to 10%, of R/W2 | — | 12 | 200 | ns |

Note 4: Test numbers refer to encircled numbers in Figure 4.
$f_{in}$ = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

## PIN DESCRIPTION TABLE

| Name | Symbol | Pin | Description |
|---|---|---|---|
| Head Select | HS | 9 | Head Select input selects between the head I/O pins: center-tap, erase, and read/write. A HIGH selects Head 0 and a LOW selects Head 1. |
| $\overline{\text{Write Gate}}$ | $\overline{WG}$ | 4 | $\overline{\text{Write Gate}}$ input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current. |
| $\overline{\text{Write Data}}$ | $\overline{WD}$ | 5 | $\overline{\text{Write Data}}$ input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils. |
| IRW Select | IRWS | 8 | IRW Select input selects the amount of write current to be used. When LOW, the current equals the value found in Figure 5, according to the external resistor. When HIGH, the current equals the low current + 33%. |
| $V_{ref}$<br>$I_{ref}$ | $V_{ref}$<br>$I_{ref}$ | 1<br>2 | A resistor between these pins sets the write current. Laser trimming reliably produces 3 mA of current for a 10 k resistor. A capacitor from $V_{ref}$ to Gnd will adjust the Degauss period. |
| Center-tap 0 | CT0 | 14 | Center-tap 0 output is connected to the center tap of Head 0. It will be pulled to Gnd or $V_{BB}$ (+12 or +24) depending on mode and head selection. |
| $\overline{\text{Erase 0}}$ | $\overline{E0}$ | 13 | $\overline{\text{Erase 0}}$ will be LOW for writing on Head 0, and floating for other conditions. |
| Center-tap 1 | CT1 | 16 | Center-tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or $V_{BB}$ (+12 or +24) depending on mode and head selection. |
| $\overline{\text{Erase 1}}$ | $\overline{E1}$ | 11 | $\overline{\text{Erase 1}}$ will be LOW for writing on Head 1, and floating for other conditions. |
| R/W2 | R/W2 | 6 | R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads. |
| R/W1 | R/W1 | 7 | R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads. |
|  | $V_{CC}$ | 10 | +5 V Power |
|  | $V_{BB}$ | 15 | +12 V or + 24 V Power |
|  | Gnd | 12 | Coil grounds |
|  | Gnd | 3 | Reference and logic ground |

FIGURE 1 — LOGIC DIAGRAM


R/W1
R/W2
7
6
VBB
VBB
15
VCC
10
3
12
Write Data
5
T
Q
Q̄
Write Gate
4
oc
VCC
IRWS
8
oc
1
*
Rext
*
CDG
2
VBB
2X
6X
−
+
oc
oc
E̅0̅
13
oc
E̅1̅
11
CT1
16
CT0
14
Head Select
9
oc

*External Component
oc — open collector

FIGURE 2 — AC TIMING DIAGRAM

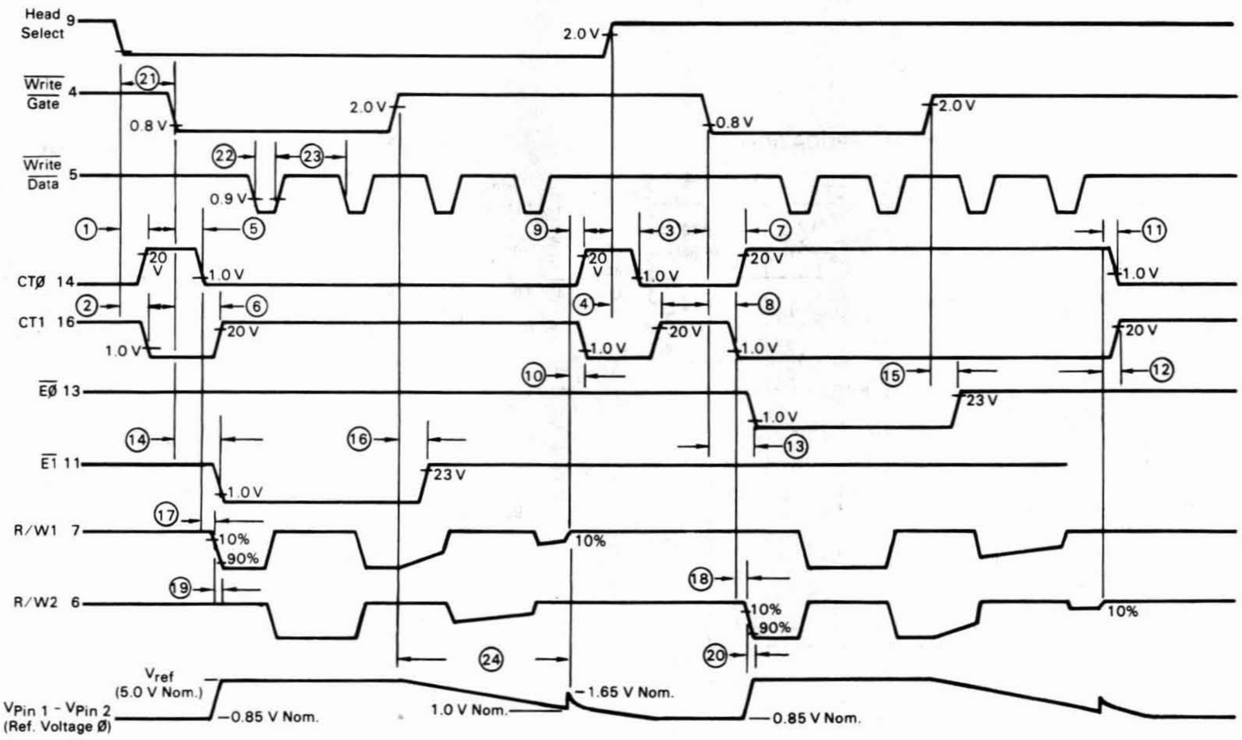
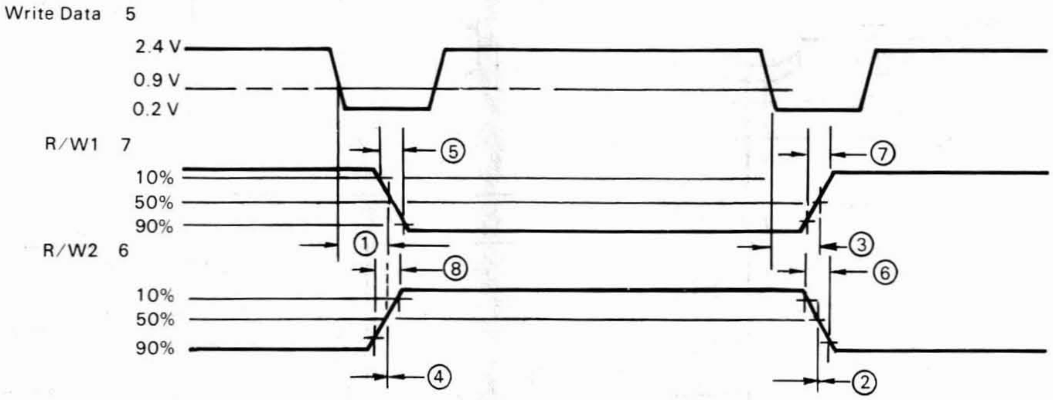

Head Select 9
2.0 V
Write Gate 4
㉑
0.8 V
2.0 V
0.8 V
2.0 V
Write Data 5
㉒
㉓
0.9 V
①
⑤
⑨
③
⑦
⑪
CT0 14
20 V
1.0 V
20 V
1.0 V
20 V
1.0 V
②
⑥
④
⑧
CT1 16
1.0 V
20 V
1.0 V
20 V
1.0 V
20 V
⑩
⑮
⑫
E̅0̅ 13
1.0 V
23 V
⑭
⑯
⑬
E̅1̅ 11
1.0 V
23 V
⑰
R/W1 7
10%
90%
10%
⑲
⑱
R/W2 6
10%
90%
10%
㉔
⑳
Vref
(5.0 V Nom.)
VPin 1 - VPin 2
(Ref. Voltage 0)
0.85 V Nom.
1.0 V Nom.
1.65 V Nom.
0.85 V Nom.

FIGURE 3 — R/W1 AND R/W2 RELATIONSHIP


Write Data 5
2.4 V
0.9 V
0.2 V
R/W1 7
10%
50%
90%
R/W2 6
10%
50%
90%
①
②
③
④
⑤
⑥
⑦
⑧

## APPLICATION INFORMATION

The MC3469P serves as a complete interface between the Write Control functional signals (Head Select, Write Data, Write Gate and inner track compensation, IRWS) and the head itself. A typical configuration is shown in Figure 4. $L_E$'s are erase coils.

### WRITE CURRENT SELECTION

Although the MC3469P has been specified for 3.0 mA write current (with a 10 kΩ external resistor), a range of write current values can be chosen by varying $R_{ext}$ using the plot in Figure 5. This current can also be derived using the relationship $I_{Write}\,(\mathrm{mA}) = \frac{30}{R_{ext}(\mathrm{k}\Omega)}$

**$I_{Ref}$, the current flowing in $R_{ext}$ (required only for dissipation calculations) can be worst case using the fact that the differential voltage between Pins 1 and 2 ($V_{Ref}$) shown in Figure 3 never exceeds 5.0 volts. With a low value of $R_{ext}$ = 1.0 kΩ, $P_D$ = 25 mW.**

### WRITE CURRENT DAMPING

Referring to Figure 4, resistors $R_D$ are used to dampen any ringing that results from applying the relatively fast risetime write current pulse to the inductive head load. Values chosen will be a funciton of head characteristics and the desired damping. $R_P$ serves as a common pullup resistor to the head supply $V_{BB}$.

FIGURE 4 — TYPICAL APPLICATION

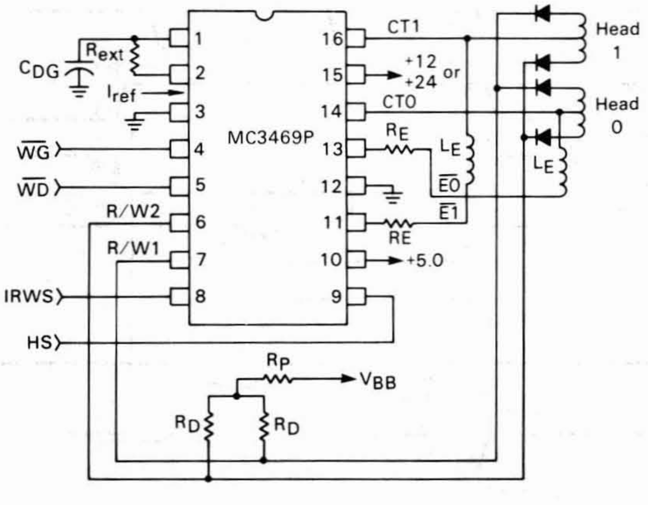
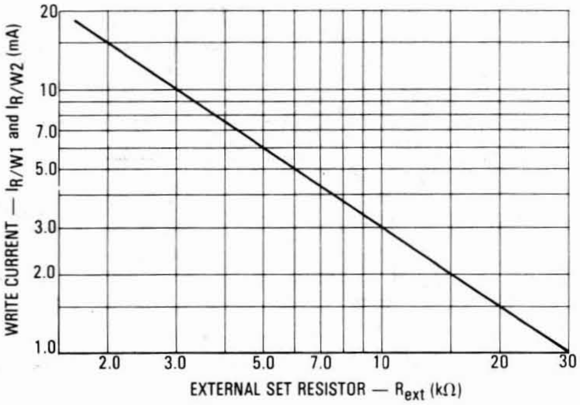

MC3469P
CDG
Rext
Iref
WG
WD
R/W2
R/W1
IRWS
HS
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
CT1
+12 or +24
CTO
RE
LE
E0
E1
RE
+5.0
Head 1
Head 0
LE
RP
VBB
RD
RD

FIGURE 5 — WRITE CURRENT versus $R_{ext}$



## DEGAUSS PERIOD

Degauss of the read/write head can be accomplished at the end of each write operation by attaching a capacitor from pin 1 to ground. The timing relationship that results is shown in Figure 7. A simplified diagram of this function is shown in Figure 6.

While $\overline{WG}$ is low, the selected write current flows into pin 6 or pin 7 (R/W1 or R/W2) and is mirrored through the external resistor, $R_{ext}$. The degauss capacitor, $C_{DG}$, will be charged to approximately 5.7 volts. After $\overline{WG}$ goes high, the voltage on $C_{DG}$ begins to decay toward 0.7 V. When the voltage reaches the comparator threshold of 1.7 V, the comparator output triggers the internal logic to completely turn off the write current. At this point, the pulse amplitude on the R/W1 and R/W2 pins has returned to 10% of its maximum value.

Figure 7, Degauss Period shows the relationship between $C_{DG}$ and Degauss Period for $R_{ext}$ = 10 kΩ. This period is equal to the exponential delay time for the voltage as mentioned plus some internal delay times.

## POWER-UP WRITE CURRENT CONTROL

During power-up, under certain conditions ($V_{BB}$ comes up first while $\overline{WG}$ is low), there can be a write current transient on Pins 6 and 7 (R/W1 and R/W2) of sufficient magnitude to cause writing to occur if the head is loaded.

This transient can be eliminated by placing a capacitor from Pin 2 to ground. This also delays the write current when $\overline{WG}$ goes low and this delay must be accounted for when the capacitor on Pin 2 is used. The delay is 3.0 μs for a 2700 pF capacitor, and $R_{ext}$ = 10 kΩ. Values up to 7000 pF may be used.

FIGURE 6 — SIMPLIFIED DEGAUSS CIRCUIT

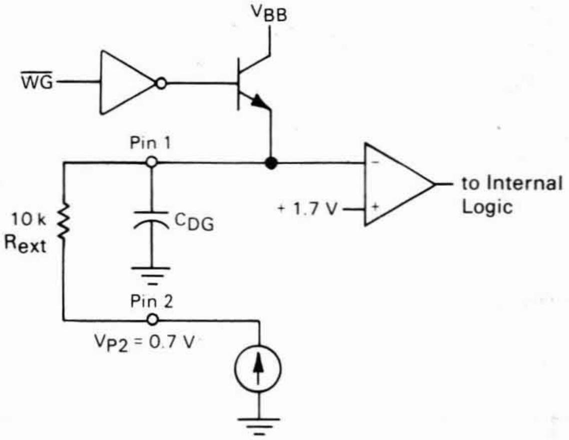


FIGURE 7 — DEGAUSS PERIOD versus CAPACITANCE ($C_{DG}$)

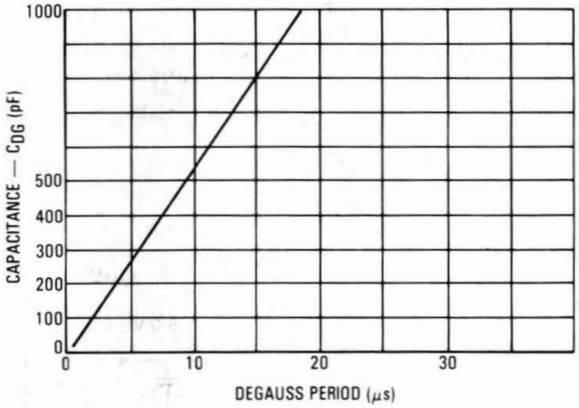
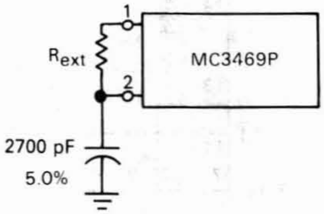
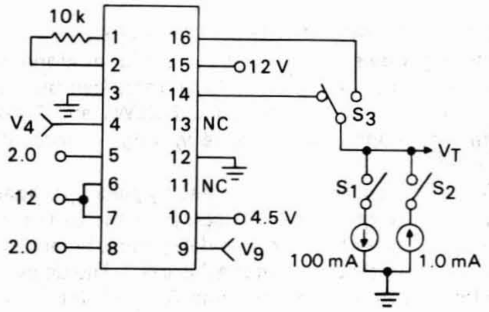


FIGURE 8 — TURN-ON WRITE PROTECTION



## TEST FIGURES

### FIGURE 9 — CENTER TAP OUTPUT VOLTAGE (PINS 14 AND 16)

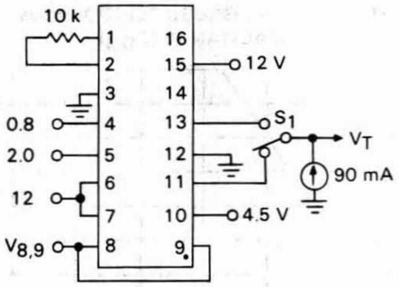

10 k
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
12 V
NC
NC
4.5 V
$V_4$
2.0
12
2.0
$V_9$
$S_3$
$V_T$
$S_1$
$S_2$
100 mA
1.0 mA

**CONDITIONS**

| Measure | Set | | | | |
|---|---|---|---|---|---|
| $V_T$ | $S_1$ | $S_2$ | $S_3$ | $V_4$* | $V_9$* |
| $V_{OH}$ (P14) | On | Off | P14 | 0.8 | 2.0 |
| | | | | 2.0 | 0.8 |
| $V_{OH}$ (P16) | On | Off | P16 | 2.0 | 2.0 |
| | | | | 0.8 | 0.8 |
| $V_{OL}$ (P14) | Off | On | P14 | 0.8 | 0.8 |
| | | | | 2.0 | 2.0 |
| $V_{OL}$ (P16) | Off | On | P16 | 2.0 | 0.8 |
| | | | | 0.8 | 2.0 |

*Volts

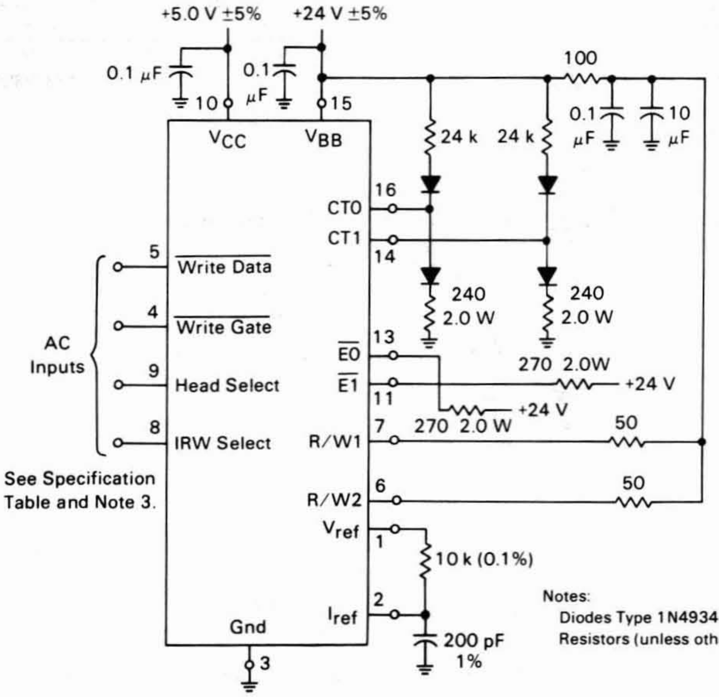
### FIGURE 10 — ERASE OUTPUT LOW VOLTAGE (PINS 11 AND 13)


10 k
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
12 V
0.8
2.0
12
$V_{8,9}$
4.5 V
$S_1$
$V_T$
90 mA

**CONDITIONS**

| Measure | Set | |
|---|---|---|
| $V_T$ | $S_1$ | $V_{8,9}$ |
| $V_{OL}$ (P11) | P11 | 0.8V |
| $V_{OL}$ (P13) | P13 | 2.0 V |

### FIGURE 11 — TIMING TEST CIRCUIT


+5.0 V ±5%
+24 V ±5%
0.1 μF
0.1 μF
10
15
$V_{CC}$
$V_{BB}$
100
0.1 μF
10 μF
24 k
24 k
16
CT0
CT1
14
240 2.0 W
240 2.0 W
5
Write Data
4
Write Gate
AC Inputs
9
Head Select
8
IRW Select
13
$\overline{E0}$
$\overline{E1}$
11
270 2.0W
+24 V
+24 V
7
270 2.0 W
50
R/W1
6
R/W2
50
$V_{ref}$
1
10 k (0.1%)
2
$I_{ref}$
200 pF 1%
Gnd
3

See Specification Table and Note 3.

Notes:
Diodes Type 1N4934.
Resistors (unless otherwise noted) are 1/4 W, 5%.

### ERASE CURRENT

The value of $R_E$, the erase current set resistor, is found by referring to Figure 12 and selecting the desired erase current.

Looking at the simplified erase current path in Figure 12, when writing, CTO will be high ($V_{OH(min)} = 21$ V) and EO will be low ($V_{OL(max)} = 0.6$ V). If the erase coil resistance is 10 Ω and 40 mA of erase current is desired, then:

$$(R_E + 10\ \Omega) \times 40\ \text{mA} = (21 - 0.6)\ \text{V}$$

or

$$R_E = \frac{20.4\ \text{V}}{0.04\ \text{A}} - 10\ \Omega = 500\ \Omega$$

$$P_D = (0.04)(20.4) = 0.816\ \text{W or } 1.0\ \text{W}$$

This gives the minimum value $R_E$ for worst case $V_{OH}/V_{OL}$ conditions. It is also recommended that a diode be used as required for inductive back emf suppression.

Erase timing is provided internally and is active during Write Gate low for the selected head.

**FIGURE 12 — ERASE CURRENT**
**($R_E$ Selection)**

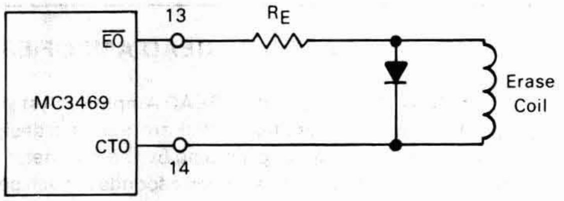
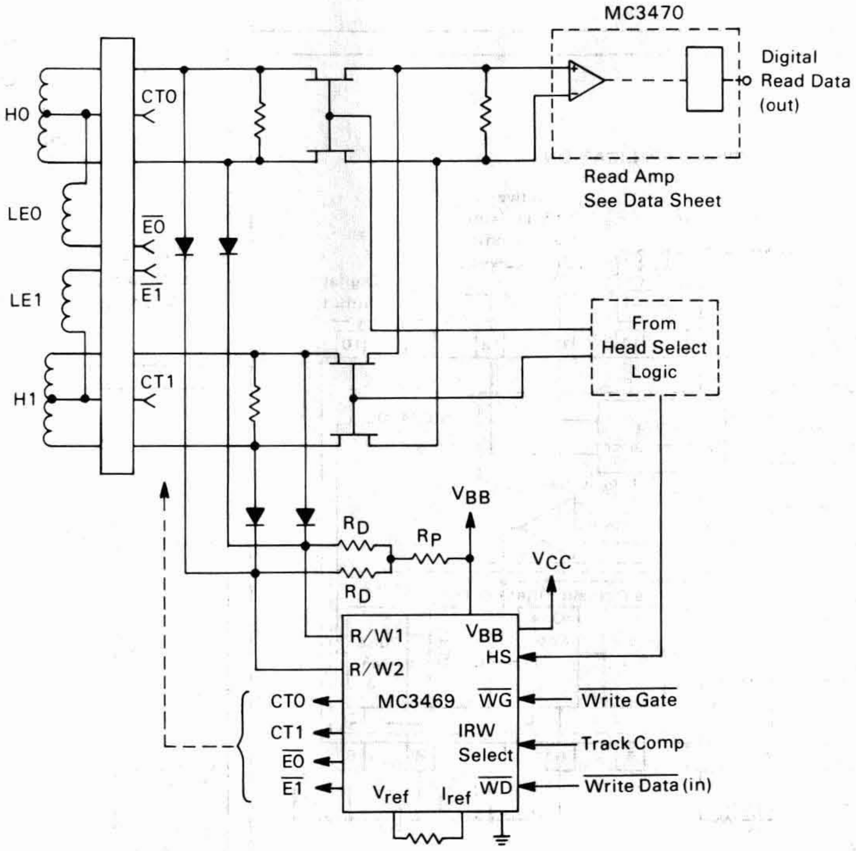

13
RE
EO
MC3469
CTO
14
Erase
Coil

**FIGURE 13 — TYPICAL DUAL HEAD FLOPPY DISK SYSTEM USING FET GATE READ CHANNEL SELECTION AND MC3469/MC3470**


MC3470
Digital
Read Data
(out)
Read Amp
See Data Sheet
HO
CTO
LEO
EO
E1
LE1
CT1
H1
From
Head Select
Logic
VBB
RD
RP
VCC
RD
R/W1
R/W2
VBB
HS
MC3469
WG
Write Gate
CTO
CT1
EO
E1
IRW
Select
Track Comp
Vref
Iref
WD
Write Data (in)

**MOTOROLA**

# MC3470P
# MC3470AP

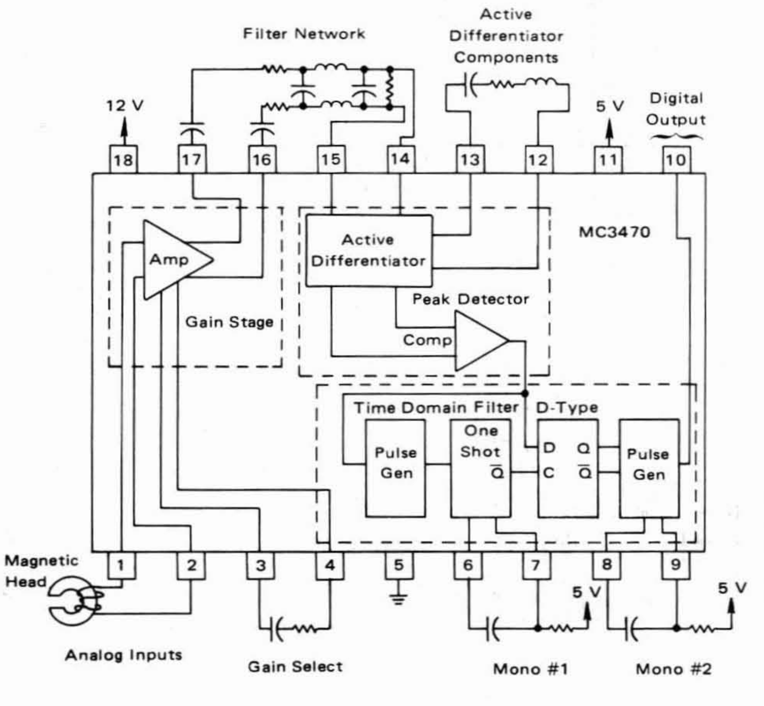
## Specifications and Applications Information

### FLOPPY DISK READ AMPLIFIER

The MC3470 is a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

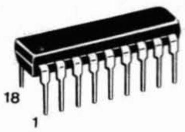
- Combines All the Active Circuitry To Perform the Floppy Disk Read Amplifier Function in One Circuit
- Guaranteed Maximum Peak Shift of 2.0% — MC3470A
- Improved (Positive) Gain $T_C$ and Tolerance
- Improved Input Common Mode

### TYPICAL APPLICATION


Filter Network
Active Differentiator Components
12 V
5 V
Digital Output
18
17
16
15
14
13
12
11
10
MC3470
Amp
Gain Stage
Active Differentiator
Peak Detector
Comp
Time Domain Filter
D-Type
Pulse Gen
One Shot
Q̄
D
Q
C
Q̄
Pulse Gen
Magnetic Head
1
2
3
4
5
6
7
8
9
5 V
5 V
Analog Inputs
Gain Select
Mono #1
Mono #2

## FLOPPY DISK READ AMPLIFIER SYSTEM

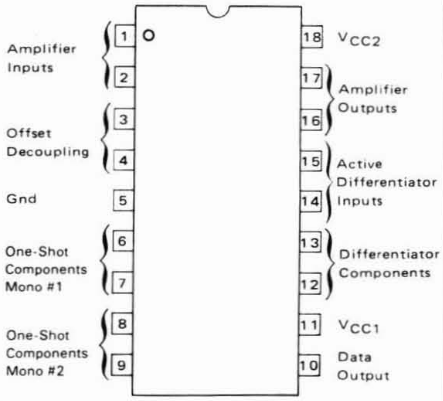
### SILICON MONOLITHIC INTEGRATED CIRCUIT



**P SUFFIX**
PLASTIC PACKAGE
CASE 707-02

**FN SUFFIX**
PLASTIC PACKAGE
CASE 775-01
PLCC-20*

***Surface Mount pin-out is different than standard package pin-out for this device. Please refer to Chapter 7 for details.**


Amplifier Inputs
1
2
Offset Decoupling
3
4
Gnd
5
One-Shot Components Mono #1
6
7
One-Shot Components Mono #2
8
9
18
VCC2
17
16
Amplifier Outputs
15
14
Active Differentiator Inputs
13
12
Differentiator Components
11
VCC1
10
Data Output

**ABSOLUTE MAXIMUM RATINGS** (Note 1) ($T_A$ = 25°C)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage (Pin 11) | $V_{CC1}$ | 7.0 | Vdc |
| Power Supply Voltage (Pin 18) | $V_{CC2}$ | 16 | Vdc |
| Input Voltage (Pins 1 and 2) | $V_I$ | -0.2 to +7.0 | Vdc |
| Output Voltage (Pin 10) | $V_O$ | -0.2 to +7.0 | Vdc |
| Operating Ambient Temperature | $T_A$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | -65 to +150 | °C |
| Operating Junction Temperature<br>Plastic Package | $T_J$ | 150 | °C |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**RECOMMENDED OPERATING CONDITIONS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | $V_{CC1}$ +4.75 to +5.25<br>$V_{CC2}$ +10 to +14 | Vdc |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |

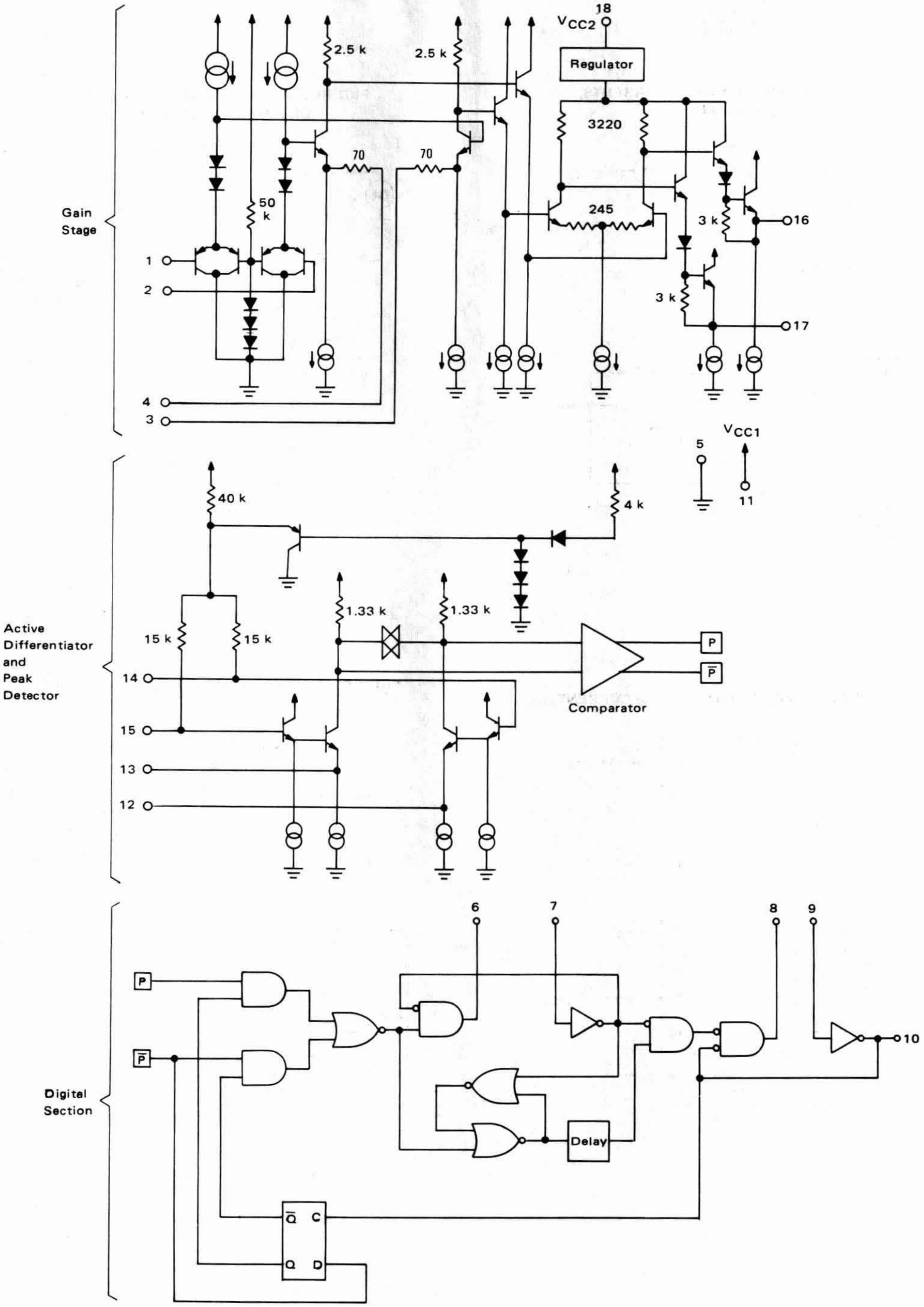
**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0 to +70°C, $V_{CC1}$ = 4.75 to 5.25 V, $V_{CC2}$ = 10 to 14 V unless otherwise noted)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Differential Voltage Gain MC3470<br>(f = 200 kHz, $V_{iD}$ = 5.0 mV(RMS)) MC3470A | 2 | $A_{VD}$ | 80<br>100 | 100<br>110 | 130<br>130 | V/V |
| Input Bias Current | 3 | $I_{IB}$ | — | -10 | -25 | μA |
| Input Common Mode Range Linear Operation<br>(5% max THD) | | $v_{iCM}$ | -0.1 | — | 1.5 | V |
| Differential Input Voltage Linear Operation<br>(5% max THD) | | $v_{iD}$ | — | — | 25 | mVp-p |
| Output Voltage Swing Differential | 2 | $v_{oD}$ | 3.0 | 4.0 | — | Vp-p |
| Output Source Current, Toggled | | $I_O$ | — | 8.0 | — | mA |
| Output Sink Current, Pins 16 and 17 | 4 | $I_{OS}$ | 2.8 | 4.0 | — | mA |
| Small Signal Input Resistance ($T_A$ = 25°C) | | $r_i$ | 100 | 250 | — | kΩ |
| Small Signal Output Resistance, Single-Ended<br>($T_A$ = 25°C, $V_{CC1}$ = 5.0 V, $V_{CC2}$ = 12 V) | | $r_o$ | — | 15 | — | Ω |
| Bandwidth, -3.0 dB ($v_{iD}$ = 2.0 mV(RMS), $T_A$ = 25°C<br>$V_{CC1}$ = 5.0 V, $V_{CC2}$ = 12 V) | 2, 17 | BW | 10 | — | — | MHz |
| Common Mode Rejection Ratio ($T_A$ = 25°C, f = 100 kHz, $A_{VD}$ = 40 dB, $v_{in}$ = 200 mVp-p, $V_{CC1}$ = 5.0 V, $V_{CC2}$ = 12 V) | 5 | CMRR | 50 | — | — | dB |
| $V_{CC1}$ Supply Rejection Ratio ($T_A$ = 25°C, $V_{CC2}$ = 12 V, $4.75 \leqslant V_{CC1} \leqslant 5.25$ V, $A_{VD}$ = 40 dB) | | — | 50 | — | — | dB |
| $V_{CC2}$ Supply Rejection Ratio ($T_A$ = 25°C, $V_{CC1}$ = 5.0 V, $10\text{ V} \leqslant V_{CC2} \leqslant 14$ V, $A_{VD}$ = 40 dB) | | — | 60 | — | — | dB |
| Differential Output Offset ($T_A$ = 25°C, $v_{iD}$ = $v_{in}$ = 0 V) | | $V_{DO}$ | — | — | 0.4 | V |
| Common Mode Output Offset ($v_{iD}$ = $V_{in}$ = 0 V,<br>Differential and Common Mode) | | $V_{CO}$ | — | 3.0 | — | V |
| Differential Noise Voltage Referred to Input<br>(BW = 10 Hz to 1.0 MHz, $T_A$ = 25°C) | 22 | $e_n$ | — | 15 | — | μV(RMS) |
| Supply Currents<br>($V_{CC1}$ = 5.25 V, $S_1$ to Pin 12 or Pin 13)<br>($V_{CC2}$ = 14 V) | 1 | <br>$I_{CC1}$<br>$I_{CC2}$ | <br>—<br>— | <br>40<br>4.8 | <br>—<br>— | mA |

**ELECTRICAL CHARACTERISTICS (continued)** ($T_A$ = 0 to +70°C, $V_{CC1}$ = 4.75 to 5.25 V, $V_{CC2}$ = 10 to 14 V unless otherwise noted)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **ACTIVE DIFFERENTIATOR SECTION** | | | | | | |
| Differentiator Output Sink Current, Pins 12 and 13 ($V_{OD}$ = $V_{CC1}$) | 6 | $I_{OD}$ | 1.0 | 1.4 | — | mA |
| Peak Shift (f = 250 kHz, $v_{iD}$ = 1.0 Vp-p, $i_{cap}$ = 500 μA,<br>where $PS = 1/2 \frac{t_{PS1} - t_{PS2}}{t_{PS1} + t_{PS2}} \times 100\%$, MC3470<br>$V_{CC1}$ = 5.0 V, $V_{CC2}$ = 12 V) MC3470A | 7, 8 | PS | <br>—<br>— | <br>—<br>— | <br>5.0<br>2.0 | % |
| Differentiator Input Resistance, Differential | | $r_{iD}$ | — | 30 | — | kΩ |
| Differentiator Output Resistance, Differential ($T_A$ = 25°C) | | $r_{oD}$ | — | 40 | — | Ω |
| **DIGITAL SECTION** | | | | | | |
| Output Voltage High Logic Level, Pin 10 ($V_{CC1}$ = 4.75 V, $V_{CC2}$ = 12 V, $I_{OH}$ = −0.4 mA) | 9 | $V_{OH}$ | 2.7 | — | — | V |
| Output Voltage Low Logic Level, Pin 10 ($V_{CC1}$ = 4.75 V, $V_{CC2}$ = 12 V, $I_{OL}$ = 8.0 mA) | 10 | $V_{OL}$ | — | — | 0.5 | V |
| Output Rise Time, Pin 10 | 11, 12 | $t_{TLH}$ | — | — | 20 | ns |
| Output Fall Time, Pin 10 | 11, 12 | $t_{THL}$ | — | — | 25 | ns |
| Timing Range Mono #1 ($t_{1A}$ and $t_{1B}$) | 13 | $t_{1A,\,B}$ | 500 | — | 4000 | ns |
| Timing Accuracy Mono #1<br>(t1 = 1.0 μs = 0.625 R1C1 + 200 ns)<br>(R1 = 6.4 kΩ, C1 = 200 pF)<br>Accuracy guaranteed for R1 in the range 1.5 kΩ ⩽ R1 ⩽ 10 kΩ and C1 in the range 150 pF ⩽ C1 ⩽ 680 pF.<br>Note: To minimize current transients, C1 should be kept as small as is convenient. | 12, 13 | $E_{t1}$ | 85 | — | 115 | % |
| Timing Range Mono #2 | 11, 12 | t2 | 150 | — | 1000 | ns |
| Timing Accuracy Mono #2<br>(t2 = 200 ns = 0.625 R2C2)<br>(R2 = 1.6 kΩ, C2 = 200 pF)<br>Accuracy guaranteed for 1.5 kΩ ⩽ R2 ⩽ 10 kΩ, 100 pF ⩽ C2 ⩽ 800 pF | 12, 13 | $E_{t2}$ | 85 | — | 115 | % |

MC3470 CIRCUIT SCHEMATIC



18
VCC2
Regulator
2.5 k
2.5 k
3220
70
70
245
50 k
3 k
3 k
16
17
Gain Stage
1
2
4
3
5
VCC1
11
40 k
4 k
1.33 k
1.33 k
15 k
15 k
P
P̄
Comparator
Active Differentiator and Peak Detector
14
15
13
12
6
7
8
9
10
Delay
Q̄
C
Q
D
Digital Section

FIGURE 1 – POWER SUPPLY CURRENTS, $I_{CC1}$ AND $I_{CC2}$

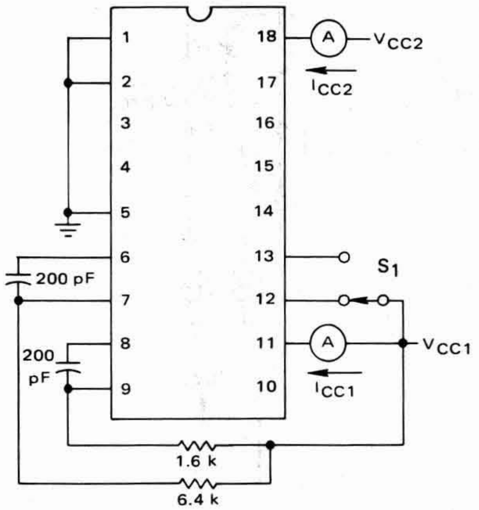

1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
A
$V_{CC2}$
$I_{CC2}$
$S_1$
A
$V_{CC1}$
$I_{CC1}$
200 pF
200 pF
1.6 k
6.4 k

FIGURE 2 – VOLTAGE GAIN, BANDWIDTH, OUTPUT VOLTAGE SWING

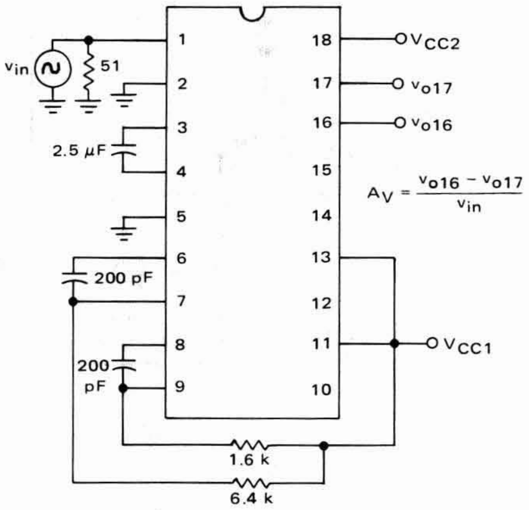

$v_{in}$
51
2.5 μF
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
$V_{CC2}$
$v_{o17}$
$v_{o16}$
$A_V = \frac{v_{o16} - v_{o17}}{v_{in}}$
$V_{CC1}$
200 pF
200 pF
1.6 k
6.4 k

FIGURE 3 – AMPLIFIER INPUT BIAS CURRENT, $I_{IB}$

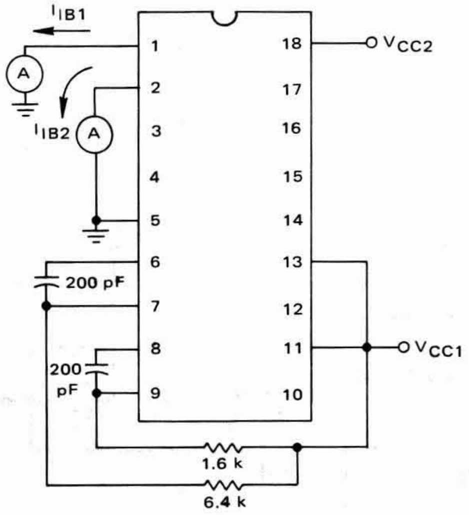

$I_{IB1}$
A
$I_{IB2}$
A
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
$V_{CC2}$
$V_{CC1}$
200 pF
200 pF
1.6 k
6.4 k

FIGURE 4 – AMPLIFIER OUTPUT SINK CURRENT, PINS 16 AND 17

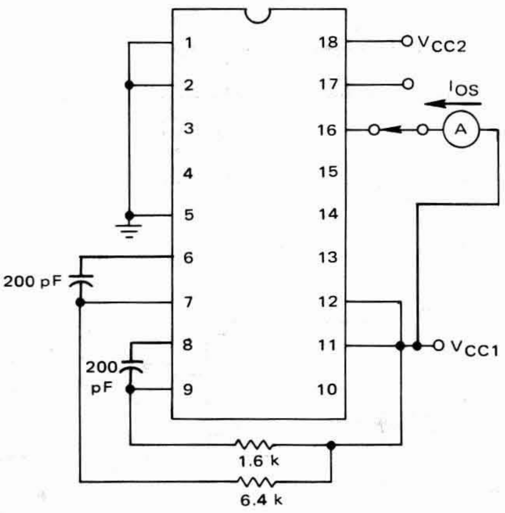
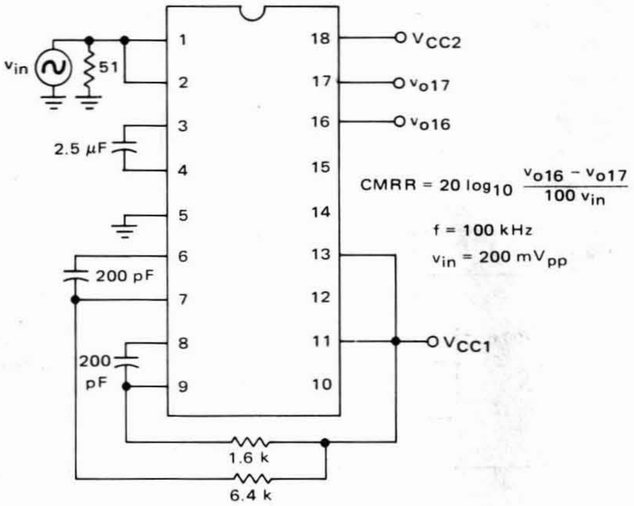

1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
$V_{CC2}$
$I_{OS}$
A
$V_{CC1}$
200 pF
200 pF
1.6 k
6.4 k

**FIGURE 5 – AMPLIFIER COMMON MODE REJECTION RATIO, CMRR**



$v_{in}$
51
2.5 μF
200 pF
200 pF
1.6 k
6.4 k
$V_{CC2}$
$v_{o17}$
$v_{o16}$
$V_{CC1}$
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10

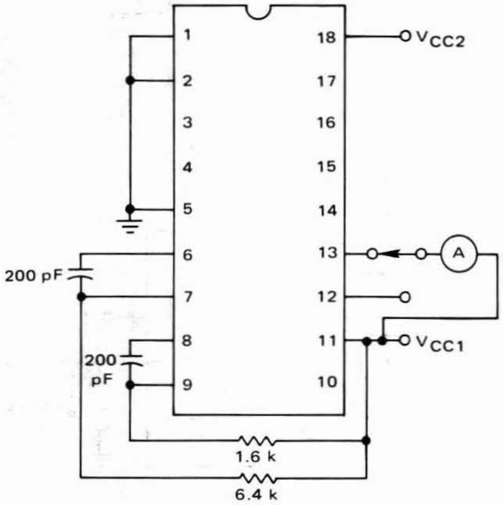
$$CMRR = 20 \log_{10} \frac{v_{o16} - v_{o17}}{100\ v_{in}}$$

f = 100 kHz

$v_{in}$ = 200 mV$_{pp}$

NOTE: Measurements may be made with vector voltmeter hp 8405A or equivalent at 1.0 MHz to guarantee 100 kHz performance.

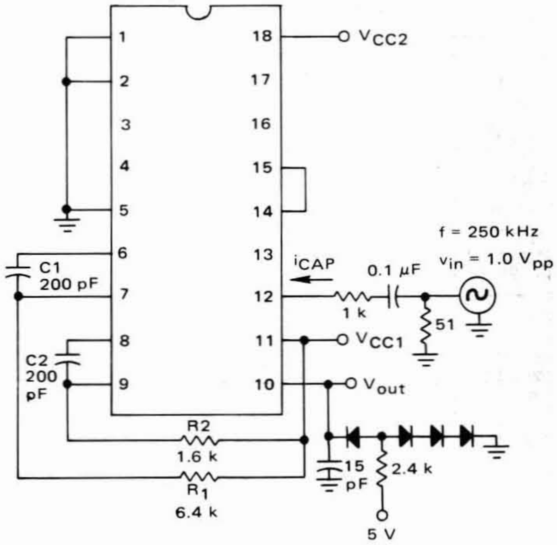
**FIGURE 6 – DIFFERENTIATOR OUTPUT SINK CURRENT, PINS 12 AND 13**



$V_{CC2}$
A
$V_{CC1}$
200 pF
200 pF
1.6 k
6.4 k
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10

**FIGURE 7 – PEAK SHIFT, PS**

See Figure 8 for Output Waveform



$V_{CC2}$
C1 200 pF
C2 200 pF
$i_{CAP}$
0.1 μF
1 k
51
$v_{in}$
$V_{CC1}$
$V_{out}$
R2 1.6 k
R1 6.4 k
15 pF
2.4 k
5 V
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10

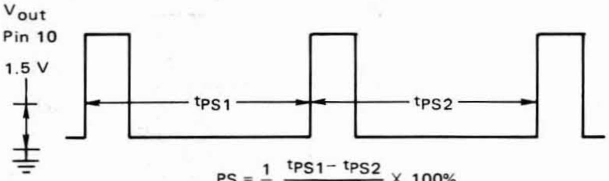
f = 250 kHz

$v_{in}$ = 1.0 V$_{pp}$

**FIGURE 8 – PEAK SHIFT, PS**

$V_{in}$ = 1.0 V$_{pp}$ f = 250 kHz

Test schematic on Figure 7



$V_{out}$ Pin 10
1.5 V
$t_{PS1}$
$t_{PS2}$

$$PS = \frac{1}{2}\ \frac{t_{PS1} - t_{PS2}}{t_{PS1} + t_{PS2}} \times 100\%$$

FIGURE 9 – DATA OUTPUT VOLTAGE HIGH, PIN 10

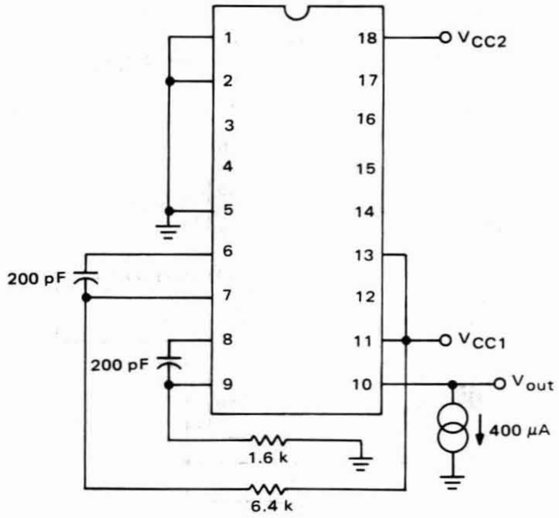

1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
$V_{CC2}$
$V_{CC1}$
$V_{out}$
200 pF
200 pF
1.6 k
6.4 k
400 μA

FIGURE 10 – DATA OUTPUT VOLTAGE LOW, PIN 10

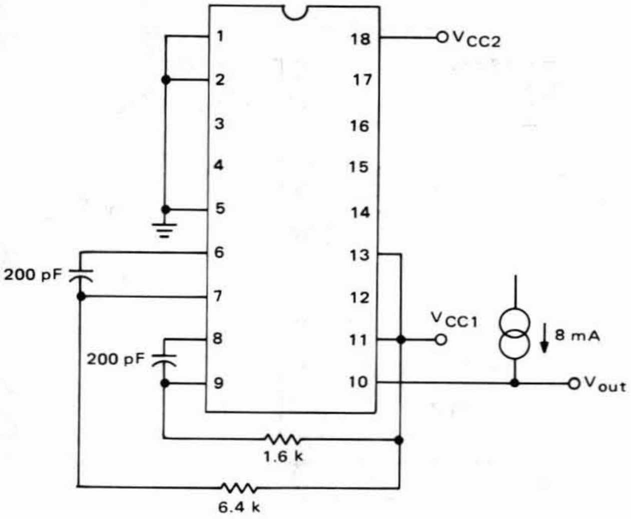
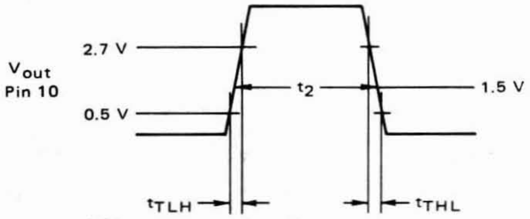

1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
$V_{CC2}$
$V_{CC1}$
$V_{out}$
200 pF
200 pF
8 mA
1.6 k
6.4 k

FIGURE 11 – DATA OUTPUT RISE TIME, $t_{TLH}$
DATA OUTPUT FALL TIME, $t_{THL}$
TIMING ACCURACY MONO #2, $E_{t2}$

$V_{in}$ is same as shown on Figure 13, test schematic on Figure 12


$V_{out}$
Pin 10
2.7 V
0.5 V
1.5 V
$t_2$
$t_{TLH}$
$t_{THL}$

$$E_{t2} = \frac{t_2}{200\text{ ns}} \times 100\%$$

FIGURE 12 – TIMING ACCURACY, $E_{t1}$ AND $E_{t2}$
DATA OUTPUT RISE AND FALL TIMES, $t_{TLH}$ AND $t_{THL}$

$V_{in}$ shown on Figure 13

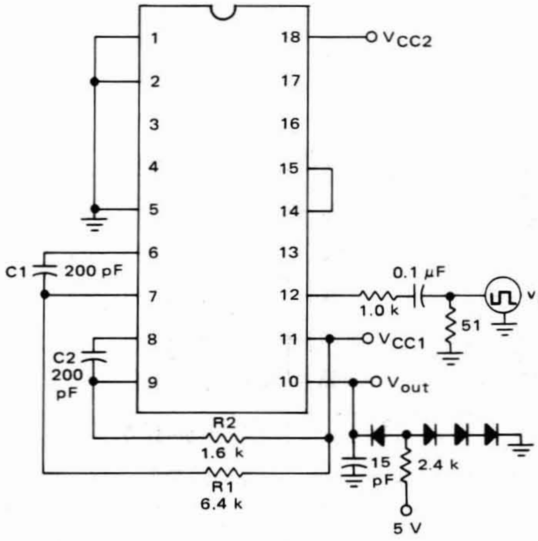
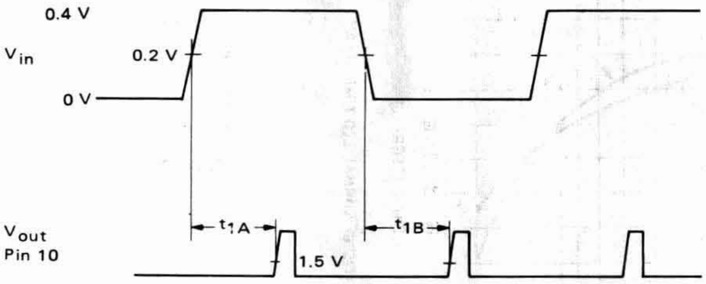

1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
$V_{CC2}$
$V_{CC1}$
$V_{out}$
$V_{in}$
C1
200 pF
C2
200
pF
0.1 μF
1.0 k
51
R2
1.6 k
R1
6.4 k
15
pF
2.4 k
5 V

**FIGURE 13 – TIMING ACCURACY MONO #1, $E_{t1}$**

$t_{TLH} = t_{THL} < 10$ ns f = 250 kHz 50% Duty Cycle

Test Schematic on Figure 12

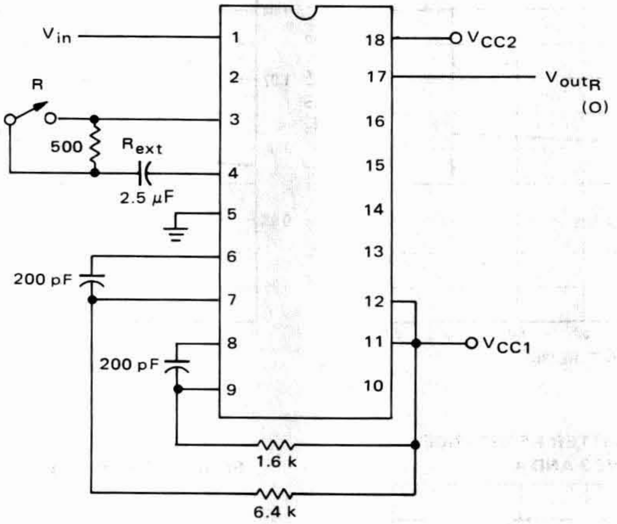

0.4 V
$V_{in}$
0.2 V
0 V
$V_{out}$
Pin 10
$t_{1A}$
$t_{1B}$
1.5 V

$$E_{t1A} = \frac{t_{1A}}{1000\ \text{ns}} \times 100\%$$

$$E_{t1B} = \frac{t_{1B}}{1000\ \text{ns}} \times 100\%$$

**FIGURE 14 – AMPLIFIER OFFSET DECOUPLING IMPEDANCE, PINS 3 AND 4**

$R_e + r_e$ and $A_V$ with $R_{ext} = 500\ \Omega$


$V_{in}$
R
500
$R_{ext}$
2.5 µF
200 pF
200 pF
1.6 k
6.4 k
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
$V_{CC2}$
$V_{outR}$
(O)
$V_{CC1}$

f = 250 kHz

$V_{in}$ = 5 mV(RMS)

$$\frac{A_{VD}}{2} = \frac{V_{out}}{V_{in}}$$

$$r_e + R_e = \frac{R_{ext}}{2\left(\frac{A_{V_O}}{A_{V_R}} - 1\right)} = \frac{500\ \Omega}{2\left(\frac{V_{out_O}}{V_{out_R}} - 1\right)}$$

**FIGURE 15 – NORMALIZED POWER SUPPLY CURRENT ($I_{CC}/I_{CC}$ 25°C) versus TEMPERATURE**

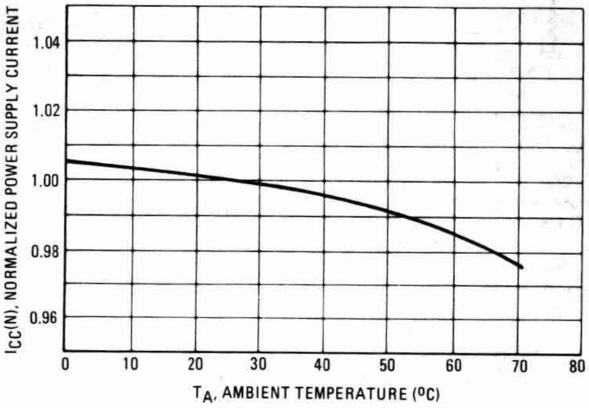


**FIGURE 16 – NORMALIZED VOLTAGE GAIN ($A_V/A_V$ 25°C) versus TEMPERATURE**

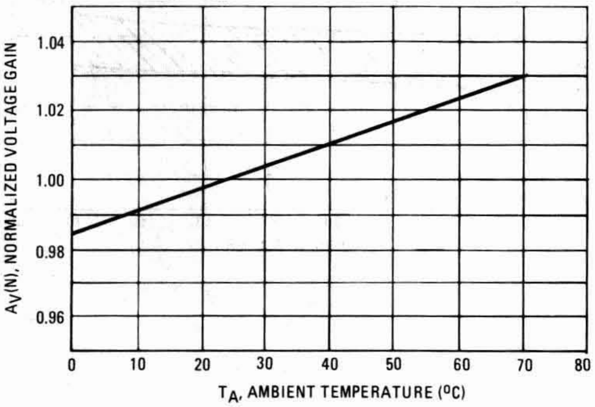


**FIGURE 17 – PHASE AND NORMALIZED VOLTAGE GAIN versus FREQUENCY**

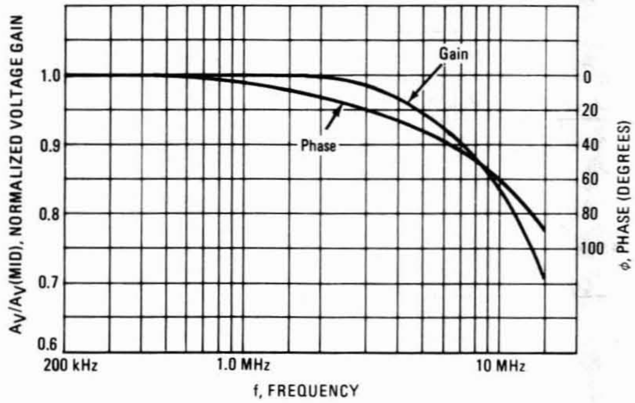


**FIGURE 18 – NORMALIZED TIME DELAY $t_1$ versus TEMPERATURE**

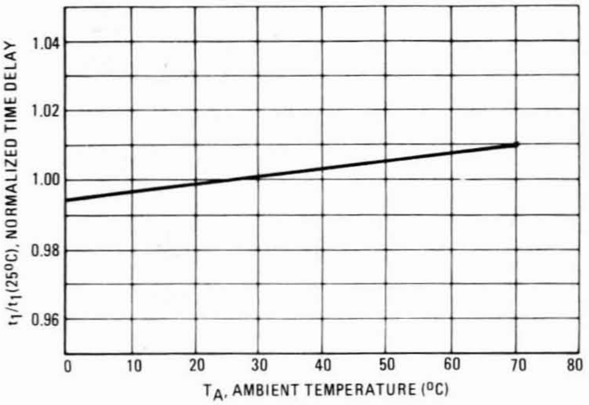


**FIGURE 19 – NORMALIZED OUTPUT PULSE WIDTH, $t_2/t_2$ 25°C**

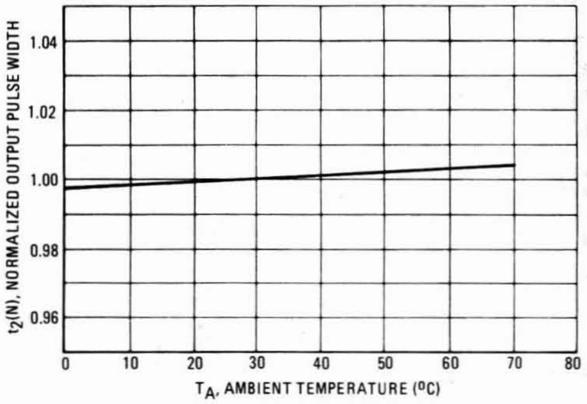


**FIGURE 20 – NORMALIZED VOLTAGE GAIN, $A_{VR}/A_{VR}$ 25°C**

See Figure 14, Switch Position R

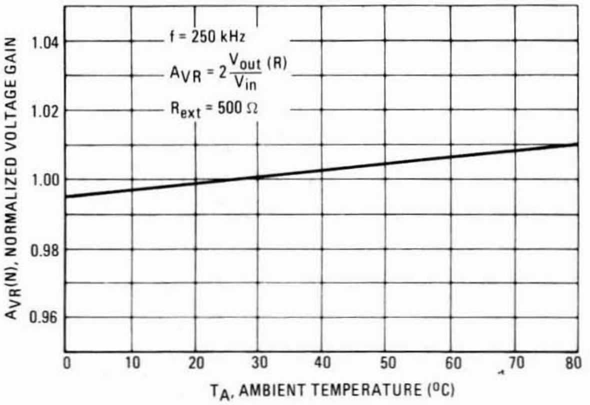


**FIGURE 21 – EFFECTIVE EMITTER RESISTANCE DISTRIBUTION, PINS 3 AND 4**

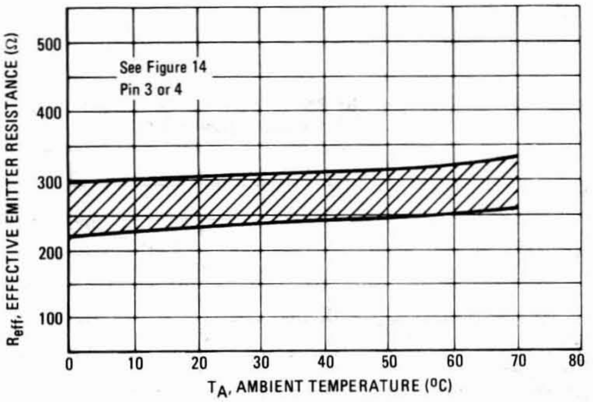
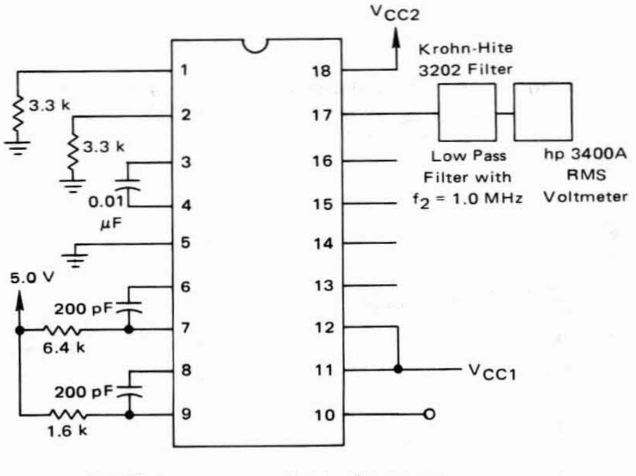


**FIGURE 22 – DIFFERENTIAL NOISE VOLTAGE**

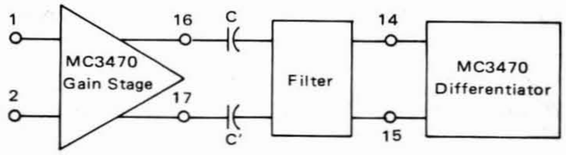

$V_{CC2}$
Krohn-Hite 3202 Filter
Low Pass Filter with $f_2$ = 1.0 MHz
hp 3400A RMS Voltmeter
3.3 k
3.3 k
0.01 µF
5.0 V
200 pF
6.4 k
200 pF
1.6 k
$V_{CC1}$
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10

NOTE: Assume uncorrelated noise sources
$e_n$ (differential noise at input) = $e_o\sqrt{2/100}$

## APPLICATION INFORMATION

The MC3470 is designed to accept a differential ac input from the magnetic head of a floppy disk drive and produce a digital output pulse that corresponds to each peak of the ac input. The gain stage amplifies the input waveform and applies it to a filter network (Figure 23a), enabling the active differentiator and time domain filter to produce the desired output.

FIGURE 23a – BLOCKING CAPACITORS USED TO ISOLATE THE DIFFERENTIATOR



### FILTER CONSIDERATIONS

The filter is used to reduce any high frequency noise present on the desired signal. Its characteristics are dictated by the floppy disk system parameters as well as the coupling requirements of the MC3470. The filter design parameters are affected by the read head characteristics, maximum and minimum slew rates, system transient response, system delay distortion, filter center frequency, and other system parameters. This design criteria varies between manufacturers; consequently, the filter configuration also varies. The coupling requirements of the MC3470 are a result of the output structure of the gain stage and the input structure of the differentiator, and must be adhered to regardless of the filter configuration.

The differentiator has an internal biasing network on each input. Therefore, any dc voltage applied to these inputs will perturbate the bias level. Disturbing the bias level does not affect the waveform at the differentiator inputs, but it does cause peak shifting in the digital output (Pin 10). Since the output of the gain stage has an associated dc voltage level, it, as well as any biasing introduced in the filter, must be isolated from the differentiator via series blocking capacitors. The transient response is minimized if the blocking capacitors C and C′ are placed before the filter as shown in Figure 23a. The charging and discharging of C and C′ is controlled by the filter termination resistor instead of the high input impedance of the differentiator.

The filter design must also include the current-sinking capacity of the amplifier output. The current source in the output structure (see circuit schematic — Pins 16 and 17) is guaranteed to sink a current of 2.8 mA. If the current requirement of the filter exceeds 2.8 mA, the current source will saturate, the output waveform will be distorted, and inaccurate peak detection will occur in the differentiator. Therefore, the total impedance of the filter must be greater than $Z_{min}$ as calculated from

$$Z_{min} = \frac{(E_pA_{VD})\ max}{2.8\ mA}$$

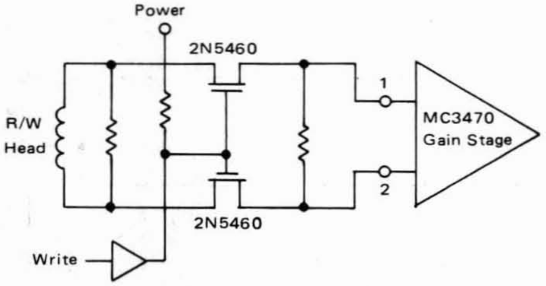
where $E_p$ is the peak differential input voltage to the MC3470.

### TRANSIENT RESPONSE

The worst-case transient response of the read channel occurs when dc switching at the amplifier input causes its output to be toggled. The dc voltage changes are a consequence of diode switching that takes place when control is transferred from the write channel to the read channel.

If the diode network is balanced, the dc change is a common mode input voltage to the amplifier. The switching of an unbalanced diode network creates a differential input voltage and a corresponding amplified swing in the outputs. The output swing will charge the blocking capacitor resulting in peak shifting in the digital output until the transient has decayed. Eliminating the differential dc changes at the amplifier input by matching the diode network or by coupling the read head to the amplifier via FET switches, as shown in Figure 23b, will minimize the filter transient response.

FIGURE 23b – FET SWITCHES USED TO COUPLE THE R/W HEAD TO THE MC3470



Two of the advantages FET switches have over diode switching are:

1. They isolate the read channel from dc voltage changes in the system; therefore, the transient response of the filter does not influence the system transient response.
2. The low voltage drop across the FETs keeps the input signal below the amplifier's internal clamp voltage; whereas, the voltage dropped across a diode switching network adds a dc bias to the input signal which may exceed the clamp voltage.

### AMPLIFIER GAIN

For some floppy systems, it may become necessary to either reduce the gain of the amplifier or reduce the

**See Application Note AN917 for further information.**

signal at the input to avoid exceeding the output swing capability of the amplifier. The voltage gain of the amplifier can be reduced by putting a resistor in series with the capacitor between Pins 3 and 4 (Figure 14). The relationship between the gain and the external resistor is given by

$$A_{VR} = A_{VO} \cdot \frac{2\,(r_e + R_e)}{2\,(r_e + R_e) + R_{ext}}$$

where $A_{VO} \triangleq$ voltage gain with the external resistor = 0,
$A_{VR} \triangleq$ voltage gain with the external resistor in,
$R_{ext} \triangleq$ the external resistor, and
$r_e + R_e \triangleq$ the resistance looking into Pin 3 or Pin 4.

Thus,

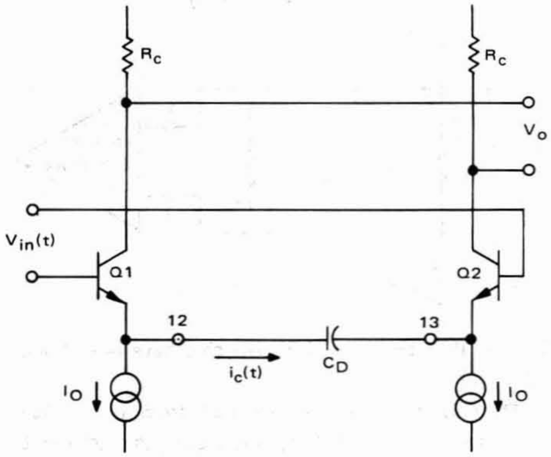
$$R_{ext} = 2\left(\frac{A_{VO}}{A_{VR}} - 1\right)(r_e + R_e).$$

A plot of $(r_e + R_e)$ versus temperature is shown in Figure 21. Figure 20 shows the normalized voltage gain versus temperature with the external resistor equal to 500 ohms.

## ACTIVE DIFFERENTIATOR

The active differentiator in the MC3470 (simplified circuit shown in Figure 24), is implemented by coupling the emitters of a differential amplifier with a capacitor resulting in a collector current that will be the derivative of the input voltage,

FIGURE 24 – ACTIVE DIFFERENTIATOR NETWORK



$$I = C\,dv/dt$$

If the output voltage is taken across a resistor through which the collector current is flowing, the resulting voltage will be the derivative of the input voltage.

$$V_o = 2Ri_c = 2RC\frac{dv_{in}(t)}{dt}$$

$V_o$ is applied to a comparator which will provide zero crossing detection of the current waveform. Since the capacitor shifts the current 90° from the input voltage, the comparator performs peak detection of the input voltage.

The following terms will be used in determining the value of C to be used in the differentiator:

$E_p \triangleq$ peak differential voltage applied to MC3470 amplifier input.
$E_p \sin \omega t \triangleq$ voltage waveform applied to MC3470 amplifier input (for purposes of discussion, assume a sine wave).
$A_{VD} \triangleq$ differential voltage gain of input amplifier.
$v_{in}(t) \triangleq$ differential voltage waveform applied to the differentiator inputs.
$= E_p A_{VD} \sin \omega t$ (Note: The filter is assumed to be lossless.)
$i_c(t) \triangleq$ current through capacitor $C_D$.
$R_O \triangleq$ output resistance of Q1 (Q2) at Pin 12 (13).

If $v_{in}(t) = E_p A_{VD} \sin \omega t$, then the current through the capacitor $C_D$ is given by

$$i_c(t) = C_D A_{VD} E_p \omega \cos \omega t$$

$$\text{and } V_O(t) = 2R_C C_D A_{VD} E_p \omega \cos \omega t.$$

Accurate zero crossing detection of $V_O(t)$ [peak detection of $v_{in}(t)$] occurs when the current waveform $i_c(t)$ crosses through zero in a minimum amount of time. This condition is satisfied by maximizing current slew rate. For a given value of $\omega$, the maximum slew rate occurs for the maximum value of $i_c$ or $\cos \omega t = 1$. Therefore,

$$i_c = C_D A_{VD} E_p \omega$$

The MC3470 current-sourcing capacity will determine the maximum value $i_c$; therefore, $C_D$ must be chosen such that the maximum $i_c$ occurs at the maximum $A_{VD} E_p \omega$ product.

$$C_D = \frac{i_{c\,max}}{(A_{VD} E_p \omega)_{max}} = \frac{1\text{ mA}}{(120)(E_p \omega)_{max}}$$

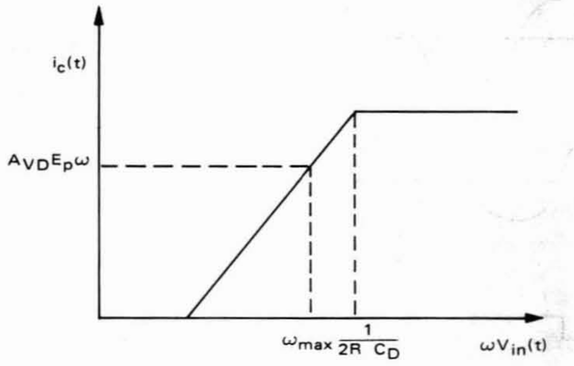
If the peak value specified for $i_c$ is exceeded, the current source ($I_O$ in Figure 24) will saturate and distort the waveform at Pins 12 and 13. Consequently, the differentiator will not accurately locate the peaks and peak shifting will occur in the digital output.

The effective output resistance $R_O$ of Q1 (Q2) will create a pole (as shown in Figure 25) at $1/2\,R_O C_D$. If this pole is ten times greater than the maximum operating frequency ($\omega_{max}$), the phase shift approaches 84°. Locating the pole at a frequency much greater than 10 $\omega_{max}$ needlessly extends the noise bandwidth thus:

$$2R_O = \frac{1}{C_D\, 10\, \omega_{max}}.$$

If $R_O$ is not large enough to satisfy this condition, a series

FIGURE 25 – RESPONSE OF DIFFERENTIATOR USING ONLY $C_D$

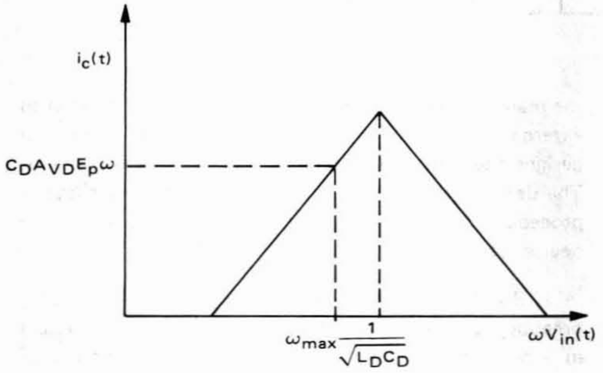


resistor can be added so that

$$R = 2R_O + R_D = \frac{1}{C_D\,10\,\omega_{max}}.$$

To further reduce the noise bandwidth, a second pole can be added (as shown in Figure 26) by putting an inductor in series with the resistor and the capacitor. The values of R and L are determined by choosing the center frequency ($\omega_o$) and the damping ratio ($\delta$) to meet the systems requirements where

FIGURE 26 – COMPLETE RESPONSE OF DIFFERENTIATOR



$$\omega_o = \frac{1}{\sqrt{LC_D}}$$

$$\delta = \frac{RC_D}{2\sqrt{LC_D}}$$

$$\omega_o = 10\,\omega_{max} = \frac{1}{\sqrt{LC_D}}$$

where $C_D$ is chosen for maximum $i_c$ as shown previously.

Solving for L gives:

$$L = \frac{1}{100\,C_D(\omega_{max})^2}$$

Using this value for L gives:

$$\delta = \frac{RC_D}{\frac{2}{10}\sqrt{\frac{C_D}{C_D(\omega_{max})^2}}}$$

Solving for R gives:

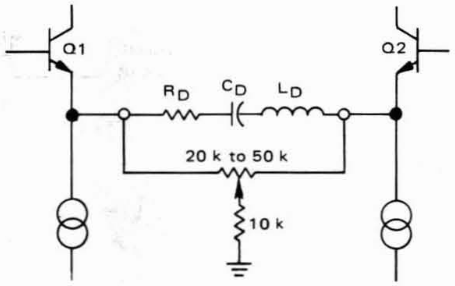
$$R = \frac{\delta}{5\,C_D\,\omega_{max}}$$

The total resistance (R) is the effective output resistance ($R_O$) plus the resistor added in the differentiator ($R_D$). Values of $\delta$ from 0.3 to 1 produce satisfactory results.

## PEAK SHIFT CONSIDERATIONS

Peak shift, resulting from current imbalance in the differentiator, offset voltage in the comparator, etc., can be eliminated by nulling the current in the emitters of the differentiator with a potentiometer as shown in Figure 27.

FIGURE 27 – PEAK SHIFT COMPENSATION



The potentiometer across the differentiator components is adjusted until a symmetrical digital output cycle is obtained at Pin 10 for a sinusoidal input with the minimum anticipated $E_p\omega$ product.

## DESIGN EQUATIONS FOR ONE-SHOTS

As shown in Figure 28, the MC3470 input waveform may have distortion at zero crossing, which can result in false triggering of the digital output. The time domain filter in the MC3470 can be used to eliminate the distortion by properly setting the period ($t_1$) of the one-shot timing elements on Pins 6 and 7. The following equation will optimize immunity to this signal distortion at zero crossing of the read head signal.

The timing equation for the time domain filter's one-shot is:

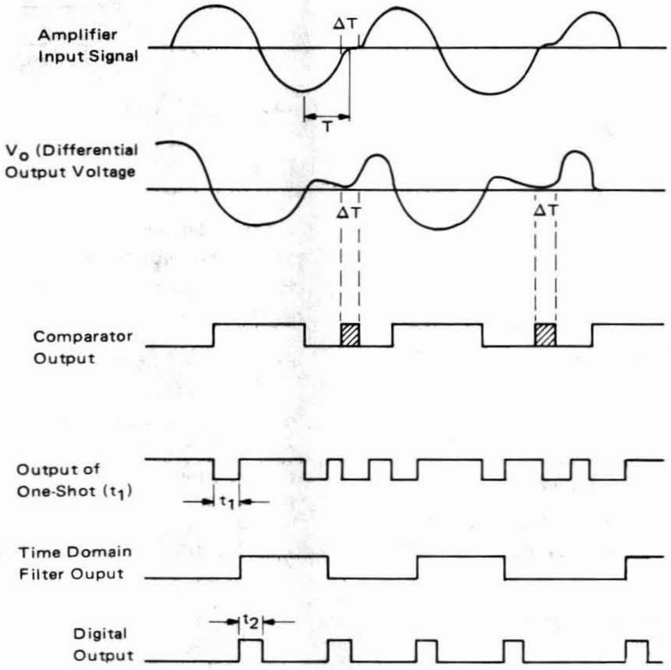
$$t_1 = R_1C_1K_1 + T_o$$

where $K_1 = 0.625$, $T_o = 200$ ns.

Actual time will be within ±15% of $t_1$ due to variations in the MC3470.

If $\Delta T$ is the maximum period of distortion (see Figure

FIGURE 28 – WAVEFORMS THROUGH THE READ CIRCUIT



28), then choose $t_1$ such that

$$\Delta T < t_1 < T - \frac{\Delta T}{2}$$

where $T = \frac{1}{4f_{(max)}}$.

The width of the digital output pulse $t_2$ (Pin 10) is determined by

$$t_2 = R_2C_2K_2$$

where $K_2 = 0.625$.

Actual pulse width will be within ±15% of $t_2$ due to variations in the MC3470.

To preserve the specified accuracy of the MC3470, $R_1$, $R_2$, $C_1$, and $C_2$ should remain in the ranges shown in the Electrical Characteristics. Also, to minimize current transients, it is important to keep the values of $C_1$ and $C_2$ as small as is convenient. For $t_1$ = 1 μs and $t_2$ = 200 ns, suggested good values for the capacitors are

$$C_1 = 250 \text{ pF}$$

$$C_2 = 160 \text{ pF}$$

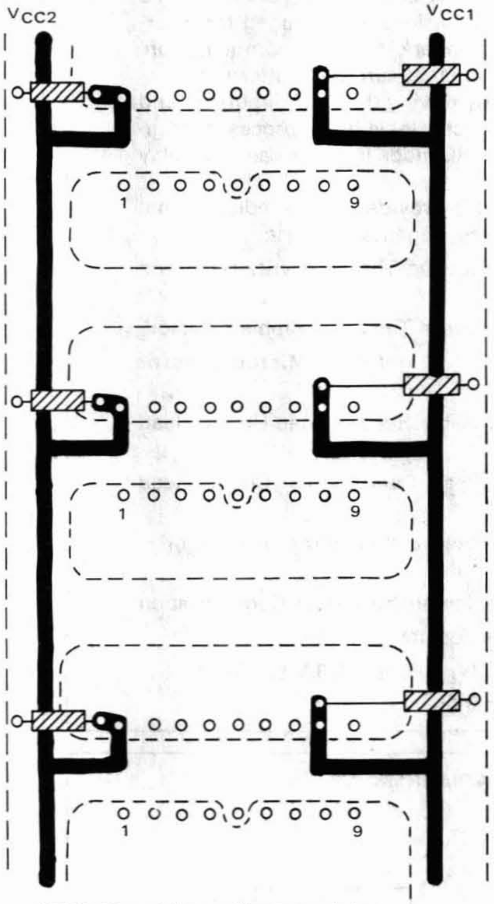
## BOARD LAYOUT AND TESTING CONSIDERATIONS

An LSI package has many input/output pins in close proximity, some carrying high level signals and others low level signals. As carefully as the on-chip isolation of the devices connected to these pins is implemented by the manufacturer, the coupling of signals or noise between external wires is under the control of the end-user who designs the integrated circuit into a piece of equipment. The designer should be familiar with the following layout procedures which will optimize the performance of the device. See Figure 29.

1. Build all circuits on printed circuit boards (including breadboards). Transmission line theory for flat conductors in a plane quite convincingly proves that coupling is far less than for round conductors in three dimensions.
2. Use a ground plane under the IC and over as much of the printed circuit board surface as possible without exceeding practical limits.
3. Avoid signal runs under the IC. Also avoid parallel runs of 1 inch or greater on the opposite or same side of board.
4. Use monolithic ceramic 0.1 μF capacitors for decoupling power supply transients: one from $V_{CC1}$ to ground and one from $V_{CC2}$ to ground for each IC package. Keep lead lengths to 1/4 inch or less and place in close proximity to the IC.
5. Keep all signal runs as short as possible.

When evaluating the device for phase jitter and frequency response, a special test jig should be designed to reduce ground loops and coupling caused by instrumentation. Instrumentation test setups must be calibrated at each test frequency and differential equipment utilized where required. A valid evaluation of the performance of any read amplifier chain requires considerable care and thought.

FIGURE 29 – POWER AND GROUND DISTRIBUTION FOR MC3470 PRINTED CIRCUIT BOARD LAYOUT



NOTE: Dotted lines outline ground plane on back side of printed circuit board.

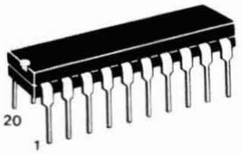
**MOTOROLA**

# MC3471P

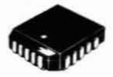
## Specifications and Applications Information

### FLOPPY DISK WRITE CONTROLLER (WITH ERASE DELAY)

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



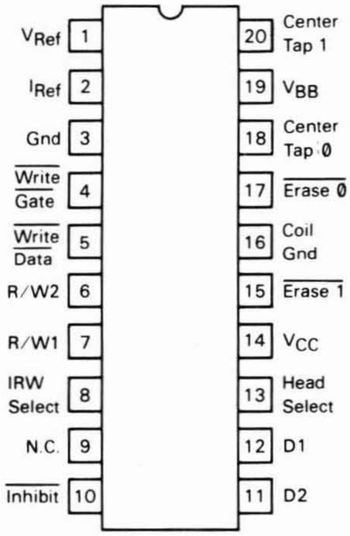
**P SUFFIX**
PLASTIC PACKAGE
CASE 738-02



**FN SUFFIX**
PLASTIC PACKAGE
CASE 775-01
PLCC-20*

***Surface Mount pin-out is different than standard package pin-out for this device. Please refer to Chapter 7 for details.**

**PIN CONNECTIONS**


$V_{Ref}$ 1
$I_{Ref}$ 2
Gnd 3
Write Gate 4
Write Data 5
R/W2 6
R/W1 7
IRW Select 8
N.C. 9
Inhibit 10
20 Center Tap 1
19 $V_{BB}$
18 Center Tap 0
17 Erase 0
16 Coil Gnd
15 Erase 1
14 $V_{CC}$
13 Head Select
12 D1
11 D2

(Top View)

### FLOPPY DISK WRITE CONTROLLER/HEAD DRIVER

The MC3471 is a monolithic integrated Write Controller/Head Driver designed to provide the entire interface between the write data and head control signals and the heads (write and erase) for either Tunnel or straddle-erase floppy disk systems.

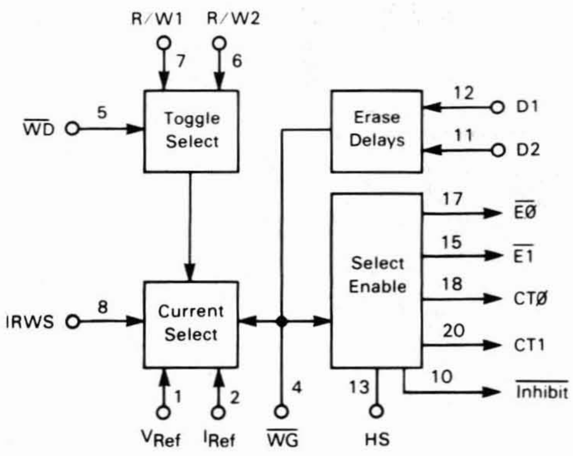
Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off.

Erase Delays are controlled by driving the delay inputs D1 and D2 with standard TTL open-collector logic (microprocessor compatible) or by using the external RC mode in which case the delay is one $\tau$ (K factor = 1.0).

In addition, an Inhibit output is provided which indicates that the heads are active during write, degauss, or erase.

- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Adjustable On-Chip Delay of Erase Timing — Stable K Factor
- Delay Pins Logic Compatible for Direct Microprocessor Compatibility
- Inhibit Output Provided to Disable Read or Step During Head Active Time
- Provides High Impedance (Read Data Enable) During Read Mode
- Head Current (Write) Guaranteed ±3% (3.0 mA using $R_{ext}$ = 10 kΩ)
- IRW Select Input Provides for Innter/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified With Head Supply ($V_{BB}$) from 10.8 V to 26.4 V
- Minimizes External Components

**BLOCK DIAGRAM**


R/W1
R/W2
7
6
WD
5
Toggle Select
Erase Delays
12
D1
11
D2
17
E0
15
E1
Select Enable
18
CT0
20
CT1
IRWS
8
Current Select
1
2
4
13
10
Inhibit
$V_{Ref}$
$I_{Ref}$
WG
HS

**ABSOLUTE MAXIMUM RATINGS** (Note 1) ($T_A = 25°C$)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage (Pin 14) | $V_{CC}$ | 7.0 | Vdc |
| Power Supply Voltage (Pin 19) | $V_{BB}$ | 30 | Vdc |
| Input Voltage (Pins 4, 5, 8, 13) | $V_I$ | 5.75 | Vdc |
| Output Applied Voltage (Pin 10) | $V_O$ | 7.0 | Vdc |
| Open-Collector Sink Current (Pin 10) | $I_O$ | 25 | mA |
| Storage Temperature | $T_{stg}$ | -55 to +150 | °C |
| Operating Junction Temperature | $T_J$ | 150 | °C |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**RECOMMENDED OPERATING CONDITIONS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage (Pin 14) | $V_{CC}$ | +4.75 to +5.25 | Vdc |
| Power Supply Voltage (Pin 19) | $V_{BB}$ | +10.8 to +26.4 | Vdc |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0 to +70°C, $V_{CC}$ = 4.75 to 5.25 V, $V_{BB}$ = 10.8 to 26.4 V unless otherwise noted. Typicals given for $V_{CC}$ = 5.0 V, $V_{BB}$ = 12 V and $T_A$ = 25°C unless otherwise noted.)

| Characteristics | Pins | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DIGITAL INPUT VOLTAGES** | | | | | | |
| Power Supply Current — $V_{CC}$ | | $I_{CC}$ | — | 22 | 60 | mA |
| $V_{BB}$ | | $I_{BB}$ | — | 15 | 30 | |
| High Level Input Voltage ($V_{CC}$ = 4.75 V) | 4, 8, 13 | $V_{IH}$ | 2.0 | — | — | V |
| Low Level Input Voltage ($V_{CC}$ = 5.25 V) | 4, 8, 13 | $V_{IL}$ | — | — | 0.8 | V |
| Input Clamp Voltage ($I_{IK}$ = -12 mA) | 4, 5, 8, 13 | $V_{IK}$ | — | -0.87 | -1.5 | V |
| Positive Threshold ($V_{CC}$ = 5.0) | 5 | $V_{T(+)}$ | 1.5 | 1.75 | 2.0 | V |
| Negative Threshold ($V_{CC}$ = 5.0) | 5 | $V_{T(-)}$ | 0.7 | 0.98 | 1.3 | V |
| Hysteresis ($V_{T(+)} - V_{T(-)}$) | | $V_{HTS}$ | | | | V |
| $T_A$ = 0°C to +70°C | 5 | | 0.2 | — | — | |
| $T_A$ = 25°C | | | 0.4 | 0.76 | — | |
| **DIGITAL INPUT CURRENTS** | | | | | | |
| High Level Input Current ($V_{CC}$ = 5.25 V, $V_{BB}$ = 26.4 V, $V_I$ = 2.4 V) | 4, 5, 8, 13 | $I_{IH}$ | — | 0.1 | 40 | µA |
| Low Level Input Current ($V_{CC}$ = 5.25 V, $V_{BB}$ = 26.4 V, $T_A$ = 25°C unless noted below) | 4, 5, 8, 13 | $I_{IL}$ | — | — | -1.6 | mA |
| $V_{BB}$ = 12 V | 4 | | — | 0.36 | — | |
| $V_{BB}$ = 24 V | 4 | | — | 0.76 | — | |
| $V_{CC}$ = 5.0 V | 5 | | — | 0.46 | — | |
| $V_{CC}$ = 5.0 V | 8, 13 | | — | 0.39 | — | |

**ELECTRICAL CHARACTERISTICS (continued)** ($T_A$ = 0 to +70°C, $V_{CC}$ = 4.75 to 5.25 V, $V_{BB}$ = 10.8 to 26.4 V unless otherwise noted. Typicals given for $V_{CC}$ = 5.0 V, $V_{BB}$ = 12 V and $T_A$ = 25°C unless otherwise noted.)

| Characteristics | Pins | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CENTER-TAP and ERASE OUTPUTS** | | | | | | |
| Output High Voltage (See Figure 14)<br>($I_{OH}$ = −100 mA, $V_{CC}$ = 4.75 V)<br>$V_{BB}$ = 10.8 to 26.4 V | 18, 20 | $V_{OH}$ | $V_{BB}$-1.5 | $V_{BB}$-1.0 | — | V |
| Output Low Voltage (See Figure 14)<br>($I_{OL}$ = 1.0 mA) | 18, 20 | $V_{OL}$ | | | | mV |
| $V_{BB}$ = 12 V | | | — | 70 | 150 | |
| $V_{BB}$ = 24 V | | | — | 70 | 150 | |
| Output High Leakage Current<br>($V_{OH}$ = 24 V, $V_{CC}$ = 4.75 V, $V_{BB}$ = 24 V) | 15, 17 | $I_{OH}$ | — | 0.01 | 100 | μA |
| Output Low Voltage (See Figure 15)<br>($I_{OL}$ = 90 mA, $V_{CC}$ = 4.75 V) | 15, 17 | $V_{OL}$ | | | | V |
| $V_{BB}$ = 12 V | | | — | 0.27 | 0.60 | |
| $V_{BB}$ = 24 V | | | — | 0.27 | 0.60 | |
| **DIGITAL OUTPUT LEVEL ($\overline{\text{Inhibit}}$)** | | | | | | |
| High Level Output Current<br>($V_{OH}$ = 7.0 V, $V_{CC}$ = 4.75 V) | 10 | $I_{OH}$ | — | — | 100 | μA |
| Low Level Output Voltage<br>($I_{OL}$ = 4.0 mA, $V_{CC}$ = 4.75 V) | 10 | $V_{OL}$ | — | — | 0.5 | V |
| **CURRENT SOURCE** | | | | | | |
| Reference Voltage | 1 | $V_{Ref}$ | — | 5.7 | — | V |
| Degauss Voltage (See Text)<br>(Voltage Pin 1 − Voltage Pin 2) | 1 | $V_{DEG}$ | — | 1.0 | — | V |
| Bias Voltage | 2 | $V_F$ | — | 0.7 | — | V |
| Write Current Off Leakage<br>($V_{OH}$ = 30 V) | 6, 7 | $I_{OH}$ | — | 0.03 | 15 | μA |
| Saturation Voltage<br>($V_{BB}$ = 12 V) | 6, 7 | $V_{sat}$ | — | 0.85 | 2.7 | V |
| Current Sink Compliance<br>(For $V_{6,\,7}$ = 4.0 V to 24 V, $V_{\overline{WG}}$ = 0.8 V) | 6, 7 | ΔI/RW2, 1 | — | 15 | 40 | μA |
| Average Value Write Current<br>($\frac{(I_{Pin\ 6} + I_{Pin\ 7})}{2}$ for $V_{BB}$ = 10.8 to 26.4 V) | 6, 7 | | | | | |
| @ $I_{R/W} = I_{LOW}$, R = 10 k | | $\overline{I_{R/W(L)}}$ | | | | mA |
| $T_A$ = 25°C | | | 2.91 | 3.0 | 3.09 | |
| $T_A$ = 0 to +70°C | | | 2.84 | — | 3.16 | |
| @ $I_{R/W} = I_{LOW}$, R = 5.0 k | | | | | | |
| $T_A$ = 25°C | | | 5.64 | 5.89 | 6.14 | |
| $T_A$ = 0 to +70°C | | | 5.51 | — | 6.28 | |
| @ $I_{R/W} = I_{HI}$, R = 10 k ($I_{HI} = I_{LOW}$ + % $I_{LOW}$) | | $\overline{\Delta I_{R/W(H)}}$ | | | | % |
| $T_A$ = 25°C | | | 31.3 | 33.3 | 35.5 | |
| $T_A$ = 0 to +70°C | | | 30.3 | 33.3 | 36.6 | |
| Difference in Write Current<br>($\|I_{Pin\ 6} - I_{Pin\ 7}\|$<br>@ $I_{R/W} = I_{LOW}$, $V_{BB}$ = 10.8 V to 26.4 V) | 6, 7 | $I_{R/W\Delta}$ | | | | mA |
| R = 10 k | | | | | | |
| $T_A$ = 25°C | | | — | 0.003 | 0.015 | |
| $T_A$ = 0 to +70°C | | | — | — | 0.023 | |
| R = 5.0 k | | | | | | |
| $T_A$ = 25°C | | | — | — | 0.030 | |
| $T_A$ = 0 to +70°C | | | — | — | 0.046 | |

**ERASE DELAY ACCURACY** ($V_{CC}$ = 4.75 to 5.25 V, $T_A$ = 0 to +70°C, $V_{BB}$ = 10.8 to 26.4 V, — refer to Figure 9.)

| Characteristics | Test | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Delay Error, Pin 11, 12<br>D1, D2 = RC $\pm E_{D1,2}$, 30 kΩ ≤ R ≤ 300 kΩ | $E_{D1,2}$ | — | — | 15 | % |

**AC SWITCHING CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $T_A$ = 25°C, $V_{BB}$ = 24 V, $I_{RWS}$ = 0.4 and $I_{R/W}$ = 3.0 mA unless otherwise noted.)

| Characteristics (Note 2) | $f_{in}$ (Note 3) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **1. Delay from Head Select going low through 0.8 V to CT0 going high through 20 V.** | HS, Pin 13 | — | 1.6 | 4.0 | μs |
| 2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V. | HS, Pin 13 | — | 2.1 | 4.0 | μs |
| **3. Delay from Head Select going high through 2.0 V to CT0 going low through 1.0 V.** | HS, Pin 13 | — | 1.7 | 4.0 | μs |
| **4. Delay from Head Select going high through 2.0 V to CT1 going high through 20 V.** | HS, Pin 13 | — | 1.4 | 4.0 | μs |
| 5. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going low through 1.0 V. | $\overline{WG}$, Pin 4 | — | 1.3 | 4.0 | μs |
| 6. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going high through 20 V. | $\overline{WG}$, Pin 4 | — | 0.8 | 4.0 | μs |
| 7. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going high through 20 V. | $\overline{WG}$, Pin 4 | — | 0.75 | 4.0 | μs |
| 8. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going low through 1.0 V. | $\overline{WG}$, Pin 4 | — | 1.2 | 4.0 | μs |
| **9. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT0 going high through 20 V.** | $\overline{WG}$, Pin 4 | 20 | 750 | — | ns |
| 10. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V. | $\overline{WG}$, Pin 4 | 20 | 1200 | — | ns |
| **11. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT0 going low through 1.0 V.** | $\overline{WG}$, Pin 4 | 20 | 1200 | — | ns |
| 12. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V. | $\overline{WG}$, Pin 4 | 20 | 600 | — | ns |
| **13. After $\overline{WG}$ goes low, delay from CT0 going low through 1.0 V to R/W1 turning on through 10%.** | $\overline{WG}$, Pin 4 | 20 | 750 | — | ns |
| 14. After $\overline{WG}$ goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%. | $\overline{WG}$, Pin 4 | 20 | 750 | — | ns |
| 15. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W1. | $\overline{WG}$, Pin 4 | — | 5.0 | 200 | ns |
| 16. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W2. | $\overline{WG}$, Pin 4 | — | 5.0 | 200 | ns |
| 17. Setup time, Head Select going low before $\overline{WG}$ going low. | $\overline{WG}$, Pin 4 | 4.0 | — | — | μs |
| 18. $\overline{\text{Write Data}}$ low Hold Time | $\overline{WD}$, Pin 5 | 200 | — | — | ns |
| 19. $\overline{\text{Write Data}}$ high Hold Time | $\overline{WD}$, Pin 5 | 500 | — | — | ns |
| 20. Delay from $\overline{WG}$ going high through 2.0 V to R/W 1 turning off through 10% of on value. | $\overline{WG}$, Pin 4 | — | 3.9 | — | μs |
| 21. Delay from $\overline{WG}$ going low thru 0.8 V to $\overline{\text{Inhibit}}$ going low thru 0.5 V (Note 5) | $\overline{WG}$, Pin 4 | — | 0.08 | 4.0 | μs |
| 22. After $\overline{WG}$ goes high, delay from R/W1 turning off thru 10% to $\overline{\text{Inhibit}}$ going high thru 1.5 V (10 k pullup on Inhibit, Note 5) | $\overline{WG}$, Pin 4 | 20 | 750 | — | ns |
| **23. After $\overline{WG}$ goes high, delay from $\overline{E1}$ going high thru 23 V to $\overline{\text{Inhibit}}$ going high thru 1.5 V (10 k pullup on Inhibit, Note 5)** | $\overline{WG}$ | 20 | 750 | — | ns |

Note 2: Test numbers refer to encircled numbers in Figures 3 & 16.
Note 3: AC test waveforms applied to the designated pins as follows:
Note 4: 22. or 23., whichever produces the longer delay, will control $\overline{\text{Inhibit}}$.

| Pin | $f_{in}$ | Amplitude | Duty Cycle |
|---|---|---|---|
| HS, Pin 13 | 50 kHz | 0.4 to 2.4 V | 50% |
| $\overline{WG}$, Pin 4 | 50 kHz | 0.4 to 2.4 V | 50% |
| $\overline{WD}$, Pin 5 | 1.0 MHz | 0.2 to 2.4 V | 50% |

### AC SWITCHING CHARACTERISTICS (continued)

($V_{CC}$ = 5.0 V, $T_A$ = 25°C, $V_{BB}$ = 24 V, $\overline{WG}$ = 0.4 unless otherwise noted)

| Characteristics (Note 4) | Min | Typ | Max | Unit |
|---|---|---|---|---|
| 1. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning on through 50%. | — | 85 | — | ns |
| 2. Delay skew, difference of R/W1 turning off and R/W2 turning on through 50% after $\overline{\text{Write Data}}$ going low through 0.9 V. | — | 1.0 | ±40 | ns |
| 3. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning off through 50%. | — | 80 | — | ns |
| 4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after $\overline{\text{Write Data}}$ going low through 0.9 V. | — | 1.0 | ±40 | ns |
| 5. Fall time, 10% to 90%, of R/W1 | — | 1.7 | 200 | ns |
| 6. Fall time, 10% to 90%, of R/W2 | — | 1.7 | 200 | ns |
| 7. Rise time, 90% to 10%, of R/W1 | — | 12 | 200 | ns |
| 8. Rise time, 90% to 10%, of R/W2 | — | 12 | 200 | ns |

Note 5: Test numbers refer to encircled numbers in Figures 2 & 15.
$f_{in}$ = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

## PIN DESCRIPTION TABLE

| Name | Symbol | Pin | Description |
|---|---|---|---|
| Head Select | HS | 13 | Head Select input selects between the head I/O pins; center-tap, erase, and read/write. A HIGH selects Head 0 and a LOW selects Head 1. |
| $\overline{\text{Write Gate}}$ | $\overline{\text{WG}}$ | 4 | $\overline{\text{Write Gate}}$ input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current. |
| $\overline{\text{Write Data}}$ | $\overline{\text{WD}}$ | 5 | $\overline{\text{Write Data}}$ input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils. |
| IRW Select | IRWS | 8 | IRW Select input selects the amount of write current to be used. When LOW, the current equals the value found in Figure 5, according to the external resistor. When HIGH, the current equals the low current + 33%. |
| $V_{Ref}$<br>$I_{Ref}$ | $V_{Ref}$<br>$I_{Ref}$ | 1<br>2 | A resistor between these pins sets the write current. (Refer to Figure 4.) A capacitor from $V_{Ref}$ to Gnd will adjust the Degauss period. |
| Center-Tap 0 | CT0 | 18 | Center-Tap 0 output is connected to the center tap of Head 0. It will be pulled to Gnd or $V_{BB}$ (+12 or +24) depending on mode and head selection. |
| $\overline{\text{Erase 0}}$ | $\overline{\text{E0}}$ | 17 | $\overline{\text{Erase 0}}$ will be LOW for writing on Head 0, and floating for other conditions. |
| Center-Tap 1 | CT1 | 20 | Center-Tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or $V_{BB}$ (+12 or +24) depending on mode and head selection. |
| $\overline{\text{Erase 1}}$ | $\overline{\text{E1}}$ | 15 | $\overline{\text{Erase 1}}$ will be LOW for writing on Head 1, and floating for other conditions. |
| R/W2 | R/W2 | 6 | R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads. |
| R/W1 | R/W1 | 7 | R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads. |
| | $V_{CC}$ | 14 | +5.0 V Power |
| | $V_{BB}$ | 19 | +12 V or + 24 V Power |
| | Gnd | 16 | Coil grounds |
| | Gnd | 3 | Reference and logic ground |
| Delay 1 | D1 | 12 | Erase Turn-On Delay adjust (RC or Logic) |
| Delay 2 | D2 | 11 | Erase Turn-Off Delay adjust (RC or Logic) |
| Inhibit | $\overline{\text{Inhibit}}$ | 10 | Active low open-collector output provided to indicate heads are active in the write, degauss or erase mode. (Used for step or read inhibit.) |

FIGURE 1 — LOGIC DIAGRAM

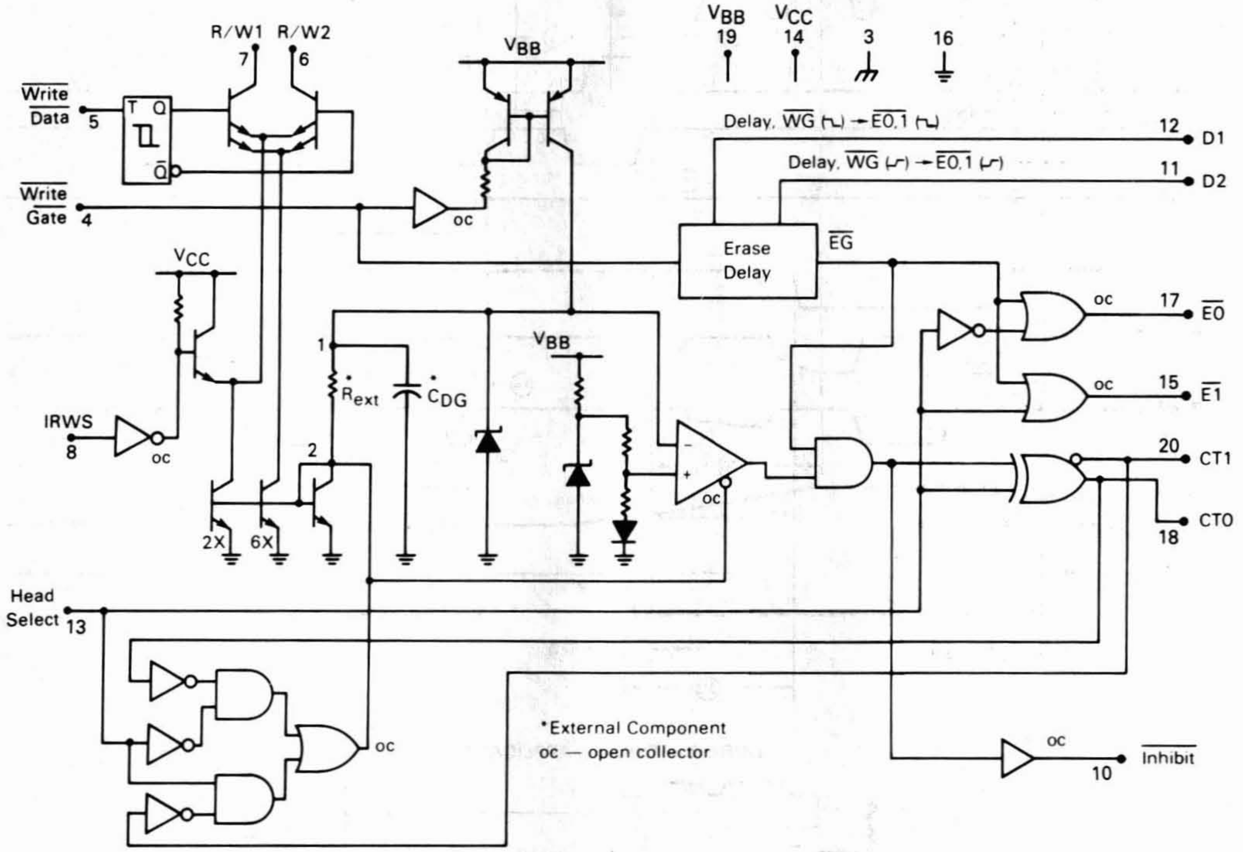

R/W1
R/W2
7
6
Write Data 5
T Q
Q̄
Write Gate 4
VBB
oc
VBB 19
VCC 14
3
16
Delay, WG (⊓) → E0,1 (⊓)
Delay, WG (⊔) → E0,1 (⊔)
12 D1
11 D2
Erase Delay
EG
oc
17 E0
oc
15 E1
20 CT1
CT0 18
VCC
IRWS 8
oc
1
Rext*
CDG*
VBB
2
2X
6X
oc
Head Select 13
oc
*External Component
oc — open collector
oc
10 Inhibit

FIGURE 2 — R/W1 AND R/W2 RELATIONSHIP

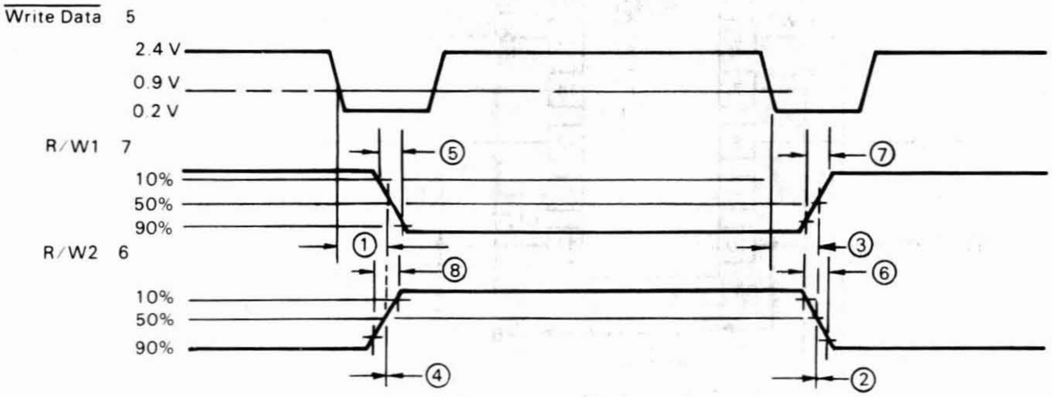

Write Data 5
2.4 V
0.9 V
0.2 V
R/W1 7
10%
50%
90%
R/W2 6
10%
50%
90%
①
②
③
④
⑤
⑥
⑦
⑧

FIGURE 3 — AC TIMING DIAGRAM

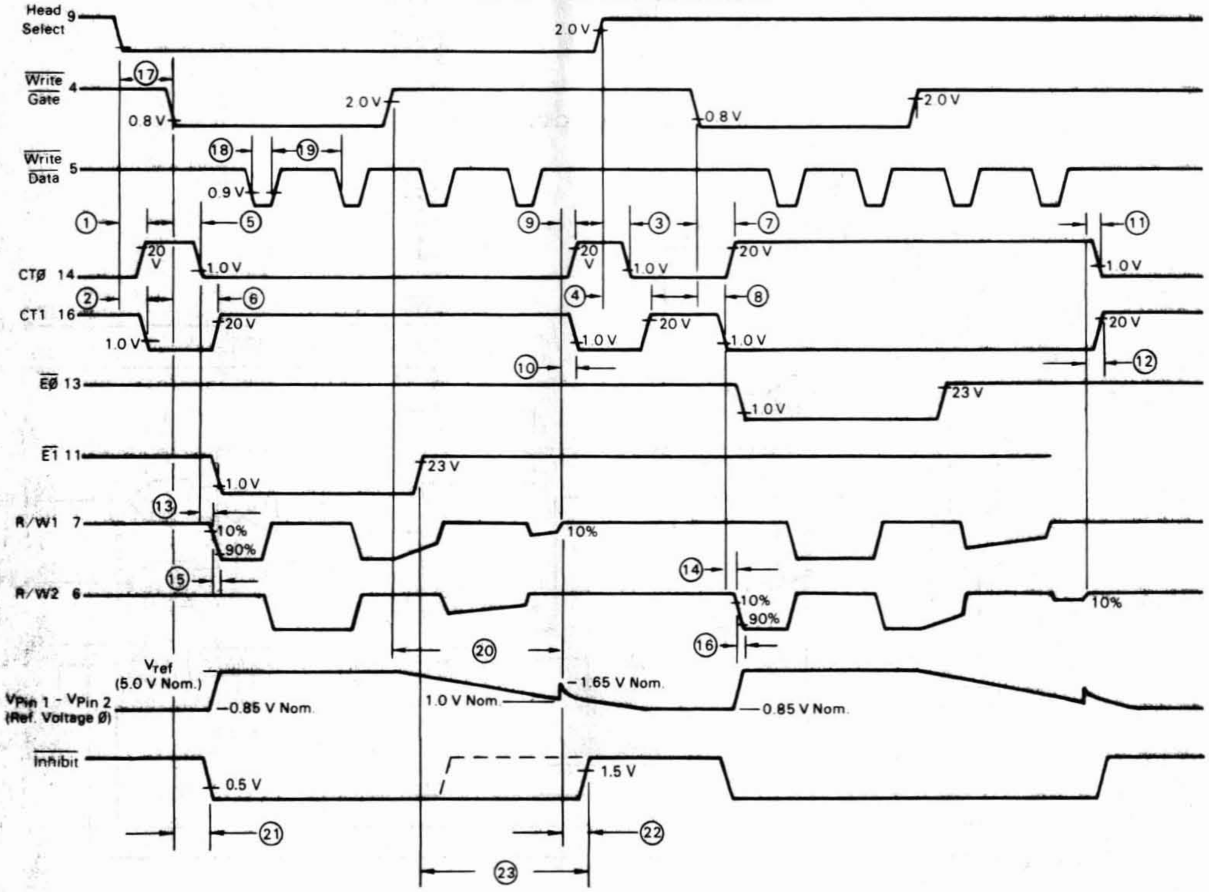
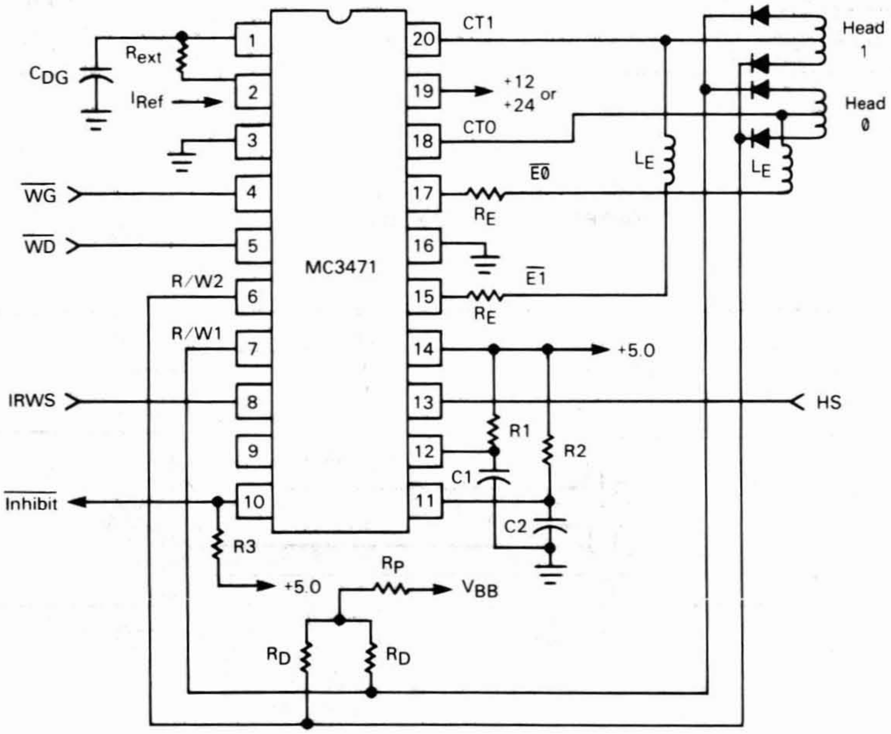

Head Select 9
2.0 V
Write Gate 4
⑰
0.8 V
2.0 V
0.8 V
2.0 V
Write Data 5
⑱
⑲
0.9 V
①
⑤
⑨
③
⑦
⑪
CTØ 14
20 V
1.0 V
20 V
1.0 V
20 V
1.0 V
②
⑥
④
⑧
CT1 16
1.0 V
20 V
1.0 V
20 V
1.0 V
20 V
⑩
⑫
EØ 13
1.0 V
23 V
E1 11
1.0 V
23 V
⑬
R/W1 7
10%
90%
10%
⑭
⑮
R/W2 6
10%
90%
10%
⑯
⑳
Vref (5.0 V Nom.)
VPin 1 - VPin 2 (Ref. Voltage Ø)
0.85 V Nom.
1.0 V Nom.
1.65 V Nom.
0.85 V Nom.
Inhibit
0.5 V
1.5 V
㉑
㉒
㉓

FIGURE 4 — TYPICAL APPLICATION


CDG
Rext
IRef
WG
WD
R/W2
R/W1
IRWS
Inhibit
R3
+5.0
RP
VBB
RD
RD
MC3471
1
2
3
4
5
6
7
8
9
10
20
19
18
17
16
15
14
13
12
11
CT1
+12 or +24
CTO
E0
RE
E1
RE
+5.0
HS
R1
R2
C1
C2
LE
LE
Head 1
Head Ø

## APPLICATION INFORMATION

The MC3471P serves as a complete interface between the Write Control functional signals (Head Select, Write Data, Write Gate and inner track compensation, IRWS) and the head itself. A typical configuration is shown in Figure 4. $L_E$'s are erase coils.

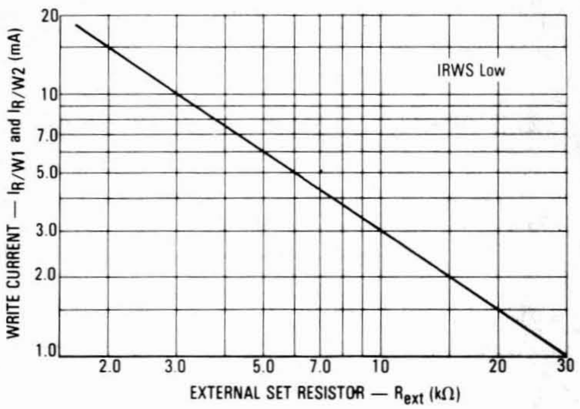
### WRITE CURRENT SELECTION

Although the MC3471P has been specified for 3.0 mA write current (with a 10 kΩ external resistor), a range of write current values can be chosen by varying $R_{ext}$ using the plot in Figure 5. This current can also be derived using

the relationship $I_{Write}\ (mA) = \dfrac{30}{R_{ext}(k\Omega)}$

**$I_{Ref}$, the current flowing in $R_{ext}$ (required only for dissipation calculations) can be worst case using the fact that the differential voltage between Pins 1 and 2 ($V_{Ref}$) shown in Figure 3 never exceeds 5.0 volts. With a low value of $R_{ext}$ = 1.0 kΩ, $P_D$ = 25 mW.**

FIGURE 5 — WRITE CURRENT versus $R_{ext}$



### WRITE CURRENT DAMPING

Referring to Figure 4, resistors $R_D$ are used to dampen any ringing that results from applying the relatively fast risetime write current pulse to the inductive head load. Values chosen will be a funciton of head characteristics and the desired damping. $R_P$ serves as a common pullup resistor to the head supply $V_{BB}$.

### DEGAUSS PERIOD

Degauss of the read/write head can be accomplished at the end of each write operation by attaching a capacitor from Pin 1 to ground. The time relationship that results is shown in Figure 7. A simplified diagram of this function is shown in Figure 6.

While $\overline{WG}$ is low, the selected write current flows into Pin 6 or Pin 7 (R/W1 or R/W2) and is mirrored through the external resistor, $R_{ext}$. The degauss capacitor, $C_{DG}$, will be charged to approximately 5.7 volts. After $\overline{WG}$ goes high, the voltage on $C_{DG}$ begins to decay toward 0.7 V. When the voltage reaches the comparator threshold of 1.7 V, the comparator output triggers the internal logic to completely turn off the write current. At this point, the pulse amplitude on the R/W1 and R/W2 pins has returned to 10% of its maximum value.

Figure 7, Degauss Period shows the relationship between $C_{DG}$ and Degauss Period for $R_{ext}$ = 10 kΩ. This period is equal to the exponential delay time for the voltage as mentioned plus internal delay times.

FIGURE 6 — SIMPLIFIED DEGAUSS CIRCUIT

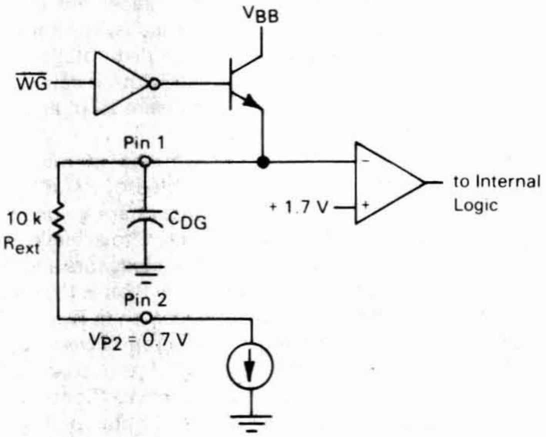
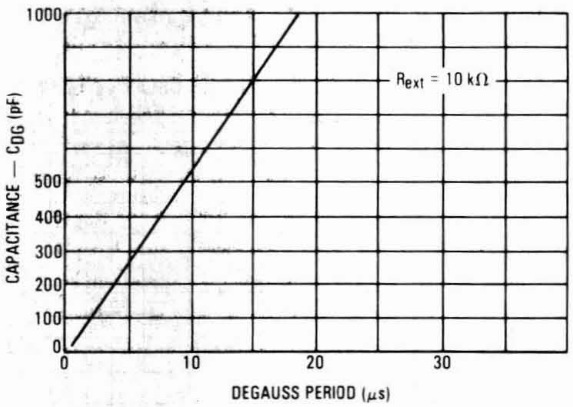


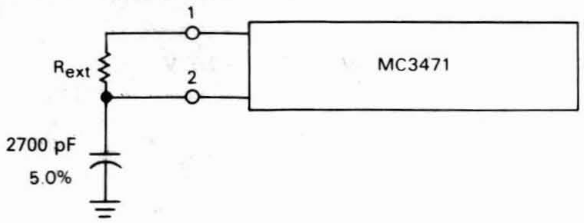
FIGURE 7 — DEGAUSS PERIOD versus CAPACITANCE ($C_{DG}$)



### POWER-UP WRITE CURRENT CONTROL

**During power-up, under certain conditions ($V_{BB}$ comes up first while $\overline{WG}$ is low), there can be a write current transient on Pins 6 and 7 (R/W1 and R/W2) of sufficient magnitude to cause writing to occur if the head is loaded.**

**This transient can be eliminated by placing a capacitor from Pin 2 to ground. This also delays the write current when $\overline{WG}$ goes low and this delay must be accounted for when the capacitor on Pin 2 is used. The delay is 3.0 μs for a 2700 pF capacitor, and $R_{ext}$ = 10 kΩ. Values up to 7000 pF may be used.**



**See Application Note AN917 for further information.**

## ERASE DELAY

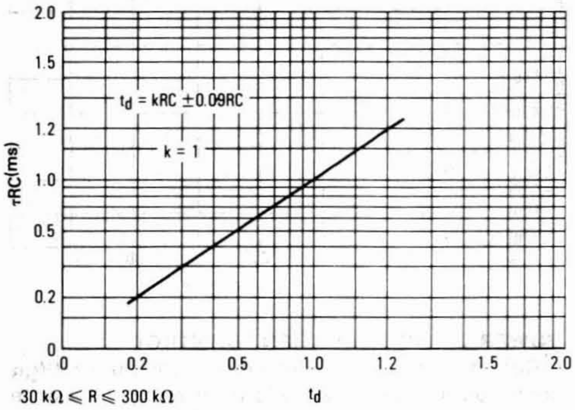
The MC3471P can be used with both straddle and tunnel erase heads. When using the tunnel erase heads, it is necessary to delay the erase current in time with respect to $\overline{WG}$ due to the physical placement of the erase gap behind the R/W gap on the heads. The amount of delay required depends upon the disk rotation velocity, recording density and format. Turn-on delay and turn-off delay must also be independent to guarantee erase is on for the entire block.

Nominal delays of 500 μs turn-on; and 1.0 ms turn-off are available by adjusting the value of R1, R2 and C1, C2 shown in Figure 4. These delays are adjustable over a broad range as shown in Figure 9 to achieve any practical delay required. By using 5% capacitors and 1% resistors, total timing accuracy is better than ± 15% over temperature and supply. Timing is shown in Figure 10.

In applications using logic or microprocessor controlled delays, the D1 and D2 inputs can be used directly to turn-on and turn-off the erase current. (Controlling outputs should be Open-collector w/10 k pullup). Figure 11 shows the relative timing involved for the microprocessor and logic controlled applications.

In straddle erase systems, the erase delays can be eliminated by pulling D1 and D2 high thru a 10 kΩ pullup resistor to +5.0 V.

FIGURE 9 — TYPICAL $\overline{WG}$ TO E0, 1 DELAY versus RC



## ERASE CURRENT

The value of $R_E$, the erase current set resistor, is found by referring to Figure 12 and selecting the desired erase current.

Looking at the simplified erase current path in Figure 12, when writing, CT0 will be high ($V_{OH(min)}$ = 22.5 V) and E0 will be low ($V_{OL(max)}$ = 0.6 V). If the erase coil resistance is 10 Ω and 40 mA of erase current is desired then:

$$(R_E + 10\ \Omega) \times 40\ \text{mA} = (22.5 - 0.6)\ \text{V}$$

or

$$R_E = \frac{21.9\ \text{V}}{0.04\ \text{A}} - 10\ \Omega = 537\ \Omega$$

$$P_D = (537)\,(0.04)^2 = 0.86\ \text{W}$$

This gives the minimum value $R_E$ for worst case $V_{OH}/V_{OL}$ conditions. It is also recommended that a diode be used as indicated for inductive back emf suppression.

FIGURE 10 — DELAY INPUT FUNCTION/TIMING WITH RC ELEMENTS

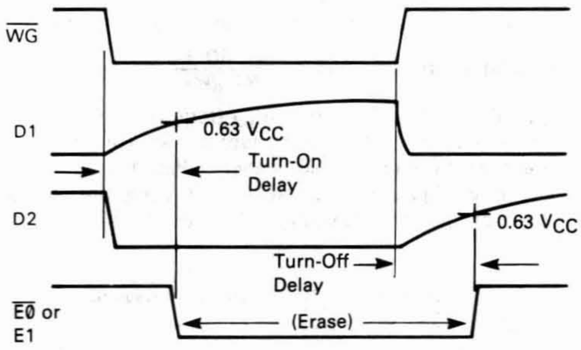


FIGURE 11 — DELAY INPUT FUNCTION/TIMING WITH LOGIC CONTROL

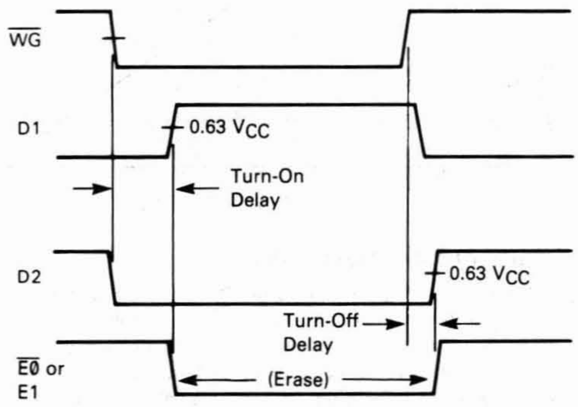


FIGURE 12 — ERASE CURRENT ($R_E$ Selection)

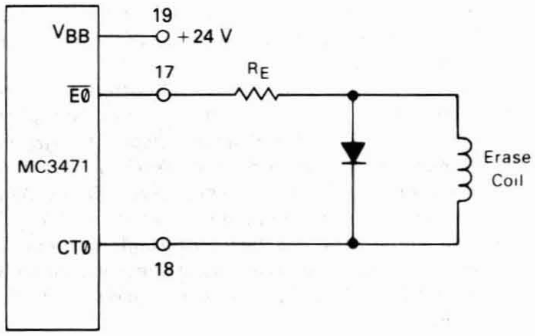
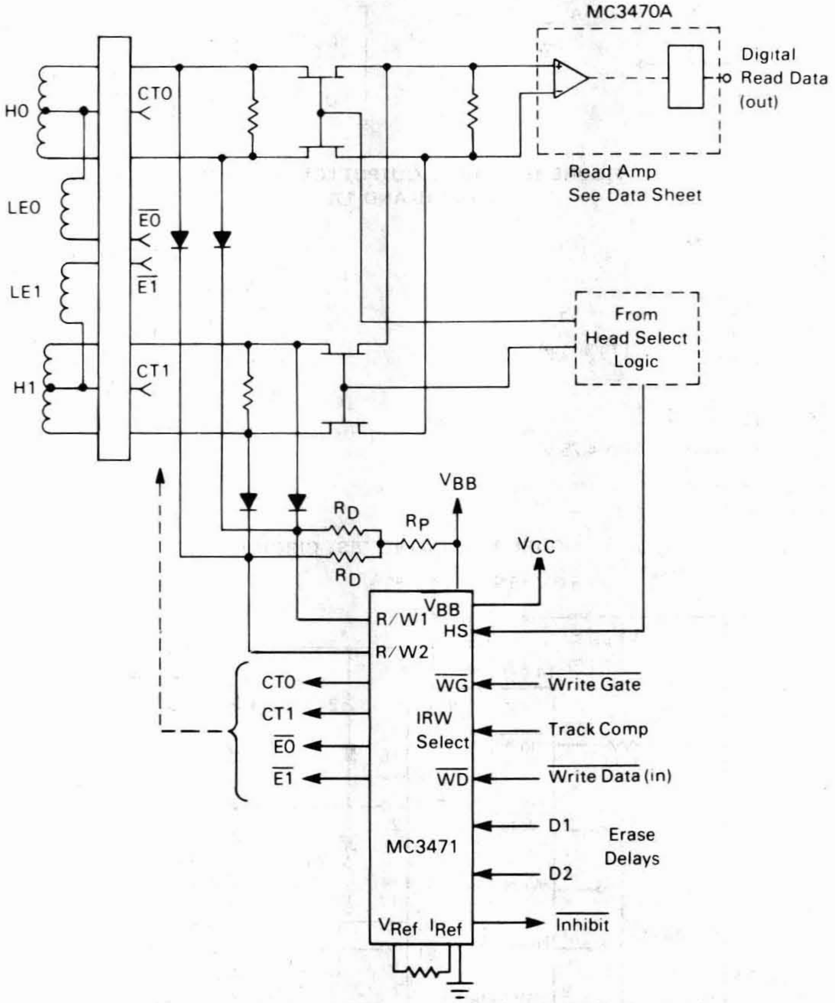


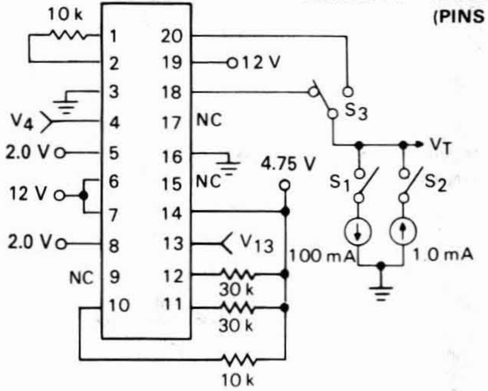
FIGURE 13 — TYPICAL DUAL HEAD FLOPPY DISK SYSTEM USING FET GATE READ CHANNEL SELECTION AND MC3471/MC3470A


MC3470A
Digital Read Data (out)
Read Amp See Data Sheet
H0
CT0
LE0
E0
LE1
E1
CT1
H1
From Head Select Logic
VBB
RD
RP
VCC
RD
R/W1
VBB
HS
R/W2
CT0
CT1
E0
E1
WG
IRW Select
WD
Write Gate
Track Comp
Write Data (in)
D1
D2
Erase Delays
MC3471
VRef
IRef
Inhibit

| Function | CT0 | CT1 | E0 | E1 |
|---|---|---|---|---|
| Write 0 | $V_{BB}$ | 0 V | On | Off |
| Write 1 | 0 V | $V_{BB}$ | Off | On |
| Read 0 | 0 V | $V_{BB}$ | Off | Off |
| Read 1 | $V_{BB}$ | 0 V | Off | Off |

## TEST FIGURES

### FIGURE 14 — CENTER TAP OUTPUT VOLTAGE (PINS 18 AND 20)

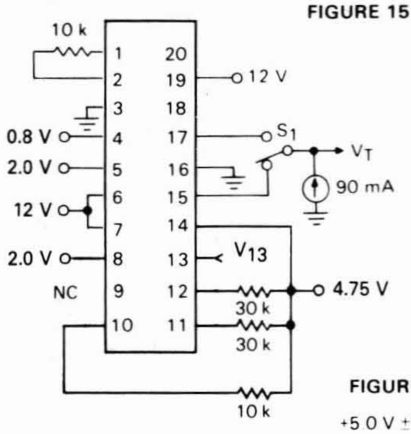

10 k
1
2
3
4
5
6
7
8
9
10
20
19
18
17
16
15
14
13
12
11
12 V
NC
NC
4.75 V
V4
2.0 V
12 V
2.0 V
NC
V13
30 k
30 k
10 k
S3
VT
S1
S2
100 mA
1.0 mA

CONDITIONS

| Measure | Set | | | | |
|---|---|---|---|---|---|
| $V_T$ | $S_1$ | $S_2$ | $S_3$ | $V_4$* | $V_{13}$* |
| $V_{OH}$ (P18) | On | Off | P 18 | 0.8 | 2.0 |
| | | | | 2.0 | 0.8 |
| $V_{OH}$ (P20) | On | Off | P 20 | 2.0 | 2.0 |
| | | | | 0.8 | 0.8 |
| $V_{OL}$ (P18) | Off | On | P 18 | 0.8 | 0.8 |
| | | | | 2.0 | 2.0 |
| $V_{OL}$ (P20) | Off | On | P 20 | 2.0 | 0.8 |
| | | | | 0.8 | 2.0 |

*Volts

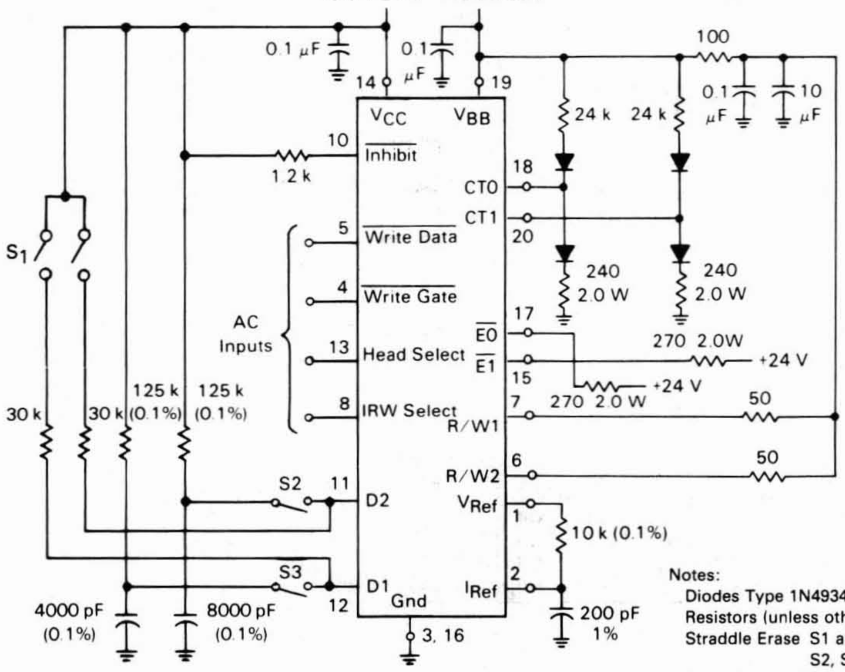
### FIGURE 15 — ERASE OUTPUT LOW VOLTAGE (PINS 15 AND 17)


10 k
1
2
3
4
5
6
7
8
9
10
20
19
18
17
16
15
14
13
12
11
12 V
0.8 V
2.0 V
12 V
2.0 V
NC
S1
VT
90 mA
V13
4.75 V
30 k
30 k
10 k

CONDITIONS

| Measure | Set | |
|---|---|---|
| $V_T$ | $S_1$ | $V_{13}$ |
| $V_{OL}$ (P15) | P15 | 0.8V |
| $V_{OL}$ (P17) | P17 | 2.0 V |

### FIGURE 16 — TIMING TEST CIRCUIT


+5.0 V ±5%
+24 V ±5%
0.1 μF
0.1 μF
14
19
100
0.1 μF
10 μF
VCC
VBB
24 k
24 k
10
Inhibit
1.2 k
18
CTO
CT1
20
5
Write Data
4
Write Gate
240 2.0 W
240 2.0 W
S1
AC Inputs
17
E0
13
Head Select
E1
270 2.0W
+24 V
15
+24 V
270 2.0 W
125 k (0.1%)
125 k (0.1%)
30 k
30 k
8
IRW Select
7
R/W1
50
6
R/W2
50
S2
11
D2
VRef
1
10 k (0.1%)
S3
D1
Gnd
IRef
2
12
4000 pF (0.1%)
8000 pF (0.1%)
3, 16
200 pF 1%

Notes:
Diodes Type 1N4934
Resistors (unless otherwise noted) are 1/4 W 5%
Straddle Erase S1 and S4 Closed
S2, S3 Open
Tunnel Erase S1 and S4 Open
S2, S3 Closed

**MOTOROLA**

# MC3480

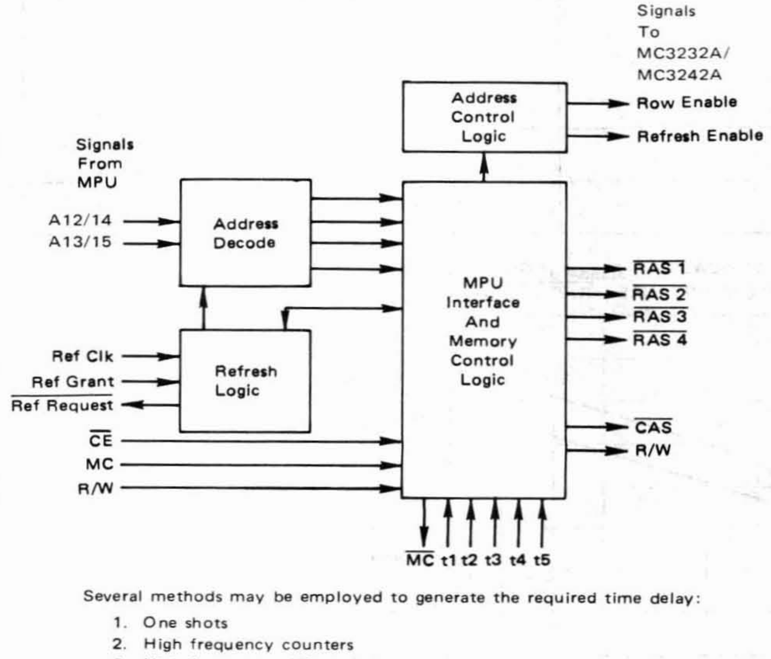
## Specifications and Applications Information

### MEMORY CONTROLLER FOR 16 PIN 4K, 16K AND 64K DYNAMIC RAMs

The memory controller chip is designed to greatly simplify the interface logic required to control the popular 16 pin multiplexed dynamic NMOS RAMs in a microprocessor system such as the M6800. The controller will generate, on command from the microprocessor, the proper timing signals required to successfully transfer data between the microprocessor and the NMOS memories. The controller, in conjunction with an oscillator, will also generate the necessary signals required to insure that the dynamic memories are refreshed for the retention of data.

- Greatly Simplify the MPU-Dynamic Memory Interface
- Reduce Package Count and System Access/Cycle Times 30%
- Chip Enable for Expansion to Larger Word Capacity
- Generate 1 of 4 $\overline{\text{RAS}}$ Signals for an Optimum 16K/64K Memory System
- High Input Impedance for Minimum Loading of MPU Bus
- Schottky TTL Technology for High Performance
- Useful with 4K and 16K and Future Expanded Dynamic RAMs

### BLOCK DIAGRAM


Signals To MC3232A/ MC3242A
Address Control Logic
Row Enable
Refresh Enable
Signals From MPU
A12/14
A13/15
Address Decode
MPU Interface And Memory Control Logic
RAS 1
RAS 2
RAS 3
RAS 4
Ref Clk
Ref Grant
Ref Request
Refresh Logic
CE
MC
R/W
CAS
R/W
MC t1 t2 t3 t4 t5

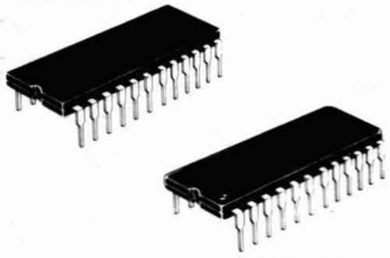
Several methods may be employed to generate the required time delay:

1. One shots
2. High frequency counters
3. High frequency shift registers
4. Delay lines
5. Signals from MPU Clock

## DYNAMIC MEMORY CONTROLLER

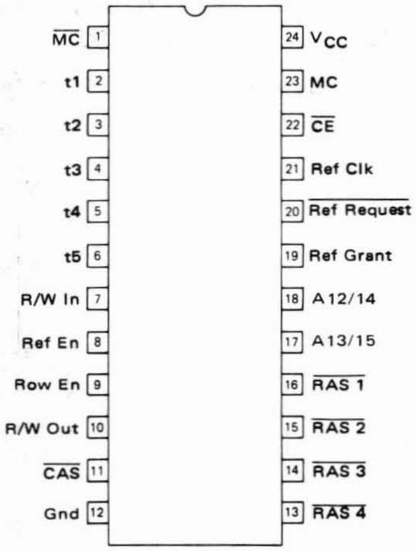
### SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT

**L SUFFIX**
CERAMIC PACKAGE
CASE 623-05



**P SUFFIX**
PLASTIC PACKAGE
CASE 649-03

**PIN CONNECTIONS**


MC 1
t1 2
t2 3
t3 4
t4 5
t5 6
R/W In 7
Ref En 8
Row En 9
R/W Out 10
CAS 11
Gnd 12
24 VCC
23 MC
22 CE
21 Ref Clk
20 Ref Request
19 Ref Grant
18 A12/14
17 A13/15
16 RAS 1
15 RAS 2
14 RAS 3
13 RAS 4

See Pin Descriptions

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 7.0 | Vdc |
| Input Voltage | $V_I$ | −0.5 to +7.0 | Vdc |
| Output Voltage | $V_O$ | −0.5 to +7.0 | Vdc |
| Operating Ambient Temperature | $T_A$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |
| Operating Junction Temperature<br>Ceramic Package<br>Plastic Package | $T_J$ | <br>175<br>150 | °C |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

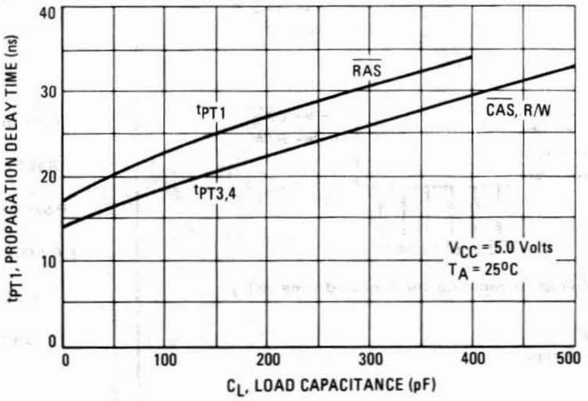
## RECOMMENDED OPERATING CONDITIONS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +4.50 to +5.50 | Vdc |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |

## ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply over recommended power supply and temperature ranges.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage – Low Logic State | $V_{IL}$ | – | – | 0.8 | V |
| Input Voltage – High Logic State | $V_{IH}$ | 2.0 | – | – | V |
| Input Current – Low Logic State<br>($V_{IL}$ = 0.5 V) | $I_{IL}$ | – | – | -250 | µA |
| Input Current – High Logic State ($V_{IH}$ = 2.7 V)<br>($V_{IH}$ = 5.5 V) | $I_{IH}$ | – | – | 40<br>100 | µA |
| Input Clamp Voltages<br>($I_{IK}$ = 18 mA) | $V_{IK}$ | – | – | -1.5 | V |
| Output Voltage – Low Logic State<br>($I_{OL}$ = 24 mA for $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and R/$\overline{\text{W}}$)<br>($I_{OL}$ = 8.0 mA for Row En, Ref En, $\overline{\text{MC}}$, $\overline{\text{Ref Req}}$) | $V_{OL}$ | <br>–<br>– | <br>–<br>– | <br>0.5<br>0.5 | V |
| Output Voltage – High Logic State<br>($I_{OH}$ = -1.0 mA for $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and R/$\overline{\text{W}}$)<br>($I_{OH}$ = -0.4 mA for Row En, Ref En, and $\overline{\text{MC}}$)<br>$I_{OH}$ = -0.2 mA for $\overline{\text{Ref Req}}$<br>(Note: $\overline{\text{Ref Req}}$ output has internal 5.0 k resistive pullup to $V_{CC}$.) | $V_{OH}$ | <br>3.0<br>2.4<br>2.4 | <br>–<br>–<br>– | <br>–<br>–<br>– | V |
| Power Supply Current – During R/W or Refresh<br>– During Idle | $I_{CC}$ | – | – | 65<br>40 | mA |
| Output Short-Circuit Current<br>($V_{OL}$ = 0 V for Row En, Ref En, and $\overline{\text{MC}}$) | $I_{OS}$ | -10 | – | -55 | mA |

FIGURE 1 – TYPICAL $t_{PT1,3,\text{and}4}$ (HIGH TO LOW) versus LOAD CAPACITANCE – $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and R/$\overline{\text{W}}$



**SWITCHING CHARACTERISTICS** (Unless otherwise noted, $V_{CC}$ = 5.0 V, $T_A$ = 25°C

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Times (Full AC Load – All Outputs) | | | | | ns |
| MC to $\overline{MC}$ – Low to High | $t_{PLH(\overline{MC})}$ | – | 7.0 | 14 | |
| MC to $\overline{MC}$ – High to Low | $t_{PHL(\overline{MC})}$ | – | 9.0 | 17 | |
| t1 to $\overline{RAS}$ | $t_{PT1}$ | 18 | 26 | 40 | |
| t2 to Row En | $t_{PT2}$ | 16 | 21 | 35 | |
| t3 to $\overline{CAS}$ | $t_{PT3}$ | 17 | 26 | 45 | |
| t4 to R/W | $t_{PT4}$ | 16 | 22 | 45 | |
| t5 to $\overline{CAS}$ | $t_{PT5C}$ | 22 | 30 | 42 | |
| to $\overline{RAS}$ | $t_{PT5R}$ | 19 | 26 | 40 | |
| to R/W | $t_{PT5W}$ | 30 | 42 | 58 | |
| to Row En (Refresh) | $t_{PT5ER}$ | 30 | 50 | 65 | |
| to Row En (R/W) | $t_{PT5E}$ | 25 | 32 | 48 | |
| to Refresh En | $t_{PT5F}$ | 22 | 46 | 55 | |
| Ref Clk to $\overline{Ref\ Req}$ | $t_{PCQ}$ | 10 | 17 | 27 | |
| Ref Grant to Row En<br>to Ref En | $t_{PGS}$ | 20 | 30 | 43 | |
| t1 to $\overline{Ref\ Req}$ (Ref only) Note 2 | $t_{PTQ}$ | 22 | 60 | 75 | |
| Setup Times (Full AC Load – All Pins) | | | | | ns |
| Ref Clk before Ref Grant | $t_{su(RC)}$ | 35 | – | – | |
| A12, A13 before t1 | $t_{su(A)}$ | 10 | – | – | |
| R/W Input before t4 | $t_{su(R/W)}$ | 33 | – | – | |
| $\overline{CE}$ before t1 | $t_{su(\overline{CE})}$ | 20 | – | – | |
| Ref Grant before t1 | $t_{su(RG)}$ | 50 | – | – | |
| Hold Times (Full AC Load – All Pins) | | | | | ns |
| A12, A13 after t5 | $t_{h(A)}$ | 15 | – | – | |
| $\overline{CE}$ after t1 | $t_{h(\overline{CE})}$ | 0 | – | – | |
| R/W after t4 | $t_{h(R/W)}$ | 0 | – | – | |
| MC Rising after t1 Rising | $t_{h(MC)}$ | 30 | – | – | |
| Minimum Delay Times (Note 2 – Full AC Load – All Pins) | | | | | ns |
| t1 Low to High to t2 Low to High | $t_{d(1-2)}$ | 30 | – | – | |
| t1 Low to High to t4 Low to High | $t_{d(1-4)}$ | 33 | – | – | |
| t2 Low to High to t3 Low to High | $t_{d(2-3)}$ | 30 | – | – | |
| t3 Low to High to t5 Low to High | $t_{d(3-5)}$ | 30 | – | – | |
| Minimum Pulse Widths | | | | | ns |
| t1 through t5 Low | $t_{WL(t)}$ | 30 | – | – | |
| High | $t_{WH(t)}$ | 30 | – | – | |
| MC | $t_{W(MC)}$ | 30 | – | – | |
| Ref Grant | $t_{W(RG)}$ | 25 | – | – | |

**Note 2:** **$\overline{Ref.\ Req.}$ has an internal 5.0 kΩ pullup to $V_{CC}$. If faster propagation delay is required ($t_{PTQ}$), then an external registor can be added in parallel to the internal one to decrease the propagation delay. The value of resistance needed is a function of the capacitive loaded connection to $\overline{Ref.\ Req.}$ The minimum value of R that can be used is 5.0 V/8.0 mA = 625 Ω, assuming there are no other dc loads connected to that pin.**

**Note 3:** **If delays between t1–t5 are less than the minimum specified, the succeeding outputs may not switch.**

**AC LOADS (Note 4)**

| | |
|---|---|
| R/W and $\overline{CAS}$ Outputs | 450 pF to Gnd* |
| $\overline{RAS}$ Outputs | 150 pF to Gnd* |
| $\overline{MC}$, Row En, Ref En, and $\overline{Ref\ Req}$ Outputs | 15 pF to Gnd* |

*Includes probe and jig capacitance.

**Note 4:** **All outputs can drive larger capacitive loads than those shown with a small decrease in speed. See Figure 1.**

## PIN DESCRIPTION TABLE

| Name | No. | Function |
|---|---|---|
| $\overline{\text{RAS1}}$ *<br>$\overline{\text{RAS2}}$<br>$\overline{\text{RAS3}}$<br>$\overline{\text{RAS4}}$ | 16<br>15<br>14<br>13 | Row Address Strobe pins which connect to each of the dynamic RAMs to latch in row address on memory chips. Decoded to 1 of 4 during R/W cycle. All 4 go low during refresh cycle. |
| $\overline{\text{CAS}}$ * | 11 | Column Address Strobe pin which connects to each dynamic RAM to latch in column address. |
| R/W Out * | 10 | This pin signals the dynamic RAM whether the RAM is to be read from or written into. |
| Row En | 9 | Row Enable output which goes to the MC3232A (MC3242A). It signals the Address Multiplexer that the lower half (Row Addresses) or the upper half (Column Addresses) of the address lines are to be multiplexed into the dynamic RAM address inputs. A Logic 1 on this output indicates the Row Addresses, and a Logic 0 indicates Column Addresses. |
| Ref En | 8 | Refresh Enable output. A Logic 1 signals the Address Multiplexer that a refresh cycle is to be done, and a Logic 0 indicates that address multiplexing should be done. |
| $\overline{\text{CE}}$ | 22 | Chip Enable Input. A Logic 1 on this pin disables all chip functions, except that of Refresh and the $\overline{\text{MC}}$ output. $\overline{\text{CE}}$ must be low during t1 low to high transition to initiate R/W cycle. Once t1 is initiated, the cycle is independent of $\overline{\text{CE}}$. |
| R/W In | 7 | The Read/Write input pin receives information from the M6800 MPU as to the direction of data exchange in the dynamic RAM. It transmits a Logic 0 to the R/W output for a Write Cycle and a Logic 1 for a Read Cycle. |
| A13 (A15)<br>A12 (A14) | 17<br>18 | Upper Order Address lines from the M6800. These two inputs decode to four signals controlling the four $\overline{\text{RAS}}$ outputs. A14 and A15 apply to 16K RAMs. |
| MC | 23 | Memory Clock input from MC6875 clock or other signal source. The rising edge of MC must occur after the rising edge of t1 to avoid aborting the refresh cycle. When MC rises, it resets an internal flag that will terminate refresh at the end of the current cycle. Failure to reset the flag forces the 3480 to refresh every cycle thereafter. MC can be connected to t2 or t3 in noncritical applications. |
| $\overline{\text{MC}}$ | 1 | The buffered complement output of MC. It is a buffered output which may be used to drive the circuitry creating the time delays used on inputs t1 through t5. |
| t1<br>t2<br>t3<br>t4<br>t5 | 2<br>3<br>4<br>5<br>6 | These pins use external timing inputs to sequentially select the outputs to be enabled. They are positive-edge triggered inputs. Assuming a Read/Write cycle is to be executed, a positive edge on t1 forces a logic 0 on one of the four $\overline{\text{RAS}}$ outputs as determined by the A12/14, A13/15 inputs. After a delay, a positive edge on t2 causes Row En to go to a Logic 0, providing address-multiplexing information to the MC3232A or MC3242A. t3 enables the $\overline{\text{CAS}}$ output and it goes low. t4 enables the R/W output and it goes low, assuming the R/W input was low. t5 resets all the outputs to a Logic 1 (with the exception of $\overline{\text{MC}}$, Ref En, and $\overline{\text{Ref Req}}$). The inputs t1, t2, t3, and t5 are daisy-chained, so they must be sequentially driven to obtain the desired output signals. t4 can be driven at any time after t1. |
| Ref Clk | 21 | The 32 kHz (64 kHz) Refresh Clock signals this pin that another refresh cycle is required. It is a positive-edge triggered input, and upon triggering, the $\overline{\text{Ref Req}}$ pin goes to a Logic 0. |
| $\overline{\text{Ref Req}}$ | 20 | The $\overline{\text{Refresh Request}}$ output acts as an input to the MPU system, requesting a refresh cycle. This output has a 5 kΩ pullup resistor to the $V_{CC}$ supply to allow wire-ORing if desired. |
| Ref Grant | 19 | Through the Refresh Grant input, the MC6875 initiates a refresh cycle. This input is positive-edge triggered and is enabled only after the $\overline{\text{Ref Req}}$ pin has gone low. This allows the MC3480 to discern between a Refresh Grant or a DMA Grant even though they appear on the same line. When employing both dynamic memory (refresh) and DMA in a microprocessor-based system with a combined Refresh/DMA Request control on the clock, provision must be made for holding off a DMA request during a refresh period (and visa versa). If this provision is not made, clock stretching (cycle stealing) will continue indefinitely and dynamic microprocessor data will be lost. The positive edge on Ref Grant causes Row En output to go low and Ref En output to go high. This signals the MC3232A (MC3242A) that a refresh address is required. The refresh cycle occurs with the succeeding pulses on t1-t5. A positive edge on t1 causes $\overline{\text{Ref Req}}$ to go high and all the $\overline{\text{RAS}}$ outputs to go low. A positive going edge on t2 causes no change in the outputs, since it controls the address multiplexing (Row En) during the Read/Write cycles. There is no output change when t3 and t4 go high because no $\overline{\text{CAS}}$ or R/W signal is needed during refresh. A positive edge on t5 resets the $\overline{\text{RAS}}$ and Row En to a Logic 1 state, and Ref En to a Logic 0 state, ready for the next Read/Write cycle. |
| $V_{CC}$ | 24 | +5.0 V supply. A 0.1 μF capacitor is recommended to bypass pin 24 to ground. |
| Gnd | 12 | System Ground. |

*These outputs are designed to drive the highly capacitive inputs of multiple dynamic RAMs/(150 pF for $\overline{\text{RAS}}$ outputs, and 450 pF for $\overline{\text{CAS}}$ and R/W outputs). Consequently, these outputs have no short-circuit limit and must be handled accordingly. Good high capacitance load driving techniques usually include a 10 Ω or greater series damping resistor. It is highly recommended that this be done on $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and R/W outputs of the MC3480. The effect of these series damping resistors on rise and fall times must be included in timing considerations.

NOTE: All other outputs are LS/TTL totem-pole configuration unless otherwise noted.

## TIME DELAY INFORMATION

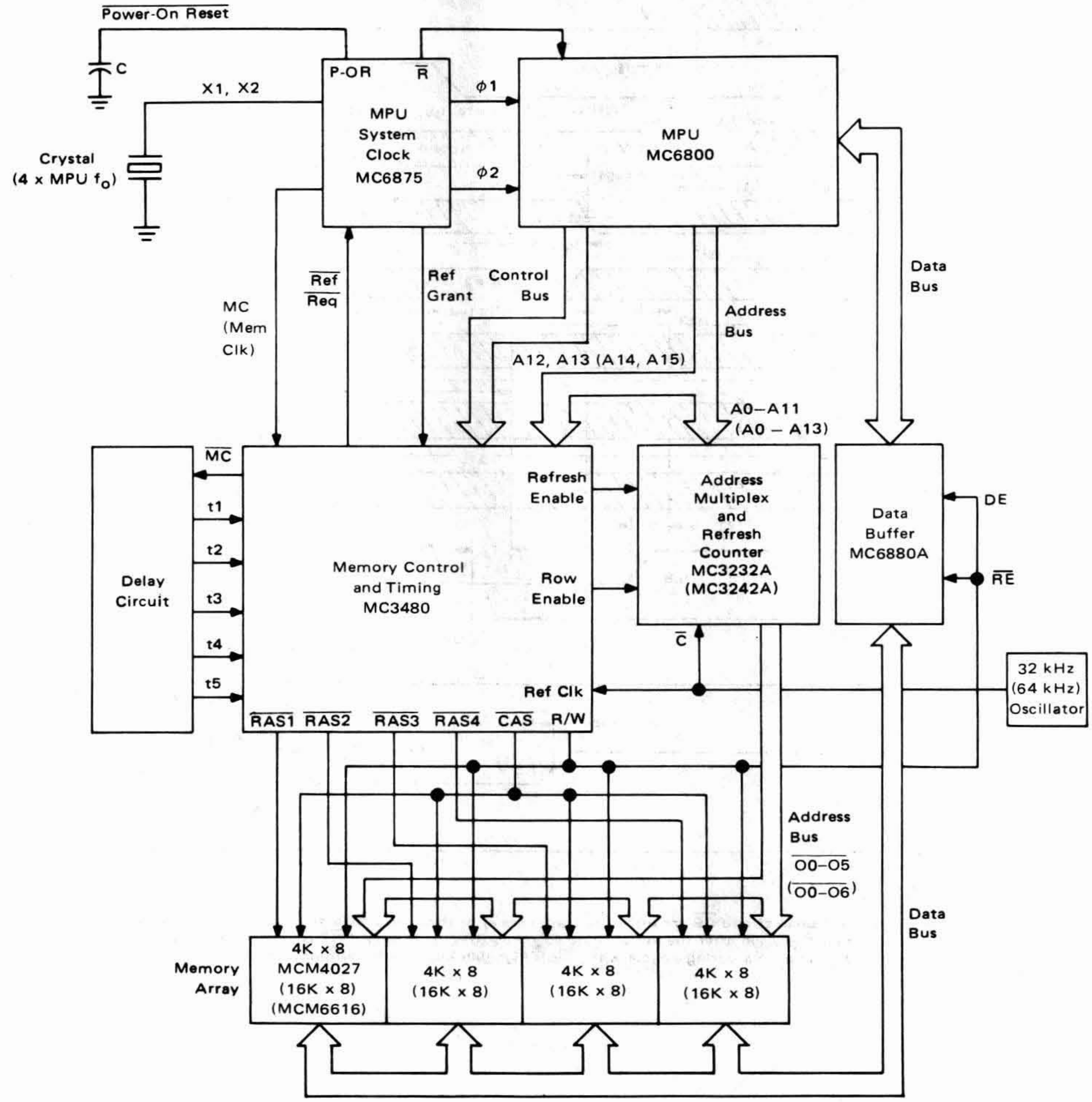
### TIMING REQUIREMENT CONSTRAINTS

| | |
|---|---|
| Δt1 | Minimum is determined by MPU Address Delay ($t_{AD}$), plus RAM Row Address Set-Up Time ($t_{ASR}$), minus MC3480 Propagation Delay ($t_{PT1}$). |
| Δt2 - Δt1 | Minimum is determined by RAM Row Address Hold Time ($t_{RAH}$) minus the minimum MC3232A/3242A Row Enable to Output Delay ($t_{00MIN}$). |
| Δt3 - Δt2 | Minimum is determined by RAM Column Address Set-Up Time ($t_{ASC\ minimum}$) plus maximum MC3232A/3242A Row Enable to Output Delay ($t_{001MAX}$). |
| Δt4 - Δt3 | No Minimum |
| Δt5 - Δt3 | Minimum is determined by RAM minimum $\overline{\text{CAS}}$ Pulse Width ($t_{CAS}$) or Access Time from $\overline{\text{CAS}}$ ($t_{CAC}$) plus Data Set-Up Time of MPU ($t_{DSR}$). |
| Δt5 - Δt4 | Minimum is determined by the RAM minimum Write Pulse Width ($t_{WP}$). |

Note: Also required in computing time delays are the various delays incurred by the particular delay scheme used; i.e., delays between 4 x $f_o$, 2 x $f_o$, and $f_o$ from the MC6875 which are used as inputs or the gate delays of the gates used in Figures 5A through 5C.

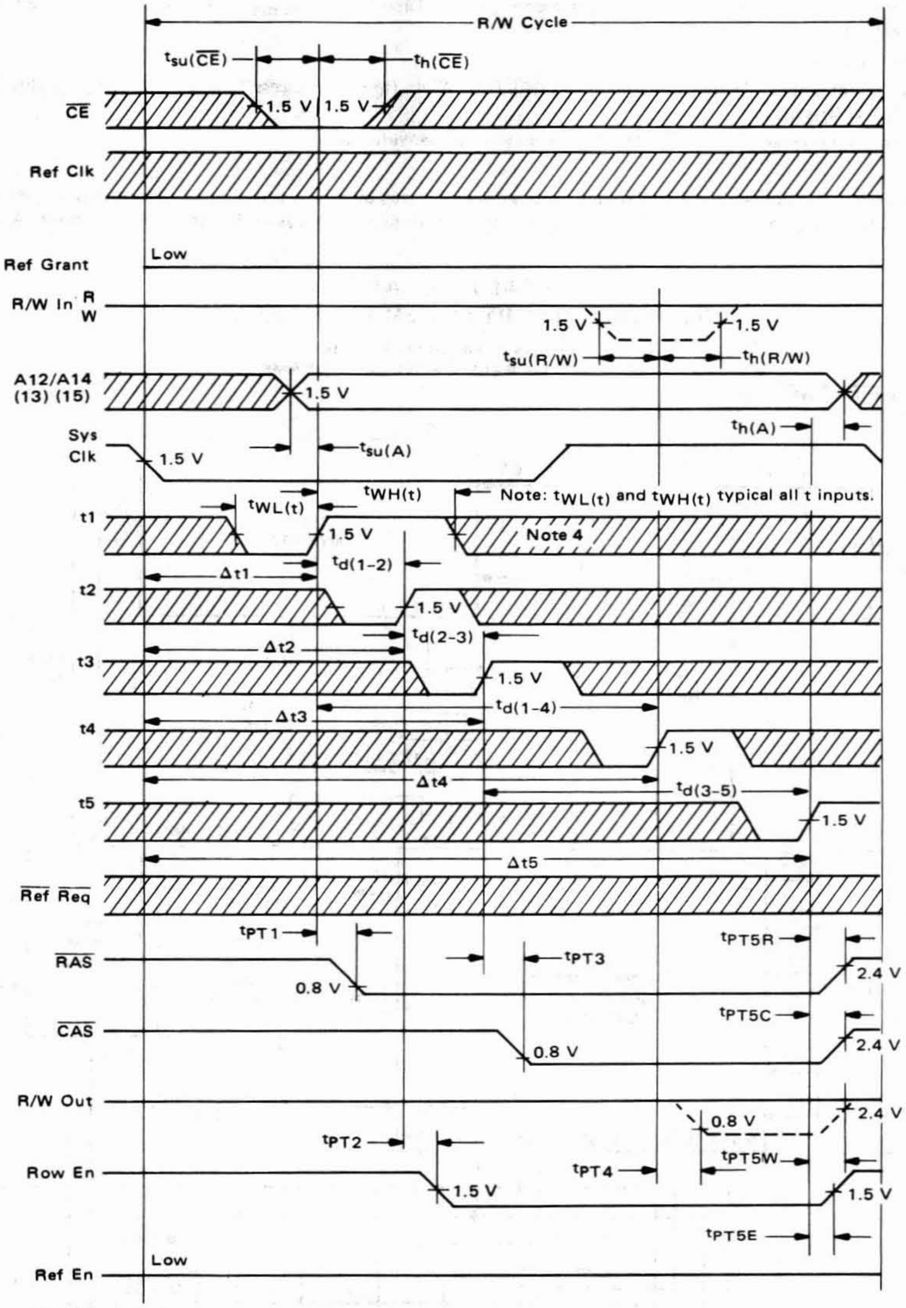
## TYPICAL APPLICATION
## 16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate part types or values for 16K x 1 RAMs



Power-On Reset
C
X1, X2
Crystal (4 x MPU $f_o$)
P-OR
$\overline{\text{R}}$
MPU System Clock MC6875
φ1
φ2
MPU MC6800
MC (Mem Clk)
$\overline{\text{Ref Req}}$
Ref Grant
Control Bus
Address Bus
Data Bus
A12, A13 (A14, A15)
A0–A11 (A0 – A13)
$\overline{\text{MC}}$
t1
t2
t3
t4
t5
Delay Circuit
Memory Control and Timing MC3480
Refresh Enable
Row Enable
Ref Clk
$\overline{\text{RAS1}}$
$\overline{\text{RAS2}}$
$\overline{\text{RAS3}}$
$\overline{\text{RAS4}}$
$\overline{\text{CAS}}$
R/W
Address Multiplex and Refresh Counter MC3232A (MC3242A)
$\overline{\text{C}}$
Data Buffer MC6880A
DE
$\overline{\text{RE}}$
32 kHz (64 kHz) Oscillator
Address Bus
$\overline{\text{O0–O5}}$
($\overline{\text{O0–O6}}$)
Data Bus
Memory Array
4K x 8 MCM4027 (16K x 8) (MCM6616)
4K x 8 (16K x 8)
4K x 8 (16K x 8)
4K x 8 (16K x 8)

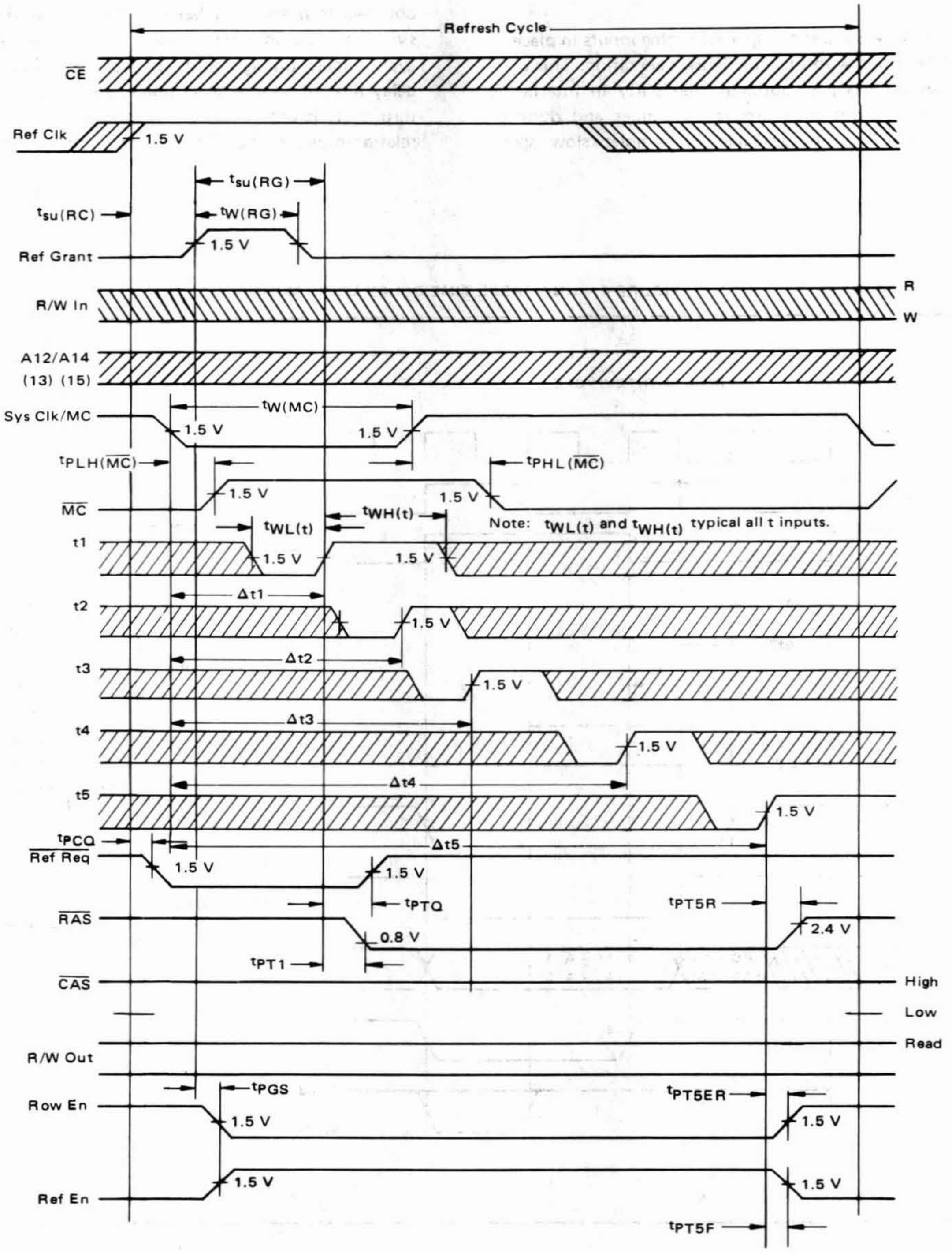
FIGURE 2 – READ/WRITE TIMING CYCLE


R/W Cycle
$t_{su(\overline{CE})}$
$t_{h(\overline{CE})}$
$\overline{CE}$
1.5 V
1.5 V
Ref Clk
Ref Grant
Low
R/W In R W
1.5 V
1.5 V
$t_{su(R/W)}$
$t_{h(R/W)}$
A12/A14 (13) (15)
1.5 V
$t_{h(A)}$
Sys Clk
1.5 V
$t_{su(A)}$
t1
$t_{WL(t)}$
$t_{WH(t)}$
Note: $t_{WL(t)}$ and $t_{WH(t)}$ typical all t inputs.
1.5 V
Note 4
$\Delta t1$
$t_{d(1-2)}$
t2
1.5 V
$\Delta t2$
$t_{d(2-3)}$
t3
1.5 V
$\Delta t3$
$t_{d(1-4)}$
t4
1.5 V
$\Delta t4$
$t_{d(3-5)}$
t5
1.5 V
$\Delta t5$
$\overline{Ref\ Req}$
$t_{PT1}$
$t_{PT5R}$
$\overline{RAS}$
$t_{PT3}$
0.8 V
2.4 V
$t_{PT5C}$
$\overline{CAS}$
0.8 V
2.4 V
R/W Out
0.8 V
2.4 V
$t_{PT2}$
$t_{PT5W}$
$t_{PT4}$
Row En
1.5 V
1.5 V
$t_{PT5E}$
Low
Ref En

▨ = Don't care.

**NOTE 4:** Although t1 and $\overline{CE}$ are shown as don't care after their respective minimum hold times, t1 may rise again after the initial rising edge in a R/W cycle only if $\overline{CE}$ is low. Bringing t1 high a second time during a cycle when $\overline{CE}$ is high will improperly terminate the cycle.

FIGURE 3 – REFRESH TIMING CYCLE

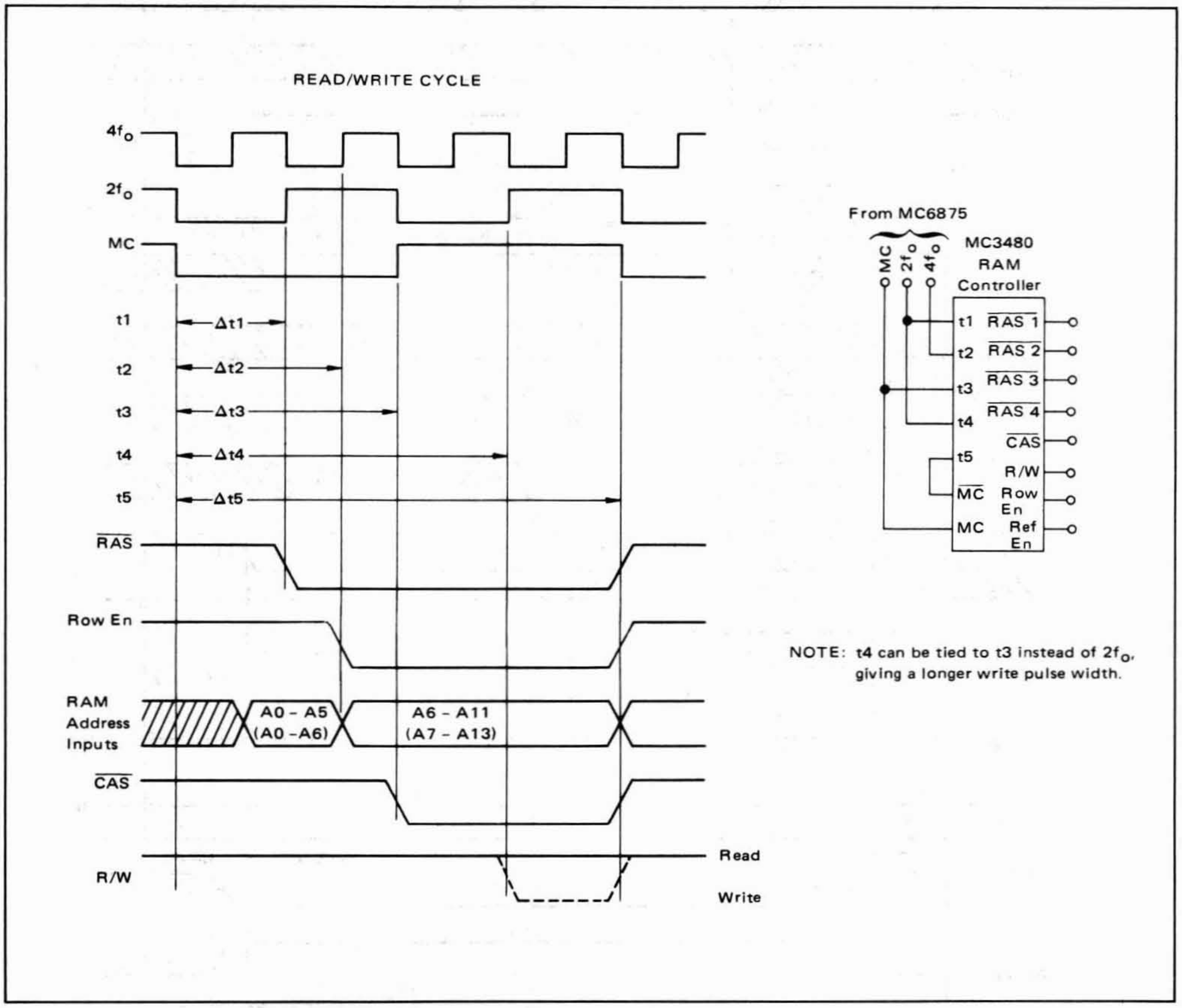

Refresh Cycle
CE
Ref Clk
1.5 V
tsu(RG)
tsu(RC)
tW(RG)
Ref Grant
1.5 V
R/W In
R
W
A12/A14
(13) (15)
Sys Clk/MC
tW(MC)
1.5 V
1.5 V
tPLH(MC)
tPHL(MC)
MC
1.5 V
1.5 V
tWL(t)
tWH(t)
Note: tWL(t) and tWH(t) typical all t inputs.
t1
1.5 V
1.5 V
t2
Δt1
1.5 V
t3
Δt2
1.5 V
t4
Δt3
1.5 V
t5
Δt4
1.5 V
tPCQ
Ref Req
Δt5
1.5 V
1.5 V
tPTQ
tPT5R
RAS
0.8 V
2.4 V
tPT1
CAS
High
Low
R/W Out
Read
tPGS
tPT5ER
Row En
1.5 V
1.5 V
1.5 V
1.5 V
Ref En
tPT5F

## APPLICATIONS INFORMATION

### GENERAL DESCRIPTION

The MC3480 uses five general timing inputs in place of a master clock with on-chip timing generation. This gives the system designer optimum flexibility in interfacing with the various microprocessor families and dynamic memories that are available. In simpler slow speed systems, the timing signals required can be directly obtained from those available from the microprocessor. In systems requiring high speed memory/microprocessor cycle times, timing input t1-t5 can be obtained using delay lines or a range of techniques as shown in Figures 4 thru 8. It is only necessary to maintain the time delay relationships shown under time delay information.

FIGURE 4 – UNIVERSAL TIME DELAY USING MC6875


READ/WRITE CYCLE
4f_o
2f_o
MC
t1
t2
t3
t4
t5
Δt1
Δt2
Δt3
Δt4
Δt5
RAS
Row En
RAM Address Inputs
A0 - A5
(A0 - A6)
A6 - A11
(A7 - A13)
CAS
R/W
Read
Write
From MC6875
MC
2f_o
4f_o
MC3480 RAM Controller
t1
t2
t3
t4
t5
MC
MC
RAS 1
RAS 2
RAS 3
RAS 4
CAS
R/W
Row En
Ref En

NOTE: t4 can be tied to t3 instead of $2f_o$, giving a longer write pulse width.

**FIGURE 5 – ALTERNATE TIME DELAYS USING MC6875**
**(Read/Write Cycle Shown)**

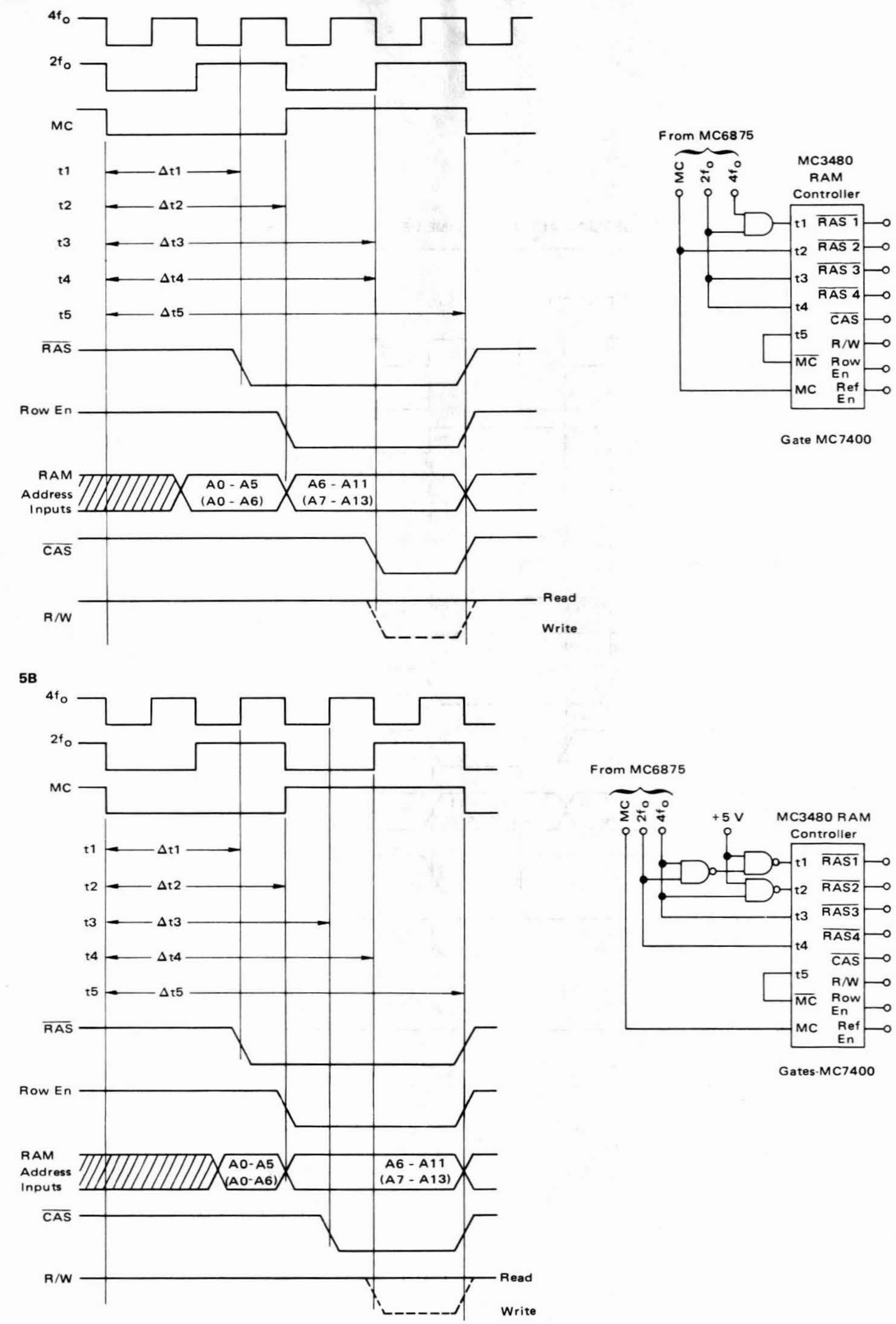
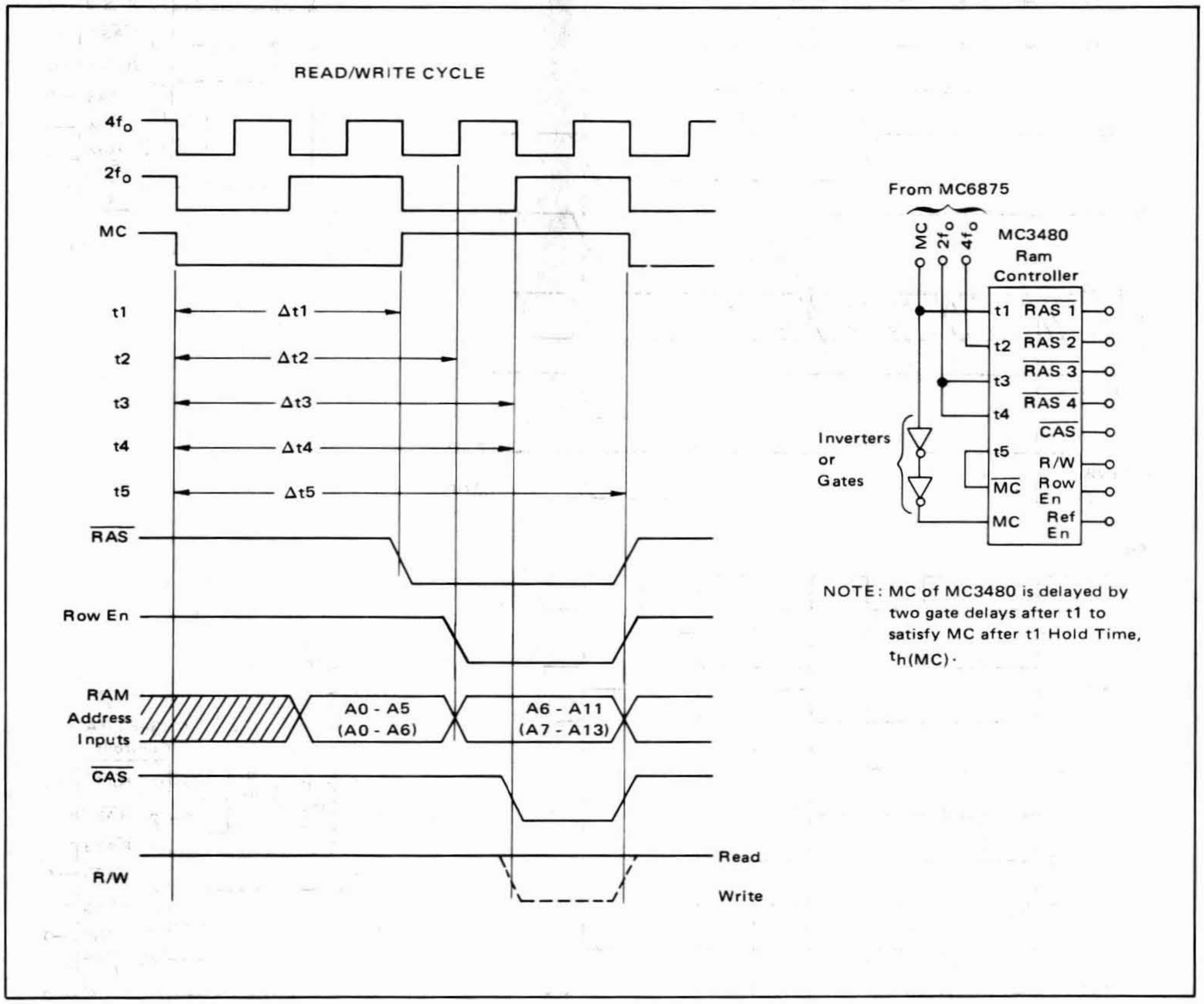
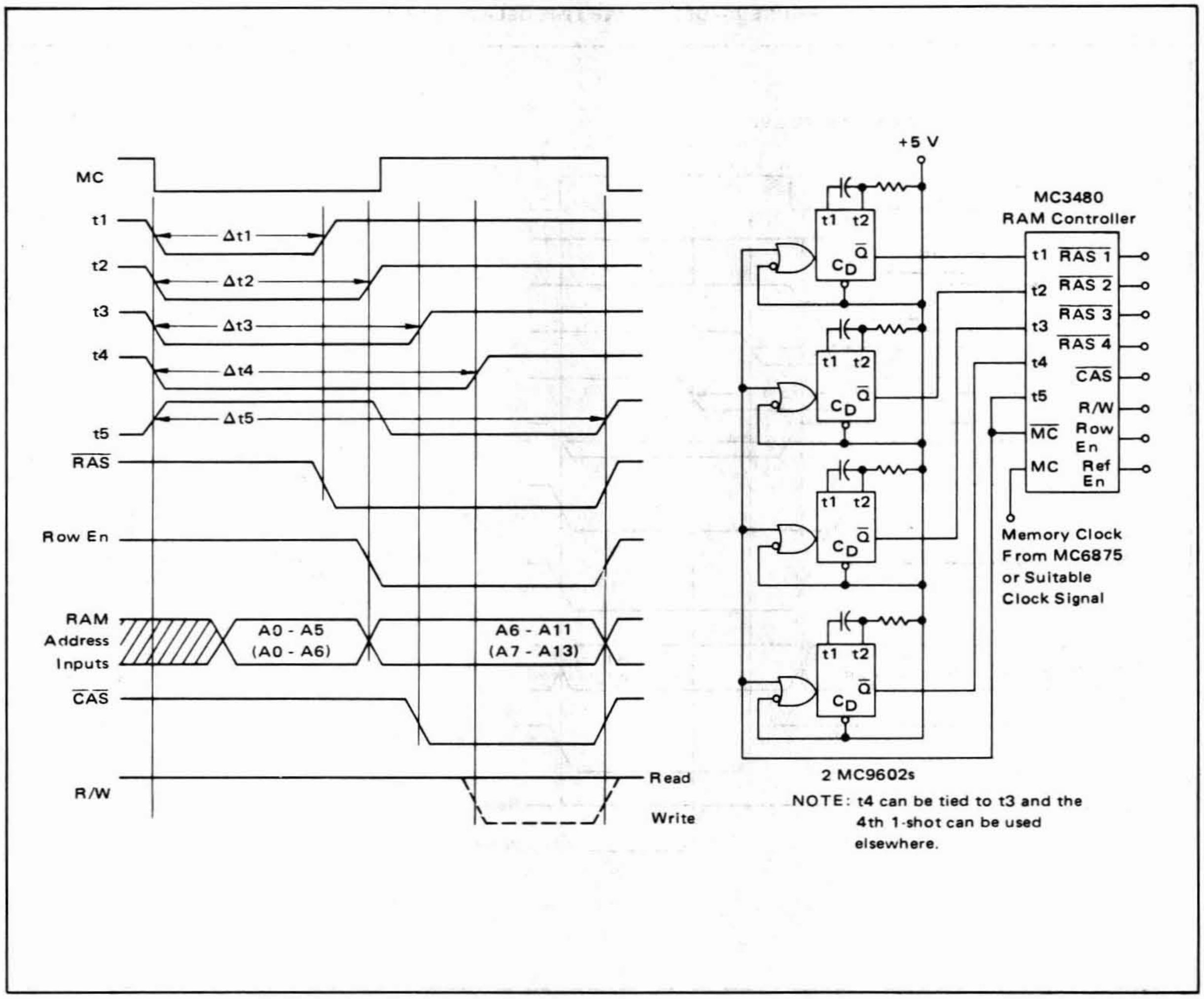

5A
4f$_o$
2f$_o$
MC
t1
Δt1
t2
Δt2
t3
Δt3
t4
Δt4
t5
Δt5
$\overline{RAS}$
Row En
RAM Address Inputs
A0 - A5
(A0 - A6)
A6 - A11
(A7 - A13)
$\overline{CAS}$
R/W
Read
Write
From MC6875
MC
2f$_o$
4f$_o$
MC3480 RAM Controller
t1
t2
t3
t4
t5
$\overline{MC}$
MC
$\overline{RAS\ 1}$
$\overline{RAS\ 2}$
$\overline{RAS\ 3}$
$\overline{RAS\ 4}$
$\overline{CAS}$
R/W
Row En
Ref En
Gate MC7400
5B
4f$_o$
2f$_o$
MC
t1
Δt1
t2
Δt2
t3
Δt3
t4
Δt4
t5
Δt5
$\overline{RAS}$
Row En
RAM Address Inputs
A0-A5
(A0-A6)
A6 - A11
(A7 - A13)
$\overline{CAS}$
R/W
Read
Write
From MC6875
MC
2f$_o$
4f$_o$
+5 V
MC3480 RAM Controller
t1
t2
t3
t4
t5
$\overline{MC}$
MC
$\overline{RAS1}$
$\overline{RAS2}$
$\overline{RAS3}$
$\overline{RAS4}$
$\overline{CAS}$
R/W
Row En
Ref En
Gates-MC7400

FIGURE 5C – ALTERNATE TIME DELAYS USING MC6875


READ/WRITE CYCLE
4fo
2fo
MC
t1
t2
t3
t4
t5
Δt1
Δt2
Δt3
Δt4
Δt5
RAS
Row En
RAM Address Inputs
A0 - A5
(A0 - A6)
A6 - A11
(A7 - A13)
CAS
R/W
Read
Write
From MC6875
MC
2fo
4fo
MC3480
Ram
Controller
t1
t2
t3
t4
t5
MC
MC
RAS 1
RAS 2
RAS 3
RAS 4
CAS
R/W
Row En
Ref En
Inverters or Gates

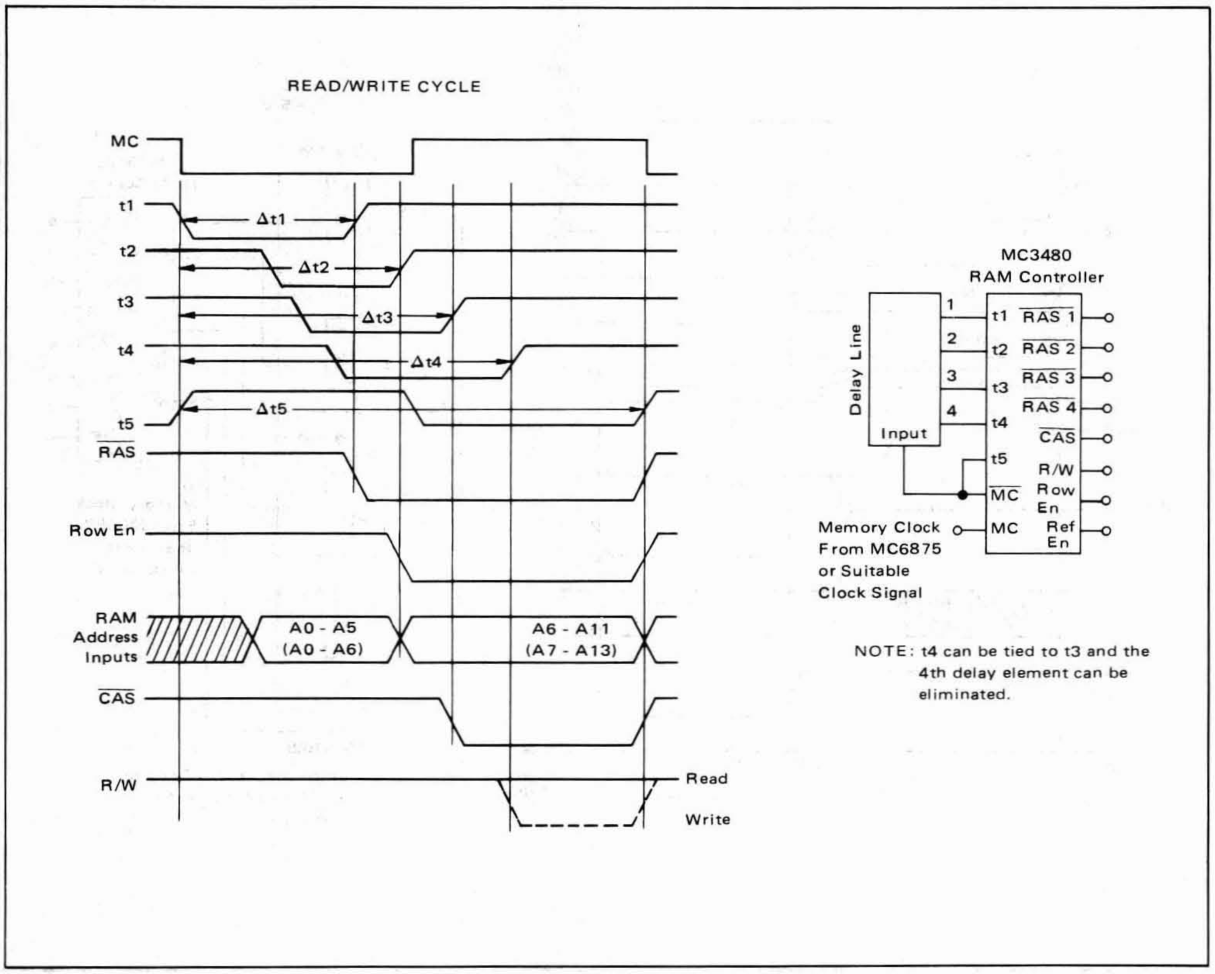
NOTE: MC of MC3480 is delayed by two gate delays after t1 to satisfy MC after t1 Hold Time, $t_{h(MC)}$.

FIGURE 6 – ONE SHOT TIME DELAY METHOD


MC
t1
t2
t3
t4
t5
RAS
Row En
RAM Address Inputs
CAS
R/W
Δt1
Δt2
Δt3
Δt4
Δt5
A0 - A5
(A0 - A6)
A6 - A11
(A7 - A13)
Read
Write
+5 V
t1 t2
$C_D$ $\overline{Q}$
MC3480
RAM Controller
t1
t2
t3
t4
t5
$\overline{MC}$
MC
$\overline{RAS\ 1}$
$\overline{RAS\ 2}$
$\overline{RAS\ 3}$
$\overline{RAS\ 4}$
$\overline{CAS}$
R/W
Row En
Ref En
Memory Clock
From MC6875
or Suitable
Clock Signal
2 MC9602s

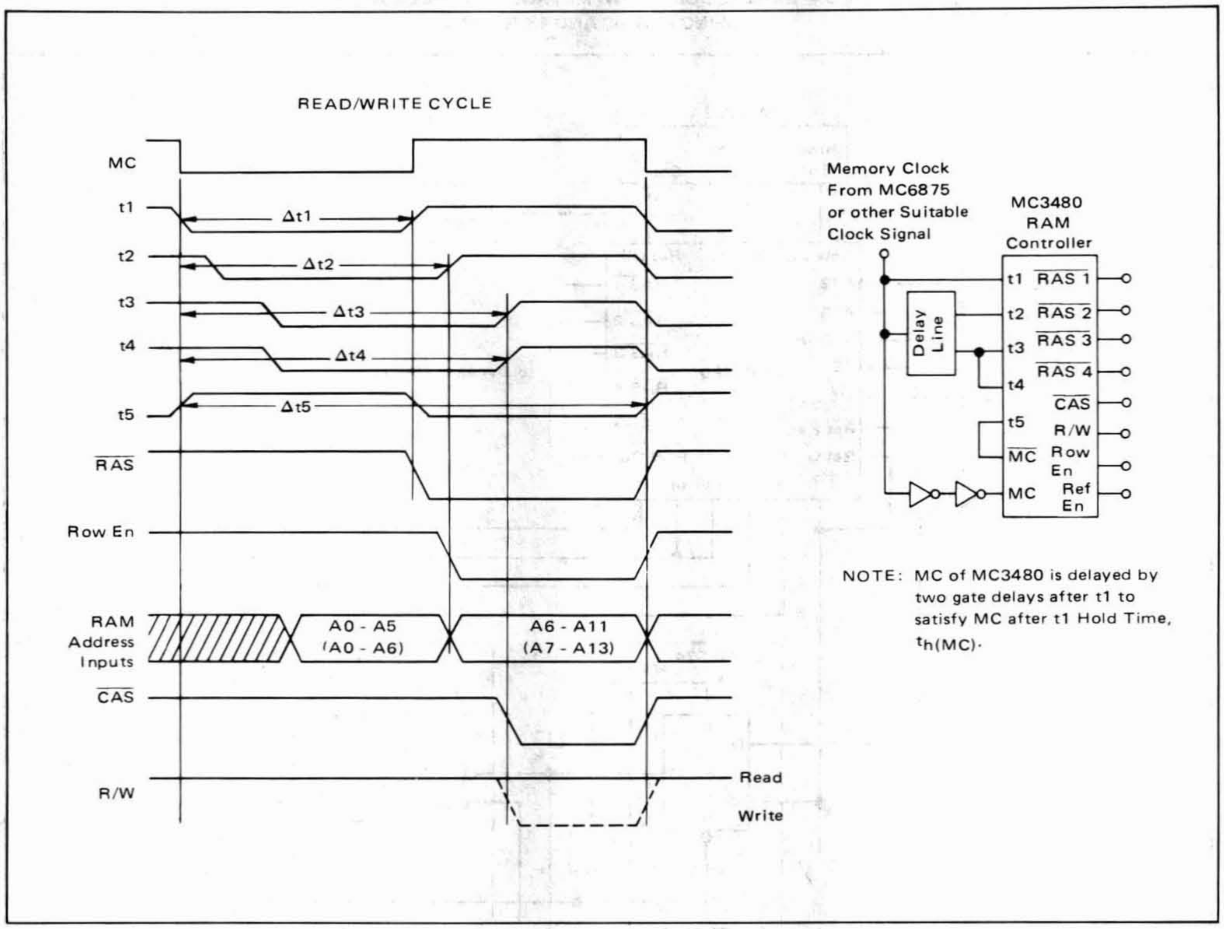
NOTE: t4 can be tied to t3 and the 4th 1-shot can be used elsewhere.

FIGURE 7 — DELAY LINE TIME DELAY METHOD


READ/WRITE CYCLE
MC
t1
Δt1
t2
Δt2
t3
Δt3
t4
Δt4
t5
Δt5
RAS
Row En
RAM Address Inputs
A0 - A5
(A0 - A6)
A6 - A11
(A7 - A13)
CAS
R/W
Read
Write
MC3480
RAM Controller
Delay Line
Input
1
2
3
4
t1
t2
t3
t4
t5
MC
MC
RAS 1
RAS 2
RAS 3
RAS 4
CAS
R/W
Row En
Ref En
Memory Clock From MC6875 or Suitable Clock Signal

NOTE: t4 can be tied to t3 and the 4th delay element can be eliminated.

FIGURE 8 – DELAY LINE TIME DELAY (ALTERNATE METHOD)


READ/WRITE CYCLE
MC
t1
Δt1
t2
Δt2
t3
Δt3
t4
Δt4
t5
Δt5
$\overline{RAS}$
Row En
RAM Address Inputs
A0 - A5 (A0 - A6)
A6 - A11 (A7 - A13)
$\overline{CAS}$
R/W
Read
Write
Memory Clock From MC6875 or other Suitable Clock Signal
MC3480 RAM Controller
Delay Line
t1
t2
t3
t4
t5
$\overline{MC}$
MC
$\overline{RAS\ 1}$
$\overline{RAS\ 2}$
$\overline{RAS\ 3}$
$\overline{RAS\ 4}$
$\overline{CAS}$
R/W
Row En
Ref En

NOTE: MC of MC3480 is delayed by two gate delays after t1 to satisfy MC after t1 Hold Time, $t_{h(MC)}$.

## REFRESH CONSIDERATIONS

The MC3480/MC3232A (MC3242A) memory control system can be used with either cycle steal or transparent refresh methods. Figure 9 shows one transparent technique employing refresh during $\phi 2$ low in an M6800 microprocessor-based system. Using this technique requires that the memory be capable of completing a Read/Write Cycle and a Refresh Cycle sequentially during the M6800 cycle. The minimum cycle time at the time of printing for dynamic multiplexed RAMs is 320 ns, therefore limiting the microprocessor to 1.56 MHz operation. The D flip-flops of Figure 9 produce a trigger at the beginning of both $\phi 1$ and $\phi 2$. For a 1.0 MHz system, the t1 – t5 inputs should be adjusted for the following delays:

$\overline{RAS}$ falls at 150 ns (triggered by t1)
Row En falls at 250 ns (triggered by t2)
$\overline{CAS}$, R/W falls at 300 ns (triggered by t3)
t5 rises at 500 ns.

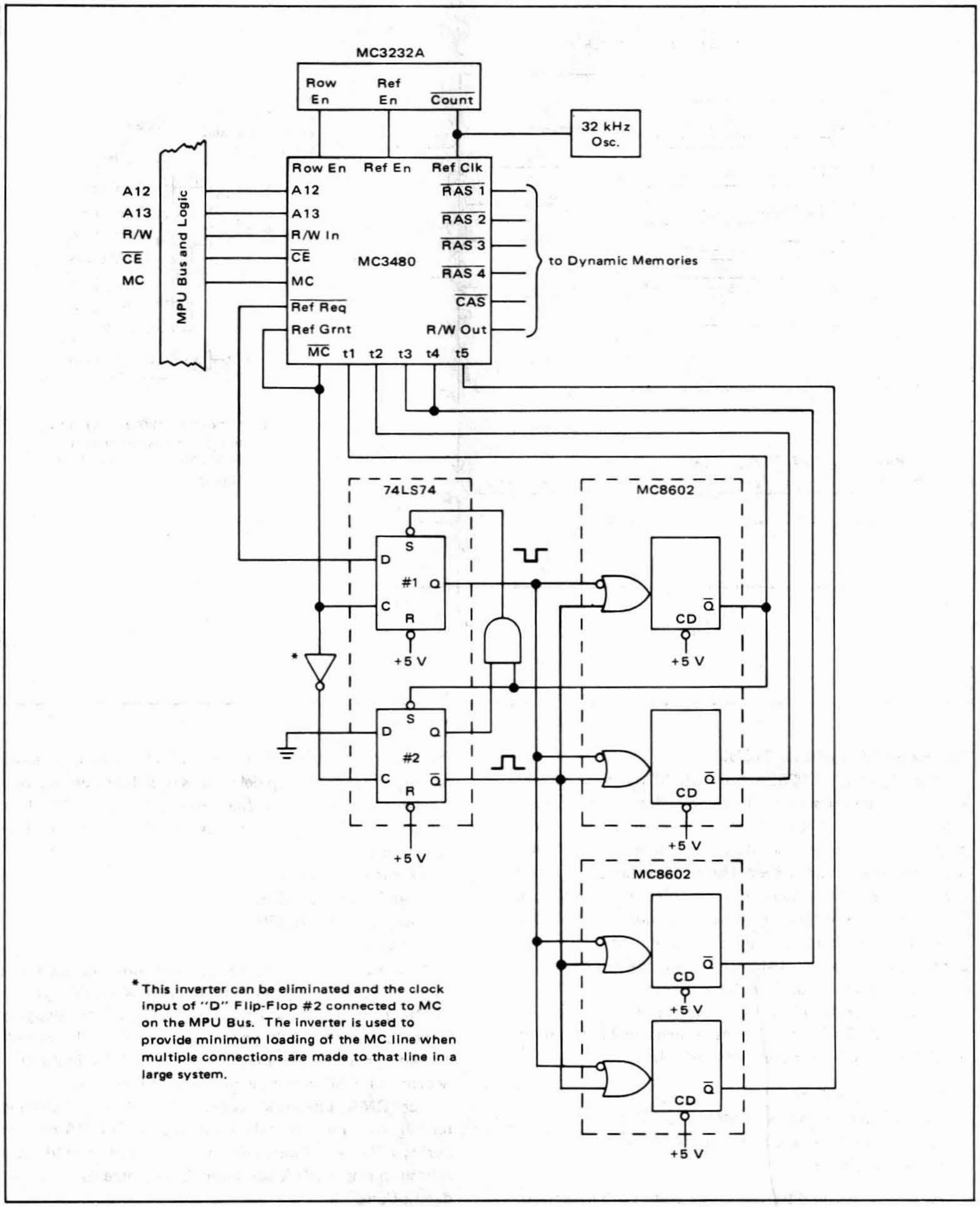
A delay line could be used to generate t1-t5 in place of the four monostables. For the 1.0 MHz system, it would require either two 5 tap delay lines with 50 ns per tap or a 10 tap line with 50 ns/tap. For use with a 600 kHz system, a delay line with 5 taps of 150 ns each could be used. For this case:

$\overline{RAS}$ falls at 150 ns
Row En falls at 300 ns
$\overline{CAS}$, R/W falls at 450 ns
t5 rises at 750 ns

Figure 10 shows typical refresh oscillator configurations for both 32 kHz ($f_{REF}$min for 4K) and 64 kHz ($f_{REF}$min for 16K). In the case of transparent refresh, if the designer is not concerned with power consumption, the refresh oscillator may be eliminated and the Ref Clk input connected to the MC input yielding a refresh every $\phi 1$.

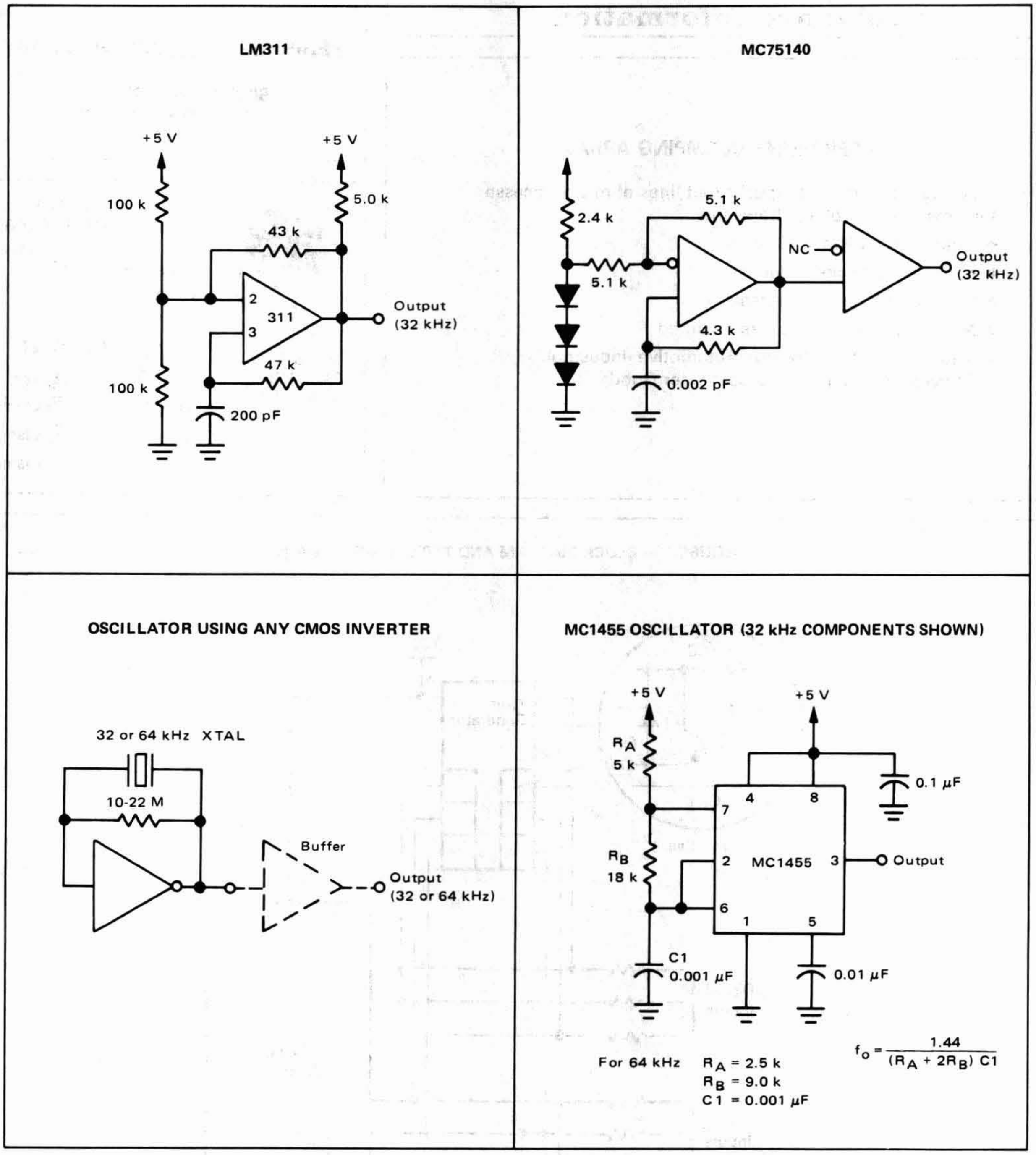
For DMA operation combined with cycle stealing refresh, care must be taken not to allow a DMA request during a $\overline{\text{Refresh Request}}$/Grant period and to hold off a refresh during a DMA operation. See comments under pin descriptions, Pin 19.

FIGURE 9 – EXAMPLE OF $\phi 2$ LOW METHOD OF HIDDEN REFRESH USING MC3480 AND 4K RAMS


MC3232A
Row En
Ref En
Count
32 kHz Osc.
MPU Bus and Logic
A12
A13
R/W
CE
MC
Row En
Ref En
Ref Clk
A12
A13
R/W In
CE
MC3480
MC
Ref Req
Ref Grnt
RAS 1
RAS 2
RAS 3
RAS 4
CAS
R/W Out
to Dynamic Memories
MC
t1
t2
t3
t4
t5
74LS74
S
D
#1
Q
C
R
+5 V
*
S
D
Q
#2
C
R
Q̄
+5 V
MC8602
Q̄
CD
+5 V
Q̄
CD
+5 V
MC8602
Q̄
CD
+5 V
Q̄
CD
+5 V

*This inverter can be eliminated and the clock input of "D" Flip-Flop #2 connected to MC on the MPU Bus. The inverter is used to provide minimum loading of the MC line when multiple connections are made to that line in a large system.

FIGURE 10 – SUGGESTED 32 kHz OSCILLATORS


LM311
+5 V
+5 V
100 k
5.0 k
43 k
2
311
3
Output
(32 kHz)
47 k
100 k
200 pF
MC75140
2.4 k
5.1 k
5.1 k
NC
Output
(32 kHz)
4.3 k
0.002 pF
OSCILLATOR USING ANY CMOS INVERTER
32 or 64 kHz XTAL
10-22 M
Buffer
Output
(32 or 64 kHz)
MC1455 OSCILLATOR (32 kHz COMPONENTS SHOWN)
+5 V
+5 V
RA
5 k
4
8
0.1 μF
7
RB
18 k
2
MC1455
3
Output
6
1
5
C1
0.001 μF
0.01 μF

For 64 kHz $R_A = 2.5$ k
$R_B = 9.0$ k
$C1 = 0.001\ \mu F$

$$f_o = \frac{1.44}{(R_A + 2R_B)\,C1}$$

**MOTOROLA**

# TCF6000

## Advance Information

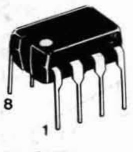
## PERIPHERAL CLAMPING ARRAY

SILICON MONOLITHIC
INTEGRATED CIRCUIT

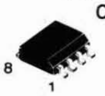
### PERIPHERAL CLAMPING ARRAY

. . . designed to protect input/output lines of microprocessor systems against voltage transients.

- Optimized for HMOS System
- Minimal Component Count
- Low Board Space Requirement
- No P.C.B. Track Crossovers Required
- Applications Areas Include Automotive, Industrial, Telecommunications and Consumer Goods



**P1 SUFFIX**
PLASTIC
PACKAGE
CASE 626-04



**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8

**PIN ASSIGNMENT**

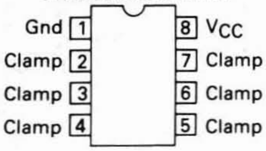
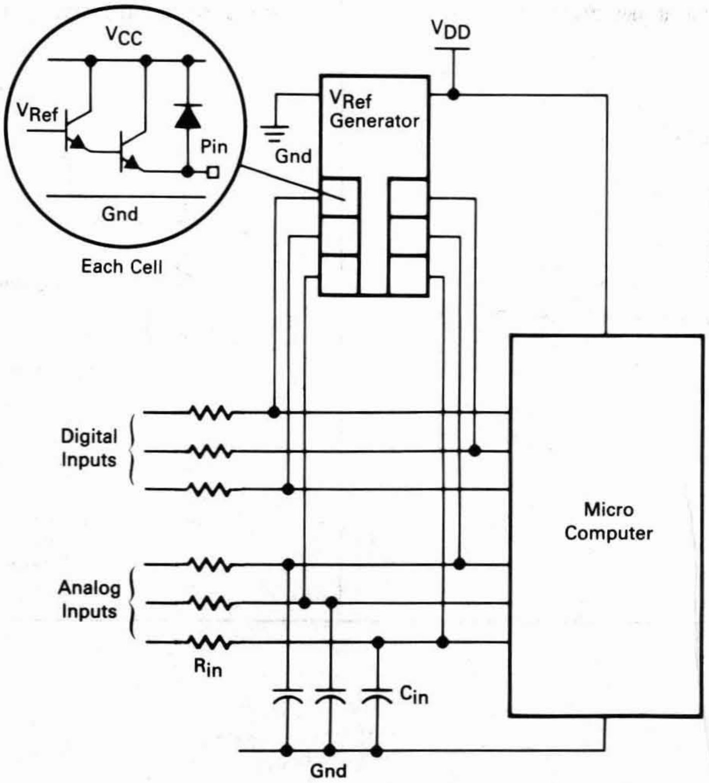

Gnd 1
Clamp 2
Clamp 3
Clamp 4
8 VCC
7 Clamp
6 Clamp
5 Clamp

**FIGURE 1 — BLOCK DIAGRAM AND TYPICAL APPLICATION**


VCC
VRef
Pin
Gnd
Each Cell
VDD
VRef Generator
Gnd
Digital Inputs
Analog Inputs
Rin
Cin
Micro Computer
Gnd

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted, Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 6.0 | V |
| Supply Current | $I_i$ | 300 | mA |
| Clamping Current | $I_{IK}$ | ±50 | mA |
| Junction Temperature | $T_J$ | 125 | °C |
| Power Dissipation ($T_A$ = +85°C) | $P_D$ | 400 | mW |
| Thermal Resistance (Junction-Ambient) | $\theta_{JA}$ | 100 | °C/W |
| Operating Ambient Temperature Range | $T_A$ | −40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

Note 1: Values beyond which damage may occur.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, $4.5 \leq V_{CC} \leq 5.5$ V; if not otherwise noted.)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Positive Clamping Voltage (Note 2)<br>($I_{IK}$ = 10 mA, −40°C ≤ $T_A$ ≤ +85°C) | $V_{(IK)}$ | — | $V_{CC}$ + 1.0 | V |
| Positive Peak Clamping Current | $I_{IK(P)}$ | — | 20 | mA |
| Negative Peak Clamping Voltage<br>($I_{IK}$ = −10 mA, −40°C ≤ $T_A$ ≤ +85°C) | $V_{(IK)}$ | −0.3 | — | V |
| Negative Peak Clamping Current | $I_{IK(P)}$ | −20 | — | mA |
| Output Leakage Current<br>(0 V ≤ $V_{in}$ ≤ $V_{CC}$)<br>(0 V ≤ $V_{in}$ ≤ $V_{CC}$, −40°C ≤ $T_A$ ≤ +85°C) | <br>$I_L$<br>$I_{LT}$ | <br>—<br>— | <br>1.0<br>5.0 | μA |
| Channel Crosstalk ($A_{CT}$ = 20 log $I_L/I_{IK}$) | $A_{CT}$ | 100 | — | dB |
| Quiescent Current (Package) | $I_B$ | — | 2.0 | mA |

Note 2: The device might not give 100% protection in CMOS applications.

## CIRCUIT DESCRIPTION

To ensure the reliable operation of any integrated circuit based electronics system, care has to be taken that voltage transients do not reach the device I/O pins. Most NMOS, HMOS and Bipolar integrated circuits are particularly sensitive to negative voltage peaks which can provoke latch-up or otherwise disturb the normal functioning of the circuit, and in extreme cases may destroy the device.

Generally the maximum rating for a negative voltage transients on integral circuits is −0.3 V over the whole temperature range. Classical protection units have consisted of diode/resistor networks as shown in Figures 2a and 2b.

The arrangement in Figure 2a does not, in general, meet the specification and is therefore inadequate.

The problem with the solution shown in Figure 2b lies mainly with the high current drain through the biassing devices $R_1$ and $D_3$. A second problem exists if the input line carries an analog signal. When $V_{in}$ is close to the ground potential, currents arising from leakage and mismatch between $D_3$ and $D_2$ can be sourced into the input line, thus disturbing the reading.

FIGURE 2 — CLASSICAL PROTECTION CIRCUITS

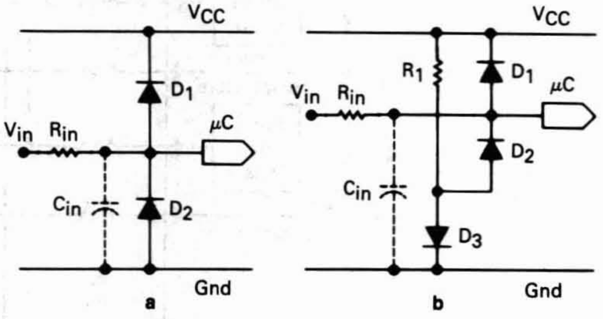
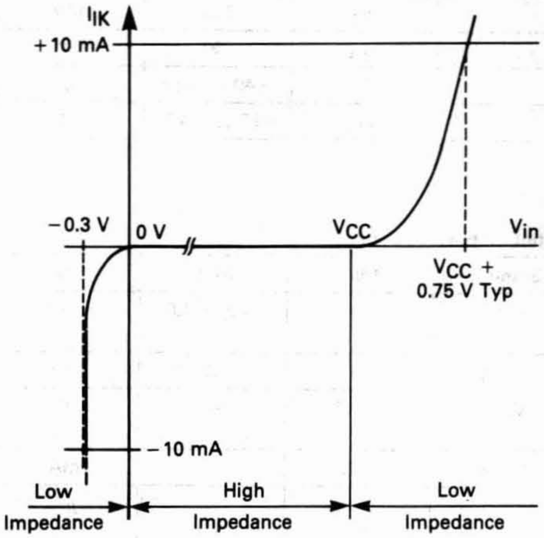


Figure 3 shows the clamping characteristics which are common to each of the six cells in the Peripheral Clamping Array.

As with the classical protection circuits, positive voltage transients are clamped by means of a fast diode to the $V_{CC}$ supply line.

FIGURE 3 — CLAMPING CHARACTERISTICS



## APPLICATIONS INFORMATION

Figure 4 depicts a typical application in a microcomputer based automotive ignition system.

The TCF6000 is being used not only to protect the system's normal inputs but also the (bidirectional) serial diagnostics port.

The value of the input resistors, $R_{in}$, is determined by the clamping current and the anticipated value of the spikes.

Thus:

$$R_{in} = \frac{V}{I_{IK}} \text{ Ohms}$$

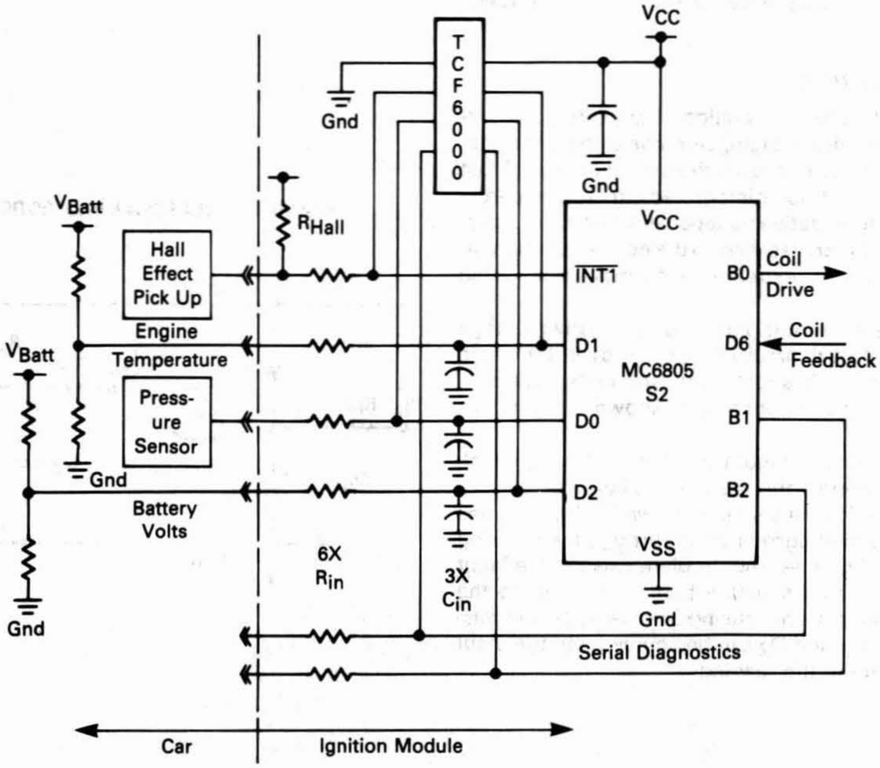
where $V$ = Peak volts (Volts)
$I_{IK}$ = Clamping current (Amps)

So, taking
$V$ = 300 V typically (SAE J1211)
$I_{IK}$ = 10 mA (recommended)

gives
$R_{in}$ = 30 k

Resistors of this value will not usually cause any problems in MOS systems, but their presence needs to be taken into account by the designer. Their effect will normally need to be compensated for in Bipolar systems.

FIGURE 4 — TYPICAL AUTOMOTIVE APPLICATION



$V_{CC}$
TCF6000
Gnd
Gnd
$V_{Batt}$
$R_{Hall}$
Hall Effect Pick Up
Engine Temperature
$V_{Batt}$
Press-ure Sensor
Gnd
Battery Volts
Gnd
6X $R_{in}$
3X $C_{in}$
$V_{CC}$
$\overline{INT1}$
D1
D0
D2
B0
D6
B1
B2
MC6805 S2
$V_{SS}$
Gnd
Coil Drive
Coil Feedback
Serial Diagnostics
Car
Ignition Module

The use of $C_{in}$ is not mandatory, and is not recommended where the lines to be protected are used for output or for both input and output. For digital input lines, the use of a small capacitor in the range of 50 to 220 pF is recommended as this will reduce the rate of rise of voltage seen by the TCF6000 and hence the possibility of overshoot.

In the case of the analog inputs, such as that from the pressure sensor, the capacitor $C_{in}$ is necessary for devices, such as the MC6805S2 shown, which present a low impedance during the sampling period. The maximum value for $C_{in}$ is determined by the accuracy required, the time taken to sample the input and the input impedance during that time, while the maximum value is determined by the required frequency response and the value of $R_{in}$.

Thus for a resistive input A/D connector where:

$T_S$ = Sample time (Seconds)
$R_D$ = Device input resistance (Ohms)
$V_{in}$ = Input voltage (Volts)
k = Required accuracy (%)
$Q_1$ = Charge on capacitor before sampling
$Q_2$ = Charge on capacitor after sampling
$I_D$ = Device input current (Amps)

Thus:

$$Q_1 - Q_2 = \frac{k.Q_1}{100}$$

but $Q_1 = C_{in}\,V_{in}$

and $Q_1 - Q_2 = I_D.T_S$

so that $I_D\,T_S = \dfrac{k.C_{in} \cdot V_{in}}{100}$

and $C_{in}\,(\text{min}) = \dfrac{I_D.T_S}{V_{in}.k}$ Farad

so $C_{in}\,(\text{min}) = \dfrac{100.T_S}{k.R_D}$ Farad

The calculation for a sample and hold type converter is even simpler:

k = Required accuracy (%)
$C_H$ = Hold capacitor (Farad)

$$C_{in}\,(\text{min}) = \frac{100.C_H}{k}\ \text{Farad}$$

For the MC6805S2 this comes out at:

$$C_{in}\,(\text{min}) = \frac{100.25\ \text{pF}}{0.25} = 10\ \text{nF for 1/4\% accuracy}$$

MOTOROLA

# MC8T95/MC6885
# MC8T96/MC6886
# MC8T97/MC6887
# MC8T98/MC6888

## HEX THREE-STATE BUFFER INVERTERS

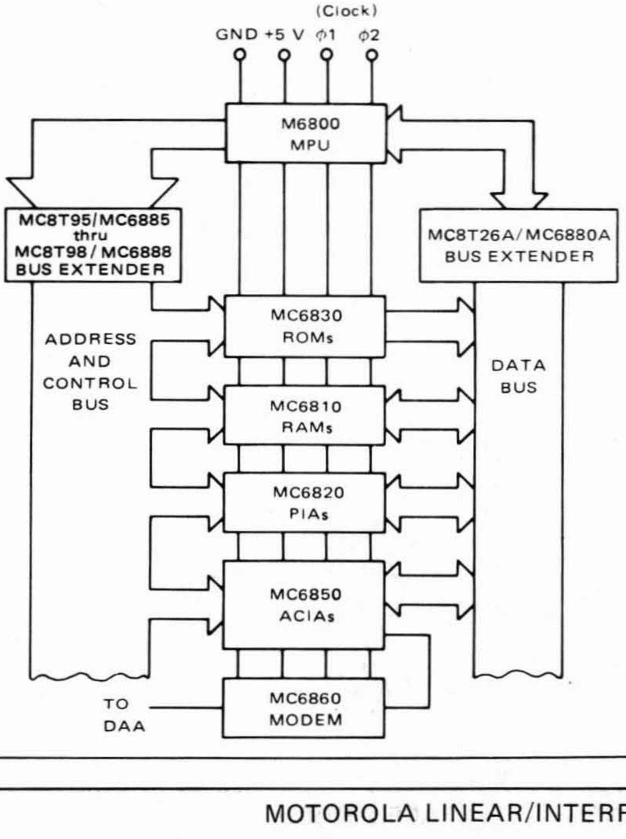
This series of devices combines three features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows high-speed operation.

The devices differ in that the non-inverting MC8T95/MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the non-inverting MC8T97/MC6887 and inverting MC8T98/MC6888 provide two Enable inputs – one controlling four buffers and the other controlling the remaining two buffers.

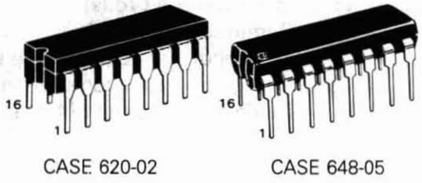
The units are well-suited for Address buffers on the M6800 or similar microprocessor application.

- High Speed – 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74LS Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

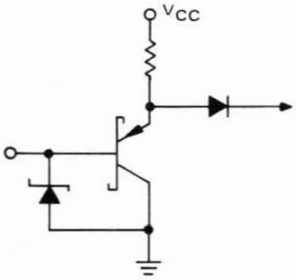
### MICROPROCESSOR BUS EXTENDER APPLICATION


(Clock)
GND +5 V φ1 φ2
M6800 MPU
MC8T95/MC6885 thru MC8T98/MC6888 BUS EXTENDER
MC8T26A/MC6880A BUS EXTENDER
MC6830 ROMs
ADDRESS AND CONTROL BUS
DATA BUS
MC6810 RAMs
MC6820 PIAs
MC6850 ACIAs
TO DAA
MC6860 MODEM

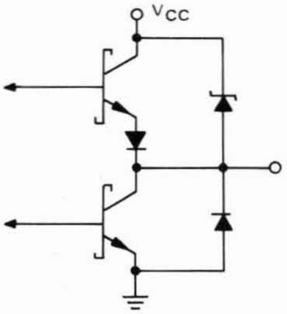
## HEX THREE-STATE BUFFER/INVERTERS


16
1
16
1
CASE 620-02
CASE 648-05

### INPUT EQUIVALENT CIRCUIT



### OUTPUT EQUIVALENT CIRCUIT



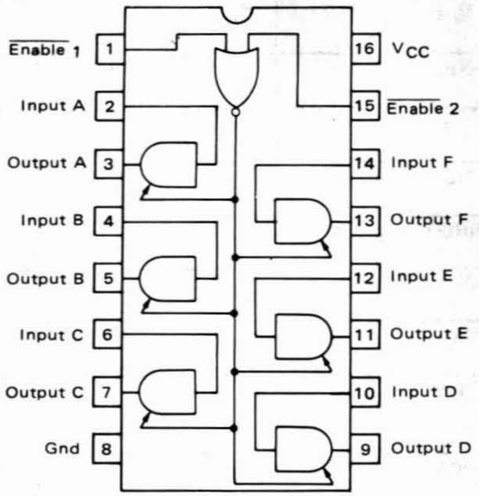
### ORDERING INFORMATION

(Temperature Range for the following devices = 0 to +75°C)

| DEVICE | ALTERNATE | PACKAGE |
|---|---|---|
| MC8T95L | MC6885L | Ceramic DIP |
| MC8T96L | MC6886L | Ceramic DIP |
| MC8T97L | MC6887L | Ceramic DIP |
| MC8T98L | MC6888L | Ceramic DIP |
| MC8T95P | MC6885P | Plastic DIP |
| MC8T96P | MC6886P | Plastic DIP |
| MC8T97P | MC6887P | Plastic DIP |
| MC8T98P | MC6888P | Plastic DIP |

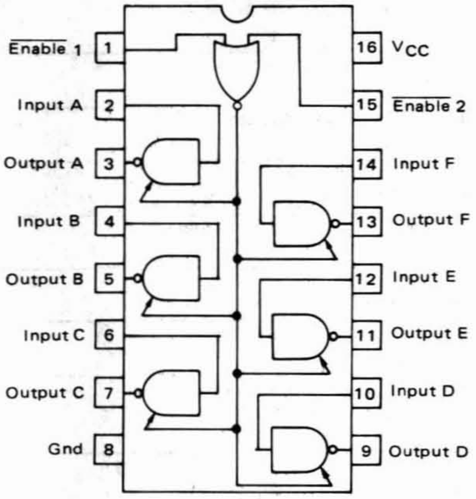
## PIN CONNECTIONS AND TRUTH TABLES

**MC8T95/MC6885**


$\overline{\text{Enable}}$ 1
1
Input A
2
Output A
3
Input B
4
Output B
5
Input C
6
Output C
7
Gnd
8
16
$V_{CC}$
15
$\overline{\text{Enable}}$ 2
14
Input F
13
Output F
12
Input E
11
Output E
10
Input D
9
Output D

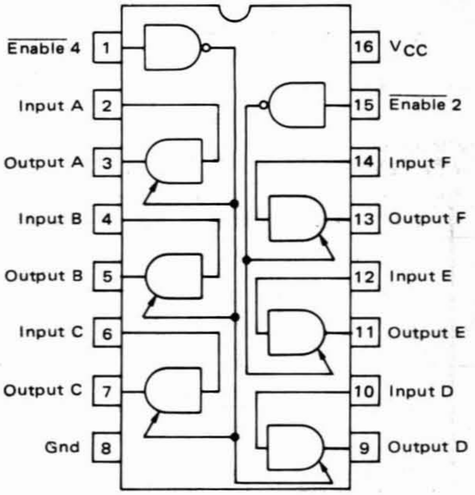
| $\overline{\text{Enable}}$ 2 | $\overline{\text{Enable}}$ 1 | Input | Output |
|---|---|---|---|
| L | L | L | L |
| L | L | H | H |
| L | H | X | Z |
| H | L | X | Z |
| H | H | X | Z |

**MC8T96/MC6886**


$\overline{\text{Enable}}$ 1
1
Input A
2
Output A
3
Input B
4
Output B
5
Input C
6
Output C
7
Gnd
8
16
$V_{CC}$
15
$\overline{\text{Enable}}$ 2
14
Input F
13
Output F
12
Input E
11
Output E
10
Input D
9
Output D

| $\overline{\text{Enable}}$ 2 | $\overline{\text{Enable}}$ 1 | Input | Output |
|---|---|---|---|
| L | L | L | H |
| L | L | H | L |
| L | H | X | Z |
| H | L | X | Z |
| H | H | X | Z |

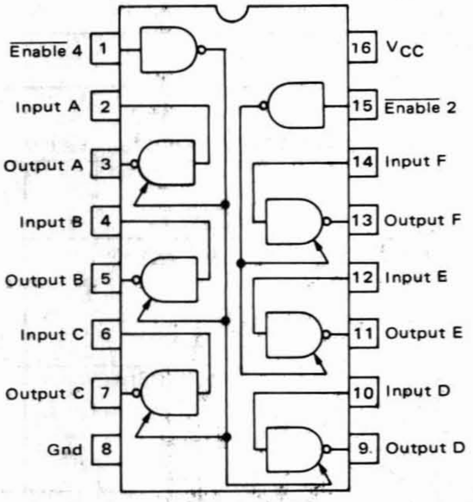
**MC8T97/MC6887**


$\overline{\text{Enable}}$ 4
1
Input A
2
Output A
3
Input B
4
Output B
5
Input C
6
Output C
7
Gnd
8
16
$V_{CC}$
15
$\overline{\text{Enable}}$ 2
14
Input F
13
Output F
12
Input E
11
Output E
10
Input D
9
Output D

| $\overline{\text{Enable}}$ | Input | Output |
|---|---|---|
| L | L | L |
| L | H | H |
| H | X | Z |

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
X = Irrelevant

**MC8T98/MC6888**


$\overline{\text{Enable}}$ 4
1
Input A
2
Output A
3
Input B
4
Output B
5
Input C
6
Output C
7
Gnd
8
16
$V_{CC}$
15
$\overline{\text{Enable}}$ 2
14
Input F
13
Output F
12
Input E
11
Output E
10
Input D
9
Output D

| $\overline{\text{Enable}}$ | Input | Output |
|---|---|---|
| L | L | H |
| L | H | L |
| H | X | Z |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 8.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Operating Ambient Temperature Range | $T_A$ | 0 to +75 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | | °C |
| Plastic Package | | 150 | |
| Ceramic Package | | 175 | |

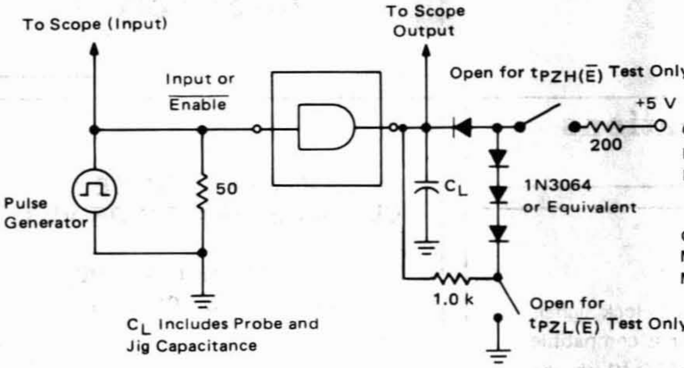
## ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 0°C $\leqslant T_A \leqslant$ 75°C and 4.75 V $\leqslant V_{CC} \leqslant$ 5.25 V)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage – High Logic State ($V_{CC}$ = 4.75 V, $T_A$ = 25°C) | $V_{IH}$ | 2.0 | – | – | V |
| Input Voltage – Low Logic State ($V_{CC}$ = 4.75 V, $T_A$ = 25°C) | $V_{IL}$ | – | – | 0.8 | V |
| Input Current – High Logic State ($V_{CC}$ = 5.25 V, $V_{IH}$ = 2.4 V) | $I_{IH}$ | – | – | 40 | µA |
| Input Current – Low Logic State ($V_{CC}$ = 5.25 V, $V_{IL}$ = 0.5 V, $V_{IL(\overline{E})}$ = 0.5 V) | $I_{IL}$ | – | – | -400 | µA |
| Input Current – High Impedance State ($V_{CC}$ = 5.25 V, $V_{IL(I)}$ = 0.5 V, $V_{IH(\overline{E})}$= 2.0 V) | $I_{IH(\overline{E})}$ | – | – | -40 | µA |
| Output Voltage – High Logic State ($V_{CC}$ = 4.75 V, $I_{OH}$ = -5.2 mA) | $V_{OH}$ | 2.4 | – | – | V |
| Output Voltage – Low Logic State ($I_{OL}$ = 48 mA) | $V_{OL}$ | – | – | 0.5 | V |
| Output Current – High Impedance State | $I_{OZ}$ | | | | µA |
| ($V_{CC}$ = 5.25 V, $V_{OH}$ = 2.4 V) | | – | – | 40 | |
| ($V_{CC}$ = 5.25 V, $V_{OL}$ = 0.5 V) | | – | – | -40 | |
| Output Short-Circuit Current ($V_{CC}$ = 5.25 V, $V_O$ = 0) (only one output can be shorted at a time) | $I_{OS}$ | -40 | -80 | -115 | mA |
| Power Supply Current ($V_{CC}$ = 5.25 V) | $I_{CC}$ | | | | mA |
| MC8T95, MC8T97, MC6885, MC6887 | | – | 65 | 98 | |
| MC8T96, MC8T98, MC6886, MC6888 | | – | 59 | 89 | |
| Input Clamp Voltage ($V_{CC}$ = 4.75 V, $I_{IC}$ = -12 mA) | $V_{IC}$ | – | – | -1.5 | V |
| Output $V_{CC}$ Clamp Voltage ($V_{CC}$ = 0, $I_{OC}$ = 12 mA) | $V_{OC}$ | – | – | 1.5 | V |
| Output Gnd Clamp Voltage ($V_{CC}$ = 0, $I_{OC}$ = -12 mA) | $V_{OC}$ | – | – | -1.5 | V |
| Input Voltage ($I_I$ = 1.0 mA) | $V_I$ | 5.5 | – | – | V |

## SWITCHING CHARACTERISTICS ($V_{CC}$ = 5.0 V, $T_A$ = 25°C unless otherwise noted.)

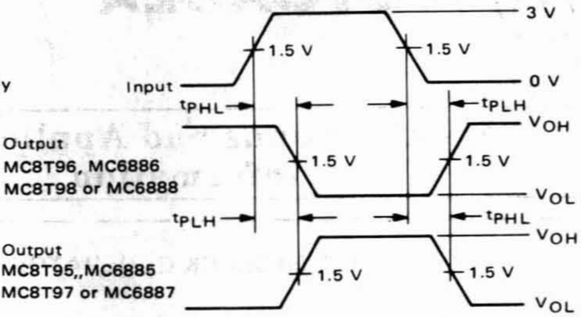
| Characteristic | Symbol | MC8T95/97<br>MC6885/87 | | | MC8T96/98<br>MC6886/88 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Propagation Delay Time – High to Low State | $t_{PHL}$ | | | | | | | ns |
| ($C_L$ = 50 pF) | | 3.0 | – | 12 | 4.0 | – | 11 | |
| ($C_L$ = 250 pF) | | – | 16 | – | – | 15 | – | |
| ($C_L$ = 375 pF) | | – | 20 | – | – | 18 | – | |
| ($C_L$ = 500 pF) | | – | 23 | – | – | 22 | – | |
| Propagation Delay Time – Low to High State | $t_{PLH}$ | | | | | | | ns |
| ($C_L$ = 50 pF) | | 3.0 | – | 13 | 3.0 | – | 10 | |
| ($C_L$ = 250 pF) | | – | 25 | – | – | 22 | – | |
| ($C_L$ = 375 pF) | | – | 33 | – | – | 28 | – | |
| ($C_L$ = 500 pF) | | – | 42 | – | – | 35 | – | |
| Transition Time – High to Low State | $t_{THL}$ | | | | | | | ns |
| ($C_L$ = 250 pF) | | – | 10 | – | – | 10 | – | |
| ($C_L$ = 375 pF) | | – | 11 | – | – | 13 | – | |
| ($C_L$ = 500 pF) | | – | 14 | – | – | 15 | – | |
| Transition Time – Low to High State | $t_{TLH}$ | | | | | | | ns |
| ($C_L$ = 250 pF) | | – | 32 | – | – | 28 | – | |
| ($C_L$ = 375 pF) | | – | 42 | – | – | 38 | – | |
| ($C_L$ = 500 pF) | | – | 60 | – | – | 53 | – | |
| Propagation Delay Time – High State to Third State ($C_L$ = 5.0 pF) | $t_{PHZ(\overline{E})}$ | – | – | 10 | – | – | 10 | ns |
| Propagation Delay Time – Low State to Third State ($C_L$ = 5.0 pF) | $t_{PLZ(\overline{E})}$ | – | – | 12 | – | – | 16 | ns |
| Propagation Delay Time – Third State to High State ($C_L$ = 50 pF) | $t_{PZH(\overline{E})}$ | – | – | 25 | – | – | 22 | ns |
| Propagation Delay Time – Third State to Low State ($C_L$ = 50 pF) | $t_{PZL(\overline{E})}$ | – | – | 25 | – | – | 24 | ns |

FIGURE 1 – TEST CIRCUIT FOR SWITCHING CHARACTERISTICS


To Scope (Input)
To Scope Output
Input or Enable
Open for tPZH(E) Test Only
+5 V
200
Pulse Generator
50
CL
1N3064 or Equivalent
1.0 k
Open for tPZL(E) Test Only

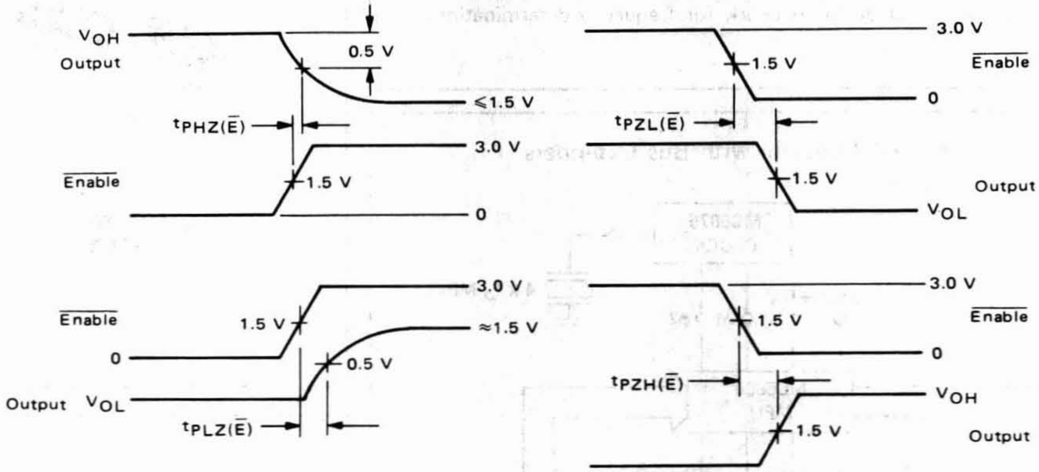
CL Includes Probe and Jig Capacitance

FIGURE 2 – WAVEFORMS FOR PROPAGATION DELAY TIMES INPUT TO OUTPUT


3 V
1.5 V
1.5 V
Input
0 V
tPHL
tPLH
VOH
Output MC8T96, MC6886 MC8T98 or MC6888
1.5 V
1.5 V
VOL
tPLH
tPHL
VOH
Output MC8T95, MC6885 MC8T97 or MC6887
1.5 V
1.5 V
VOL

Input Pulse Conditions
$t_{THL} = t_{TLH} \leq 10$ ns
f = 1.0 MHz

FIGURE 3 – WAVEFORMS FOR PROPAGATION DELAY TIMES – $\overline{\text{ENABLE}}$ TO OUTPUT


VOH
Output
0.5 V
≤1.5 V
tPHZ(E)
3.0 V
Enable
1.5 V
0
3.0 V
Enable
1.5 V
0
tPZL(E)
1.5 V
Output
VOL
Enable
1.5 V
3.0 V
≈1.5 V
0
0.5 V
Output VOL
tPLZ(E)
3.0 V
Enable
1.5 V
0
tPZH(E)
VOH
1.5 V
Output

H = High-Logic State, L = Low-Logic State, Z = High Impedance State

**MOTOROLA**

# MC6875
# MC6875A

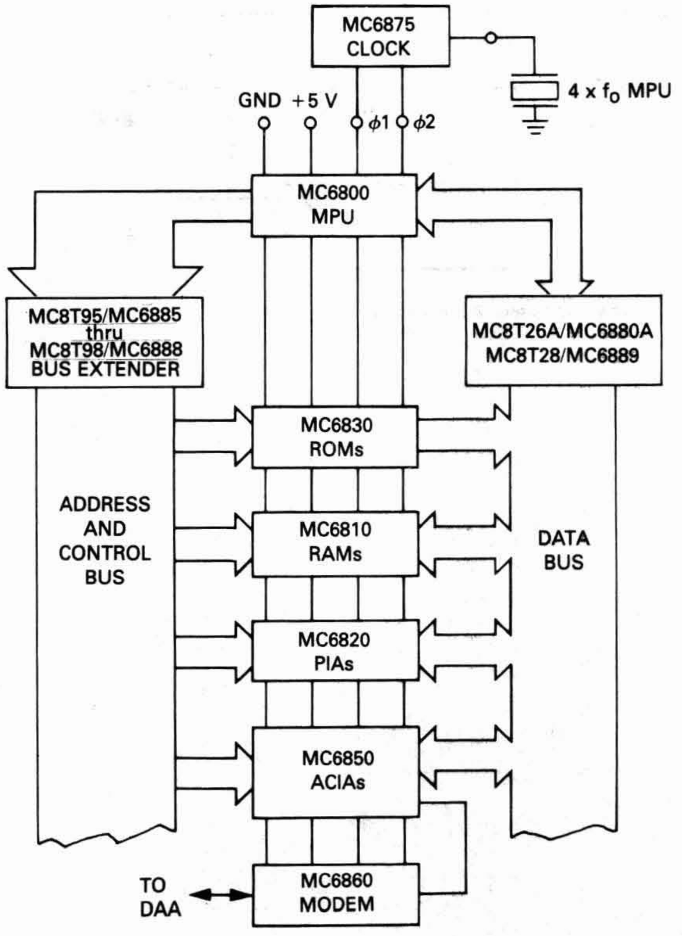
## Specifications and Applications Information

## M6800 CLOCK GENERATOR

Intended to supply the non-overlapping $\phi 1$ and $\phi 2$ clock signals required by the microprocessor, this clock generator is compatible with 1.0, 1.5, and 2.0 MHz versions of the MC6800. Both the oscillator and high capacitance driver elements are included along with numerous other logic accessory functions for easy system expansion.

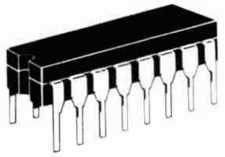
Schottky technology is employed for high speed and PNP-buffered inputs are employed for NMOS compatibility. A single +5 V power supply, and a crystal or RC network for frequency determination are required.

### Typical MPU System with Bus Extenders


MC6875
CLOCK
4 x $f_0$ MPU
GND
+5 V
$\phi 1$
$\phi 2$
MC6800
MPU
MC8T95/MC6885
thru
MC8T98/MC6888
BUS EXTENDER
MC8T26A/MC6880A
MC8T28/MC6889
MC6830
ROMs
MC6810
RAMs
MC6820
PIAs
MC6850
ACIAs
MC6860
MODEM
ADDRESS
AND
CONTROL
BUS
DATA
BUS
TO
DAA

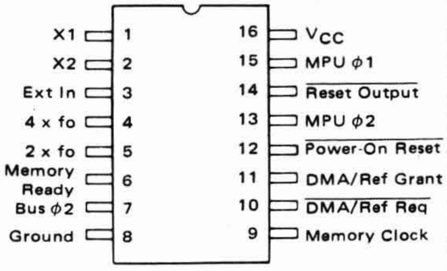
## M6800 TWO-PHASE CLOCK GENERATOR/DRIVER

SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT



**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

### PIN CONNECTIONS


X1 1
X2 2
Ext In 3
4 x fo 4
2 x fo 5
Memory Ready 6
Bus $\phi 2$ 7
Ground 8
16 $V_{CC}$
15 MPU $\phi 1$
14 $\overline{\text{Reset Output}}$
13 MPU $\phi 2$
12 $\overline{\text{Power-On Reset}}$
11 DMA/Ref Grant
10 $\overline{\text{DMA/Ref Req}}$
9 Memory Clock

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC6875L | 0 to +70°C | Ceramic |
| MC6875AL | -55 to +125°C | DIP |

## ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted $T_A = 25^{\circ}C$.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +7.0 | Vdc |
| Input Voltage | $V_I$ | +5.5 | Vdc |
| Operating Ambient Temperature Range<br>MC6875L<br>MC6875AL | $T_A$ | <br>0 to +70<br>-55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | 175 | °C |

NOTE:
Operation of the MC6875AL over the full military temperature range (to maximum $T_A$) will result in excessive operating junction temperature.

The use of a clip on 16 pin heat sink similar to AAVID Engineering, Inc., Model 5007 ($R_{\theta CA} = 18^{\circ}C/W$) is recommended above $T_A \approx 95^{\circ}C$.

Contact AAVID Engineering, Inc.
30 Cook Court
Laconia, New Hampshire 03246
Tel. (603) 524-4443

## RECOMMENDED OPERATING CONDITIONS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +4.75 to +5.25 | Vdc |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |

## ELECTRICAL CHARACTERISTICS

(Unless otherwise noted specifications apply over recommended power supply and temperature ranges. Typical values measured at $V_{CC} = 5.0$ V and $T_A = 25^{\circ}C$.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage — High Logic State | | | | | |
| MPU $\phi 1$ and $\phi 2$ Outputs | | | | | V |
| ($V_{CC} = 4.75$ V, $I_{OHM} = -200\ \mu A$) | $V_{OHM}$ | $V_{CC} - 0.6$ | – | – | |
| ($V_{CC} = 5.25$ V, $I_{OHMK} = +5.0$ mA) | $V_{OHMK}$ | – | – | $V_{CC} + 1.0$ | |
| Bus $\phi 2$ Output | | | | | V |
| ($V_{CC} = 4.75$ V, $I_{OHB} = -10$ mA) | $V_{OHB}$ | 2.4 | – | – | |
| ($V_{CC} = 5.25$ V, $I_{OHBK} = +5.0$ mA) | $V_{OHBK}$ | – | – | $V_{CC} + 1.0$ | |
| 4 x fo Output<br>($V_{CC} = 4.75$ V, $V_{IH} = 2.0$ V, $I_{OH4X} = -500\ \mu A$) | $V_{OH4X}$ | 2.4 | – | – | V |
| 2 x fo, DMA/Refresh Grant and Memory Clock Outputs<br>($V_{CC} = 4.75$ V, $I_{OH} = -500\ \mu A$) | $V_{OH}$ | 2.4 | – | – | V |
| $\overline{\text{Reset}}$ Output<br>($V_{CC} = 4.75$ V, $V_{IH} = 3.3$ V, $I_{OH\overline{R}} = -100\ \mu A$) | $V_{OH\overline{R}}$ | 2.4 | – | – | V |
| Output Voltage — Low Logic State | | | | | |
| MPU $\phi 1$ and $\phi 2$ Outputs | | | | | V |
| ($V_{CC} = 4.75$ V, $I_{OLM} = +200\ \mu A$) | $V_{OLM}$ | – | – | 0.4 | |
| ($V_{CC} = 4.75$ V, $I_{OLMK} = -5.0$ mA) | $V_{OLMK}$ | – | – | -1.0 | |
| Bus $\phi 2$ Output | | | | | V |
| ($V_{CC} = 4.75$ V, $I_{OLB} = +48$ mA) | $V_{OLB}$ | – | – | 0.5 | |
| ($V_{CC} = 4.75$ V, $I_{OLBK} = -5.0$ mA) | $V_{OLBK}$ | – | – | -1.0 | |
| 4 x fo Output<br>($V_{CC} = 4.75$ V, $V_{IL} = 0.8$ V, $I_{OL4X} = 16$ mA) | $V_{OL4X}$ | – | – | 0.5 | V |
| 2 x fo, DMA/Refresh Grant and Memory Clock Outputs<br>($V_{CC} = 4.75$ V, $I_{OL} = 16$ mA) | $V_{OL}$ | – | – | 0.5 | V |
| $\overline{\text{Reset}}$ Output<br>($V_{CC} = 4.75$ V, $V_{IL} = 0.8$ V, $I_{OL\overline{R}} = 3.2$ mA) | $V_{OL\overline{R}}$ | – | – | 0.5 | V |
| Input Voltage — High Logic State<br>Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs | $V_{IH}$ | 2.0 | – | – | V |
| Input Voltage — Low Logic State<br>Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs | $V_{IL}$ | – | – | 0.8 | V |
| Input Thresholds — $\overline{\text{Power-On Reset}}$ Input (See Figure 2) | | | | | V |
| Output Low to High | $V_{ILH}$ | – | 2.8 | 3.6 | |
| Output High to Low | $V_{IHL}$ | 0.8 | 1.4 | – | |
| Input Clamp Voltage MC6875L | $V_{IK}$ | – | – | -1.0 | V |
| ($V_{CC} = 4.75$ V, $I_{IC} = -5.0$ mA) MC6875AL | | – | – | -1.5 | |
| Input Current — High Logic State | | | | | |
| Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs<br>($V_{CC} = 4.75$ V, $V_{IH} = 5.0$ V) | $I_{IH}$ | – | – | 25 | μA |
| $\overline{\text{Power-On Reset}}$<br>($V_{CC} = 5.0$ V, $V_{IH\overline{R}} = 5.0$ V) | $I_{IH\overline{R}}$ | – | – | 50 | μA |
| Input Current — Low Logic State | | | | | |
| Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs<br>($V_{CC} = 5.25$ V, $V_{IL} = 0.5$ V) | $I_{IL}$ | – | – | -250 | μA |
| $\overline{\text{Power-On Reset}}$ Input<br>($V_{CC} = 5.25$ V, $V_{IL} = 0.5$ V) | $I_{IL\overline{R}}$ | – | – | -250 | μA |

## OPERATING DYNAMIC POWER SUPPLY CURRENT

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Currents<br>($V_{CC}$ = 5.25 V, $f_{osc}$ = 8.0 MHz, $V_{IL}$ = 0 V, $V_{IH}$ = 3.0 V)<br>Normal Operation<br>(Memory Ready and DMA/Refresh Request Inputs at High Logic State) | $I_{CCN}$ | – | – | 150 | mA |
| Memory Ready Stretch Operation<br>(Memory Ready Input at Low Logic State; DMA/Refresh Request Input at High Logic State) | $I_{CCMR}$ | – | – | 135 | mA |
| DMA/Refresh Request Stretch Operation<br>(Memory Ready Input at High Logic State; DMA/Refresh Request Input at Low Logic State) | $I_{CCDR}$ | – | – | 135 | mA |

## SWITCHING CHARACTERISTICS

(These specifications apply whether the Internal Oscillator (see Figure 9) or an External Oscillator is used (see Figure 10).
Typical values measured at $V_{CC}$ = 5.0 V, $T_A$ = 25°C, fo = 1.0 MHz (see Figure 8).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **MPU φ1 AND φ2 CHARACTERISTICS** | | | | | |
| Output Period (Figure 3) | $t_o$ | 500 | | – | ns |
| Pulse Width (Figure 3) | $t_{PWM}$ | | | | ns |
| (fo = 1.0 MHz) | | 400 | – | – | |
| (fo = 1.5 MHz) | | 230 | – | – | |
| (fo = 2.0 MHz) | | 180 | – | – | |
| Total Up Time (Figure 3) | $t_{UPM}$ | | | | ns |
| (fo = 1.0 MHz) | | 900 | – | – | |
| (fo = 1.5 MHz) | | 600 | – | – | |
| (fo = 2.0 MHz) | | 440 | – | – | |
| Delay Time Referenced to Output Complement (Figure 3)<br>Output High to Low State (Clock Overlap at 1.0 V) | $t_{PLHM}$ | 0 | – | – | ns |
| Delay Times Referenced to 2 x fo (Figure 4 MPU φ2 only) | | | | | |
| Output Low to High Logic State | $t_{PLHM2X}$ | – | – | 85 | ns |
| Output High to Low Logic State | $t_{PHLM2X}$ | – | – | 70 | ns |
| Transition Times (Figure 3) | | | | | |
| Output Low to High Logic State | $t_{TLHM}$ | – | – | 25 | ns |
| Output High to Low Logic State | $t_{THLM}$ | – | – | 25 | ns |
| **BUS φ2 CHARACTERISTICS** | | | | | |
| Pulse Width – Low Logic State (Figure 4) | $t_{PWLB}$ | | | | ns |
| (fo = 1.0 MHz) | | 430 | – | – | |
| (fo = 1.5 MHz) | | 280 | – | – | |
| (fo = 2.0 MHz) | | 210 | – | – | |
| Pulse Width – High Logic State | $t_{PWHB}$ | | | | ns |
| (fo = 1.0 MHz) | | 450 | – | – | |
| (fo = 1.5 MHz) | | 295 | – | – | |
| (fo = 2.0 MHz) | | 235 | – | – | |
| Delay Times – (Referenced to MPU φ1) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLHBM1}$ | | | | ns |
| (fo = 1.0 MHz) | | 480 | – | – | |
| (fo = 1.5 MHz) | | 320 | – | – | |
| (fo = 2.0 MHz) | | 240 | – | – | |
| Output High to Low Logic State | $t_{PHLBM1}$ | | | | |
| ($C_L$ = 300 pF) | | – | – | 25 | |
| ($C_L$ = 100 pF) | | – | – | 20 | |
| Delay Times (Referenced to MPU φ2) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLHBM2}$ | –30 | – | +25 | ns |
| Output High to Low Logic State | $t_{PHLBM2}$ | 0 | – | +40 | ns |
| Transition Times (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{TLHB}$ | – | – | 20 | ns |
| Output High to Low Logic State | $t_{THLB}$ | – | – | 20 | ns |

## SWITCHING CHARACTERISTICS (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **MEMORY CLOCK CHARACTERISTICS** | | | | | |
| Delay Times (Referenced to MPU $\phi 2$) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLHCM}$ | -50 | – | +25 | ns |
| Output High to Low Logic State | $t_{PHLCM}$ | 0 | – | +40 | ns |
| Delay Times (Referenced to 2 x fo) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLHC2X}$ | – | – | 65 | ns |
| Output High to Low Logic State | $t_{PHLC2X}$ | – | – | 85 | ns |
| Transition Times (Figure 4) | | | | | |
| Output Low to High State | $t_{TLHC}$ | – | – | 25 | ns |
| Output High to Low State | $t_{THLC}$ | – | – | 25 | ns |
| **2 x fo CHARACTERISTICS** | | | | | |
| Delay Times (Referenced to 4 x fo) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLH2X}$ | – | – | 50 | ns |
| Output High to Low Logic State | $t_{PHL2X}$ | – | – | 65 | ns |
| Delay Time (Referenced to MPU $\phi 1$) (Figure 4) | | | | | |
| Output High to Low Logic State | $t_{PHL2XM1}$ | | | | ns |
| (fo = 1.0 MHz) | | 365 | – | – | |
| (fo = 1.5 MHz) | | 220 | – | – | |
| Transition Times (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{TLH2X}$ | – | – | 25 | ns |
| Output High to Low Logic State | $t_{THL2X}$ | – | – | 25 | ns |
| **4 x fo CHARACTERISTICS** | | | | | |
| Delay Times (Referenced to Ext. In) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLH4X}$ | – | – | 50 | ns |
| Output High to Low Logic State | $t_{PHL4X}$ | – | – | 30 | ns |
| Transition Time (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{TLH4X}$ | – | – | 25 | ns |
| Output High to Low Logic State | $t_{THL4X}$ | – | – | 25 | ns |
| **MEMORY READY CHARACTERISTICS** | | | | | |
| Set-Up Times (Figure 5) | | | | | |
| Low Input Logic State | $t_{SMRL}$ | 55 | – | – | ns |
| High Input Logic State | $t_{SMRH}$ | 75 | – | – | ns |
| Hold Time (Figure 5) | | | | | |
| Low Input Logic State | $t_{HMRL}$ | 10 | – | – | ns |
| **$\overline{\text{DMA/REFRESH REQUEST}}$ CHARACTERISTICS** | | | | | |
| Set-Up Times (Figure 6) | | | | | |
| Low Input Logic State | $t_{SDRL}$ | 65 | – | – | ns |
| High Input Logic State | $t_{SDRH}$ | 75 | – | – | ns |
| Hold Time (Figure 6) | | | | | |
| Low Input Logic State | $t_{HDRL}$ | 10 | – | – | ns |
| **DMA/REFRESH GRANT CHARACTERISTICS** | | | | | |
| Delay Time Referenced to Memory Clock (Figure 6) | | | | | |
| Output Low to High Logic State | $t_{PLHG}$ | -15 | – | +25 | ns |
| Output High to Low Logic State | $t_{PHLG}$ | -25 | – | +15 | ns |
| Transition Times (Figure 6) | | | | | |
| Output Low to High Logic State | $t_{TLHG}$ | – | – | 25 | ns |
| Output High to Low Logic State | $t_{THLG}$ | – | – | 25 | ns |
| **$\overline{\text{RESET}}$ CHARACTERISTICS** | | | | | |
| Delay Time Referenced to $\overline{\text{Power-On Reset}}$ (Figure 7) | | | | | |
| Output Low to High Logic State | $t_{PLH\overline{R}}$ | – | – | 1000 | ns |
| Output High to Low Logic State | $t_{PHL\overline{R}}$ | – | – | 250 | ns |
| Transition Times (Figure 7) | | | | | |
| Output Low to High Logic State | $t_{TLH\overline{R}}$ | – | – | 100 | ns |
| Output High to Low Logic State | $t_{THL\overline{R}}$ | – | – | 50 | ns |

## DESCRIPTION OF PIN FUNCTIONS

- 4 x fo – A free running oscillator at four times the MPU clock rate useful for a system sync signal.
- 2 x fo – A free running oscillator at two times the MPU clock rate.
- $\overline{\text{DMA/REF REQ}}$ – An asynchronous input used to freeze the MPU clocks in the $\phi 1$ high, $\phi 2$ low state for dynamic memory refresh or cycle steal DMA (Direct Memory Access).
- REF GRANT – A synchronous output used to synchronize the refresh or DMA operation to the MPU.
- MEMORY READY – An asynchronous input used to freeze the MPU clocks in the $\phi 1$ low, $\phi 2$ high state for slow memory interface.
- MPU $\phi 1$ MPU $\phi 2$ – Capable of driving the $\phi 1$ and $\phi 2$ inputs on two MC6800s.
- BUS $\phi 2$ – An output nominally in phase with MPU $\phi 2$ having MC8T26A type drive capability.
- MEMORY CLOCK – An output nominally in phase with MPU $\phi 2$ which free runs during a refresh request cycle.
- $\overline{\text{POWER-ON RESET}}$ – A Schmitt trigger input which controls $\overline{\text{Reset}}$. A capacitor to ground is required to set the desired time constant. Internal 50 k resistor to $V_{CC}$. See General Design Suggestions for Manual Reset Operation.
- $\overline{\text{RESET}}$ – An output to the MPU and I/O devices.
- X1, X2 – Provision to attach a series resonant crystal or RC network.
- EXT IN – Allows driving by an external TTL signal to synchronize the MPU to an external system.

FIGURE 1 – BLOCK DIAGRAM

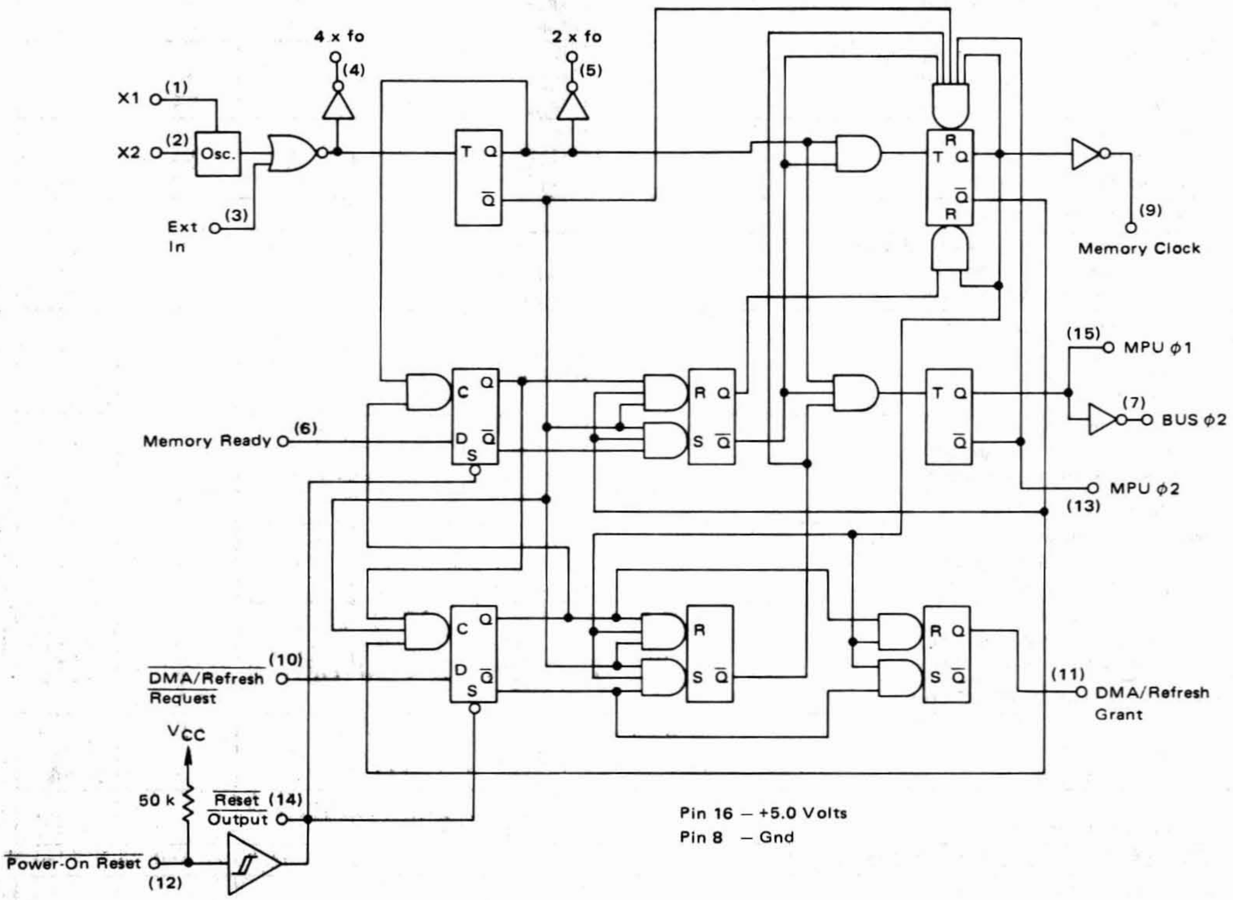

4 x fo
(4)
2 x fo
(5)
X1 (1)
X2 (2)
Osc.
Ext In (3)
T Q
Q̄
R
T Q
Q̄
R
(9)
Memory Clock
(15) MPU φ1
(7) BUS φ2
MPU φ2
(13)
C Q
D Q̄
S
R Q
S Q̄
T Q
Q̄
Memory Ready (6)
DMA/Refresh Request (10)
C Q
D Q̄
S
R
S Q̄
R Q
S Q̄
(11) DMA/Refresh Grant
VCC
50 k
Reset Output (14)
Power-On Reset (12)
Pin 16 – +5.0 Volts
Pin 8 – Gnd

FIGURE 2 – TYPICAL HYSTERESIS CHARACTERISTIC OF $\overline{\text{RESET}}$ FUNCTION

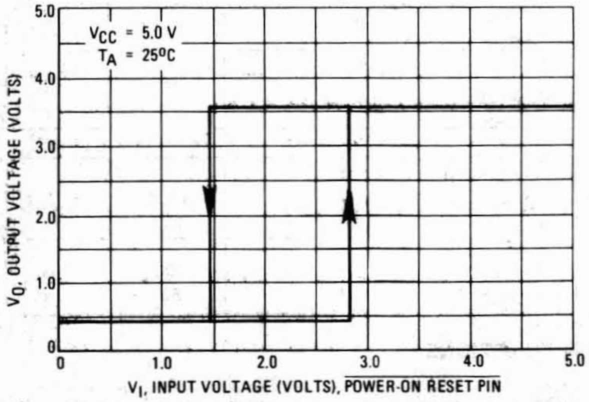
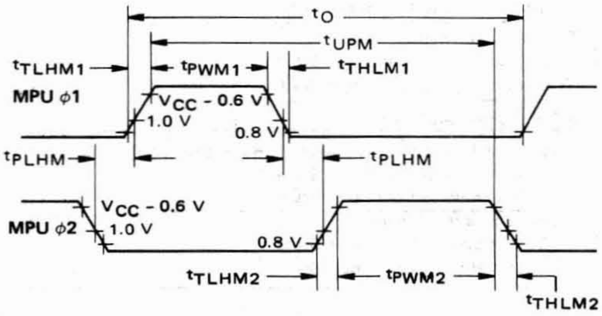


FIGURE 3 – TIMING DIAGRAM FOR MPU φ1 AND φ2


tO
tUPM
tTLHM1
tPWM1
tTHLM1
MPU φ1
VCC - 0.6 V
1.0 V
0.8 V
tPLHM
tPLHM
MPU φ2
VCC - 0.6 V
1.0 V
0.8 V
tTLHM2
tPWM2
tTHLM2

$V_{OV}$ = 1.0 V = Clock Overlap measurement point

**FIGURE 4 – TIMING DIAGRAM FOR NON-STRETCHED OPERATION**
**(Memory Ready and $\overline{\text{DMA/Refresh Request}}$ held high continuously)**
**Ext. In Input Voltage: 0 V to 3.0 V, f = 8.0 MHz, Duty Cycle = 50%, $t_{TLHEX} = t_{THLEX} = 5.0$ ns**

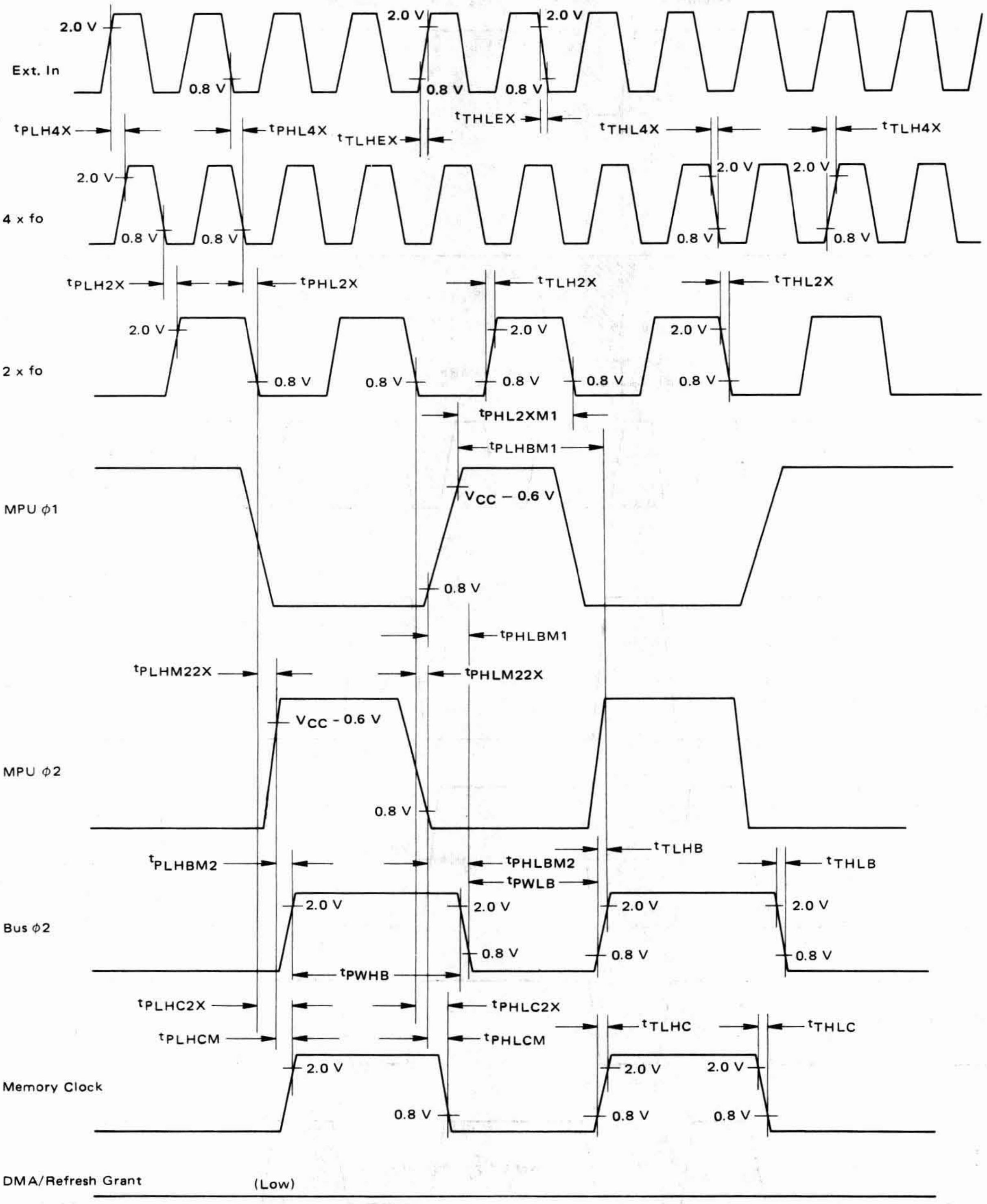

Ext. In
2.0 V
0.8 V
tPLH4X
tPHL4X
tTLHEX
tTHLEX
tTHL4X
tTLH4X
4 x fo
tPLH2X
tPHL2X
tTLH2X
tTHL2X
2 x fo
tPHL2XM1
tPLHBM1
MPU φ1
VCC – 0.6 V
tPHLBM1
tPLHM22X
tPHLM22X
MPU φ2
tPLHBM2
tPHLBM2
tPWLB
tTLHB
tTHLB
Bus φ2
tPWHB
tPLHC2X
tPHLC2X
tPLHCM
tPHLCM
tTLHC
tTHLC
Memory Clock
DMA/Refresh Grant
(Low)

FIGURE 5 – TIMING DIAGRAM FOR MEMORY READY STRETCH OPERATION
(Minimum Stretch Shown)
Input Voltage: 3.0 to 0 V, $t_{THLMR} = t_{TLHMR} = 5.0$ ns

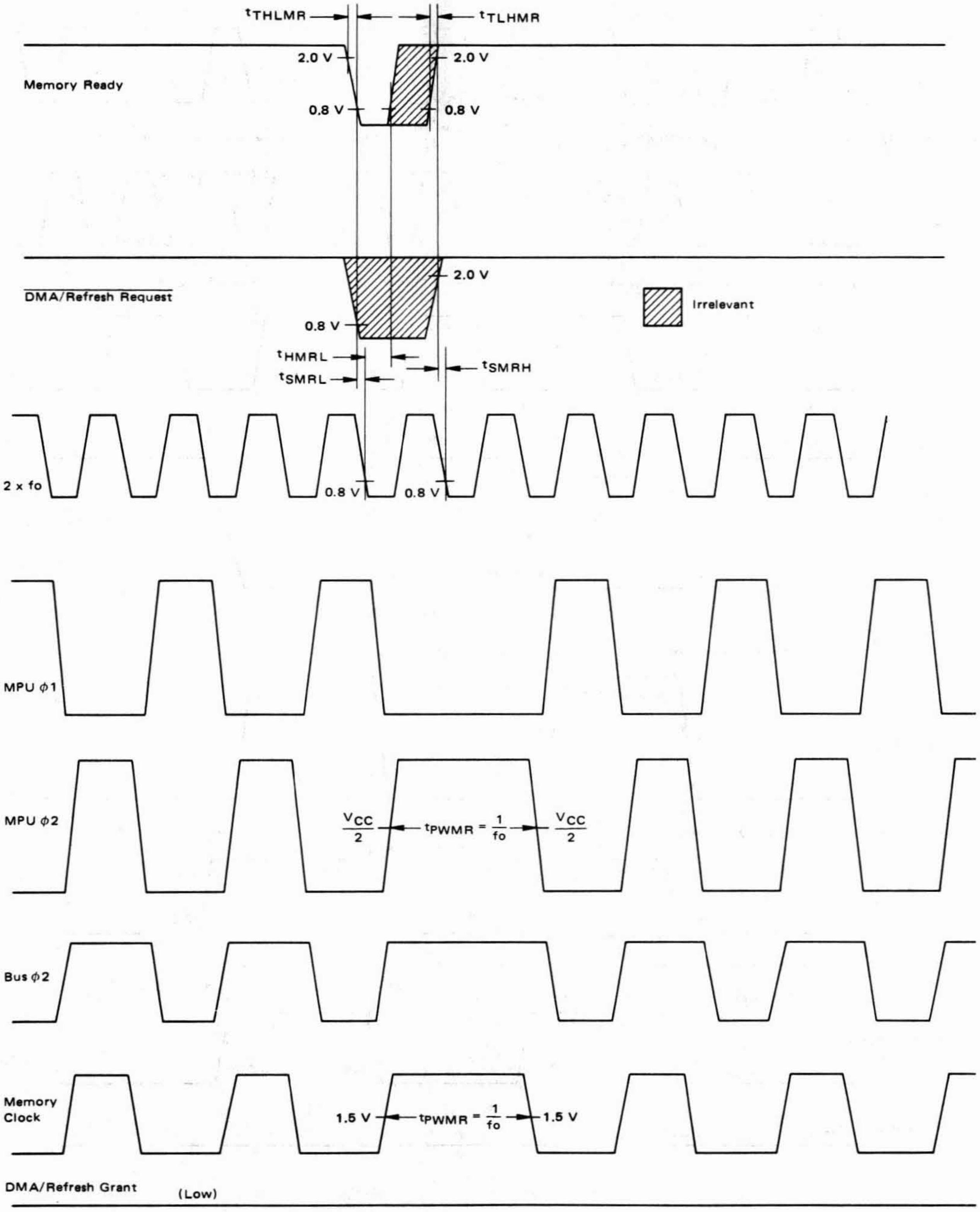

tTHLMR
tTLHMR
2.0 V
2.0 V
Memory Ready
0.8 V
0.8 V
2.0 V
DMA/Refresh Request
Irrelevant
0.8 V
tHMRL
tSMRL
tSMRH
2 x fo
0.8 V
0.8 V
MPU φ1
MPU φ2
VCC/2
tPWMR = 1/fo
VCC/2
Bus φ2
Memory Clock
1.5 V
tPWMR = 1/fo
1.5 V
DMA/Refresh Grant
(Low)

FIGURE 6 – TIMING DIAGRAM FOR $\overline{\text{DMA/REFRESH REQUEST}}$ STRETCH OPERATION
(Minimum Stretch Shown)
Input Voltage: 3.0 to 0 V, $t_{THLDR} = t_{TLHDR} = 5.0$ ns

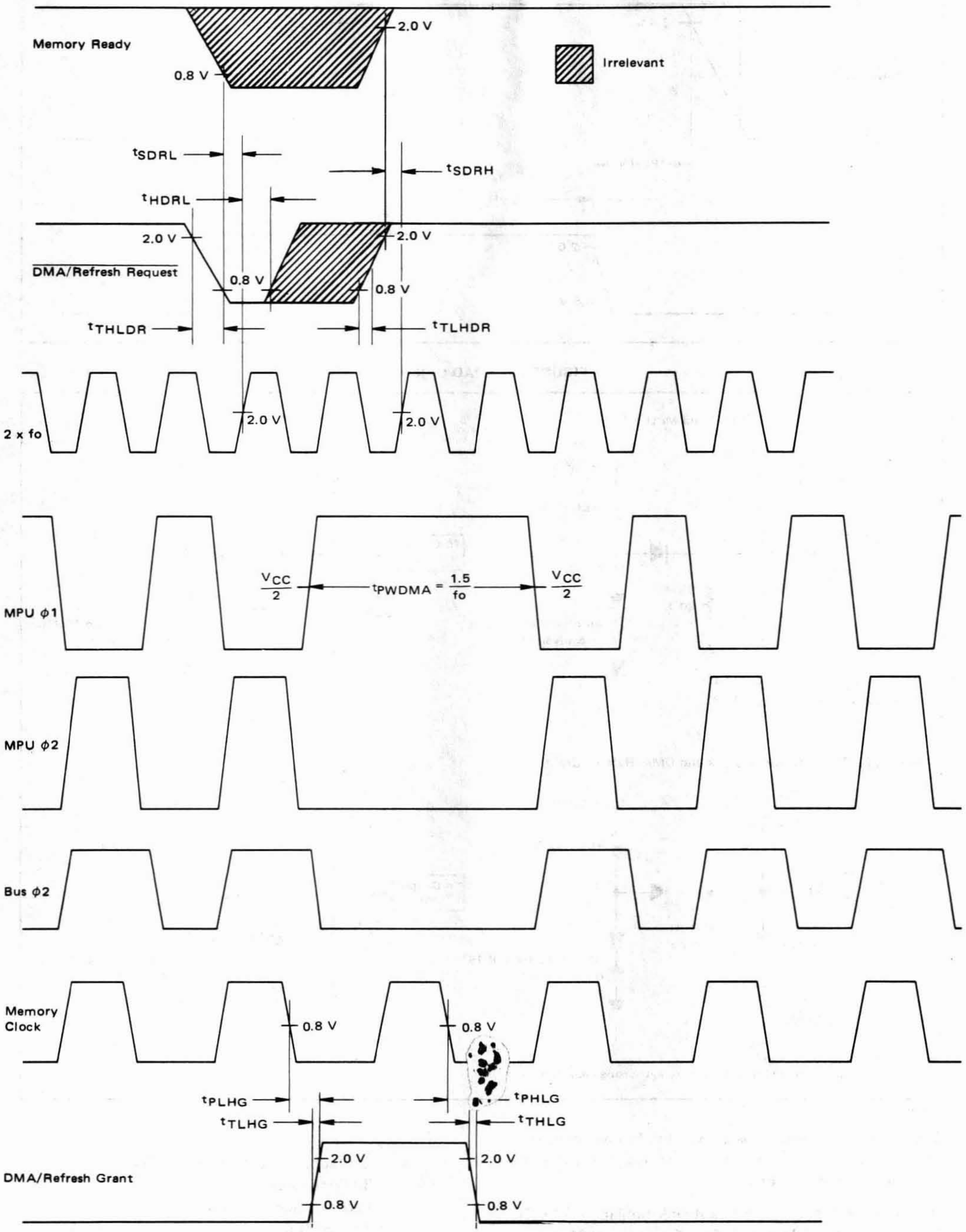

Memory Ready
2.0 V
0.8 V
Irrelevant
tSDRL
tSDRH
tHDRL
2.0 V
2.0 V
DMA/Refresh Request
0.8 V
0.8 V
tTHLDR
tTLHDR
2 x fo
2.0 V
2.0 V
MPU ϕ1
VCC/2
tPWDMA = 1.5/fo
VCC/2
MPU ϕ2
Bus ϕ2
Memory Clock
0.8 V
0.8 V
tPLHG
tPHLG
tTLHG
tTHLG
2.0 V
2.0 V
DMA/Refresh Grant
0.8 V
0.8 V

FIGURE 7 – $\overline{\text{POWER ON RESET}}$

**Input Voltage: 0 to 5.0 V, f = 100 kHz – Pulse Width = 1.0 μs, $t_{TLH} = t_{THL}$ = 25 ns**

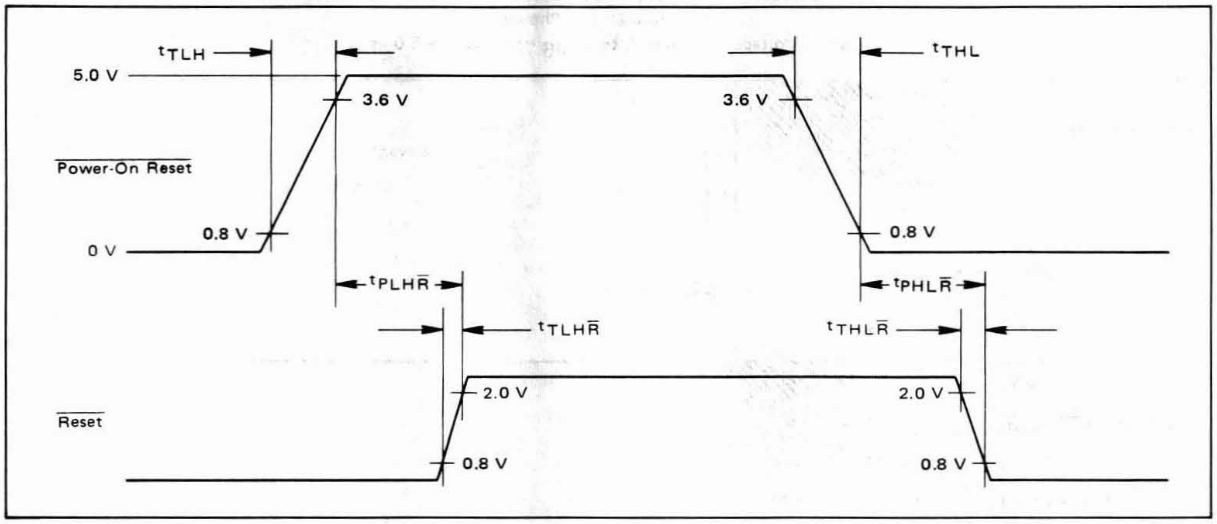
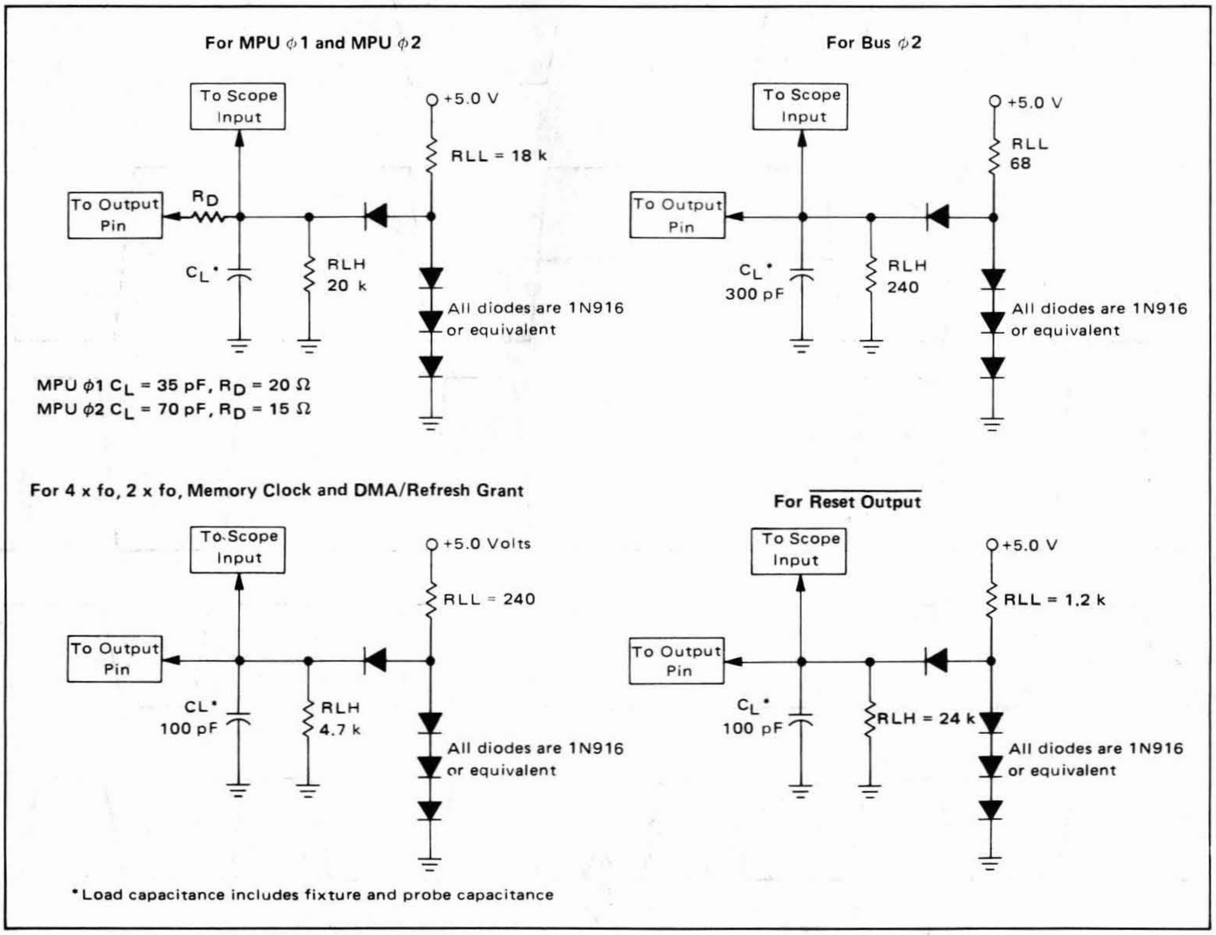

$t_{TLH}$
$t_{THL}$
5.0 V
3.6 V
3.6 V
$\overline{\text{Power-On Reset}}$
0.8 V
0.8 V
0 V
$t_{PLH\overline{R}}$
$t_{PHL\overline{R}}$
$t_{TLH\overline{R}}$
$t_{THL\overline{R}}$
2.0 V
2.0 V
$\overline{\text{Reset}}$
0.8 V
0.8 V

FIGURE 8 – LOAD CIRCUITS


For MPU φ1 and MPU φ2
To Scope Input
+5.0 V
RLL = 18 k
To Output Pin
$R_D$
$C_L$*
RLH 20 k
All diodes are 1N916 or equivalent
MPU φ1 $C_L$ = 35 pF, $R_D$ = 20 Ω
MPU φ2 $C_L$ = 70 pF, $R_D$ = 15 Ω
For Bus φ2
To Scope Input
+5.0 V
RLL 68
To Output Pin
$C_L$* 300 pF
RLH 240
All diodes are 1N916 or equivalent
For 4 x fo, 2 x fo, Memory Clock and DMA/Refresh Grant
To Scope Input
+5.0 Volts
RLL = 240
To Output Pin
CL* 100 pF
RLH 4.7 k
All diodes are 1N916 or equivalent
For $\overline{\text{Reset}}$ Output
To Scope Input
+5.0 V
RLL = 1.2 k
To Output Pin
$C_L$* 100 pF
RLH = 24 k
All diodes are 1N916 or equivalent
*Load capacitance includes fixture and probe capacitance

NOTE:
Operation of the MC6875AL over the full military temperature range (to maximum $T_A$) will result in excessive operating junction temperature.

The use of a clip on 16 pin heat sink similar to AAVID Engineering, Inc., Model 5007 ($R_{\theta CA}$ = 18°C/W) is recommended above $T_A \approx 95°C$.

Contact AAVID Engineering, Inc.
30 Cook Court
Laconia, New Hampshire 03246
Tel. (603) 524-4443

## APPLICATIONS INFORMATION

FIGURE 9 – TYPICAL RC FREQUENCY versus VOLTAGE

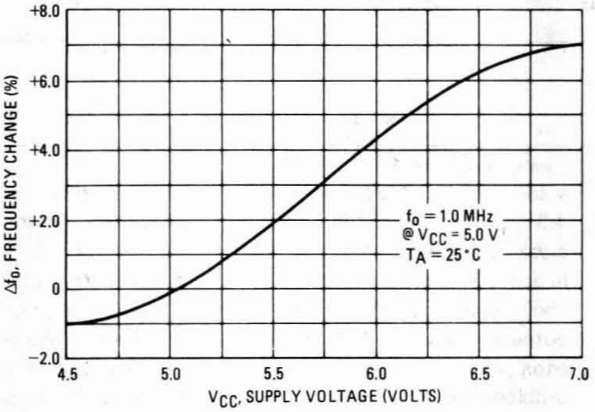


FIGURE 10 – TYPICAL RC FREQUENCY versus TEMPERATURE

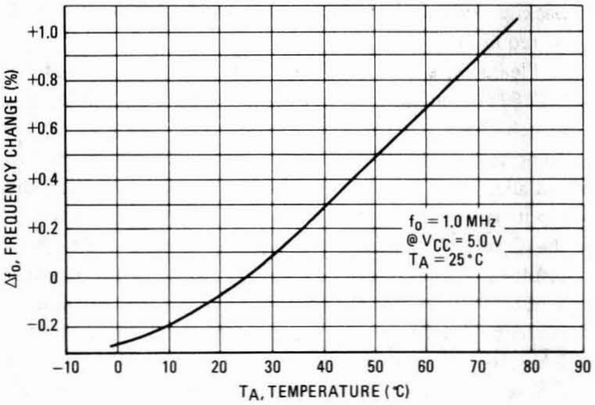
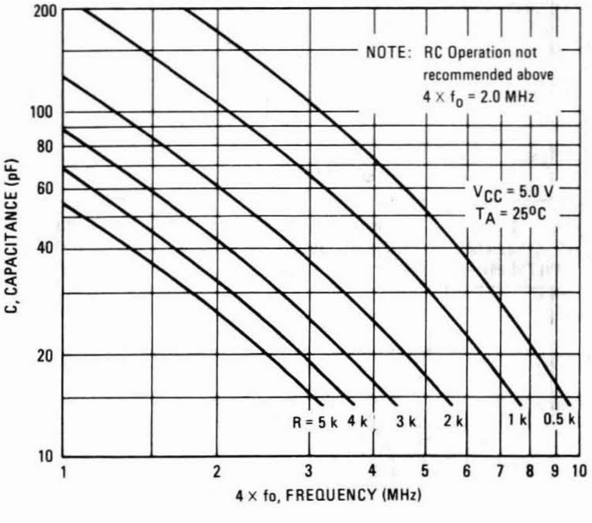


FIGURE 11 – TYPICAL FREQUENCY versus RESISTANCE FOR C VARIABLE



### GENERAL

The MC6875 Clock Generator/Driver should be located on the same board and within two inches of the MC6800 MPU. Series damping resistors of 10-30 ohms may be utilized between the MC6875 and the MC6800 on the $\phi1$ and $\phi2$ clocks to suppress overshoot and reflections.

The $V_{CC}$ pin (pin 16) of the MC6875 should be bypassed to the ground pin (pin 8) at the package with a 0.1 µF capacitor. Because of the high peak currents associated with driving highly capacitive loads, an adequately large ground strip to pin 8 should be used on the MC6875. Grounds should be carefully routed to minimize coupling of noise to the sensitive oscillator inputs. Unnecessary grounds or ground planes should be avoided near pin 2 or the frequency determining components. These components should be located as near as possible to the respective pins of the MC6875. Stray capacitance near pin 2 or the crystal, can affect the frequency. The can of the crystal should not be grounded. The ground side of the crystal or the C of the R-C oscillator should be connected as directly as possible to pin 8.

Unused inputs should be connected to $V_{CC}$ or ground. $\overline{\text{Memory Ready}}$, $\overline{\text{DMA/Refresh Request}}$ and $\overline{\text{Power-On Reset}}$ should be connected to $V_{CC}$ when not used. The External Input should be connected to ground when not used.

### OSCILLATOR

A tank circuit tuned to the desired crystal frequency connected between terminals $X_1$ and $X_2$ as shown in Figure 12, is recommended to prevent the oscillator from starting at other than the desired frequency. The 1kΩ resistor reduces the Q sufficiently to maintain stable crystal control. Crystal manufacturers may recommend a capacitance ($C_L$) to be used in series with the crystal for optimum performance at series resonance.

See Figures 9 and 10 for typical oscillator temperature and $V_{CC}$ supply dependence for R-C operation.

FIGURE 12 – OSCILLATOR–CRYSTAL OPERATION

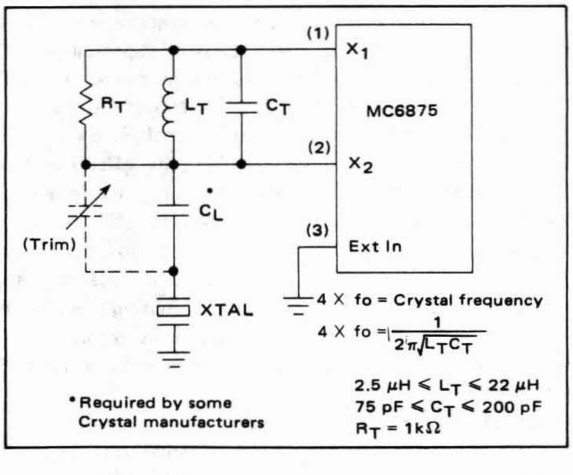
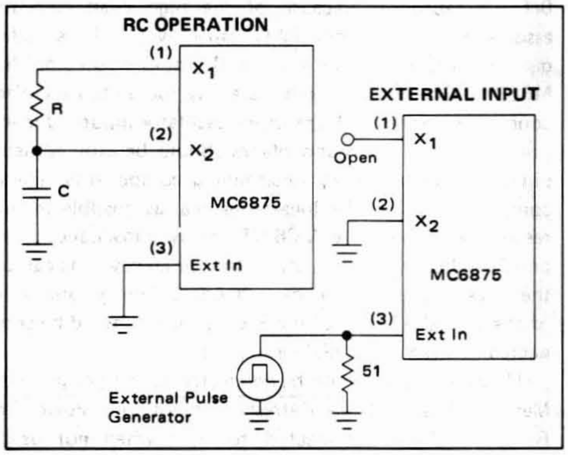


TABLE 1 – OSCILLATOR COMPONENTS

| TANK CIRCUIT PARAMETERS | | APPROXIMATE CRYSTAL PARAMETERS | | | | CTS KNIGHTS<br>400 REIMANN AVE.<br>SANDWICH, IL<br>60548<br>(815) 786-8411 | McCOY ELECT. CO.<br>WATTS & CHESTNUTS STS.<br>MT. HOLLY SPRING, PA<br>17065<br>(717) 486-3411 | TYCO CRYSTAL PRODUCTS<br>3940 W. MONTECITO<br>PHOENIX, AZ<br>85019<br>(602) 272-7945 |
|---|---|---|---|---|---|---|---|---|
| $L_T$ µH | $C_T$ pF | $R_S$ Ohms | Co pF | $C_1$ mpF | fo MHz | | | |
| 10 | 150 | 15-75 | 3-6 | 12 | 4.0 | MP-04A<br>• 390 pF | 113–31 | 150-3260 |
| 4.7 | 82 | 8-45 | 4-7 | 23 | 8.0 | MP-080<br>• 47 pF | 113–32 | 150-3270 |

Inductors may be obtained from: Coilcraft, Cary, IL 60013 (312) 639-2361

FIGURE 13



To precisely time a crystal to desired frequency, a variable trimmer capacitor in the range of 7 to 40 pF would typically be used. Note it is not a recommended practice to tune the crystal with a parallel load capacitance.

The table above shows typical values for $C_T$ and $L_T$, typical crystal characteristics, and manufacturers' part numbers for 4.0 and 8.0 megahertz operation.

The MC6875 will function as an R-C oscillator when connected as shown in Figure 13. The desired output frequency (M$\phi$1) is approximately:

Formula

$$4 \times fo \approx \frac{320}{C\,(R + .27) + 23}$$

C in picofarads
R in K ohms
4 x fo in Megahertz

(See Figure 11)

It would be desirable to select a capacitor greater than 15 pF to minimize the effects of stray capacitance. It is also desirable to keep the resistor in the 1 to 5 k Ω range. There is a nominal 270 Ω resistor internally at $X_1$ which is in series with the external R. By keeping the external R as large as possible, the effects due to process variations of the internal resistor on the frequency will be reduced. There will, however, still be some variation in frequency in a production lot both from the resistance variations, external and internal, and process variations of the input switching thresholds. Therefore, in a production system, it is recommended a potentiometer be placed in series with a fixed R between $X_1$ and $X_2$.

## POWER-ON RESET

As the power to the MC6875 comes up, the $\overline{\text{Reset Output}}$ will be in a high impedance state and will not give a solid $V_{OL}$ output level until $V_{CC}$ has reached 3.5 to 4.0 V. During this time transients may appear on the clock outputs as the oscillator begins to start. This happens at approximately $V_{CC}$ = 3 V. At some $V_{CC}$ level above that, where $\overline{\text{Reset Output}}$ goes low, all the clock outputs will begin functioning normally. This phenomenon of the start-up sequence should not cause any problems except possibly in systems with battery back-up memory. The transients on the clock lines during the time the $\overline{\text{Reset Output}}$ is high impedance could initiate the system in some unknown mode and possibly write into the backup memory system. Therefore in battery backup systems, more elaborate reset circuitry will be required.

Please note that the $\overline{\text{Power-On Reset}}$ input pin of the MC6875 is not suitable for use with a manual MPU reset switch if the $\overline{\text{DMA/Ref Req}}$ or Memory Ready inputs are going to be used. The power on reset circuitry is used to initialize the internal control logic and whenever the input is switched low, the MC6875 is irresponsive to the $\overline{\text{DMA/Ref Req}}$ or Memory Ready inputs. This may result in the loss of dynamic memory and/or possibly a byte of slow static memory. The circuit of Figure 14 is recommended for applications which do not utilize the $\overline{\text{DMA/Ref Req}}$ or Memory Ready inputs. The circuit of Figure 15 is recommended for those applications that do.

FIGURE 14 – MANUAL RESET FOR APPLICATIONS NOT USING $\overline{\text{DMA/REFRESH REQUEST}}$ OR MEMORY READY INPUTS

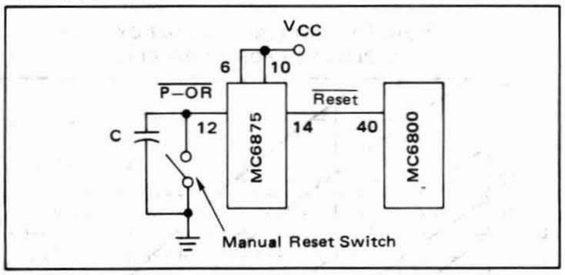
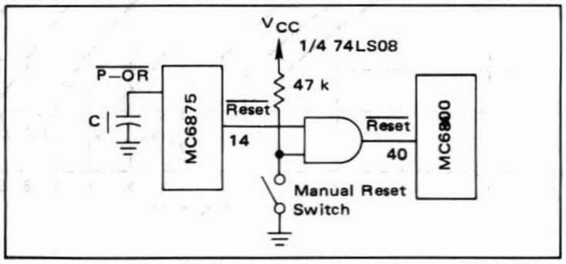


FIGURE 15 – MANUAL RESET FOR SYSTEMS USING DYNAMIC RAM OR SLOW STATIC RAM IN CONJUNCTION WITH MEMORY READY OR $\overline{\text{DMA/REFRESH REQUEST}}$ INPUTS



**MOTOROLA**

# AM26LS31

## QUAD LINE DRIVER WITH NAND ENABLED THREE-STATE OUTPUTS

The Motorola AM26LS31 is a quad differential line driver intended for digital data transmission over balanced lines. It meets all the requirements of EIA Standard RS-422 and Federal Standard 1020.

The AM26LS31 provides an enable/disable function common to all four drivers as opposed to the split enables on the MC3487 RS-422 driver.

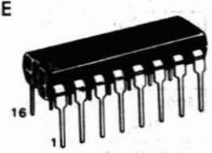
The high impedance output state is assured during power down.

- Full RS-422 Standard Compliance
- Single +5 V Supply
- Meets Full $V_O = 6.0$ V, $V_{CC} = 0$ V, $I_O < 100\ \mu A$ Requirement
- Output Short Circuit Protection
- Complementary Outputs for Balanced Line Operation
- High Output Drive Capability
- Advanced LS Processing
- PNP Inputs for MOS Compatibility

## QUAD RS-422 LINE DRIVER WITH THREE-STATE OUTPUTS

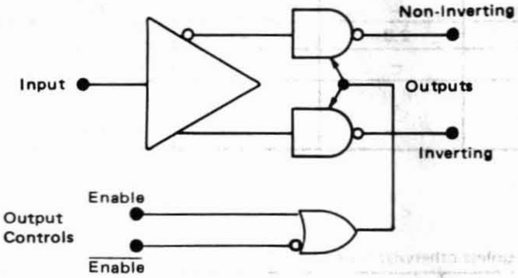
**SILICON MONOLITHIC INTEGRATED CIRCUIT**

**D SUFFIX**
CERAMIC PACKAGE
CASE 620-02

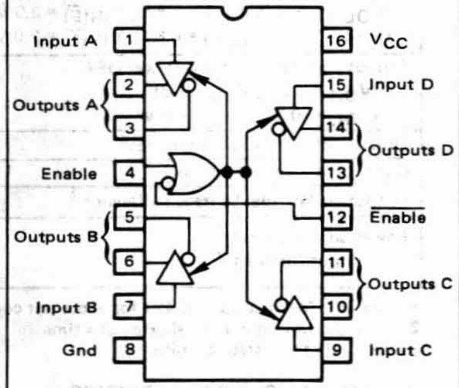


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### DRIVER BLOCK DIAGRAM


Non-Inverting
Input
Outputs
Inverting
Enable
Output Controls
$\overline{\text{Enable}}$

### PIN CONNECTIONS


Input A 1
Outputs A 2 3
Enable 4
Outputs B 5 6
Input B 7
Gnd 8
16 $V_{CC}$
15 Input D
14 13 Outputs D
12 $\overline{\text{Enable}}$
11 10 Outputs C
9 Input C

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| AM26LS31DC | 0 to 70°C | Ceramic DIP |
| AM26LS31PC | 0 to 70°C | Plastic DIP |

### TRUTH TABLE

| Input | Control Inputs ($E/\overline{E}$) | Non-Inverting Output | Inverting Output |
|---|---|---|---|
| H | H/L | H | L |
| L | H/L | L | H |
| X | L/H | Z | Z |

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

## *ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 8.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Operating Junction Temperature Range<br>Ceramic Package<br>Plastic Package | $T_J$ | <br>175<br>150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

*"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted specifications apply $4.75\text{ V} \le V_{CC} \le 5.25\text{ V}$ and $0^\circ\text{C} \le T_A \le 70^\circ\text{C}$. Typical values measured at $V_{CC} = 5.0\text{ V}$, and $T_A = 25^\circ\text{C}$.)

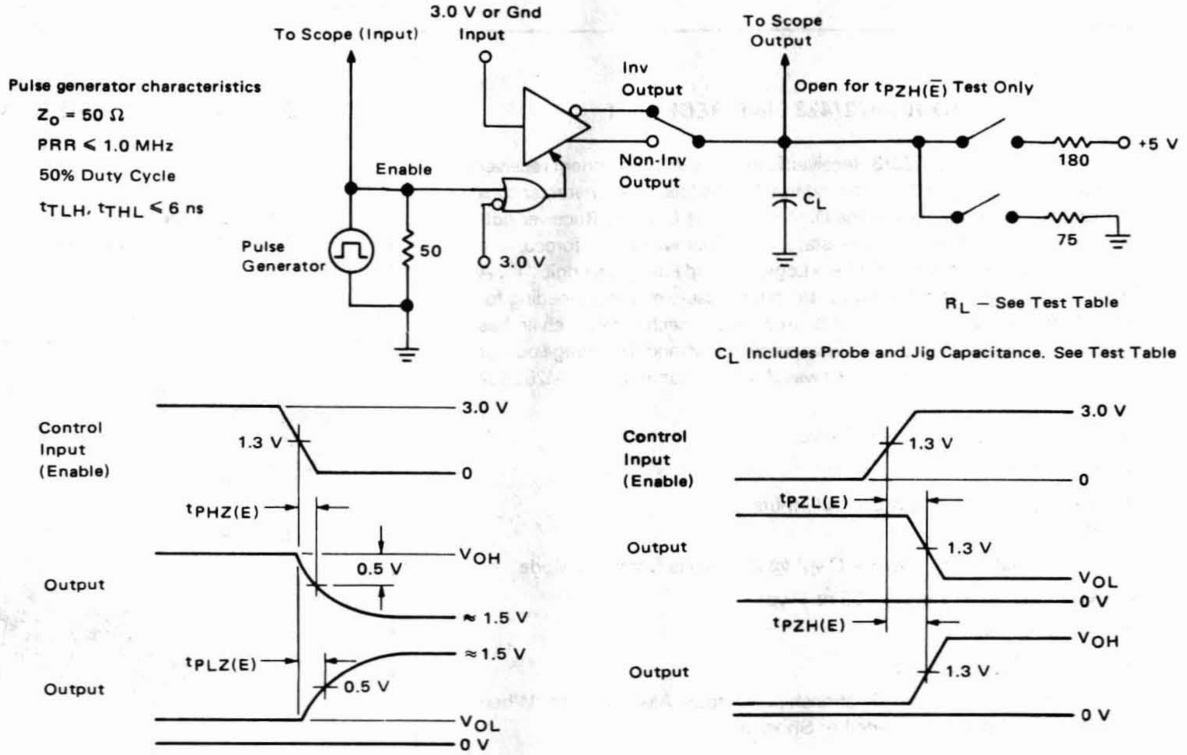
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage – Low Logic State | $V_{IL}$ | – | – | 0.8 | Vdc |
| Input Voltage – High Logic State | $V_{IH}$ | 2.0 | – | – | Vdc |
| Input Current – Low Logic State<br>($V_{IL} = 0.4$ V) | $I_{IL}$ | – | – | −360 | µA |
| Input Current – High Logic State<br>($V_{IH} = 2.7$ V)<br>($V_{IH} = 7.0$ V) | $I_{IH}$ | <br>–<br>– | <br>–<br>– | <br>+20<br>+100 | µA |
| Input Clamp Voltage<br>($I_{IK} = -18$ mA) | $V_{IK}$ | – | – | −1.5 | V |
| Output Voltage – Low Logic State<br>($I_{OL} = 20$ mA) | $V_{OL}$ | – | – | 0.5 | V |
| Output Voltage – High Logic State<br>($I_{OH} = -20$ mA) | $V_{OH}$ | 2.5 | – | – | V |
| Output Short-Circuit Current<br>($V_{IH} = 2.0$ V) [2] | $I_{OS}$ | −30 | – | −150 | mA |
| Output Leakage Current – Hi-Z State<br>($V_{OL} = 0.5$ V, $V_{IL(E)} = 0.8$ V, $V_{IH(\overline{E})} = 2.0$ V)<br>($V_{OH} = 2.5$ V, $V_{IL(E)} = 0.8$ V, $V_{IH(\overline{E})} = 2.0$ V) | $I_{O(Z)}$ | <br>–<br>– | <br>–<br>– | <br>−20<br>+20 | µA |
| Output Leakage Current – Power OFF<br>($V_{OH} = 6.0$ V, $V_{CC} = 0$ V)<br>($V_{OL} = -0.25$ V, $V_{CC} = 0$ V) | $I_{O(off)}$ | <br>–<br>– | <br>–<br>– | <br>+100<br>−100 | µA |
| Output Offset Voltage Difference[1] | $V_{OS}-\overline{V}_{OS}$ | – | – | ±0.4 | V |
| Output Differential Voltage 1 | $V_{OD}$ | 2.0 | – | – | V |
| Output Differential Voltage Difference 1 | $\lvert\Delta V_{OD}\rvert$ | – | – | ±0.4 | V |
| Power Supply Current<br>(Output Disabled)[3] | $I_{CCX}$ | – | 60 | 80 | mA |

1. See EIA Specification RS-422 for exact test conditions.
2. Only one output may be shorted at a time.
3. Circuit in three-state condition.

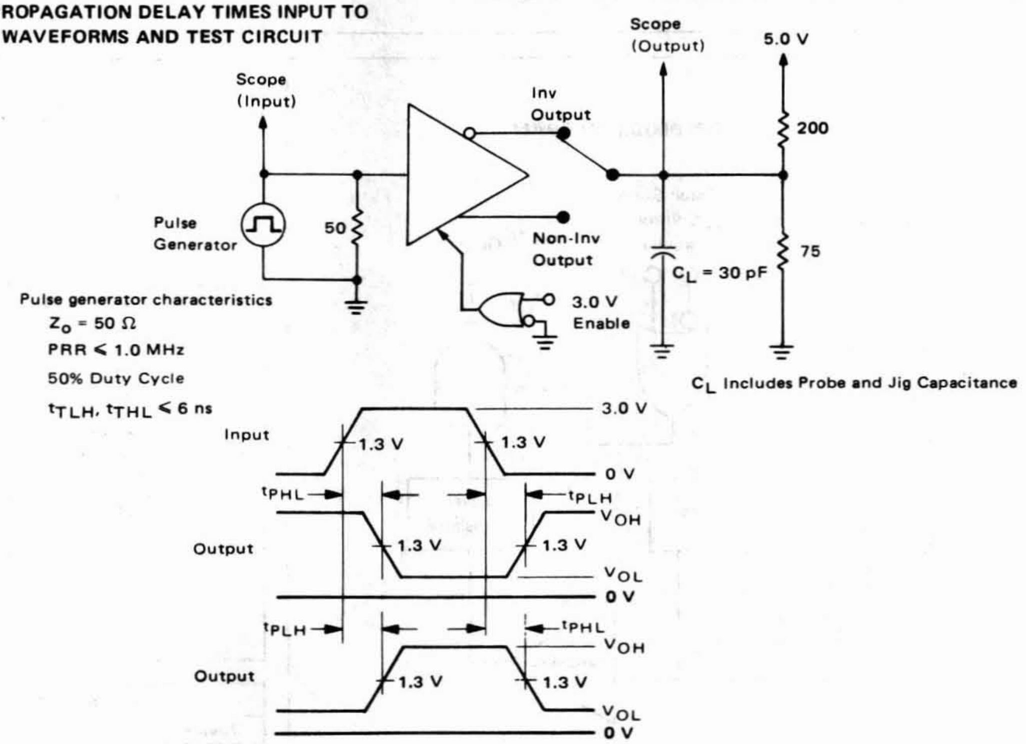
**SWITCHING CHARACTERISTICS** ($V_{CC} = 5.0$ V, $T_A = 25^\circ$C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Times<br>High to Low Output<br>Low to High Output | <br>$t_{PHL}$<br>$t_{PLH}$ | <br>–<br>– | <br>–<br>– | <br>20<br>20 | ns |
| Output Skew | | – | – | 6.0 | ns |
| Propagation Delay – Control to Output<br>($C_L = 10$ pF, $R_L = 75\ \Omega$ to Gnd)<br>($C_L = 10$ pF, $R_L = 180\ \Omega$ to $V_{CC}$)<br>($C_L = 30$ pF, $R_L = 75\ \Omega$ to Gnd)<br>($C_L = 30$ pF, $R_L = 180\ \Omega$ to $V_{CC}$) | <br>$t_{PHZ(E)}$<br>$t_{PLZ(E)}$<br>$t_{PZH(E)}$<br>$t_{PZL(E)}$ | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | <br>30<br>35<br>40<br>45 | ns |

## FIGURE 1 – THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS


Pulse generator characteristics
$Z_o$ = 50 Ω
PRR ≤ 1.0 MHz
50% Duty Cycle
$t_{TLH}$, $t_{THL}$ ≤ 6 ns
To Scope (Input)
3.0 V or Gnd
Input
Enable
Pulse Generator
50
3.0 V
Inv Output
Non-Inv Output
To Scope Output
Open for $t_{PZH(\overline{E})}$ Test Only
+5 V
180
75
$C_L$
$R_L$ – See Test Table
$C_L$ Includes Probe and Jig Capacitance. See Test Table
Control Input (Enable)
1.3 V
3.0 V
0
$t_{PHZ(E)}$
Output
$V_{OH}$
0.5 V
≈ 1.5 V
$t_{PLZ(E)}$
Output
≈1.5 V
0.5 V
$V_{OL}$
0 V
Control Input (Enable)
1.3 V
3.0 V
0
$t_{PZL(E)}$
Output
1.3 V
$V_{OL}$
0 V
$t_{PZH(E)}$
$V_{OH}$
Output
1.3 V
0 V

## FIGURE 2 – PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT


Scope (Input)
Pulse Generator
50
Inv Output
Non-Inv Output
3.0 V
Enable
Scope (Output)
5.0 V
200
75
$C_L$ = 30 pF
$C_L$ Includes Probe and Jig Capacitance
Pulse generator characteristics
$Z_o$ = 50 Ω
PRR ≤ 1.0 MHz
50% Duty Cycle
$t_{TLH}$, $t_{THL}$ ≤ 6 ns
Input
1.3 V
1.3 V
3.0 V
0 V
$t_{PHL}$
$t_{PLH}$
Output
1.3 V
1.3 V
$V_{OH}$
$V_{OL}$
0 V
$t_{PLH}$
$t_{PHL}$
Output
1.3 V
1.3 V
$V_{OH}$
$V_{OL}$
0 V

**MOTOROLA**

# AM26LS32

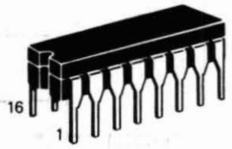
## QUAD RS-422/423 LINE RECEIVER

Motorola's Quad RS-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when Pin 4 is a Logic "0" and Pin 12 is a Logic "1". A PNP device buffers each output control pin to assure minimum loading for either Logic "1" or Logic "0" inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of AM26LS32 features include:

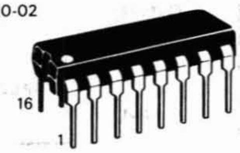
- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis — 30 mV (Typ) @ Zero Volts Common Mode
- Fast Propagation Times — 25 ns (Typ)
- TTL Compatible
- Single 5 V Supply Voltage
- Fail-Safe Input-Output Relationship. Output Always High When Inputs Are Open, Terminated or Shorted
- 6K Minimum Input Impedance

## QUAD RS-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

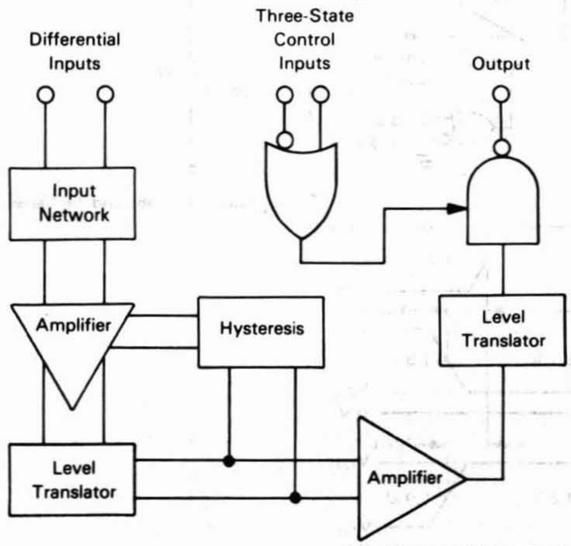


**D SUFFIX**
CERAMIC PACKAGE
CASE 620-02

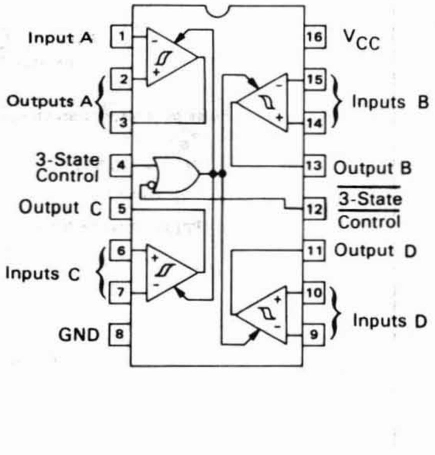


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### RECEIVER CHAIN BLOCK DIAGRAM


Differential Inputs
Three-State Control Inputs
Output
Input Network
Amplifier
Hysteresis
Level Translator
Level Translator
Amplifier

### PIN CONNECTIONS


Input A
1
Outputs A
2
3
3-State Control
4
Output C
5
Inputs C
6
7
GND
8
16
$V_{CC}$
15
14
Inputs B
13
Output B
12
$\overline{\text{3-State}}$ Control
11
Output D
10
9
Inputs D

| ORDERING INFORMATION | | |
|---|---|---|
| **Device** | **Temperature** | **Package** |
| AM26LS32D | 0 to +70°C | Ceramic DIP |
| AM26LS32P | 0 to +70°C | Plastic DIP |

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 7.0 | Vdc |
| Input Common Mode Voltage | $V_{ICM}$ | ±25 | Vdc |
| Input Differential Voltage | $V_{ID}$ | ±25 | Vdc |
| Three-State Control Input Voltage | $V_I$ | 7.0 | Vdc |
| Output Sink Current | $I_O$ | 50 | mA |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | | °C |
| Ceramic Package | | +175 | |
| Plastic Package | | +150 | |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

## RECOMMENDED OPERATING CONDITIONS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.75 to 5.25 | Vdc |
| Operating Ambient Temperature | $T_A$ | 0 to +70 | °C |
| Input Common Mode Voltage Range | $V_{ICR}$ | −7.0 to +7.0 | Vdc |
| Input Differential Voltage Range | $V_{IDR}$ | 6.0 | Vdc |

## ELECTRICAL CHARACTERISTICS

(Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25°C$, $V_{CC} = 5.0$ V and $V_{IC} = 0$.V. See Note 1.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage — High Logic State<br>(Three-State Control) | $V_{IH}$ | 2.0 | — | — | V |
| Input Voltage — Low Logic State<br>(Three-State Control) | $V_{IL}$ | — | — | 0.8 | V |
| Differential Input Threshold Voltage (Note 4)<br>$(-7.0\text{ V} \leqslant V_{IC} \leqslant 7.0\text{ V}, V_{IH} = 2.0\text{ V})$<br>$(I_O = -0.4\text{ mA}, V_{OH} \geqslant 2.7\text{ V})$<br>$(I_O = 8.0\text{ mA}, V_{OL} \leqslant 0.45\text{ V})$ | $V_{TH(D)}$ | <br><br>—<br>— | <br><br>—<br>— | <br><br>0.2<br>-0.2 | V |
| Input Bias Current<br>$(V_{CC} = 0\text{ V or } 5.25)$ (Other Inputs at $-15\text{ V} \leqslant V_{in} \leqslant +15\text{ V}$)<br>$V_{in} = +15$ V<br>$V_{in} = -15$ V | $I_{IB(D)}$ | <br><br>—<br>— | <br><br>—<br>— | <br><br>2.3<br>-2.8 | mA |
| Input Resistance $(-15\text{ V} \leqslant V_{in} \leqslant +15\text{ V})$ | $R_{in}$ | 6.0 K | — | — | Ohms |
| Input Balance and Output Level<br>$(-7.0\text{ V} \leqslant V_{IC} \leqslant 7.0\text{ V}, V_{IH} = 2.0\text{ V},$<br>See Note 3)<br>$(I_O = -0.4\text{ mA}, V_{ID} = 0.4\text{ V})$<br>$(I_O = 8.0\text{ mA}, V_{ID} = -0.4\text{ V})$ | <br><br><br>$V_{OH}$<br>$V_{OL}$ | <br><br><br>2.7<br>— | <br><br><br>—<br>— | <br><br><br>—<br>0.45 | V |
| Output Third State Leakage Current<br>$(V_{I(D)} = +3.0\text{ V}, V_{IL} = 0.8\text{ V}, V_O = 0.4\text{ V})$<br>$(V_{I(D)} = -3.0\text{ V}, V_{IL} = 0.8\text{ V}, V_O = 2.4\text{ V})$ | $I_{OZ}$ | <br>—<br>— | <br>—<br>— | <br>-20<br>20 | µA |
| Output Short-Circuit Current<br>$(V_{I(D)} = 3.0\text{ V}, V_{IH} = 2.0\text{ V}, V_O = 0\text{ V})$<br>See Note 2) | $I_{OS}$ | −15 | — | -85 | mA |
| Input Current — Low Logic State<br>(Three-State Control)<br>$(V_{IL} = 0.4\text{ V})$ | $I_{IL}$ | | — | -360 | µA |
| Input Current — High Logic State<br>(Three-State Control)<br>$(V_{IH} = 2.7\text{ V})$<br>$(V_{IH} = 5.5\text{ V})$ | $I_{IH}$ | <br><br>—<br>— | <br><br>—<br>— | <br><br>20<br>100 | µA |
| Input Clamp Diode Voltage<br>(Three-State Control)<br>$(I_{IC} = -18\text{ mA})$ | $V_{IC}$ | — | — | -1.5 | V |
| Power Supply Current<br>$(V_{IL} = 0\text{ V})$ (All Inputs Grounded) | $I_{CC}$ | — | — | 70 | mA |

**SWITCHING CHARACTERISTICS** (Unless otherwise noted, $V_{CC}$ = 5.0 V and $T_A$ = 25°C)

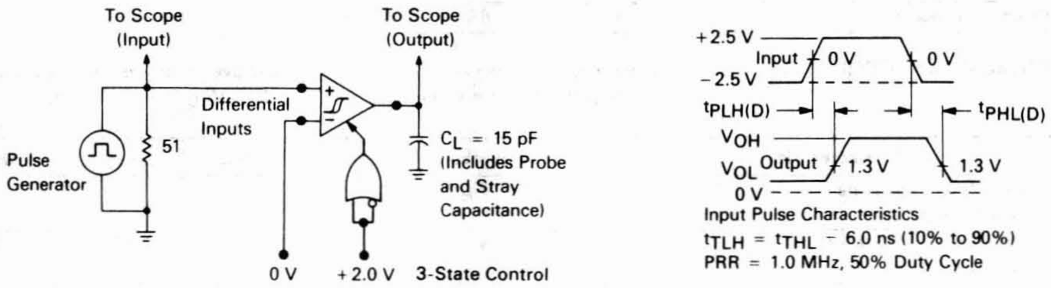
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Time — Differential Inputs to Output | | | | | ns |
| (Output High to Low) | $t_{PHL(D)}$ | – | – | 30 | |
| (Output Low to High) | $t_{PLH(D)}$ | – | – | 30 | |
| Propagation Delay Time — Three-State Control to Output | | | | | ns |
| (Output Low to Third State) | $t_{PLZ}$ | – | – | 35 | |
| (Output High to Third State) | $t_{PHZ}$ | – | – | 35 | |
| (Output Third State to High) | $t_{PZH}$ | – | – | 30 | |
| (Output Third State to Low) | $t_{PZL}$ | – | – | 30 | |

**NOTES:**

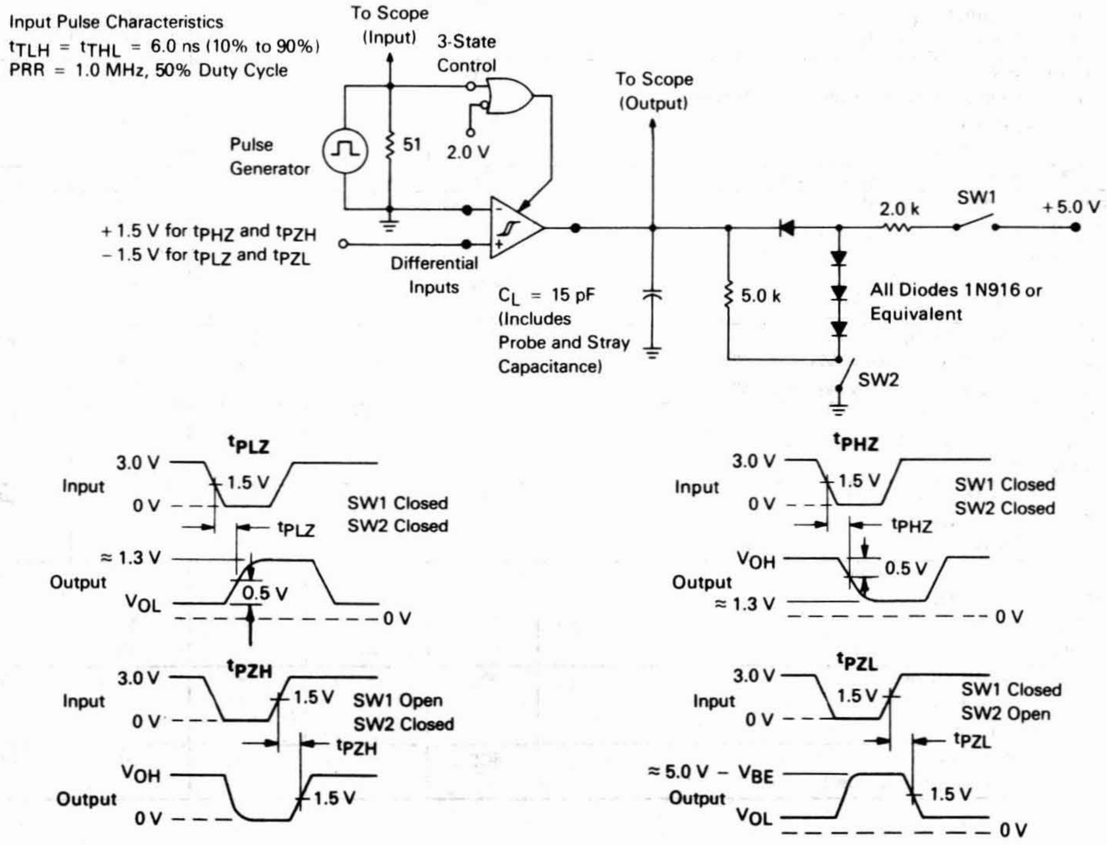
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Only one output at a time should be shorted.
3. Refer to EIA RS422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.

## SWITCHING TEST CIRCUIT AND WAVE FOR

### FIGURE 1 - PROPAGATION DELAY DIFFERENTIAL INPUT TO OUTPUT


To Scope (Input)
To Scope (Output)
Differential Inputs
Pulse Generator
51
$C_L$ = 15 pF (Includes Probe and Stray Capacitance)
0 V
+2.0 V
3-State Control
+2.5 V
Input
0 V
0 V
−2.5 V
$t_{PLH(D)}$
$t_{PHL(D)}$
$V_{OH}$
$V_{OL}$
Output
1.3 V
1.3 V
0 V
Input Pulse Characteristics
$t_{TLH}$ = $t_{THL}$ = 6.0 ns (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle

### FIGURE 2 — PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT


Input Pulse Characteristics
$t_{TLH}$ = $t_{THL}$ = 6.0 ns (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle
To Scope (Input)
3-State Control
To Scope (Output)
Pulse Generator
51
2.0 V
+1.5 V for $t_{PHZ}$ and $t_{PZH}$
−1.5 V for $t_{PLZ}$ and $t_{PZL}$
Differential Inputs
$C_L$ = 15 pF (Includes Probe and Stray Capacitance)
2.0 k
SW1
+5.0 V
5.0 k
All Diodes 1N916 or Equivalent
SW2
$t_{PLZ}$
3.0 V
Input
1.5 V
0 V
SW1 Closed
SW2 Closed
$t_{PLZ}$
≈ 1.3 V
Output
$V_{OL}$
0.5 V
0 V
$t_{PHZ}$
3.0 V
Input
1.5 V
0 V
SW1 Closed
SW2 Closed
$t_{PHZ}$
$V_{OH}$
0.5 V
Output
≈ 1.3 V
0 V
$t_{PZH}$
3.0 V
Input
1.5 V
0 V
SW1 Open
SW2 Closed
$t_{PZH}$
$V_{OH}$
Output
1.5 V
0 V
$t_{PZL}$
3.0 V
Input
1.5 V
0 V
SW1 Closed
SW2 Open
$t_{PZL}$
≈ 5.0 V − $V_{BE}$
Output
1.5 V
$V_{OL}$
0 V

**MOTOROLA**

# MC8T26A
# MC6880A

## QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the −48 mA driver and −20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

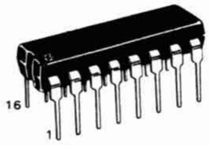
The MC8T26A is identical to the NE8T26A and it operates from a single +5 V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor

## QUAD THREE-STATE BUS TRANSCEIVER

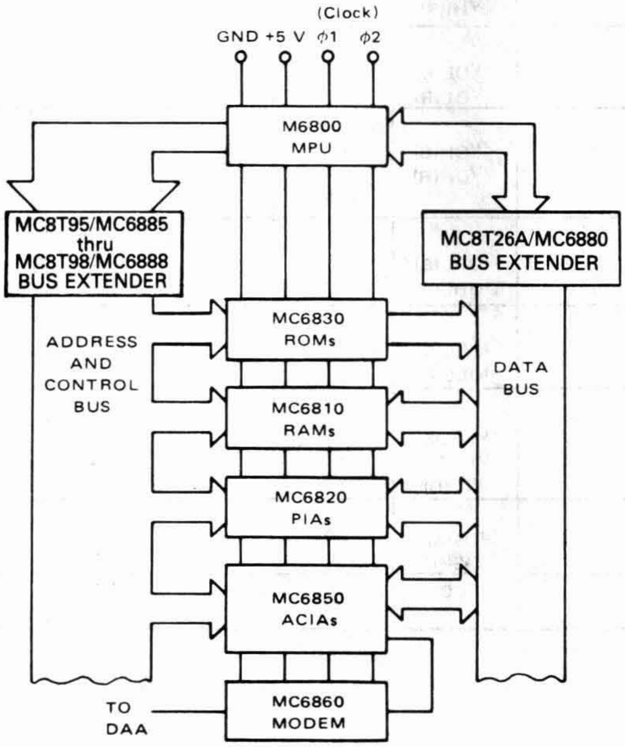
**MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS**

**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

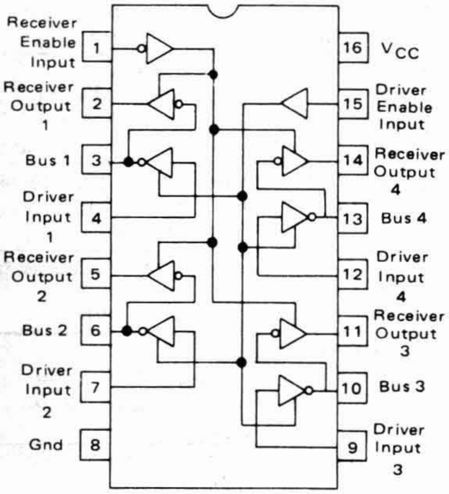


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### MICROPROCESSOR BUS EXTENDER APPLICATION


(Clock)
GND +5 V ϕ1 ϕ2
M6800 MPU
MC8T95/MC6885 thru MC8T98/MC6888 BUS EXTENDER
MC8T26A/MC6880 BUS EXTENDER
MC6830 ROMs
MC6810 RAMs
MC6820 PIAs
MC6850 ACIAs
MC6860 MODEM
ADDRESS AND CONTROL BUS
DATA BUS
TO DAA

### PIN CONNECTIONS – MC8T26A MC6880A


Receiver Enable Input 1
Receiver Output 1 2
Bus 1 3
Driver Input 1 4
Receiver Output 2 5
Bus 2 6
Driver Input 2 7
Gnd 8
16 VCC
15 Driver Enable Input
14 Receiver Output 4
13 Bus 4
12 Driver Input 4
11 Receiver Output 3
10 Bus 3
9 Driver Input 3

**ORDERING INFORMATION**

| Device | Alternate | Temperature Range | Package |
|---|---|---|---|
| MC6880AL | MC8T26AL | 0 to +75°C | Ceramic DIP |
| MC6880AP | MC8T26AP | 0 to +75°C | Plastic DIP |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 8.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Junction Temperature | $T_J$ | | °C |
| Ceramic Package | | 175 | |
| Plastic Package | | 150 | |
| Operating Ambient Temperature Range | $T_A$ | 0 to +75 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** (4.75 V ≤ $V_{CC}$ ≤ 5.25 V and 0°C ≤ $T_A$ ≤ 75°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Current – Low Logic State | | | | | |
| (Receiver Enable Input, $V_{IL(\overline{RE})}$ = 0.4 V) | $I_{IL(\overline{RE})}$ | – | – | -200 | µA |
| (Driver Enable Input, $V_{IL(DE)}$ = 0.4 V) | $I_{IL(DE)}$ | – | – | -200 | |
| (Driver Input, $V_{IL(D)}$ = 0.4 V) | $I_{IL(D)}$ | – | – | -200 | |
| (Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V) | $I_{IL(B)}$ | – | – | -200 | |
| Input Disabled Current – Low Logic State<br>(Driver Input, $V_{IL(D)}$ = 0.4 V) | $I_{IL(D)\,DIS}$ | – | – | -25 | µA |
| Input Current-High Logic State | | | | | |
| (Receiver Enable Input, $V_{IH(\overline{RE})}$ = 5.25 V) | $I_{IH(\overline{RE})}$ | – | – | 25 | µA |
| (Driver Enable Input, $V_{IH(DE)}$ = 5.25 V) | $I_{IH(DE)}$ | – | – | 25 | |
| (Driver Input, $V_{IH(D)}$ = 5.25 V) | $I_{IH(D)}$ | – | – | 25 | |
| (Receiver Input, $V_{IH(B)}$ = 5.25 V) | $I_{IH(B)}$ | – | – | 100 | |
| Input Voltage – Low Logic State | | | | | |
| (Receiver Enable Input) | $V_{IL(\overline{RE})}$ | – | – | 0.85 | V |
| (Driver Enable Input | $V_{IL(DE)}$ | – | – | 0.85 | |
| (Driver Input) | $V_{IL(D)}$ | – | – | 0.85 | |
| (Receiver Input) | $V_{IL(B)}$ | – | – | 0.85 | |
| Input Voltage – High Logic State | | | | | |
| (Receiver Enable Input) | $V_{IH(\overline{RE})}$ | 2.0 | – | – | V |
| (Driver Enable Input) | $V_{IH(DE)}$ | 2.0 | – | – | |
| (Driver Input) | $V_{IH(D)}$ | 2.0 | – | – | |
| (Receiver Input) | $V_{IH(B)}$ | 2.0 | – | – | |
| Output Voltage – Low Logic State | | | | | |
| (Bus Driver) Output, $I_{OL(B)}$ = 48 mA) | $V_{OL(B)}$ | – | – | 0.5 | V |
| (Receiver Output, $I_{OL(R)}$ = 20 mA) | $V_{OL(R)}$ | – | – | 0.5 | |
| Output Voltage – High Logic State | | | | | |
| (Bus (Driver) Output, $I_{OH(B)}$ = –10 mA) | $V_{OH(B)}$ | 2.4 | 3.1 | – | V |
| (Receiver Output, $I_{OH(R)}$ = –2.0 mA) | $V_{OH(R)}$ | 2.4 | 3.1 | – | |
| (Receiver Output, $I_{OH(R)}$ = –100 µA, $V_{CC}$ = 5.0 V) | | 3.5 | – | – | |
| Output Disabled Leakage Current – High Logic State | | | | | |
| (Bus Driver) Output, $V_{OH(B)}$ = 2.4 V) | $I_{OHL(B)}$ | – | – | 100 | µA |
| (Receiver Output, $V_{OH(R)}$ = 2.4 V) | $I_{OHL(R)}$ | – | – | 100 | |
| Output Disabled Leakage Current – Low Logic State | | | | | |
| (Bus Output, $V_{OL(B)}$ = 0.5 V) | $I_{OLL(B)}$ | – | – | –100 | µA |
| (Receiver Output, $V_{OL(R)}$ = 0.5 V) | $I_{OLL(R)}$ | – | – | –100 | |
| Input Clamp Voltage | | | | | |
| (Driver Enable Input $I_{ID(DE)}$ = –12 mA) | $V_{IC(DE)}$ | – | – | -1.0 | V |
| (Receiver Enable Input $I_{IC(RE)}$ = +12 mA) | $V_{IC(RE)}$ | – | – | -1.0 | |
| (Driver Input $I_{IC(D)}$ = –12 mA) | $V_{IC(D)}$ | – | – | -1.0 | |
| Output Short-Circuit Current, $V_{CC}$ = 5.25 V (1) | | | | | |
| (Bus (Driver) Output) | $I_{OS(B)}$ | -50 | – | -150 | mA |
| (Receiver Output) | $I_{OS(R)}$ | -30 | – | -75 | |
| Power Supply Current<br>($V_{CC}$ = 5.25 V) | $I_{CC}$ | – | – | 87 | mA |

(1) Only one output may be short-circuited at a time.

**SWITCHING CHARACTERISTICS** (Unless otherwise noted, specifications apply at $T_A = 25^{\circ}C$ and $V_{CC} = 5.0$ V)

| Characteristic | Symbol | Figure | Min | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output | $t_{PLH(R)}$ | 1 | – | 14 | ns |
| Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output | $t_{PHL(R)}$ | 1 | – | 14 | ns |
| Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output | $t_{PLH(D)}$ | 2 | – | 14 | ns |
| Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output | $t_{PHL(D)}$ | 2 | – | 14 | ns |
| Propagation Delay Time from $\overline{\text{Receiver}}$ $\overline{\text{Enable}}$ Input to High Impedance (Open) Logic State Receiver Output | $t_{PLZ(RE)}$ | 3 | – | 15 | ns |
| Propagation Delay Time from $\overline{\text{Receiver}}$ $\overline{\text{Enable}}$ Input to Low Logic Level Receiver Output | $t_{PZL(RE)}$ | 3 | – | 20 | ns |
| Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output | $t_{PLZ(DE)}$ | 4 | – | 20 | ns |
| Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output | $t_{PZL(DE)}$ | 4 | – | 25 | ns |

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$ AND $t_{PHL(R)}$

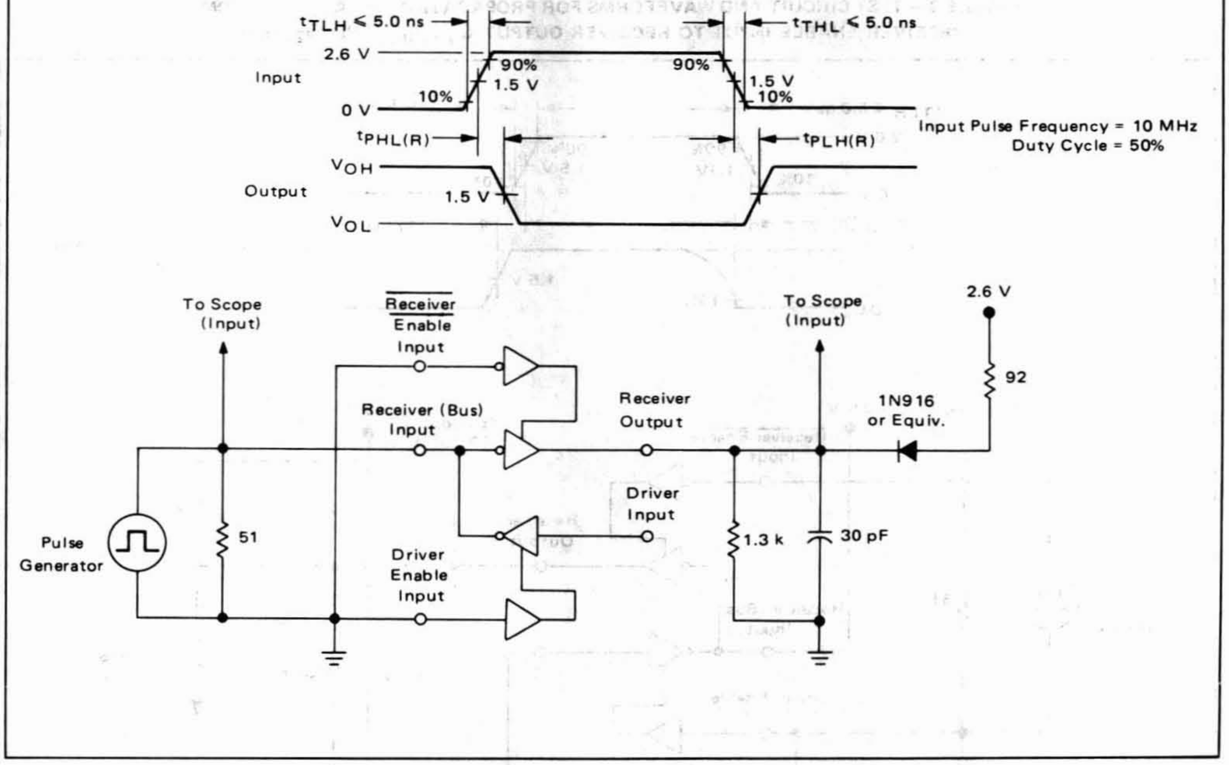

$t_{TLH} \leq 5.0$ ns
$t_{THL} \leq 5.0$ ns
2.6 V
Input
0 V
90%
1.5 V
10%
90%
1.5 V
10%
$t_{PHL(R)}$
$t_{PLH(R)}$
Input Pulse Frequency = 10 MHz
Duty Cycle = 50%
$V_{OH}$
Output
1.5 V
$V_{OL}$
To Scope (Input)
$\overline{\text{Receiver}}$ $\overline{\text{Enable}}$ Input
Receiver (Bus) Input
Receiver Output
To Scope (Input)
2.6 V
92
1N916 or Equiv.
Driver Input
Pulse Generator
51
1.3 k
30 pF
Driver Enable Input

**FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$**

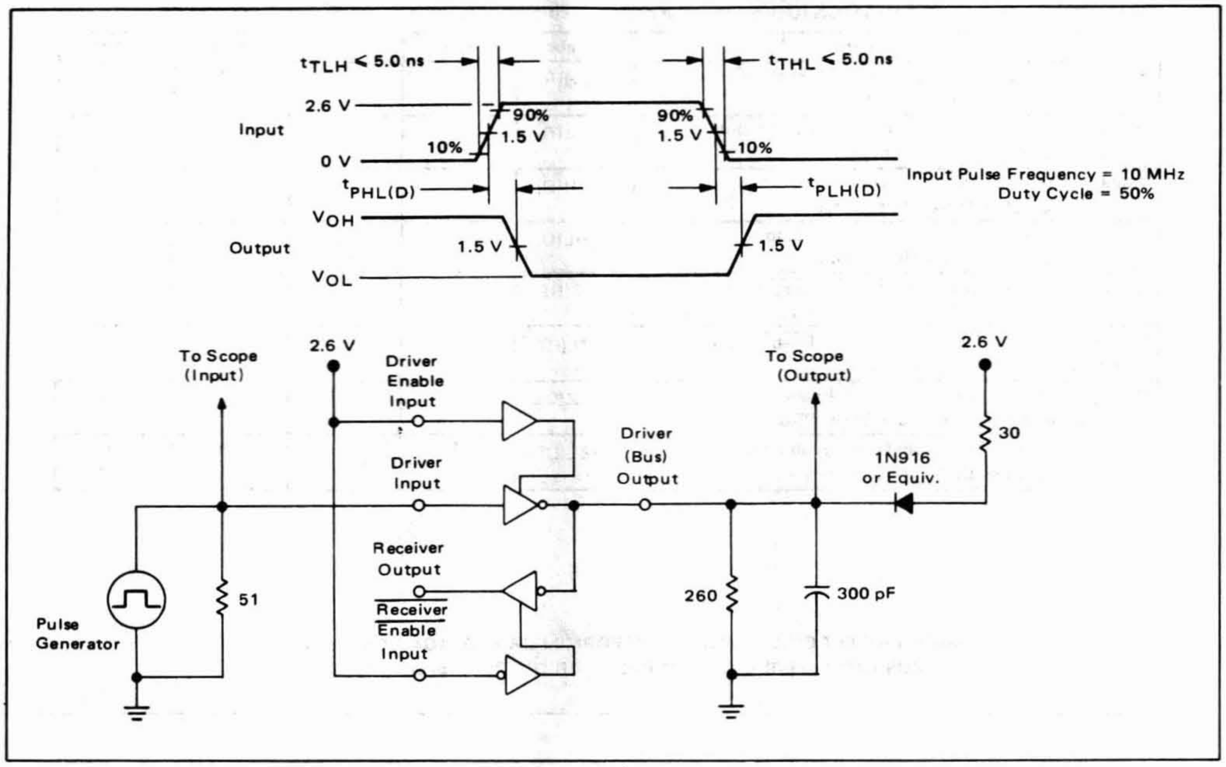

t_TLH ≤ 5.0 ns
t_THL ≤ 5.0 ns
2.6 V
Input
90%
1.5 V
10%
0 V
90%
1.5 V
10%
t_PHL(D)
t_PLH(D)
Input Pulse Frequency = 10 MHz
Duty Cycle = 50%
V_OH
Output
1.5 V
1.5 V
V_OL
To Scope (Input)
2.6 V
Driver Enable Input
Driver Input
Receiver Output
Receiver Enable Input
Pulse Generator
51
Driver (Bus) Output
To Scope (Output)
2.6 V
30
1N916 or Equiv.
260
300 pF

**FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$**

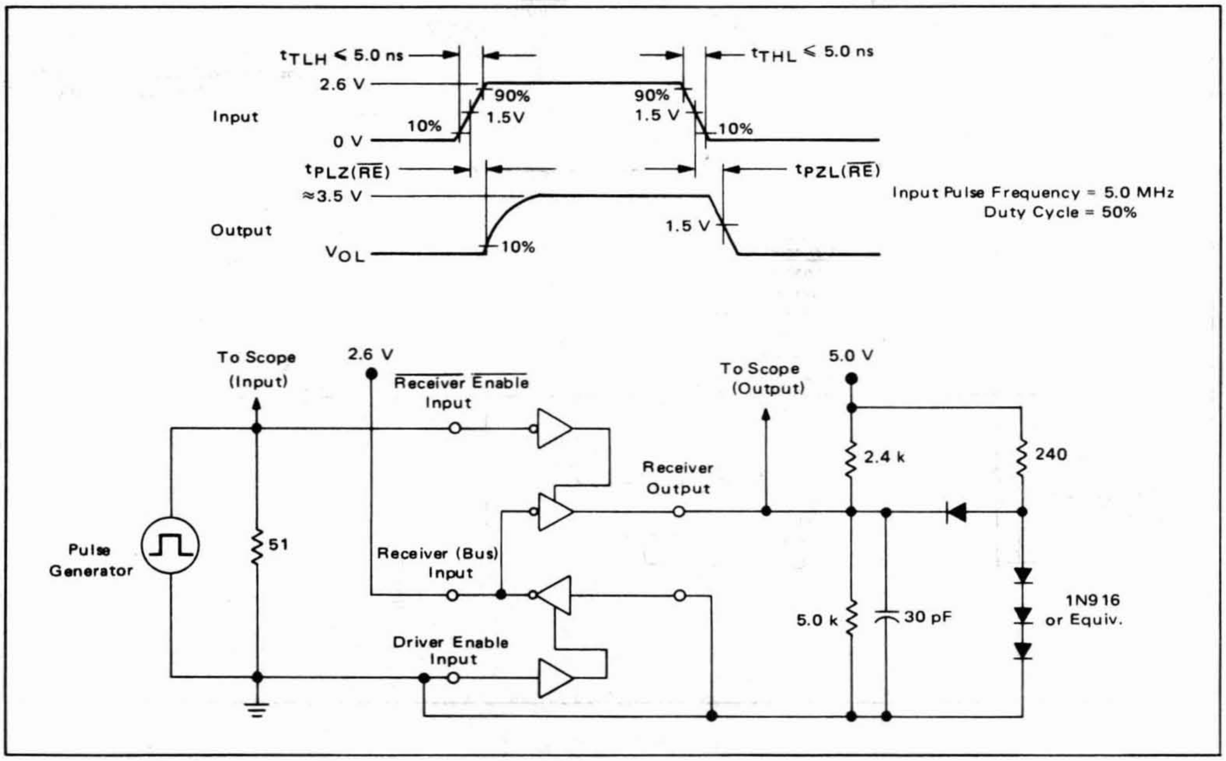

t_TLH ≤ 5.0 ns
t_THL ≤ 5.0 ns
2.6 V
Input
90%
1.5V
10%
0 V
90%
1.5 V
10%
t_PLZ(RE)
t_PZL(RE)
≈3.5 V
Output
1.5 V
V_OL
10%
Input Pulse Frequency = 5.0 MHz
Duty Cycle = 50%
To Scope (Input)
2.6 V
Receiver Enable Input
To Scope (Output)
5.0 V
2.4 k
240
Receiver Output
Pulse Generator
51
Receiver (Bus) Input
5.0 k
30 pF
1N916 or Equiv.
Driver Enable Input

FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PZL(DE)}$

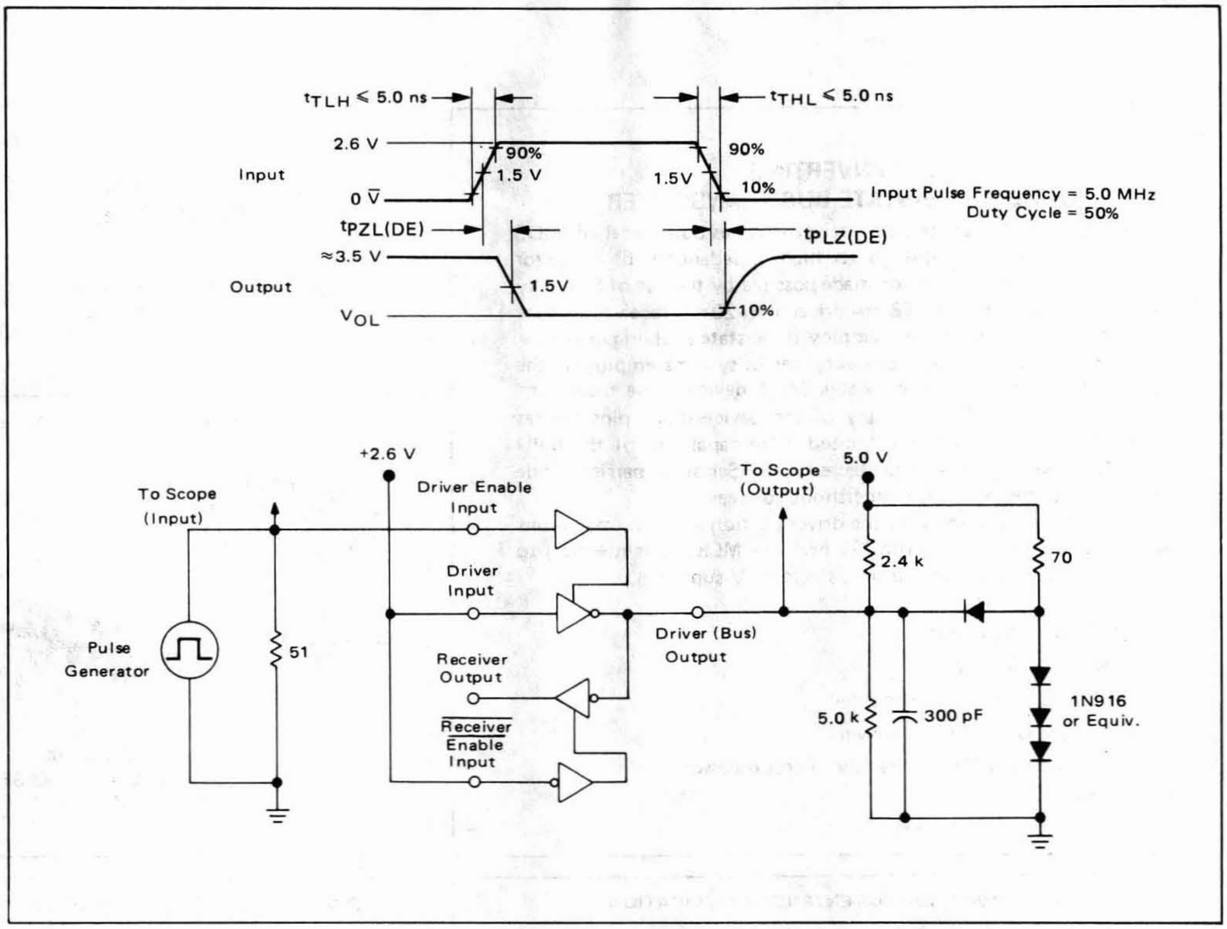
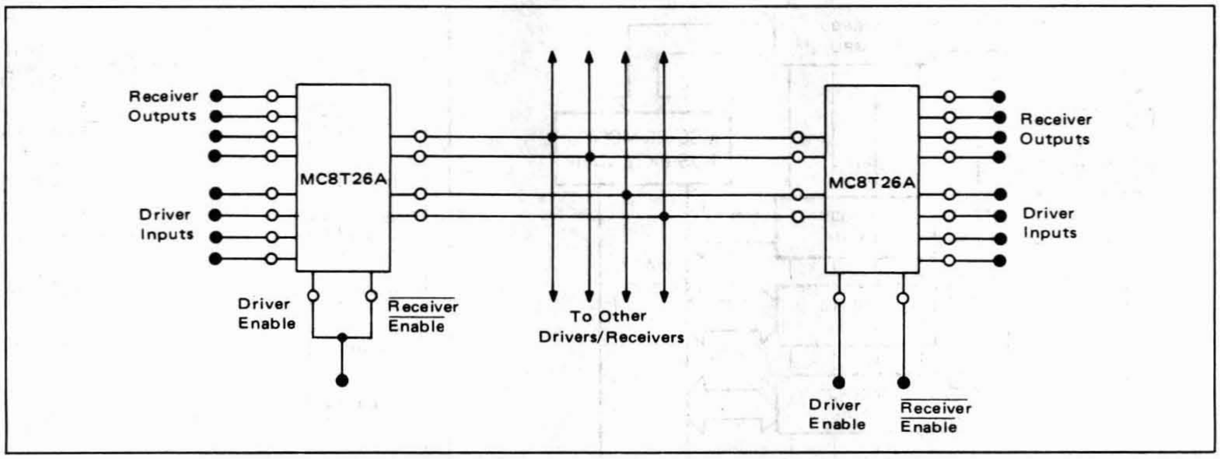

$t_{TLH} \leq 5.0$ ns
$t_{THL} \leq 5.0$ ns
2.6 V
90%
1.5 V
1.5V
90%
10%
Input
0 V
Input Pulse Frequency = 5.0 MHz
Duty Cycle = 50%
$t_{PZL(DE)}$
$t_{PLZ(DE)}$
≈3.5 V
Output
1.5V
$V_{OL}$
10%
+2.6 V
To Scope (Input)
Driver Enable Input
Driver Input
Pulse Generator
51
Receiver Output
Receiver Enable Input
Driver (Bus) Output
To Scope (Output)
5.0 V
2.4 k
70
5.0 k
300 pF
1N916 or Equiv.

FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS


Receiver Outputs
Driver Inputs
MC8T26A
Driver Enable
Receiver Enable
To Other Drivers/Receivers
MC8T26A
Receiver Outputs
Driver Inputs
Driver Enable
Receiver Enable

**MOTOROLA**

# MC8T28
# MC6889

## NONINVERTING BUS TRANSCEIVER

### MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS

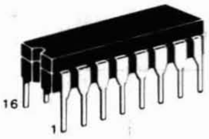
## NONINVERTING QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the -48 mA driver and -20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

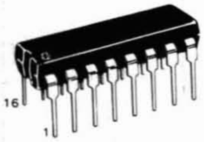
The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

Propagation delay times for the driver portion are 17 ns maximum while the receiver portion runs 17 ns. The MC8T28 is identical to the NE8T28 and it operates from a single +5 V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor
- Non-Inverting

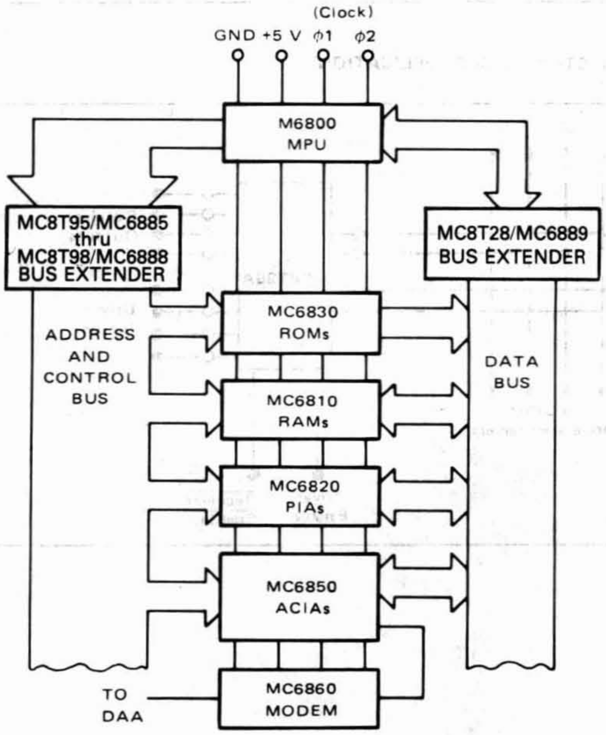


**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

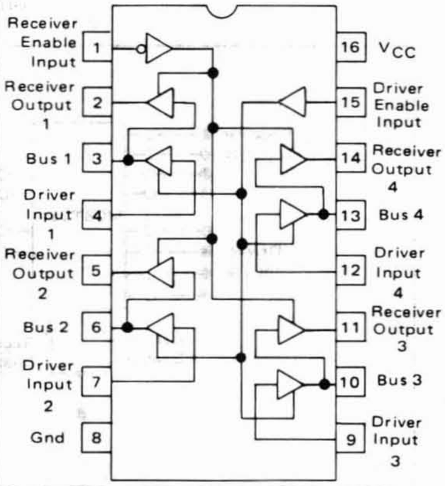


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

**MICROPROCESSOR BUS EXTENDER APPLICATION**


(Clock)
GND +5 V φ1 φ2
M6800 MPU
MC8T95/MC6885 thru MC8T98/MC6888 BUS EXTENDER
MC8T28/MC6889 BUS EXTENDER
ADDRESS AND CONTROL BUS
MC6830 ROMs
DATA BUS
MC6810 RAMs
MC6820 PIAs
MC6850 ACIAs
MC6860 MODEM
TO DAA

**PIN CONNECTIONS — MC8T28 MC6889**


Receiver Enable Input 1
Receiver Output 1 2
Bus 1 3
Driver Input 1 4
Receiver Output 2 5
Bus 2 6
Driver Input 2 7
Gnd 8
16 VCC
15 Driver Enable Input
14 Receiver Output 4
13 Bus 4
12 Driver Input 4
11 Receiver Output 3
10 Bus 3
9 Driver Input 3

**ORDERING INFORMATION**

| Device | Alternate | Temperature Range | Package |
|---|---|---|---|
| MC8T28L | MC6889L | 0 to +75°C | Ceramic DIP |
| MC8T28P | MC6889P | 0 to +75°C | Plastic DIP |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 8.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Junction Temperature | $T_J$ | | °C |
| Ceramic Package | | 175 | |
| Plastic Package | | 150 | |
| Operating Ambient Temperature Range | $T_A$ | 0 to +75 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** (4.75 V ≤ $V_{CC}$ ≤ 5.25 V and 0°C ≤ $T_A$ ≤ 75°C unless otherwise noted.)

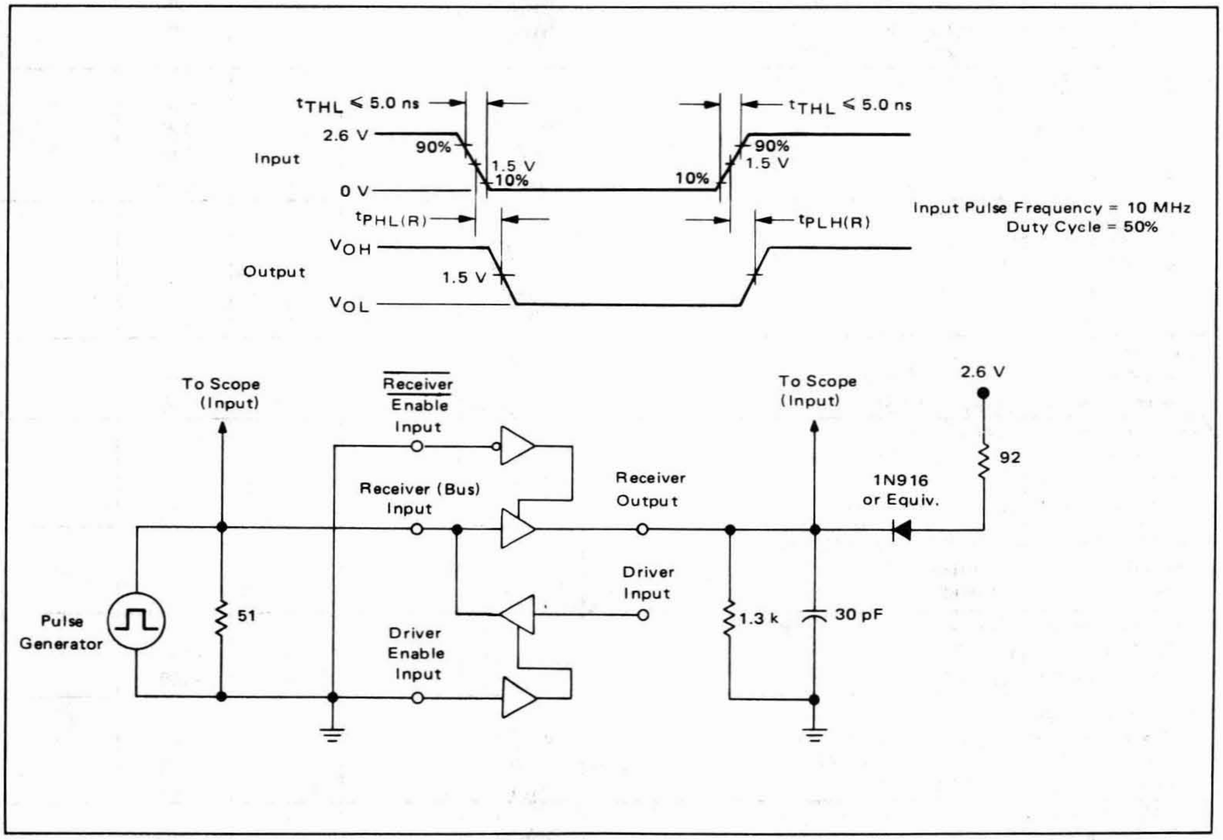
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Current – Low Logic State | | | | | |
| (Receiver Enable Input, $V_{IL(\overline{RE})}$ = 0.4 V) | $I_{IL(\overline{RE})}$ | – | – | -200 | μA |
| (Driver Enable Input, $V_{IL(DE)}$ = 0.4 V) | $I_{IL(DE)}$ | – | – | -200 | |
| (Driver Input, $V_{IL(D)}$ = 0.4 V) | $I_{IL(D)}$ | – | – | -200 | |
| (Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V) | $I_{IL(B)}$ | – | -- | -200 | |
| Input Disabled Current – Low Logic State | $I_{IL(D)\,DIS}$ | | | | |
| (Driver Input, $V_{IL(D)}$ = 0.4 V) | | – | – | -25 | μA |
| Input Current-High Logic State | | | | | |
| (Receiver Enable Input, $V_{IH(\overline{RE})}$ = 5.25 V) | $I_{IH(\overline{RE})}$ | – | – | 25 | μA |
| (Driver Enable Input, $V_{IH(DE)}$ = 5.25 V) | $I_{IH(DE)}$ | – | – | 25 | |
| (Driver Input, $V_{IH(D)}$ = 5.25 V) | $I_{IH(D)}$ | – | – | 25 | |
| Input Voltage – Low Logic State | | | | | |
| (Receiver Enable Input) | $V_{IL(\overline{RE})}$ | – | – | 0.85 | V |
| (Driver Enable Input | $V_{IL(DE)}$ | – | – | 0.85 | |
| (Driver Input) | $V_{IL(D)}$ | – | – | 0.85 | |
| (Receiver Input) | $V_{IL(B)}$ | – | – | 0.85 | |
| Input Voltage – High Logic State | | | | | |
| (Receiver Enable Input) | $V_{IH(\overline{RE})}$ | 2.0 | – | – | V |
| (Driver Enable Input) | $V_{IH(DE)}$ | 2.0 | – | – | |
| (Driver Input) | $V_{IH(D)}$ | 2.0 | – | – | |
| (Receiver Input) | $V_{IH(B)}$ | 2.0 | – | – | |
| Output Voltage – Low Logic State | | | | | |
| (Bus Driver) Output, $I_{OL(B)}$ = 48 mA) | $V_{OL(B)}$ | – | – | 0.5 | V |
| (Receiver Output, $I_{OL(R)}$ = 20 mA) | $V_{OL(R)}$ | – | – | 0.5 | |
| Output Voltage – High Logic State | | | | | |
| (Bus (Driver) Output, $I_{OH(B)}$ = −10 mA) | $V_{OH(B)}$ | 2.4 | 3.1 | – | V |
| (Receiver Output, $I_{OH(R)}$ = −2.0 mA) | $V_{OH(R)}$ | 2.4 | 3.1 | – | |
| (Receiver Output, $I_{OH(R)}$ = −100/μA, $V_{CC}$ = 5.0 V) | | 3.5 | – | – | |
| Output Disabled Leakage Current – High Logic State | | | | | |
| (Bus Driver) Output, $V_{OH(B)}$ = 2.4 V) | $I_{OHL(B)}$ | – | – | 100 | μA |
| (Receiver Output, $V_{OH(R)}$ = 2.4 V) | $I_{OHL(R)}$ | – | – | 100 | |
| Output Disabled Leakage Current – Low Logic State | | | | | |
| (Bus Output, $V_{OL(B)}$ = 0.5 V) | $I_{OLL(B)}$ | – | – | -100 | μA |
| (Receiver Output, $V_{OL(R)}$ = 0.5 V) | $I_{OLL(R)}$ | – | – | -100 | |
| Input Clamp Voltage | | | | | |
| (Driver Enable Input $I_{ID(DE)}$ = −12 mA) | $V_{IC(DE)}$ | – | – | -1.0 | V |
| (Receiver Enable Input $I_{IC(RE)}$ = +12 mA) | $V_{IC(RE)}$ | – | – | -1.0 | |
| (Driver Input $I_{IC(D)}$ = −12 mA) | $V_{IC(D)}$ | – | – | -1.0 | |
| Output Short-Circuit Current, $V_{CC}$ = 5.25 V (1) | | | | | |
| (Bus (Driver) Output) | $I_{OS(B)}$ | -50 | – | -150 | mA |
| (Receiver Output) | $I_{OS(R)}$ | -30 | – | -75 | |
| Power Supply Current ($V_{CC}$ = 5.25 V) | $I_{CC}$ | – | – | 110 | mA |

(1) Only one output may be short-circuited at a time.

**SWITCHING CHARACTERISTICS** (Unless otherwise noted, $V_{CC}$ = 5.0 V and $T_A$ = 25°C)

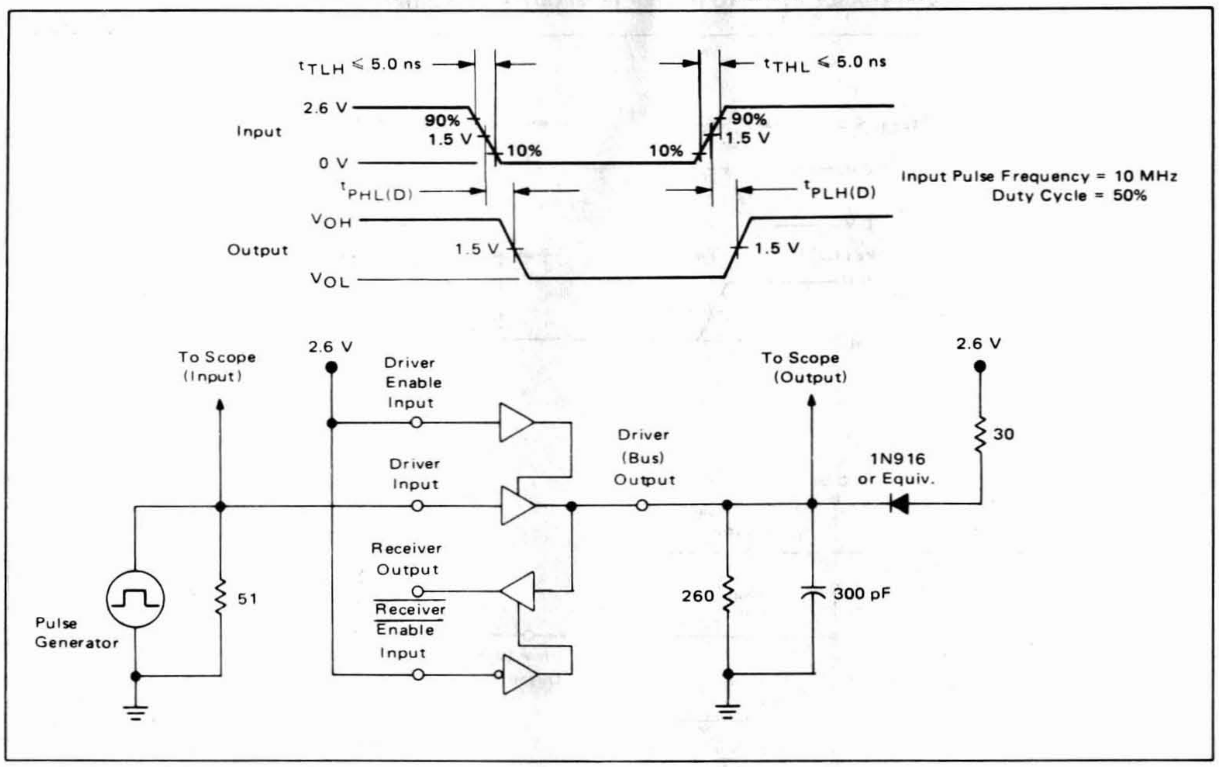
| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Propagation Delay Time—Receiver ($C_L$ = 30 pF) | $t_{PLH(R)}$<br>$t_{PHL(R)}$ | – | 17<br>17 | ns |
| Propagation Delay Time—Driver ($C_L$ = 300 pF) | $t_{PLH(D)}$<br>$t_{PHL(D)}$ | – | 17<br>17 | ns |
| Propagation Delay Time—Enable ($C_L$ = 30 pF)<br>– Receiver | $t_{PZL(R)}$<br>$t_{PLZ(R)}$ | –<br>– | 23<br>18 | ns |
| – Driver Enable ($C_L$ 300 pF) | $t_{PZL(D)}$<br>$t_{PLZ(D)}$ | –<br>– | 28<br>23 | |

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$ AND $t_{PHL(R)}$



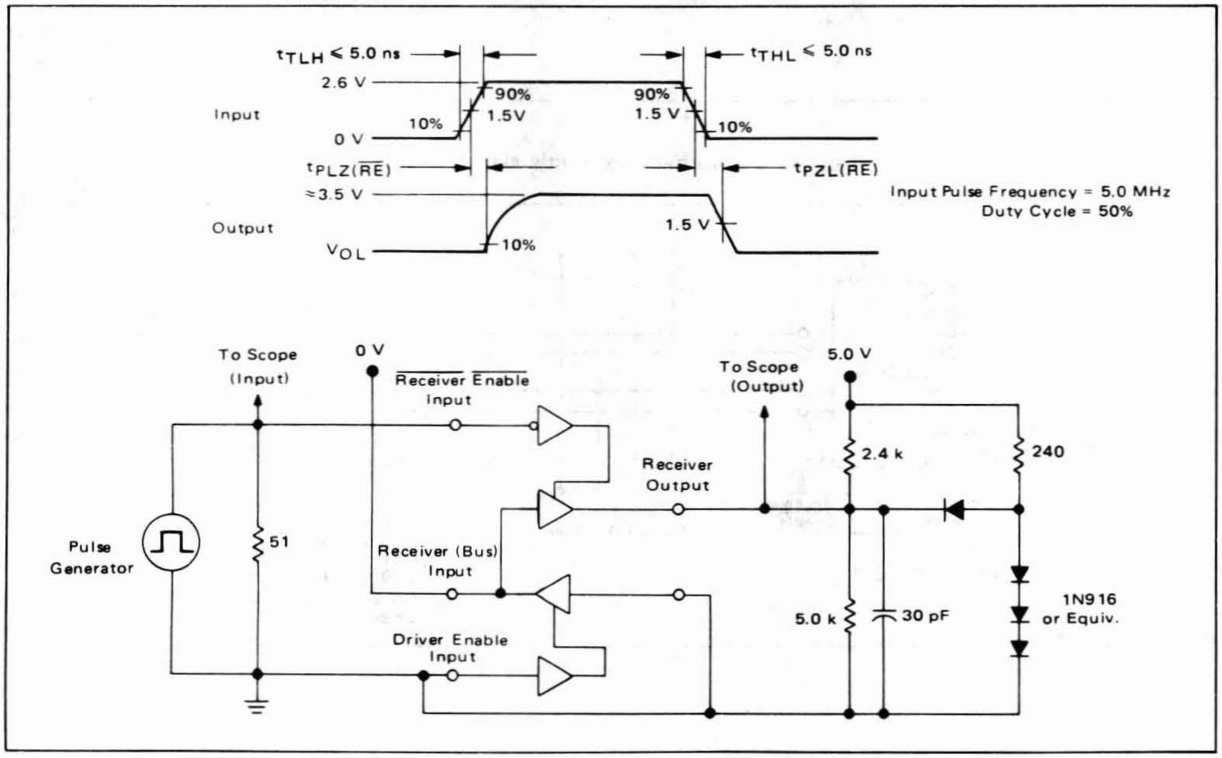
$t_{THL}$ ≤ 5.0 ns
$t_{THL}$ ≤ 5.0 ns
2.6 V
Input
0 V
90%
1.5 V
10%
10%
90%
1.5 V
$t_{PHL(R)}$
$t_{PLH(R)}$
Input Pulse Frequency = 10 MHz
Duty Cycle = 50%
$V_{OH}$
Output
1.5 V
$V_{OL}$
To Scope (Input)
Receiver Enable Input
To Scope (Input)
2.6 V
92
Receiver (Bus) Input
Receiver Output
1N916 or Equiv.
Driver Input
Pulse Generator
51
Driver Enable Input
1.3 k
30 pF

FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$



tTLH ≤ 5.0 ns
tTHL ≤ 5.0 ns
2.6 V
Input
90%
1.5 V
10%
10%
90%
1.5 V
0 V
tPHL(D)
tPLH(D)
Input Pulse Frequency = 10 MHz
Duty Cycle = 50%
VOH
Output
1.5 V
1.5 V
VOL
To Scope (Input)
2.6 V
Driver Enable Input
To Scope (Output)
2.6 V
Driver (Bus) Output
30
Driver Input
1N916 or Equiv.
Receiver Output
Receiver Enable Input
260
300 pF
51
Pulse Generator

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$



tTLH ≤ 5.0 ns
tTHL ≤ 5.0 ns
2.6 V
90%
90%
Input
10%
1.5V
1.5 V
10%
0 V
tPLZ(RE)
tPZL(RE)
≈3.5 V
Input Pulse Frequency = 5.0 MHz
Duty Cycle = 50%
Output
1.5 V
VOL
10%
To Scope (Input)
0 V
Receiver Enable Input
To Scope (Output)
5.0 V
2.4 k
240
Receiver Output
Pulse Generator
51
Receiver (Bus) Input
1N916 or Equiv.
5.0 k
30 pF
Driver Enable Input

**FIGURE 4 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PZL(DE)}$**

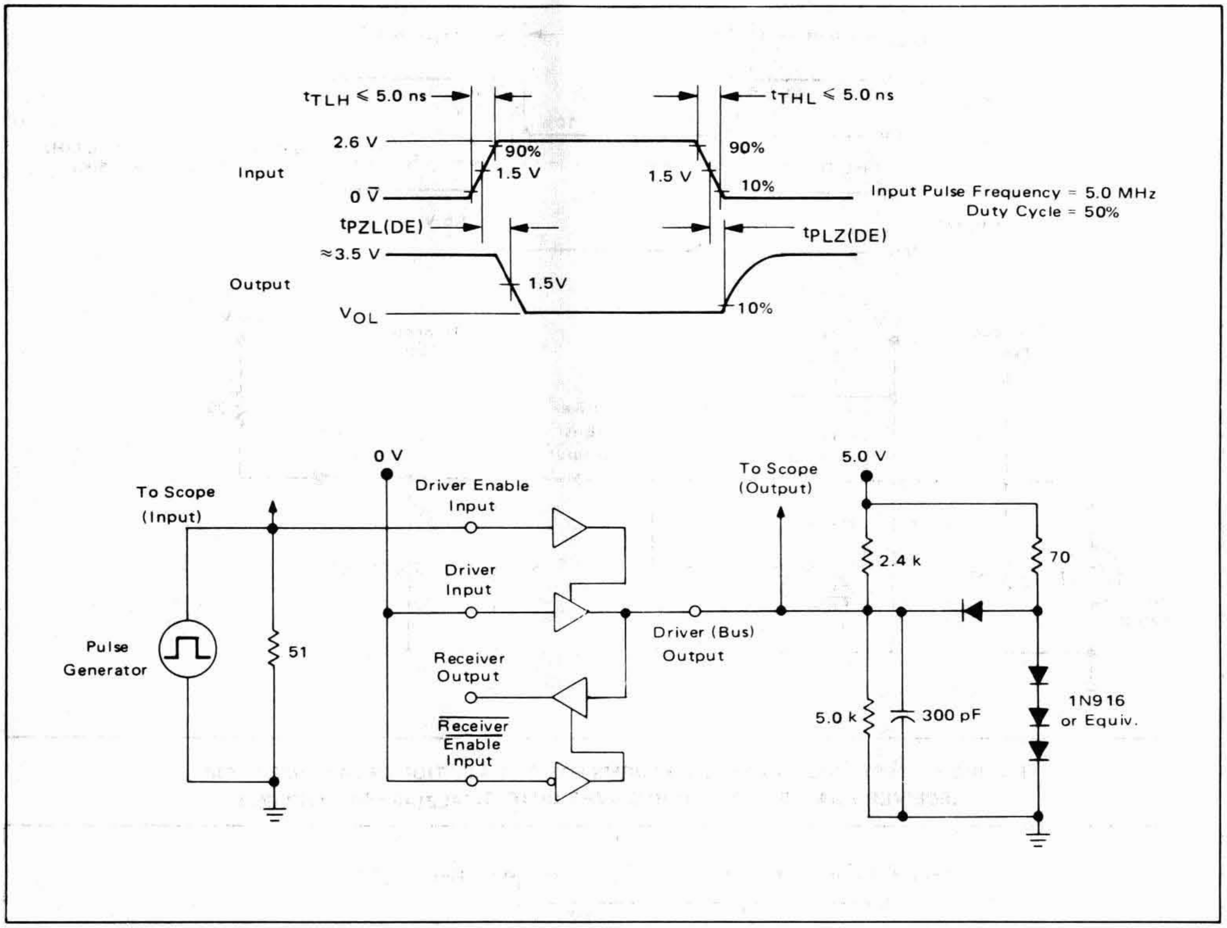
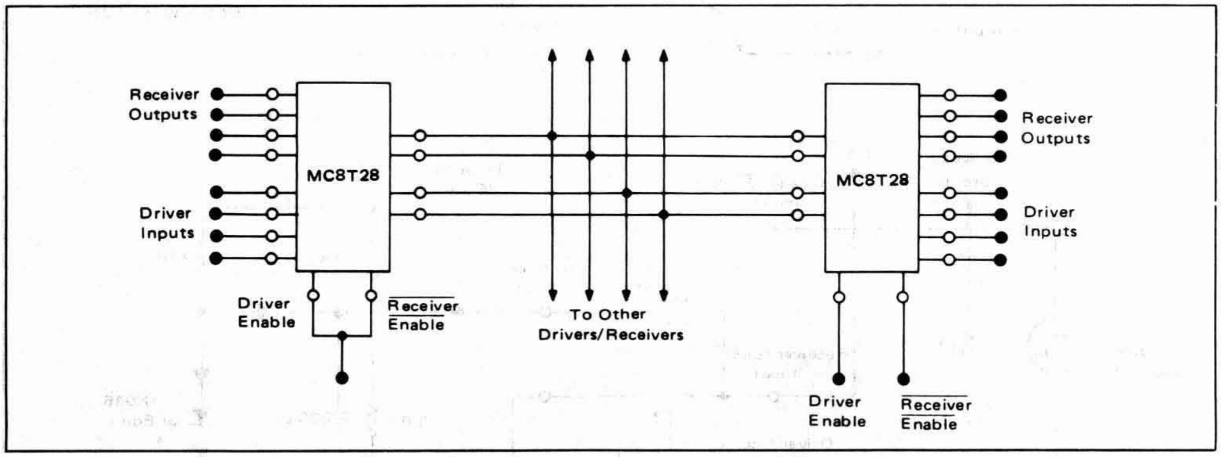

$t_{TLH} \leq 5.0$ ns
$t_{THL} \leq 5.0$ ns
2.6 V
90%
1.5 V
Input
0 V
1.5 V
90%
10%
Input Pulse Frequency = 5.0 MHz
Duty Cycle = 50%
$t_{PZL(DE)}$
$t_{PLZ(DE)}$
≈3.5 V
Output
1.5V
$V_{OL}$
10%
0 V
To Scope (Input)
Driver Enable Input
To Scope (Output)
5.0 V
Driver Input
2.4 k
70
Pulse Generator
51
Receiver Output
Driver (Bus) Output
Receiver Enable Input
5.0 k
300 pF
1N916 or Equiv.

**FIGURE 5 — BIDIRECTIONAL BUS APPLICATIONS**


Receiver Outputs
Driver Inputs
MC8T28
Driver Enable
Receiver Enable
To Other Drivers/Receivers
MC8T28
Receiver Outputs
Driver Inputs
Driver Enable
Receiver Enable

# MC26S10

## QUAD OPEN-COLLECTOR BUS TRANSCEIVER

This quad transceiver is designed to mate Schottky TTL or NMOS logic to a low impedance bus. The Enable and Driver inputs are PNP buffered to ensure low input loading. The Driver (Bus) output is open-collector and can sink up to 100 mA at 0.8 V, thus the bus can drive impedances as low as 100 Ω. The receiver output is active pull-up and can drive ten Schottky TTL loads.

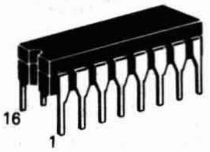
An active-low $\overline{\text{Enable}}$ controls all four drivers allowing the outputs of different device drivers to be connected together for party-line operation. The line can be terminated at both ends and still give considerable noise margin at the receiver. Typical receiver threshold is 2.0 V.

Advanced Schottky processing is utilized to assure fast propagation delay times. Two ground pins are provided to improve ground current handling and allow close decoupling between $V_{CC}$ and ground at the package. Both ground pins should be tied to the ground bus external to the package.

- Driver Can Sink 100 mA at 0.8 V (Max)
- PNP Inputs for Low-Logic Loading
- Typical Driver Delay = 10 ns
- Typical Receiver Delay = 10 ns
- Schottky Processing for High Speed
- Inverting Driver

## QUAD OPEN-COLLECTOR BUS TRANSCEIVER

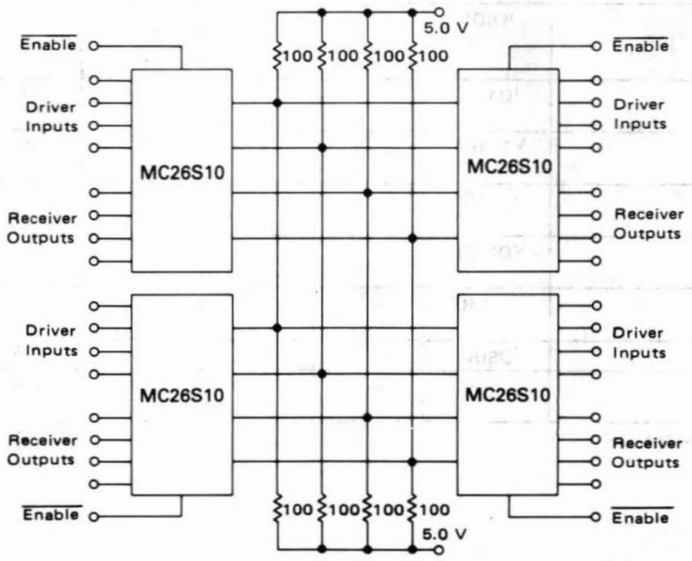
**SCHOTTKY SILICON MONOLITHIC INTEGRATED CIRCUIT**



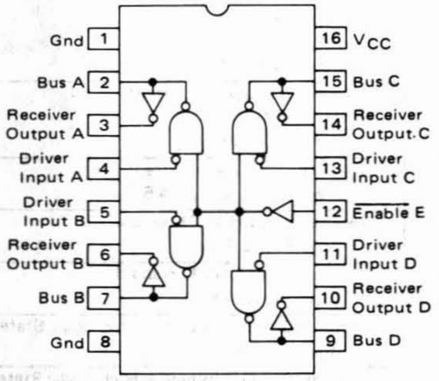
**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### TYPICAL APPLICATION


Enable
Driver Inputs
Receiver Outputs
MC26S10
5.0 V
100
100
100
100
Enable
Driver Inputs
Receiver Outputs
MC26S10
Driver Inputs
Receiver Outputs
MC26S10
Enable
MC26S10
Driver Inputs
Receiver Outputs
100
100
100
100
5.0 V
Enable

### PIN CONNECTIONS


Gnd 1
Bus A 2
Receiver Output A 3
Driver Input A 4
Driver Input B 5
Receiver Output B 6
Bus B 7
Gnd 8
16 VCC
15 Bus C
14 Receiver Output C
13 Driver Input C
12 Enable E
11 Driver Input D
10 Receiver Output D
9 Bus D

### TRUTH TABLE

| $\overline{\text{Enable}}$ | Driver Input | Bus | Receiver Output |
|---|---|---|---|
| L | L | H | L |
| L | H | L | H |
| H | X | Y | Y |

L = Low Logic State
H = High Logic State
X = Irrelevant
Y = Assumes condition controlled by other elements on the bus

## MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | -0.5 to +7.0 | Vdc |
| Input Voltage | $V_I$ | -0.5 to +5.5 | Vdc |
| Input Current | $I_I$ | -3.0 to +5.0 | mA |
| Output Voltage – High Impedance State | $V_{O\,(Hi\text{-}z)}$ | -0.5 to $V_{CC}$ | V |
| Output Current–Bus | $I_{o(B)}$ | 200 | mA |
| Output Current–Receiver | $I_{o(R)}$ | 30 | mA |
| Operating Ambient Temperature | $T_A$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | -65 to +150 | °C |
| Junction Temperature<br>Ceramic Package<br>Plastic Package | $T_J$ | <br>175<br>150 | °C |

## ELECTRICAL CHARACTERISTICS (Unless otherwise noted $V_{CC}$ = 4.75 to 5.25 V and $T_A$ = 0 to +70°C. Typical values measured at $V_{CC}$ = 5.0 V and $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage – Low Logic State<br>(Driver and $\overline{\text{Enable}}$ Inputs) | $V_{IL}$ | – | – | 0.8 | V |
| Input Voltage – High Logic State<br>(Driver and $\overline{\text{Enable}}$ Inputs) | $V_{IH}$ | 2.0 | – | – | V |
| Input Clamp Voltage<br>(Driver and Enable Inputs)<br>($I_{IK}$ = -18 mA) | $V_{IK}$ | – | – | -1.2 | V |
| Input Current – Low Logic State<br>($V_{IL}$ = 0.4 V)<br>($\overline{\text{Enable}}$ Input)<br>(Driver Inputs) | $I_{IL}$ | <br><br>–<br>– | <br><br>–<br>– | <br><br>-0.36<br>-0.54 | mA |
| Input Current – High Logic State ($V_{IH}$ = 2.7 V)<br>($\overline{\text{Enable}}$ Input)<br>(Driver Inputs) | $I_{IH}$ | <br>–<br>– | <br>–<br>– | <br>20<br>30 | µA |
| Input Current – Maximum Voltage<br>($V_{IH1}$ = 5.5 V)<br>($\overline{\text{Enable}}$ or Driver Inputs) | $I_{IH1}$ | – | – | 100 | µA |
| Driver Output Voltage – Low Logic State<br>($I_{OL}$ = 40 mA)<br>($I_{OL}$ = 70 mA)<br>($I_{OL}$ = 100 mA) | $V_{OL(D)}$ | <br>–<br>–<br>– | <br>0.33<br>0.42<br>0.51 | <br>0.5<br>0.7<br>0.8 | V |
| Driver (Bus) Leakage Current<br>($V_{OH}$ = 4.5 V)<br>($V_{OL}$ = 0.8 V) | $I_{O(D)}$ | <br>–<br>– | <br>–<br>– | <br>100<br>-50 | µA |
| Driver (Bus) Leakage Current<br>($V_{CC}$ = 0 V, $V_{OH}$ = 4.5 V) | $I_{O1(D)}$ | – | – | 100 | µA |
| Receiver Input High Threshold<br>($V_{IH(\overline{E})}$ = 2.4 V) | $V_{TH(R)}$ | 2.25 | 2.0 | – | V |
| Receiver Input Low Threshold<br>($V_{IH(\overline{E})}$ = 2.4 V) | $V_{TL(R)}$ | – | 2.0 | 1.75 | V |
| Receiver Output Voltage – Low Logic State<br>($I_{OL}$ = 20 mA) | $V_{OL(R)}$ | – | – | 0.5 | V |
| Receiver Output Voltage – High Logic State<br>($I_{OH}$ = -1.0 mA) | $V_{OH(R)}$ | 2.7 | 3.4 | – | V |
| Receiver Output Short-Circuit Current (Note 1) | $I_{OS(R)}$ | -18 | – | -60 | mA |
| Power Supply Current – Output Low State<br>($V_{IL(\overline{E})}$ = 0 V) | $I_{CC}$ | – | 45 | 70 | mA |

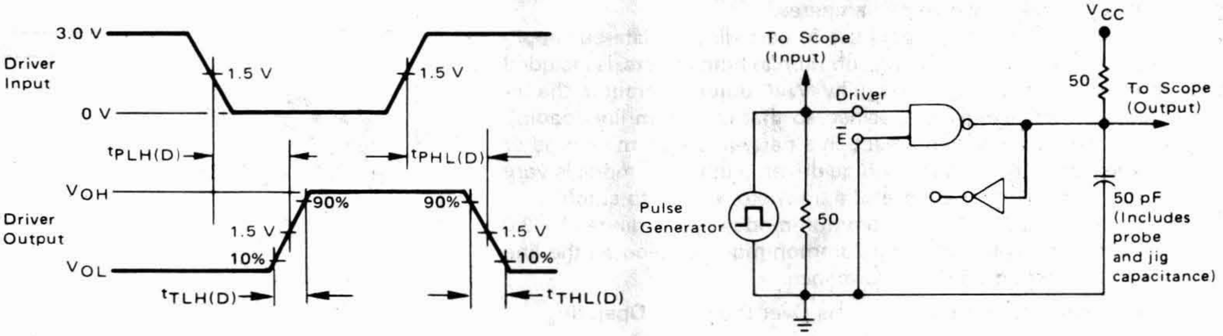
NOTE 1: One output shorted at a time. Duration not to exceed 1.0 second.

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $T_A$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Time Driver Input to Output | $t_{PLH(D)}$<br>$t_{PHL(D)}$ | —<br>— | 10<br>10 | 15<br>15 | ns |
| Propagation Delay Time $\overline{\text{Enable}}$ Input to Output | $t_{PLH(\overline{E})}$<br>$t_{PHL(\overline{E})}$ | —<br>— | 14<br>13 | 18<br>18 | ns |
| Propagation Delay Time Bus to Receiver Output | $t_{PLH(R)}$<br>$t_{PHL(R)}$ | —<br>— | 10<br>10 | 15<br>15 | ns |
| Rise and Fall Time of Driver Output | $t_{TLH(D)}$<br>$t_{THL(D)}$ | 4.0<br>2.0 | 10<br>4.0 | —<br>— | ns |

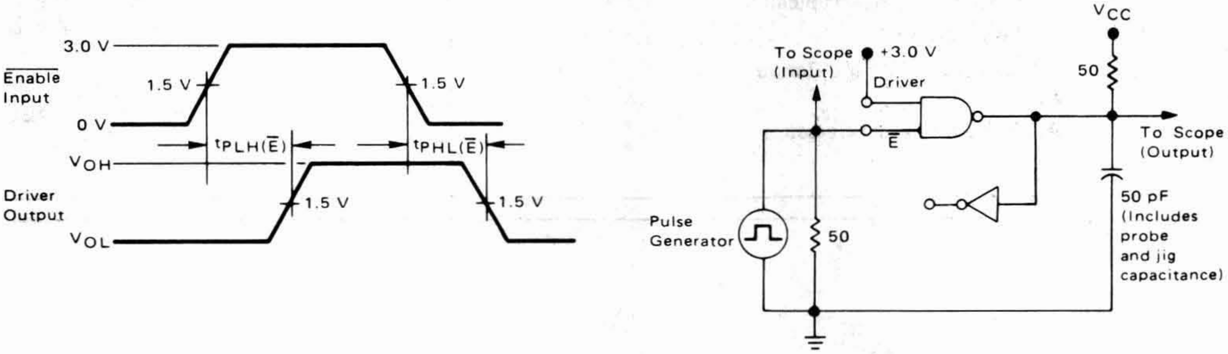
## SWITCHING WAVEFORMS AND CIRCUITS

FIGURE 1 — DATA INPUT TO BUS OUTPUT (DRIVER)



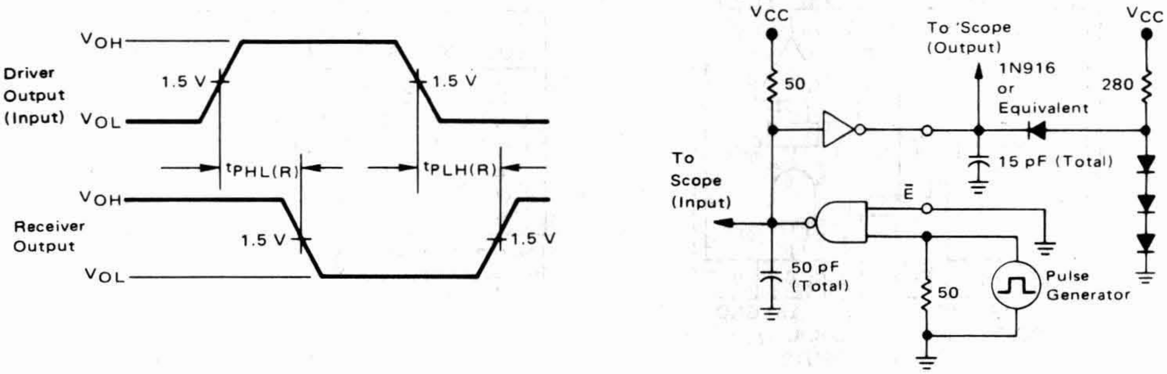
3.0 V
Driver Input
1.5 V
1.5 V
0 V
$t_{PLH(D)}$
$t_{PHL(D)}$
$V_{OH}$
Driver Output
90%
90%
1.5 V
1.5 V
10%
10%
$V_{OL}$
$t_{TLH(D)}$
$t_{THL(D)}$
To Scope (Input)
Driver
$\overline{E}$
Pulse Generator
50
$V_{CC}$
50
To Scope (Output)
50 pF (Includes probe and jig capacitance)

FIGURE 2 — ENABLE INPUT TO BUS OUTPUT (DRIVER)



3.0 V
$\overline{\text{Enable}}$ Input
1.5 V
1.5 V
0 V
$t_{PLH(\overline{E})}$
$t_{PHL(\overline{E})}$
$V_{OH}$
Driver Output
1.5 V
1.5 V
$V_{OL}$
To Scope (Input)
+3.0 V
Driver
$\overline{E}$
Pulse Generator
50
$V_{CC}$
50
To Scope (Output)
50 pF (Includes probe and jig capacitance)

FIGURE 3 — BUS INPUT TO RECEIVER OUTPUT



$V_{OH}$
Driver Output (Input)
$V_{OL}$
1.5 V
1.5 V
$t_{PHL(R)}$
$t_{PLH(R)}$
$V_{OH}$
Receiver Output
1.5 V
1.5 V
$V_{OL}$
$V_{CC}$
50
To Scope (Input)
50 pF (Total)
To 'Scope (Output)
1N916 or Equivalent
15 pF (Total)
$\overline{E}$
50
Pulse Generator
$V_{CC}$
280

**MOTOROLA**

# MC75S110

## MONOLITHIC DUAL LINE DRIVER

The MC75S110 dual line driver features independent channels with common voltage supply and ground terminals. Each driver circuit provides a constant output current that switches to either of two output terminals subject to the appropriate logic levels at the input terminals. Output current can be switched "off" (inhibited) by appropriate logic levels at the inhibit inputs. Output current is nominally twelve milliamperes.

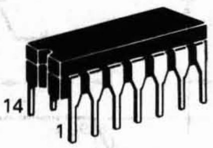
The inhibit feature permits use in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included to increase driver-logic versatility. With output current in the inhibited mode, $I_{O(off)}$ is specified so that minimum line loading occurs when the driver is used in a party-line system with other drivers. Output impedance of the driver in inhibited mode is very high (the output impedance of a transistor biased to cutoff).

All driver outputs have a common-mode voltage range of −3.0 volts to +3.0 volts, allowing common-mode voltage on the line without affecting driver performance.

- Insensitive to Supply Variations Over the Entire Operating Range
- MTTL Input Compatibility
- Current-Mode Output (12 mA Typical)
- High Output Impedance
- Common-Mode Output Voltage Range (−3.0 V to +3.0 V)
- Inhibitor Available for Driver Selection

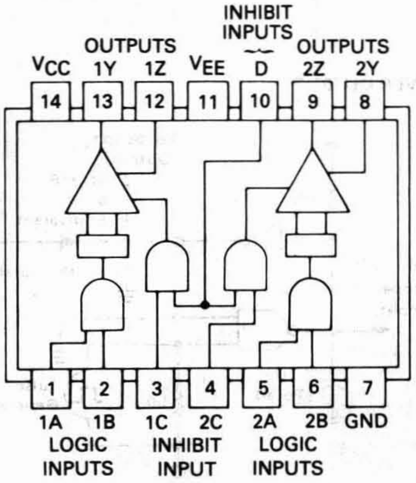
## DUAL LINE DRIVERS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA
(TO-116)

**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05



**TRUTH TABLE**

| LOGIC INPUTS | | INHIBITOR INPUTS | | OUTPUTS | |
|---|---|---|---|---|---|
| A | B | C | D | Y | Z |
| L or H | L or H | L | L or H | H | H |
| L or H | L or H | L or H | L | H | H |
| L | L or H | H | H | L | H |
| L or H | L | H | H | L | H |
| H | H | H | H | H | L |

Low output represents the "on" state.
High output represents the "off" state.

**MAXIMUM RATINGS** ($T_A$ = 0 to +70°C unless otherwise noted.)

| Ratings | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltages<br>(See Note 1) | $V_{CC}$<br>$V_{EE}$ | +7.0<br>−7.0 | Volts |
| Logic and Inhibitor Input Voltages<br>(See Note 1) | $V_{in}$ | 5.5 | Volts |
| Common-Mode Output Voltage Range<br>(See Note 1) | $V_{OCR}$ | −5.0 to +7.0 | Volts |
| Power Dissipation (Package Limitation)<br>Plastic and Ceramic Dual In-Line Packages<br>Derate above $T_A$ = +25°C | $P_D$ | <br>1000<br>3.85 | <br>mW<br>mW/°C |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

NOTE 1. These voltage values are with respect to the ground terminal.

**RECOMMENDED OPERATING CONDITIONS** (See Notes 1 and 2.)

| Characteristic | Symbol | Min | Nom | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltages | $V_{CC}$<br>$V_{EE}$ | +4.75<br>−4.75 | +5.0<br>−5.0 | +5.25<br>−5.25 | Volts |
| Common-Mode Output Voltage Range | $V_{OCR}$ | −3.0 | — | +3.0 | Volts |

NOTE 2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

**DEFINITIONS OF INPUT LOGIC LEVELS***

| Characteristic | Symbol | Test Figure | Min | Max | Unit |
|---|---|---|---|---|---|
| High-Level Input Voltage (at any input) | $V_{IH}$ | 1,2 | 2.0 | 5.25 | Volts |
| Low-Level Input Voltage (at any input) | $V_{IL}$ | 1,2 | 0 | 0.8 | Volts |

* The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

## THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\ (Typ)}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

$T_A$ = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}$ (Typ) = Typical Thermal Resistance Junction to Ambient

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0 to +70°C unless otherwise noted.)

| Characteristic** | Symbol | Test Figure | Min | Typ* | Max | Unit |
|---|---|---|---|---|---|---|
| High-Level Input Current to 1A, 1B, 2A or 2B | $I_{IH_L}$ | 1 | | | | |
| ($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH_L}$ = 2.4 V)* | | | — | — | 40 | μA |
| ($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH_L}$ = $V_{CC}$ Max) | | | — | — | 1.0 | mA |
| Low-Level Input Current to 1A, 1B, 2A or 2B<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IL_L}$ = 0.4 V) | $I_{IL_L}$ | 1 | — | — | −3.0 | mA |
| High-Level Input Current into 1C or 2C | $I_{IH_I}$ | 1 | | | | |
| ($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH_I}$ = 2.4 V) | | | — | — | 40 | μA |
| ($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH_I}$ = $V_{CC}$ Max) | | | — | — | 1.0 | mA |
| Low-Level Input Current into 1C or 2C<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IL_I}$ = 0.4 V) | $I_{IL_I}$ | 1 | — | — | −3.0 | mA |
| High-Level Input Current into D | $I_{IH_I}$ | 1 | | | | |
| ($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH_I}$ = 2.4 V) | | | — | — | 80 | μA |
| ($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH_I}$ = $V_{CC}$ Max) | | | — | — | 2.0 | mA |
| Low-Level Input Current into D<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IL_I}$ = 0.4 V) | $I_{IL_I}$ | 1 | — | — | −6.0 | mA |
| Output Current ("on" state) | $I_{O(on)}$ | 2 | | | | mA |
| ($V_{CC}$ = Max, $V_{EE}$ = Max) | | | — | 12 | 15 | |
| ($V_{CC}$ = Min, $V_{EE}$ = Min) | | | 6.5 | — | — | |
| Output Current ("off" state) | $I_{O(off)}$ | 2 | | | | μA |
| ($V_{CC}$ = Max, $V_{EE}$ = Max) | | | — | — | 100 | |
| ($V_{CC}$ = Min, $V_{EE}$ = Min) | | | — | — | 100 | |
| Supply Current from $V_{CC}$ (with driver enabled)<br>($V_{IL_L}$ = 0.4 V, $V_{IH_I}$ = 2.0 V) | $I_{CC(on)}$ | 3 | — | — | 35 | mA |
| Supply Current from $V_{EE}$ (with driver enabled)<br>($V_{IL_L}$ = 0.4 V, $V_{IH_I}$ = 2.0 V) | $I_{EE(on)}$ | 3 | — | — | −50 | mA |
| Supply Current from $V_{CC}$ (with driver inhibited)<br>($V_{IL_L}$ = 0.4 V, $V_{IL_I}$ = 0.4 V) | $I_{CC(off)}$ | 3 | — | — | 35 | mA |
| Supply Current from $V_{EE}$ (with driver inhibited)<br>($V_{IL_L}$ = 0.4 V, $V_{IL_I}$ = 0.4 V) | $I_{EE(off)}$ | 3 | — | — | −50 | mA |

*All typical values are at $V_{CC}$ = +5.0 V, $V_{EE}$ = −5.0 V.

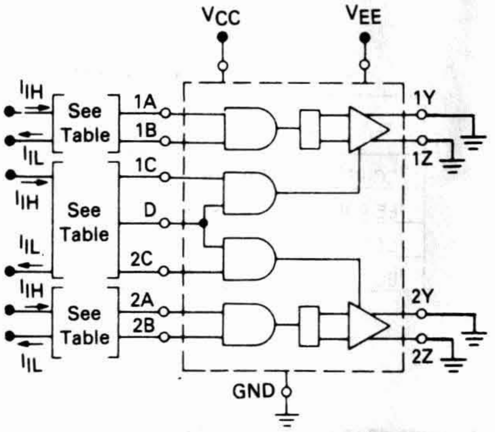
**For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = +5.0 V, $V_{EE}$ = −5.0 V, $T_A$ = +25°C.)

| Characteristic | Symbol | Test Figure | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation Delay Time from Logic Input A or B to Output Y or Z ($R_L$ = 50 ohms, $C_L$ = 40 pF) | $t_{PLH_L}$<br>$t_{PHL_L}$ | 4 | —<br>— | 9.0<br>9.0 | 15<br>15 | ns |
| Propagation Delay Time from Inhibitor Input C or D to Output Y or Z ($R_L$ = 50 ohms, $C_L$ = 40 pF) | $t_{PLH_I}$<br>$t_{PHL_I}$ | 4 | —<br>— | 16<br>13 | 25<br>25 | ns |

## TEST CIRCUITS

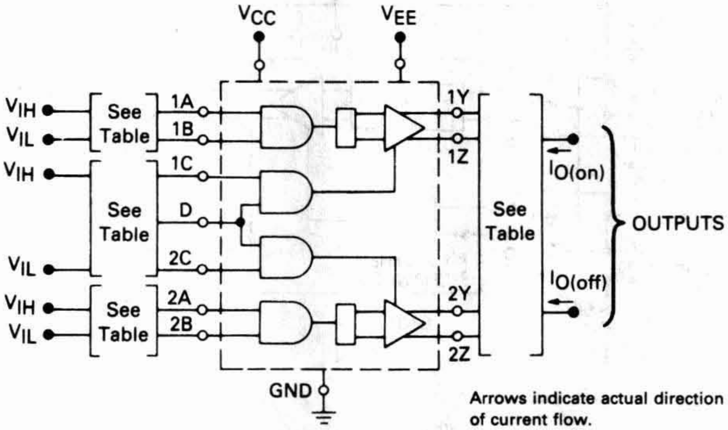
### FIGURE 1 — $I_{IH}$, $I_{IL}$


VCC
VEE
IIH
IIL
See Table
1A
1B
1C
D
2C
2A
2B
1Y
1Z
2Y
2Z
GND

**TEST TABLE**

| TEST AT ANY INPUT | ADJACENT INPUTS NOT UNDER TEST |
|---|---|
| $I_{IH}$ | GND |
| $I_{IL}$ | 4.5 V |

### FIGURE 2 — $I_{O(on)}$ and $I_{O(off)}$


VCC
VEE
VIH
VIL
See Table
1A
1B
1C
D
2C
2A
2B
1Y
1Z
2Y
2Z
IO(on)
IO(off)
OUTPUTS
GND

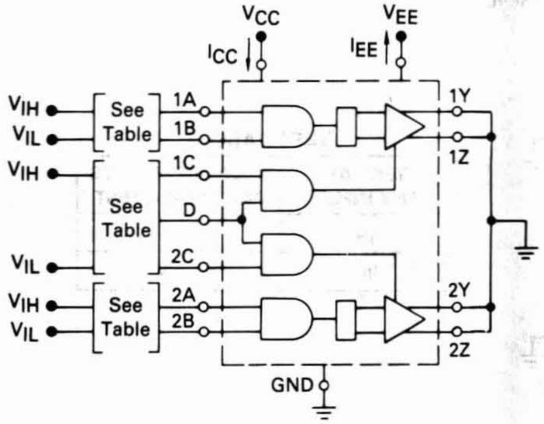
Arrows indicate actual direction of current flow.

**TEST TABLE**

| TEST<br>Ground all output pins not under test. | | LOGIC INPUTS | | INHIBITOR INPUTS | |
|---|---|---|---|---|---|
| | | 1A or 2A | 1B or 2B | 1C or 2C | D |
| $I_{O(on)}$ | at output 1Y or 2Y | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ |
| | | $V_{IL}$ | $V_{IH}$ | | |
| | | $V_{IH}$ | $V_{IL}$ | | |
| $I_{O(on)}$ | at output 1Z or 2Z | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ |
| $I_{O(off)}$ | at output 1Y or 2Y | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ |
| $I_{O(off)}$ | at output 1Z or 2Z | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ |
| | | $V_{IL}$ | $V_{IH}$ | | |
| | | $V_{IH}$ | $V_{IL}$ | | |
| $I_{O(off)}$ | at output 1Y, 2Y, 1Z, or 2Z | Either state | Either state | $V_{IL}$ | $V_{IL}$ |
| | | | | $V_{IL}$ | $V_{IH}$ |
| | | | | $V_{IH}$ | $V_{IL}$ |

## TEST CIRCUITS (continued)

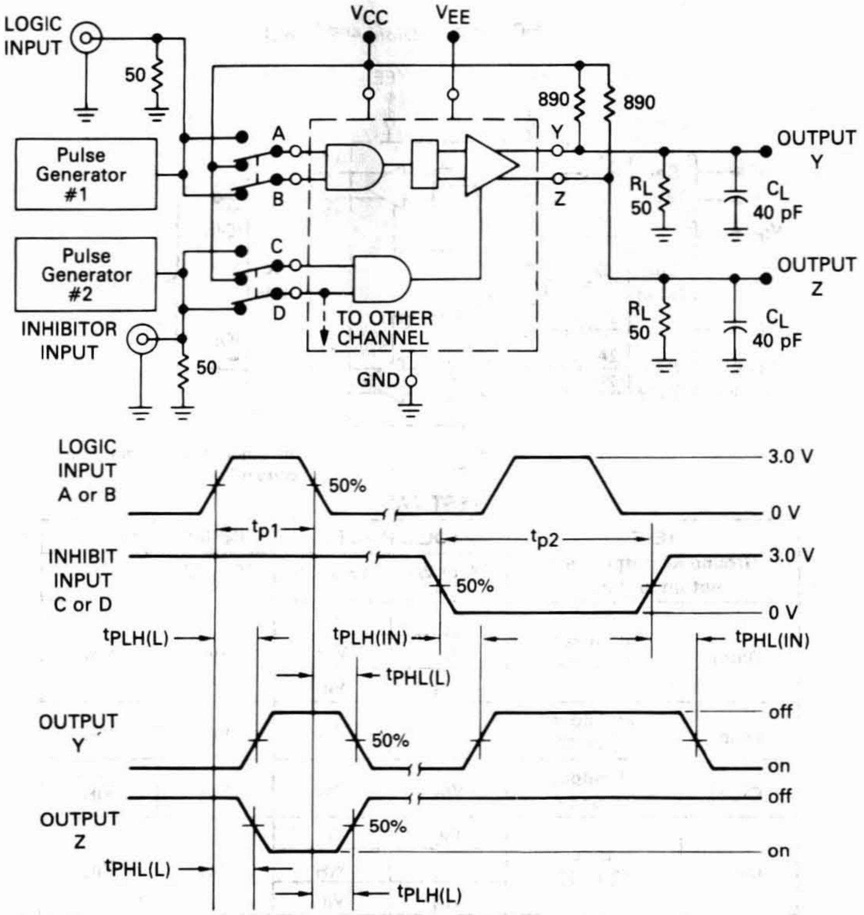
### FIGURE 3 — $I_{CC}$ and $I_{EE}$


VCC
VEE
ICC
IEE
VIH
VIL
See Table
1A
1B
1Y
1Z
VIH
1C
See Table
D
2C
VIL
VIH
VIL
See Table
2A
2B
2Y
2Z
GND

**TEST TABLE**

| TEST | | ALL LOGIC INPUTS | ALL INHIBITOR INPUTS |
|---|---|---|---|
| $I_{CC}$(on) | Driver enabled | $V_{IL}$ | $V_{IH}$ |
| $I_{EE}$(on) | Driver enabled | $V_{IL}$ | $V_{IH}$ |
| $I_{CC}$(off) | Driver inhibited | $V_{IL}$ | $V_{IL}$ |
| $I_{EE}$(off) | Driver inhibited | $V_{IL}$ | $V_{IL}$ |

### FIGURE 4 — PROPAGATION DELAY TIMES TEST CIRCUIT AND WAVEFORMS


LOGIC INPUT
50
VCC
VEE
890
890
Pulse Generator #1
A
B
Y
Z
OUTPUT Y
RL 50
CL 40 pF
Pulse Generator #2
C
D
TO OTHER CHANNEL
OUTPUT Z
RL 50
CL 40 pF
INHIBITOR INPUT
50
GND
LOGIC INPUT A or B
50%
3.0 V
0 V
tp1
tp2
INHIBIT INPUT C or D
3.0 V
50%
0 V
tPLH(L)
tPLH(IN)
tPHL(IN)
tPHL(L)
OUTPUT Y
50%
off
on
off
OUTPUT Z
50%
on
tPHL(L)
tPLH(L)

NOTES: 1. The pulse generators have the following characteristics: $z_o = 50\ \Omega$, $t_r = t_f = 10 \pm 5.0$ ns $t_{p1} = 500$ ns, PRR = 1.0 MHz, $t_{p2} = 1.0$ ms, PRR = 500 kHz.

2. $C_L$ includes probe and jig capacitance.

3. For simplicity, only one channel and the inhibitor connections are shown.

**MOTOROLA**

# MC1411 (ULN2001A)
# MC1412 (ULN2002A)
# MC1413 (ULN2003A)
# MC1416 (ULN2004A)

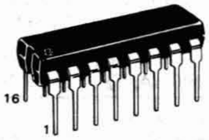
## HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The seven NPN Darlington-connected transistors in these arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 600 mA permit them to drive incandescent lamps.

The MC1411 device is a general-purpose array for use with DTL, TTL, PMOS, or CMOS Logic. The MC1412 contains a zener diode and resistor in series with the input to limit input current for use with 14 to 25 Volt PMOS Logic. The MC1413 with a 2.7 kΩ series input resistor is well suited for systems utilizing 5 Volt TTL or CMOS Logic. The MC1416 uses a series 10.5 kΩ resistor and is useful in 8–18 Volt MOS systems.

## PERIPHERAL DRIVER ARRAYS

### SILICON MONOLITHIC INTEGRATED CIRCUITS



**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

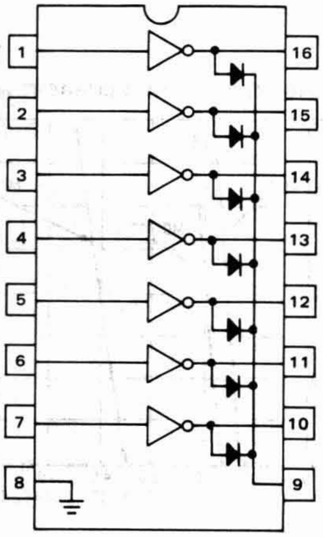
**MAXIMUM RATINGS** ($T_A$ = 25°C and rating apply to any one device in the package unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Output Voltage | $V_O$ | 50* | V |
| Input Voltage (Except MC1411) | $V_I$ | 30 | V |
| Collector Current – Continuous | $I_C$ | 500 | mA |
| Base Current – Continuous | $I_B$ | 25 | mA |
| Operating Ambient Temperature Range | $T_A$ | 0 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Junction Temperature | $T_J$ | 150 | °C |

Maximum Package Power Dissipation (See Thermal Information Section)

*Higher voltage selection available. See your local representative.

**PIN CONNECTIONS**



DEVICE CROSS-REFERENCE LISTING

9665 — SN75476* — ULN2001A — order MC1411P
9666 — SN75477 — ULN2002A — order MC1412P
9667 — SN75478 — ULN2003A — order MC1413P
9668 — ULN2004A — order MC1416P

*Similar

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Leakage Current | | $I_{CEX}$ | | | | µA |
| (*$V_O$ = 50 V, $T_A$ = +70°C) | All Types | | — | — | 100 | |
| (*$V_O$ = 50 V, $T_A$ = +25°C) | All Types | | — | — | 50 | |
| (*$V_O$ = 50 V, $T_A$ = +70°C, $V_I$ = 6.0 V) | MC1412 | | — | — | 500 | |
| (*$V_O$ = 50 V, $T_A$ = +70°C, $V_I$ = 1.0 V) | MC1416 | | — | — | 500 | |
| Collector-Emitter Saturation Voltage | | $V_{CE(sat)}$ | | | | V |
| ($I_C$ = 350 mA, $I_B$ = 500 µA) | All Types | | — | 1.1 | 1.6 | |
| ($I_C$ = 200 mA, $I_B$ = 350 µA) | All Types | | — | 0.95 | 1.3 | |
| ($I_C$ = 100 mA, $I_B$ = 250 µA) | All Types | | — | 0.85 | 1.1 | |
| Input Current — On Condition | | $I_{I(on)}$ | | | | mA |
| ($V_I$ = 17 V) | MC1412 | | — | 0.85 | 1.3 | |
| ($V_I$ = 3.85 V) | MC1413 | | — | 0.93 | 1.35 | |
| ($V_I$ = 5.0 V) | MC1416 | | — | 0.35 | 0.5 | |
| ($V_I$ = 12 V) | MC1416 | | — | 1.0 | 1.45 | |
| Input Voltage — On Condition | | $V_{I(on)}$ | | | | V |
| $V_{CE}$ = 2.0 V, $I_C$ = 300 mA) | MC1412 | | — | — | 13 | |
| $V_{CE}$ = 2.0 V, $I_C$ = 200 mA) | MC1413 | | — | — | 2.4 | |
| $V_{CE}$ = 2.0 V, $I_C$ = 250 mA) | MC1413 | | — | — | 2.7 | |
| $V_{CE}$ = 2.0 V, $I_C$ = 300 mA) | MC1413 | | — | — | 3.0 | |
| $V_{CE}$ = 2.0 V, $I_C$ = 125 mA) | MC1416 | | — | — | 5.0 | |
| $V_{CE}$ = 2.0 V, $I_C$ = 200 mA) | MC1416 | | — | — | 6.0 | |
| $V_{CE}$ = 2.0 V, $I_C$ = 275 mA) | MC1416 | | — | — | 7.0 | |
| $V_{CE}$ = 2.0 V, $I_C$ = 350 mA) | MC1416 | | — | — | 8.0 | |
| Input Current — Off Condition | All Types | $I_{I(off)}$ | 50 | 100 | — | µA |
| ($I_C$ = 500 µA, $T_A$ = +70°C) | | | | | | |
| DC Current Gain | MC1411 | $h_{FE}$ | 1000 | — | — | — |
| ($V_{CE}$ = 2.0 V, $I_C$ = 350 mA) | | | | | | |
| Input Capacitance | | $C_I$ | — | 15 | 30 | pF |
| Turn-On Delay Time | | $t_{on}$ | — | 0.25 | 1.0 | µs |
| (50% $E_I$ to 50% $E_O$) | | | | | | |
| Turn-Off Delay Time | | $t_{off}$ | — | 0.25 | 1.0 | µs |
| (50% $E_I$ to 50% $E_O$) | | | | | | |
| Clamp Diode Leakage Current | $T_A$ = +25°C | $I_R$ | — | — | 50 | µA |
| ($V_R$ = 50 V) | $T_A$ = +70°C | | | | 100 | |
| Clamp Diode Forward Voltage | | $V_F$ | — | 1.5 | 2.0 | V |
| ($I_F$ 350 mA) | | | | | | |

***Higher voltage selections available, contact your local representative.**

## TYPICAL PERFORMANCE CURVES – $T_A$ = 25°C

FIGURE 1 – OUTPUT CURRENT versus INPUT VOLTAGE

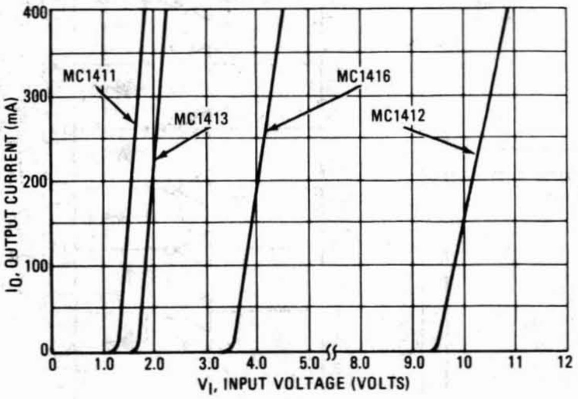
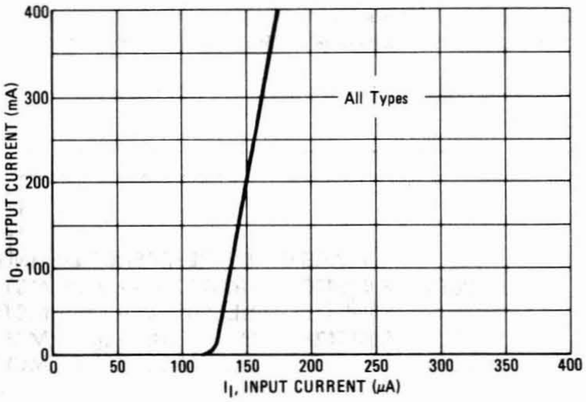


FIGURE 2 – OUTPUT CURRENT versus INPUT CURRENT



## TYPICAL CHARACTERISTIC CURVES – $T_A = 25^\circ C$ (continued)

FIGURE 3 – TYPICAL OUTPUT CHARACTERISTICS

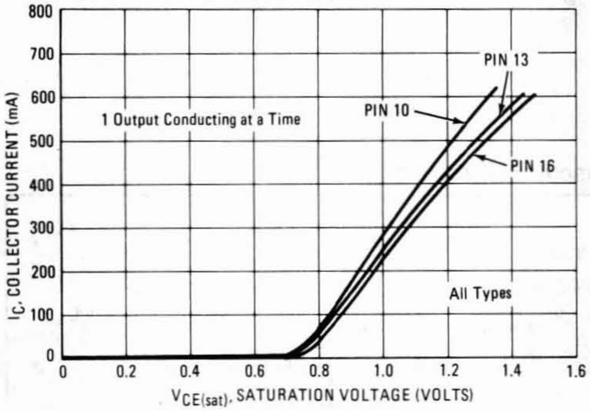


FIGURE 4 – INPUT CHARACTERISTICS – MC1412

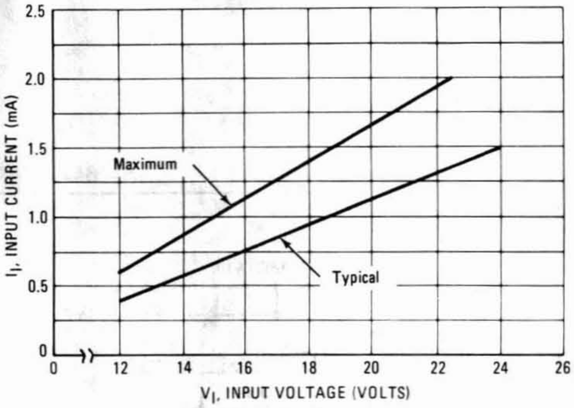


FIGURE 5 – INPUT CHARACTERISTICS – MC1413

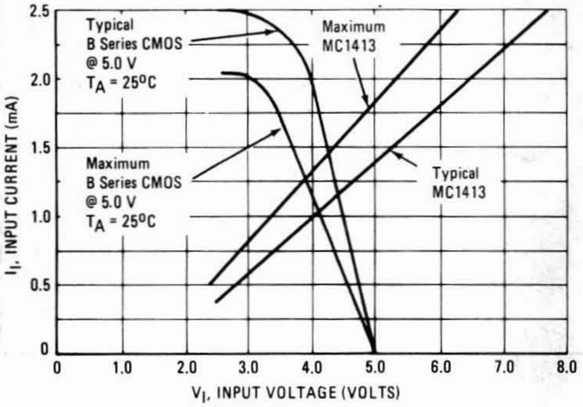


FIGURE 6 – INPUT CHARACTERISTICS – MC1416

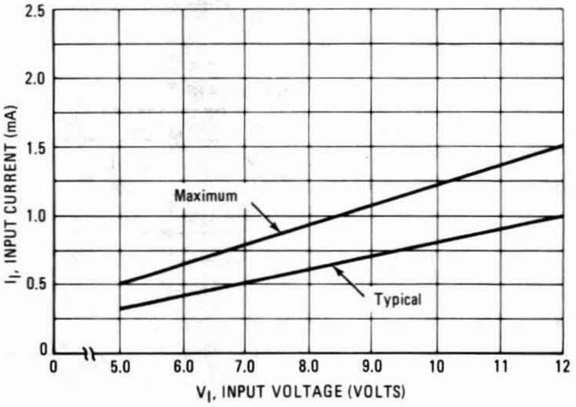


FIGURE 7 – MAXIMUM COLLECTOR CURRENT versus DUTY CYCLE (AND NUMBER OF DRIVERS IN USE) – CERAMIC

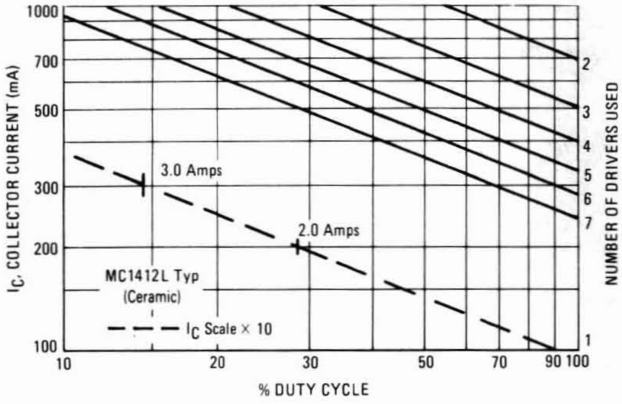
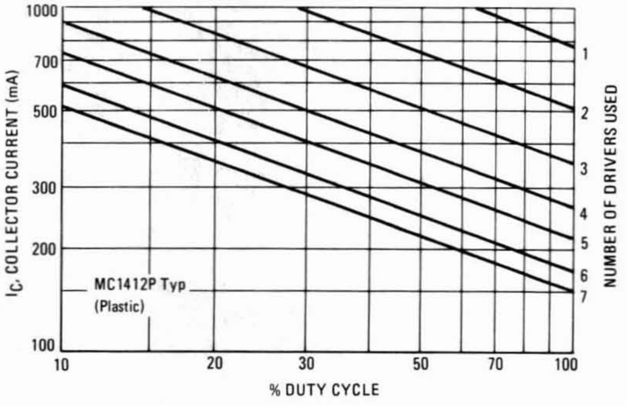
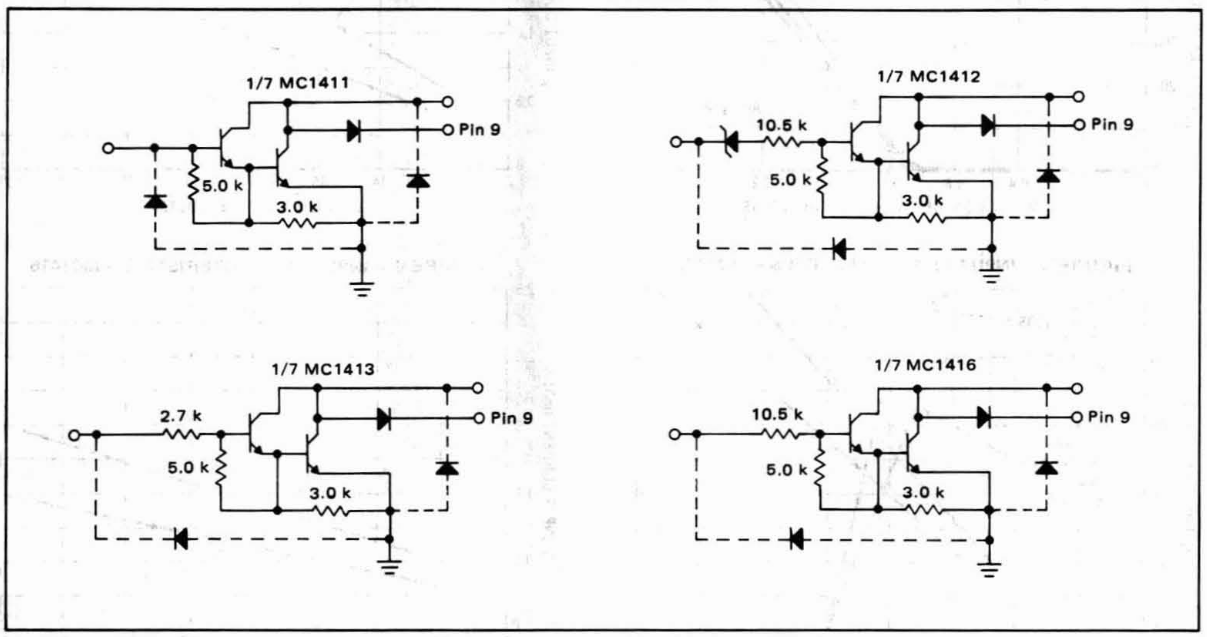


FIGURE 8 – MAXIMUM COLLECTOR CURRENT versus DUTY CYCLE (AND NUMBER OF DRIVERS IN USE) – PLASTIC



REPRESENTATIVE CIRCUIT SCHEMATICS


1/7 MC1411
Pin 9
5.0 k
3.0 k
1/7 MC1412
10.5 k
Pin 9
5.0 k
3.0 k
1/7 MC1413
2.7 k
Pin 9
5.0 k
3.0 k
1/7 MC1416
10.5 k
Pin 9
5.0 k
3.0 k

**MOTOROLA**

# MC1472

## DUAL PERIPHERAL-HIGH-VOLTAGE POSITIVE "NAND" DRIVER

The dual driver consists of a pair of PNP-buffered AND gates connected to the bases of a pair of high-voltage NPN transistors. They are similar to the MC75452 drivers but with the added advantages of: 1) 70 Volt capability 2) output suppression diodes and 3) PNP buffered inputs for MOS compatibility. These features make the MC1472 ideal for mating MOS logic or microprocessors to lamps, relays, printer hammers and incandescent displays.

- 300 mA Output Capability (each transistor)
- 70 Vdc Breakdown Voltage
- Internal Output Clamp Diodes
- Low Input Loading for MOS Compatibility (PNP buffered)

**CROSS REFERENCE**
UDN-5712 – SN75475 – MC1472

**MAXIMUM RATINGS** ($T_A$ = 25°C, Note 1).

| Rating | Value | Unit |
|---|---|---|
| Supply Voltage | 7.0 | Volts |
| Input Voltage | 5.5 | Volts |
| Output Voltage | 80 | Volts |
| Clamp Voltage | 80 | Volts |
| Output Current (Continuous) | 300 | mA |
| Operating Junction Temperature<br>Ceramic Package<br>Plastic Package | <br>+175<br>+150 | °C |
| Storage Temperature Range | -65 to +150 | °C |

Note 1: "Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

**RECOMMENDED OPERATING CONDITIONS**

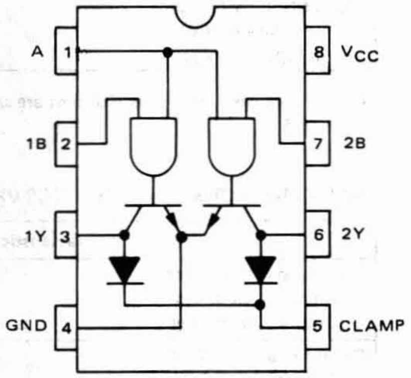
| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | Volts |
| Operating Ambient Temperature | $T_A$ | 0 | 70 | °C |
| Output Voltage | $V_O$ | $V_{CC}$ | 70 | Volts |
| Clamp Voltage | $V_C$ | $V_O$ | 70 | Volts |

**DUAL PERIPHERAL POSITIVE "NAND" DRIVER**

**SILICON MONOLITHIC INTEGRATED CIRCUITS**

**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02

**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04



Positive Logic: Y=AB*

**TRUTH TABLE**

| A | B | Y |
|---|---|---|
| L | L | H ("OFF" STATE) |
| L | H | H ("OFF" STATE) |
| H | L | H ("OFF" STATE) |
| H | H | L ("ON" STATE) |

H = Logic One
L = Logic Zero

**ORDERING INFORMATION**

| Device | Alternate | Temperature Range | Package |
|---|---|---|---|
| MC1472U | – | 0 to +70°C | Ceramic DIP |
| MC1472P1 | – | 0 to +70°C | Plastic DIP |

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted min/max limits apply across the 0°C to 70°C temperature range with 4.5 V $\leq V_{CC} \leq$ 5.5 V. All typical values are for $T_A$ = 25°C, $V_{CC}$ = 5.0 Volts.)

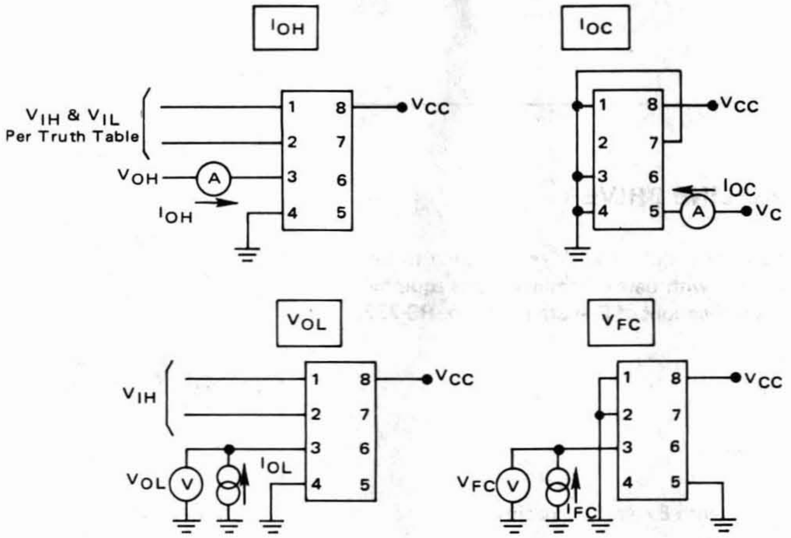
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage — High Logic State | $V_{IH}$ | 2.0 | — | 5.5 | Vdc |
| Input Voltage — Low Logic State | $V_{IL}$ | 0 | — | 0.8 | Vdc |
| Input Current — Low Logic State<br>($V_{IL}$ = 0.4 V)<br>A Input<br>B Input | $I_{IL}$ | — | — | −0.3<br>−0.15 | mA |
| Input Current — High Logic State<br>($V_{IH}$ = 2.4 V)<br>A Input<br>B Input<br>($V_{IH}$ = 5.5 V)<br>A Input<br>B Input | $I_{IH}$ | —<br>—<br>—<br>— | —<br>—<br>—<br>— | 40<br>20<br>200<br>100 | µA |
| Input Clamp Voltage<br>($I_{CC}$ = −12 mA) | $V_{IK}$ | — | — | −1.5 | V |
| Output Leakage Current — High Logic State<br>($V_O$ = 70 V, See Test Figure) | $I_{OH}$ | | — | 100 | µA |
| Output Voltage — Low Logic State<br>($I_{OL}$ = 100 mA)<br>($I_{OL}$ = 300 mA) | $V_{OL}$ | —<br>— | —<br>— | 0.4<br>0.7 | V |
| Output Clamp Diode Leakage Current<br>($V_C$ = 70 V, See Test Figure) | $I_{OC}$ | — | — | 100 | V |
| Output Clamp Forward Voltage<br>($I_{FC}$ = 300 mA, See Test Figure) | $V_{FC}$ | — | — | 1.7 | V |
| Power Supply Current<br>(All Inputs at $V_{IH}$)<br>(All Inputs at $V_{IL}$) | $I_{CC}$ | —<br>— | —<br>— | 70<br>15 | mA |

NOTE: All currents into device pins are shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted.

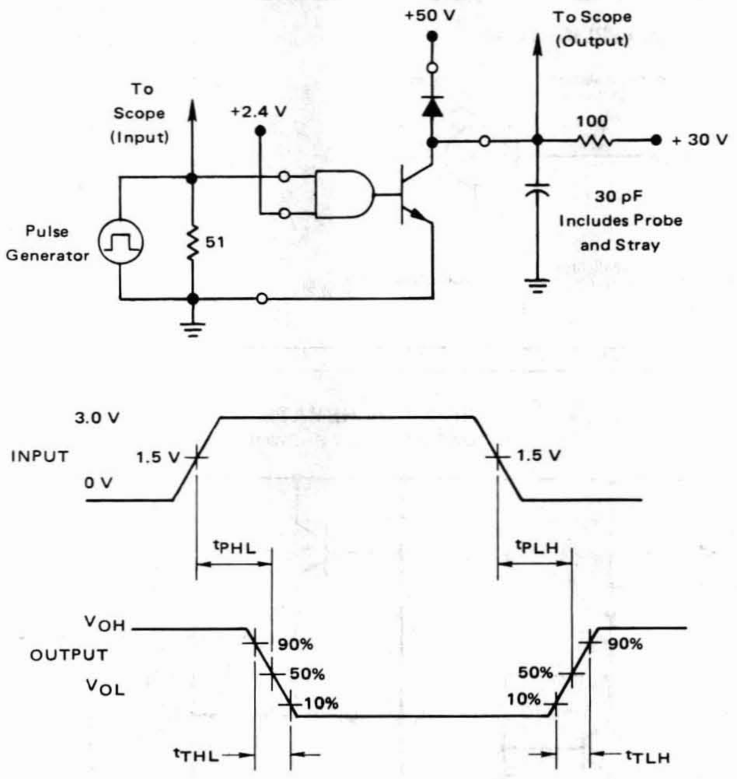
**SWITCHING CHARACTERISTICS** $V_{CC}$ = 5.0V, $T_A$ = 25°C

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Time<br>Output High to Low<br>Output Low to High | $t_{PHL}$<br>$t_{PLH}$ | –<br>– | –<br>– | 1.0<br>0.75 | µs |
| Output Transition Time<br>Output High to Low<br>Output Low to High | $t_{THL}$<br>$t_{TLH}$ | –<br>– | –<br>– | 0.1<br>0.1 | µs |

## TEST CIRCUITS


$I_{OH}$
$V_{IH}$ & $V_{IL}$ Per Truth Table
$V_{OH}$
A
$I_{OH}$
1
2
3
4
8
7
6
5
$V_{CC}$
$I_{OC}$
$I_{OC}$
A
$V_C$
$V_{CC}$
$V_{OL}$
$V_{IH}$
$V_{OL}$
V
$I_{OL}$
$V_{CC}$
$V_{FC}$
$V_{FC}$
V
$I_{FC}$
$V_{CC}$

## SWITCHING TEST CIRCUIT AND WAVEFORM


+50 V
To Scope (Output)
To Scope (Input)
+2.4 V
100
+ 30 V
Pulse Generator
51
30 pF Includes Probe and Stray
3.0 V
INPUT
1.5 V
0 V
1.5 V
$t_{PHL}$
$t_{PLH}$
$V_{OH}$
OUTPUT
$V_{OL}$
90%
50%
10%
90%
50%
10%
$t_{THL}$
$t_{TLH}$

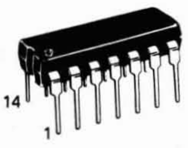
**MOTOROLA**

# MC1488

## QUAD MDTL LINE DRIVER
## RS-232C

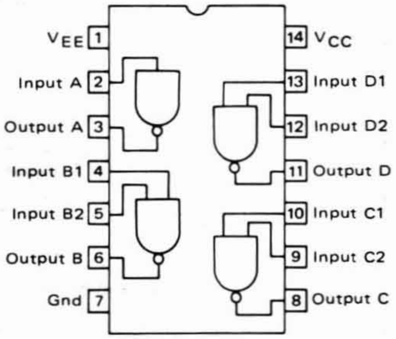
SILICON MONOLITHIC
INTEGRATED CIRCUIT

**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

### PIN CONNECTIONS


VEE 1
Input A 2
Output A 3
Input B1 4
Input B2 5
Output B 6
Gnd 7
14 VCC
13 Input D1
12 Input D2
11 Output D
10 Input C1
9 Input C2
8 Output C

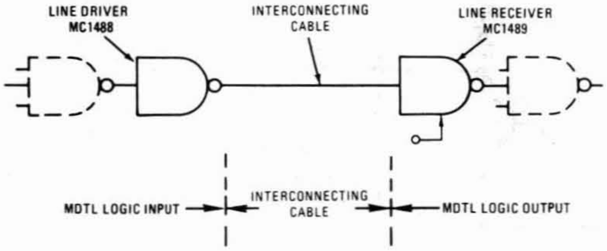
## QUAD LINE DRIVER

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

**Features:**

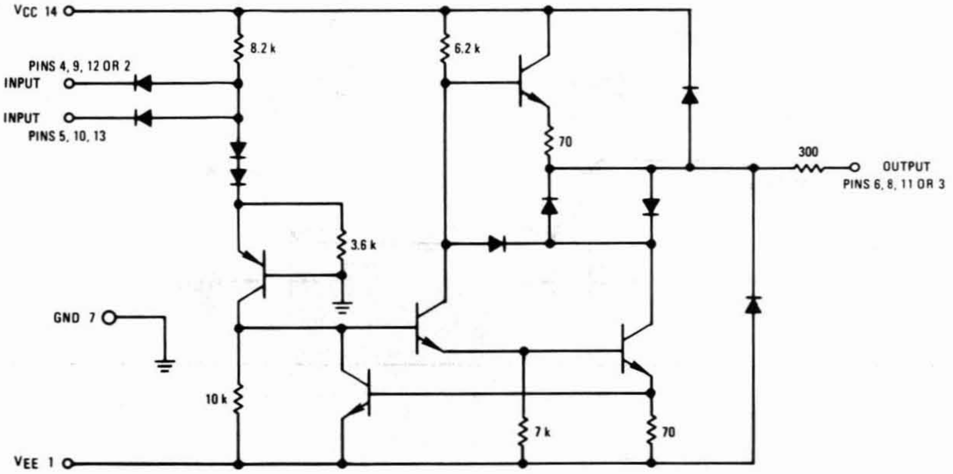
- Current Limited Output
  ±10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

### TYPICAL APPLICATION


LINE DRIVER
MC1488
INTERCONNECTING
CABLE
LINE RECEIVER
MC1489
MDTL LOGIC INPUT
INTERCONNECTING
CABLE
MDTL LOGIC OUTPUT

### CIRCUIT SCHEMATIC

(1/4 OF CIRCUIT SHOWN)


VCC 14
8.2 k
6.2 k
PINS 4, 9, 12 OR 2
INPUT
INPUT
PINS 5, 10, 13
70
300
OUTPUT
PINS 6, 8, 11 OR 3
3.6 k
GND 7
10 k
7 k
70
VEE 1

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +15<br>-15 | Vdc |
| Input Voltage Range | $V_{IR}$ | $-15 \leq V_{IR} \leq 7.0$ | Vdc |
| Output Signal Voltage | $V_O$ | ±15 | Vdc |
| Power Derating (Package Limitation, Ceramic and Plastic Dual-In-Line Package)<br>Derate above $T_A$ = +25°C | $P_D$<br>$1/R_{\theta JA}$ | 1000<br>6.7 | mW<br>mW/°C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +75 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +175 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +9.0 ±10% Vdc, $V_{EE}$ = −9.0 ±10% Vdc, $T_A$ = 0 to 75°C unless otherwise noted.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Current – Low Logic State ($V_{IL}$ = 0) | 1 | $I_{IL}$ | – | 1.0 | 1.6 | mA |
| Input Current – High Logic State ($V_{IH}$ = 5.0 V) | 1 | $I_{IH}$ | – | – | 10 | µA |
| Output Voltage – High Logic State | 2 | $V_{OH}$ | | | | Vdc |
| ($V_{IL}$ = 0.8 Vdc, $R_L$ = 3.0 kΩ, $V_{CC}$ = +9.0 Vdc, $V_{EE}$ = -9.0 Vdc) | | | +6.0 | +7.0 | – | |
| ($V_{IL}$ = 0.8 Vdc, $R_L$ = 3.0 kΩ, $V_{CC}$ = +13.2 Vdc, $V_{EE}$ = -13.2 Vdc) | | | +9.0 | +10.5 | – | |
| Output Voltage – Low Logic State | 2 | $V_{OL}$ | | | | Vdc |
| ($V_{IH}$ = 1.9 Vdc, $R_L$ = 3.0 kΩ, $V_{CC}$ = +9.0 Vdc, $V_{EE}$ = -9.0 Vdc) | | | -6.0 | -7.0 | – | |
| ($V_{IH}$ = 1.9 Vdc, $R_L$ = 3.0 kΩ, $V_{CC}$ = +13.2 Vdc, $V_{EE}$ = -13.2 Vdc) | | | -9.0 | -10.5 | – | |
| Positive Output Short-Circuit Current (1) | 3 | $I_{OS+}$ | +6.0 | +10 | +12 | mA |
| Negative Output Short-Circuit Current (1) | 3 | $I_{OS-}$ | -6.0 | -10 | -12 | mA |
| Output Resistance ($V_{CC}$ = $V_{EE}$ = 0, $\|V_O\|$ = ±2.0 V) | 4 | $r_o$ | 300 | – | – | Ohms |
| Positive Supply Current ($R_l$ = ∞) | 5 | $I_{CC}$ | | | | mA |
| ($V_{IH}$ = 1.9 Vdc, $V_{CC}$ = +9.0 Vdc) | | | – | +15 | +20 | |
| ($V_{IL}$ = 0.8 Vdc, $V_{CC}$ = +9.0 Vdc) | | | – | +4.5 | +6.0 | |
| ($V_{IH}$ = 1.9 Vdc, $V_{CC}$ = +12 Vdc) | | | – | +19 | +25 | |
| ($V_{IL}$ = 0.8 Vdc, $V_{CC}$ = +12 Vdc) | | | – | +5.5 | +7.0 | |
| ($V_{IH}$ = 1.9 Vdc, $V_{CC}$ = +15 Vdc) | | | – | – | +34 | |
| ($V_{IL}$ = 0.8 Vdc, $V_{CC}$ = +15 Vdc) | | | – | – | +12 | |
| Negative Supply Current ($R_L$ = ∞) | 5 | $I_{EE}$ | | | | |
| ($V_{IH}$ = 1.9 Vdc, $V_{EE}$ = -9.0 Vdc) | | | – | -13 | -17 | mA |
| ($V_{IL}$ = 0.8 Vdc, $V_{EE}$ = -9.0 Vdc) | | | – | – | -15 | µA |
| ($V_{IH}$ = 1.9 Vdc, $V_{EE}$ = -12 Vdc) | | | – | -18 | -23 | mA |
| ($V_{IL}$ = 0.8 Vdc, $V_{EE}$ = -12 Vdc) | | | – | – | -15 | µA |
| ($V_{IH}$ = 1.9 Vdc, $V_{EE}$ = -15 Vdc) | | | – | – | -34 | mA |
| ($V_{IL}$ = 0.8 Vdc, $V_{EE}$ = -15 Vdc) | | | – | – | -2.5 | mA |
| Power Consumption | | $P_C$ | | | | mW |
| ($V_{CC}$ = 9.0 Vdc, $V_{EE}$ = -9.0 Vdc) | | | – | – | 333 | |
| ($V_{CC}$ = 12 Vdc, $V_{EE}$ = -12 Vdc) | | | – | – | 576 | |

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = +9.0 ± 1% Vdc, $V_{EE}$ = -9.0 ± 1% Vdc, $T_A$ = +25°C.)

| | | | | | | |
|---|---|---|---|---|---|---|
| Propagation Delay Time ($z_l$ = 3.0 k and 15 pF) | 6 | $t_{PLH}$ | – | 275 | 350 | ns |
| Fall Time ($z_l$ = 3.0 k and 15 pF) | 6 | $t_{THL}$ | – | 45 | 75 | ns |
| Propagation Delay Time ($z_l$ = 3.0 k and 15 pF) | 6 | $t_{PHL}$ | – | 110 | 175 | ns |
| Rise Time ($z_l$ = 3.0 k and 15 pF) | 6 | $t_{TLH}$ | – | 55 | 100 | ns |

(1) Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

## CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

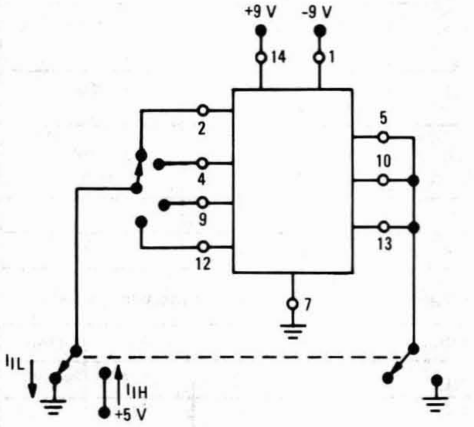

+9 V
-9 V
14
1
2
4
9
12
5
10
13
7
$I_{IL}$
$I_{IH}$
+5 V

FIGURE 2 – OUTPUT VOLTAGE

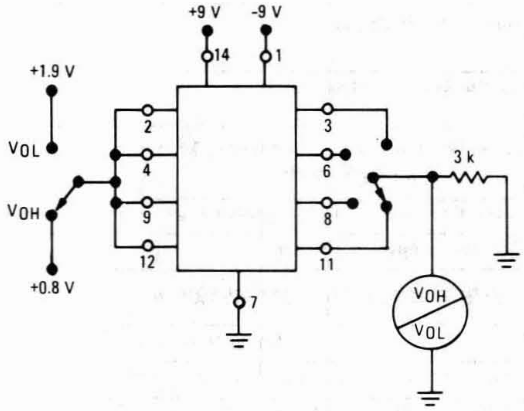

+9 V
-9 V
14
1
+1.9 V
$V_{OL}$
$V_{OH}$
+0.8 V
2
4
9
12
3
6
8
11
7
3 k
$V_{OH}$
$V_{OL}$

FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

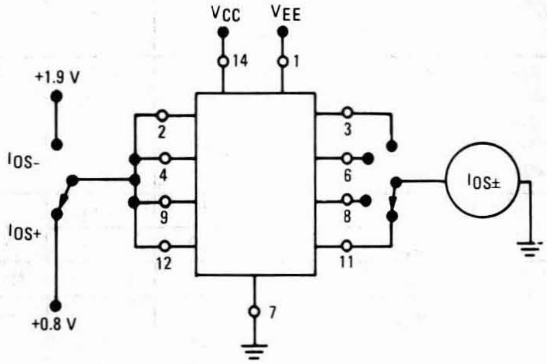

$V_{CC}$
$V_{EE}$
14
1
+1.9 V
$I_{OS-}$
$I_{OS+}$
+0.8 V
2
4
9
12
3
6
8
11
7
$I_{OS\pm}$

FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

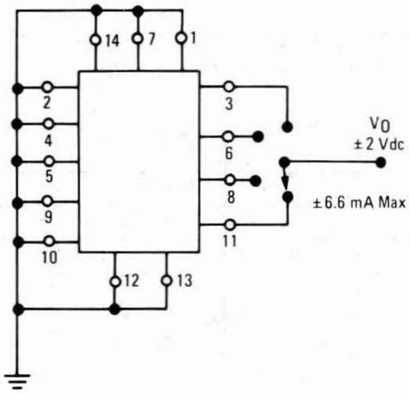

14
7
1
2
4
5
9
10
12
13
3
6
8
11
$V_O$
± 2 Vdc
± 6.6 mA Max

FIGURE 5 – POWER-SUPPLY CURRENTS

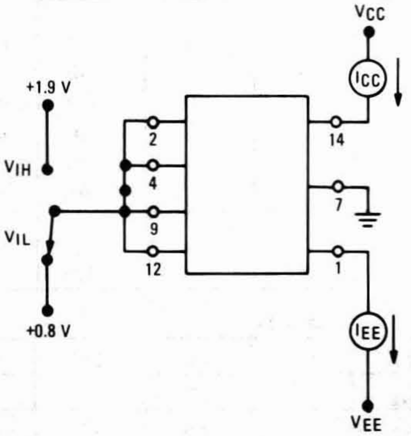
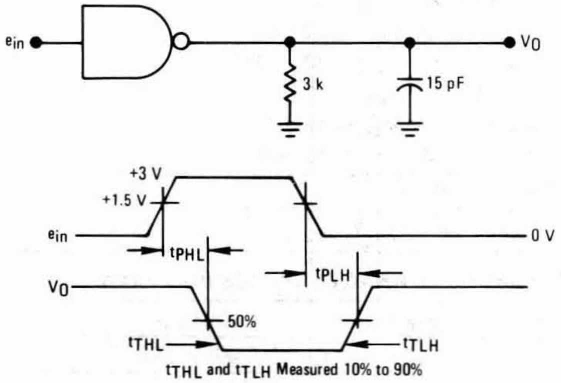

$V_{CC}$
$I_{CC}$
+1.9 V
$V_{IH}$
$V_{IL}$
+0.8 V
2
4
9
12
14
7
1
$I_{EE}$
$V_{EE}$

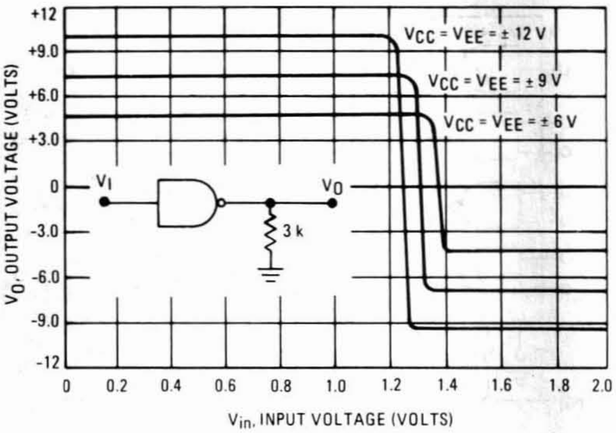
FIGURE 6 – SWITCHING RESPONSE


$e_{in}$
$V_O$
3 k
15 pF
+3 V
+1.5 V
$e_{in}$
0 V
$t_{PHL}$
$t_{PLH}$
$V_O$
50%
$t_{THL}$
$t_{TLH}$
$t_{THL}$ and $t_{TLH}$ Measured 10% to 90%

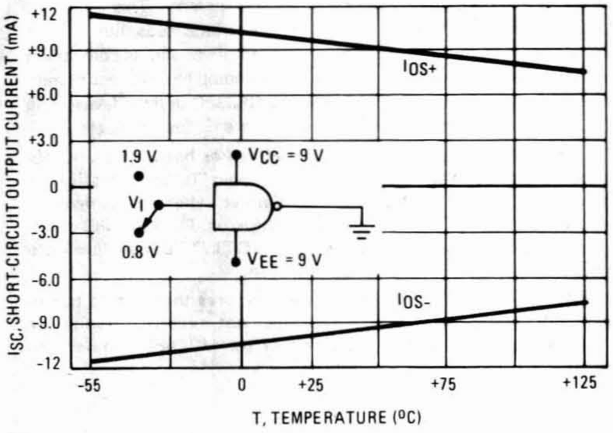
## TYPICAL CHARACTERISTICS

($T_A$ = +25°C unless otherwise noted.)

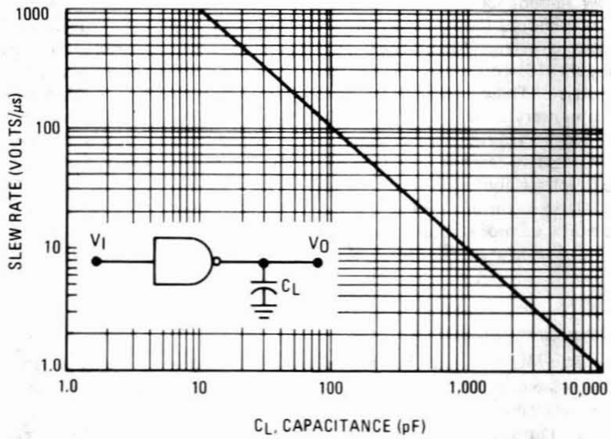
### FIGURE 7 – TRANSFER CHARACTERISTICS versus POWER-SUPPLY VOLTAGE



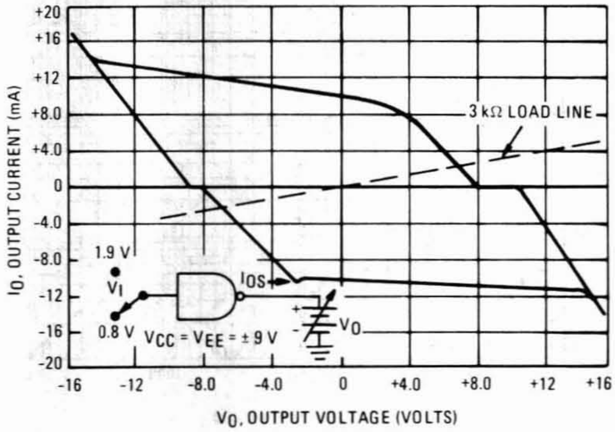
### FIGURE 8 – SHORT-CIRCUIT OUTPUT CURRENT versus TEMPERATURE



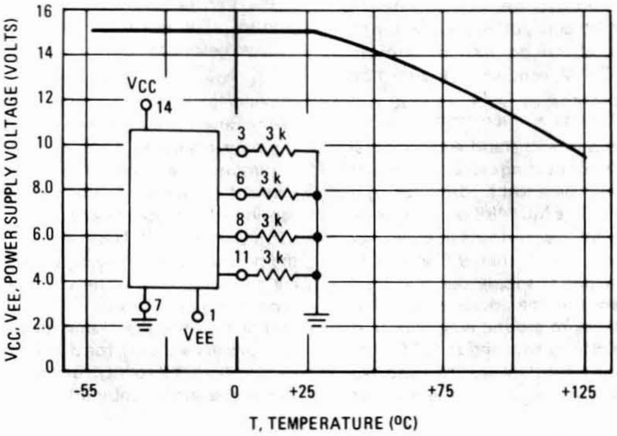
### FIGURE 9 – OUTPUT SLEW RATE versus LOAD CAPACITANCE



### FIGURE 10 – OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS



### FIGURE 11 – MAXIMUM OPERATING TEMPERATURE versus POWER-SUPPLY VOLTAGE



## APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) RS232C specification detail the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

FIGURE 12 – SLEW RATE versus CAPACITANCE FOR $I_{SC}$ = 10 mA

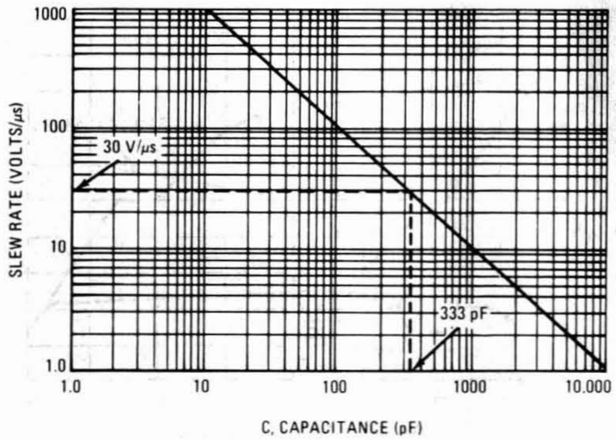
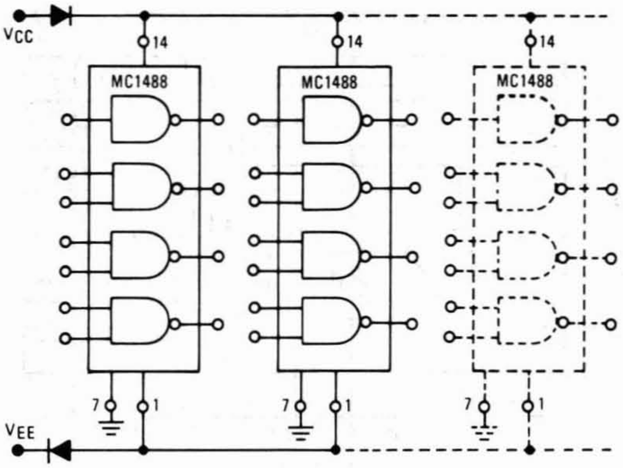


FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geqslant 9.0$ V; $V_{EE} \leqslant -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

### Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power-Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488 will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

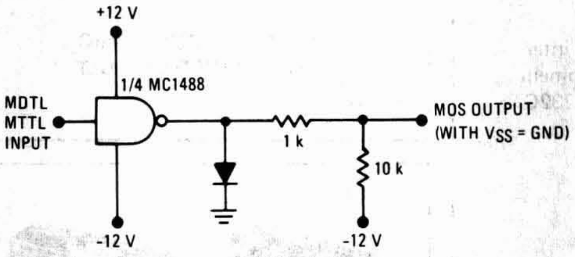
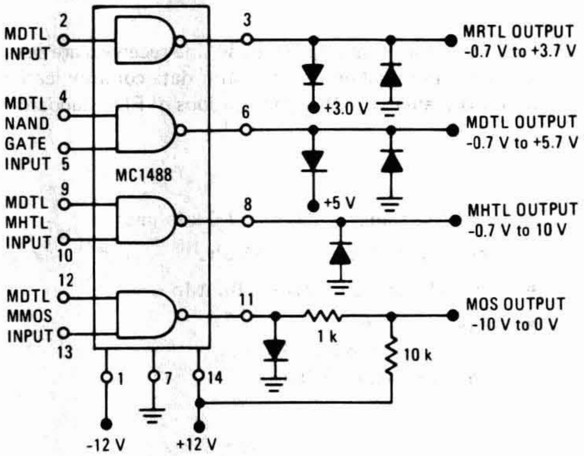

+12 V
1/4 MC1488
MDTL
MTTL
INPUT
1 k
10 k
MOS OUTPUT
(WITH $V_{SS}$ = GND)
-12 V
-12 V

FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS


MDTL INPUT
2
3
MRTL OUTPUT
-0.7 V to +3.7 V
+3.0 V
MDTL NAND GATE INPUT
4
5
6
MDTL OUTPUT
-0.7 V to +5.7 V
+5 V
MC1488
MDTL MHTL INPUT
9
10
8
MHTL OUTPUT
-0.7 V to 10 V
MDTL MMOS INPUT
12
13
11
1 k
10 k
MOS OUTPUT
-10 V to 0 V
1
7
14
-12 V
+12 V

**MOTOROLA**

# MC1489
# MC1489A

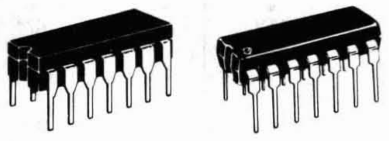
## QUAD LINE RECEIVERS

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

- Input Resistance – 3.0 k to 7.0 kilohms
- Input Signal Range – ± 30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering

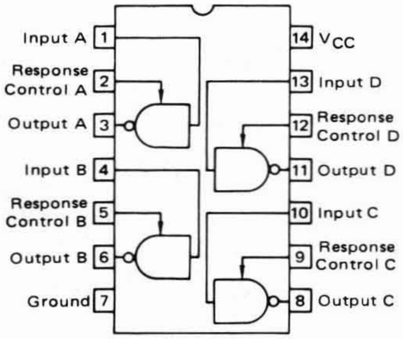
## QUAD MDTL LINE RECEIVERS RS-232C

SILICON MONOLITHIC INTEGRATED CIRCUIT

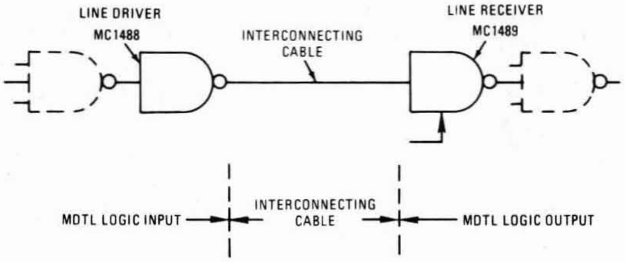


**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA

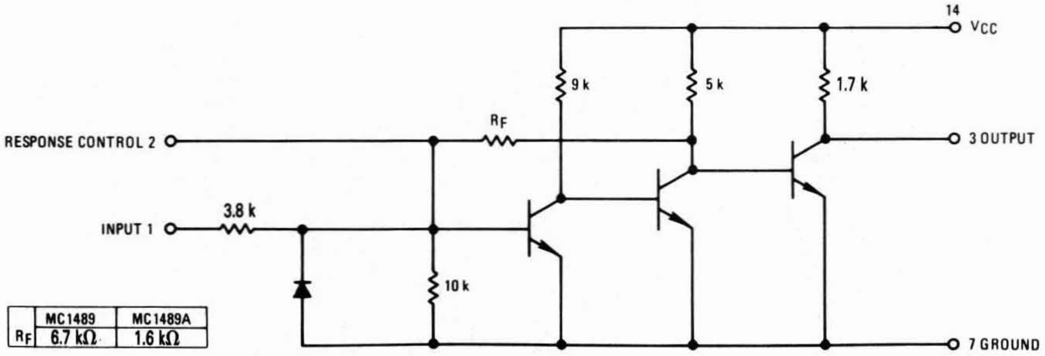
**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05


Input A 1
Response Control A 2
Output A 3
Input B 4
Response Control B 5
Output B 6
Ground 7
14 VCC
13 Input D
12 Response Control D
11 Output D
10 Input C
9 Response Control C
8 Output C

## TYPICAL APPLICATION


LINE DRIVER
MC1488
INTERCONNECTING CABLE
LINE RECEIVER
MC1489
MDTL LOGIC INPUT
INTERCONNECTING CABLE
MDTL LOGIC OUTPUT

**EQUIVALENT CIRCUIT SCHEMATIC** (1/4 OF CIRCUIT SHOWN)


14
VCC
9 k
5 k
1.7 k
RF
RESPONSE CONTROL 2
3 OUTPUT
INPUT 1
3.8 k
10 k
7 GROUND

| | MC1489 | MC1489A |
|---|---|---|
| RF | 6.7 kΩ | 1.6 kΩ |

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 10 | Vdc |
| Input Voltage Range | $V_{IR}$ | ±30 | Vdc |
| Output Load Current | $I_L$ | 20 | mA |
| Power Dissipation (Package Limitation, Ceramic and Plastic Dual In-Line Package)<br>Derate above $T_A$ = +25°C | $P_D$<br>$1/\theta_{JA}$ | 1000<br>6.7 | mW<br>mW/°C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +75 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +175 | °C |

**ELECTRICAL CHARACTERISTICS** (Response control pin is open.) ($V_{CC}$ = +5.0 Vdc ±10%, $T_A$ = 0 to +75°C unless otherwise noted)

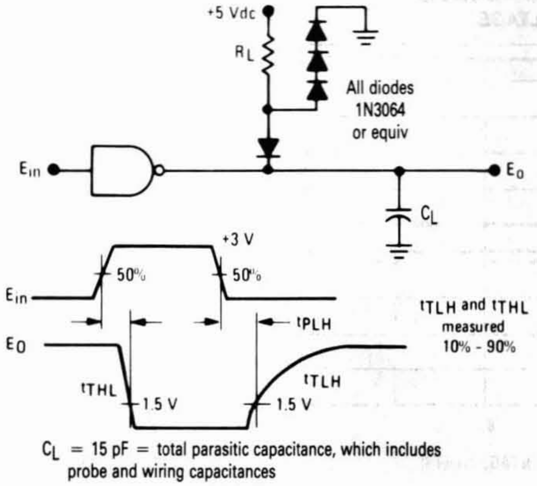
| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Positive Input Current ($V_{IH}$ = +25 Vdc)<br>($V_{IH}$ = +3.0 Vdc) | $I_{IH}$ | 3.6<br>0.43 | —<br>— | 8.3<br>— | mA |
| Negative Input Current ($V_{IL}$ = −25 Vdc)<br>($V_{IL}$ = −3.0 Vdc) | $I_{IL}$ | −3.6<br>−0.43 | —<br>— | −8.3<br>— | mA |
| Input Turn-On Threshold Voltage<br>($T_A$ = +25°C, $V_{OL}$ ≤ 0.45 V) MC1489<br>MC1489A | $V_{IH}$ | <br>1.0<br>1.75 | <br>—<br>1.95 | <br>1.5<br>2.25 | Vdc |
| Input Turn-Off Threshold Voltage<br>($T_A$ = +25°C, $V_{OH}$ ≥ 2.5 V, $I_L$ = −0.5 mA) MC1489<br>MC1489A | $V_{IL}$ | <br>0.75<br>0.75 | <br>—<br>0.8 | <br>1.25<br>1.25 | Vdc |
| Output Voltage High ($V_{IH}$ = 0.75 V, $I_L$ = −0.5 mA)<br>(Input Open Circuit, $I_L$ = −0.5 mA) | $V_{OH}$ | 2.5<br>2.5 | 4.0<br>4.0 | 5.0<br>5.0 | Vdc |
| Output Voltage Low ($V_{IL}$ = 3.0 V, $I_L$ = 10 mA) | $V_{OL}$ | — | 0.2 | 0.45 | Vdc |
| Output Short-Circuit Current | $I_{OS}$ | — | −3.0 | −4.0 | mA |
| Power Supply Current (All Gates "on," $I_{out}$ = 0 mA, $V_{IH}$ = +5.0 Vdc) | $I_{CC}$ | — | 16 | 26 | mA |
| Power Consumption ($V_{IH}$ = +5.0 Vdc) | $P_C$ | — | 80 | 130 | mW |

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = 5.0 Vdc ±1%, $T_A$ = +25°C, See Figure 1.)

| | | | | | |
|---|---|---|---|---|---|
| Propagation Delay Time ($R_L$ = 3.9 kΩ) | $t_{PLH}$ | — | 25 | 85 | ns |
| Rise Time ($R_L$ = 3.9 kΩ) | $t_{TLH}$ | — | 120 | 175 | ns |
| Propagation Delay Time ($R_L$ = 390 kΩ) | $t_{PHL}$ | — | 25 | 50 | ns |
| Fall Time ($R_L$ = 390 kΩ) | $t_{THL}$ | — | 10 | 20 | ns |

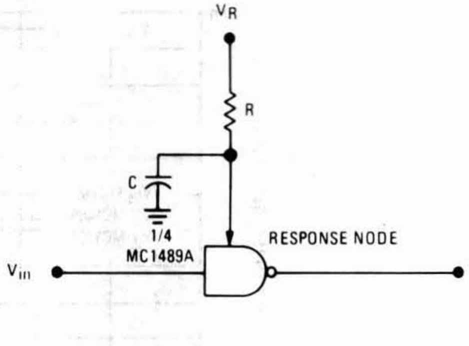
## TEST CIRCUITS

### FIGURE 1 — SWITCHING RESPONSE



$C_L$ = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances

### FIGURE 2 — RESPONSE CONTROL NODE



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

## TYPICAL CHARACTERISTICS

($V_{CC}$ = 5.0 Vdc, $T_A$ = +25°C unless otherwise noted)

FIGURE 3 — INPUT CURRENT

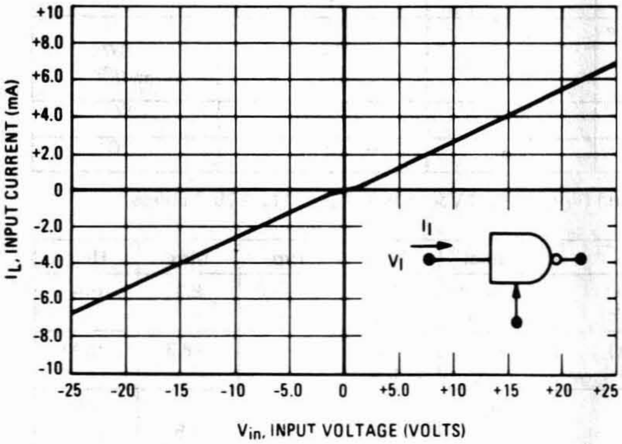


FIGURE 4 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

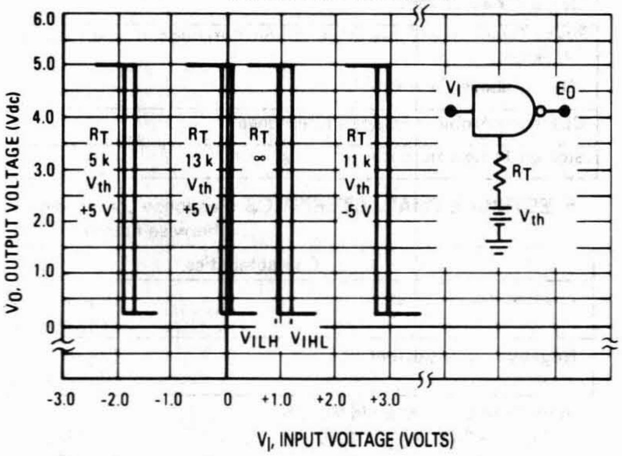


FIGURE 5 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

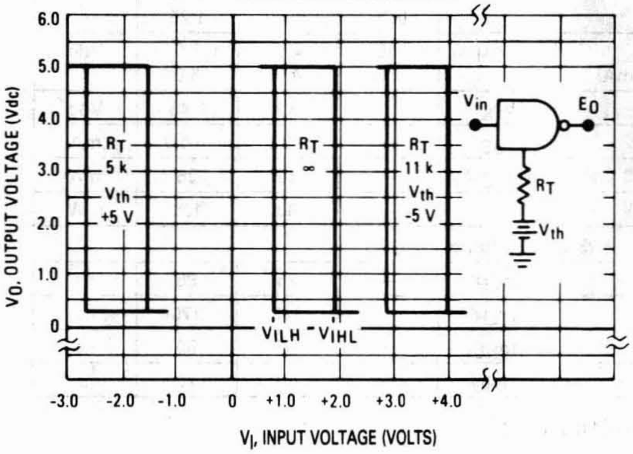


FIGURE 6 — INPUT THRESHOLD VOLTAGE versus TEMPERATURE

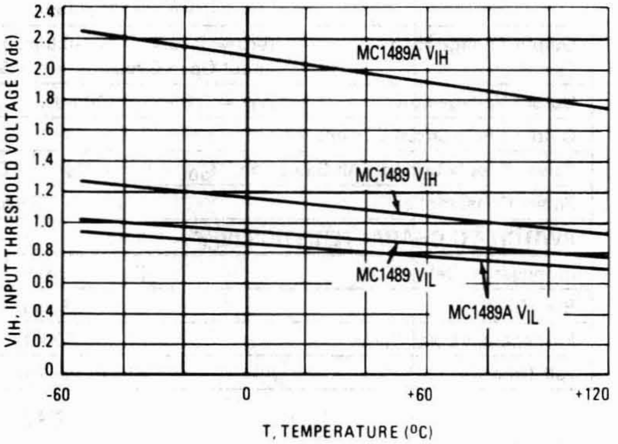
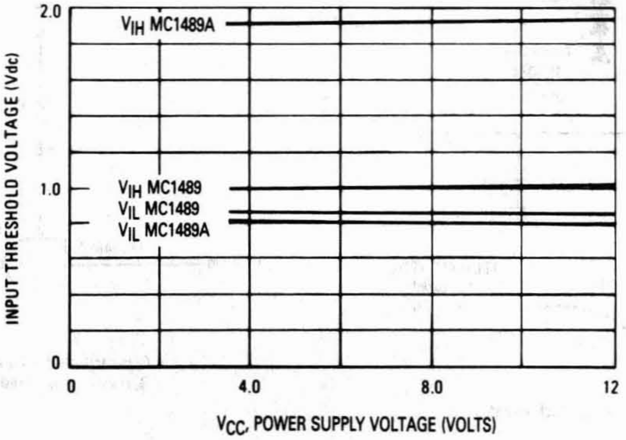


FIGURE 7 — INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



## APPLICATIONS INFORMATION

### General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one $V_{BE}$.

The receiver shall detect a voltage between −3.0 and −25 volts as a Logic "1" and inputs between +3.0 and +25 volts as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

### Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

FIGURE 8 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

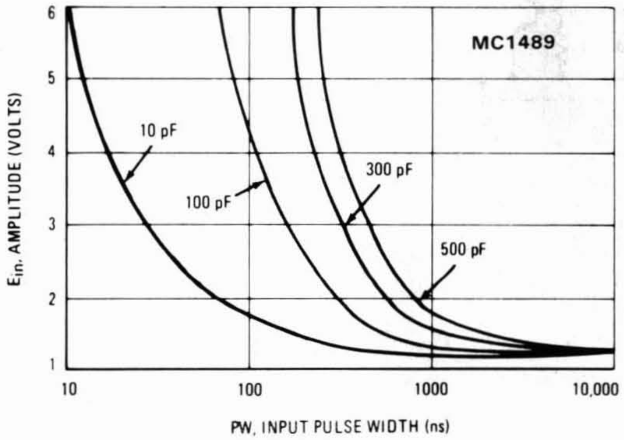
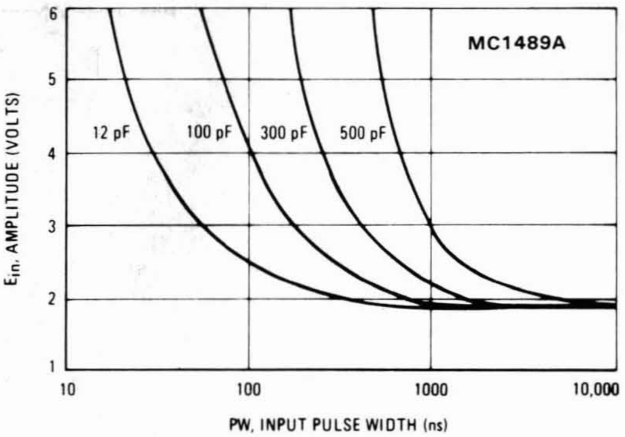


FIGURE 9 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



## APPLICATIONS INFORMATION (continued)

FIGURE 10 — TYPICAL TRANSLATOR APPLICATION — MOS TO DTL OR TTL

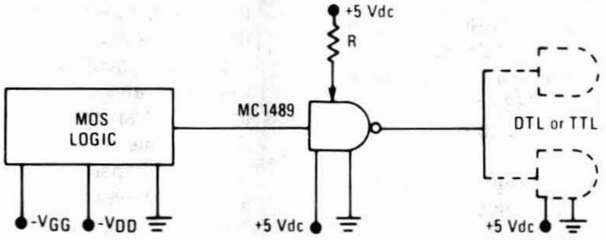
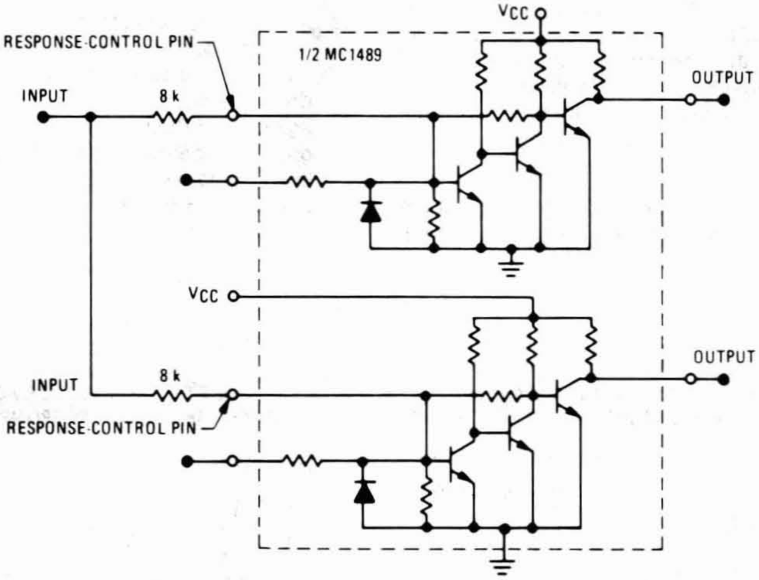

+5 Vdc
R
MOS LOGIC
MC1489
DTL or TTL
-VGG
-VDD
+5 Vdc
+5 Vdc

FIGURE 11 — TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C


VCC
RESPONSE-CONTROL PIN
1/2 MC1489
INPUT
8 k
OUTPUT
VCC
OUTPUT
INPUT
8 k
RESPONSE-CONTROL PIN

**MOTOROLA**

# MC3437

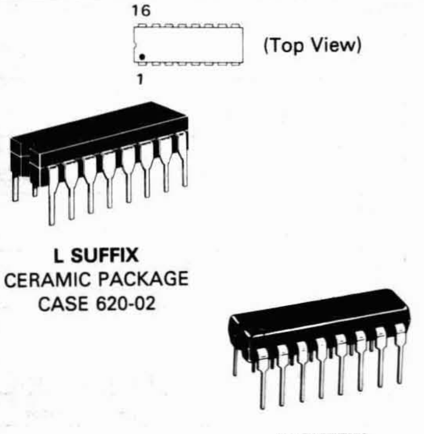
## HEX BUS RECEIVER WITH INPUT HYSTERESIS

These high-speed bus receivers are useful in bus organized data transmission systems employing terminated 120 Ω lines. The receivers feature input hysteresis to obtain improved noise immunity. The receivers low input current requirement allows up to 27 driver/receiver pairs to share a common bus. A pair of Disable Inputs are provided. These Disable Inputs along with the receiver outputs are MTTL compatible.

- Built in receiver hysteresis
- Receiver input threshold is not affected by temperature
- Propagation delay time — 20 ns (Typ)
- Direct Replacement for DM8837

### HEX BUS RECEIVER

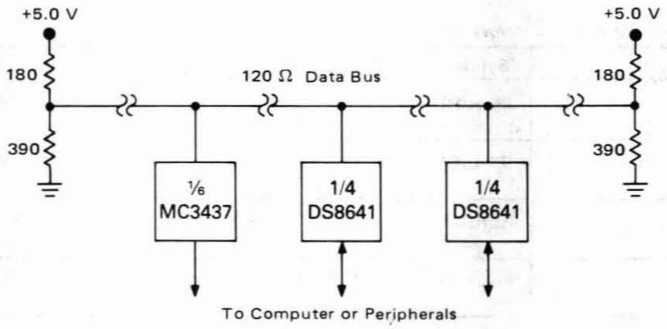
### SILICON MONOLITHIC INTEGRATED CIRCUIT


16
(Top View)
1

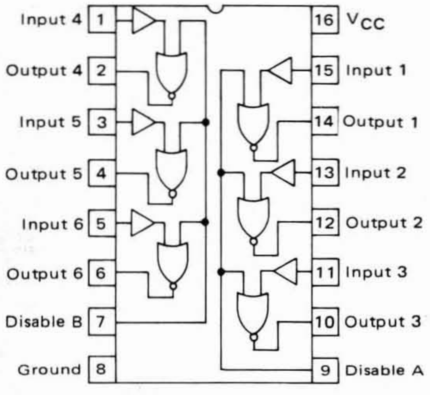
**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

FIGURE 1 – TYPICAL APPLICATION


+5.0 V
+5.0 V
180
120 Ω Data Bus
180
390
390
1/6 MC3437
1/4 DS8641
1/4 DS8641
To Computer or Peripherals

PIN CONNECTIONS


Input 4 1
Output 4 2
Input 5 3
Output 5 4
Input 6 5
Output 6 6
Disable B 7
Ground 8
16 $V_{CC}$
15 Input 1
14 Output 1
13 Input 2
12 Output 2
11 Input 3
10 Output 3
9 Disable A

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 7.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Power Dissipation<br>Derate above 25°C | $P_D$ | 625<br>3.85 | mW<br>mW/°C |
| Operating Ambient Temperature Range | $T_A$ | 0 to 70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

TRUTH TABLE

| Input | Disable | Output |
|---|---|---|
| O | L | H |
| O | H | L |
| I | L | L |
| I | H | L |

O = < 1.05 V
I = > 2.5 V
H = High Logic State
L = Low Logic State

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted, specifications apply for $0 \leqslant T_A \leqslant 70^{\circ}C$ and $4.75\ V \leqslant V_{CC} \leqslant 5.25\ V$.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Receiver Input Threshold Voltage – High Logic State<br>($V_{IL(DA)} = 0.8\ V$, $I_{OL} = 16\ mA$, $V_{OL} \leqslant 0.4\ V$) | $V_{ILH(R)}$ | 1.80 | 2.25 | 2.50 | V |
| Receiver Input Threshold Voltage – Low Logic State<br>($V_{IL(DA)} = 0.8\ V$, $I_{OH} = -400\ \mu A$, $V_{OH} \geqslant 2.4\ V$) | $V_{IHL(R)}$ | 1.05 | 1.30 | 1.55 | V |
| Receiver Input Current<br>($V_{I(R)} = 4.0\ V$, $V_{CC} = 5.25\ V$)<br>($V_{I(R)} = 4.0\ V$, $V_{CC} = 0\ V$) | $I_{I(R)}$ | <br>–<br>– | <br>15<br>1.0 | <br>50<br>50 | µA |
| Disable Input Voltage – High Logic State<br>($V_{I(R)} = 0.5\ V$, $V_{OL} \leqslant 0.4\ V$, $I_{OL} = 16\ mA$) | $V_{IH(DA)}$ | 2.0 | – | – | V |
| Disable Input Voltage – Low Logic State<br>($V_{I(R)} = 0.5\ V$, $V_{OH} \geqslant 2.4\ V$, $I_{OH} = -400\ \mu A$) | $V_{IL(DA)}$ | – | – | 0.8 | V |
| Output Voltage – High Logic State<br>($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0.8\ V$, $I_{OH} = -400\ \mu A$) | $V_{OH}$ | 2.4 | – | – | V |
| Output Voltage – Low Logic State<br>($V_{I(R)} = 4.0\ V$, $V_{IL(DA)} = 0.8\ V$, $I_{OL} = 16\ mA$) | $V_{OL}$ | – | 0.25 | 0.4 | V |
| Disable Input Current – High Logic State<br>($V_{IH(DA)} = 2.4\ V$)<br>($V_{IH(DA)} = 5.5\ V$) | $I_{IH(DA)}$ | <br>–<br>– | <br>–<br>– | <br>80<br>2.0 | <br>µA<br>mA |
| Disable Input Current – Low Logic State<br>($V_{I(R)} = 4.0\ V$, $V_{IL(DA)} = 0.4\ V$) | $I_{IL(DA)}$ | – | – | -3.2 | mA |
| Output Short Circuit Current<br>($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0\ V$, $V_{CC} = 5.25\ V$) | $I_{OS}$ | -18 | – | -55 | mA |
| Power Supply Current<br>($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0\ V$) | $I_{CC}$ | – | 45 | 65 | mA |
| Input Clamp Diode Voltage<br>($I_{I(R)} = -12\ mA$, $I_{I(DA)} = -12\ mA$, | $V_I$ | – | -1.0 | -1.5 | V |

**SWITCHING CHARACTERISTICS** ($T_A = 25^{\circ}C$, $V_{CC} = 5.0\ V$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Time from Receiver Input to High Logic State Output | $t_{PLH(R)}$ | – | 20 | 30 | ns |
| Propagation Delay Time from Receiver Input to Low Logic State Output | $t_{PHL(R)}$ | – | 18 | 30 | ns |
| Propagation Delay Time from Disable Input to High Logic State Output | $t_{PLH(DA)}$ | – | 9.0 | 15 | ns |
| Propagation Delay Time from Disable Input to Low Logic State Output | $t_{PHL(DA)}$ | – | 4.0 | 15 | ns |

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

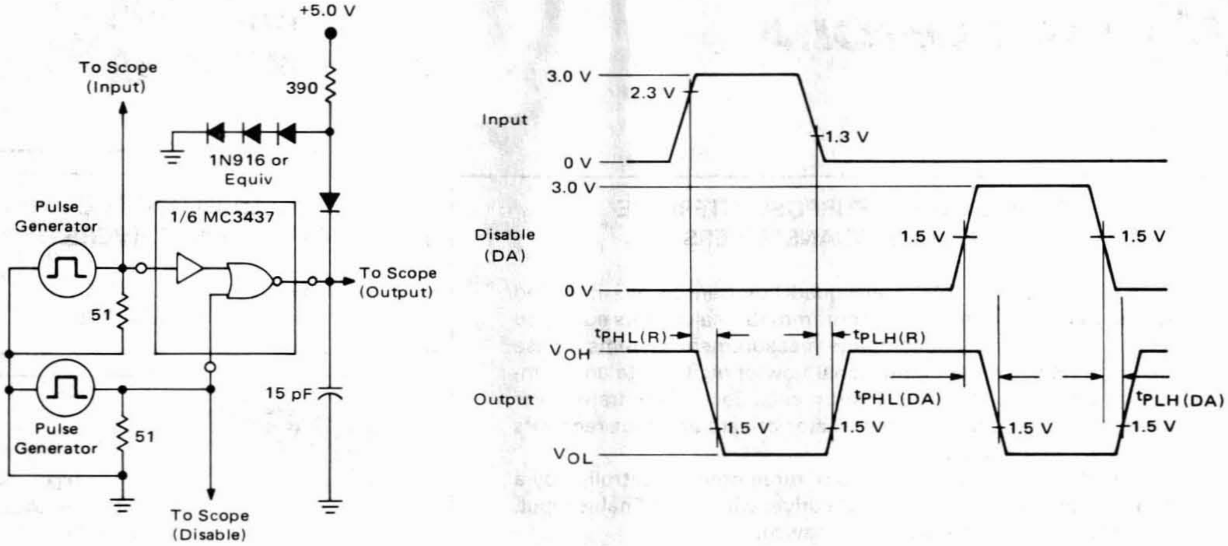
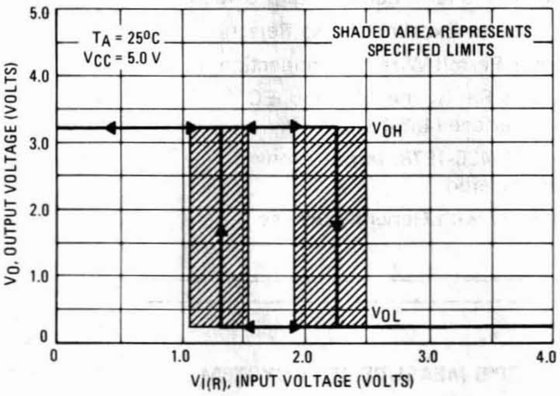
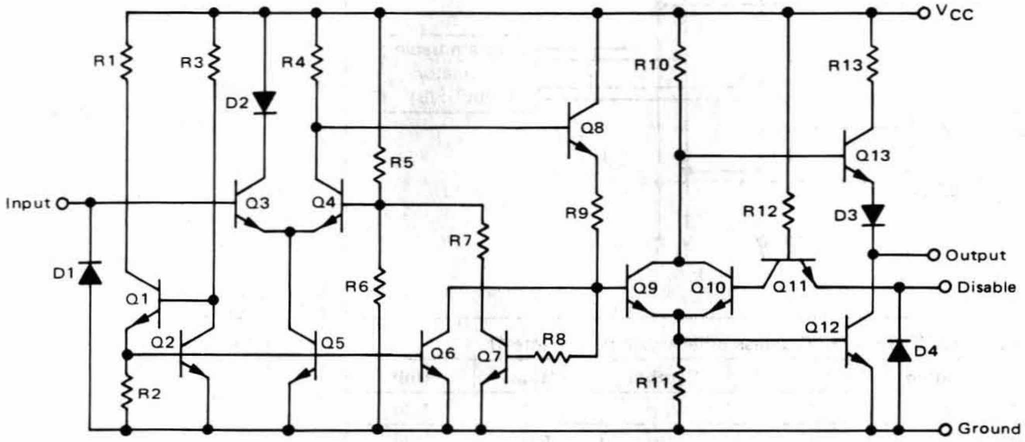

+5.0 V
To Scope
(Input)
390
1N916 or
Equiv
Pulse
Generator
1/6 MC3437
To Scope
(Output)
51
15 pF
Pulse
Generator
51
To Scope
(Disable)
3.0 V
2.3 V
Input
1.3 V
0 V
3.0 V
Disable
(DA)
1.5 V
1.5 V
0 V
$t_{PHL(R)}$
$t_{PLH(R)}$
$V_{OH}$
Output
$t_{PHL(DA)}$
$t_{PLH(DA)}$
1.5 V
1.5 V
1.5 V
1.5 V
$V_{OL}$

FIGURE 3 – TYPICAL HYSTERESIS



REPRESENTATIVE CIRCUIT SCHEMATIC
(1/6 Shown)


$V_{CC}$
R1
R3
R4
D2
R10
R13
Q8
R5
Q13
Input
Q3
Q4
R9
R12
D3
R7
Output
D1
R6
Q9
Q10
Q11
Disable
Q1
Q2
Q5
Q6
Q7
R8
Q12
D4
R2
R11
Ground

**MOTOROLA**

# MC3440A
# MC3441A

## QUAD GENERAL-PURPOSE INTERFACE BUS (GPIB) TRANSCEIVERS

The MC3440A, MC3441A are quad bus transceivers intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. These transceivers allow the bidirectional flow of digital data and commands between the various instruments. Each of the transceiver versions provides four open-collector drivers and four receivers featuring input hysteresis.

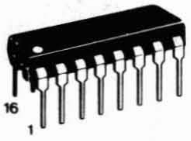
The MC3440A version consists of three drivers controlled by a common Enable input and a single driver without an Enable input. Terminations are provided in the device.

The MC3441A differs in that all four drivers are controlled by the common Enable input. Again, the terminations are provided.

- Receiver Input Hysteresis Provides Excellent Noise Rejection
- Open-Collector Driver Outputs Permit Wire-OR Connection
- Tailored to Meet the Standards Set by the IEEE and IEC Committees on Instrument Interface (488-1978)
- Terminations comply with IEEE 488-1978; terminations removed when device is unpowered
- Provides Electrical Compatibility with General-Purpose Interface Bus

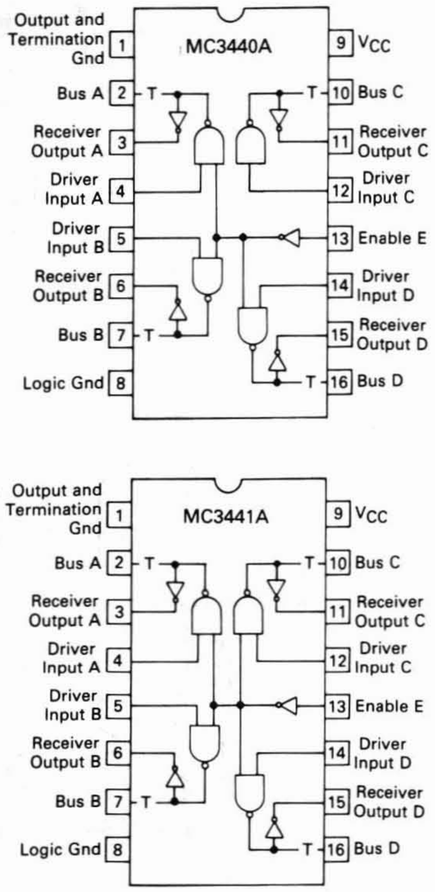
## QUAD INTERFACE BUS TRANSCEIVERS

**SILICON MONOLITHIC INTEGRATED CIRCUITS**



**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

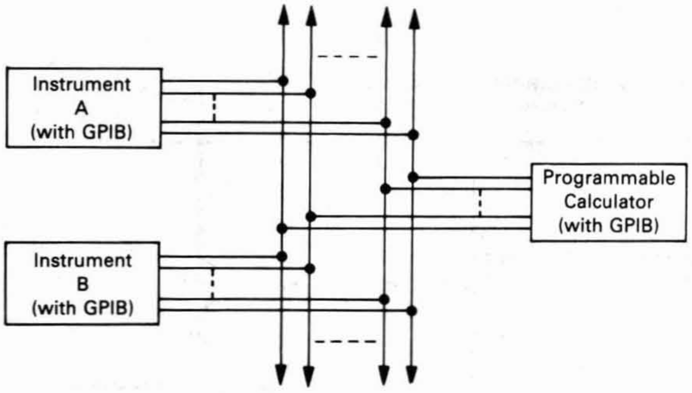
### PIN CONNECTIONS



MC3440A
Output and Termination Gnd 1
Bus A 2
Receiver Output A 3
Driver Input A 4
Driver Input B 5
Receiver Output B 6
Bus B 7
Logic Gnd 8
9 VCC
10 Bus C
11 Receiver Output C
12 Driver Input C
13 Enable E
14 Driver Input D
15 Receiver Output D
16 Bus D
T
MC3441A
Output and Termination Gnd 1
Bus A 2
Receiver Output A 3
Driver Input A 4
Driver Input B 5
Receiver Output B 6
Bus B 7
Logic Gnd 8
9 VCC
10 Bus C
11 Receiver Output C
12 Driver Input C
13 Enable E
14 Driver Input D
15 Receiver Output D
16 Bus D
T

— T — = Bus Termination

### TYPICAL APPLICATION — GPIB MEASUREMENT SYSTEM



Instrument A (with GPIB)
Instrument B (with GPIB)
Programmable Calculator (with GPIB)

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted.) (Note 1)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 7.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Driver Output Current | $I_{O(D)}$ | 150 | mA |
| Power Dissipation (Package Limitation)<br>Derate above 25°C | $P_D$ | 830<br>6.7 | mW<br>mW/°C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

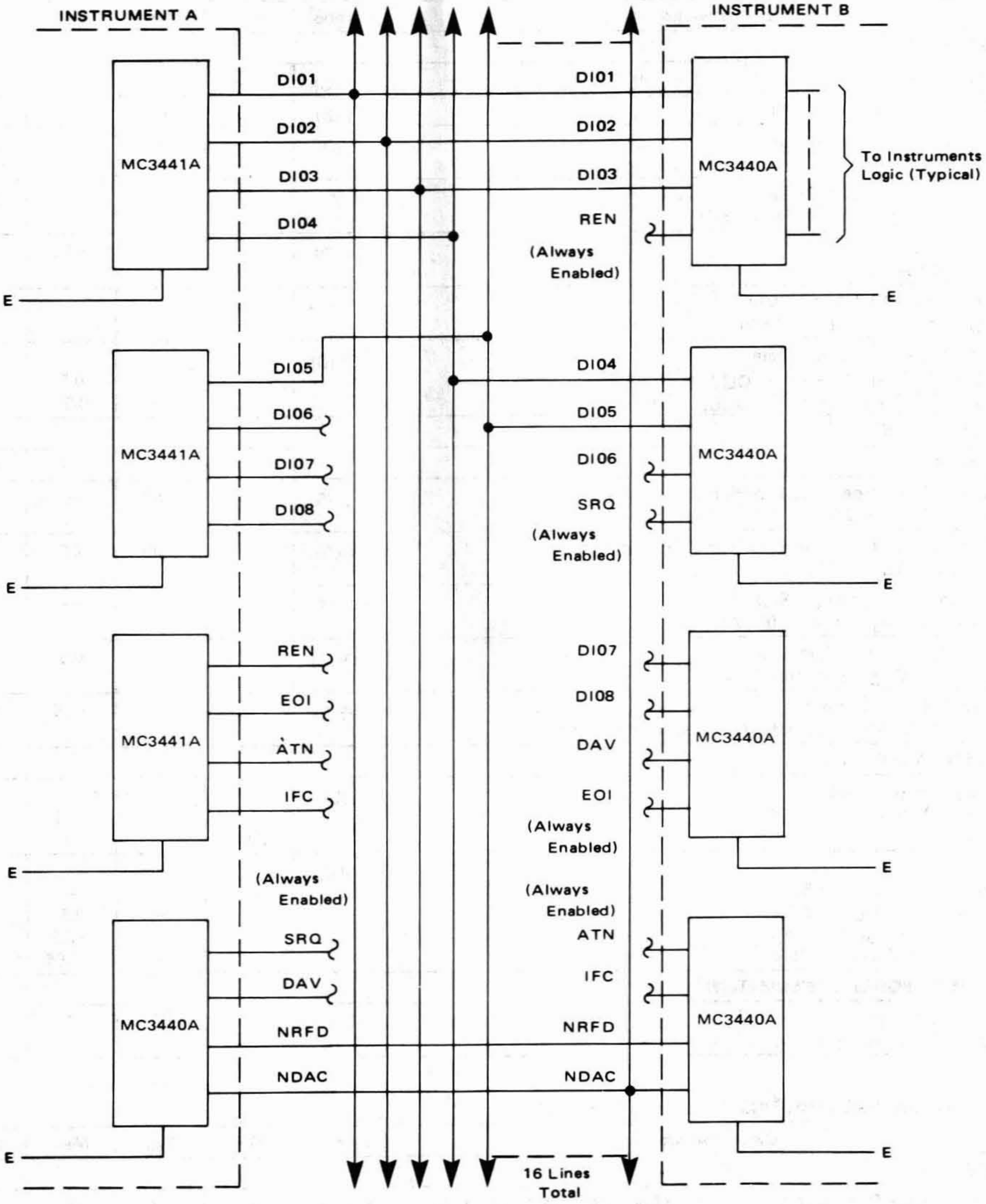
**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted, 4.5 V ≤ $V_{CC}$ ≤ 5.5 V and 0 ≤ $T_A$ ≤ 70°C, typical values are at $T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **DRIVER PORTION** | | | | | |
| Input Voltage — High Logic State | $V_{IH(D)}$ | 2.0 | — | — | V |
| Input Voltage — Low Logic State | $V_{IL(D)}$ | — | — | 0.8 | V |
| Input Current — High Logic State<br>($V_{IH}$ = 2.4 V) | $I_{IH(D)}$ | — | — | 40 | μA |
| Input Current — Low Logic State<br>($V_{IL}$ = 0.4 V, $V_{CC}$ = 5.0 V, $T_A$ = 25°C) | $I_{IL(D)}$ | | | −0.25 | mA |
| Input Clamp Voltage<br>($I_{IK}$ = −12 mA) | $V_{IK(D)}$ | — | — | −1.5 | V |
| Output Voltage — High Logic State<br>($V_{IH(S)}$ = 2.4 V or $V_{IL(D)}$ = 0.8 V) | $V_{OH(D)}$ | 2.5 | — | — | V |
| Output Voltage — Low Logic State<br>($V_{IH(S)}$ = 2.0 V, $V_{IL(E)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA)<br>($V_{IH(D)}$ = 2.0 V, $V_{IL(E)}$ = 0.8 V, $I_{OL(D)}$ = 100 mA) | $V_{OL(D)}$ | <br>—<br>— | <br>—<br>— | <br>0.5<br>0.80 | V |
| **RECEIVER PORTION** | | | | | |
| Input Hysteresis | — | 400 | 580 | — | mV |
| Input Threshold Voltage — Low to High Output Logic State<br>($V_{CC}$ = 5.0 V, $T_A$ = 25°C) | $V_{ILH(R)}$ | 0.8 | 0.98 | — | V |
| Input Threshold Voltage — High to Low Output Logic State<br>($V_{CC}$ = 5.0 V, $T_A$ = 25°C) | $V_{IHL(R)}$ | — | 1.56 | 2.0 | V |
| Output Voltage — High Logic State<br>($V_{IL(R)}$ = 0.8 V, $I_{OH(R)}$ = −400 μA) | $V_{OH(R)}$ | 2.4 | — | — | V |
| Output Voltage — Low Logic State<br>($V_{IH(R)}$ = 2.0 V, $I_{OL(R)}$ = 16 mA) | $V_{OL(R)}$ | — | — | 0.5 | V |
| Output Short-Circuit Current<br>($V_{IL(R)}$ = 0.8 V) (Only one output may be shorted at a time) | $I_{OS(R)}$ | −20 | — | −55 | mA |
| **BUS TERMINATION PORTION** | | | | | |
| Bus Voltage ($V_{IL(D)}$ = 0.8 V)<br>($I_{BUS}$ = −12 mA)<br>(No Load) | $V_{BUS}$ | <br>—<br>2.50 | <br>—<br>— | <br>−1.5<br>3.70 | V |
| Bus Current<br>($V_{IL(D)}$ = 0.8 V, $V_{BUS}$ ≥ 5.0 V)<br>($V_{IL(D)}$ = 0.8 V, $V_{BUS}$ ≤ 5.5 V)<br>($V_{IL(D)}$ = 0.8 V, $V_{BUS}$ = 0.5 V)<br>($V_{CC}$ = 0, 0 ≤ $V_{BUS}$ ≤ 2.75 V) | $I_{BUS}$ | <br>0.7<br>—<br>−1.3<br>— | <br>—<br>—<br>—<br>— | <br>—<br>2.5<br>−3.2<br>+0.04 | mA |
| **TOTAL DEVICE POWER CONSUMPTION** | | | | | |
| Power Supply Current<br>($V_{IH(D)}$ = 2.4 V, $V_{IL(E)}$ = 0 V) | $I_{CC}$ | 30 | 56 | 75 | mA |

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $T_A$ = 25°C)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **DRIVER PORTION** | | | | | |
| Propagation Delay Time from Driver Input to Low Logic State Bus Output | $t_{PHL(D)}$ | — | 13 | 30 | ns |
| Propagation Delay Time from Driver Input to High Logic State Bus Output | $t_{PLH(D)}$ | — | 17 | 30 | ns |
| Propagation Delay Time from Enable Input to Low Logic State Bus Output | $t_{PHL(E)}$ | — | 25 | 40 | ns |
| Propagation Delay Time from Enable Input to High Logic State Bus Output | $t_{PLH(E)}$ | — | 25 | 40 | ns |
| **RECEIVER PORTION** | | | | | |
| Propagation Delay Time from Bus Input to High Logic State Receiver Output | $t_{PLH(R)}$ | — | 15 | 30 | ns |
| Propagation Delay Time from Bus Input to Low Logic State Receiver Output | $t_{PHL(R)}$ | — | 15 | 30 | ns |

## GENERAL PURPOSE INTERFACE BUS APPLICATION


INSTRUMENT A
INSTRUMENT B
MC3441A
MC3441A
MC3441A
MC3440A
MC3440A
MC3440A
MC3440A
MC3440A
DI01
DI02
DI03
DI04
DI05
DI06
DI07
DI08
REN
EOI
ATN
IFC
SRQ
DAV
NRFD
NDAC
(Always Enabled)
To Instruments Logic (Typical)
E
16 Lines Total

GPIB SIGNALS:

8 Line Data Bus: DI01 – DI08

5 General Interrupt Transfer Control Bus:
- REN – Remote Enable
- SRQ – Service Request
- EOI – End or Identify
- ATN – Attention
- IFC – Interface Clear

3 Data Byte Transfer Control Bus
- DAV – Data Valid
- NRFD – Not Ready for Data
- NDAC – Not Data Accepted

16 Total Signal Lines

**FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT**

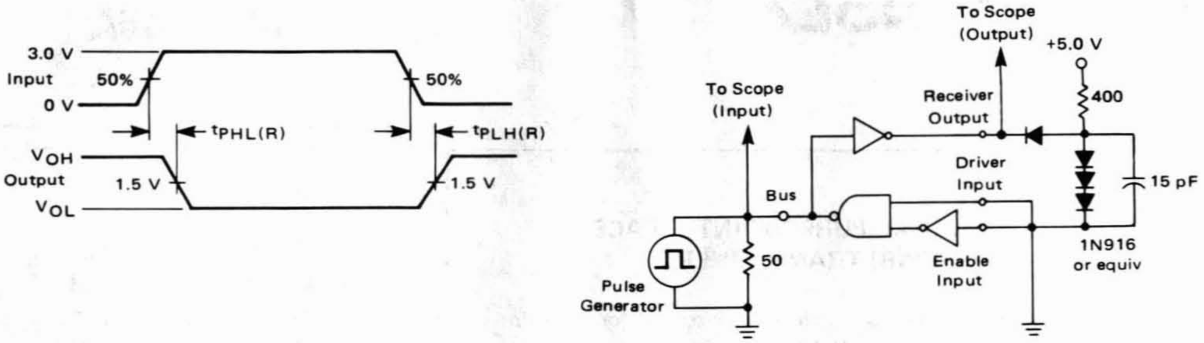

3.0 V
Input
50%
50%
0 V
tPHL(R)
tPLH(R)
VOH
Output
1.5 V
1.5 V
VOL
To Scope (Output)
+5.0 V
To Scope (Input)
Receiver Output
400
Driver Input
15 pF
Bus
50
Enable Input
1N916 or equiv
Pulse Generator

**FIGURE 2 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)**

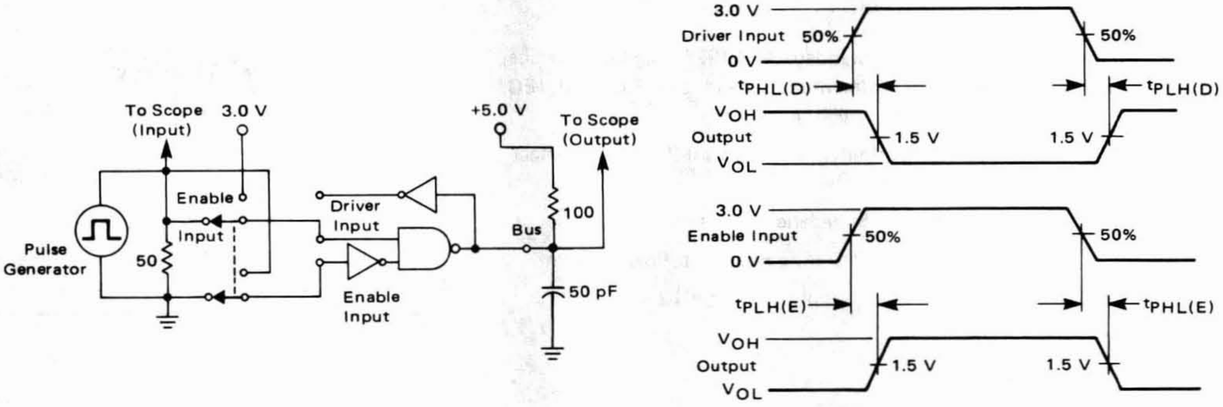
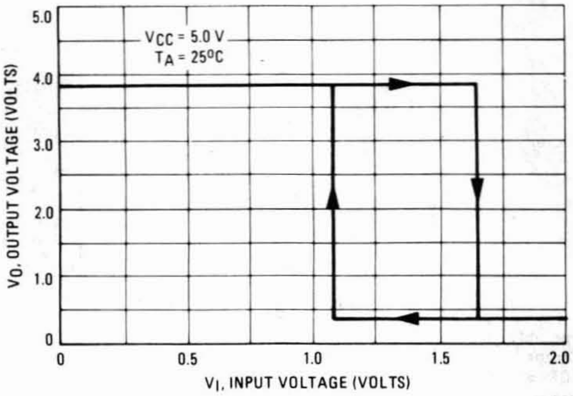

3.0 V
Driver Input
50%
50%
0 V
tPHL(D)
tPLH(D)
VOH
Output
1.5 V
1.5 V
VOL
3.0 V
Enable Input
50%
50%
0 V
tPLH(E)
tPHL(E)
VOH
Output
1.5 V
1.5 V
VOL
To Scope (Input)
3.0 V
+5.0 V
To Scope (Output)
Enable
Driver Input
Input
100
Bus
Pulse Generator
50
50 pF
Enable Input

**FIGURE 3 — TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS**



**MOTOROLA**

# MC3446A

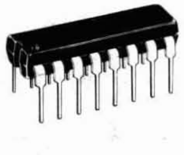
## QUAD GENERAL-PURPOSE INTERFACE BUS (GPIB) TRANSCEIVER

The MC3446A is a quad bus transceiver intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. This transceiver allows the bidirectional flow of digital data and commands between the various instruments. The transceiver provides four open-collector drivers and four receivers featuring hysteresis.

- Tailored to Meet the IEEE Standard 488-1978 (Digital Interface for Programmable Instrumentation) and the Proposed IEC Standard on Instrument Interface
- Provides Electrical Compatibility with General-Purpose Interface Bus (GPIB)
- MOS Compatible with High Impedance Inputs
- Driver Output Guaranteed Off During Power Up/Power Down
- Low Power — Average Power Supply Current = 12 mA
- Terminations Provided

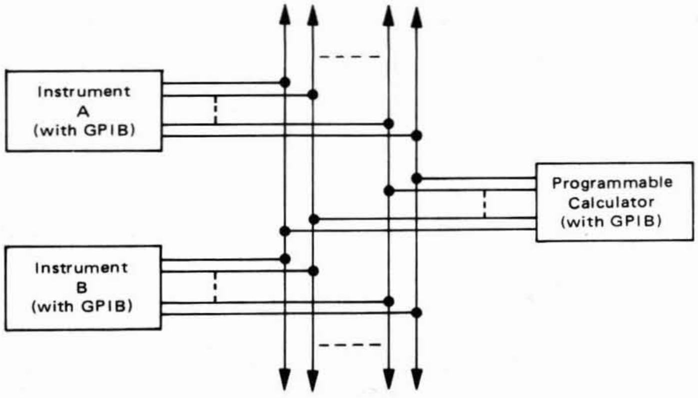
## QUAD INTERFACE BUS TRANSCEIVER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



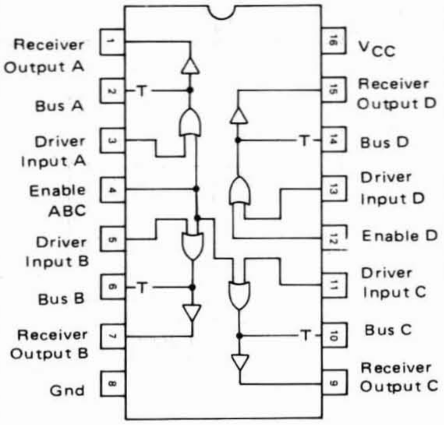
**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

**TYPICAL MEASUREMENT SYSTEM APPLICATION**


Instrument A (with GPIB)
Programmable Calculator (with GPIB)
Instrument B (with GPIB)

16 Lines Total

**PIN CONNECTIONS**


Receiver Output A
Bus A
Driver Input A
Enable ABC
Driver Input B
Bus B
Receiver Output B
Gnd
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VCC
Receiver Output D
Bus D
Driver Input D
Enable D
Driver Input C
Bus C
Receiver Output C
T
T
T
T

— T — = Bus Termination

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 7.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Driver Output Current | $I_{O(D)}$ | 150 | mA |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS**
(Unless otherwise noted, 4.5 V ≤ $V_{CC}$ ≤ 5.5 V and 0 ≤ $T_A$ ≤ 70°C, typical values are at $T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **DRIVER PORTION** | | | | | |
| Input Voltage – High Logic State | $V_{IH(D)}$ | 2.0 | – | – | V |
| Input Voltage – Low Logic State | $V_{IL(D)}$ | – | – | 0.8 | V |
| Input Current – High Logic State ($V_{IH}$ = 2.4 V) | $I_{IH(D)}$ | – | 5.0 | 40 | µA |
| Input Current – Low Logic State ($V_{IL}$ = 0.4 V, $V_{CC}$ = 5.0 V, $T_A$ = 25°C) | $I_{IL(D)}$ | – | -0.2 | -0.25 | mA |
| Input Clamp Voltage ($I_{IK}$ = -12 mA) | $V_{IK(D)}$ | – | – | -1.5 | V |
| Output Voltage – High Logic State (1) ($V_{IH(S)}$ = 2.4 V or $V_{IH(D)}$ = 2.0 V) | $V_{OH(D)}$ | 2.5 | 3.3 | 3.7 | V |
| Output Voltage – Low Logic State ($V_{IL(S)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA) | $V_{OL(D)}$ | – | – | 0.5 | |
| Input Breakdown Current ($V_{I(D)}$ = 5.5 V) | $I_{IB(D)}$ | – | – | 1.0 | mA |
| **RECEIVER PORTION** | | | | | |
| Input Hysteresis | – | 400 | 625 | – | mV |
| Input Threshold Voltage – Low to High Output Logic State | $V_{ILH(R)}$ | – | 1.66 | 2.0 | V |
| Input Threshold Voltage – High to Low Output Logic State | $V_{IHL(R)}$ | 0.8 | 1.03 | – | V |
| Output Voltage – High Logic State ($V_{IH(R)}$ = 2.0 V, $I_{OH(R)}$ = -400 µA) | $V_{OH(R)}$ | 2.4 | – | – | V |
| Output Voltage – Low Logic State ($V_{IL(R)}$ = 0.8 V, $I_{OL(R)}$ = 8.0 mA) | $V_{OL(R)}$ | – | – | 0.5 | V |
| Output Short-Circuit Current ($V_{IH(R)}$ = 2.0 V) (Only one output may be shorted at a time) | $I_{OS(R)}$ | 4.0 | – | 14 | mA |
| **BUS LOAD CHARACTERISTICS** | | | | | |
| Bus Voltage ($V_{IH(E)}$ = 2.4 V) | $V_{(BUS)}$ | 2.5 | 3.3 | 3.7 | V |
| ($I_{BUS}$ = -12 mA) | | – | – | -1.5 | |
| Bus Current ($V_{IH(O)}$= 2.4 V, $V_{BUS}$ ≥ 5.0 V) | $I_{(BUS)}$ | 0.7 | – | – | mA |
| ($V_{IH(D)}$ = 2.4 V, $V_{BUS}$ = 0.5 V) | | -1.3 | – | -3.2 | |
| ($V_{BUS}$ ≤ 5.5 V) | | – | – | 2.5 | |
| ($V_{CC}$ = 0, 0 V ≤ $V_{BUS}$ ≤ 2.75 V) | | – | – | 0.04 | |
| **TOTAL DEVICE POWER CONSUMPTION** | | | | | |
| Power Supply Current | $I_{CC}$ | | | | mA |
| (All Drivers OFF) | | – | 12 | 19 | |
| (All Drivers ON) | | – | 32 | 40 | |

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $T_A$ = 25°C)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **DRIVER PORTION** | | | | | |
| Propagation Delay Time from Driver Input to Low Logic State Bus Output | $t_{PHL(D)}$ | – | – | 50 | ns |
| Propagation Delay Time from Driver Input to High Logic State Bus Output | $t_{PLH(D)}$ | – | – | 40 | ns |
| Propagation Delay Time from Enable Input to Low Logic State Bus Output | $t_{PHL(E)}$ | – | – | 50 | ns |
| Propagation Delay Time from Enable Input to High Logic State Bus Output | $t_{PLH(E)}$ | – | – | 50 | ns |
| **RECEIVER PORTION** | | | | | |
| Propagation Delay Time from Bus Input to High Logic State Receiver Output | $t_{PLH(R)}$ | – | – | 50 | ns |
| Propagation Delay Time from Bus Input to Low Logic State Receiver Output | $t_{PHL(R)}$ | – | – | 40 | ns |

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

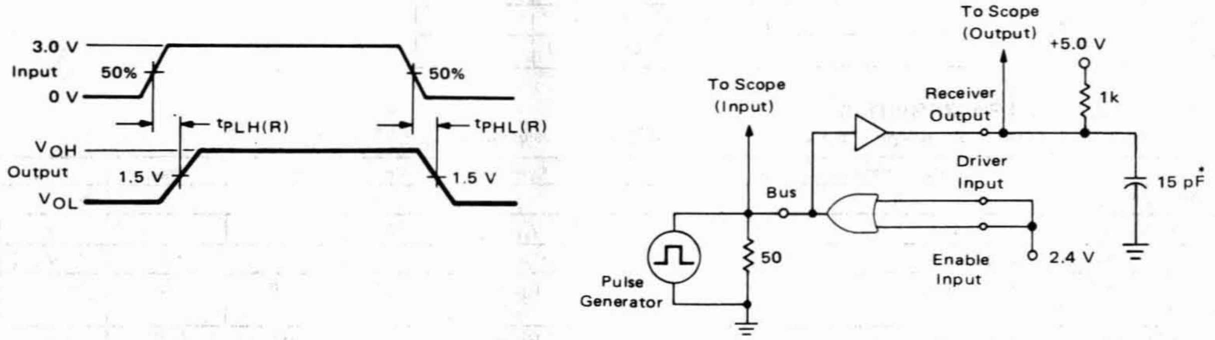
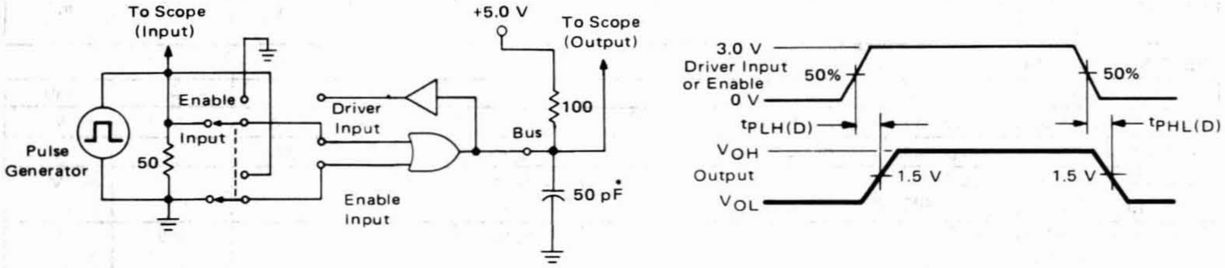

3.0 V
Input
50%
0 V
50%
tPLH(R)
tPHL(R)
VOH
Output
1.5 V
1.5 V
VOL
To Scope (Output)
+5.0 V
To Scope (Input)
Receiver Output
1k
Driver Input
15 pF*
Bus
50
Pulse Generator
Enable Input
2.4 V

FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)


To Scope (Input)
Pulse Generator
Enable
Input
50
Driver Input
Enable Input
+5.0 V
To Scope (Output)
100
Bus
50 pF*
3.0 V
Driver Input or Enable
50%
0 V
50%
tPLH(D)
tPHL(D)
VOH
Output
1.5 V
1.5 V
VOL

* Includes Probe and Jig Capacitance

FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

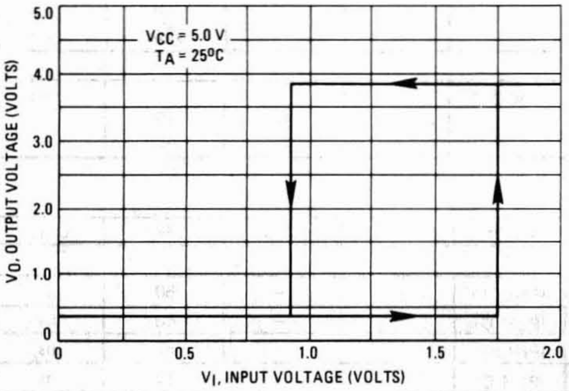
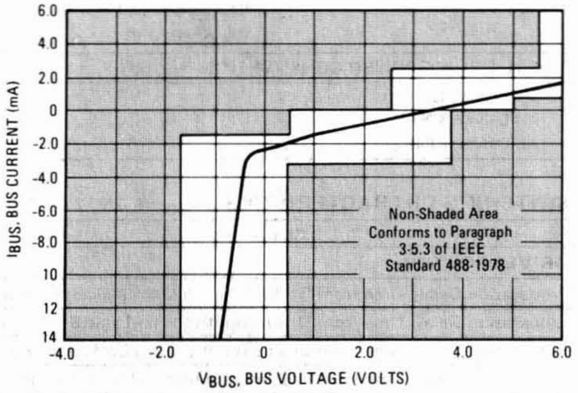


FIGURE 4 – TYPICAL BUS LOAD LINE



**MOTOROLA**

# MC3447

## OCTAL BIDIRECTIONAL BUS TRANSCEIVER WITH TERMINATION NETWORKS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

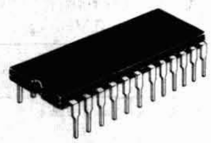
## BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

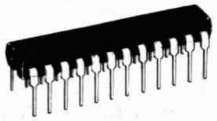
Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Low Power – Average Power Supply Current = 30 mA Listening
  75 mA Talking
- Eight Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis – 600 mV (Typ)
- Fast Propagation Times – 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output with Terminations
- Power Up/Power Down Protection (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power is Removed From Device
- Required Termination Characteristics Provided

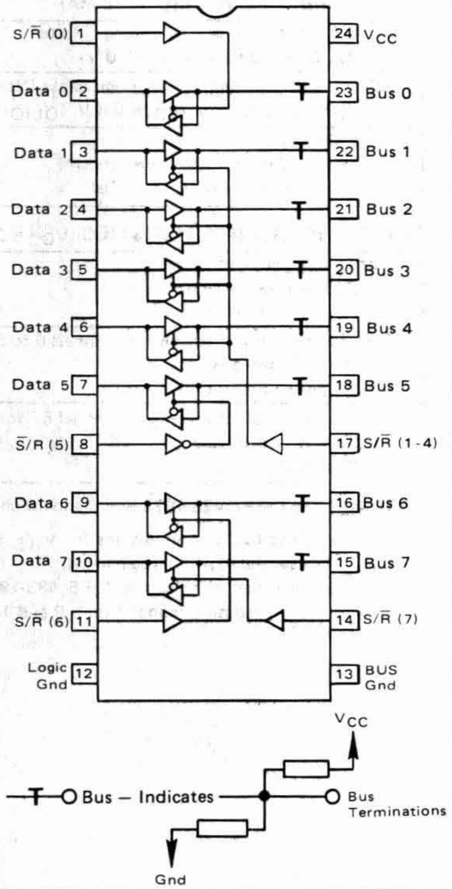


**L SUFFIX**
CERAMIC PACKAGE
CASE 623-05



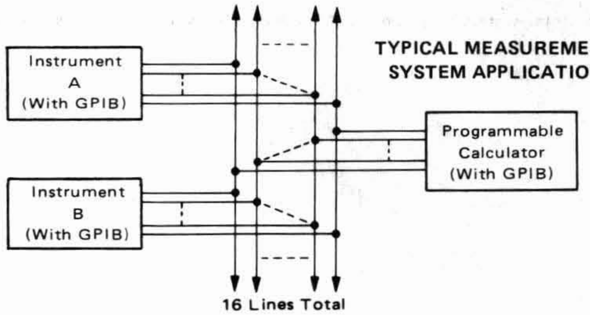
**P3 SUFFIX**
PLASTIC PACKAGE
CASE 724-02

**PIN ASSIGNMENTS**


S/R̄ (0) 1
24 VCC
Data 0 2
23 Bus 0
Data 1 3
22 Bus 1
Data 2 4
21 Bus 2
Data 3 5
20 Bus 3
Data 4 6
19 Bus 4
Data 5 7
18 Bus 5
S̄/R (5) 8
17 S/R̄ (1-4)
Data 6 9
16 Bus 6
Data 7 10
15 Bus 7
S/R̄ (6) 11
14 S/R̄ (7)
Logic Gnd 12
13 BUS Gnd
VCC
Bus – Indicates
Bus Terminations
Gnd

**MAXIMUM RATINGS** ($T_A = 25^{\circ}C$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 7.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Driver Output Current | $I_{O(D)}$ | 150 | mA |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |


Instrument A (With GPIB)
Programmable Calculator (With GPIB)
Instrument B (With GPIB)
16 Lines Total

**TYPICAL MEASUREMENT SYSTEM APPLICATION**

## ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.50 V $\leq V_{CC} \leq$ 5.50 V and 0 $\leq T_A \leq$ 70°C; typical values are at $T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Characteristic – Note 2 | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Bus Voltage<br>(Bus Pin Open)($V_{I(S/\overline{R})}$ = 0.8 V)<br>($I_{(Bus)}$ = −12 mA) | $V_{(Bus)}$<br>$V_{IC(Bus)}$ | 2.5<br>– | –<br>– | 3.7<br>−1.5 | V |
| Bus Current<br>(5.0 V $\leq V_{(Bus)} \leq$ 5.5 V)<br>($V_{(Bus)}$ = 0.5 V)<br>($V_{CC}$ = 0 V, 0 V $\leq V_{(Bus)} \leq$ 2.75 V) | $I_{(Bus)}$ | 0.7<br>−1.3<br>– | –<br>–<br>– | 2.5<br>−3.2<br>+0.04 | mA |
| Receiver Input Hysteresis<br>($V_{I(S/\overline{R})}$ = 0.8 V) | – | 400 | 600 | – | mV |
| Receiver Input Threshold<br>($V_{I(S/\overline{R})}$ = 0.8 V) Low to High<br>High to Low | $V_{ILH(R)}$<br>$V_{IHL(R)}$ | –<br>0.8 | 1.6<br>1.0 | 2.0<br>– | V |
| Receiver Output Voltage – High Logic State<br>($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OH(R)}$ = −200 µA, $V_{(Bus)}$ = 2.0 V) | $V_{OH(R)}$ | 2.4 | – | – | V |
| Receiver Output Voltage – Low Logic State<br>($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OL(R)}$ = 4.0 mA, ($V_{(Bus)}$ = 0.8 V | $V_{OL(R)}$ | – | – | 0.5 | V |
| Receiver Output Short Circuit Current<br>($V_{I(S/\overline{R})}$ = 0.8 V, $V_{(Bus)}$ = 2.0 V) | $I_{OS(R)}$ | −4.0 | – | −20 | mA |
| Driver Input Voltage – High Logic State<br>($V_{I(S/\overline{R})}$ = 2.0 V) | $V_{IH(D)}$ | 2.0 | – | – | V |
| Driver Input Voltage – Low Logic State<br>($V_{I(S/\overline{R})}$ = 2.0 V) | $V_{IL(D)}$ | – | – | 0.8 | V |
| Driver Input Current – Data Pins<br>($V_{I(S/\overline{R})}$ = 2.0 V)<br>(0.5 $\leq V_{I(D)} \leq$ 2.7 V)<br>($V_{I(D)}$ = 5.5 V) | $I_{I(D)}$<br>$I_{IB(D)}$ | −100<br>– | –<br>– | 40<br>200 | µA |
| Input Current – Send/Receive<br>(0.5 $\leq V_{I(S/R)} \leq$ 2.7 V)<br>($V_{I(S/\overline{R})}$ = 5.5 V) | $I_{I(S/\overline{R})}$<br>$I_{IB(S/\overline{R})}$ | −250<br>– | –<br>– | 20<br>100 | µA |
| Driver Input Clamp Voltage<br>($V_{I(S/\overline{R})}$ = 2.0 V, $I_{IC(D)}$ = −18 mA) | $V_{IC(D)}$ | – | – | −1.5 | V |
| Driver Output Voltage – High Logic State<br>($V_{IS/\overline{R})}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V) | $V_{OH(D)}$ | 2.5 | – | – | V |
| Driver Output Voltage – Low Logic State (Note 1)<br>($V_{I(S/\overline{R})}$ = 2.0 V, $V_{IL(D)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA) | $V_{OL(D)}$ | – | – | 0.5 | V |
| Power Supply Current<br>(Listening Mode – All Receivers On)<br>(Talking Mode – All Drivers On) | $I_{CCL}$<br>$I_{CCH}$ | –<br>– | 30<br>75 | 45<br>95 | mA |

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $T_A$ = 25°C unless otherwise noted)

| | | | | | |
|---|---|---|---|---|---|
| Propagation Delay of Driver<br>(Output Low to High)<br>(Output High to Low) | $t_{PLH(D)}$<br>$t_{PHL(D)}$ | –<br>– | 7.0<br>16 | 15<br>30 | ns |
| Propagation Delay of Receiver (Channels 0 to 5, 7)<br>(Output Low to High)<br>(Output High to Low) | $t_{PLH(R)}$<br>$t_{PHL(R)}$ | –<br>– | 28<br>15 | 50<br>30 | ns |
| Propagation Delay of Receiver (Channel 6, Note 3)<br>(Output Low to High)<br>(Output High to Low) | $t_{PLH(R)}$<br>$t_{PHL(R)}$ | –<br>– | 17<br>12 | 30<br>22 | ns |

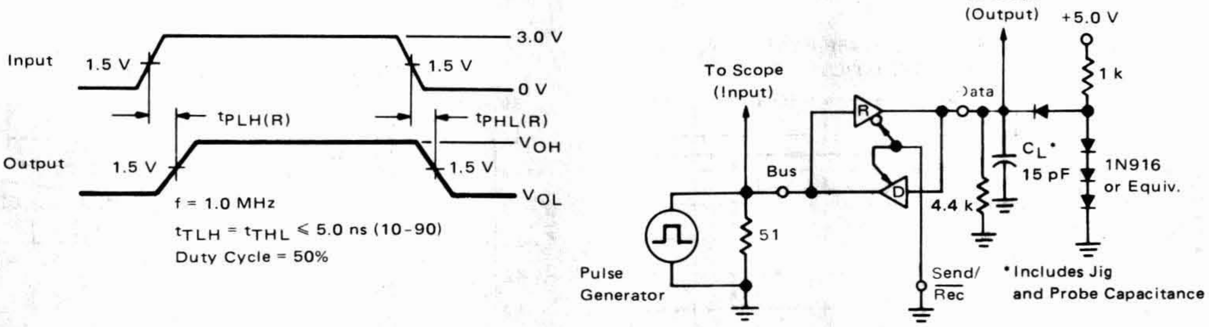
NOTES:
1. The IEEE 488-1978 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.
2. Specified test conditions for $V_{I(S/\overline{R})}$ are 0.8 V (Low) and 2.0 V (High). Where $V_{I(S/\overline{R})}$ is specified as a test condition, $V_{I(\overline{S}/R)}$ uses the opposite logic levels.
3. In order to meet the IEEE 488-1978 standard for total system delay on the ATN and EOI channels, a fast receiver has been provided on Channel 6 (pins 9 and 16).

**SWITCHING CHARACTERISTICS (continued)** ($V_{CC}$ = 5.0 V, $T_A$ = 25°C unless otherwise noted)

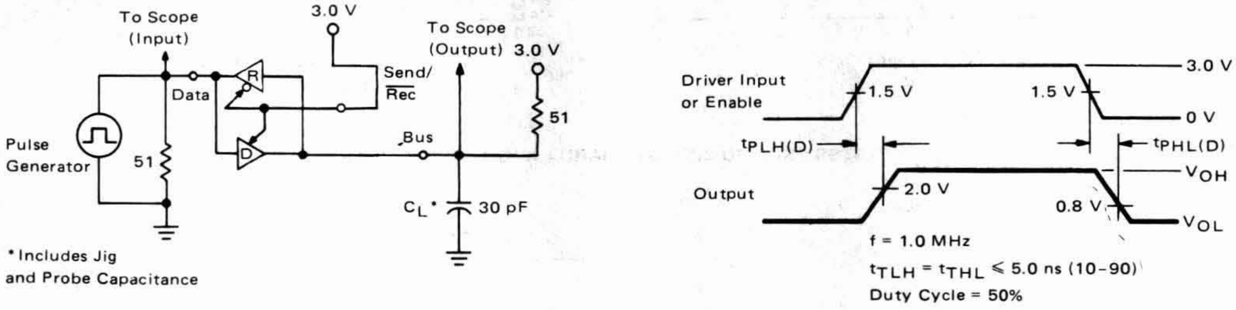
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Time – Send/Receiver to Data | | | | | ns |
| Logic High to Third State | $t_{PHZ(R)}$ | – | 15 | 30 | |
| Third State to Logic High | $t_{PZH(R)}$ | – | 15 | 30 | |
| Logic Low to Third State | $t_{PLZ(R)}$ | – | 15 | 25 | |
| Third State to Logic Low | $t_{PZL(R)}$ | – | 10 | 25 | |
| Propagation Delay Time – Send/Receiver to Bus | | | | | ns |
| Logic Low to Third State | $t_{PLZ(D)}$ | – | 13 | 25 | |
| Third State to Logic Low | $t_{PZL(D)}$ | – | 30 | 50 | |

## PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

### FIGURE 1 – BUS INPUT TO DATA OUTPUT (RECEIVER)


Input
1.5 V
3.0 V
1.5 V
0 V
$t_{PLH(R)}$
$t_{PHL(R)}$
$V_{OH}$
Output
1.5 V
1.5 V
$V_{OL}$
f = 1.0 MHz
$t_{TLH}$ = $t_{THL}$ ≤ 5.0 ns (10–90)
Duty Cycle = 50%
To Scope (Output)
+5.0 V
1 k
To Scope (Input)
Data
R
D
Bus
$C_L$*
15 pF
1N916 or Equiv.
4.4 k
51
Pulse Generator
Send/$\overline{Rec}$
*Includes Jig and Probe Capacitance

### FIGURE 2 – DATA INPUT TO BUS OUTPUT (DRIVER)


To Scope (Input)
3.0 V
To Scope (Output)
3.0 V
Data
R
Send/$\overline{Rec}$
51
Pulse Generator
51
D
Bus
$C_L$*
30 pF
*Includes Jig and Probe Capacitance
Driver Input or Enable
1.5 V
1.5 V
3.0 V
0 V
$t_{PLH(D)}$
$t_{PHL(D)}$
$V_{OH}$
Output
2.0 V
0.8 V
$V_{OL}$
f = 1.0 MHz
$t_{TLH}$ = $t_{THL}$ ≤ 5.0 ns (10–90)
Duty Cycle = 50%

### FIGURE 3 – SEND/$\overline{\text{RECEIVE}}$ INPUT TO BUS OUTPUT (DRIVER)

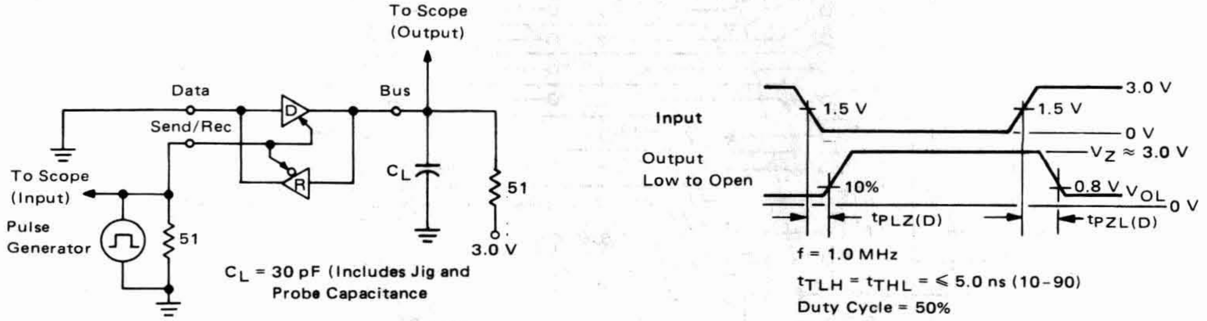
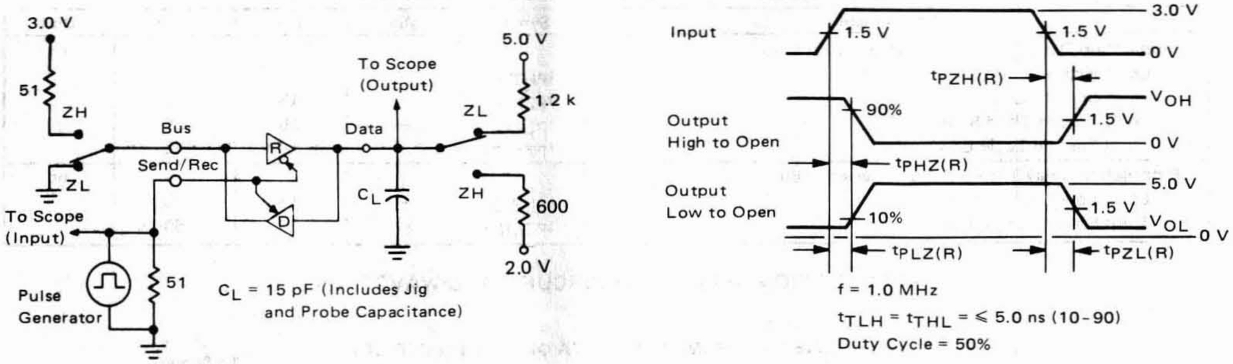

To Scope (Output)
Data
Bus
D
Send/Rec
R
$C_L$
51
To Scope (Input)
Pulse Generator
51
3.0 V
$C_L$ = 30 pF (Includes Jig and Probe Capacitance
Input
1.5 V
1.5 V
3.0 V
0 V
Output Low to Open
$V_Z$ ≈ 3.0 V
10%
0.8 V
$V_{OL}$
0 V
$t_{PLZ(D)}$
$t_{PZL(D)}$
f = 1.0 MHz
$t_{TLH}$ = $t_{THL}$ = ≤ 5.0 ns (10–90)
Duty Cycle = 50%

FIGURE 4 – SEND/$\overline{\text{RECEIVE}}$ INPUT TO DATA OUTPUT (RECEIVER)


3.0 V
51
ZH
ZL
To Scope
(Input)
Pulse
Generator
51
Bus
Send/Rec
R
D
To Scope
(Output)
Data
CL
5.0 V
ZL
1.2 k
ZH
600
2.0 V
Input
1.5 V
1.5 V
3.0 V
0 V
tPZH(R)
VOH
Output
High to Open
90%
1.5 V
0 V
tPHZ(R)
Output
Low to Open
5.0 V
1.5 V
10%
VOL
0 V
tPLZ(R)
tPZL(R)

$C_L$ = 15 pF (Includes Jig and Probe Capacitance)

f = 1.0 MHz

$t_{TLH} = t_{THL} = \leq 5.0$ ns (10–90)

Duty Cycle = 50%

FIGURE 5 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

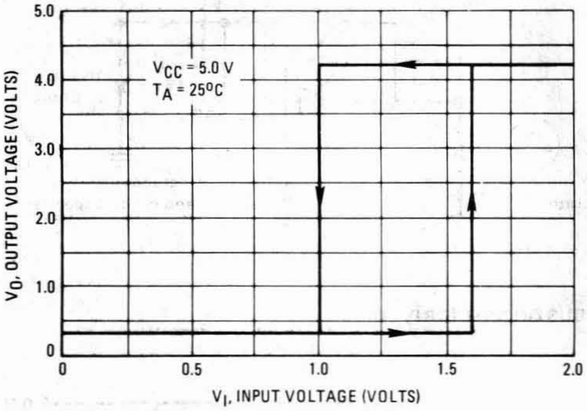


FIGURE 6 – TYPICAL BUS LOAD LINE

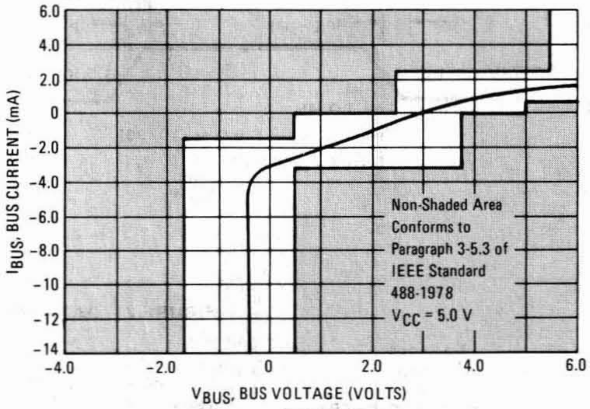


FIGURE 7 – SUGGESTED PRINTED CIRCUIT BOARD LAYOUT USING MC3447s AND MC68488

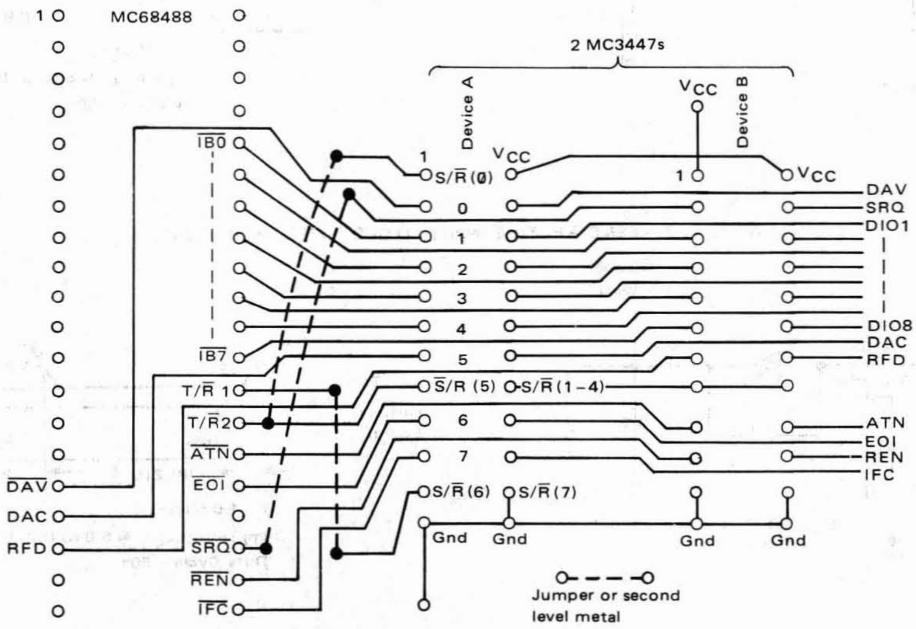
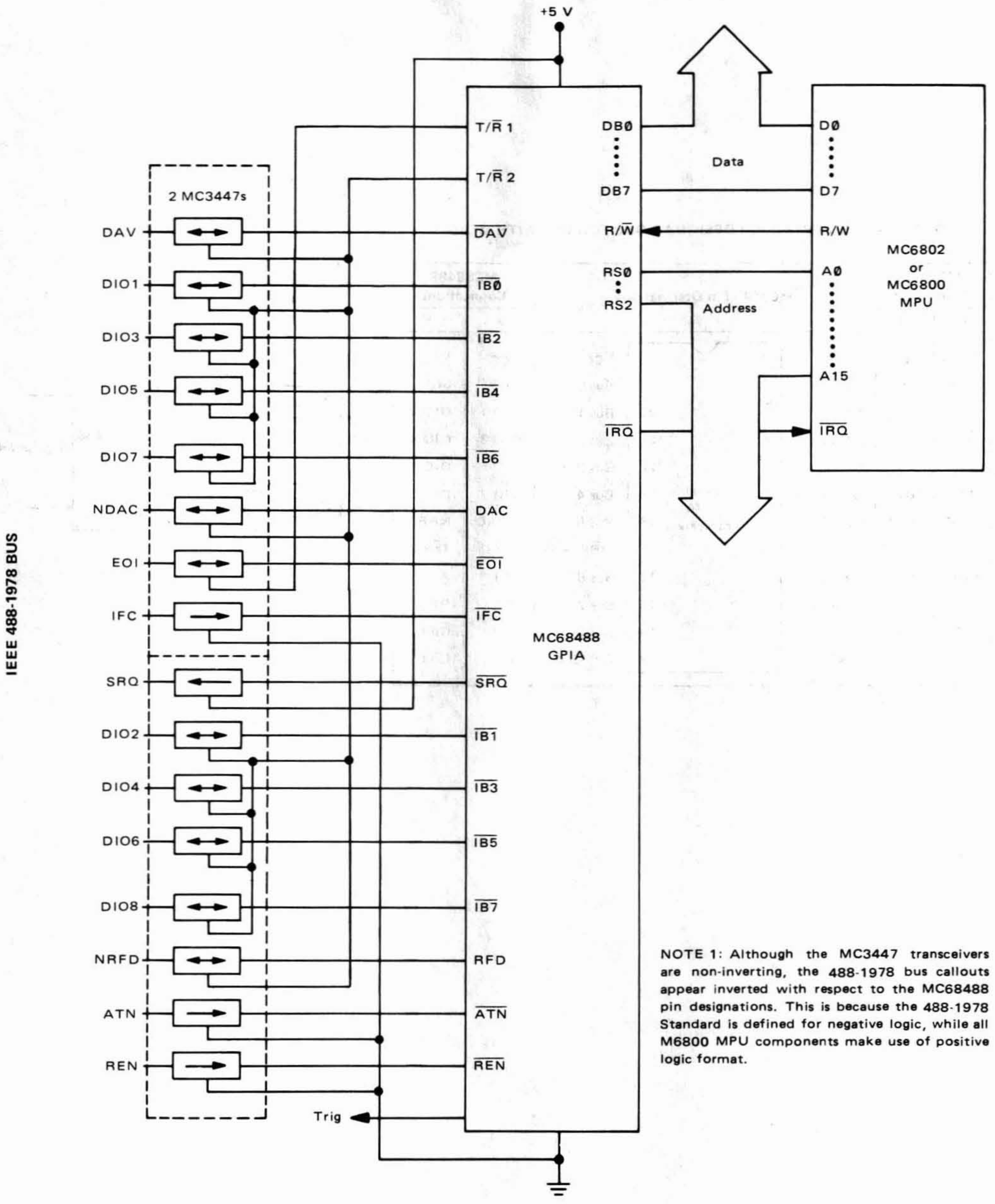

1
MC68488
$\overline{\text{IB0}}$
$\overline{\text{IB7}}$
T/R 1
T/R2
$\overline{\text{ATN}}$
$\overline{\text{EOI}}$
$\overline{\text{SRQ}}$
$\overline{\text{REN}}$
$\overline{\text{IFC}}$
$\overline{\text{DAV}}$
DAC
RFD
2 MC3447s
Device A
Device B
VCC
VCC
VCC
1
S/R (0)
0
1
2
3
4
5
S/R (5)
S/R (1–4)
6
7
S/R (6)
S/R (7)
1
DAV
SRQ
DIO1
DIO8
DAC
RFD
ATN
EOI
REN
IFC
Gnd
Gnd
Gnd
Gnd
Jumper or second
level metal

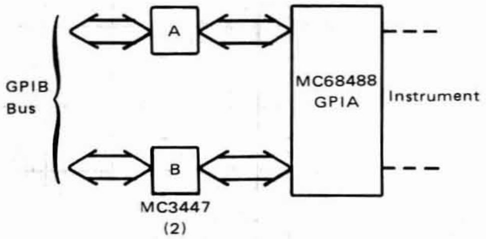
FIGURE 8 – SIMPLE SYSTEM CONFIGURATION


+5 V
2 MC3447s
IEEE 488-1978 BUS
DAV
DIO1
DIO3
DIO5
DIO7
NDAC
EOI
IFC
SRQ
DIO2
DIO4
DIO6
DIO8
NRFD
ATN
REN
Trig
T/R̄ 1
T/R̄ 2
DAV
IB0
IB2
IB4
IB6
DAC
EOI
IFC
SRQ
IB1
IB3
IB5
IB7
RFD
ATN
REN
MC68488
GPIA
DB0
DB7
R/W̄
RS0
RS2
IRQ
Data
Address
D0
D7
R/W
A0
A15
IRQ
MC6802
or
MC6800
MPU

NOTE 1: Although the MC3447 transceivers are non-inverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

FIGURE 9 — SUGGESTED PIN DESIGNATIONS FOR USE WITH MC68488

| MC68488 Connections |  | MC3447 Pin Designations |  |  |  |  | MC68488 Connections |  |
|---|---|---|---|---|---|---|---|---|
| A | B |  |  |  |  |  | A | B |
| T/$\overline{R}$ 2 | $V_{CC}$ | S/$\overline{R}$ (0) | 1 |  | 24 | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| $\overline{DAV}$ | $\overline{SRQ}$ | Data 0 0 | 2 |  | 23 | Bus 0 | DAV | SRQ |
| $\overline{IB0}$ | $\overline{IB1}$ | Data 1 | 3 |  | 22 | Bus 1 | DIO 1 | DIO 2 |
| $\overline{IB2}$ | $\overline{IB3}$ | Data 2 | 4 |  | 21 | Bus 2 | DIO 3 | DIO 4 |
| $\overline{IB4}$ | $\overline{IB5}$ | Data 3 | 5 |  | 20 | Bus 3 | DIO 5 | DIO 6 |
| $\overline{IB6}$ | $\overline{IB7}$ | Data 4 | 6 | Octal GPIB Transceiver | 19 | Bus 4 | DIO 7 | DIO 8 |
| DAC | RFD | Data 5 | 7 |  | 18 | Bus 5 | NDAC | NRFD |
| T/$\overline{R}$ 2 | T/$\overline{R}$ 2 | $\overline{S}$/R (5) | 8 |  | 17 | S/$\overline{R}$ (1–4) | T/$\overline{R}$ 2 | T/$\overline{R}$ 2 |
| $\overline{EOI}$ | $\overline{ATN}$ | Data 6 | 9 |  | 16 | Bus 6 | EOI | ATN |
| $\overline{IFC}$ | $\overline{REN}$ | Data 7 | 10 |  | 15 | Bus 7 | IFC | REN |
| T/$\overline{R}$ 1 | Gnd | S/$\overline{R}$ (6) | 11 |  | 14 | S/$\overline{R}$ (7) | Gnd | Gnd |
| Gnd | Gnd | Logic Gnd | 12 |  | 13 | Bus Gnd | Gnd | Gnd |



**MOTOROLA**

# MC3448A

## BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

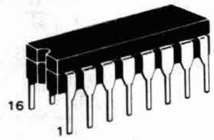
This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver outputs to be operated in an open collector(1) or active pull-up configuration. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

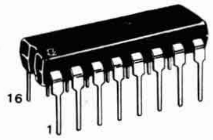
- Four Independent Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis – 600 mV (Typ)
- Fast Propagation Times – 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output Option(1)
- Power Up/Power Down Protection
  (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power Is Removed From Device
- Required Termination Characteristics Provided

## QUAD THREE-STATE BUS TRANSCEIVER WITH TERMINATION NETWORKS

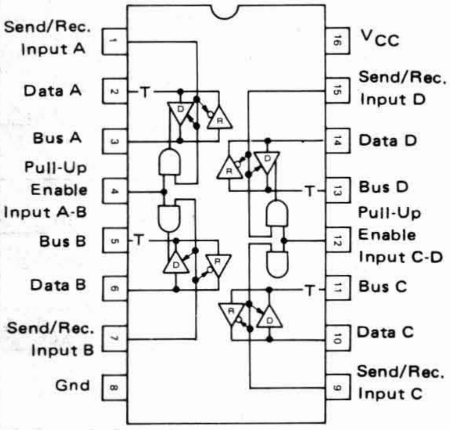
**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02



**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

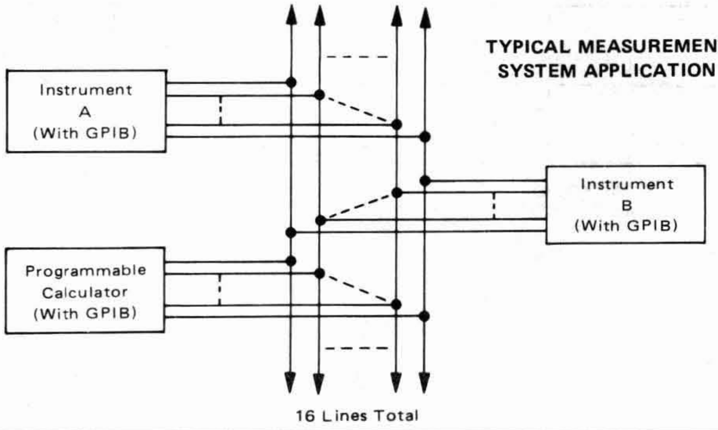

Send/Rec. Input A
Data A
Bus A
Pull-Up Enable Input A-B
Bus B
Data B
Send/Rec. Input B
Gnd
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VCC
Send/Rec. Input D
Data D
Bus D
Pull-Up Enable Input C-D
Bus C
Data C
Send/Rec. Input C
T
D
R

–T– = Bus Termination

## MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 7.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Driver Output Current | $I_{O(D)}$ | 150 | mA |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**TYPICAL MEASUREMENT SYSTEM APPLICATION**


Instrument A (With GPIB)
Instrument B (With GPIB)
Programmable Calculator (With GPIB)
16 Lines Total

**TRUTH TABLE**

| Send/Rec. | Enable | Info. Flow | Comments |
|---|---|---|---|
| 0 | X | Bus → Data | – |
| 1 | 1 | Data → Bus | Active Pull-Up |
| 1 | 0 | Data → Bus | Open Col. |

X = Don't Care

---

(1) Selection of the "Open Collector" configuration, in fact, selects an open collector device with a passive pull-up load/termination which conforms to Figure 7, IEEE 488-1978 Bus Standard.

## ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.75 V ≤ $V_{CC}$ ≤ 5.25 V and 0 ≤ $T_A$ ≤ 70°C; typical values are at $T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Bus Voltage | | | | | V |
| (Bus Pin Open)($V_{I(S/R)}$ = 0.8 V) | $V_{(BUS)}$ | 2.75 | – | 3.7 | |
| ($I_{(BUS)}$ = −12 mA) | $V_{IC(BUS)}$ | – | – | −1.5 | |
| Bus Current | $I_{(BUS)}$ | | | | mA |
| (5.0 V ≤ $V_{(BUS)}$ ≤ 5.5 V) | | 0.7 | – | 2.5 | |
| ($V_{(BUS)}$ = 0.5 V) | | −1.3 | – | −3.2 | |
| ($V_{CC}$ = 0 V, 0 V ≤ $V_{(BUS)}$ ≤ 2.75 V) | | – | – | +0.04 | |
| Receiver Input Hysteresis<br>($V_{I(S/R)}$ = 0.8 V) | – | 400 | 600 | – | mV |
| Receiver Input Threshold | | | | | V |
| ($V_{I(S/R)}$ = 0.8 V, Low to High) | $V_{ILH(R)}$ | – | 1.6 | 1.8 | |
| ($V_{I(S/R)}$ = 0.8 V, High to Low) | $V_{IHL(R)}$ | 0.8 | 1.0 | – | |
| Receiver Output Voltage – High Logic State<br>($V_{I(S/R)}$ = 0.8 V, $I_{OH(R)}$ = −800 µA, $V_{(BUS)}$ = 2.0 V) | $V_{OH(R)}$ | 2.7 | – | – | V |
| Receiver Output Voltage – Low Logic State<br>($V_{I(S/R)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{(BUS)}$ = 0.8 V) | $V_{OL(R)}$ | – | – | 0.5 | V |
| Receiver Output Short Circuit Current<br>($V_{I(S/R)}$ = 0.8 V, $V_{(BUS)}$ = 2.0 V) | $I_{OS(R)}$ | −15 | – | −75 | mA |
| Driver Input Voltage – High Logic State<br>($V_{I(S/R)}$ = 2.0 V) | $V_{IH(D)}$ | 2.0 | – | – | V |
| Driver Input Voltage – Low Logic State<br>($V_{I(S/R)}$ = 2.0 V) | $V_{IL(D)}$ | – | – | 0.8 | V |
| Driver Input Current – Data Pins<br>($V_{I(S/R)}$ = $V_{I(E)}$ = 2.0 V) | | | | | µA |
| (0.5 ≤ $V_{I(D)}$ ≤ 2.7 V) | $I_{I(D)}$ | −200 | – | 40 | |
| ($V_{I(D)}$ = 5.5 V) | $I_{IB(D)}$ | – | – | 200 | |
| Input Current – Send/Receive | | | | | µA |
| (0.5 ≤ $V_{I(S/R)}$ ≤ 2.7 V) | $I_{I(S/R)}$ | −100 | – | 20 | |
| ($V_{I(S/R)}$ = 5.5 V) | $I_{IB(S/R)}$ | – | – | 100 | |
| Input Current – Enable | | | | | µA |
| (0.5 ≤ $V_{I(E)}$ ≤ 2.7 V) | $I_{I(E)}$ | −200 | – | 20 | |
| ($V_{I(E)}$ = 5.5 V) | $I_{IB(E)}$ | – | – | 100 | |
| Driver Input Clamp Voltage<br>($V_{I(S/R)}$ = 2.0 V, $I_{IC(D)}$ = −18 mA) | $V_{IC(D)}$ | – | – | −1.5 | V |
| Driver Output Voltage – High Logic State<br>($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V, $I_{OH}$ = −5.2 mA) | $V_{OH(D)}$ | 2.5 | – | – | V |
| Driver Output Voltage – Low Logic State (Note 1)<br>($V_{I(S/R)}$ = 2.0 V, $I_{OL(D)}$ = 48 mA) | $V_{OL(D)}$ | – | – | 0.5 | V |
| Output Short Circuit Current<br>($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V) | $I_{OS(D)}$ | −30 | – | −120 | mA |
| Power Supply Current | | | | | mA |
| (Listening Mode – All Receivers On) | $I_{CCL}$ | – | 63 | 85 | |
| (Talking Mode – All Drivers On) | $I_{CCH}$ | – | 106 | 125 | |

## SWITCHING CHARACTERISTICS

($V_{CC}$ = 5.0 V, $T_A$ = 25°C unless otherwise noted)

| | | | | | |
|---|---|---|---|---|---|
| Propagation Delay of Driver | | | | | ns |
| (Output Low to High) | $t_{PLH(D)}$ | – | – | 15 | |
| (Output High to Low) | $t_{PHL(D)}$ | – | – | 17 | |
| Propagation Delay of Receiver | | | | | ns |
| (Output Low to High) | $t_{PLH(R)}$ | – | – | 25 | |
| (Output High to Low) | $t_{PHL(R)}$ | – | – | 23 | |

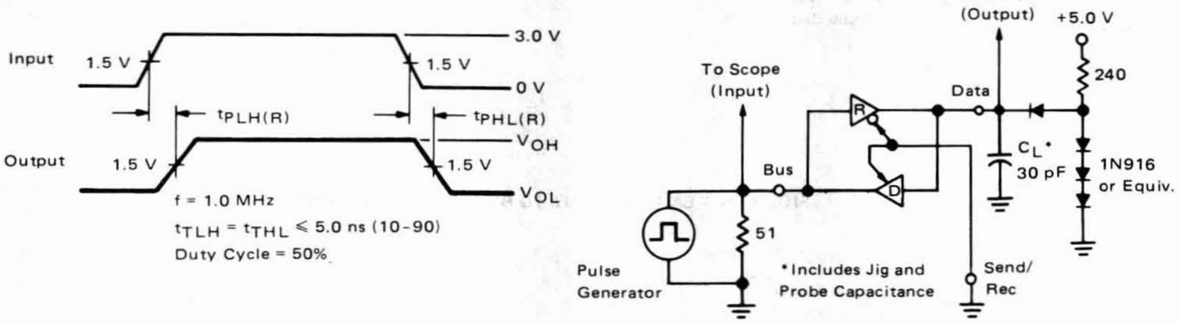
NOTE 1. A modification of the IEEE 488-1978 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

**SWITCHING CHARACTERISTICS (continued)** ($V_{CC}$ = 5.0 V, $T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Time – Send/Receive to Data | | | | | ns |
| Logic High to Third State | $t_{PHZ(R)}$ | – | – | 30 | |
| Third State to Logic High | $t_{PZH(R)}$ | – | – | 30 | |
| Logic Low to Third State | $t_{PLZ(R)}$ | – | – | 30 | |
| Third State to Logic Low | $t_{PZL(R)}$ | – | – | 30 | |
| Propagation Delay Time – Send/Receive to Bus | | | | | ns |
| Logic High to Third State | $t_{PHZ(D)}$ | – | – | 30 | |
| Third State to Logic High | $t_{PZH(D)}$ | – | – | 30 | |
| Logic Low to Third State | $t_{PLZ(D)}$ | – | – | 30 | |
| Third State to Logic Low | $t_{PZL(D)}$ | – | – | 30 | |
| Turn-On Time – Enable to Bus | | | | | ns |
| Pull-Up Enable to Open Collector | $t_{POFF(E)}$ | – | – | 30 | |
| Open Collector to Pull-Up Enable | $t_{PON(E)}$ | – | – | 20 | |

## PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

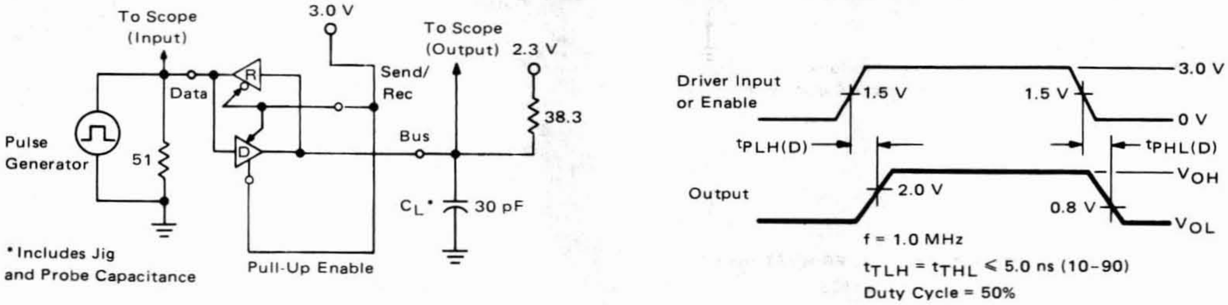
FIGURE 1 – BUS INPUT TO DATA OUTPUT (RECEIVER)


Input
1.5 V
3.0 V
1.5 V
0 V
tPLH(R)
tPHL(R)
Output
1.5 V
VOH
1.5 V
VOL
To Scope (Output)
+5.0 V
240
To Scope (Input)
Data
R
CL*
30 pF
1N916 or Equiv.
Bus
D
51
Pulse Generator
Send/Rec

f = 1.0 MHz
$t_{TLH} = t_{THL} \leqslant$ 5.0 ns (10–90)
Duty Cycle = 50%

*Includes Jig and Probe Capacitance

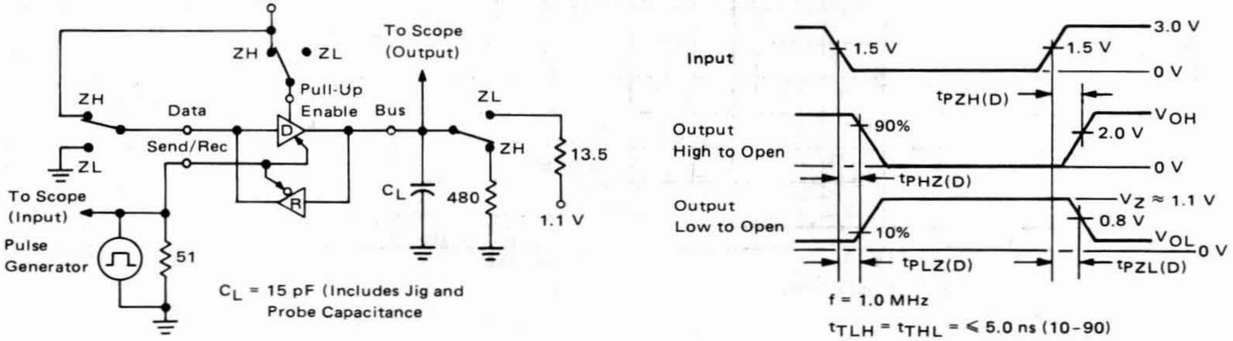
FIGURE 2 – DATA INPUT TO BUS OUTPUT (DRIVER)


To Scope (Input)
3.0 V
To Scope (Output)
2.3 V
Send/Rec
Data
R
38.3
Pulse Generator
51
D
Bus
CL*
30 pF
Pull-Up Enable
Driver Input or Enable
1.5 V
1.5 V
3.0 V
0 V
tPLH(D)
tPHL(D)
Output
2.0 V
0.8 V
VOH
VOL

*Includes Jig and Probe Capacitance

f = 1.0 MHz
$t_{TLH} = t_{THL} \leqslant$ 5.0 ns (10–90)
Duty Cycle = 50%

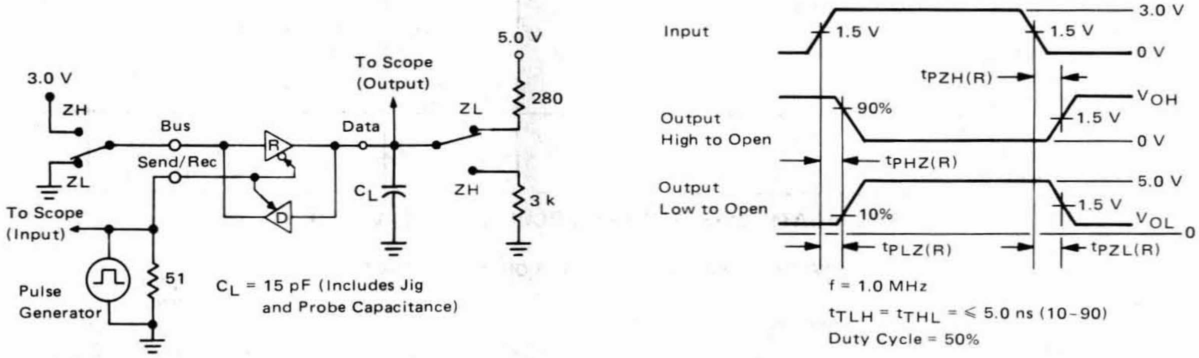
FIGURE 3 – SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)


3.0 V
ZH
ZL
To Scope (Output)
Pull-Up Enable
ZH
Data
Bus
ZL
Send/Rec
D
ZH
13.5
ZL
To Scope (Input)
R
CL
480
1.1 V
Pulse Generator
51
Input
1.5 V
1.5 V
3.0 V
0 V
tPZH(D)
Output High to Open
90%
VOH
2.0 V
0 V
tPHZ(D)
Output Low to Open
VZ ≈ 1.1 V
0.8 V
10%
VOL
0 V
tPLZ(D)
tPZL(D)

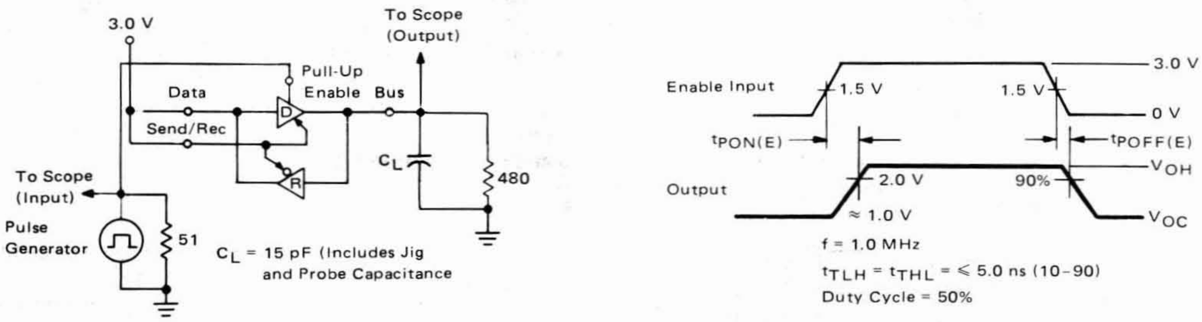
$C_L$ = 15 pF (Includes Jig and Probe Capacitance

f = 1.0 MHz
$t_{TLH} = t_{THL} = \leqslant$ 5.0 ns (10–90)
Duty Cycle = 50%

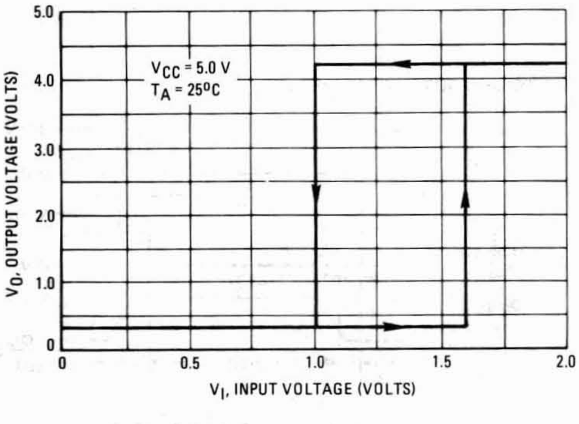
### FIGURE 4 – SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)


3.0 V
ZH
ZL
Bus
Send/Rec
R
D
Data
To Scope
(Output)
5.0 V
280
ZL
ZH
3 k
$C_L$
To Scope
(Input)
Pulse
Generator
51
$C_L$ = 15 pF (Includes Jig
and Probe Capacitance)
Input
1.5 V
1.5 V
3.0 V
0 V
$t_{PZH(R)}$
Output
High to Open
90%
$V_{OH}$
1.5 V
0 V
$t_{PHZ(R)}$
Output
Low to Open
5.0 V
10%
1.5 V
$V_{OL}$
0 V
$t_{PLZ(R)}$
$t_{PZL(R)}$
f = 1.0 MHz
$t_{TLH} = t_{THL} = \leqslant 5.0$ ns (10–90)
Duty Cycle = 50%

### FIGURE 5 – ENABLE INPUT TO BUS OUTPUT (DRIVER)


3.0 V
Data
Send/Rec
Pull-Up
Enable
Bus
D
R
To Scope
(Output)
$C_L$
480
To Scope
(Input)
Pulse
Generator
51
$C_L$ = 15 pF (Includes Jig
and Probe Capacitance
Enable Input
1.5 V
1.5 V
3.0 V
0 V
$t_{PON(E)}$
$t_{POFF(E)}$
Output
2.0 V
90%
$V_{OH}$
≈ 1.0 V
$V_{OC}$
f = 1.0 MHz
$t_{TLH} = t_{THL} = \leqslant 5.0$ ns (10–90)
Duty Cycle = 50%

### FIGURE 6 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS



### FIGURE 7 – TYPICAL BUS LOAD LINE

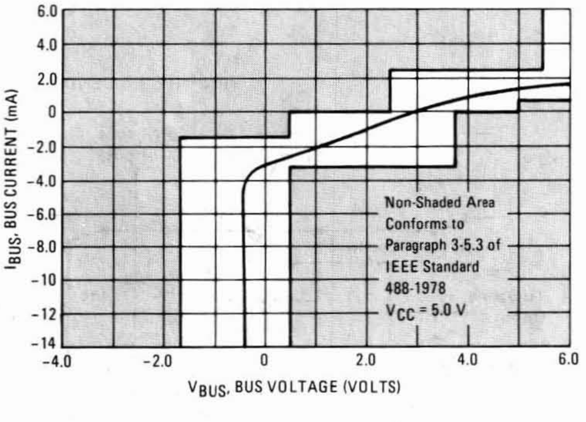
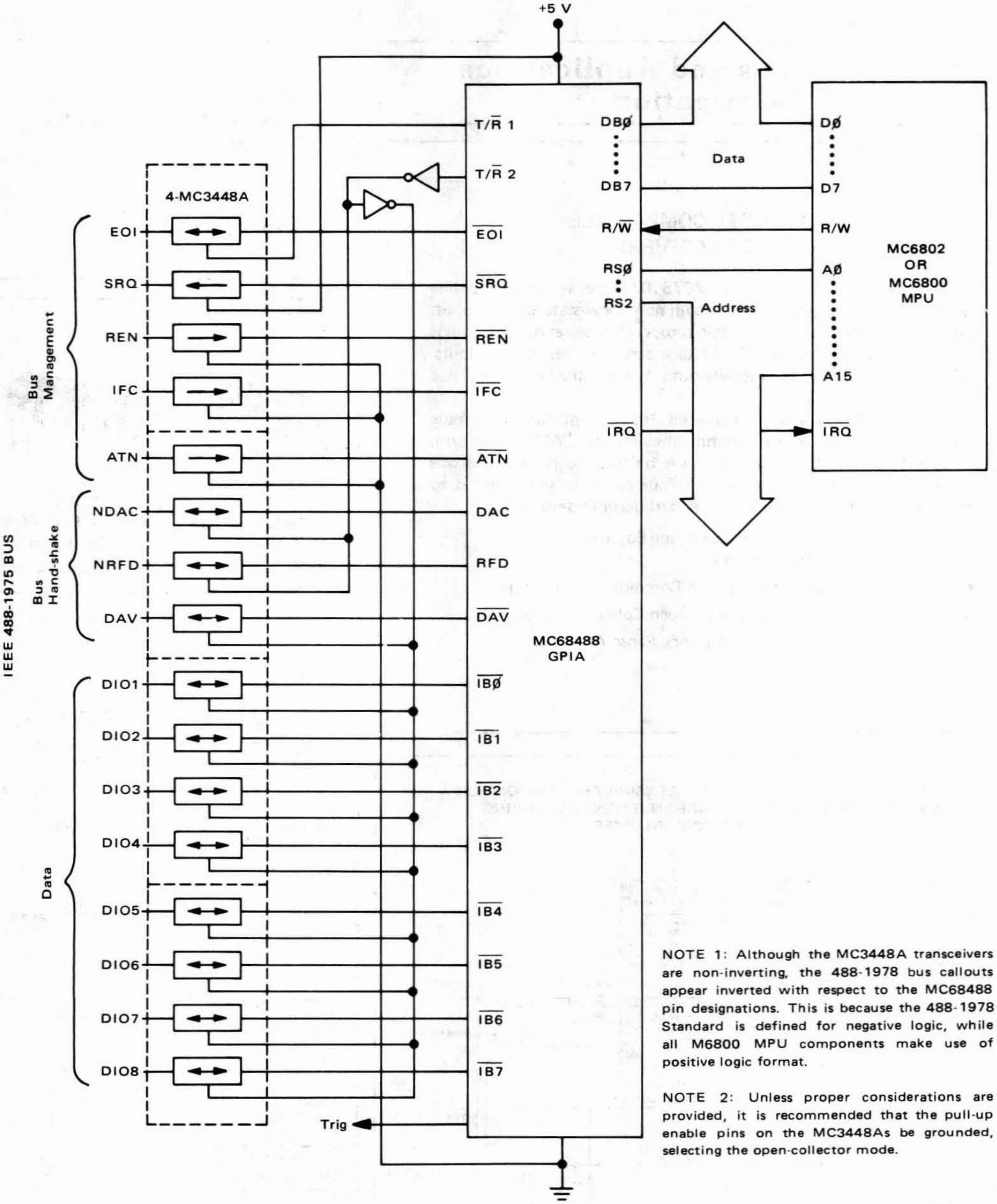


FIGURE 8 — SIMPLE SYSTEM CONFIGURATION


+5 V
4-MC3448A
EOI
SRQ
REN
IFC
ATN
NDAC
NRFD
DAV
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
Bus Management
Bus Hand-shake
Data
IEEE 488-1975 BUS
T/R̄ 1
T/R̄ 2
EOI
SRQ
REN
IFC
ATN
DAC
RFD
DAV
IBØ
IB1
IB2
IB3
IB4
IB5
IB6
IB7
Trig
MC68488
GPIA
DBØ
DB7
R/W̄
RSØ
RS2
IRQ
Data
Address
DØ
D7
R/W
AØ
A15
IRQ
MC6802
OR
MC6800
MPU

NOTE 1: Although the MC3448A transceivers are non-inverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

NOTE 2: Unless proper considerations are provided, it is recommended that the pull-up enable pins on the MC3448As be grounded, selecting the open-collector mode.

**MOTOROLA**

# MC3450
# MC3452

## Specifications and Applications Information

### QUAD MTTL COMPATIBLE LINE RECEIVERS

The MC3450 features four MC75107 type active pullup line receivers with the addition of a common three-state strobe input. When the strobe input is at a logic zero, each receiver output state is determined by the differential voltage across its respective inputs. With the strobe high, the receiver outputs are in the high impedance state.

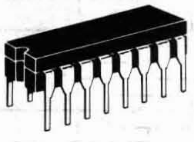
The MC3452 is the same as the MC3450 except that the outputs are open collector which permits the implied "AND" function.

The strobe input on both devices is buffered to present a strobe loading factor of only one for all four receivers and inverted to provide best compatability with standard decoder devices.

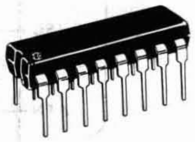
- Receiver Performance Identical to the Popular MC75107/MC75108 Series
- Four Independent Receivers with Common Strobe Input
- Implied "AND" Capability with Open Collector Outputs
- Useful as a Quad 1103 type Memory Sense Amplifier

QUAD LINE RECEIVERS WITH COMMON THREE-STATE STROBE INPUT

**SILICON MONOLITHIC INTEGRATED CIRCUITS**



**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02



**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

**CONNECTION DIAGRAM**

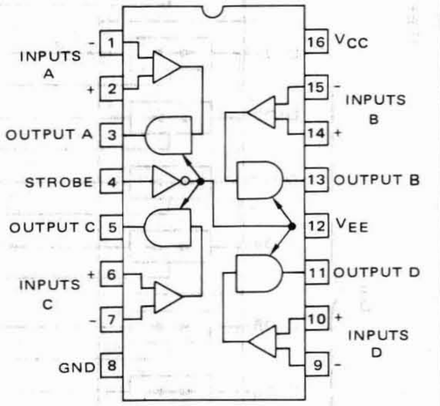
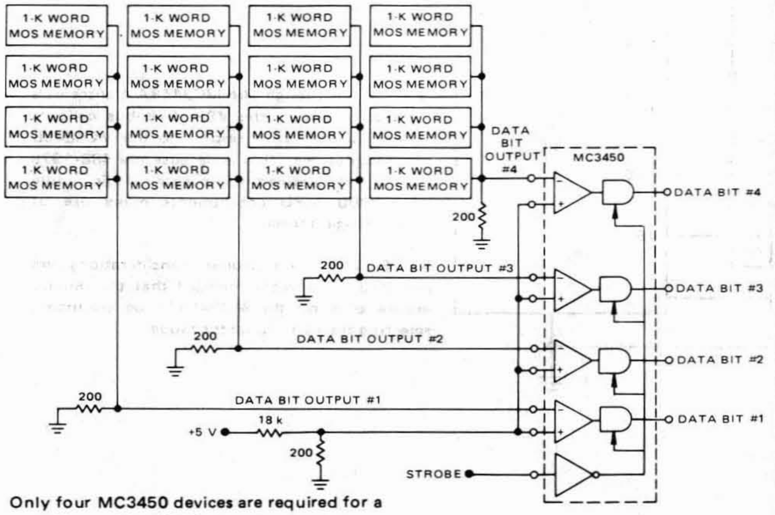

INPUTS A
1
2
OUTPUT A
3
STROBE
4
OUTPUT C
5
INPUTS C
6
7
GND
8
16
VCC
15
INPUTS B
14
13
OUTPUT B
12
VEE
11
OUTPUT D
10
INPUTS D
9

**FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES**


1-K WORD MOS MEMORY
DATA BIT OUTPUT #4
MC3450
DATA BIT #4
200
DATA BIT OUTPUT #3
DATA BIT #3
DATA BIT OUTPUT #2
DATA BIT #2
DATA BIT OUTPUT #1
DATA BIT #1
18 k
+5 V
STROBE

Only four MC3450 devices are required for a 4-k word by 16-bit memory system.

**TRUTH TABLE**

| INPUT | STROBE | OUTPUT MC3450 | OUTPUT MC3452 |
|---|---|---|---|
| $V_{ID} \geqslant +25$ mV | L | H | Off |
|  | H | Z | Off |
| $-25$ mV $\leqslant V_{ID} \leqslant +25$ mV | L | I | I |
|  | H | Z | Off |
| $V_{ID} \leqslant -25$ mV | L | L | L |
|  | H | Z | Off |

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
I = Indeterminate State

**MAXIMUM RATINGS** ($T_A$ = 0 to +70°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltages | $V_{CC}$, $V_{EE}$ | ±7.0 | Vdc |
| Differential-Mode Input Signal Voltage Range | $V_{IDR}$ | ±6.0 | Vdc |
| Common-Mode Input Voltage Range | $V_{ICR}$ | ±5.0 | Vdc |
| Strobe Input Voltage | $V_{I(S)}$ | 5.5 | Vdc |
| Power Dissipation (Package Limitation) | $P_D$ | | |
| Ceramic Dual In-Line Package | | 1000 | mW |
| Derate above $T_A$ = +25°C | | 6.6 | mW/°C |
| Plastic Dual In-Line Package | | 1000 | mW |
| Derate above $T_A$ = +25°C | | 6.6 | mW/°C |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**RECOMMENDED OPERATING CONDITIONS** ($T_A$ = 0 to +70°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltages | $V_{CC}$<br>$V_{EE}$ | +4.75<br>-4.75 | +5.0<br>-5.0 | +5.25<br>-5.25 | Vdc |
| Output Load Current | $I_{OL}$ | – | – | 16 | mA |
| Differential-Mode Input Voltage Range | $V_{IDR}$ | -5.0 | – | +5.0 | Vdc |
| Common-Mode Input Voltage Range | $V_{ICR}$ | -3.0 | – | +3.0 | Vdc |
| Input Voltage Range (any input to Ground) | $V_{IR}$ | -5.0 | – | +3.0 | Vdc |

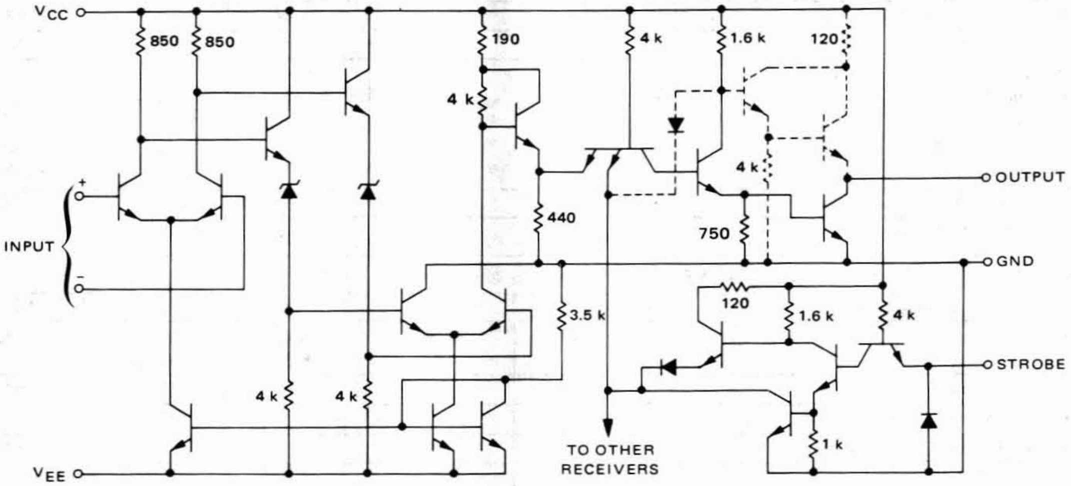
**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $V_{EE}$ = -5.0 Vdc, $T_A$ = 0 to +70°C unless otherwise noted.)

| | | | MC3450 | | | MC3452 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Characteristic | Symbol | Fig. | Min | Typ | Max | Min | Typ | Max | Unit |
| High Level Input Current to Receiver Input | $I_{IH(I)}$ | 7 | – | – | 75 | – | – | 75 | μA |
| Low Level Input Current to Receiver Input | $I_{IL(I)}$ | 8 | – | – | -10 | – | – | -10 | μA |
| High Level Input Current to Strobe Input | $I_{IH(S)}$ | 5 | | | | | | | |
| $V_{IH(S)}$ = +2.4 V | | | – | – | 40 | – | – | 40 | μA |
| $V_{IH(S)}$ = +5.25 V | | | – | – | 1.0 | – | – | 1.0 | mA |
| Low Level Input Current to Strobe Input<br>$V_{IH(S)}$ = +0.4 V | $I_{IL(S)}$ | 5 | – | – | -1.6 | – | – | -1.6 | mA |
| High Level Output Voltage | $V_{OH}$ | 3 | 2.4 | – | – | – | – | – | Vdc |
| High Level Output Leakage Current | $I_{CEX}$ | 3 | – | – | – | – | – | 250 | μA |
| Low Level Output Voltage | $V_{OL}$ | 3 | – | – | 0.5 | – | – | 0.5 | Vdc |
| Short-Circuit Output Current | $I_{OS}$ | 6 | -18 | – | -70 | – | – | – | mA |
| Output Disable Leakage Current | $I_{off}$ | 9 | – | – | 40 | – | – | – | μA |
| High Logic Level Supply Current from $V_{CC}$ | $I_{CCH}$ | 4 | – | 45 | 60 | – | 45 | 60 | mA |
| High Logic Level Supply Current from $V_{EE}$ | $I_{EEH}$ | 4 | – | -17 | -30 | – | -17 | -30 | mA |

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = +5.0 Vdc, $V_{EE}$ = -5.0 Vdc, $T_A$ = +25°C unless otherwise noted.)

| | | | MC3450 | | | MC3452 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Characteristic | Symbol | Fig. | Min | Typ | Max | Min | Typ | Max | Unit |
| High to Low Logic Level Propagation Delay Time (Differential Inputs) | $t_{PHL(D)}$ | 10 | – | – | 25 | – | – | 25 | ns |
| Low to High Logic Level Propagation Delay Time (Differential Inputs) | $t_{PLH(D)}$ | 10 | – | – | 25 | – | – | 25 | ns |
| Open State to High Logic Level Propagation Delay Time (Strobe) | $t_{PZH(S)}$ | 11 | – | – | 21 | – | – | – | ns |
| High Logic Level to Open State Propagation Delay Time (Strobe) | $t_{PHZ(S)}$ | 11 | – | – | 18 | – | – | – | ns |
| Open State to Low Logic Level Propagation Delay Time (Strobe) | $t_{PZL(S)}$ | 11 | – | – | 27 | – | – | – | ns |
| Low Logic Level to Open State Propagation Delay Time (Strobe) | $t_{PLZ(S)}$ | 11 | – | – | 29 | – | – | – | ns |
| High Logic to Low Logic Level Propagation Delay Time (Strobe) | $t_{PHL(S)}$ | 12 | – | – | – | – | – | 25 | ns |
| Low Logic to High Logic Level Propagation Delay Time (Strobe) | $t_{PLH(S)}$ | 12 | – | – | – | – | – | 25 | ns |

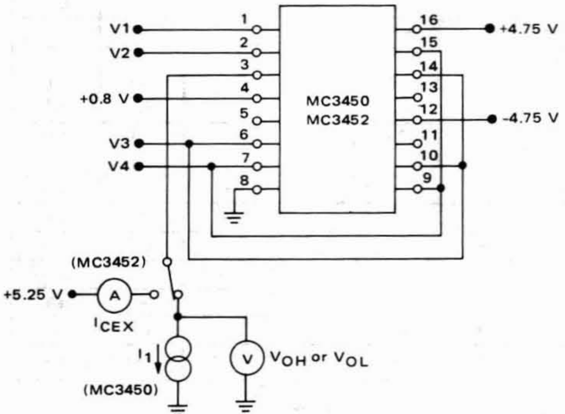
FIGURE 2 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)


VCC
850
850
190
4 k
1.6 k
120
4 k
4 k
440
750
OUTPUT
INPUT
+
–
GND
120
1.6 k
4 k
3.5 k
STROBE
4 k
4 k
1 k
TO OTHER RECEIVERS
VEE

Dashed components apply to the MC3450 circuit only.

## TEST CIRCUITS

FIGURE 3 – $I_{CEX}$, $V_{OH}$, AND $V_{OL}$


V1
V2
+0.8 V
V3
V4
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MC3450
MC3452
+4.75 V
-4.75 V
(MC3452)
+5.25 V
A
ICEX
I1
(MC3450)
V
VOH or VOL

TEST TABLE

| | V1 | | V2 | | V3 | | V4 | | |
|---|---|---|---|---|---|---|---|---|---|
| | MC3450 | MC3452 | MC3450 | MC3452 | MC3450 | MC3452 | MC3450 | MC3452 | I1 |
| $V_{OH}$ | +2.975 V | – | +3.0 V | – | +3.0 V | – | GND | – | +0.4 mA |
| | -3.0 V | – | -2.975 V | – | GND | – | -3.0 V | – | |
| $I_{CEX}$ | – | +2.975 V | – | +3.0 V | – | +3.0 V | – | GND | – |
| | – | -3.0 V | – | -2.975 V | – | GND | – | -3.0 V | – |
| $V_{OL}$ | +3.0 V | +3.0 V | +2.975 V | +2.975 V | GND | GND | +3.0 V | +3.0 V | -16 mA |
| | -2.975 V | -2.975 V | -3.0 V | -3.0 V | -3.0 V | -3.0 V | GND | GND | |

Channel A shown under test. Other channels are tested similarly.

FIGURE 4 – $I_{CCH}$ AND $I_{EEH}$

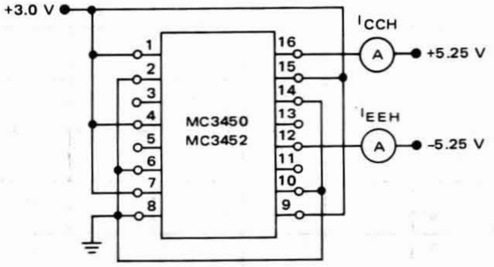
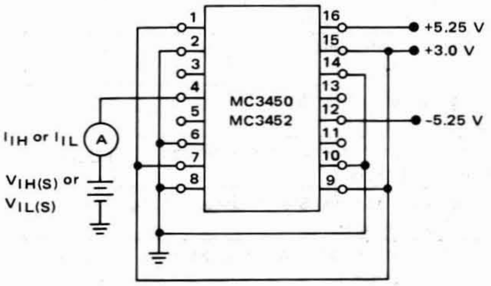
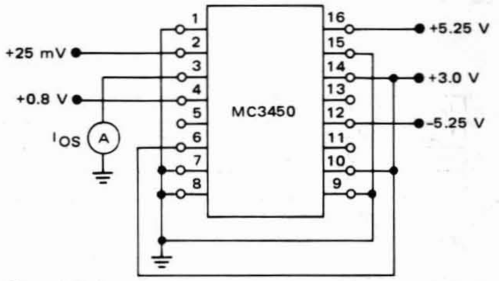

+3.0 V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MC3450
MC3452
ICCH
A
+5.25 V
IEEH
A
-5.25 V

FIGURE 5 – $I_{IH(S)}$ AND $I_{IL(S)}$


1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
MC3450
MC3452
+5.25 V
+3.0 V
-5.25 V
IIH or IIL
A
VIH(S) or
VIL(S)

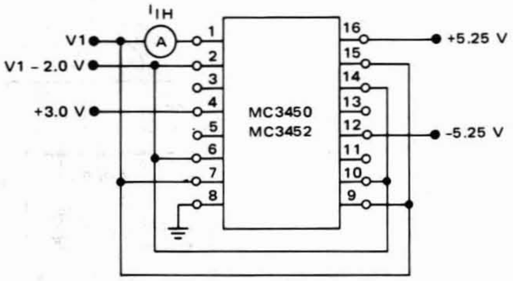
## TEST CIRCUITS (continued)

FIGURE 6 – $I_{OS}$


+25 mV
+0.8 V
IOS
A
MC3450
+5.25 V
+3.0 V
-5.25 V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9

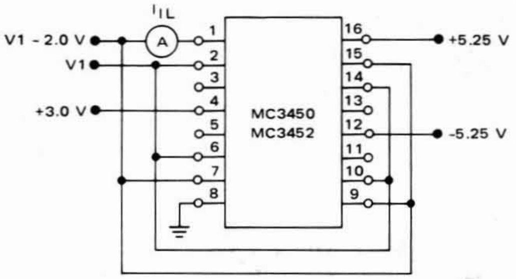
Channel A shown under test, other channels are tested similarly. Only one output shorted at a time.

FIGURE 7 – $I_{IH}$


IIH
A
V1
V1 - 2.0 V
+3.0 V
MC3450
MC3452
+5.25 V
-5.25 V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9

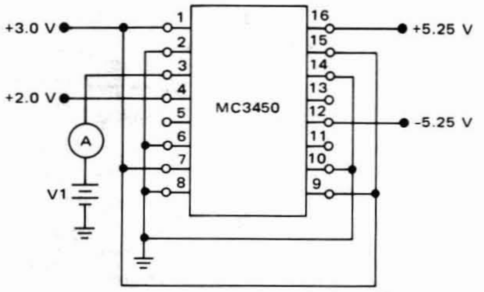
Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to –3.0 V.

FIGURE 8 – $I_{IL}$


IIL
A
V1 - 2.0 V
V1
+3.0 V
MC3450
MC3452
+5.25 V
-5.25 V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9

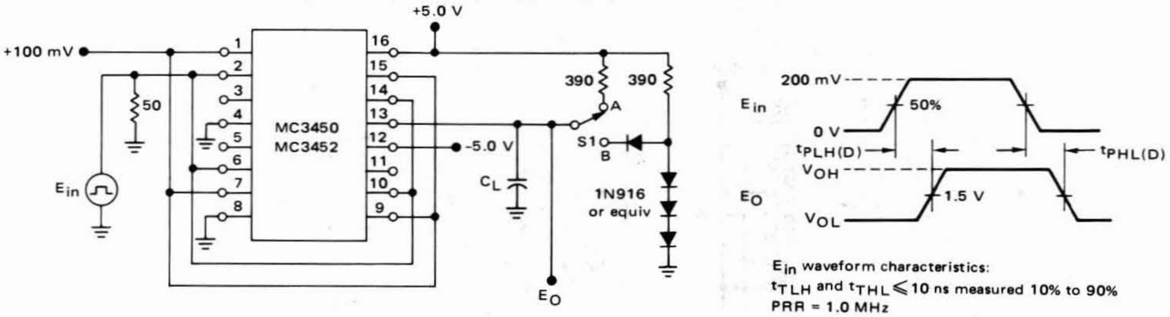
Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to –3.0 V.

FIGURE 9 – $I_{off}$


+3.0 V
+2.0 V
A
V1
MC3450
+5.25 V
-5.25 V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9

Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4 V and +2.4 V.

FIGURE 10 – RECEIVER PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$


+5.0 V
+100 mV
50
Ein
MC3450
MC3452
-5.0 V
CL
390
390
A
S1
B
1N916
or equiv
EO
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
200 mV
Ein
50%
0 V
tPLH(D)
tPHL(D)
VOH
EO
1.5 V
VOL

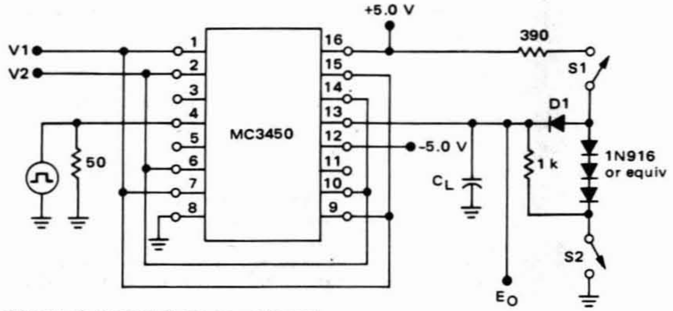
$E_{in}$ waveform characteristics:
$t_{TLH}$ and $t_{THL} \leqslant 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

Output of Channel B shown under test, other channels are tested similarly.

S1 at "A" for MC3452
S1 at "B" for MC3450
$C_L$ = 15 pF total for MC3452
$C_L$ = 50 pF total for MC3450

## TEST CIRCUITS (continued)

### FIGURE 11 – STROBE PROPAGATION DELAY TIMES $t_{PLZ(S)}$, $t_{PZL(S)}$ $t_{PHZ(S)}$ and $t_{PZH(S)}$


+5.0 V
V1
V2
MC3450
390
S1
D1
1N916 or equiv
-5.0 V
1 k
$C_L$
50
S2
$E_O$
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

Output of Channel B shown under test, other channels are tested similarly.

| | V1 | V2 | S1 | S2 | $C_L$ |
|---|---|---|---|---|---|
| $t_{PLZ(S)}$ | 100 mV | GND | Closed | Closed | 15 pF |
| $t_{PZL(S)}$ | 100 mV | GND | Closed | Open | 50 pF |
| $t_{PHZ(S)}$ | GND | 100 mV | Closed | Closed | 15 pF |
| $t_{PZH(S)}$ | GND | 100 mV | Open | Closed | 50 pF |

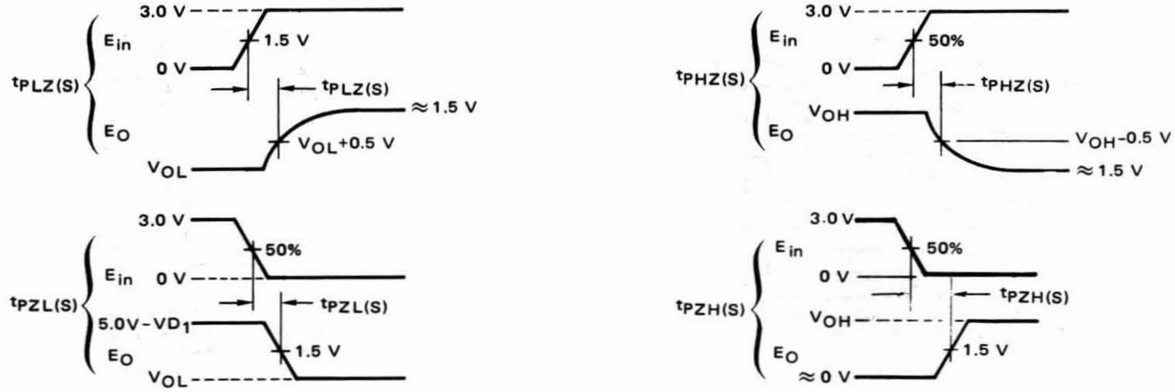
$C_L$ includes jig and probe capacitance.

$E_{in}$ waveform characteristics:

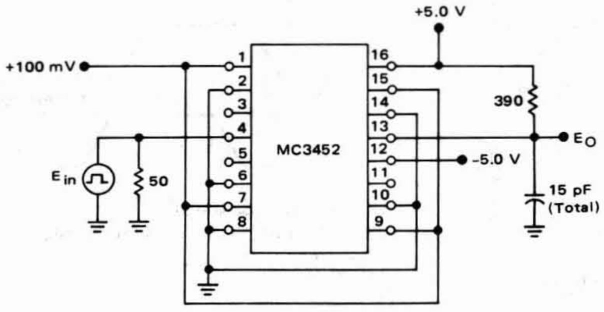
$t_{TLH}$ and $t_{THL} \leqslant 10$ ns measured 10% to 90%.

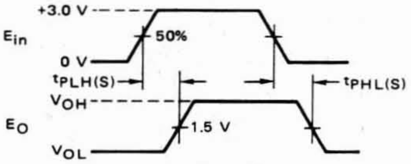
PRR = 1.0 MHz

Duty Cycle = 50%


$t_{PLZ(S)}$
$E_{in}$
3.0 V
1.5 V
0 V
$t_{PLZ(S)}$
≈1.5 V
$E_O$
$V_{OL}+0.5$ V
$V_{OL}$
$t_{PHZ(S)}$
$E_{in}$
3.0 V
50%
0 V
$t_{PHZ(S)}$
$V_{OH}$
$E_O$
$V_{OH}-0.5$ V
≈1.5 V
$t_{PZL(S)}$
3.0 V
50%
$E_{in}$
0 V
$t_{PZL(S)}$
$5.0V-VD_1$
$E_O$
1.5 V
$V_{OL}$
$t_{PZH(S)}$
3.0 V
$E_{in}$
50%
0 V
$t_{PZH(S)}$
$V_{OH}$
$E_O$
1.5 V
≈0 V

### FIGURE 12 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$


+5.0 V
+100 mV
MC3452
390
$E_O$
-5.0 V
$E_{in}$
50
15 pF (Total)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16


$E_{in}$
+3.0 V
50%
0 V
$t_{PLH(S)}$
$t_{PHL(S)}$
$V_{OH}$
$E_O$
1.5 V
$V_{OL}$

$E_{in}$ waveform characteristics:

$t_{TLH}$ and $t_{THL} \leqslant 10$ ns measured 10% to 90%

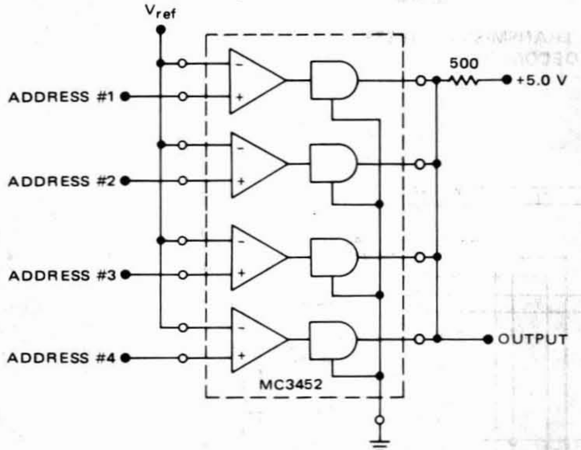
PRR = 1.0 MHz

Duty Cycle = 500 ns

Output of Channel B shown under test, other channels are tested similarly.

## APPLICATIONS INFORMATION

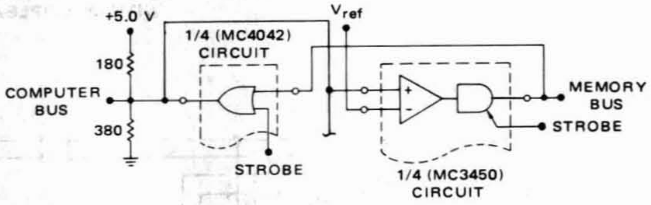
### FIGURE 13 – IMPLIED "AND" GATING



V_ref
500
+5.0 V
ADDRESS #1
ADDRESS #2
ADDRESS #3
ADDRESS #4
OUTPUT
MC3452

The MC3452 can be used for address decoding as illustrated above. All outputs of the MC3452 are tied together through a common resistor to +5.0 volts. In this configuration the MC3452 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

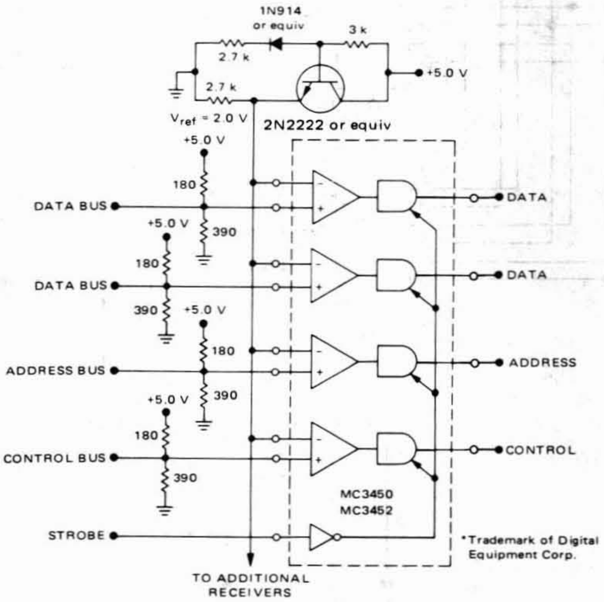
### FIGURE 14 – BIDIRECTIONAL DATA TRANSMISSION



+5.0 V
V_ref
1/4 (MC4042) CIRCUIT
180
COMPUTER BUS
380
STROBE
MEMORY BUS
STROBE
1/4 (MC3450) CIRCUIT

The three-state capability of the MC3450 permits bidirectional data transmission as illustrated.

### FIGURE 15 – SINGLE-ENDED UNI-BUS* LINE RECEIVER APPLICATION FOR MINICOMPUTERS

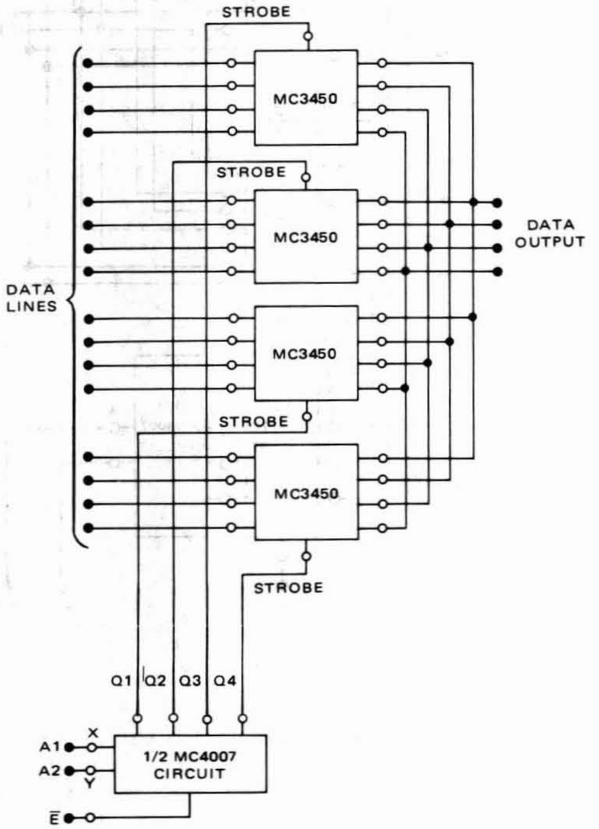


1N914 or equiv
3 k
2.7 k
2.7 k
+5.0 V
V_ref = 2.0 V
2N2222 or equiv
+5.0 V
180
DATA BUS
+5.0 V
390
180
DATA BUS
390
+5.0 V
180
ADDRESS BUS
+5.0 V
390
180
CONTROL BUS
390
STROBE
DATA
DATA
ADDRESS
CONTROL
MC3450
MC3452
TO ADDITIONAL RECEIVERS

*Trademark of Digital Equipment Corp.

The MC3450/3452 can be used for single-ended as well as differential line receiving. For single-ended line receiver applications, such as are encountered in minicomputers, the configuration shown in Figure 15 can be used. The voltage source, which generates $V_{ref}$, should be designed so that the $V_{ref}$ voltage is halfway between $V_{OH}$(min) and $V_{OL}$(max). The maximum input overdrive required to guarantee a given logic state is extremely small, 25 mV maximum. This low-input overdrive enhances differential noise immunity. Also the high-input impedance of the line receiver permits many receivers to be placed on a single line with minimum load effects.

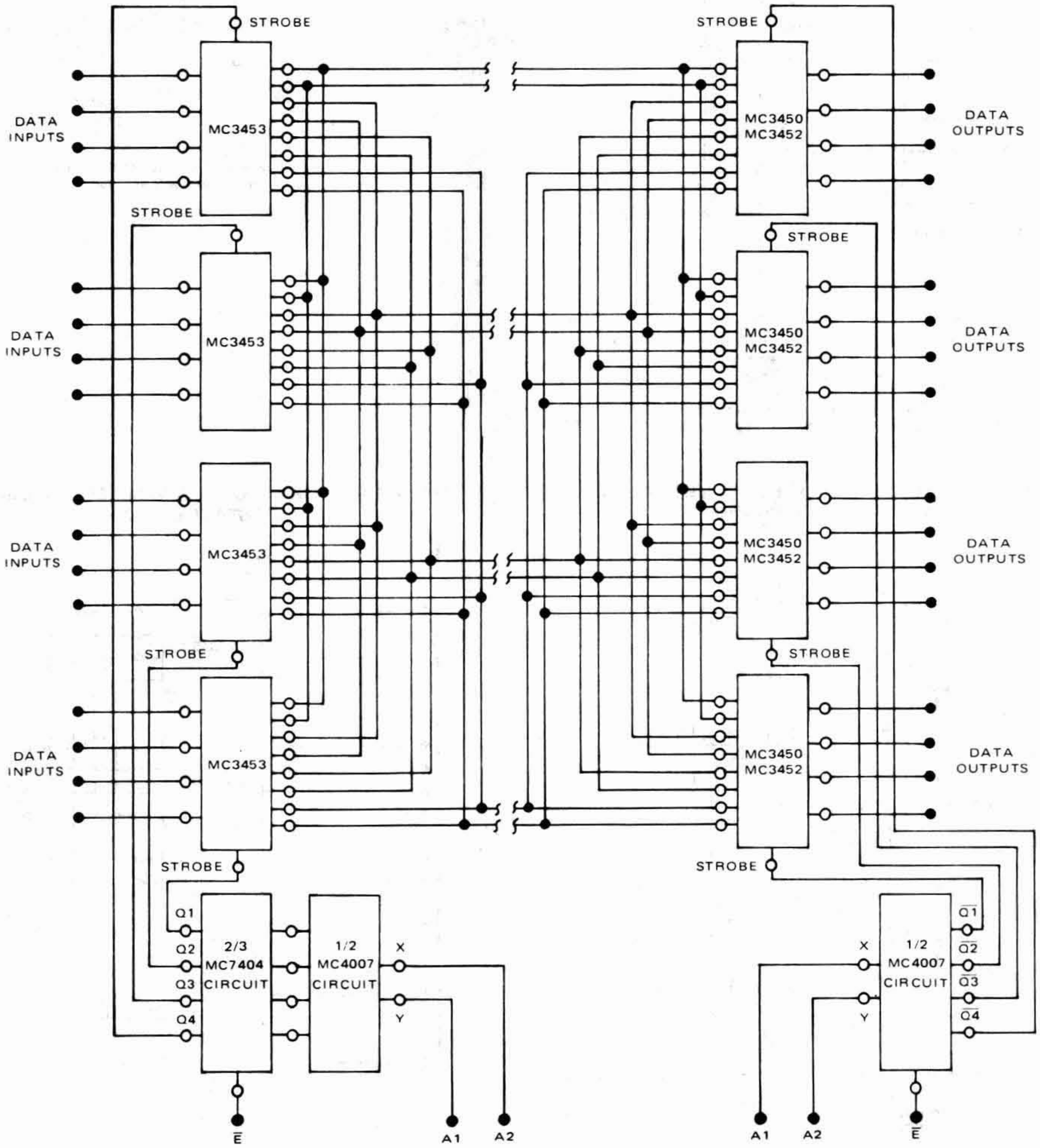
### FIGURE 16 – WIRED "OR" DATA SELECTION USING THREE-STATE LOGIC



STROBE
MC3450
STROBE
MC3450
DATA OUTPUT
DATA LINES
MC3450
STROBE
MC3450
STROBE
Q1
Q2
Q3
Q4
X
A1
A2
Y
1/2 MC4007 CIRCUIT
Ē

## APPLICATIONS INFORMATION (continued)

FIGURE 17 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING


STROBE
DATA INPUTS
MC3453
STROBE
DATA INPUTS
MC3453
DATA INPUTS
MC3453
STROBE
DATA INPUTS
MC3453
STROBE
Q1
Q2
Q3
Q4
2/3 MC7404 CIRCUIT
1/2 MC4007 CIRCUIT
X
Y
$\overline{E}$
A1
A2
STROBE
MC3450 MC3452
DATA OUTPUTS
STROBE
MC3450 MC3452
DATA OUTPUTS
MC3450 MC3452
DATA OUTPUTS
STROBE
MC3450 MC3452
DATA OUTPUTS
STROBE
X
Y
1/2 MC4007 CIRCUIT
$\overline{Q1}$
$\overline{Q2}$
$\overline{Q3}$
$\overline{Q4}$
A1
A2
$\overline{E}$

**MOTOROLA**

# MC3453

## QUAD LINE DRIVER WITH COMMON INHIBIT INPUT

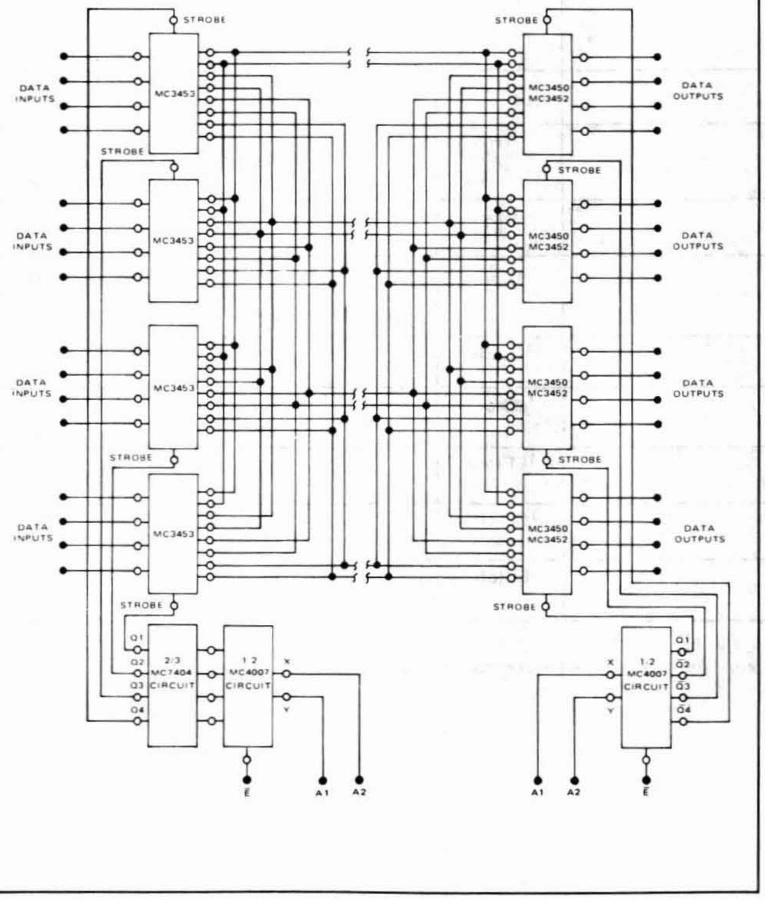
**SILICON MONOLITHIC INTEGRATED CIRCUIT**

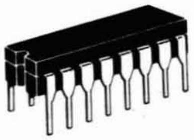
## MTTL COMPATIBLE QUAD LINE DRIVER

The MC3453 features four SN75110 type line drivers with a common inhibit input. When the inhibit input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the inhibit is low, all channel outputs are nonconductive (transistors biased to cut-off). This minimizes loading in party-line systems where a large number of drivers share the same line.

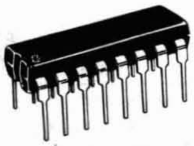
- Four Independent Drivers with Common Inhibit Input
- −3.0 Volts Output Common-Mode Voltage Over Entire Operating Range
- Improved Driver Design Exceeds Performance of Popular SN75110

FIGURE 1 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING


STROBE
DATA INPUTS
MC3453
MC3450
MC3452
DATA OUTPUTS
Q1
Q2
Q3
Q4
2/3 MC7404 CIRCUIT
1/2 MC4007 CIRCUIT
X
Y
E
A1
A2

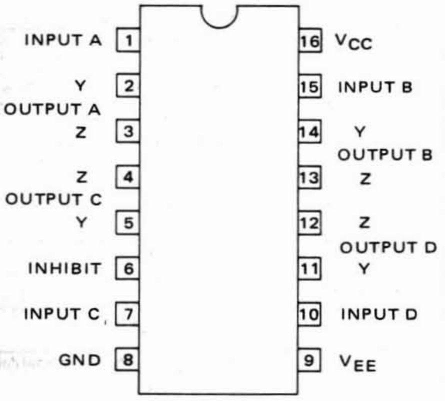


**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02



**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

**CONNECTION DIAGRAM**


INPUT A 1
Y OUTPUT A 2
Z 3
Z OUTPUT C 4
Y 5
INHIBIT 6
INPUT C 7
GND 8
16 VCC
15 INPUT B
14 Y OUTPUT B
13 Z
12 Z OUTPUT D
11 Y
10 INPUT D
9 VEE

**TRUTH TABLE**
(positive logic)

| LOGIC INPUT | INHIBIT INPUT | OUTPUT CURRENT Z | OUTPUT CURRENT Y |
|---|---|---|---|
| H | H | On | Off |
| L | H | Off | On |
| H | L | Off | Off |
| L | L | Off | Off |

L = Low Logic Level
H = High Logic Level

**MAXIMUM RATINGS** ($T_A$ = 0 to +70°C unless otherwise noted.)

| Ratings | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>$V_{EE}$ | +7.0<br>-7.0 | Volts |
| Logic and Inhibitor Input Voltages | $V_{in}$ | 5.5 | Volts |
| Common-Mode Output Voltage Range | $V_{OCR}$ | -5.0 to +12 | Volts |
| Power Dissipation (Package Limitation) | $P_D$ | | |
| Plastic and Ceramic Dual In-Line Packages | | 1000 | mW |
| Derate above $T_A$ = +25°C | | 6.6 | mW/°C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range<br>Plastic and Ceramic Dual In-Line Packages | $T_{stg}$ | -65 to +150 | °C |

**RECOMMENDED OPERATING CONDITIONS** (See Notes 1 and 2.)

| Characteristic | Symbol | Min | Nom | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltages | $V_{CC}$<br>$V_{EE}$ | +4.75<br>-4.75 | +5.0<br>-5.0 | +5.25<br>-5.25 | Volts |
| Common-Mode Output Voltage Range | $V_{OCR}$ | | | | Volts |
| Positive | | 0 | – | +10 | |
| Negative | | 0 | – | -3.0 | |

Note 1. These voltage values are in respect to the ground terminal.

Note 2. When not using all four channels, unused outputs must be grounded.

**DEFINITIONS OF INPUT LOGIC LEVELS***

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-Level Input Voltage (at any input) | $V_{IH}$ | 2.0 | 5.5 | Volts |
| Low-Level Input Voltage (at any input) | $V_{IL}$ | 0 | 0.8 | Volts |

*The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0 to +70°C unless otherwise noted.)

| Characteristic## | Symbol | Min | Typ# | Max | Unit |
|---|---|---|---|---|---|
| High-Level Input Current (Logic Inputs) | $I_{IH_L}$ | | | | |
| ($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH_L}$ = 2.4 V) | | – | – | 40 | µA |
| ($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH_L}$ = $V_{CC}$ Max) | | – | – | 1.0 | mA |
| Low-Level Input Current (Logic Inputs)<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IL_L}$ = 0.4 V) | $I_{IL_L}$ | – | – | -1.6 | mA |
| High-Level Input Current (Inhibit Input) | $I_{IH_I}$ | | | | |
| ($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH_I}$ = 2.4 V) | | – | – | 40 | µA |
| ($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH_I}$ = $V_{CC}$ Max) | | – | – | 1.0 | mA |
| Low-Level Input Current (Inhibit Input)<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IL_I}$ = 0.4 V) | $I_{IL_I}$ | – | – | -1.6 | mA |
| Output Current ("on" state) | $I_{O(on)}$ | | | | mA |
| ($V_{CC}$ = Max, $V_{EE}$ = Max) | | – | 11 | 15 | |
| ($V_{CC}$ = Min, $V_{EE}$ = Min) | | 6.5 | 11 | – | |
| Output Current ("off" state)<br>($V_{CC}$ = Min, $V_{EE}$ = Min) | $I_{O(off)}$ | – | 5.0 | 100 | µA |
| Supply Current from $V_{CC}$ (with driver enabled)<br>($V_{IL_L}$ = 0.4 V, $V_{IH_I}$ = 2.0 V) | $I_{CC(on)}$ | – | 35 | 50 | mA |
| Supply Current from $V_{EE}$ (with driver enabled)<br>($V_{IL_L}$ = 0.4 V, $V_{IH_I}$ = 2.0 V) | $I_{EE(on)}$ | – | 65 | 90 | mA |
| Supply Current from $V_{CC}$ (with driver inhibited)<br>($V_{IL_L}$ = 0.4 V, $V_{IL_I}$ = 0.4 V) | $I_{CC(off)}$ | – | 35 | 50 | mA |
| Supply Current from $V_{EE}$ (with driver inhibited)<br>($V_{IL_L}$ = 0.4 V, $V_{IL_I}$ = 0.4 V) | $I_{EE(off)}$ | – | 25 | 40 | mA |

#All typical values are at $V_{CC}$ = +5.0 V, $V_{EE}$ = -5.0 V, $T_A$ = +25°C.

##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
Ground unused inputs and outputs.

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = +5.0 V, $V_{EE}$ = −5.0 V, $T_A$ = +25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Time from Logic Input to Output Y or Z ($R_L$ = 50 ohms, $C_L$ = 40 pF) | $t_{PLH_L}$<br>$t_{PHL_L}$ | –<br>– | 9.0<br>9.0 | 15<br>15 | ns |
| Propagation Delay Time from Inhibit Input to Output Y or Z ($R_L$ = 50 ohms, $C_L$ = 40 pF) | $t_{PLH_I}$<br>$t_{PHL_I}$ | –<br>– | 16<br>20 | 25<br>25 | ns |

FIGURE 2 – LOGIC INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS

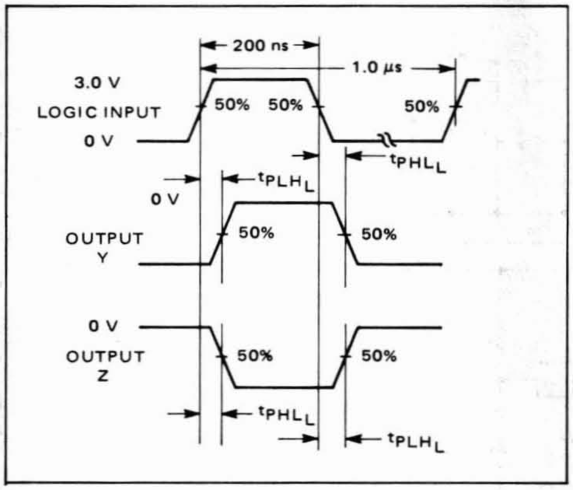
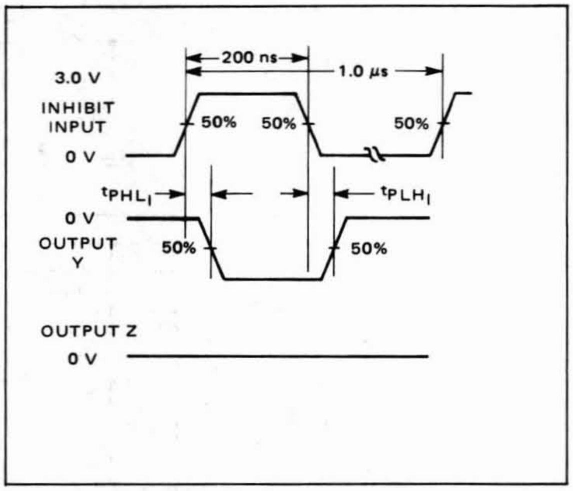
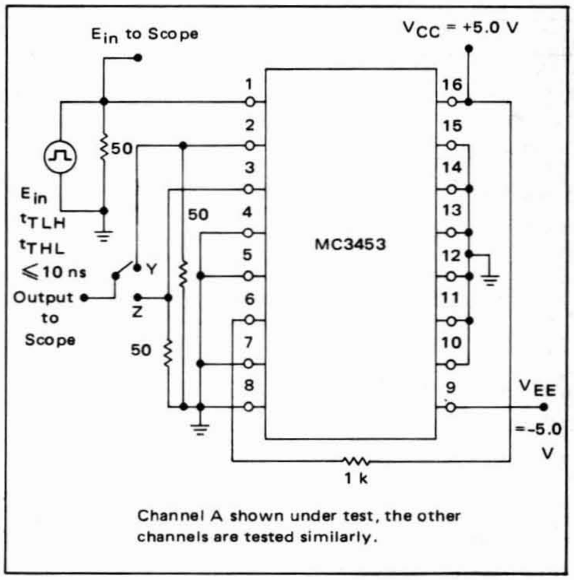

200 ns
1.0 µs
3.0 V
LOGIC INPUT
0 V
50%
50%
50%
$t_{PHL_L}$
$t_{PLH_L}$
0 V
OUTPUT Y
50%
50%
0 V
OUTPUT Z
50%
50%
$t_{PHL_L}$
$t_{PLH_L}$

FIGURE 3 – INHIBIT INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS


200 ns
1.0 µs
3.0 V
INHIBIT INPUT
0 V
50%
50%
50%
$t_{PHL_I}$
$t_{PLH_I}$
0 V
OUTPUT Y
50%
50%
OUTPUT Z
0 V

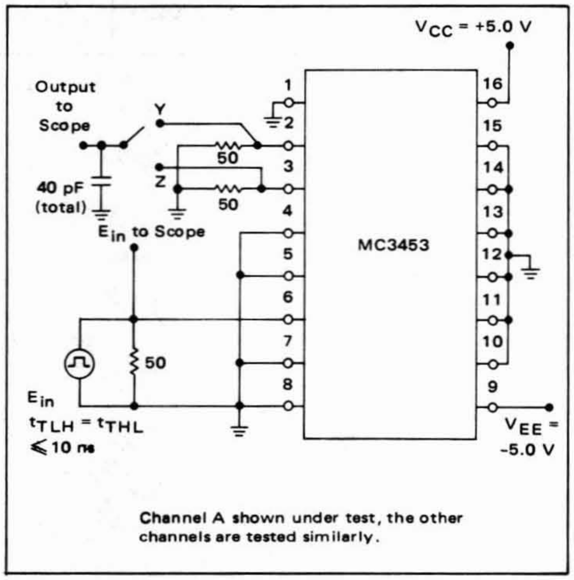
## TEST CIRCUITS

FIGURE 4 – LOGIC INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT


$E_{in}$ to Scope
$V_{CC}$ = +5.0 V
50
$E_{in}$
$t_{TLH}$
$t_{THL}$
⩽10 ns
Y
Output to Scope
Z
50
50
MC3453
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
$V_{EE}$ = −5.0 V
1 k

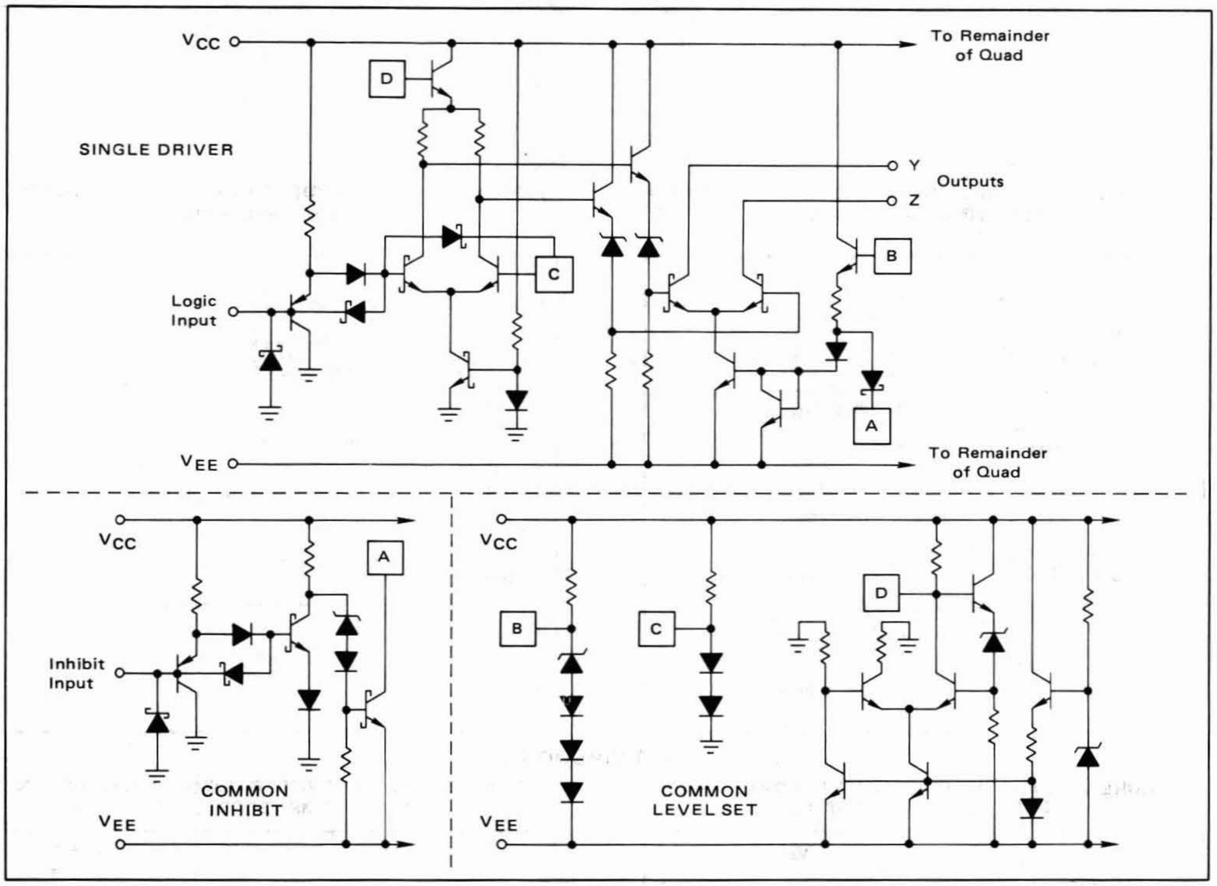
Channel A shown under test, the other channels are tested similarly.

FIGURE 5 – INHIBIT INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT


$V_{CC}$ = +5.0 V
Output to Scope
Y
50
Z
50
40 pF (total)
$E_{in}$ to Scope
MC3453
50
$E_{in}$
$t_{TLH}$ = $t_{THL}$
⩽10 ns
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
$V_{EE}$ = −5.0 V

Channel A shown under test, the other channels are tested similarly.

**FIGURE 6 – CIRCUIT SCHEMATIC**
**(1/4 Circuit Shown)**


VCC
To Remainder of Quad
D
SINGLE DRIVER
Y
Outputs
Z
C
B
Logic Input
A
VEE
To Remainder of Quad
VCC
A
Inhibit Input
COMMON INHIBIT
VEE
VCC
D
B
C
COMMON LEVEL SET
VEE

**MOTOROLA**

# MC3481
# MC3485

## QUAD SINGLE-ENDED LINE DRIVER

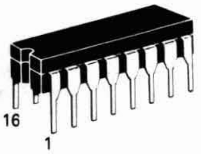
The MC3481 and MC3485 are quad single-ended line drivers specifically designed to meet the IBM 360/370 I/O specification (GA22-6974-3).

Output levels are guaranteed over the full range of output load and fault conditions. Compliance with the IBM requirements for fault protection, flagging, and power up/power down protection for the bus make this an ideal line driver for party line operations.

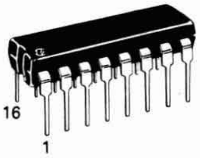
- Separate Enable and Fault Flags — MC3481
- Common Enable and Fault Flag — MC3485
- Power Up/Down Does Not Disturb Bus
- Schottky Circuitry for High-Speed — PNP Inputs
- Internal Bootstraps for Faster Rise Times
- Driver Output Current Foldback Protection
- MC3485 has LS Totem Pole $\overline{\text{Driver Output}}$

## IBM 360/370 QUAD LINE DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

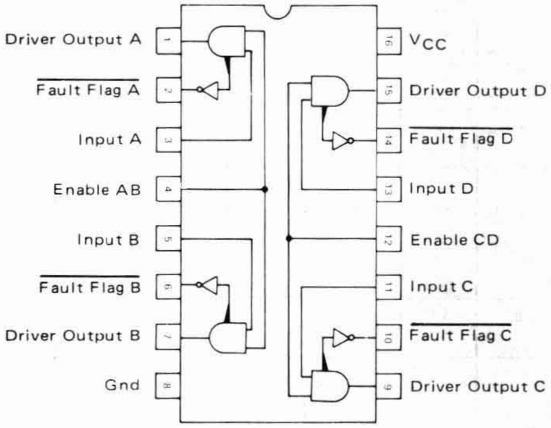


**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

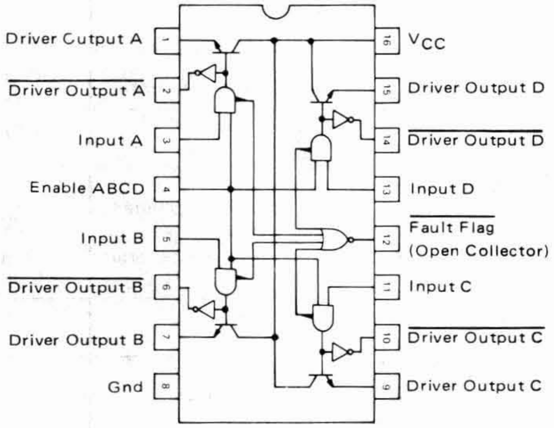


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

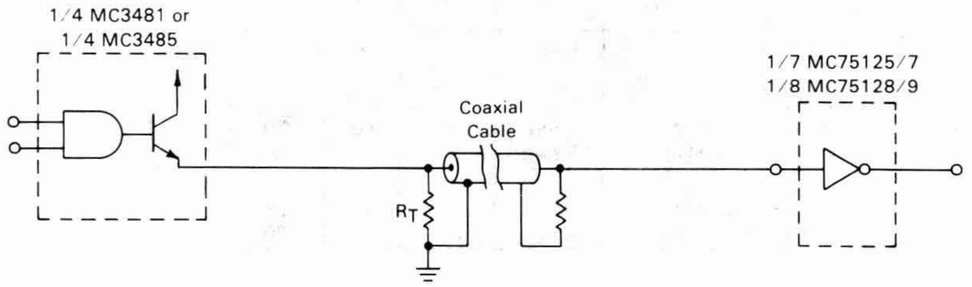
MC3481
DUAL ENABLE
INDIVIDUAL FAULT FLAG


Driver Output A
$\overline{\text{Fault Flag A}}$
Input A
Enable AB
Input B
$\overline{\text{Fault Flag B}}$
Driver Output B
Gnd
VCC
Driver Output D
$\overline{\text{Fault Flag D}}$
Input D
Enable CD
Input C
$\overline{\text{Fault Flag C}}$
Driver Output C
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

MC3485
COMMON ENABLE
COMMON FAULT FLAG


Driver Output A
$\overline{\text{Driver Output A}}$
Input A
Enable ABCD
Input B
$\overline{\text{Driver Output B}}$
Driver Output B
Gnd
VCC
Driver Output D
$\overline{\text{Driver Output D}}$
Input D
$\overline{\text{Fault Flag}}$
(Open Collector)
Input C
$\overline{\text{Driver Output C}}$
Driver Output C
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

### TYPICAL APPLICATION


1/4 MC3481 or
1/4 MC3485
Coaxial
Cable
$R_T$
1/7 MC75125/7
1/8 MC75128/9

**RECOMMENDED OPERATING CONDITIONS**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.95 | Vdc |
| High Level Output Current | $I_{OH}$ | — | — | -59.3 | mA |
| Operating Ambient Temperature Range | $T_A$ | 0 | — | +70 | °C |

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at $T_A$ = 25°C and $V_{CC}$ = +5.0 V)

| Characteristic | Symbol | MC3481 | | | MC3485 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **High-Level Input Voltage Note 2** | $V_{IH}$ | 2.0 | — | — | 2.0 | — | — | V |
| **Low-Level Input Voltage Note 2** | $V_{IL}$ | — | — | 0.8 | — | — | 0.8 | V |
| High-Level Input Current | $I_{IH}$ | | | | | | | µA |
| ($V_{CC}$ = 4.5 V, $V_{IH}$ = 2.7 V) - Input | | — | — | 20 | — | — | 20 | |
| Enable | | — | — | 40 | — | — | 80 | |
| ($V_{CC}$ = 4.5 V, $V_{IH}$ = 5.5 V) - Input | | — | — | 100 | — | — | 100 | |
| Enable | | — | — | 200 | — | — | 400 | |
| Low-Level Input Current | $I_{IL}$ | | | | | | | µA |
| ($V_{CC}$ = 5.95 V, $V_{IL}$ = 0.4 V) - Input | | — | — | -250 | — | — | -250 | |
| Enable | | — | — | -500 | — | — | -1000 | |
| Input Clamp Voltage | $V_{IC}$ | | | | | | | V |
| ($I_{IC}$ = -18 mA) | | — | — | -1.5 | — | — | -1.5 | |
| High-Level Driver Output Voltage | | | | | | | | V |
| ($V_{CC}$ = 4.5 V, $V_{IH}$ = 2.0 V, $I_{OH}$ = -59.3 mA) | $V_{OH(D)}$ | 3.11 | 3.6 | — | 3.11 | 3.6 | — | |
| ($V_{CC}$ = 5.25 V, $V_{IH}$ = 2.0 V, $I_{OH}$ = -41 mA) | $V_{OH(DS)}$ | 3.9 | — | — | 3.9 | — | — | |
| Low-Level Driver Output Voltage | | | | | | | | V |
| ($V_{CC}$ = 5.5 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = -240 µA) | $V_{OL(D)}$ | — | — | +0.15 | — | — | +0.15 | |
| ($V_{CC}$ = 5.95 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = -1.0 mA) | $V_{OL(DS)}$ | — | — | +0.15 | — | — | +0.15 | |
| Driver Output Short Circuit Current | | | | | | | | mA |
| ($V_{CC}$ = 5.5 V, $V_{IH}$ = 2.0 V, $V_{OS}$ = 0 V) | $I_{OS(D)}$ | — | — | -5.0 | — | — | -5.0 | |
| ($V_{CC}$ = 5.95 V, $V_{IH}$ = 2.0 V, $V_{OS}$ = 0 V) | $I_{OS(DS)}$ | — | — | -5.0 | — | — | -5.0 | |
| Driver Output Reverse Leakage Current | | | | | | | | µA |
| ($V_{CC}$ = 4.5 V, $V_{IL}$ = 0 V, $V_O$ = 3.11 V) | $I_{OR1}$ | — | — | +100 | — | — | +100 | |
| ($V_{CC}$ = 0 V, $V_{IL}$ = 0 V, $V_O$ = 3.11 V) | $I_{OR2}$ | — | — | +200 | — | — | +200 | |
| High-Level $\overline{\text{Driver Output}}$ Voltage<br>($V_{CC}$ = 4.5 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = -400 µA) | $V_{OH(\overline{D})}$ | — | — | — | 2.5 | 3.0 | — | V |
| Low-Level $\overline{\text{Driver Output}}$ Voltage<br>($V_{CC}$ = 4.5 V, $V_{IH}$ = 2.0 V, $I_{OL}$ = +8.0 mA) | $V_{OL(\overline{D})}$ | — | — | — | — | — | 0.5 | V |
| $\overline{\text{Driver Output}}$ Short Circuit Current | | | | | | | | mA |
| ($V_{CC}$ = 5.5 V, $V_{OS}$ = 0 V, only one output shorted at a time) | $I_{OS(\overline{D})}$ | — | — | — | -15 | -60 | -100 | |
| ($V_{CC}$ = 5.95 V, $V_{OS}$ = 0 V, only one output shorted at a time) | $I_{OS(\overline{D}S)}$ | — | — | — | -15 | — | -110 | |
| High-Level $\overline{\text{Fault Flag}}$ Output Voltage<br>($V_{CC}$ = 4.5 V, $I_{OH}$ = -400 µA) | $V_{OH(\overline{F})}$ | 2.5 | 3.0 | — | — | — | — | V |
| Low-Level $\overline{\text{Fault Flag}}$ Output Voltage<br>($V_{CC}$ = 4.5 V, $V_{IH}$ = 2.0 V, $I_{OL}$ = +8.0 mA, Driver Output shorted to Ground | $V_{OL(\overline{F})}$ | — | — | 0.5 | — | — | 0.5 | V |
| $\overline{\text{Fault Flag}}$ Output Short Circuit Current | | | | | | | | mA |
| ($V_{CC}$ = 5.5 V, $V_{OS}$ = 0 V, only one output shorted at a time) | $I_{OS(\overline{F})}$ | -15 | — | -100 | — | — | — | |
| ($V_{CC}$ = 5.95 V, $V_{OS}$ = 0 V, only one output shorted at a time) | $I_{OS(\overline{F}S)}$ | -15 | — | -110 | — | — | — | |
| High-Level $\overline{\text{Fault Flag}}$ Output Current<br>($V_{CC}$ = 5.95 V, $V_{OH}$ = 5.95 V) | $I_{OH(\overline{F})}$ | — | — | — | — | — | +100 | µA |
| High-Level Power Supply Current | | | | | | | | mA |
| ($V_{CC}$ = 5.5 V, $V_{IH}$ = 2.0 V, no output loading) | $I_{CCH}$ | — | 50 | 70 | — | 55 | 75 | |
| ($V_{CC}$ = 5.95 V, $V_{IH}$ = 2.0 V, no output loading) | $I_{CCHS}$ | — | — | 80 | — | — | 85 | |
| Low-Level Power Supply Current | | | | | | | | mA |
| ($V_{CC}$ = 5.5 V, $V_{IL}$ = 0.8 V, no output loading) | $I_{CCL}$ | — | 35 | 55 | — | 35 | 55 | |
| ($V_{CC}$ = 5.95 V, $V_{IL}$ = 0.8 V, no output loading) | $I_{CCLS}$ | — | — | 70 | — | — | 70 | |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power Supply Voltage | | $V_{CC}$ | +7.0 | V |
| Input Voltage | | $V_I$ | 10 | V |
| Driver Output Voltage | | $V_O$ | 5.5 | V |
| Power Dissipation (Package Limitation) | Ceramic Package<br>Plastic Package | $P_D$ | 1150<br>962 | mW |
| Derate Above $T_A$ = 25°C | | $1/R_{\theta JA}$ | 7.7 | mW/°C |
| Operating Ambient Temperature Range | | $T_A$ | 0 to +70 | °C |
| Junction Temperature | Ceramic Package<br>Plastic Package | $T_J$ | +175<br>+150 | °C |
| Storage Temperature Range | | $T_{stg}$ | −65 to +150 | °C |

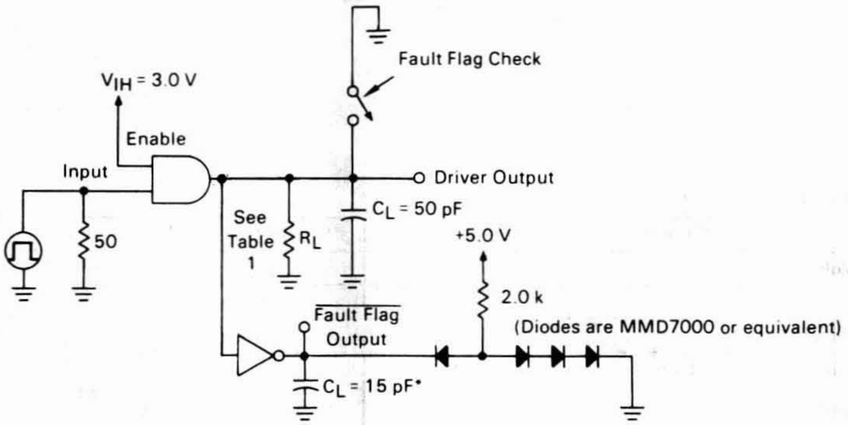
**SWITCHING CHARACTERISTICS** (See Note 1. Unless otherwise noted, these specifications apply over recommended temperature range. I/O Driver characteristics are guaranteed for $V_{CC}$ = 5.0 V ±10% and Select-Out Driver characteristics are guaranteed for $V_{CC}$ = 5.25 to 5.95 V. Typical values measured at $T_A$ = 25°C and $V_{CC}$ = 5.0 V. See Tables 1 and 2, Figures 1 and 2 for load conditions.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Time | | | | | ns |
| High-to-Low-Level, Driver Output | | | | | |
| As I/O Driver | $t_{PHL(D)}$ | — | 18 | — | |
| As Select-Out Driver | $t_{PHL(DS)}$ | — | 19 | — | |
| Low-to-High-Level, Driver Output | | | | | |
| As I/O Driver | $t_{PLH(D)}$ | — | 20 | — | |
| As Select-Out Driver | $t_{PLH(DS)}$ | — | 21 | — | |
| High-to-Low-Level, $\overline{\text{Driver Output}}$ | | | | | |
| As I/O Driver | $t_{PHL(\overline{D})}$ | — | 25 | — | |
| As Select-Out Driver | $t_{PHL(\overline{DS})}$ | — | 26 | — | |
| Low-to-High-Level, $\overline{\text{Driver Output}}$ | | | | | |
| As I/O Driver | $t_{PLH(\overline{D})}$ | — | 25 | — | |
| As Select-Out Driver | $t_{PLH(\overline{DS})}$ | — | 26 | — | |
| High-to-Low-Level, $\overline{\text{Fault Flag}}$ — MC3481 | | | | | |
| As I/O Driver | $t_{PHL(\overline{F})}$ | — | 45 | — | |
| As Select-Out Driver | $t_{PHL(\overline{FS})}$ | — | 47 | — | |
| Low-to-High-Level, $\overline{\text{Fault Flag}}$ — MC3481 | | | | | |
| As I/O Driver | $t_{PLH(\overline{F})}$ | — | 40 | — | |
| As Select-Out Driver | $t_{PLH(\overline{FS})}$ | — | 42 | — | |
| Ratio of Propagation Delay Times<br>As I/O Driver | $\frac{t_{PLH(D)}}{t_{PHL(D)}}$ | — | 1.0 | — | |

Note 1. Reference IBM specification GA22-6974-3 for test terminology.

2. The fault protection circuitry of the MC3481/85 requires relatively clean input voltage waveforms for current operation. Noise pulses which enter the threshold region (0.8 to 2.0 V) may cause the output to enter the fault protect mode. To exit the protect mode, it is necessary to gate an input of the effected driver to the low logic state.

FIGURE 1 — MC3481 AC TEST CIRCUIT AND WAVEFORMS


Fault Flag Check
$V_{IH}$ = 3.0 V
Enable
Input
Driver Output
See Table 1
$R_L$
50
$C_L$ = 50 pF
+5.0 V
2.0 k
(Diodes are MMD7000 or equivalent)
Fault Flag Output
$C_L$ = 15 pF*

* Load Capacitance shown includes Fixture and Probe Capacitance

| Table | Driver Application | |
|---|---|---|
| 1 | I/O | Select-Out |
| $V_{OH}$ | 3.11 V | 3.9 V |
| Input Frequency | 5 MHz | 1 MHz |
| Input Pulse Width | 100 ns | 500 ns |
| Input Amplitude | 0 V to 4 V | 0 V to 4 V |
| Input $t_{TLH}$ | ≤6 ns | ≤ 6 ns |
| Input $t_{THL}$ | ≤6 ns | ≤6 ns |
| Load Resistance ($R_L$) | 50 | 90 |

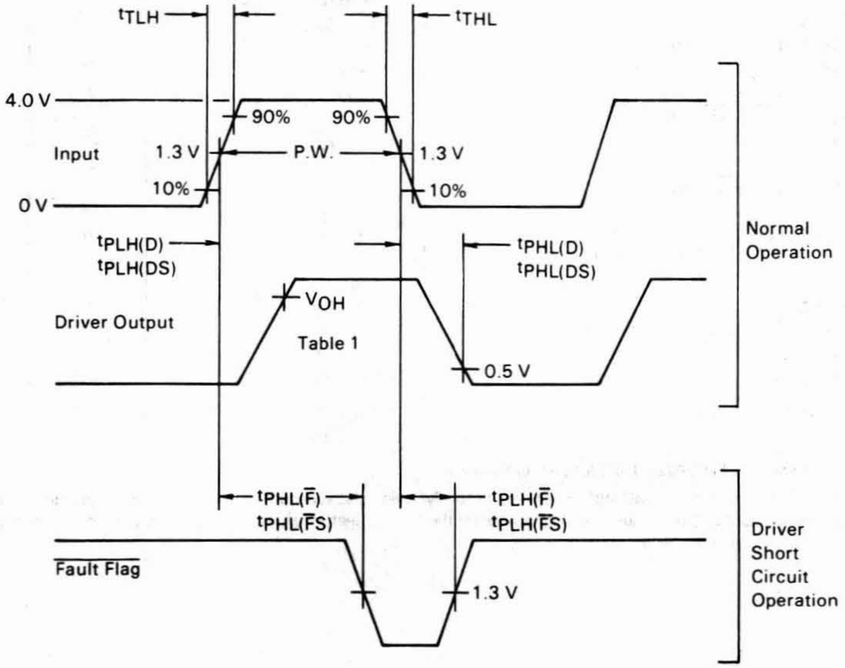
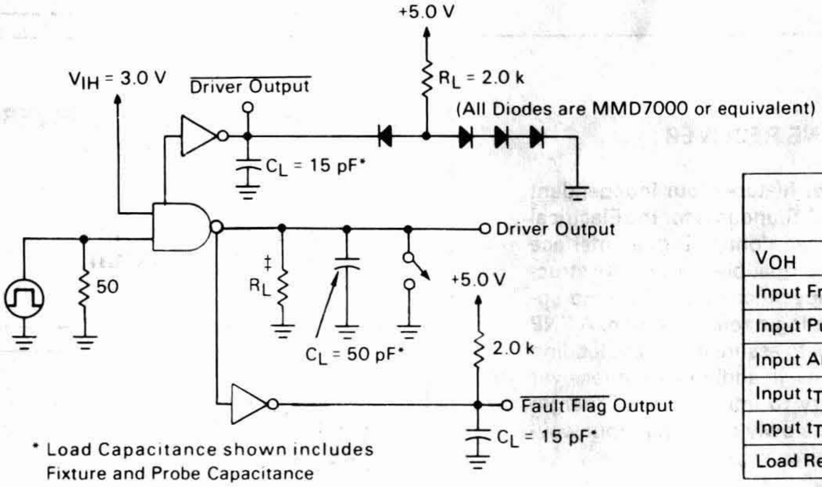

$t_{TLH}$
$t_{THL}$
4.0 V
90%
90%
Input
1.3 V
P.W.
1.3 V
10%
10%
0 V
$t_{PLH(D)}$
$t_{PLH(DS)}$
$t_{PHL(D)}$
$t_{PHL(DS)}$
Driver Output
$V_{OH}$
Table 1
0.5 V
Normal Operation
$t_{PHL(\overline{F})}$
$t_{PHL(\overline{FS})}$
$t_{PLH(\overline{F})}$
$t_{PLH(\overline{FS})}$
Fault Flag
1.3 V
Driver Short Circuit Operation

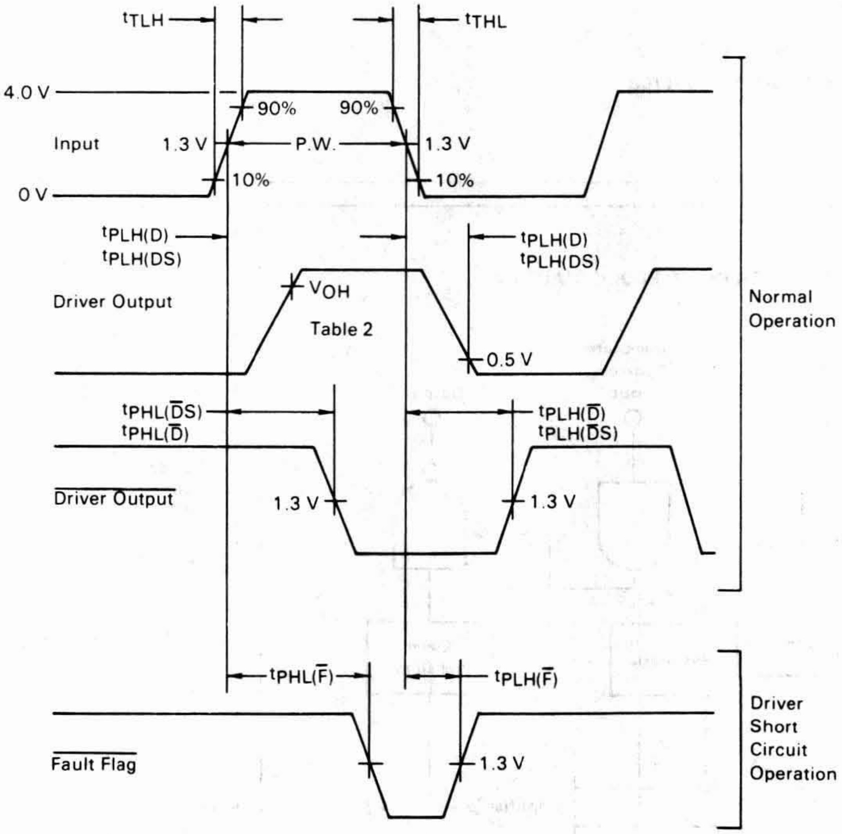
FIGURE 2 — MC3485 AC TEST CIRCUIT AND WAVEFORMS


+5.0 V
$R_L$ = 2.0 k
(All Diodes are MMD7000 or equivalent)
$V_{IH}$ = 3.0 V
Driver Output (overlined)
$C_L$ = 15 pF*
Driver Output
50
‡
$R_L$
$C_L$ = 50 pF*
+5.0 V
2.0 k
Fault Flag Output (overlined)
$C_L$ = 15 pF*

* Load Capacitance shown includes Fixture and Probe Capacitance

‡ See Table 2

| Table 2 | Driver Application | |
|---|---|---|
| | I/O | Select-Out |
| $V_{OH}$ | 3.11 V | 3.9 V |
| Input Frequency | 5 MHz | 1 MHz |
| Input Pulse Width | 100 ns | 500 ns |
| Input Amplitude | 0 V to 4 V | 0 V to 4 V |
| Input $t_{TLH}$ | ≤6 ns | ≤6 ns |
| Input $t_{THL}$ | ≤6 ns | ≤6 ns |
| Load Resistance ($R_L$) | 50 | 90 |


$t_{TLH}$
$t_{THL}$
4.0 V
Input
0 V
1.3 V
90%
10%
P.W.
$t_{PLH(D)}$
$t_{PLH(DS)}$
Driver Output
$V_{OH}$
Table 2
0.5 V
$t_{PHL(\overline{DS})}$
$t_{PHL(\overline{D})}$
$t_{PLH(\overline{D})}$
$t_{PLH(\overline{DS})}$
Driver Output (overlined)
1.3 V
$t_{PHL(\overline{F})}$
$t_{PLH(\overline{F})}$
Fault Flag (overlined)
Normal Operation
Driver Short Circuit Operation

**MOTOROLA**

# MC3486

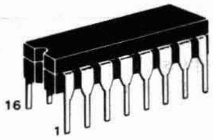
## QUAD RS-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

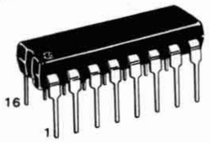
## QUAD RS-422/423 LINE RECEIVER

Motorola's Quad RS-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of MC3486 features include:

- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis −30 mV (Typ) @ Zero Volts Common Mode
- Fast Propagation Times −25 ns (Typ)
- TTL Compatible
- Single 5.0 V Supply Voltage
- DS 3486 Provides Second Source

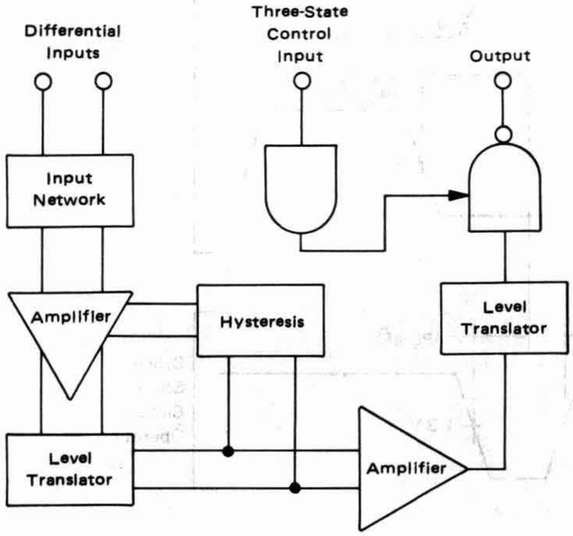


**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

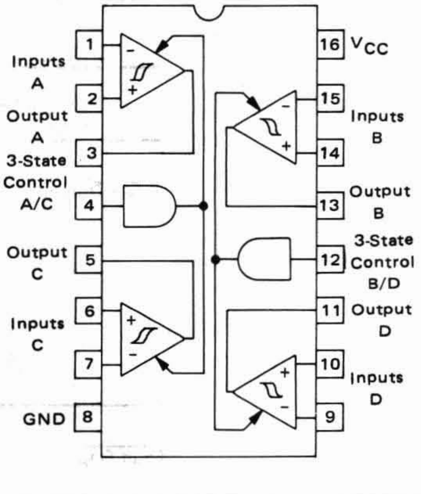


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### RECEIVER CHAIN BLOCK DIAGRAM


Differential Inputs
Three-State Control Input
Output
Input Network
Amplifier
Hysteresis
Level Translator
Level Translator
Amplifier

### PIN CONNECTIONS


Inputs A
1
2
Output A
3
3-State Control A/C
4
Output C
5
Inputs C
6
7
GND
8
16
VCC
15
Inputs B
14
13
Output B
12
3-State Control B/D
11
Output D
10
Inputs D
9

| ORDERING INFORMATION | | |
|---|---|---|
| DEVICE | TEMPERATURE RANGE | PACKAGE |
| MC3486L | 0 to +70°C | Ceramic DIP |
| MC3486P | 0 to +70°C | Plastic DIP |

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 8.0 | Vdc |
| Input Common Mode Voltage | $V_{ICM}$ | ±15 | Vdc |
| Input Differential Voltage | $V_{ID}$ | ±25 | Vdc |
| Three-State Control Input Voltage | $V_I$ | 8.0 | Vdc |
| Output Sink Current | $I_O$ | 50 | mA |
| Storage Temperature | $T_{stg}$ | -65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | | °C |
| Ceramic Package | | +175 | |
| Plastic Package | | +150 | |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

## RECOMMENDED OPERATING CONDITIONS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.75 to 5.25 | Vdc |
| Operating Ambient Temperature | $T_A$ | 0 to +70 | °C |
| Input Common Mode Voltage Range | $V_{ICR}$ | -7.0 to +7.0 | Vdc |
| Input Differential Voltage Range | $V_{IDR}$ | 6.0 | Vdc |

## ELECTRICAL CHARACTERISTICS

(Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25^oC$, $V_{CC} = 5.0$ V and $V_{IK} = 0$ V. See Note 1.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage — High Logic State (Three-State Control) | $V_{IH}$ | 2.0 | – | – | V |
| Input Voltage — Low Logic State (Three-State Control) | $V_{IL}$ | – | – | 0.8 | V |
| Differential Input Threshold Voltage (Note 4) ($-7.0\ V \leq V_{IC} \leq 7.0\ V$, $V_{IH} = 2.0$ V) | $V_{TH(D)}$ | | | | V |
| ($I_O = -0.4$ mA, $V_{OH} \geq 2.7$ V) | | – | – | 0.2 | |
| ($I_O = 8.0$ mA, $V_{OL} \geq 0.5$ V) | | – | – | -0.2 | |
| Input Bias Current ($V_{CC} = 0$ V or 5.25) (Other Inputs at 0 V) | $I_{IB(D)}$ | | | | mA |
| ($V_I = -10$ V) | | – | – | -3.25 | |
| ($V_I = -3.0$ V) | | – | – | -1.50 | |
| ($V_I = +3.0$ V) | | – | – | +1.50 | |
| ($V_I = +10$ V) | | – | – | +3.25 | |
| Input Balance and Output Level ($-7.0\ V \leq V_{IC} \leq 7.0\ V$, $V_{IH} = 2.0$ V, See Note 3) | | | | | V |
| ($I_O = -0.4$ mA, $V_{ID} = 0.4$ V) | $V_{OH}$ | 2.7 | – | – | |
| ($I_O = 8.0$ mA, $V_{ID} = -0.4$ V) | $V_{OL}$ | – | – | 0.5 | |
| Output Third State Leakage Current | $I_{OZ}$ | | | | µA |
| ($V_{I(D)} = +3.0$ V, $V_{IL} = 0.8$ V, $V_{OL} = 0.5$ V) | | – | – | -40 | |
| ($V_{I(D)} = -3.0$ V, $V_{IL} = 0.8$ V, $V_{OH} = 2.7$ V) | | – | – | 40 | |
| Output Short-Circuit Current ($V_{I(D)} = 3.0$ V, $V_{IH} = 2.0$ V, $V_O = 0$ V) See Note 2) | $I_{OS}$ | -15 | – | -100 | mA |
| Input Current — Low Logic State (Three-State Control) ($V_{IL} = 0.5$ V) | $I_{IL}$ | – | – | -100 | µA |
| Input Current — High Logic State (Three-State Control) | $I_{IH}$ | | | | µA |
| ($V_{IH} = 2.7$ V) | | – | – | 20 | |
| ($V_{IH} = 5.25$ V) | | – | – | 100 | |
| Input Clamp Diode Voltage (Three-State Control) ($I_{IK} = -10$ mA) | $V_{IK}$ | – | – | -1.5 | V |
| Power Supply Current ($V_{IL} = 0$ V) | $I_{CC}$ | – | – | 85 | mA |

**SWITCHING CHARACTERISTICS** (Unless otherwise noted, $V_{CC}$ = 5.0 V and $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Time — Differential Inputs to Output | | | | | ns |
| (Output High to Low) | $t_{PHL(D)}$ | – | – | 35 | |
| (Output Low to High) | $t_{PLH(D)}$ | – | – | 30 | |
| Propagation Delay time — Three-State Control to Output | | | | | ns |
| (Output Low to Third State) | $t_{PLZ}$ | – | – | 35 | |
| (Output High to Third State) | $t_{PHZ}$ | – | – | 35 | |
| (Output Third State to High) | $t_{PZH}$ | – | – | 30 | |
| (Output Third State to Low) | $t_{PZL}$ | – | – | 30 | |

**NOTES:**

1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Only one output at a time should be shorted.
3. Refer to EIA RS422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.

**FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS**

Propagation Delay Differential Input to Output

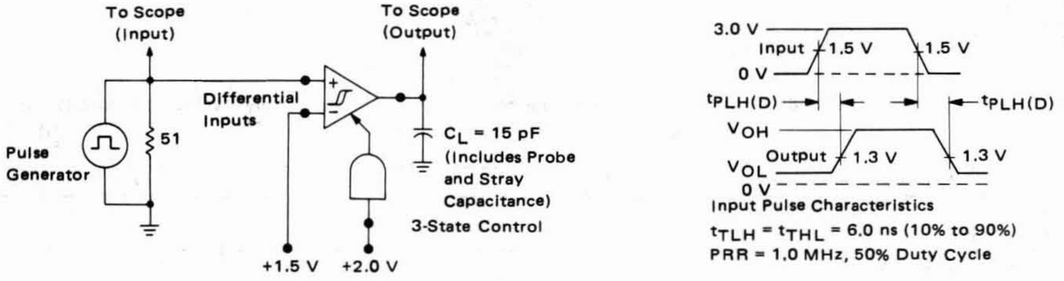
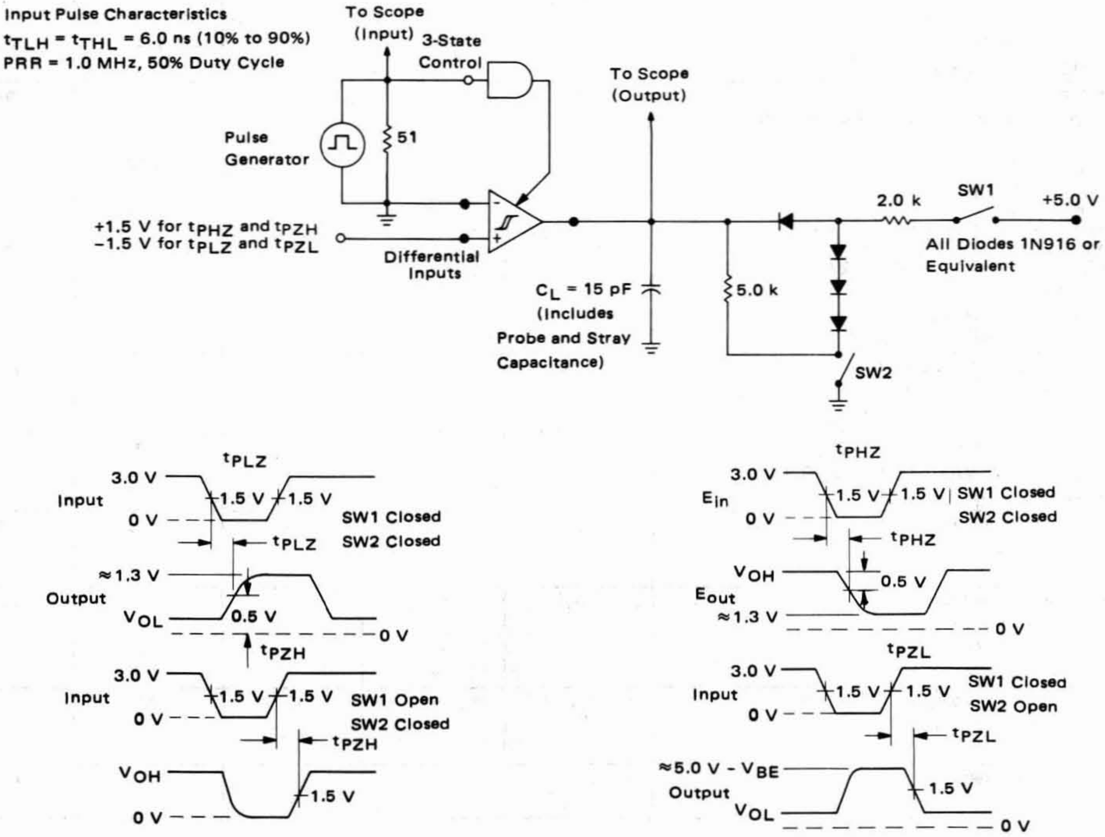

To Scope (Input)
To Scope (Output)
Differential Inputs
51
Pulse Generator
CL = 15 pF (Includes Probe and Stray Capacitance)
3-State Control
+1.5 V
+2.0 V
3.0 V
Input
1.5 V
1.5 V
0 V
tPLH(D)
tPLH(D)
VOH
Output
1.3 V
1.3 V
VOL
0 V
Input Pulse Characteristics
tTLH = tTHL = 6.0 ns (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle

**FIGURE 2 — PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT**


Input Pulse Characteristics
tTLH = tTHL = 6.0 ns (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle
To Scope (Input)
3-State Control
To Scope (Output)
Pulse Generator
51
+1.5 V for tPHZ and tPZH
−1.5 V for tPLZ and tPZL
Differential Inputs
2.0 k
SW1
+5.0 V
All Diodes 1N916 or Equivalent
CL = 15 pF (Includes Probe and Stray Capacitance)
5.0 k
SW2
tPLZ
3.0 V
Input
1.5 V
1.5 V
0 V
SW1 Closed
SW2 Closed
tPLZ
≈1.3 V
Output
VOL
0.5 V
0 V
tPZH
3.0 V
Input
1.5 V
1.5 V
0 V
SW1 Open
SW2 Closed
tPZH
VOH
1.5 V
0 V
tPHZ
3.0 V
Ein
1.5 V
1.5 V
SW1 Closed
SW2 Closed
0 V
tPHZ
VOH
0.5 V
Eout
≈1.3 V
0 V
tPZL
3.0 V
Input
1.5 V
1.5 V
SW1 Closed
SW2 Open
0 V
tPZL
≈5.0 V - VBE
Output
1.5 V
VOL
0 V

**MOTOROLA**

# MC3487

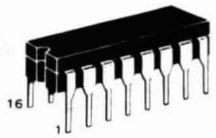
## QUAD RS-422 LINE DRIVER WITH THREE-STATE OUTPUTS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

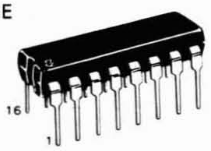
## QUAD LINE DRIVER WITH THREE-STATE OUTPUTS

Motorola's Quad RS-422 Driver features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down. A summary of MC3487 features include:

- Four Independent Driver Chains
- Three-State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Fast Propagation Times (Typ 15 ns)
- TTL Compatible
- Single 5 V Supply Voltage
- Output Rise and Fall Times Less Than 20 ns
- DS 3487 Provides Second Source

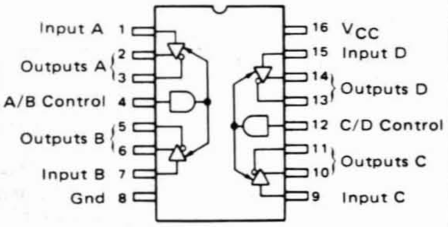


**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

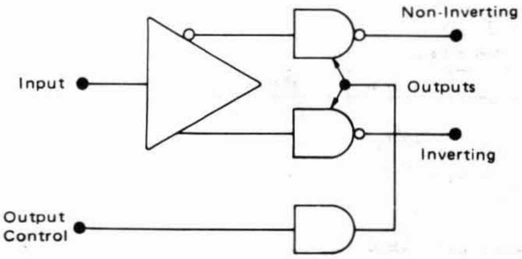


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### PIN CONNECTIONS


Input A 1
Outputs A 2
3
A/B Control 4
Outputs B 5
6
Input B 7
Gnd 8
16 VCC
15 Input D
14 Outputs D
13
12 C/D Control
11 Outputs C
10
9 Input C

### DRIVER BLOCK DIAGRAM


Non-Inverting
Input
Outputs
Inverting
Output Control

| TRUTH TABLE | | | |
|---|---|---|---|
| **Input** | **Control Input** | **Non-Inverting Output** | **Inverting Output** |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

| *ABSOLUTE MAXIMUM RATINGS | | | |
|---|---|---|---|
| **Rating** | **Symbol** | **Value** | **Unit** |
| Power Supply Voltage | $V_{CC}$ | 8.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Operating Junction Temperature Range | $T_J$ | | °C |
| Ceramic Package | | 175 | |
| Plastic Package | | 150 | |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

*"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted specifications apply $4.75\ V \leq V_{CC} \leq 5.25\ V$ and $0°C \leq T_A \leq 70°C$. Typical values measured at $V_{CC} = 5.0$ V, and $T_A = 25°C$.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage – Low Logic State | $V_{IL}$ | – | – | 0.8 | Vdc |
| Input Voltage – High Logic State | $V_{IH}$ | 2.0 | – | – | Vdc |
| Input Current – Low Logic State<br>($V_{IL} = 0.5$ V) | $I_{IL}$ | – | – | -400 | µA |
| Input Current – High Logic State | $I_{IH}$ | | | | µA |
| ($V_{IH} = 2.7$ V) | | – | – | +50 | |
| ($V_{IH} = 5.5$ V) | | – | – | +100 | |
| Input Clamp Voltage<br>($I_{IK} = -18$ mA) | $V_{IK}$ | – | – | -1.5 | V |
| Output Voltage – Low Logic State<br>($I_{OL} = 48$ mA) | $V_{OL}$ | – | – | 0.5 | V |
| Output Voltage – High Logic State<br>($I_{OH} = -20$ mA) | $V_{OH}$ | 2.5 | – | – | V |
| Output Short-Circuit Current<br>($V_{IH} = 2.0$ V) 2 | $I_{OS}$ | -40 | – | -140 | mA |
| Output Leakage Current – Hi-Z State | $I_{OL(Z)}$ | | | | µA |
| ($V_{IL} = 0.5$ V, $V_{IL(Z)} = 0.8$ V) | | – | – | ±100 | |
| ($V_{IH} = 2.7$ V, $V_{IL(Z)} = 0.8$ V) | | – | – | ±100 | |
| Output Leakage Current – Power OFF | $I_{OL(off)}$ | | | | µA |
| ($V_{OH} = 6.0$ V, $V_{CC} = 0$ V) | | – | – | +100 | |
| ($V_{OL} = -0.25$ V, $V_{CC} = 0$ V) | | – | – | -100 | |
| Output Offset Voltage Difference1 | $V_{OS}-\overline{V}_{OS}$ | – | – | ±0.4 | V |
| Output Differential Voltage 1 | $V_{OD}$ | 2.0 | – | – | V |
| Output Differential Voltage Difference 1 | $\lvert\Delta V_{OD}\rvert$ | – | – | ±0.4 | V |
| Power Supply Current | | | | | mA |
| (Control Pins = Gnd)3 | $I_{CCX}$ | – | – | 105 | |
| (Control Pins = 2.0 V) | $I_{CC}$ | – | – | 85 | |

1. See EIA Specification RS-422 for exact test conditions.
2. Only one output may be shorted at a time.
3. Circuit in three-state condition.

**SWITCHING CHARACTERISTICS** ($V_{CC} = 5.0$ V, $T_A = 25°C$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Times | | | | | ns |
| High to Low Output | $t_{PHL}$ | – | – | 20 | |
| Low to High Output | $t_{PLH}$ | – | – | 20 | |
| Output Transition Times – Differential | | | | | ns |
| High to Low Output | $t_{THL}$ | – | – | 20 | |
| Low to High Output | $t_{TLH}$ | – | – | 20 | |
| Propagation Delay – Control to Output | | | | | ns |
| ($R_L = 200\ \Omega$, $C_L = 50$ pF) | $t_{PHZ(E)}$ | – | – | 25 | |
| ($R_L = 200\ \Omega$, $C_L = 50$ pF) | $t_{PLZ(E)}$ | – | – | 25 | |
| ($R_L = \infty$, $C_L = 50$ pF) | $t_{PZH(E)}$ | – | – | 30 | |
| ($R_L = 200\ \Omega$, $C_L = 50$ pF) | $t_{PZL(E)}$ | – | – | 30 | |

FIGURE 1 – THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS

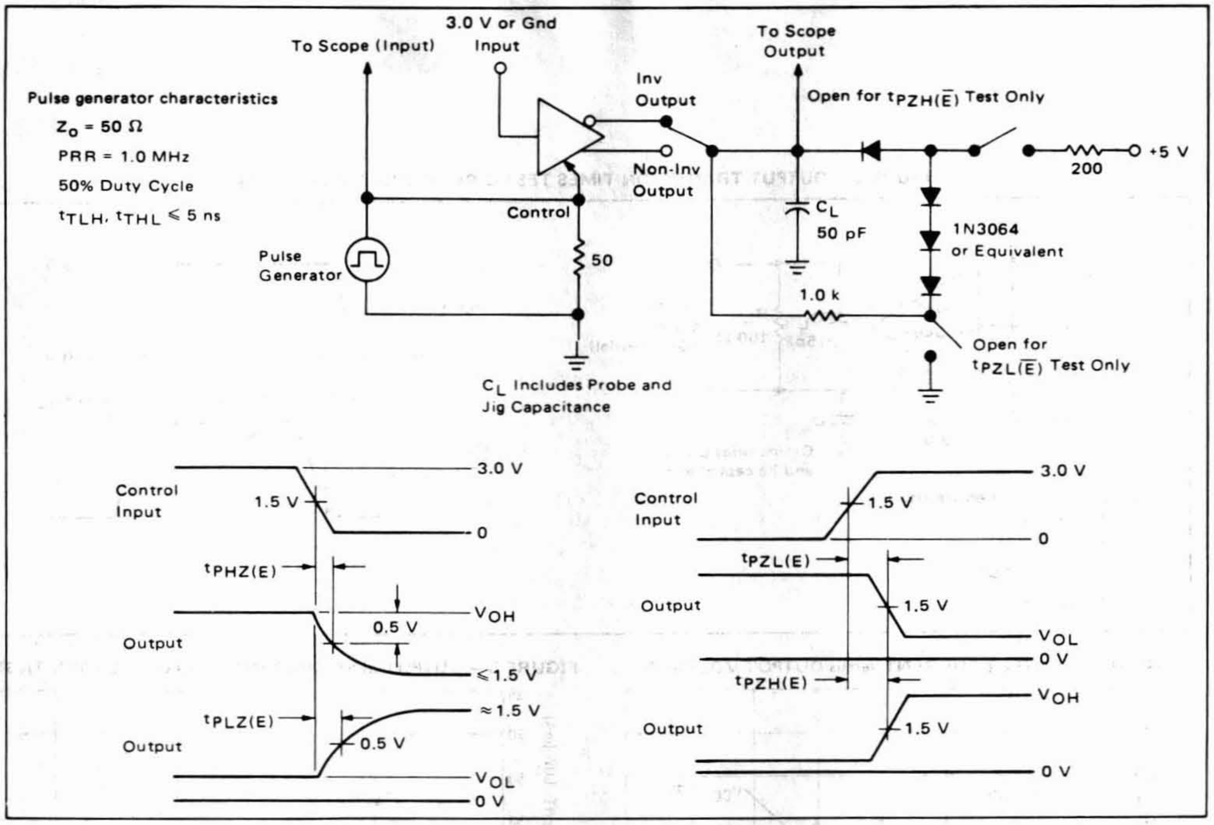

3.0 V or Gnd
Input
To Scope (Input)
To Scope
Output
Pulse generator characteristics
$Z_o = 50\ \Omega$
PRR = 1.0 MHz
50% Duty Cycle
$t_{TLH}, t_{THL} \leq 5$ ns
Inv
Output
Open for $t_{PZH(\overline{E})}$ Test Only
200
+5 V
Non-Inv
Output
Control
$C_L$
50 pF
1N3064
or Equivalent
Pulse
Generator
50
1.0 k
Open for
$t_{PZL(\overline{E})}$ Test Only
$C_L$ Includes Probe and
Jig Capacitance
Control
Input
1.5 V
3.0 V
0
$t_{PHZ(E)}$
$V_{OH}$
0.5 V
Output
≤1.5 V
$t_{PLZ(E)}$
≈1.5 V
0.5 V
Output
$V_{OL}$
0 V
Control
Input
1.5 V
3.0 V
0
$t_{PZL(E)}$
Output
1.5 V
$V_{OL}$
0 V
$t_{PZH(E)}$
$V_{OH}$
Output
1.5 V
0 V

FIGURE 2 – PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT

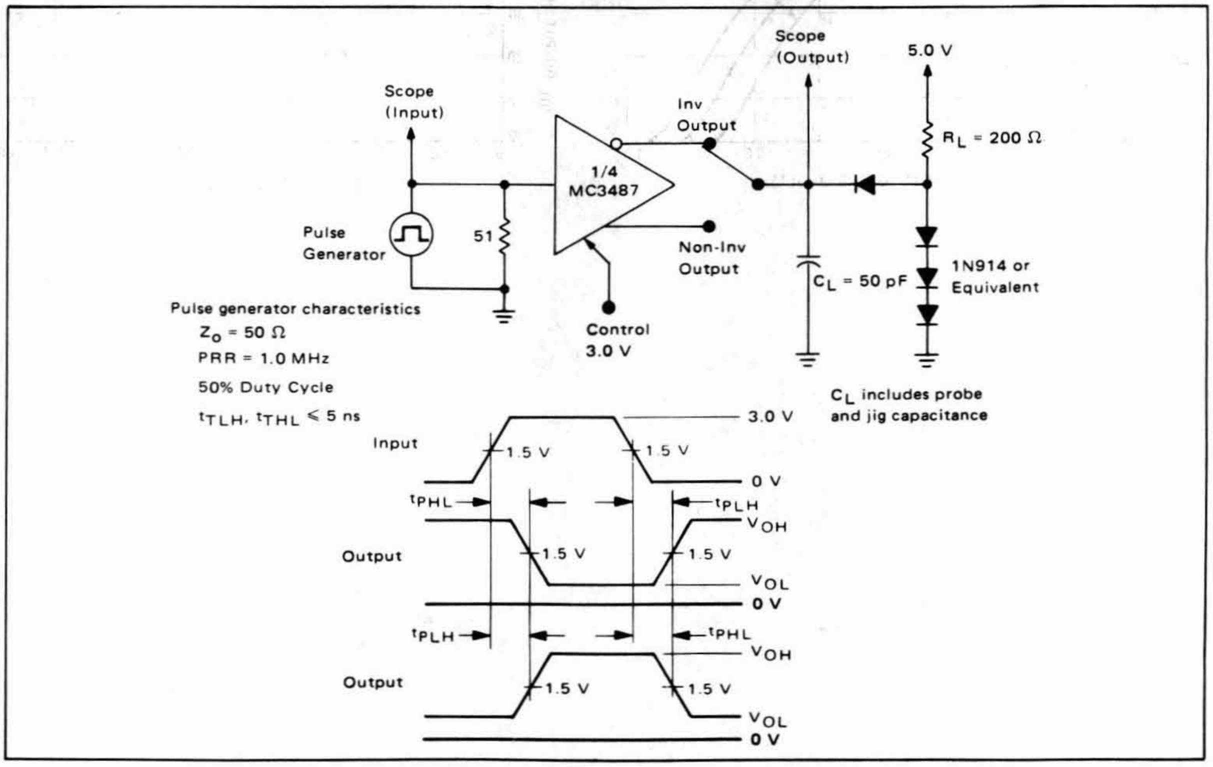

Scope
(Output)
5.0 V
Scope
(Input)
Inv
Output
$R_L = 200\ \Omega$
1/4
MC3487
Pulse
Generator
51
Non-Inv
Output
1N914 or
Equivalent
$C_L = 50$ pF
Pulse generator characteristics
$Z_o = 50\ \Omega$
PRR = 1.0 MHz
50% Duty Cycle
$t_{TLH}, t_{THL} \leq 5$ ns
Control
3.0 V
$C_L$ includes probe
and jig capacitance
Input
1.5 V
1.5 V
3.0 V
0 V
$t_{PHL}$
$t_{PLH}$
$V_{OH}$
Output
1.5 V
1.5 V
$V_{OL}$
0 V
$t_{PLH}$
$t_{PHL}$
$V_{OH}$
Output
1.5 V
1.5 V
$V_{OL}$
0 V

FIGURE 3 – OUTPUT TRANSITION TIMES TEST CIRCUIT AND WAVEFORMS

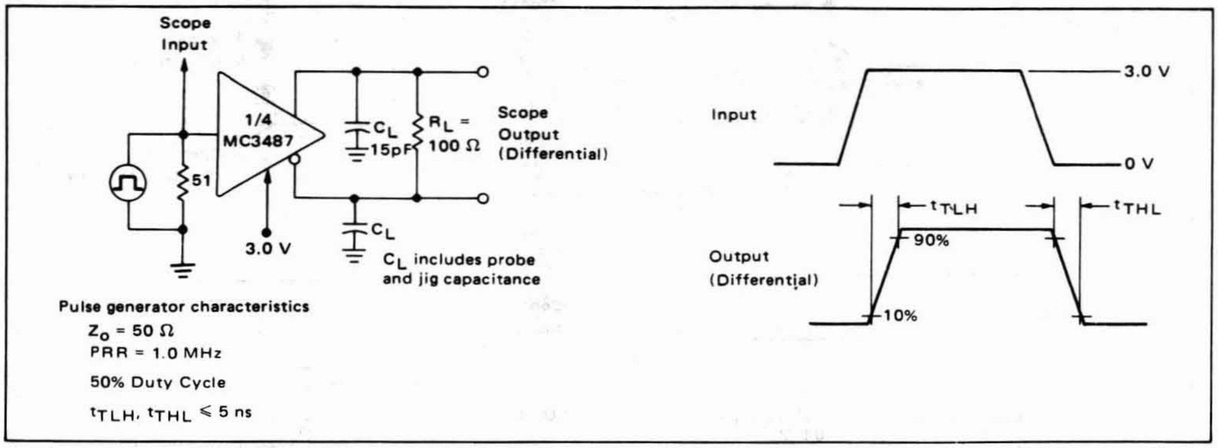

Scope Input
1/4 MC3487
51
3.0 V
$C_L$ 15pF
$R_L$ = 100 Ω
Scope Output (Differential)
$C_L$
$C_L$ includes probe and jig capacitance
Pulse generator characteristics
$Z_o$ = 50 Ω
PRR = 1.0 MHz
50% Duty Cycle
$t_{TLH}$, $t_{THL}$ ≤ 5 ns
Input
3.0 V
0 V
$t_{TLH}$
$t_{THL}$
90%
Output (Differential)
10%

FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE

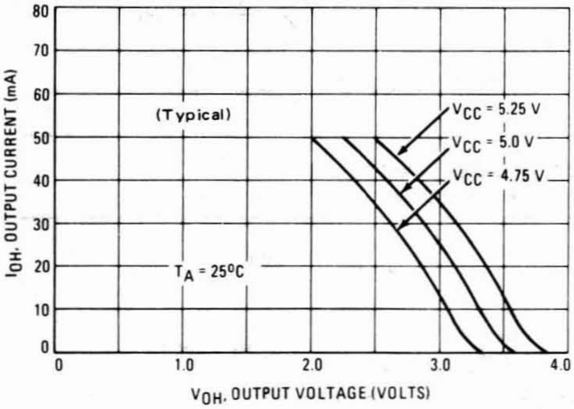
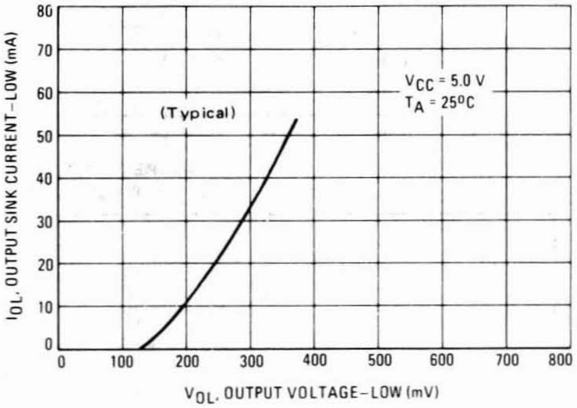


FIGURE 5 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



**MOTOROLA**

# MC3488A

## DUAL RS-423/RS-232C LINE DRIVER

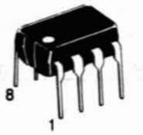
The MC3488A dual single-ended line driver has been designed to satisfy the requirements of EIA standards RS-423 and RS-232C, as well as CCITT X.26, X.28 and Federal Standard FIDS1030. It is suitable for use where signal wave shaping is desired and the output load resistance is greater than 450 ohms. Output slew rates are adjustable from 1.0 μs to 100 μs by a single external resistor. Output level and slew rate are insensitive to power supply variations. Input undershoot diodes limit transients below ground and output current limiting is provided in both output states.

The MC3488A has a standard 1.5 V input logic threshold for TTL or NMOS compatibility.

- PNP Buffered Inputs to Minimize Input Loading
- Short Circuit Protection
- Adjustable Slew Rate Limiting
- MC3488A Equivalent to 9636A
- Output Levels and Slew Rates are Insensitive to Power Supply Voltages
- No External Blocking Diode Required for $V_{EE}$ Supply
- Second Source μA9636A

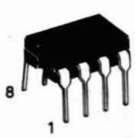
## DUAL RS-423/RS-232C DRIVER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

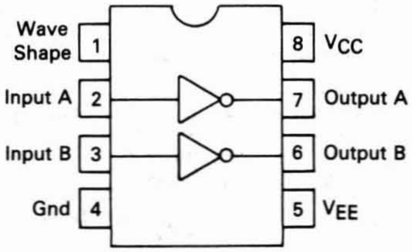


**P1 SUFFIX**
PLASTIC PACKAGE
CASE 626-04

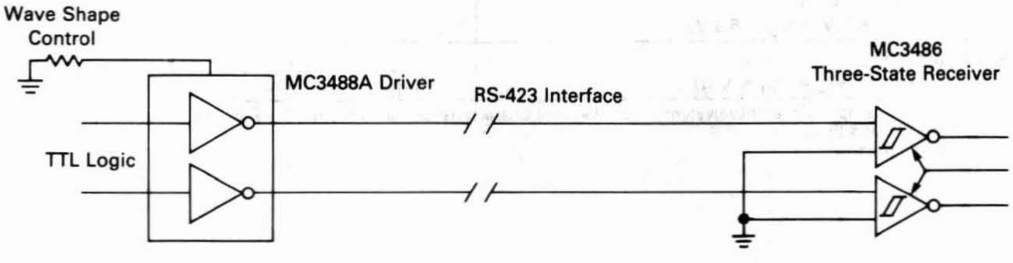
**U SUFFIX**
CERAMIC PACKAGE
CASE 693-02



**PIN CONNECTIONS**


Wave Shape
1
Input A
2
Input B
3
Gnd
4
8
$V_{CC}$
7
Output A
6
Output B
5
$V_{EE}$

**TYPICAL APPLICATION**


Wave Shape Control
MC3488A Driver
TTL Logic
RS-423 Interface
MC3486
Three-State Receiver

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltages | $V_{CC}$<br>$V_{EE}$ | +15<br>−15 | V |
| Output Current<br>Source<br>Sink | <br>$I_{O+}$<br>$I_{O-}$ | <br>+150<br>−150 | mA |
| Operating Ambient Temperature | $T_A$ | 0 to +70 | °C |
| Junction Temperature Range<br>Ceramic Package<br>Plastic Package | $T_J$ | <br>175<br>150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltages | $V_{CC}$<br>$V_{EE}$ | 10.8<br>−13.2 | 12<br>−12 | 13.2<br>−10.8 | V |
| Operating Temperature Range | $T_A$ | 0 | 25 | 70 | °C |
| Wave Shaping Resistor | $R_{WS}$ | 10 | — | 1000 | kΩ |

## TARGET ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply over recommended operating conditions)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage — Low Logic State | $V_{IL}$ | — | — | 0.8 | V |
| Input Voltage — High Logic State | $V_{IH}$ | 2.0 | — | — | V |
| Input Current — Low Logic State<br>($V_{IL}$ = 0.4 V) | $I_{IL}$ | −80 | — | — | μA |
| Input Current — High Logic State<br>($V_{IH}$ = 2.4 V)<br>($V_{IH}$ = 5.5 V) | <br>$I_{IH1}$<br>$I_{IH2}$ | <br>—<br>— | <br>—<br>— | <br>10<br>100 | μA |
| Input Clamp Diode Voltage<br>($I_{IK}$ = −15 mA) | $V_{IK}$ | −1.5 | — | — | V |
| Output Voltage — Low Logic State<br>($R_L$ = ∞) RS-423<br>($R_L$ = 3.0 kΩ) RS-232C<br>($R_L$ = 450 Ω) RS-423 | $V_{OL}$ | <br>−6.0<br>−6.0<br>−6.0 | <br>—<br>—<br>— | <br>−5.0<br>−5.0<br>−4.0 | V |
| Output Voltage — High Logic State<br>($R_L$ = ∞) RS-423<br>($R_L$ = 3.0 kΩ) RS-232C<br>($R_L$ = 450 Ω) RS-423 | $V_{OH}$ | <br>5.0<br>5.0<br>4.0 | <br>—<br>—<br>— | <br>6.0<br>6.0<br>6.0 | V |
| Output Resistance<br>($R_L$ ≥ 450 Ω) | $R_O$ | — | 25 | 50 | Ω |
| Output Short-Circuit Current (Note 2)<br>($V_{in}$ = $V_{out}$ = 0 V)<br>($V_{in}$ = $V_{IH(Min)}$, $V_{out}$ = 0 V) | <br>$I_{OSH}$<br>$I_{OSL}$ | <br>−150<br>+15 | <br>—<br>— | <br>−15<br>+150 | mA |
| Output Leakage Current (Note 3)<br>($V_{CC}$ = $V_{EE}$ = 0 V, −6.0 V ≤ $V_o$ ≤ 6.0 V) | $I_{ox}$ | −100 | — | 100 | μA |
| Power Supply Currents<br>($R_W$ = 100 kΩ, $R_L$ = ∞, $V_{IL}$ ≤ $V_{in}$ ≤ $V_{IH}$) | $I_{CC}$<br>$I_{EE}$ | —<br>−18 | —<br>— | +18<br>— | mA |

Note 1: Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation.
2: One output shorted at a time.
3: No $V_{EE}$ diode required.

**TRANSITION TIMES** (Unless otherwise noted, $C_L$ = 30 pF, f = 1.0 kHz, $V_{CC}$ = $-V_{EE}$ = 12.0 V ± 10%, $T_A$ = 25°C, $R_L$ = 450 Ω. Transition times measured 10% to 90% and 90% to 10%)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Transition Time, Low-to-High State Output | $t_{TLH}$ | | | | μs |
| ($R_W$ = 10 kΩ) | | 0.8 | — | 1.4 | |
| ($R_W$ = 100 kΩ) | | 8.0 | — | 14 | |
| ($R_W$ = 500 kΩ) | | 40 | — | 70 | |
| ($R_W$ = 1000 kΩ) | | 80 | — | 140 | |
| Transition Time, High-to-Low State Output | $t_{THL}$ | | | | μs |
| ($R_W$ = 10 kΩ) | | 0.8 | — | 1.4 | |
| ($R_W$ = 100 kΩ) | | 8.0 | — | 14 | |
| ($R_W$ = 500 kΩ) | | 40 | — | 70 | |
| ($R_W$ = 1000 kΩ) | | 80 | — | 140 | |

FIGURE 1 — TEST CIRCUIT & WAVEFORMS FOR TRANSITION TIMES

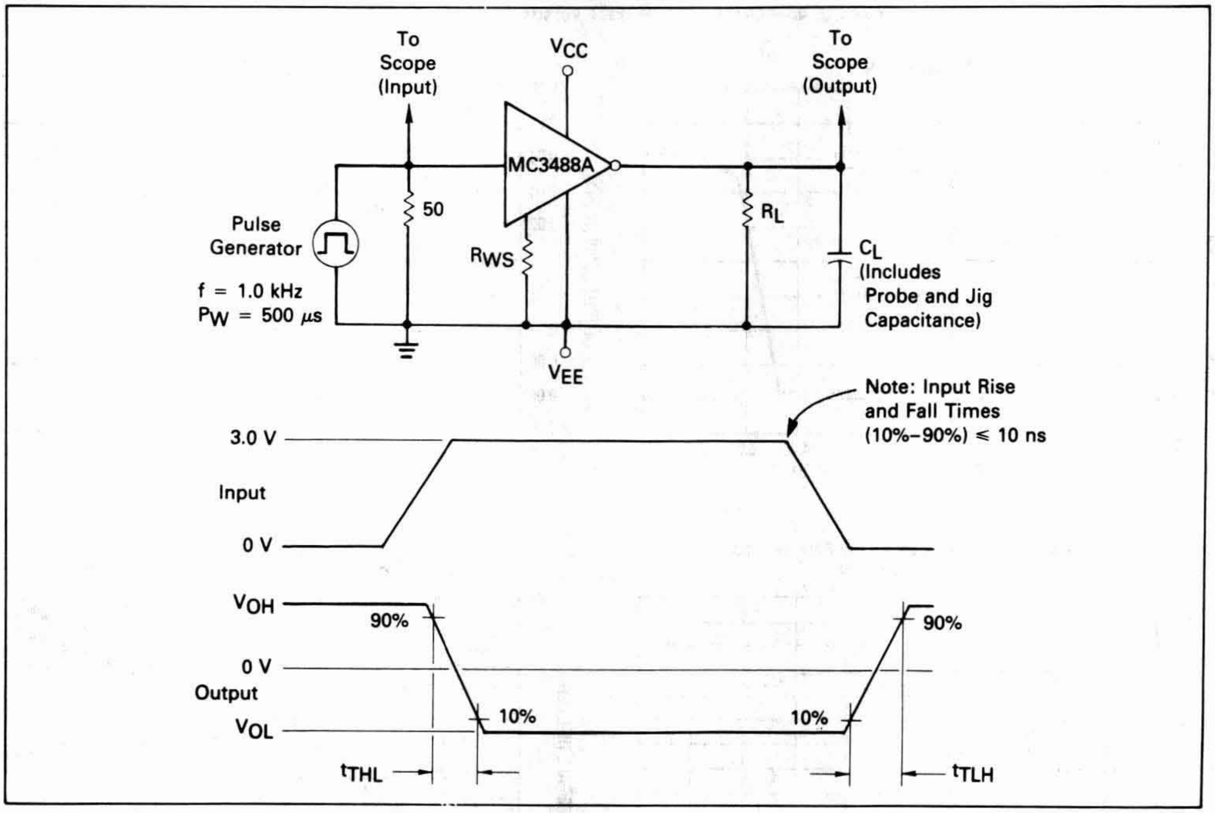

To Scope (Input)
$V_{CC}$
To Scope (Output)
MC3488A
50
$R_L$
Pulse Generator
$R_{WS}$
$C_L$ (Includes Probe and Jig Capacitance)
f = 1.0 kHz
$P_W$ = 500 μs
$V_{EE}$
Note: Input Rise and Fall Times (10%–90%) ≤ 10 ns
3.0 V
Input
0 V
$V_{OH}$
90%
90%
0 V
Output
$V_{OL}$
10%
10%
$t_{THL}$
$t_{TLH}$

**FIGURE 2 — OUTPUT TRANSISTION TIMES versus WAVE SHAPE RESISTOR VALUE**

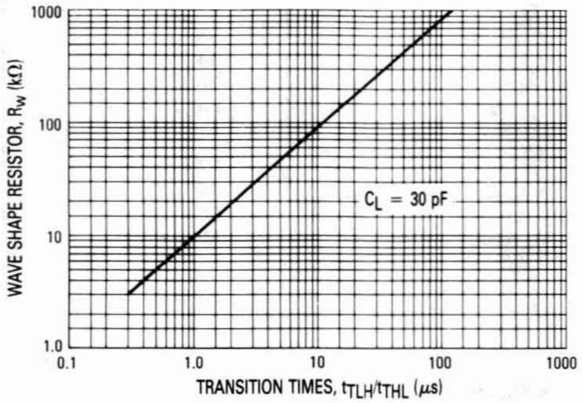


**FIGURE 3 — INPUT/OUTPUT CHARACTERISTICS versus TEMPERATURE**

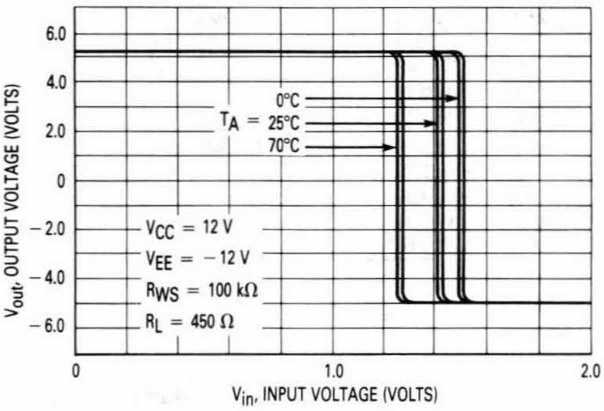


**FIGURE 4 — OUTPUT CURRENT versus OUTPUT VOLTAGE**

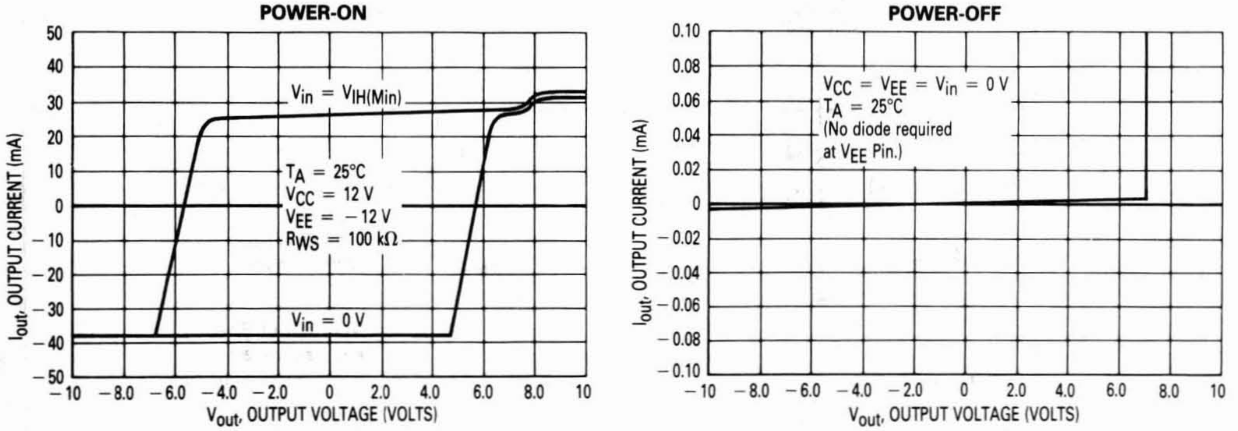


**FIGURE 5 — SUPPLY CURRENT versus TEMPERATURE**

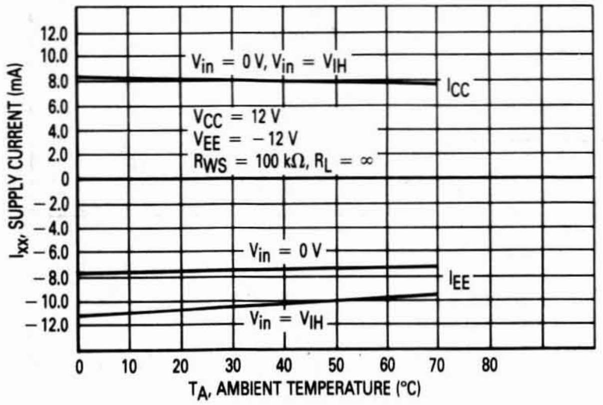
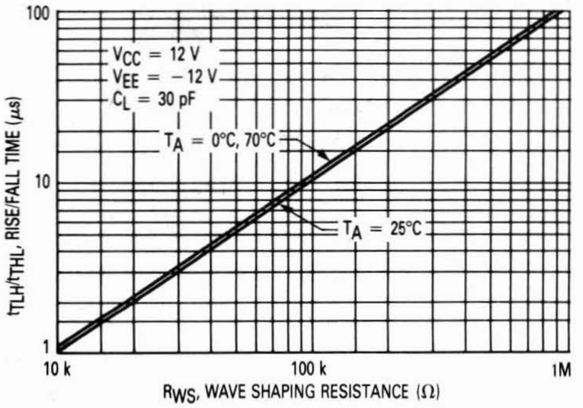


**FIGURE 6 — RISE/FALL TIME versus $R_{WS}$**



**MOTOROLA**

# MC75107
# MC75108

## DUAL LINE RECEIVERS

The MC75107 and MC75108 are MTTL compatible dual line receivers featuring independent channels with common voltage supply and ground terminals. The MC75107 circuit features an active pull-up (totem-pole) output. The MC75108 circuit features an open-collector output configuration that permits the Wired-OR logic connection with similar outputs (such as the MC5401/MC7401 MTTL gate or additional MC75108 receivers). Thus a level of logic is implemented without extra delay.

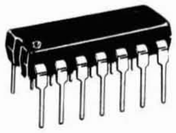
The MC75107 and MC75108 circuits are designed to detect input signals of greater than 25 millivolts amplitude and convert the polarity of the signal into appropriate MTTL compatible output logic levels.

- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Voltage Range of ±3.0 V
- Differential Input Common-Mode Voltage of More Than ± 15 V Using External Attenuator
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- MTTL or MDTL Drive Capability
- High DC Noise Margins
- MC55107 Available as JM38510/10401

## DUAL LINE RECEIVERS

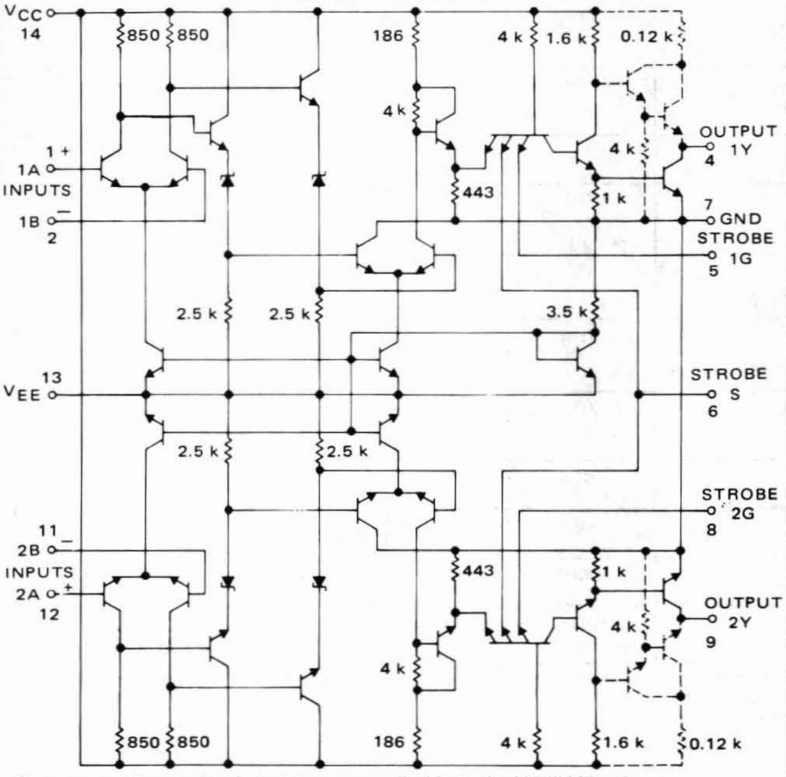
### SILICON MONOLITHIC INTEGRATED CIRCUITS

**L SUFFIX**
CERAMIC PACKAGE
CASE 632-02
MO-001AA

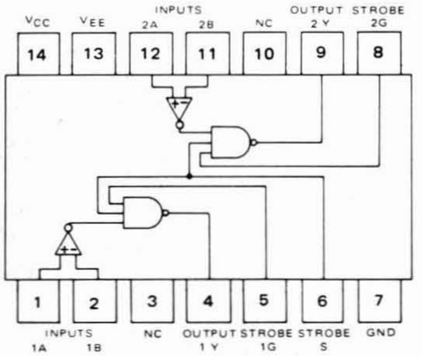


**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

### CIRCUIT SCHEMATIC


$V_{CC}$ 14
850
850
186
4 k
1.6 k
0.12 k
4 k
1 +
1A
INPUTS
1B −
2
4 k
OUTPUT 1Y 4
443
1 k
7 GND
STROBE 1G 5
2.5 k
2.5 k
3.5 k
13
$V_{EE}$
STROBE S 6
2.5 k
2.5 k
STROBE 2G 8
11
2B −
INPUTS
2A +
12
443
1 k
OUTPUT 2Y 9
4 k
4 k
850
850
186
4 k
1.6 k
0.12 k

Components shown with dashed lines are applicable to the MC75107 only.


$V_{CC}$
$V_{EE}$
INPUTS
2A
2B
NC
OUTPUT 2Y
STROBE 2G
14
13
12
11
10
9
8
1
2
3
4
5
6
7
INPUTS
1A
1B
NC
OUTPUT 1Y
STROBE 1G
STROBE S
GND

### TRUTH TABLE

| DIFFERENTIAL INPUTS A-B | STROBES G | STROBES S | OUTPUT Y |
|---|---|---|---|
| $V_{ID} \geq 25$ mV | L or H | L or H | H |
| $-25$ mV $< V_{ID} < 25$ mV | L or H | L | H |
| | L | L or H | H |
| | H | H | INDETERMINATE |
| $V_{ID} \leq -25$ mV | L or H | L | H |
| | L | L or H | H |
| | H | H | L |

**MAXIMUM RATINGS** ($T_A$ = 0°C to +70°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltages | $V_{CC}$<br>$V_{EE}$ | +7.0<br>-7.0 | Vdc |
| Differential-Mode Input Signal Voltage Range | $V_{ID}$ | ±6.0 | Vdc |
| Common-Mode Input Voltage Range | $V_{ICR}$ | ±5.0 | Vdc |
| Strobe Input Voltage | $V_{I(S)}$ | 5.5 | Vdc |
| Power Dissipation (Package Limitation) | $P_D$ | | |
| Plastic and Ceramic Dual-In-Line Packages<br>Derate above $T_A$ = +25°C | | 625<br>3.85 | mW<br>mW/°C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**RECOMMENDED OPERATING CONDITIONS**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltages | $V_{CC}$<br>$V_{EE}$ | +4.75<br>-4.75 | +5.0<br>-5.0 | +5.25<br>-5.25 | Vdc |
| Output Sink Current | $I_{OS}$ | – | – | -16 | mA |
| Differential-Mode Input Voltage Range | $V_{IDR}$ | -5.0 | – | +5.0 | Vdc |
| Common-Mode Input Voltage Range | $V_{ICR}$ | -3.0 | – | +3.0 | Vdc |
| Input Voltage Range, any differential input to ground | $V_{IR}$ | -5.0 | – | +3.0 | Vdc |
| Operating Temperature Range | $T_A$ | 0 | – | +70 | °C |

**DEFINITIONS OF INPUT LOGIC LEVELS**

| Characteristic | Symbol | Test Fig. | Min | Max | Unit |
|---|---|---|---|---|---|
| High-Level Input Voltage (between differential inputs) | $V_{IDH}$ | 1 | 0.025 | 5.0 | Vdc |
| Low-Level Input Voltage (between differential inputs) | $V_{IDL}$ | 1 | -5.0† | -0.025 | Vdc |
| High-Level Input Voltage (at strobe inputs) | $V_{IH(S)}$ | 3 | 2.0 | 5.5 | Vdc |
| Low-Level Input Voltage (at strobe inputs) | $V_{IL(S)}$ | 3 | 0 | 0.8 | Vdc |

†The algebraic convention, where the most positive limit is designated maximum, is used with Low-Level Input Voltage Level ($V_{IDL}$)

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to +70°C unless otherwise noted)

| Characteristic | Symbol | Test Fig. | Min | Typ # | Max | Unit |
|---|---|---|---|---|---|---|
| High-Level Input Current to 1A or 2A Input<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{ID}$ = 0.5 V, $V_{IC}$ = -3.0 V to +3.0 V) ‡ | $I_{IH}$ | 2 | – | 30 | 75 | µA |
| Low-Level Input Current to 1A or 2A Input<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{ID}$ = -2.0 V, $V_{IC}$ = -3.0 V to +3.0 V) ‡ | $I_{IL}$ | 2 | – | – | -10 | µA |
| High-Level Input Current to 1G or 2G Input<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH(S)}$ = 2.4 V)‡<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH(S)}$ = $V_{CC}$ Max)‡ | $I_{IH}$ | 4 | <br>–<br>– | <br>–<br>– | <br>40<br>1.0 | <br>µA<br>mA |
| Low-Level Input Current to 1G or 2G Input<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IL(S)}$ = 0.4 V)‡ | $I_{IL}$ | 4 | – | – | -1.6 | mA |
| High-Level Input Current to S Input<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH(S)}$ = 2.4 V)‡<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IH(S)}$ = $V_{CC}$ Max)‡ | $I_{IH}$ | 4 | <br>–<br>– | <br>–<br>– | <br>80<br>2.0 | <br>µA<br>mA |
| Low-Level Input Current to S Input<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{IL(S)}$ = 0.4 V)‡ | $I_{IL}$ | 4 | – | – | -3.2 | mA |
| High-Level Output Voltage<br>($V_{CC}$ = Min, $V_{EE}$ = Min, $I_{load}$ = -400 µA, $V_{IC}$ = -3.0 V to +3.0 V)‡ | $V_{OH}$ | 3 | – | – | – | V |
| Low-Level Output Voltage<br>($V_{CC}$ = Min, $V_{EE}$ = Min, $I_{sink}$ = 16 mA $V_{IC}$ = -3.0 V to +3.0 V)‡ | $V_{OL}$ | 3 | – | – | 0.4 | V |
| High-Level Leakage Current<br>($V_{CC}$ = Min, $V_{EE}$ = Min, $V_{OH}$ = $V_{CC}$ Max)‡ | $I_{CEX}$ | 3 | – | – | 250 | µA |
| Short-Circuit Output Current # #<br>($V_{CC}$ = Max, $V_{EE}$ = Max)‡ | $I_{OSC}$ | 5 | – | – | – | mA |
| High Logic Level Supply Current from $V_{CC}$<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{ID}$ = 25 mV, $T_A$ = +25°C) ‡ | $I_{CCH^+}$ | 6 | – | 18 | 30 | mA |
| High Logic Level Supply Current from $V_{EE}$<br>($V_{CC}$ = Max, $V_{EE}$ = Max, $V_{ID}$ = 25 mV, $T_A$ = +25°C)‡ | $I_{CCH^-}$ | 6 | 0 | 8.4 | -15 | mA |

‡For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.

#All typical values are at $V_{CC}$ = +5.0 V, $V_{EE}$ = -5.0 V, $T_A$ = +25°C.

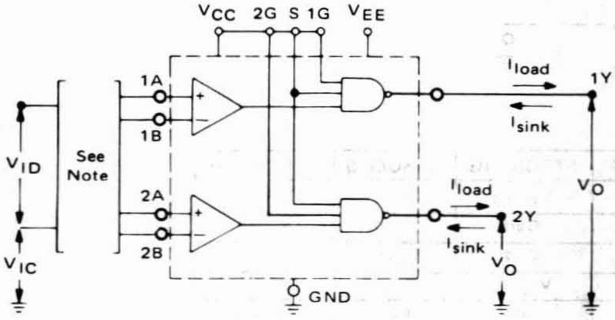
# #Not more than one output should be shorted at a time.

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = +5.0 V, $V_{EE}$ = -5.0 V, $T_A$ = +25°C)

| Characteristic | Symbol | Test Fig. | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation Delay Time, low-to-high level from differential inputs A and B to output<br>($R_L$ = 390 Ω, $C_L$ = 50 pF)<br>($R_L$ = 390 Ω, $C_L$ = 15 pF) | $t_{PLH(D)}$ | 7 | –<br>– | –<br>19 | –<br>25 | ns |
| Propagation Delay Time, high-to-low level from differential inputs A and B to output<br>($R_L$ = 390 Ω, $C_L$ = 50 pF)<br>($R_L$ = 390 Ω, $C_L$ = 15 pF) | $t_{PHL(D)}$ | 7 | –<br>– | –<br>19 | –<br>25 | ns |
| Propagation Delay Time, low-to-high level, from strobe input G or S to output<br>($R_L$ = 390 Ω, $C_L$ = 50 pF)<br>($R_L$ = 390 Ω, $C_L$ = 15 pF) | $t_{PLH(S)}$ | 7 | –<br>– | –<br>13 | –<br>20 | ns |
| Propagation Delay Time, high-to-low level, from strobe input G or S to output<br>($R_L$ = 390 Ω, $C_L$ = 50 pF)<br>($R_L$ = 390 Ω, $C_L$ = 15 pF) | $t_{PHL(S)}$ | 7 | –<br>– | –<br>13 | –<br>20 | ns |

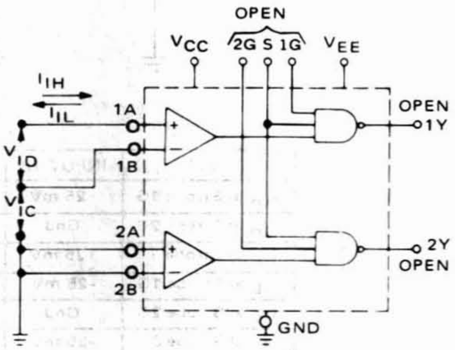
## TEST CIRCUITS

**FIGURE 1 – $V_{IDH}$ and $V_{IDL}$**


VCC
2G
S
1G
VEE
1A
1B
2A
2B
VID
VIC
See Note
Iload
Isink
1Y
2Y
VO
GND

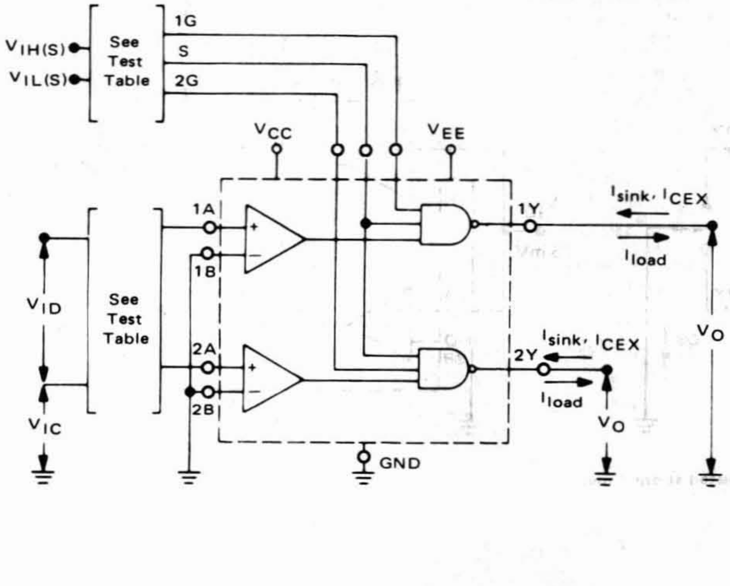
NOTE: When testing one channel, the inputs of the other channel are grounded.

**FIGURE 2 – $I_{IH}$ and $I_{IL}$**


OPEN
VCC
2G S 1G
VEE
IIH
IIL
1A
1B
2A
2B
VID
VIC
OPEN
1Y
2Y
OPEN
GND

NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded.

**FIGURE 3 – $V_{IH(S)}$, $V_{IL(S)}$, $V_{OH}$, $V_{OL}$, and $I_{OH}$**


VIH(S)
VIL(S)
See Test Table
1G
S
2G
VCC
VEE
1A
1B
2A
2B
VID
VIC
See Test Table
1Y
2Y
Isink, ICEX
Iload
VO
GND

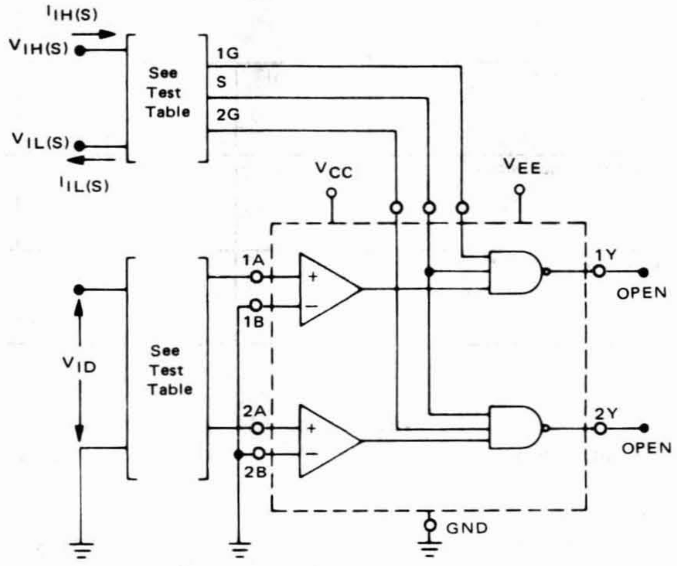
**TEST TABLE**

| MC75107 | MC75108 | $V_{ID}$ | STROBE 1G or 2G | STROBE S |
|---|---|---|---|---|
| TEST | | APPLY | | |
| $V_{OH}$ | $I_{CEX}$ | +25 mV | $V_{IH(S)}$ | $V_{IH(S)}$ |
| $V_{OH}$ | $I_{CEX}$ | -25 mV | $V_{IL(S)}$ | $V_{IH(S)}$ |
| $V_{OH}$ | $I_{CEX}$ | -25 mV | $V_{IH(S)}$ | $V_{IL(S)}$ |
| $V_{OL}$ | $V_{OL}$ | -25 mV | $V_{IH(S)}$ | $V_{IH(S)}$ |

NOTES: 1. $V_{IC}$ = -3.0 V to +3.0 V.
2. When testing one channel, the inputs of the other channel should be grounded.

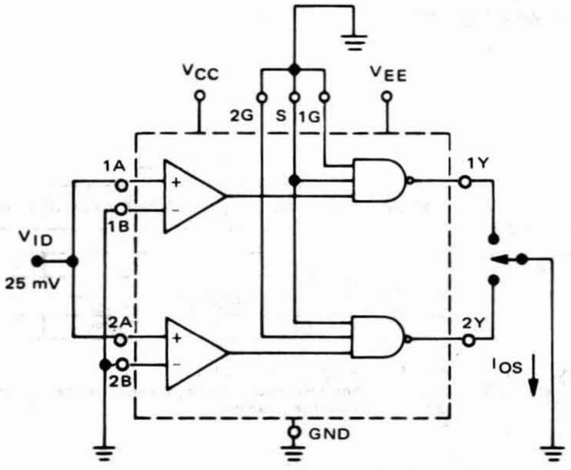
## TEST CIRCUITS (continued)

FIGURE 4 – $I_{IH(G)}$, $I_{IL(G)}$, $I_{IH(S)}$, and $I_{IL(S)}$


$I_{IH(S)}$
$V_{IH(S)}$
See Test Table
1G
S
2G
$V_{IL(S)}$
$I_{IL(S)}$
$V_{CC}$
$V_{EE}$
1A
1B
1Y
OPEN
$V_{ID}$
See Test Table
2A
2B
2Y
OPEN
GND

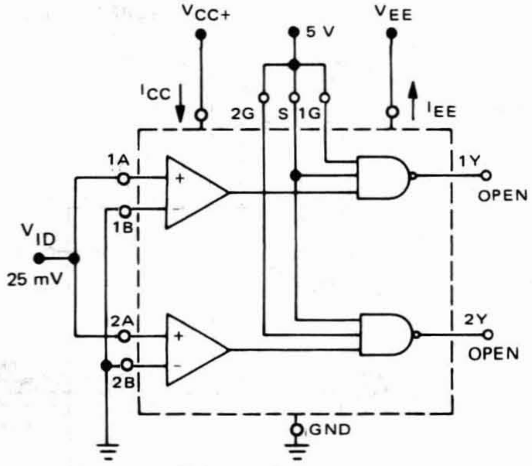
| TEST | INPUT 1A | INPUT 2A | STROBE 1G | STROBE S | STROBE 2G |
|---|---|---|---|---|---|
| $I_{IH}$ at Strobe 1G | +25 mV | Gnd | $V_{IH(S)}$ | Gnd | Gnd |
| $I_{IH}$ at Strobe 2G | Gnd | +25 mV | Gnd | Gnd | $V_{IH(S)}$ |
| $I_{IH}$ at Strobe S | +25 mV | +25 mV | Gnd | $V_{IH(S)}$ | Gnd |
| $I_{IL}$ at Strobe 1G | −25 mV | Gnd | $V_{IL(S)}$ | 4.5 V | Gnd |
| $I_{IL}$ at Strobe 2G | Gnd | −25 mV | Gnd | 4.5 V | $V_{IL(S)}$ |
| $I_{IL}$ at Strobe S | −25 mV | −25 mV | 4.5 V | $V_{IL(S)}$ | 4.5 V |

FIGURE 5 – $I_{OS}$


$V_{CC}$
$V_{EE}$
2G
S
1G
1A
1B
1Y
$V_{ID}$
25 mV
2A
2B
2Y
$I_{OS}$
GND

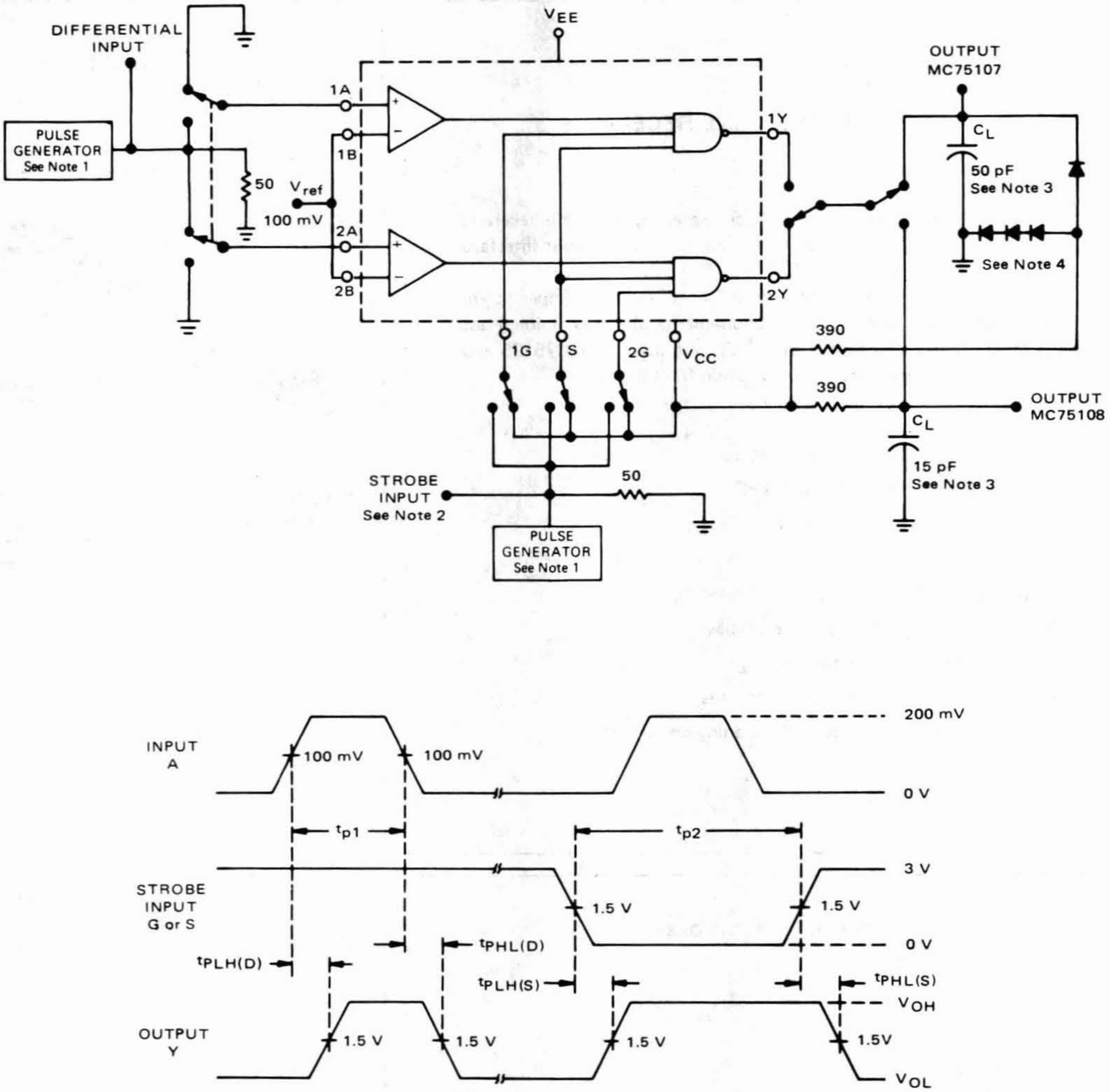
NOTES: 1. Each channel is tested separately.
2. Not more than one output should be tested at one time.

FIGURE 6 – $I_{CC}$ and $I_{EE}$


$V_{CC+}$
5 V
$V_{EE}$
$I_{CC}$
$I_{EE}$
2G
S
1G
1A
1B
1Y
OPEN
$V_{ID}$
25 mV
2A
2B
2Y
OPEN
GND

## TEST CIRCUITS (continued)

FIGURE 7 – PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS


DIFFERENTIAL INPUT
PULSE GENERATOR See Note 1
50
Vref
100 mV
VEE
1A
1B
2A
2B
1Y
2Y
1G
S
2G
VCC
OUTPUT MC75107
CL
50 pF See Note 3
See Note 4
390
390
OUTPUT MC75108
CL
15 pF See Note 3
STROBE INPUT See Note 2
50
PULSE GENERATOR See Note 1
INPUT A
100 mV
100 mV
200 mV
0 V
tp1
tp2
STROBE INPUT G or S
3 V
1.5 V
1.5 V
0 V
tPLH(D)
tPHL(D)
tPLH(S)
tPHL(S)
VOH
OUTPUT Y
1.5 V
1.5 V
1.5 V
1.5V
VOL

NOTES:
1. The pulse generators have the following characteristics: $z_o = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz $t_{p2} = 1\ \mu s$, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe 1G when Inputs 1A-1B are being tested, to Strobe S when Inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
3. $C_L$ includes probe and jig capacitance.
4. All diodes are 1N916 or equivalent.

# MC75125
# MC75127

## SEVEN CHANNEL LINE RECEIVERS

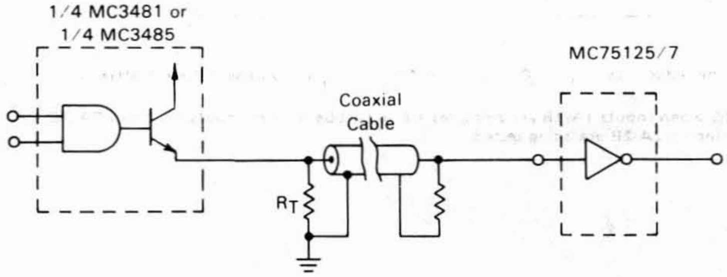
## SEVEN CHANNEL LINE RECEIVERS

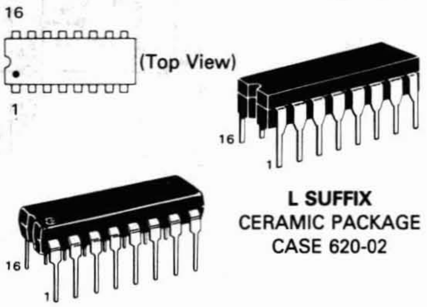
The MC75125 and MC75127 are seven-channel line receivers designed to satisfy the requirements of the input/output interface specification for IBM 360/370.

Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The MC75125 and MC75127 are characterized for operation from 0 to 70°C.

- Meets IBM 360/370 I/O Specification
- Input Resistance – 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors
- Operates from a Single 5 Volt Supply
- High-Speed – Low Propagation Delay
- Ratio Specification – $t_{PLH}/t_{PHL}$
- Seven Channels in One 16-Pin Package
- Standard $V_{CC}$ and Ground Positioning on MC75127

### TYPICAL APPLICATIONS


1/4 MC3481 or
1/4 MC3485
Coaxial Cable
MC75125/7
$R_T$

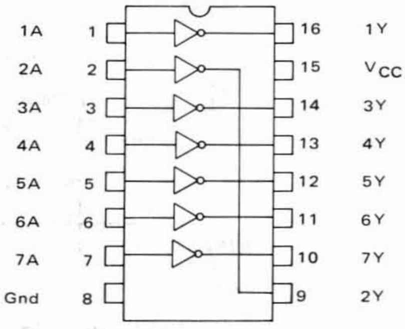

16
1
(Top View)
16
1
16
1

**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

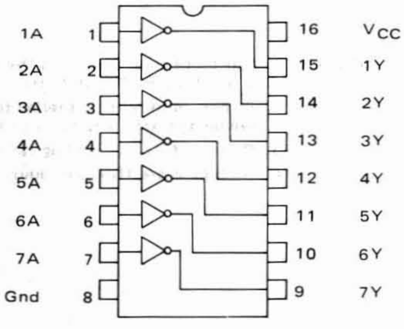
### PIN CONNECTIONS

MC75125


1A 1
2A 2
3A 3
4A 4
5A 5
6A 6
7A 7
Gnd 8
16 1Y
15 VCC
14 3Y
13 4Y
12 5Y
11 6Y
10 7Y
9 2Y

Logic: $Y = \overline{A}$

MC75127


1A 1
2A 2
3A 3
4A 4
5A 5
6A 6
7A 7
Gnd 8
16 VCC
15 1Y
14 2Y
13 3Y
12 4Y
11 5Y
10 6Y
9 7Y

Logic: $Y = \overline{A}$

**MAXIMUM RATINGS** ($T_A = 25^oC$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +7.0 | V |
| Input Voltage | $V_I$ | −2.0 to +7.0 | V |
| Power Dissipation (Package Limitation)<br>Ceramic Package<br>Plastic Package<br>Derate Above $T_A = 25^oC$ | $P_D$<br><br>$1/R_{\theta JA}$ | 1150<br>960<br>7.7 | mW<br><br>$mW/^oC$ |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | $^oC$ |
| Junction Temperature<br>Ceramic Package<br>Plastic Package | $T_J$ | <br>+175<br>+150 | $^oC$ |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | $^oC$ |

**RECOMMENDED OPERATING CONDITIONS**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | Vdc |
| High Level Output Current | $I_{OH}$ | – | – | −0.4 | mA |
| Low Level Output Current | $I_{OL}$ | – | – | 16 | mA |
| Operating Ambient Temperature Range | $T_A$ | 0 | – | +70 | $^oC$ |

**ELECTRICAL CHARACTERISTICS**

(Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at $T_A = 25^oC$ and $V_{CC} = +5.0$ V)

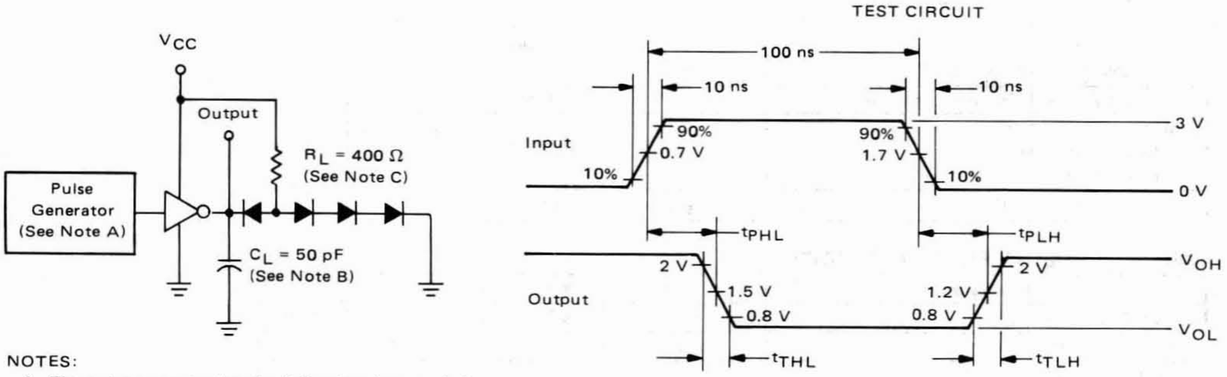
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| High-Level Input Voltage | $V_{IH}$ | 1.7 | – | – | V |
| Low-Level Input Voltage | $V_{IL}$ | – | – | 0.7 | V |
| High-Level Output Voltage ($V_{CC}$ = 4.5 V, $V_{IL}$ = 0.7 V, $I_{OH}$ = −0.4 mA) | $V_{OH}$ | 2.4 | 3.1 | – | V |
| Low-Level Output Voltage ($V_{CC}$ = 4.5 V, $V_{IH}$ = 1.7 V, $I_{OL}$ = 16 mA) | $V_{OL}$ | – | 0.4 | 0.5 | V |
| High-Level Input Current ($V_{CC}$ = 5.5 V, $V_I$ = 3.11 V) | $I_{IH}$ | 0.2 | 0.3 | 0.42 | mA |
| Low-Level Input Current ($V_{CC}$ = 5.5 V, $V_I$ = 0.15 V) | $I_{IL}$ | – | – | −0.24 | mA |
| Short Circuit Output Current* ($V_{CC}$ = 5.5 V, $V_O$ = 0) | $I_{OS}$ | −18 | – | −60 | mA |
| Input Resistance ($V_{CC}$ = 4.5 V, 0 V, or Open, $\Delta V_I$ = 0.15 V to 4.15 V) | $r_i$ | 7.4 | – | 20 | kΩ |
| Power Supply Current<br>Outputs High-Logic State ($V_{CC}$ = 5.5 V, $I_{OH}$ = −0.4 mA, all inputs at 0.7 V) | $I_{CCH}$ | – | 15 | 25 | mA |
| Power Supply Current<br>Outputs Low-Logic State ($V_{CC}$ = 5.5 V, $I_{OL}$ = 16 mA, all inputs at 4.0 V) | $I_{CCL}$ | – | 28 | 47 | mA |

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $T_A = 25^oC$, $R_L$ = 400 Ω, $C_L$ = 50 pF, unless otherwise noted. See Figure 1)

| Characteristic | Symbol | MC75125 | | | MC75127 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Propagation Delay Time<br>Low-to-High-Level Output<br>High-to-Low-Level Output | <br>$t_{PLH}$<br>$t_{PHL}$ | <br>7.0<br>10 | <br>14<br>18 | <br>25<br>30 | <br>7.0<br>10 | <br>14<br>18 | <br>25<br>30 | ns |
| Ratio of Propagation Delay Times | $t_{PLH}/t_{PHL}$ | 0.5 | 0.8 | 1.3 | 0.5 | 0.8 | 1.3 | |
| Transition Time, Low-to-High-Level Output | $t_{TLH}$ | 1.0 | 7.0 | 12 | 1.0 | 7.0 | 12 | ns |
| Transition Time, High-to-Low Level Output | $t_{THL}$ | 1.0 | 3.0 | 12 | 1.0 | 3.0 | 12 | ns |

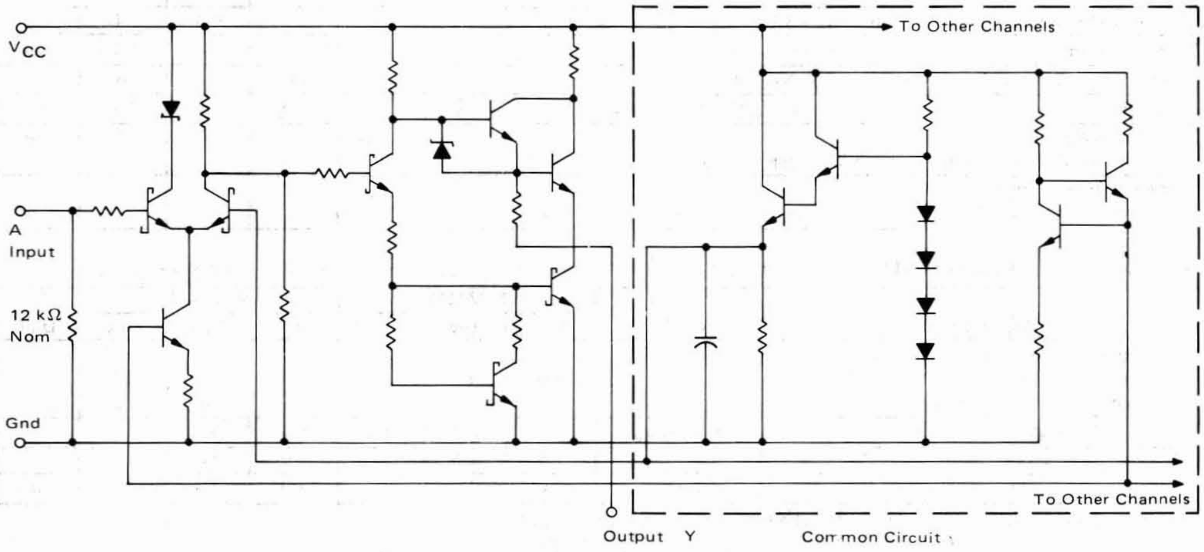
*No more than one output should be shorted at a time.

FIGURE 1 – PARAMETER MEASUREMENT INFORMATION


TEST CIRCUIT
VCC
Output
Pulse Generator (See Note A)
RL = 400 Ω (See Note C)
CL = 50 pF (See Note B)
100 ns
10 ns
10 ns
Input
90%
0.7 V
10%
90%
1.7 V
10%
3 V
0 V
tPHL
tPLH
Output
2 V
1.5 V
0.8 V
1.2 V
0.8 V
2 V
VOH
VOL
tTHL
tTLH
VOLTAGE WAVEFORMS

NOTES:
A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, PRR = 5 MHz.
B. $C_L$ includes probe and jig capacitance.
C. All diodes are MMD7000 or equivalent.

FIGURE 2 – SCHEMATIC (EACH RECEIVER)


VCC
A Input
12 kΩ Nom
Gnd
To Other Channels
To Other Channels
Output Y
Common Circuit

## TYPICAL CHARACTERISTICS

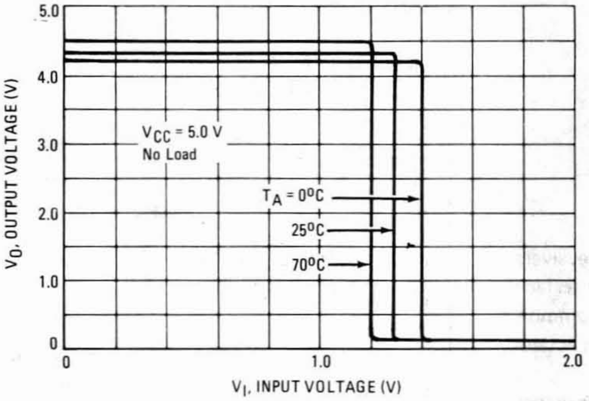


FIGURE 3 – VOLTAGE TRANSFER CHARACTERISTICS versus AMBIENT TEMPERATURE

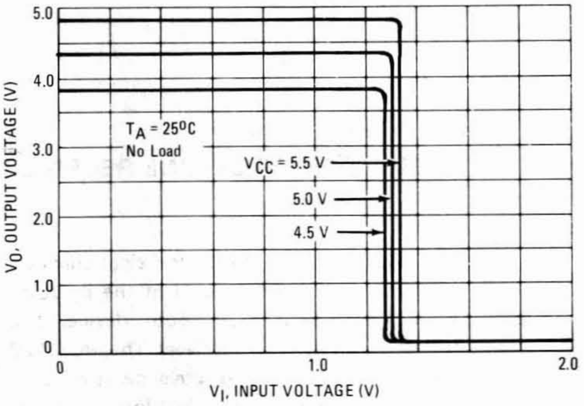


FIGURE 4 – VOLTAGE TRANSFER CHARACTERISTIC versus SUPPLY VOLTAGE

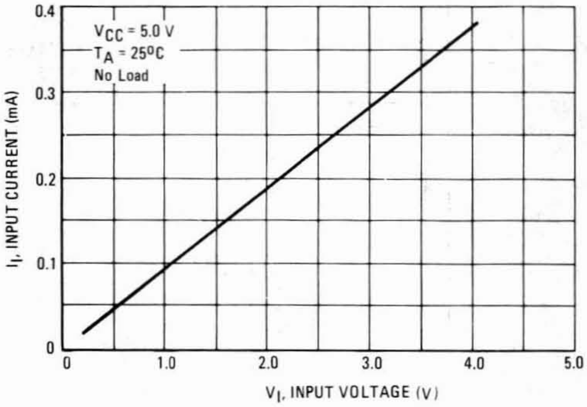


FIGURE 5 – INPUT CURRENT versus INPUT VOLTAGE

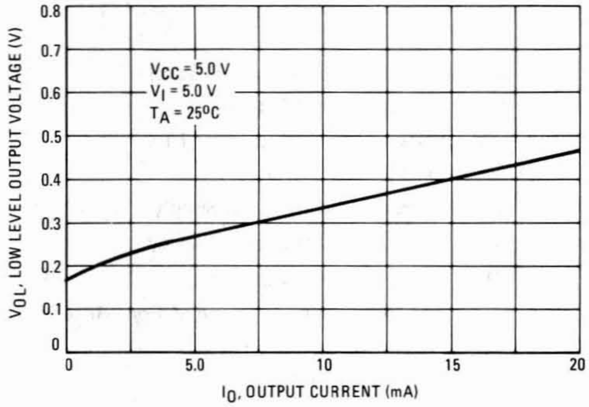


FIGURE 6 – LOW-LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT

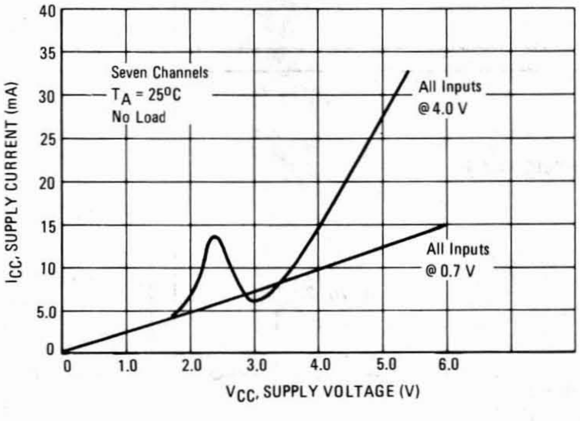


FIGURE 7 – SUPPLY CURRENT versus SUPPLY VOLTAGE

**MOTOROLA**

# MC75128
# MC75129

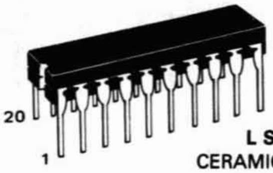
**EIGHT-CHANNEL LINE RECEIVERS**

## EIGHT-CHANNEL LINE RECEIVERS

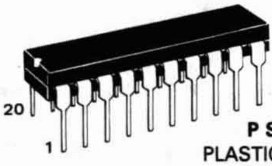
The MC75128 and MC75129 are eight-channel line receivers designed to satisfy the requirements of the input/output interface specification for IBM 360/370. Both devices feature common strobes for each group of four receivers. The MC75128 has an active-high strobe; the MC75129 has an active-low strobe.

Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. Both devices are characterized for operation from 0 to 70°C.

- Meets IBM 360/370 I/O Specification
- Input Resistance – 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors
- Operates from a Single 5 Volt Supply
- High-Speed – Low Propagation Delay
- Ratio Specification – $t_{PLH}/t_{PHL}$
- Common Strobe for Each Group of Four Receivers
- MC75128 Strobe – Active-High
  MC75129 Strobe – Active-Low



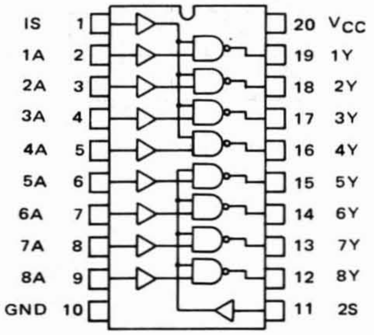
**L SUFFIX**
CERAMIC PACKAGE
CASE 732-03



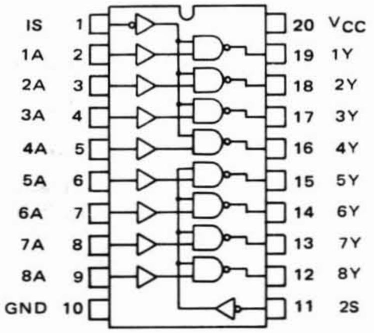
**P SUFFIX**
PLASTIC PACKAGE
CASE 738-02

**PIN CONNECTIONS**

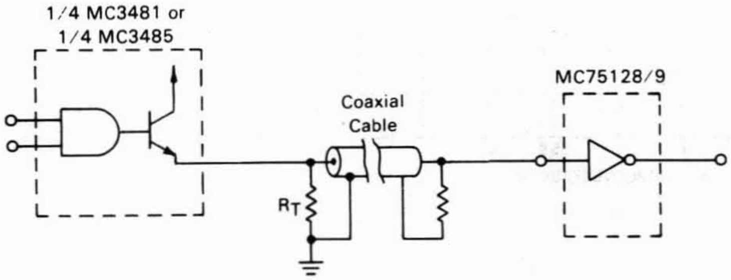
**MC75128**


IS 1
1A 2
2A 3
3A 4
4A 5
5A 6
6A 7
7A 8
8A 9
GND 10
20 VCC
19 1Y
18 2Y
17 3Y
16 4Y
15 5Y
14 6Y
13 7Y
12 8Y
11 2S

**MC75129**


IS 1
1A 2
2A 3
3A 4
4A 5
5A 6
6A 7
7A 8
8A 9
GND 10
20 VCC
19 1Y
18 2Y
17 3Y
16 4Y
15 5Y
14 6Y
13 7Y
12 8Y
11 2S

**TYPICAL APPLICATION**


1/4 MC3481 or
1/4 MC3485
Coaxial
Cable
MC75128/9
RT

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +7.0 | V |
| A Input Voltage | $V_{IA}$ | −0.15 to +7.0 | V |
| Strobe Input Voltage | $V_{IS}$ | +7.0 | V |
| Power Dissipation (Package Limitation) | | | |
| Ceramic Package | $P_D$ | 1150 | mW |
| Plastic Package | | 960 | |
| Derate Above $T_A$ = 25°C | $1/R_{\theta JA}$ | −7.7 | mW/°C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Junction Temperature | $T_J$ | | °C |
| Ceramic Package | | +175 | |
| Plastic Package | | +150 | |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**RECOMMENDED OPERATING CONDITIONS**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | Vdc |
| High Level Output Current | $I_{OH}$ | – | – | −0.4 | mA |
| Low Level Output Current | $I_{OL}$ | – | – | 16 | mA |
| Operating Ambient Temperature Range | $T_A$ | 0 | – | +70 | °C |

**ELECTRICAL CHARACTERISTICS**

(Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at $T_A$ = 25°C and $V_{CC}$ = +5.0 V)

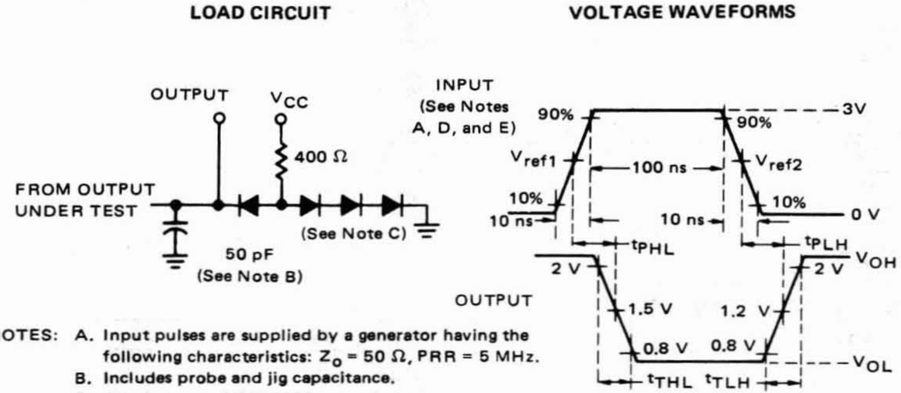
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| High-Level Input Voltage | $V_{IH}$ | | | | V |
| A Inputs | | 1.7 | – | – | |
| S Inputs | | 2.0 | – | – | |
| Low-Level Input Voltage | $V_{IL}$ | | | | V |
| A Inputs | | – | – | 0.7 | |
| S Inputs | | – | – | 0.7 | |
| High-Level Output Voltage ($V_{CC}$ = 4.5 V, $V_{IL}$ = 0.7 V, $I_{OH}$ = −0.4 mA) | $V_{OH}$ | 2.4 | 3.1 | – | V |
| Low-Level Output Voltage ($V_{CC}$ = 4.5 V, $V_{IH}$ = 1.7 V, $I_{OL}$ = 16 mA) | $V_{OL}$ | – | 0.4 | 0.5 | V |
| Input Clamp Voltage ($V_{CC}$ = 4.5 V, $I_I$ = −18 mA, S Inputs) | $V_{IK}$ | – | – | −1.5 | V |
| High-Level Input Current ($V_{CC}$ = 5.5 V, $V_I$ = 3.11 V, A Inputs) | $I_{IH}$ | – | 0.3 | 0.42 | mA |
| ($V_{CC}$ = 5.5 V, $V_I$ = 2.7 V, S Inputs) | | – | – | 20 | µA |
| Low-Level Input Current ($V_{CC}$ = 5.5 V, $V_I$ = 0.15 V, A Inputs) | $I_{IL}$ | – | – | −0.24 | mA |
| ($V_{CC}$ = 5.5 V, $V_I$ = 0.4 V, S Inputs) | | – | – | −0.4 | |
| Short Circuit Output Current * ($V_{CC}$ = 5.5 V, $V_O$ = 0) | $I_{OS}$ | −18 | – | −60 | mA |
| Input Resistance ($V_{CC}$ = 4.5 V, 0 V, or Open, $\Delta V_I$ = 0.15 V to 4.15 V) | $r_i$ | 7.0 | – | 20 | kΩ |
| Power Supply Current – Outputs High-Logic State, all inputs at 0.7 V | $I_{CCH}$ | | | | mA |
| ($V_{CC}$ = 5.5 V, Strobe at 2.4 V – MC75128) | | – | 19 | 31 | |
| ($V_{CC}$ = 5.5 V, Strobe at 0.4 V – MC75129) | | – | 19 | 31 | |
| Power Supply Current – Outputs Low-Logic State, all inputs at 4.0 V | $I_{CCL}$ | | | | mA |
| ($V_{CC}$ = 5.5 V, Strobe at 2.4 V – MC75128) | | – | 32 | 53 | |
| ($V_{CC}$ = 5.5 V, Strobe at 0.4 V – MC75129) | | – | 32 | 53 | |

**SWITCHING CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $T_A$ = 25°C, $R_L$ = 400 Ω, $C_L$ = 50 pF, unless otherwise noted, See Figures 1 and 2)

| Characteristic | Symbol | MC75128 | | | MC75129 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Propagation Delay Time – From A Inputs | | | | | | | | ns |
| Low-to-High-Level Output | $t_{PLH}(A)$ | 7.0 | 14 | 25 | 7.0 | 14 | 25 | |
| High-to-Low-Level Output | $t_{PHL}(A)$ | 10 | 18 | 30 | 10 | 18 | 30 | |
| Propagation Delay Time – From S Inputs | | | | | | | | ns |
| Low-to-High-Level Output | $t_{PLH}(S)$ | – | 26 | 40 | – | 20 | 35 | |
| High-to-Low-Level Output | $t_{PHL}(S)$ | – | 22 | 35 | – | 16 | 30 | |
| Ratio of Propagation Delay Times – A Inputs | $t_{PLH}(A)/t_{PHL}(A)$ | 0.5 | 0.8 | 1.3 | 0.5 | 0.8 | 1.3 | |
| Transition Time, Low-to-High-Level Output | $t_{TLH}$ | 1.0 | 7.0 | 12 | 1.0 | 7.0 | 12 | ns |
| Transition Time, High-to-Low-Level Output | $t_{THL}$ | 1.0 | 3.0 | 12 | 1.0 | 3.0 | 12 | ns |

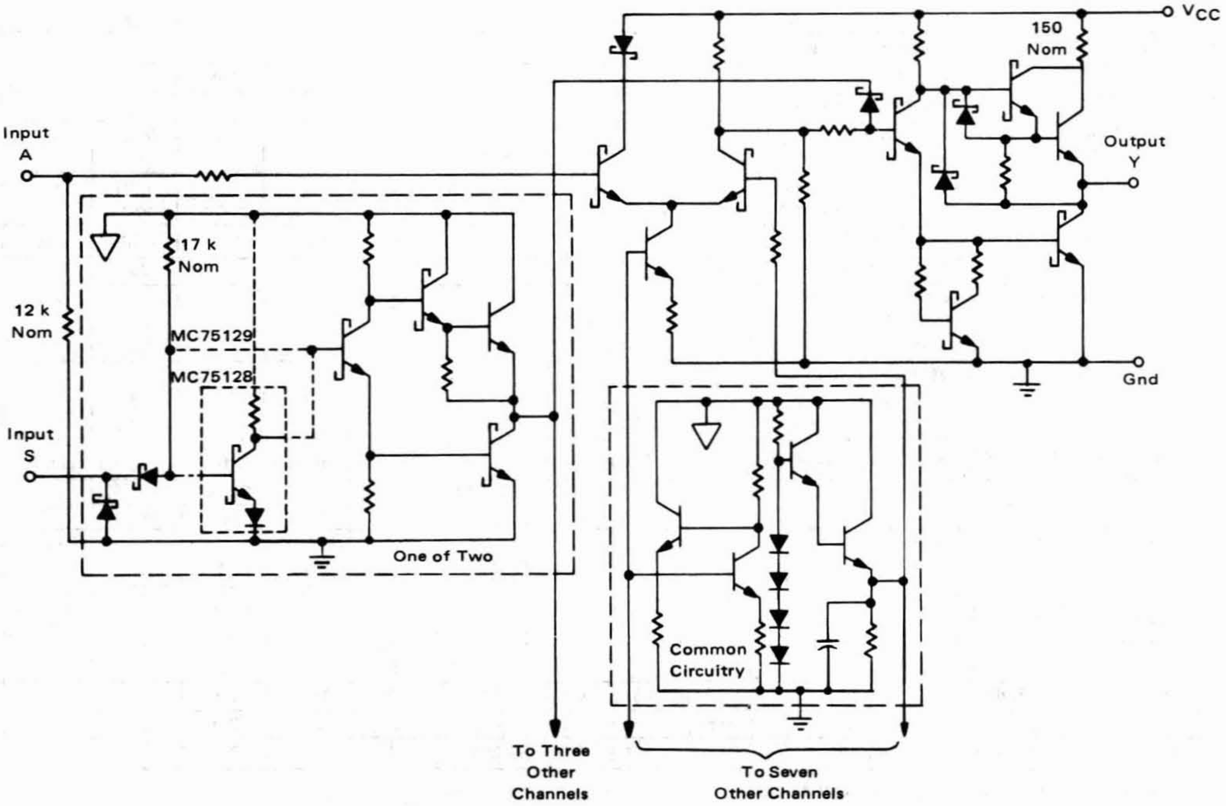
*No more than one output should be shorted at a time.

FIGURE 1 – PARAMETER MEASUREMENT INFORMATION


LOAD CIRCUIT
VOLTAGE WAVEFORMS
OUTPUT
$V_{CC}$
400 Ω
FROM OUTPUT
UNDER TEST
(See Note C)
50 pF
(See Note B)
INPUT
(See Notes
A, D, and E)
90%
90%
3V
$V_{ref1}$
100 ns
$V_{ref2}$
10%
10%
0 V
10 ns
10 ns
$t_{PHL}$
$t_{PLH}$
$V_{OH}$
2 V
2 V
OUTPUT
1.5 V
1.2 V
0.8 V
0.8 V
$V_{OL}$
$t_{THL}$
$t_{TLH}$

NOTES:
- A. Input pulses are supplied by a generator having the following characteristics: $Z_o = 50\ \Omega$, PRR = 5 MHz.
- B. Includes probe and jig capacitance.
- C. All diodes are MMD7000 or equivalent.
- D. The strobe inputs of MC75129 are in-phase with the output.
- E. $V_{ref1} = 0.7$ V and $V_{ref2} = 1.7$ V for testing data (A) inputs, $V_{ref1} = V_{ref2} = 1.3$ V for strobe inputs.

FIGURE 2 – SCHEMATIC (EACH RECEIVER)


$V_{CC}$
150
Nom
Input
A
Output
Y
17 k
Nom
12 k
Nom
MC75129
MC75128
Input
S
One of Two
Gnd
Common
Circuitry
To Three
Other
Channels
To Seven
Other Channels

## TYPICAL CHARACTERISTICS

FIGURE 3 — VOLTAGE TRANSFER CHARACTERISTICS versus AMBIENT TEMPERATURE

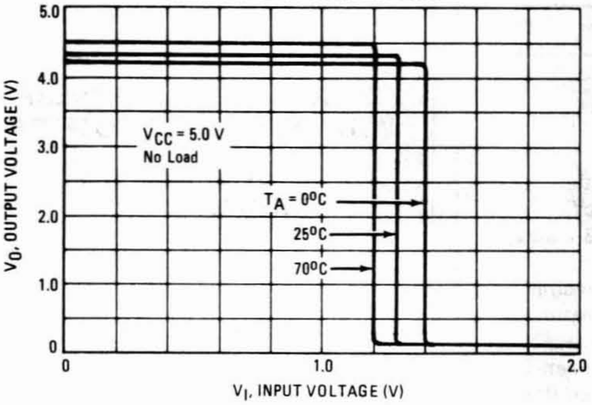


FIGURE 4 — VOLTAGE TRANSFER CHARACTERISTIC versus SUPPLY VOLTAGE

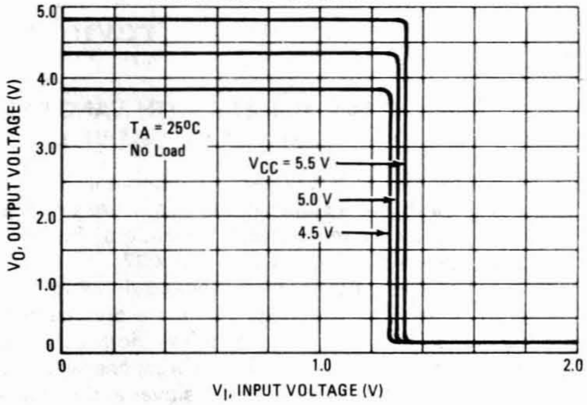


FIGURE 5 — INPUT CURRENT versus INPUT VOLTAGE

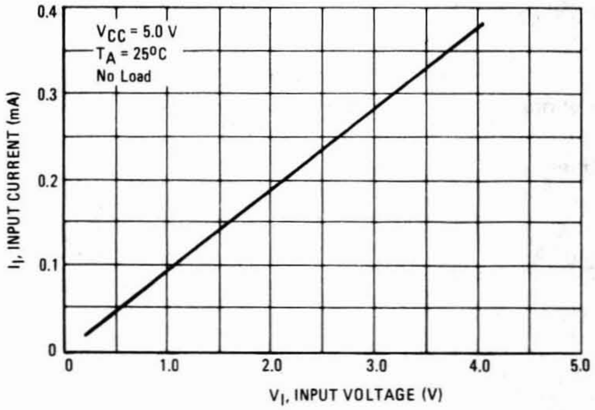
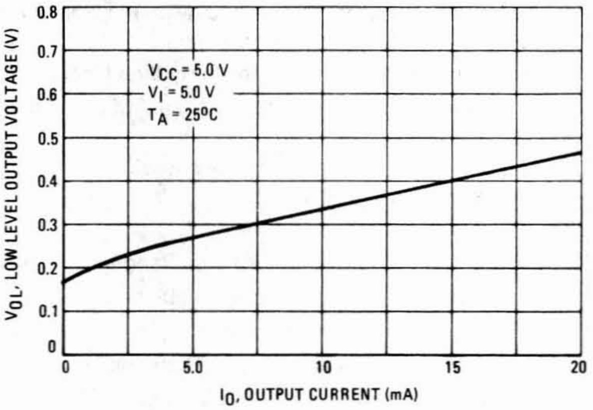


FIGURE 6 — LOW-LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT



**MOTOROLA**

# SN75172
# SN75174

## Product Preview

### QUAD LINE DRIVERS WITH NAND ENABLED THREE-STATE OUTPUTS

The Motorola SN75172/174 are monolithic quad differential line drivers with three-state outputs. They are designed specifically to meet the requirements of EIA standards RS-485, RS-422A, and CCITT recommendations V.11 and X.27.

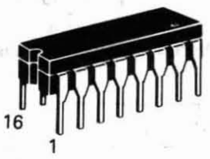
The device is optimized for balanced multipoint bus transmission at rates up to 4 megabits per second. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75172/174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. These devices offer optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

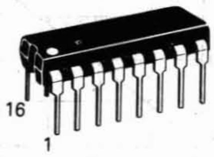
- Meets RS-485 Standard for Party-Line Operation
- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range . . . −7.0 V to 12 V
- Active-High and Active-Low Enables
- Thermal Shutdown Protection
- Positive and Negative Current Limiting
- Operates from Single 5.0 Volt Supply
- Low Power Requirements
- Functionally Interchangeable With
  AM26LS31 (SN75172)
  MC3487 (SN75174)

### QUAD RS-485 LINE DRIVERS WITH THREE-STATE OUTPUTS

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

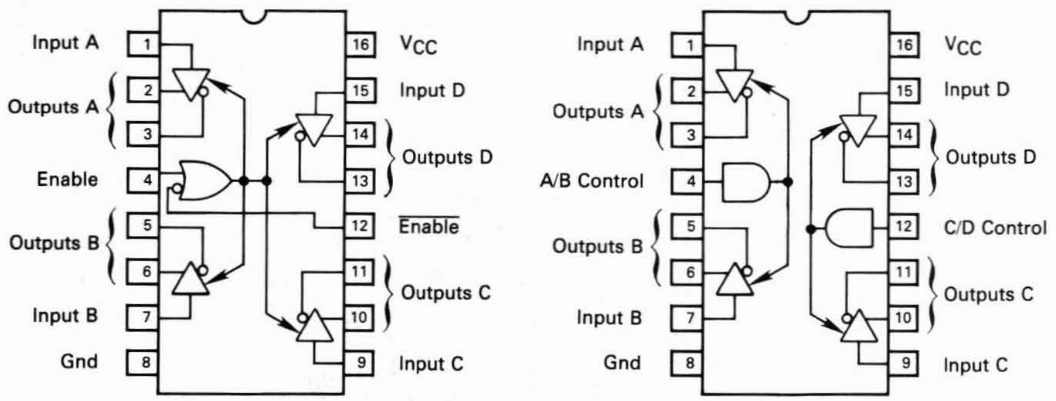


**J SUFFIX**
CERAMIC PACKAGE
CASE 620-02



**N SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### PIN CONNECTIONS


SN75172
Input A
Outputs A
Enable
Outputs B
Input B
Gnd
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VCC
Input D
Outputs D
Enable
Outputs C
Input C
SN75174
Input A
Outputs A
A/B Control
Outputs B
Input B
Gnd
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VCC
Input D
Outputs D
C/D Control
Outputs C
Input C

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

SN75172

| TRUTH TABLE | | | |
|---|---|---|---|
| Input | Control Inputs (E/$\overline{E}$) | Noninverting Output | Inverting Output |
| H | H/L | H | L |
| L | H/L | L | H |
| X | L/H | Z | Z |

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

SN75174

| TRUTH TABLE | | | |
|---|---|---|---|
| Input | Control Input | Noninverting Output | Inverting Output |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

**MOTOROLA**

# SN75173
# SN75175

## Advance Information

## QUAD RS-485 LINE RECEIVERS

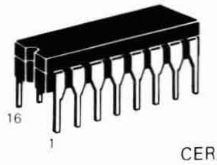
The Motorola SN75173/175 are monolithic quad differential line receivers with three-state outputs. They are designed specifically to meet the requirements of EIA standards RS-485, RS-422A/23A and CCITT recommendations.

The devices are optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. They also feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common-mode input voltage range of −12 volts to 12 volts. The SN75173/175 are designed for optimum performance when used with the SN75172 or SN75174 quad differential line drivers.

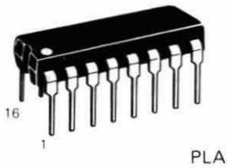
- Meets EIA Standard RS-485
- Meets EIA Standards RS-422A and RS-423A
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . −12 V to 12 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 1 RS-485 Unit Load
- Operates from Single 5.0 V Supply
- Low Power Requirements
- Plug-In Replacement for MC3486 (SN75175)
  AM26LS32 (SN75173)

## QUAD RS-485 LINE RECEIVERS WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC
INTEGRATED CIRCUITS



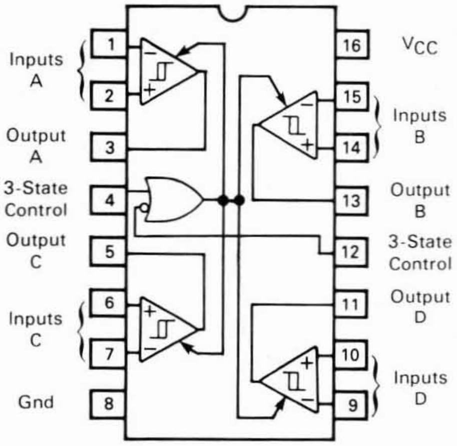
**J SUFFIX**
CERAMIC PACKAGE
CASE 620-02



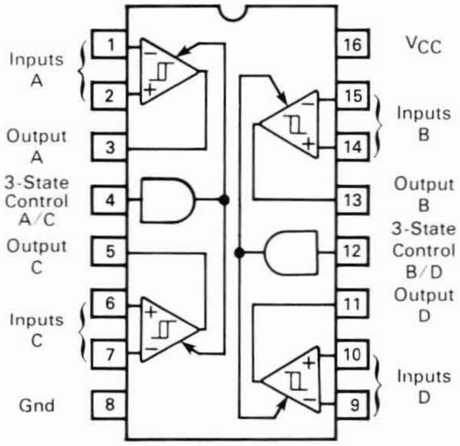
**N SUFFIX**
PLASTIC PACKAGE
CASE 648-05

### PIN CONNECTIONS

**SN75173**


Inputs A
1
2
Output A
3
3-State Control
4
Output C
5
Inputs C
6
7
Gnd
8
16
VCC
15
Inputs B
14
13
Output B
12
3-State Control
11
Output D
10
Inputs D
9
+
−

**SN75175**


Inputs A
1
2
Output A
3
3-State Control A/C
4
Output C
5
Inputs C
6
7
Gnd
8
16
VCC
15
Inputs B
14
13
Output B
12
3-State Control B/D
11
Output D
10
Inputs D
9
+
−

**ORDERING INFORMATION**

| Device | Temperature | Package |
|---|---|---|
| SN75173J | 0 to +70°C | Ceramic DIP |
| SN75173N | 0 to +70°C | Plastic DIP |

**ORDERING INFORMATION**

| Device | Temperature | Package |
|---|---|---|
| SN75175J | 0 to +70°C | Ceramic DIP |
| SN75175N | 0 to +70°C | Plastic DIP |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS (See Note)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 7.0 | Vdc |
| Input Common Mode Voltage | $V_{ICM}$ | ±25 | Vdc |
| Input Differential Voltage | $V_{ID}$ | ±25 | Vdc |
| Three-State Control Input Voltage | $V_I$ | 7.0 | Vdc |
| Output Sink Current | $I_O$ | 50 | mA |
| Storage Temperature | $T_{stg}$ | -65 to +150 | °C |
| Operating Junction Temperature — Ceramic Package<br>— Plastic Package | $T_J$ | +175<br>+150 | °C |

NOTE: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Electrical Characteristics" table provides conditions for actual device operation.

## RECOMMENDED OPERATING CONDITIONS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.75 to 5.25 | Vdc |
| Operating Ambient Temperature | $T_A$ | 0 to +70 | °C |
| Input Common Mode Voltage Range | $V_{ICM}$ | -12 to +12 | Vdc |
| Input Differential Voltage Range | $V_{IDR}$ | -12 to +12 | Vdc |

## ELECTRICAL CHARACTERISTICS (Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25°C$, $V_{CC} = 5.0$ V and $V_{ICM} = 0$ V) (Note 1)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Differential Input Threshold Voltage (Note 4)<br>($-12\text{ V} \leqslant V_{ICM} \leqslant 12\text{ V}, V_{IH} = 2.0\text{ V}$)<br>($I_O = -0.4\text{ mA}, V_{OH} \geqslant 2.7\text{ V}$)<br>($I_O = 16\text{ mA}, V_{OL} \leqslant 0.5\text{ V}$) | $V_{TH(D)}$ | <br><br>—<br>— | <br><br>—<br>— | <br><br>0.2<br>-0.2 | V |
| Input Hysteresis | $V_{T+} - V_{T-}$ | — | 50 | — | mV |
| Input Line Current (Differential Inputs)<br>(Unmeasured Input at 0 V — Note 3)<br>($V_I = +12$ V)<br>($V_I = -7.0$ V) | $I_I$ | <br><br>—<br>— | <br><br>—<br>— | <br><br>1.0<br>-0.8 | mA |
| Input Resistance (Note 5) | $r_i$ | 1 Unit Load | — | — | |
| Input Balance and Output Level (Note 3)<br>($-12\text{ V} \leqslant V_{ICM} \leqslant 12\text{ V}, V_{IH} = 2.0\text{ V}$)<br>($I_O = -0.4\text{ mA}, V_{ID} = 0.2\text{ V}$)<br>($I_O = 8.0\text{ mA}, V_{ID} = -0.2\text{ V}$)<br>($I_O = 16\text{ mA}, V_{ID} = -0.2\text{ V}$) | <br><br>$V_{OH}$<br>$V_{OL}$<br>$V_{OL}$ | <br><br>2.7<br>—<br>— | <br><br>—<br>—<br>— | <br><br>—<br>0.45<br>0.5 | V |
| Input Voltage — High Logic State (Three-State Control) | $V_{IH}$ | 2.0 | — | — | V |
| Input Voltage — Low Logic State (Three-State Control) | $V_{IL}$ | — | — | 0.8 | V |
| Input Current — High Logic State (Three-State Control)<br>($V_{IH} = 2.7$ V)<br>($V_{IH} = 5.5$ V) | $I_{IH}$ | <br>—<br>— | <br>—<br>— | <br>20<br>100 | µA |
| Input Current — Low Logic State (Three-State Control)<br>($V_{IL} = 0.4$ V) | $I_{IL}$ | — | — | -100 | µA |
| Input Clamp Diode Voltage (Three-State Control)<br>($I_{IK} = -18$ mA) | $V_{IK}$ | — | — | -1.5 | V |
| Output Third State Leakage Current<br>($V_{I(D)} = 3.0\text{ V}, V_{IL} = 0.8\text{ V}, V_O = 0.4\text{ V}$)<br>($V_{I(D)} = -3.0\text{ V}, V_{IL} = 0.8\text{ V}, V_O = 2.4\text{ V}$) | $I_{OZ}$ | <br>—<br>— | <br>—<br>— | <br>-20<br>20 | µA |
| Output Short-Circuit Current (Note 2)<br>($V_{I(D)} = 3.0\text{ V}, V_{IH} = 2.0\text{ V}, V_O = 0\text{ V}$) | $I_{OS}$ | -15 | — | -85 | mA |
| Power Supply Current<br>($V_{IL} = 0$ V) (All Inputs Grounded) | $I_{CC}$ | — | — | 70 | mA |

NOTES:

1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Only one output at a time should be shorted.
3. Refer to EIA RS-485 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
5. Input resistance should be derived from input line current specifications and is shown for reference only. See RS-485 and input line current specifications for more specific input resistance information.

**SWITCHING CHARACTERISTICS** (Unless otherwise noted, $V_{CC} = 5.0$ V and $T_A = 25°C$)

| Characteristic | Symbol | SN75173 | | | SN75175 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Propagation Delay Time — Differential Inputs to Output | | | | | | | | ns |
| (Output High to Low) | $t_{PHL(D)}$ | — | 25 | 35 | — | 25 | 35 | |
| (Output Low to High) | $t_{PLH(D)}$ | — | 25 | 35 | — | 25 | 35 | |
| Propagation Delay Time — Three-State Control to Output | | | | | | | | ns |
| (Output Low to Third State) | $t_{PLZ}$ | — | 20 | 40 | — | 16 | 35 | |
| (Output High to Third State) | $t_{PHZ}$ | — | 20 | 30 | — | 19 | 35 | |
| (Output Third State to High) | $t_{PZH}$ | — | 16 | 22 | — | 11 | 30 | |
| (Output Third State to Low) | $t_{PZL}$ | — | 16 | 25 | — | 11 | 30 | |

**SN75173**

**FUNCTION TABLE (EACH RECEIVER)**

| Differential Inputs | 3-State Control | | Output Y |
|---|---|---|---|
| | 4 | 12 | |
| $V_{ID} \geq 0.2$ V | H | X | H |
| | X | L | H |
| $-0.2$ V $< V_{ID} < 0.2$ V | H | X | ? |
| | X | L | ? |
| $V_{ID} \leq -0.2$ V | H | X | L |
| | X | L | L |
| X | L | H | Z |

**SN75175**

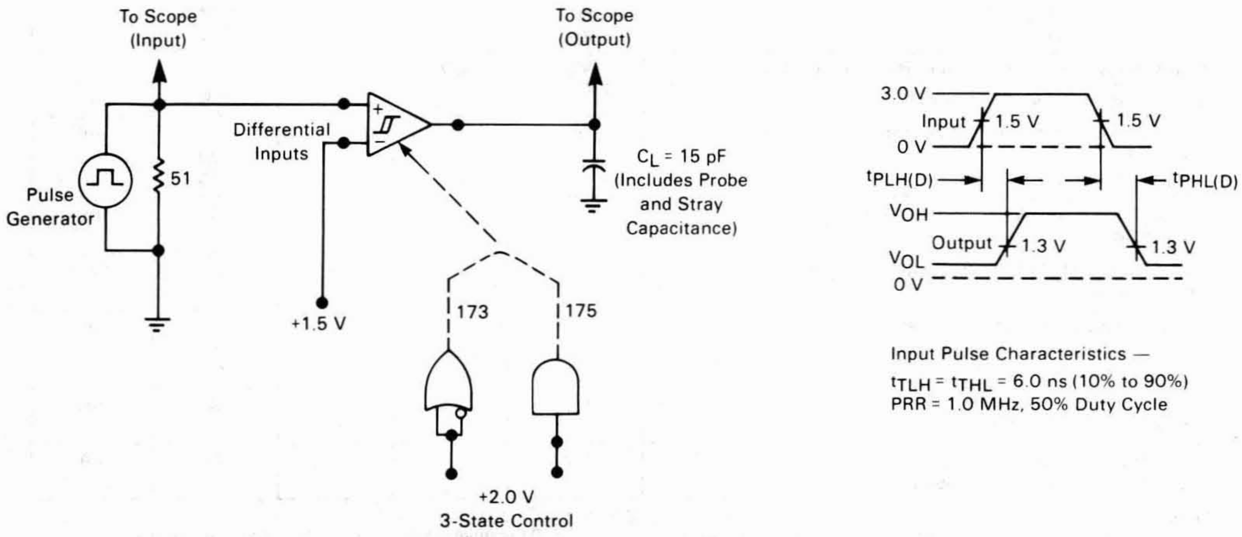
**FUNCTION TABLE (EACH RECEIVER)**

| Differential Inputs | 3-State Control | Output Y |
|---|---|---|
| $V_{ID} \geq 0.2$ V | H | H |
| $-0.2$ V $< V_{ID} < 0.2$ V | H | ? |
| $V_{ID} \leq -0.2$ V | H | L |
| X | L | Z |

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

## SWITCHING TEST CIRCUIT AND WAVEFORMS

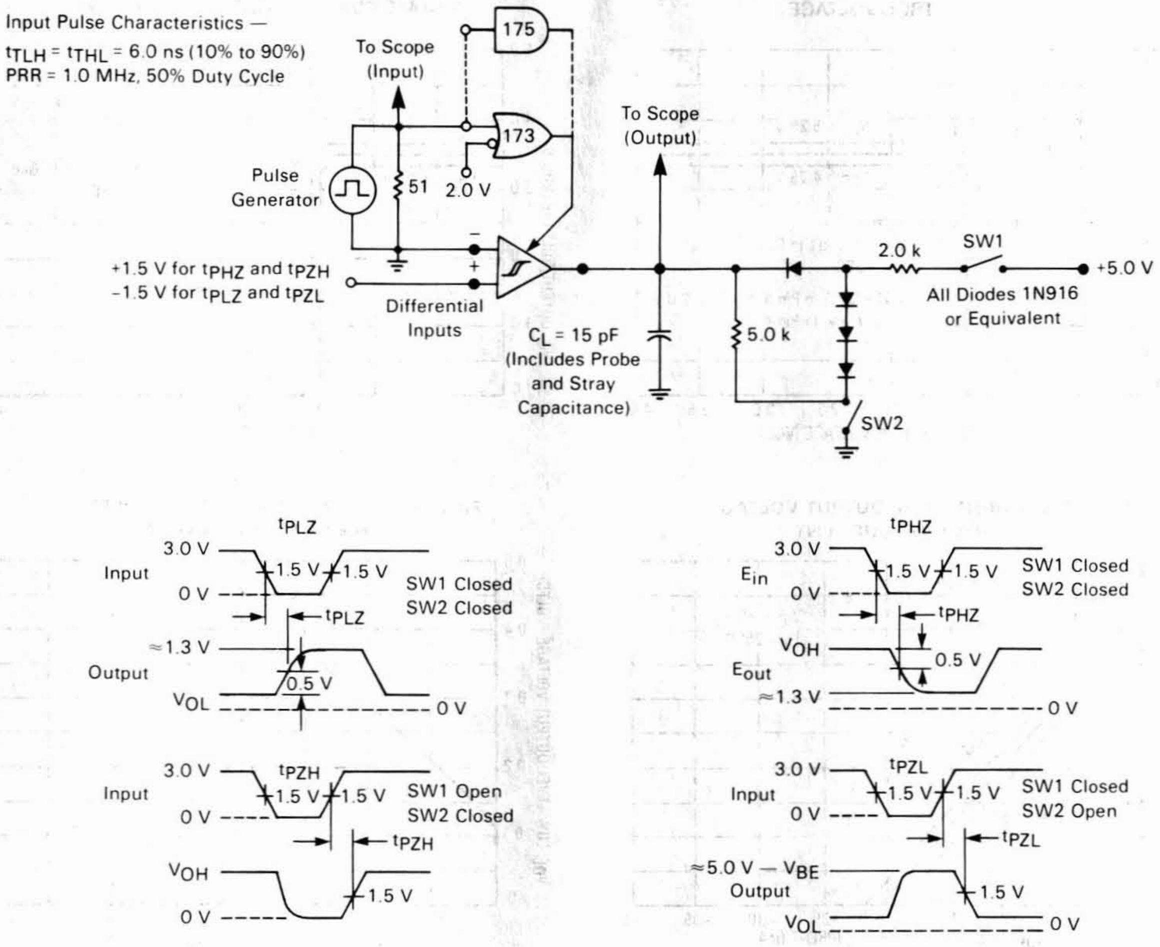
### FIGURE 1 — PROPAGATION DELAY, DIFFERENTIAL INPUT TO OUTPUT


To Scope (Input)
To Scope (Output)
Differential Inputs
Pulse Generator
51
$C_L$ = 15 pF (Includes Probe and Stray Capacitance)
+1.5 V
173
175
+2.0 V
3-State Control
3.0 V
Input
1.5 V
1.5 V
0 V
$t_{PLH(D)}$
$t_{PHL(D)}$
$V_{OH}$
Output
1.3 V
1.3 V
$V_{OL}$
0 V

Input Pulse Characteristics —
$t_{TLH} = t_{THL} = 6.0$ ns (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle

## SWITCHING TEST CIRCUIT AND WAVEFORMS (continued)

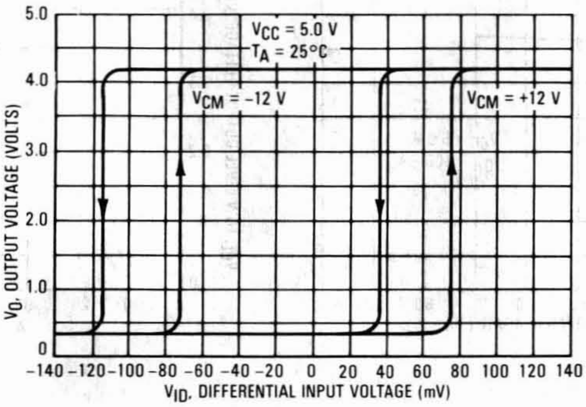
FIGURE 2 — PROPAGATION DELAY, THREE-STATE CONTROL INPUT TO OUTPUT


Input Pulse Characteristics —
$t_{TLH} = t_{THL} = 6.0$ ns (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle
To Scope (Input)
175
173
2.0 V
51
Pulse Generator
To Scope (Output)
+1.5 V for $t_{PHZ}$ and $t_{PZH}$
−1.5 V for $t_{PLZ}$ and $t_{PZL}$
Differential Inputs
$C_L$ = 15 pF (Includes Probe and Stray Capacitance)
5.0 k
2.0 k
SW1
+5.0 V
All Diodes 1N916 or Equivalent
SW2
$t_{PLZ}$
3.0 V
Input
1.5 V
1.5 V
0 V
SW1 Closed
SW2 Closed
$t_{PLZ}$
≈1.3 V
Output
0.5 V
$V_{OL}$
0 V
$t_{PHZ}$
3.0 V
$E_{in}$
1.5 V
1.5 V
0 V
SW1 Closed
SW2 Closed
$t_{PHZ}$
$V_{OH}$
0.5 V
$E_{out}$
≈1.3 V
0 V
3.0 V
$t_{PZH}$
Input
1.5 V
1.5 V
SW1 Open
SW2 Closed
0 V
$t_{PZH}$
$V_{OH}$
1.5 V
0 V
3.0 V
$t_{PZL}$
Input
1.5 V
1.5 V
SW1 Closed
SW2 Open
0 V
$t_{PZL}$
≈5.0 V − $V_{BE}$
Output
1.5 V
$V_{OL}$
0 V

## TYPICAL CHARACTERISTICS

(Both Device Types, Unless Otherwise Noted)

FIGURE 3 — OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE



## TYPICAL CHARACTERISTICS (continued)

**FIGURE 4 — OUTPUT VOLTAGE versus 3-STATE CONTROL VOLTAGE**

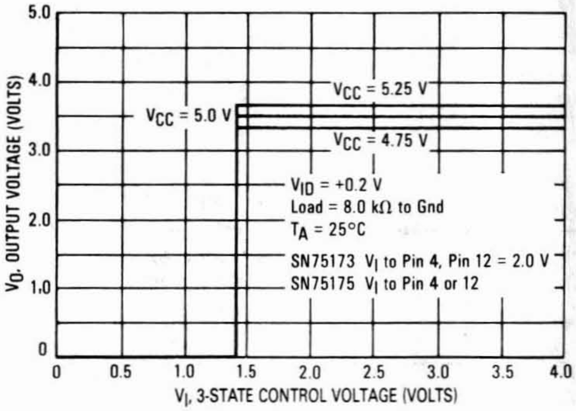


**FIGURE 5 — OUTPUT VOLTAGE versus (INVERTED) 3-STATE CONTROL VOLTAGE — SN75173**

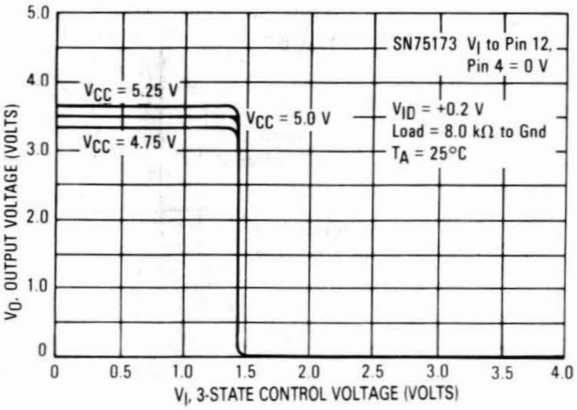


**FIGURE 6 — HIGH LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT**

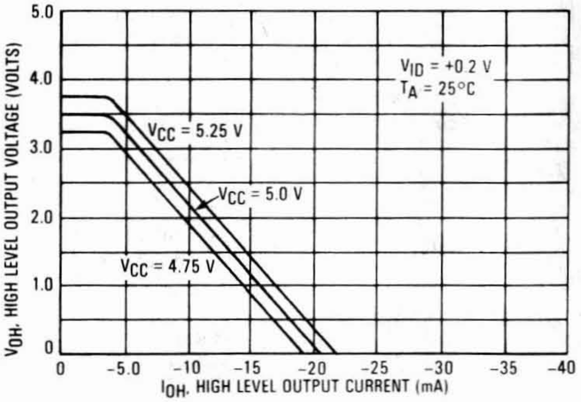


**FIGURE 7 — LOW LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT**

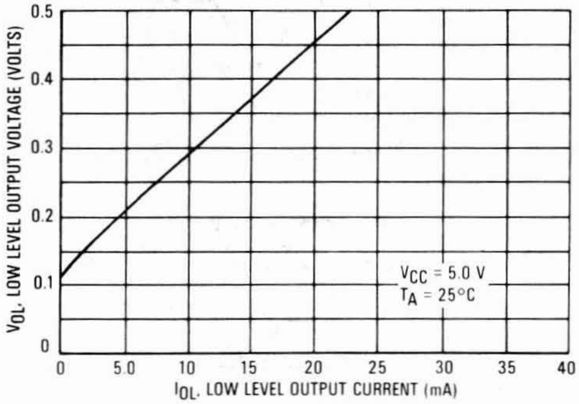


**FIGURE 8 — HIGH LEVEL OUTPUT VOLTAGE versus TEMPERATURE**

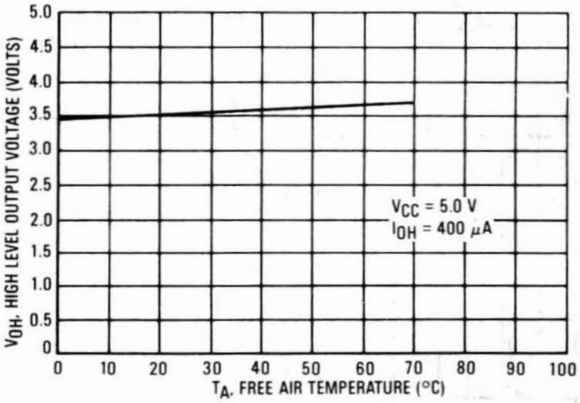
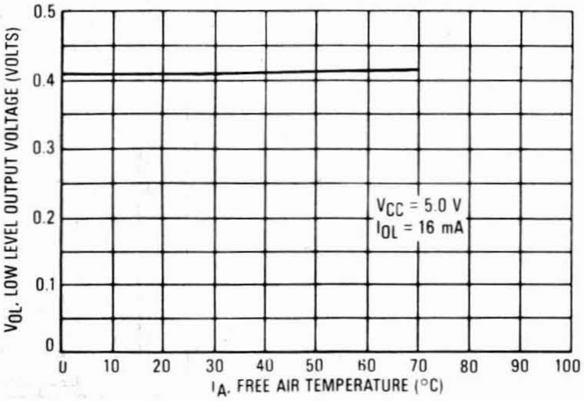


**FIGURE 9 — LOW LEVEL OUTPUT VOLTAGE versus TEMPERATURE**



**MOTOROLA**

# ULN2068B

## QUAD 1.5 A SINKING HIGH-CURRENT SWITCH

The ULN2068B is a high-voltage, high-current quad Darlington switch array designed for high-current loads, both resistive and reactive, up to 300 watts.

It is intended for interfacing between low level (TTL, DTL, LS and 5.0 V CMOS) logic families and peripheral loads such as relays, solenoids, dc and stepping motors, multiplexer LED and incandescent displays, heaters, or other high-voltage, high-current loads.

The Motorola ULN2068B is specified with minimum guaranteed breakdown of 50 V and is 100% tested for safe area using an inductive load. It includes integral transient suppression diodes. Use of a predriver stage reduces input current while still allowing the device to switch 1.5 Amps.

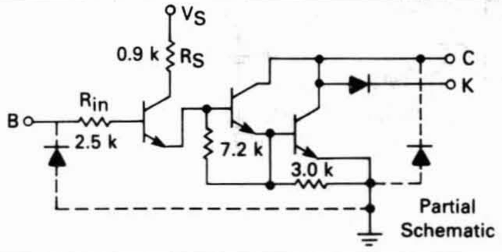
It is supplied in an improved 16-lead plastic dual-in-line package with heat sink contact tabs (Pins 4,5 and 12,13). A copper alloy lead frame allows maximum power dissipation using standard cooling techniques. The use of the contact tab lead frame facilitates attachment of a DIP heat sink while permitting the use of standard layout and mounting practices.

- TTL, DTL, LS, CMOS Compatible Inputs
- 1.5 Amp Maximum Output Current
- Low Input Current
- Internal Freewheeling Clamp Diodes
- 100% Inductive Load Tested
- Heat Tab Copper Alloy Lead Frame for Increased Dissipation

**MAXIMUM RATINGS** ($T_A$ = 25°C and ratings apply to any one device in the package unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Output Voltage | $V_O$ | 50 | V |
| Input Voltage — Note 2 | $V_I$ | 15 | V |
| Supply Voltage | $V_S$ | 10 | V |
| Collector Current — Note 1 | $I_C$ | 1.75 | A |
| Input Current — Note 3 | $I_I$ | 25 | mA |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Junction Temperature | $T_J$ | 150 | °C |

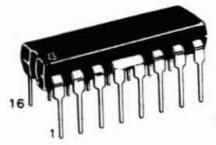
Notes:
1. Allowable output conditions shown in curves on Page 3.
2. Input voltage referenced to ground.
3. May be limited by max input voltage.



Partial Schematic

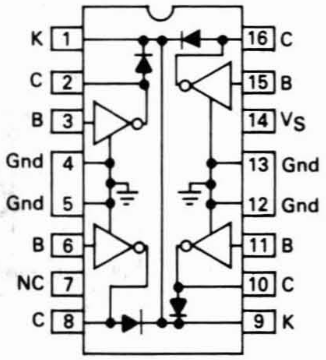
## QUAD 1.5 A DARLINGTON SWITCH

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**B SUFFIX**
PLASTIC PACKAGE
CASE 648C-01

**PIN CONNECTIONS**



**ORDERING INFORMATION***

| Device | Temperature Range | Package |
|---|---|---|
| ULN2068B | 0°C to +70°C | Plastic DIP |

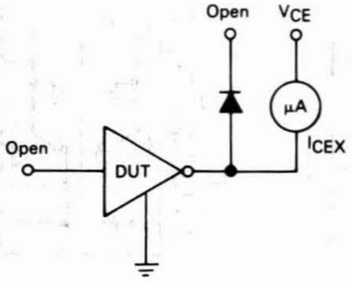
* Other options of this ULN2060/2070 series are available for volume applications. Contact your local Motorola Sales Representative.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted.)

| Characteristic | Fig. | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Leakage Current<br>($V_{CE}$ = 50 V)<br>($V_{CE}$ = 50 V, $T_A$ = 70°C) | 1 | $I_{CEX}$ | —<br>— | —<br>— | 100<br>500 | μA |
| Collector-Emitter Saturation Voltage<br>($I_C$ = 500 mA<br>($I_C$ = 750 mA<br>($I_C$ = 1.0 A<br>($I_C$ = 1.25 A<br>} $V_{in}$ = 2.4 V) | 2 | $V_{CE(sat)}$ | —<br>—<br>—<br>— | —<br>—<br>—<br>— | 1.13<br>1.25<br>1.40<br>1.60 | V |
| Input Current — On Condition<br>($V_I$ = 2.4 V)<br>($V_I$ = 3.75 V) | 4 | $I_{I(on)}$ | —<br>— | —<br>— | 0.25<br>1.0 | mA |
| Input Voltage — On Condition<br>($V_{CE}$ = 2.0 V, $I_C$ = 1.5 A) | 5 | $V_{I(on)}$ | — | — | 2.4 | V |
| Inductive Load Test<br>($V_S$ = 5.5 V, $V_{CC}$ = 24.5 V,<br>$t_{PW}$ = 4.0 ms) | 3 | $\Delta V_{out}$ | — | — | 100 | mV |
| Supply Current<br>($I_C$ = 500 mA, $V_{in}$ = 2.4 V, $V_S$ = 5.5 V) | 8 | $I_S$ | — | — | 6.0 | mA |
| Turn-On Delay Time<br>(50% $E_I$ to 50% $E_O$) | — | $t_{PHL}$ | — | — | 1.0 | μs |
| Turn-Off Delay Time<br>(50% $E_I$ to 50% $E_O$) | — | $t_{PLH}$ | — | — | 4.0 | μs |
| Clamp Diode Leakage Current<br>($V_R$ = 50 V)<br>($V_R$ = 50 V, $T_A$ = 70°C) | 6 | $I_R$ | —<br>— | —<br>— | 50<br>100 | μA |
| Clamp Diode Forward Voltage<br>($I_F$ = 1.0 A)<br>($I_F$ = 1.5 A) | 7 | $V_F$ | —<br>— | —<br>— | 1.75<br>2.0 | V |

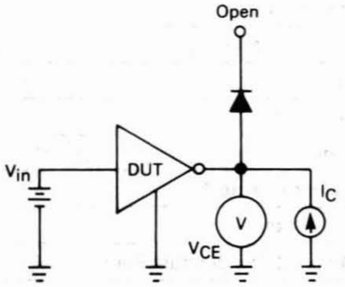
## TEST FIGURES

**FIGURE 1**



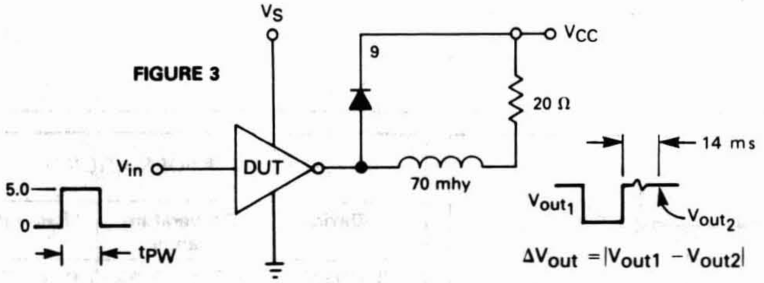
Open
VCE
μA
ICEX
Open
DUT

**FIGURE 2**



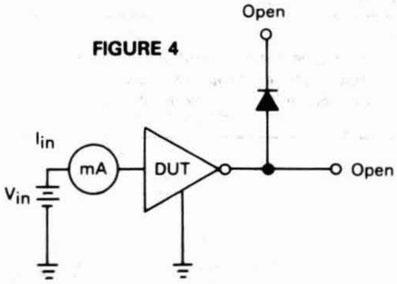
Open
Vin
DUT
IC
V
VCE

**FIGURE 3**



VS
VCC
9
20 Ω
Vin
DUT
70 mhy
5.0
0
tPW
14 ms
Vout1
Vout2
ΔVout = |Vout1 − Vout2|

**FIGURE 4**



Open
Iin
Vin
mA
DUT
Open

## TEST FIGURES (CONTINUED)

**FIGURE 5**

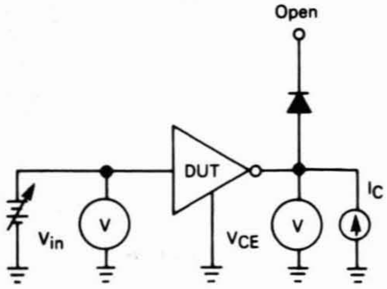

Open
DUT
$V_{in}$
V
$V_{CE}$
V
$I_C$

**FIGURE 6**

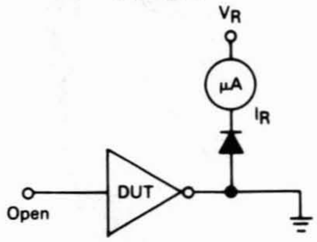

$V_R$
µA
$I_R$
Open
DUT

**FIGURE 7**

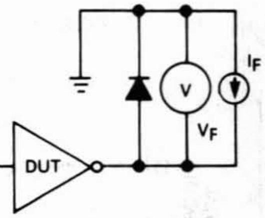
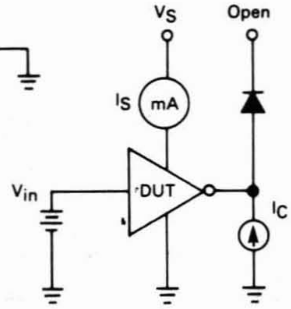

$I_F$
V
$V_F$
DUT
Open

**FIGURE 8**


$V_S$
Open
$I_S$
mA
$V_{in}$
DUT
$I_C$

5

## TYPICAL CHARACTERISTIC CURVES — $T_A$ = 25°C

**FIGURE 9 — INPUT CURRENT versus INPUT VOLTAGE**

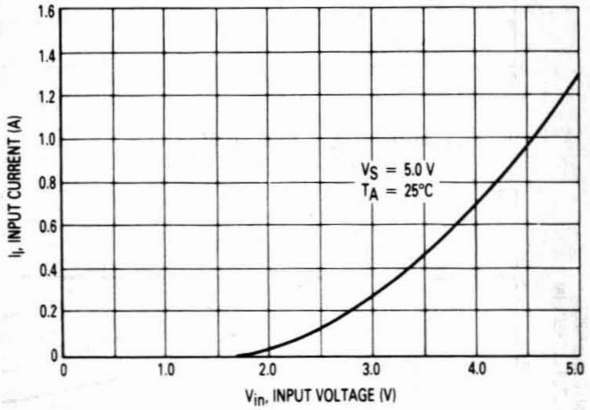


**FIGURE 10 — COLLECTOR CURRENT versus INPUT CURRENT**

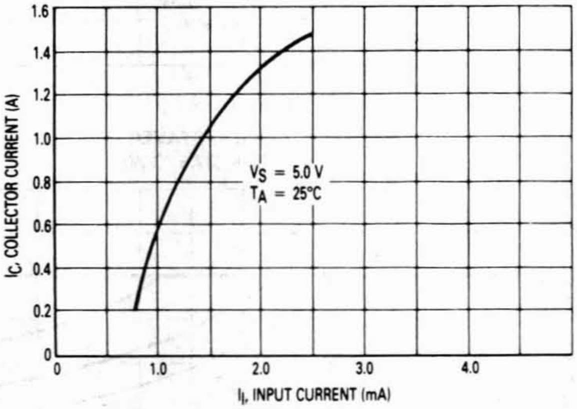


**FIGURE 11 — $T_A$ = 70°C w/o HEAT SINK**

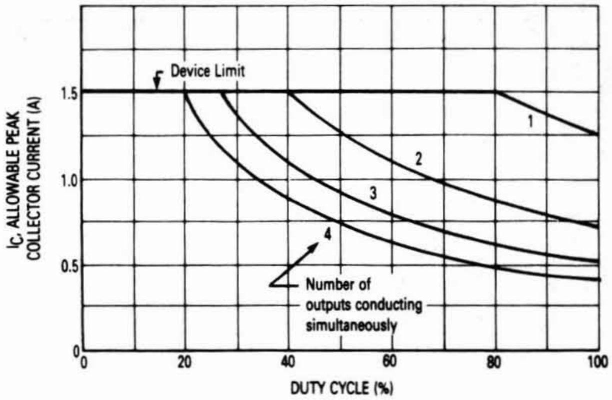


**FIGURE 12 — $T_A$ = 70°C w/STAVER V-8 HEAT SINK (37.5 °C/W)**

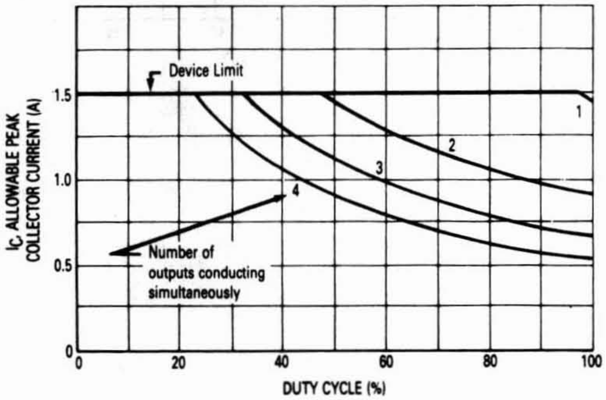


FIGURE 13 — $T_A$ = 70°C w/STAVER V-7 HEAT SINK (27.5 °C/W)

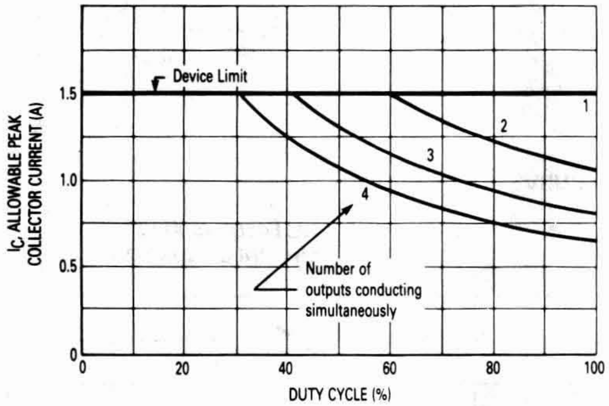


FIGURE 14 — $T_A$ = 50°C w/o HEAT SINK

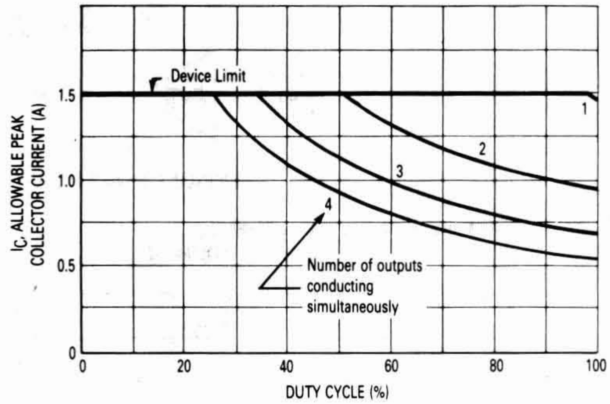


FIGURE 15 — $T_A$ = 50°C w/STAVER V-8 HEAT SINK (37.5 °C/W)

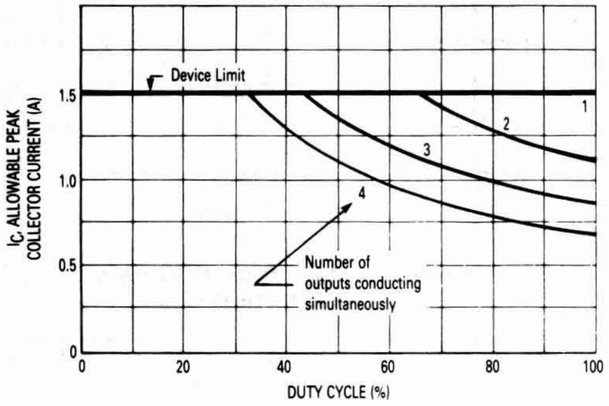
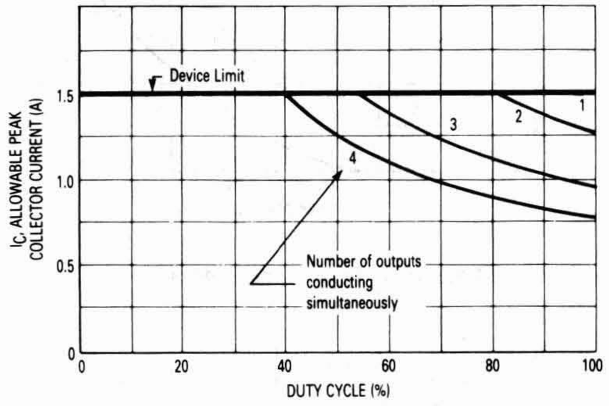


FIGURE 16 — $T_A$ = 50°C w/ STAVER V-7 HEAT SINK (27.5 °C/W)



**MOTOROLA**

# ULN2074B

## QUAD 1.5 A SINKING HIGH-CURRENT SWITCH

The ULN2074B is a high-voltage, high-current quad Darlington switch array designed for high-current loads, both resistive and reactive, up to 300 watts.

It is intended for interfacing between low level (TTL, DTL, LS and 5.0 V CMOS) logic families and peripheral loads such as relays, solenoids, dc and stepping motors, multiplexer LED and incandescent displays, heaters, or other high-voltage, high-current loads.

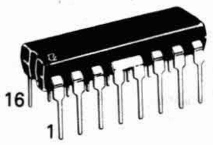
The Motorola ULN2074B is specified with minimum guaranteed breakdown of 50 V and is 100% tested for safe area using an inductive load.

It is supplied in an improved 16-lead plastic dual-in-line package with heat sink contact tabs (Pins 4, 5 and 12, 13). A copper alloy lead frame allows maximum power dissipation using standard cooling techniques. The use of the contact tab lead frame facilitates attachment of a DIP heat sink while permitting the use of standard layout and mounting practices.

- TTL, DTL, LS, CMOS Compatible Inputs
- 1.5 Amp maximum Output Current
- Low Input Current
- 100% Inductive Load Tested
- Heat Tab Copper Alloy Lead Frame for Increased Dissipation

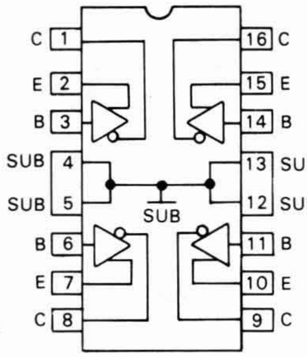
## QUAD 1.5 A DARLINGTON SWITCH

### SILICON MONOLITHIC INTEGRATED CIRCUIT



**B SUFFIX**
PLASTIC PACKAGE
CASE 648C-01

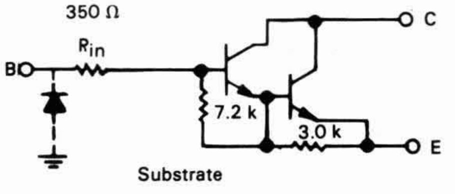
### PIN CONNECTIONS



**MAXIMUM RATINGS** ($T_A$ = 25°C and ratings apply to any one device in the package unless otherwise noted).

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Output Voltage | $V_O$ | 50 | V |
| Input Voltage — Note 2 | $V_I$ | 30 | V |
| Collector Current — Note 1 | $I_C$ | 1.75 | A |
| Input Current — Note 3 | $I_I$ | 25 | mA |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -55 to +150 | °C |
| Junction Temperature | $T_J$ | 150 | °C |

Notes:
1. Allowable output conditions shown in curves on Page 3.
2. Input voltage referenced to ground (substrate)
3. May be limited by max input voltage



Partial Schematic

**ORDERING INFORMATION***

| Device | Temperature Range | Package |
|---|---|---|
| ULN2074B | 0°C to +70°C | Plastic DIP |

* Other options of this ULN2060/2070 series are available for volume applications. Contact your local Motorola Sales Representative.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Fig. | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Leakage Current | | $I_{CEX}$ | | | | µA |
| ($V_{CE}$ = 50 V) | 1 | | — | — | 100 | |
| ($V_{CE}$ = 50 V, $T_A$ = 70°C) | | | — | — | 500 | |
| Collector-Emitter Saturation Voltage | | $V_{CE(sat)}$ | | | | V |
| ($I_C$ = 500 mA, $I_I$ = 625 µA) | | | — | — | 1.13 | |
| ($I_C$ = 750 mA, $I_I$ = 935 µA) | 2 | | — | — | 1.25 | |
| ($I_C$ = 1.0 A, $I_I$ = 1.25 mA) | | | — | — | 1.40 | |
| ($I_C$ = 1.25 A, $I_I$ = 2.0 mA) | | | — | — | 1.60 | |
| Input Current — On Condition | | $I_{I(on)}$ | | | | mA |
| ($V_I$ = 2.4 V) | 4 | | 2.0 | — | 4.3 | |
| ($V_I$ = 3.75 V) | | | 4.5 | — | 9.6 | |
| Input Voltage — On Condition | 5 | $V_{I(on)}$ | | | | V |
| ($V_{CE}$ = 2.0 V, $I_C$ = 1.0 A) | | | — | — | 2.0 | |
| ($V_{CE}$ = 2.0 V, $I_C$ = 1.5 A) | | | — | — | 2.5 | |
| Inductive Load Test<br>($V_{CC}$ = 24.5 V, $t_{PW}$ = 4.0 µs) | 3 | $\Delta V_{out}$ | — | — | 100 | mV |
| Turn-On Delay Time<br>(50% $E_I$ to 50% $E_O$) | — | $t_{PHL}$ | — | — | 1.0 | µs |
| Turn-Off Delay Time<br>(50% $E_I$ to 50% $E_O$) | — | $t_{PLH}$ | — | — | 1.5 | µs |

## TEST FIGURES

FIGURE 1

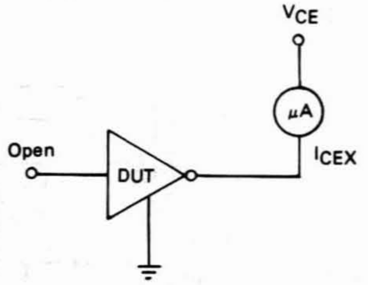

VCE
µA
ICEX
Open
DUT

FIGURE 2

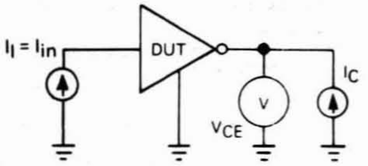

II = Iin
DUT
V
VCE
IC

FIGURE 3

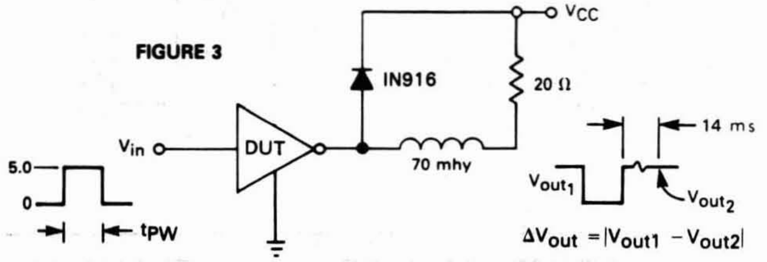

VCC
IN916
20 Ω
Vin
DUT
70 mhy
5.0
0
tPW
14 ms
Vout1
Vout2
ΔVout = |Vout1 − Vout2|

FIGURE 4

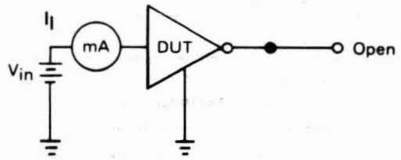
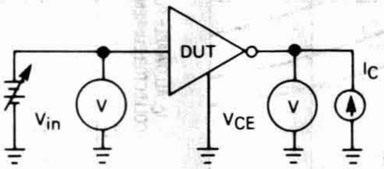

II
mA
DUT
Open
Vin

FIGURE 5



## TYPICAL CHARACTERISTIC CURVES

FIGURE 6 — INPUT CURRENT versus INPUT VOLTAGE

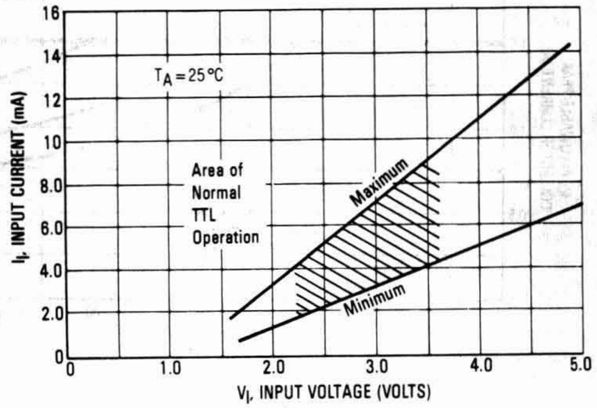


FIGURE 7 — COLLECTOR CURRENT versus INPUT CURRENT

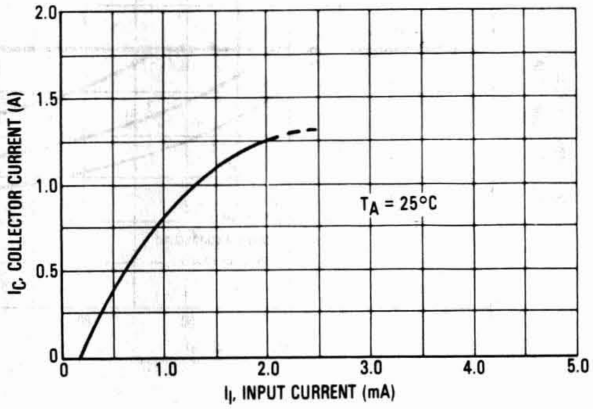


FIGURE 8 — $T_A = 70°C$ w/o HEAT SINK

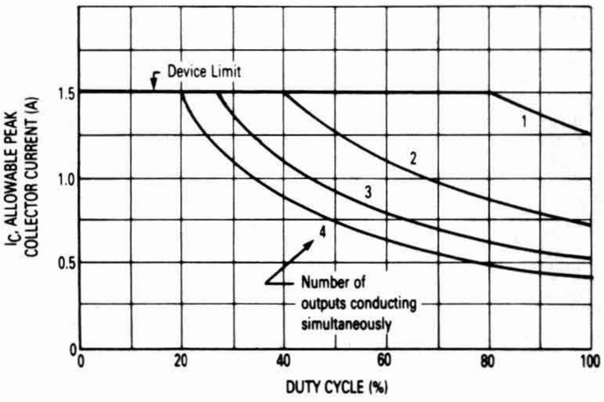


FIGURE 9 — $T_A = 70°C$ w/STAVER V-8 HEAT SINK (37.5 °C/W)

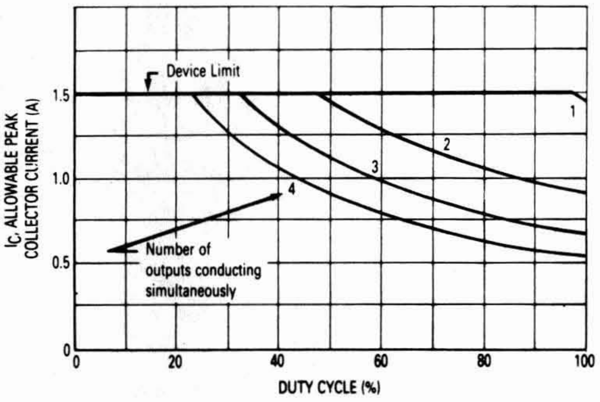


**FIGURE 10 — $T_A$ = 70°C w/STAVER V-7 HEAT SINK (27.5 °C/W)**

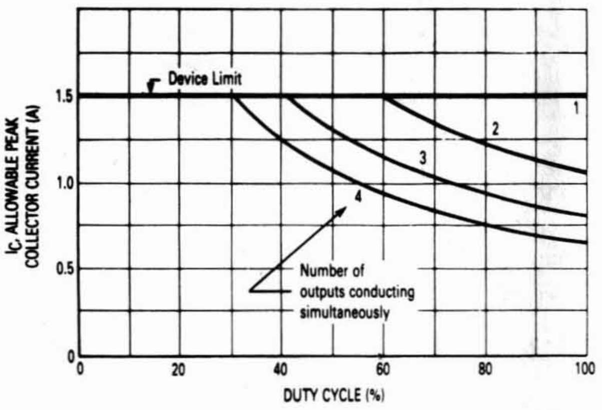


**FIGURE 11 — $T_A$ = 50°C w/o HEAT SINK**

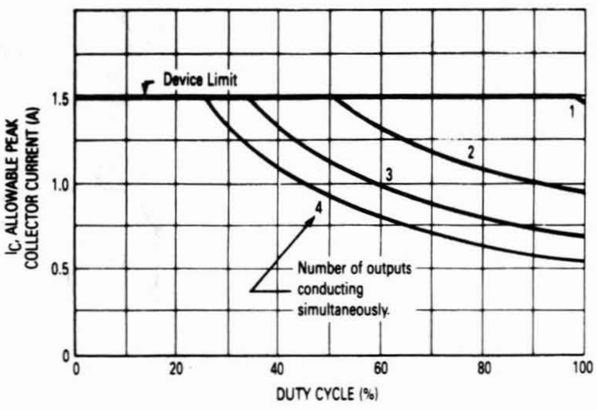


**FIGURE 12 — $T_A$ = 50°C w/STAVER V-8 HEAT SINK (37.5 °C/W)**

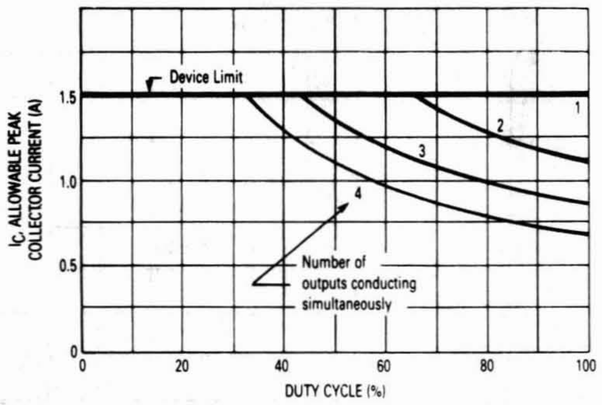
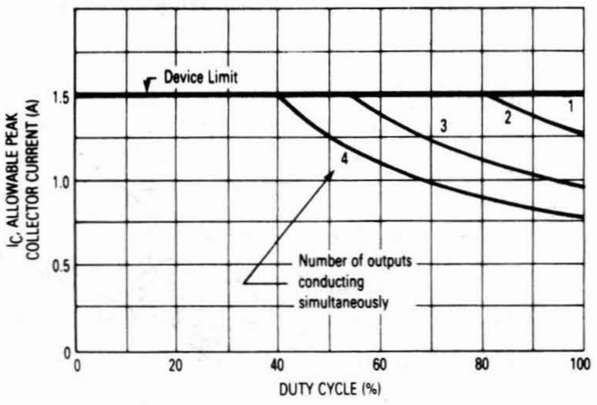


**FIGURE 13 — $T_A$ = 50°C w/STAVER V-7 HEAT SINK (27.5 °C/W)**



**MOTOROLA**

# ULN2801
# ULN2802
# ULN2803
# ULN2804

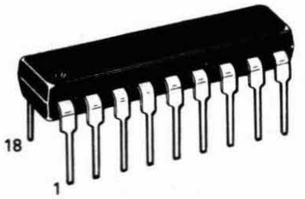
## OCTAL HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The eight NPN Darlington-connected transistors in this family of arrays are ideally suited for interfacing between low logic level digital circuitry (such as TTL, CMOS or PMOS/NMOS) and the higher current/voltage requirements of lamps, relays, printer hammers or other similar loads for a broad range of computer, industrial, and consumer applications. All devices feature open-collector outputs and free wheeling clamp diodes for transient suppression.

The ULN2801 is a general purpose device for use with CMOS, PMOS or TTL logic. The ULN2802 contains a zener diode and resistor in series with the input to limit input currents and assure compatibility with 14 to 25 volt PMOS logic. The ULN2803 is designed to be compatible with standard TTL families while the ULN2804 is optimized for 6 to 15 volt high level CMOS or PMOS.

## OCTAL PERIPHERAL DRIVER ARRAYS

### SILICON MONOLITHIC INTEGRATED CIRCUITS



**A SUFFIX**
PLASTIC PACKAGE
CASE 707-02

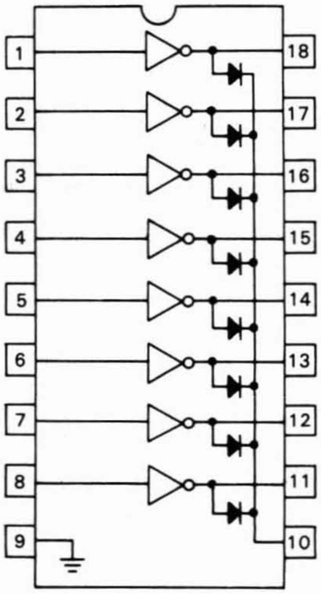
**MAXIMUM RATINGS** ($T_A$ = 25°C and rating apply to any one device in the package unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Output Voltage | $V_O$ | 50* | V |
| Input Voltage (Except ULN2801) | $V_I$ | 30 | V |
| Collector Current — Continuous | $I_C$ | 500 | mA |
| Base Current — Continuous | $I_B$ | 25 | mA |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -55 to +150 | °C |
| Junction Temperature | $T_J$ | 125 | °C |

$R_{\theta JA}$ = 55°C/W
Do not exceed maximum current
per driver

*Higher voltage selection available. See your local representative.

**PIN CONNECTIONS**



## ORDERING INFORMATION

| DEVICE | CHARACTERISTICS | | |
|---|---|---|---|
| | INPUT COMPATIBILITY | $V_{CE}(MAX)/I_C(MAX)$ | $T_A$ |
| ULN2801A | General Purpose CMOS, PMOS | 50 V/500 mA | 0 to +70°C |
| ULN2802A | 14-25 Volt PMOS | 50 V/500 mA | 0 to +70°C |
| ULN2803A | TTL, 5.0 V CMOS | 50 V/500 mA | 0 to +70°C |
| ULN2804A | 6-15 V CMOS, PMOS | 50 V/500 mA | 0 to +70°C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Fig. | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Output Leakage Current | | 1 | $I_{CEX}$ | | | | μA |
| (*$V_O$ = 50 V, $T_A$ = +70°C) | All Types | | | — | — | 100 | |
| (*$V_O$ = 50 V, $T_A$ = +25°C) | All Types | | | — | — | 50 | |
| (*$V_O$ = 50 V, $T_A$ = +70°C, $V_I$ = 6.0 V) | ULN2802 | | | — | — | 500 | |
| (*$V_O$ = 50 V, $T_A$ = +70°C, $V_I$ = 1.0 V) | ULN2804 | | | — | — | 500 | |
| Collector-Emitter Saturation Voltage | | 2 | $V_{CE(sat)}$ | | | | V |
| ($I_C$ = 350 mA, $I_B$ = 500 μA) | All Types | | | — | 1.1 | 1.6 | |
| ($I_C$ = 200 mA, $I_B$ = 350 μA) | All Types | | | — | 0.95 | 1.3 | |
| ($I_C$ = 100 mA, $I_B$ = 250 μA) | All Types | | | — | 0.85 | 1.1 | |
| Input Current — On Condition | | 4 | $I_{I(on)}$ | | | | mA |
| ($V_I$ = 17 V) | ULN2802 | | | — | 0.82 | 1.25 | |
| ($V_I$ = 3.85 V) | ULN2803 | | | — | 0.93 | 1.35 | |
| ($V_I$ = 5.0 V) | ULN2804 | | | — | 0.35 | 0.5 | |
| ($V_I$ = 12 V) | ULN2804 | | | — | 1.0 | 1.45 | |
| Input Voltage — On Condition | | 5 | $V_{I(on)}$ | | | | V |
| ($V_{CE}$ = 2.0 V, $I_C$ = 300 mA) | ULN2802 | | | — | — | 13 | |
| ($V_{CE}$ = 2.0 V, $I_C$ = 200 mA) | ULN2803 | | | — | — | 2.4 | |
| ($V_{CE}$ = 2.0 V, $I_C$ = 250 mA) | ULN2803 | | | — | — | 2.7 | |
| ($V_{CE}$ = 2.0 V, $I_C$ = 300 mA) | ULN2803 | | | — | — | 3.0 | |
| ($V_{CE}$ = 2.0 V, $I_C$ = 125 mA) | ULN2804 | | | — | — | 5.0 | |
| ($V_{CE}$ = 2.0 V, $I_C$ = 200 mA) | ULN2804 | | | — | — | 6.0 | |
| ($V_{CE}$ = 2.0 V, $I_C$ = 275 mA) | ULN2804 | | | — | — | 7.0 | |
| ($V_{CE}$ = 2.0 V, $I_C$ = 350 mA) | ULN2804 | | | — | — | 8.0 | |
| Input Current — Off Condition<br>($I_C$ = 500 μA, $T_A$ = +70°C) | All Types | 3 | $I_{I(off)}$ | 50 | 100 | — | μA |
| DC Current Gain<br>($V_{CE}$ = 2.0 V, $I_C$ = 350 mA) | ULN2801 | 2 | $h_{FE}$ | 1000 | — | — | — |
| Input Capacitance | | | $C_I$ | — | 15 | 25 | pF |
| Turn-On Delay Time<br>(50% $E_I$ to 50% $E_O$) | | | $t_{on}$ | — | 0.25 | 1.0 | μs |
| Turn-Off Delay Time<br>(50% $E_I$ to 50% $E_O$) | | | $t_{off}$ | — | 0.25 | 1.0 | μs |
| Clamp Diode Leakage Current<br>($V_R$ = 50 V) | $T_A$ = +25°C<br>$T_A$ = +70°C | 6 | $I_R$ | — | — | 50<br>100 | μA |
| Clamp Diode Forward Voltage<br>($I_F$ = 350 mA) | | 7 | $V_F$ | — | 1.5 | 2.0 | V |

*Higher voltage selections available, contact your local representative.

## TEST FIGURES

(SEE FIGURE NUMBERS IN ELECTRICAL CHARACTERISTICS TABLES)

FIGURE 1

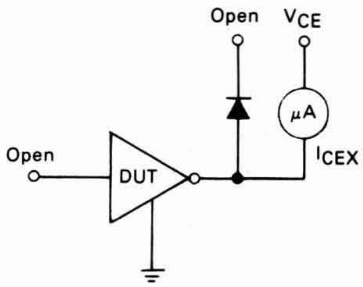

Open
VCE
μA
ICEX
Open
DUT

FIGURE 2

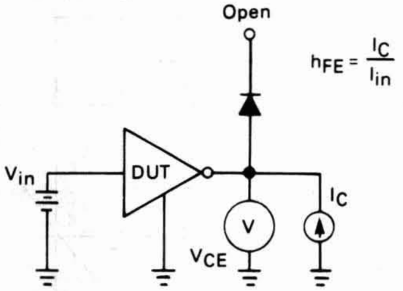

Open
hFE = IC / Iin
Vin
DUT
V
VCE
IC

FIGURE 3

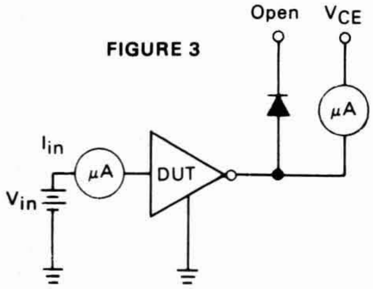

Open
VCE
μA
Iin
μA
DUT
Vin

FIGURE 4

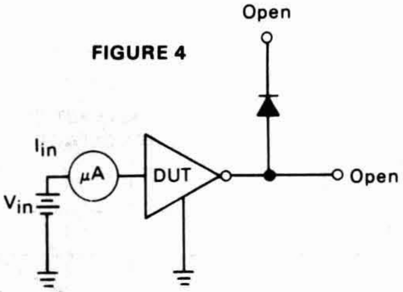

Open
Iin
μA
DUT
Open
Vin

FIGURE 5

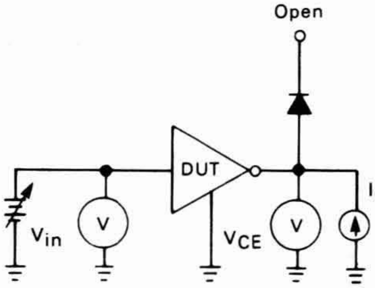

Open
DUT
IC
Vin
V
VCE
V

FIGURE 6

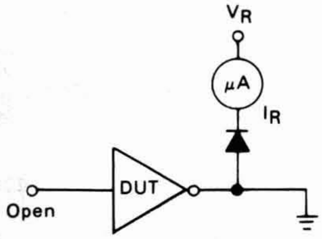
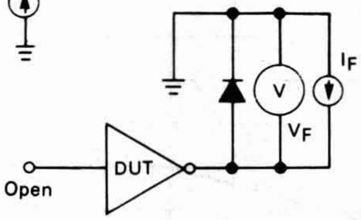

VR
μA
IR
DUT
Open

FIGURE 7


IF
V
VF
DUT
Open

## TYPICAL CHARACTERISTIC CURVES — $T_A = 25°C$
(unless otherwise noted)

### OUTPUT CHARACTERISTICS

FIGURE 8 — OUTPUT CURRENT versus SATURATION VOLTAGE

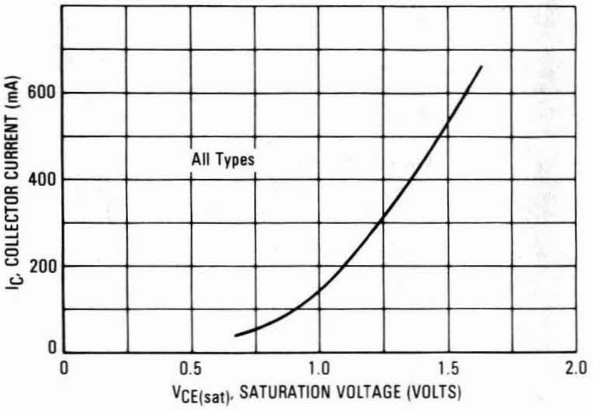
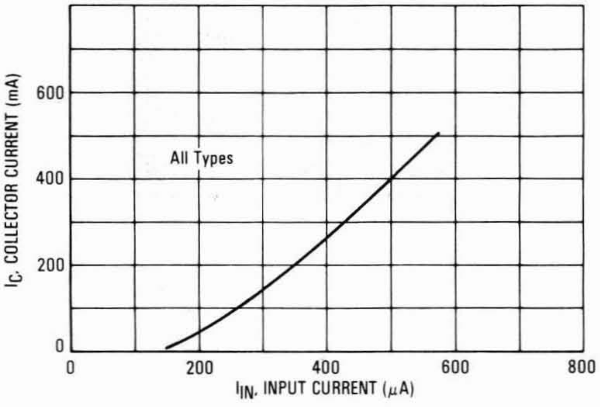


FIGURE 9 — OUTPUT CURRENT versus INPUT CURRENT



### INPUT CHARACTERISTICS

FIGURE 10 — ULN2802 INPUT CURRENT versus INPUT VOLTAGE

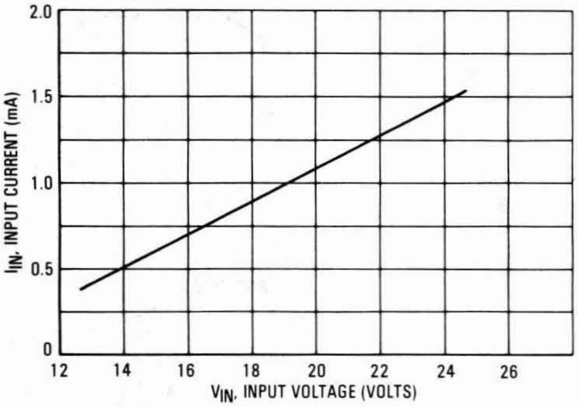


FIGURE 11 — ULN2803 INPUT CURRENT versus INPUT VOLTAGE

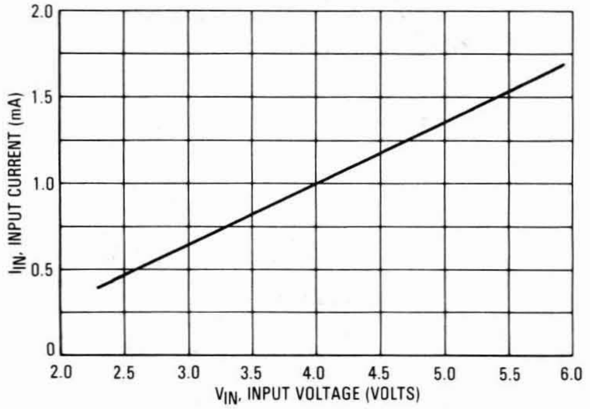
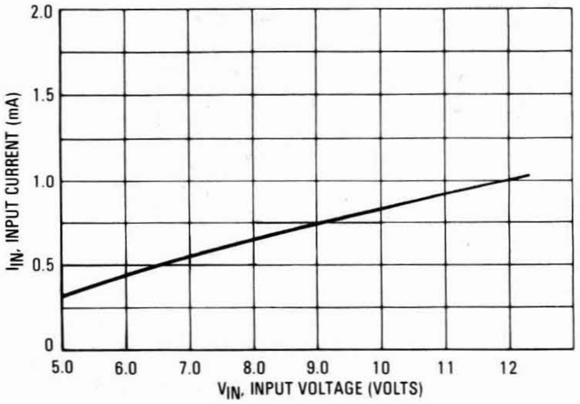
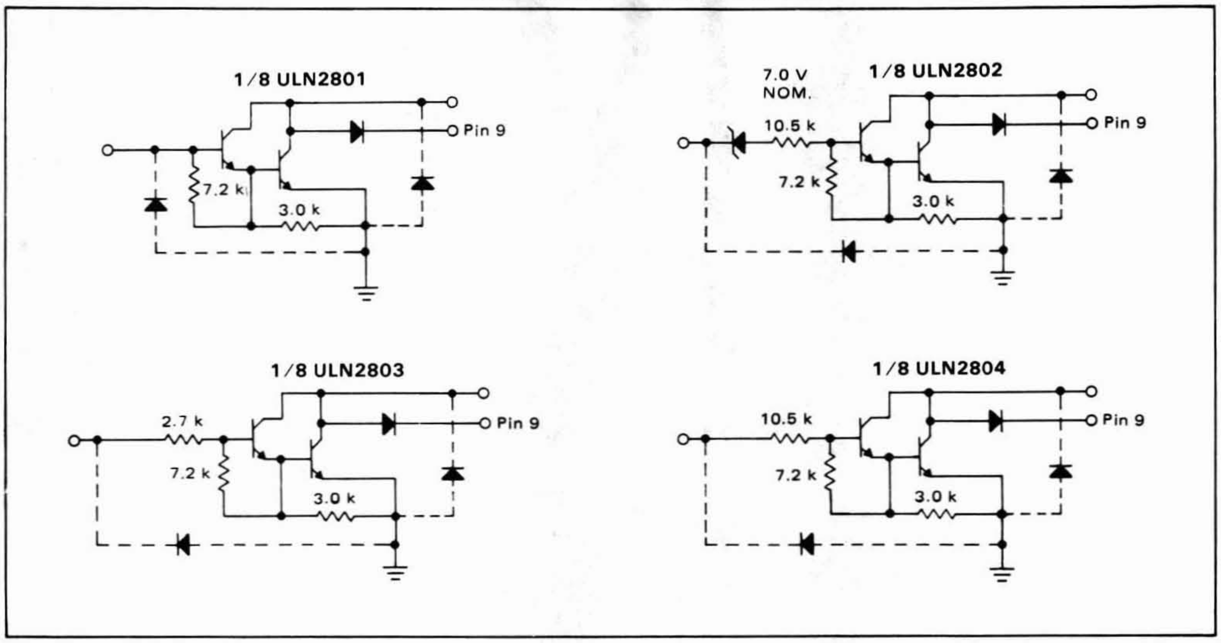


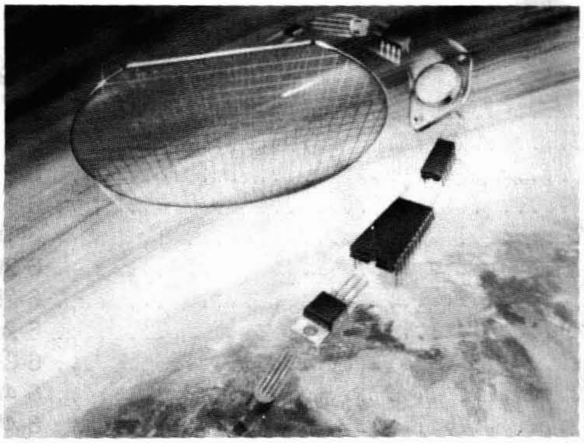
FIGURE 12 — ULN2804 INPUT CURRENT versus INPUT VOLTAGE



REPRESENTATIVE CIRCUIT SCHEMATICS


1/8 ULN2801
Pin 9
7.2 k
3.0 k
7.0 V
NOM.
1/8 ULN2802
10.5 k
Pin 9
7.2 k
3.0 k
1/8 ULN2803
2.7 k
Pin 9
7.2 k
3.0 k
1/8 ULN2804
10.5 k
Pin 9
7.2 k
3.0 k

5



# Consumer and Automotive Circuits

6

# CONSUMER AND AUTOMOTIVE CIRCUITS

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| MC1352 | TV Video IF Amplifier | 6-20 |
| MC1355 | Limiting FM IF Amplifier | 6-25 |
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| MC1358 | TV Sound IF Amplifier | 6-35 |
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| MC1373 | TV Video Modulator | 6-48 |
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| MC1394P | TV Horizontal Processor | 6-72 |
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| MC3321P | Class B Audio Drivers | 6-77 |
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| MC3334P | High Energy Ignition Circuit | 6-85 |
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| MC13002XP | Monomax Black-and-White TV Subsystem | 6-119 |
| MC13010P | TV Parallel Sound IF and AFT | 6-128 |
| MC13020P | CQUAM$^{R}$ AM Stereo Decoder | 6-133 |
| MCC3334 | High Energy Ignition Circuit | 6-85 |
| MCCF3334 | High Energy Ignition Circuit | 6-85 |
| NE565A | Phase-Locked Loop | 6-138 |
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| TCA4500A | FM Stereo Demodulator | 6-147 |
| TCA5550 | Stereo Sound Control System | 6-154 |
| TDA1190P | TV Sound System | 6-158 |
| TDA3190P | TV Sound System | 6-158 |
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| TDA3303 | TV Color Processor | 6-161 |
| TDA3330 | TV Color Processor | 6-175 |
| TDA3333 | TV Color Difference Demodulator | 6-183 |

**MOTOROLA**

# CA3054

## DUAL INDEPENDENT DIFFERENTIAL AMPLIFIER

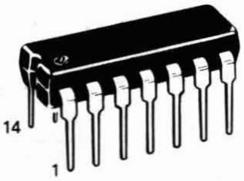
The CA3054 consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six NPN transistors which comprise the amplifiers are general purpose devices useful from dc to 120 MHz.

The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers which makes this device particularly useful in dual channel applications where matched performance of the two channels is required.

- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Maximum input offset voltage — ±5 mV

## GENERAL PURPOSE TRANSISTOR ARRAY

### SILICON MONOLITHIC INTEGRATED CIRCUIT

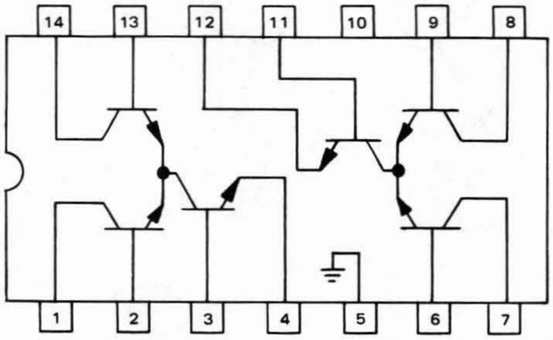


**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector-Emitter Voltage | $V_{CEO}$ | 15 | Vdc |
| Collector-Base Voltage | $V_{CBO}$ | 20 | Vdc |
| Emitter-Base Voltage | $V_{EB}$ | 5.0 | Vdc |
| Collector-Substrate Voltage | $V_{CIO}$ | 20 | Vdc |
| Collector Current — Continuous | $I_C$ | 50 | mAdc |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Temperature Range | $T_A$ | -40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

**PIN CONNECTIONS**



Pin 5 is connected to substrate and must remain at the lowest circuit potential

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER** | | | | | |
| Input Offset Voltage<br>($V_{CB}$ = 3.0 Vdc) | $V_{IO}$ | – | – | 5.0 | mV |
| Input Offset Current<br>($V_{CB}$ = 3.0 Vdc) | $I_{IO}$ | – | – | 2.0 | μA |
| Input Bias Current<br>($V_{CB}$ = 3.0 Vdc) | $I_{IB}$ | – | – | 24 | μA |
| **STATIC CHARACTERISTICS FOR EACH TRANSISTOR** | | | | | |
| Base-Emitter Voltage | $V_{BE}$ | | | | Vdc |
| ($V_{CB}$ = 3.0 Vdc, $I_C$ = 50 μA) | | – | – | 0.70 | |
| ($V_{CB}$ = 3.0 Vdc, $I_C$ = 1.0 mA) | | – | – | 0.80 | |
| ($V_{CB}$ = 3.0 Vdc, $I_C$ = 3.0 mA) | | – | – | 0.85 | |
| ($V_{CB}$ = 3.0 Vdc, $I_C$ = 10 mA) | | – | – | 0.90 | |
| Collector Cutoff Current<br>($V_{CB}$ = 10 Vdc, $I_E$ = 0) | $I_{CBO}$ | – | – | 100 | nA |
| Collector-Emitter Breakdown Voltage<br>($I_C$ = 1.0 mA) | $V_{(BR)CEO}$ | 15 | – | – | Vdc |
| Collector-Base Breakdown Voltage<br>($I_C$ = 10 μA) | $V_{(BR)CBO}$ | 20 | – | – | Vdc |
| Collector-Substrate Breakdown Voltage<br>($I_C$ = 10 μA) | $V_{(BR)CIO}$ | 20 | – | – | Vdc |
| Emitter-Base Breakdown Voltage<br>($I_E$ = 10 μA) | $V_{(BR)EBO}$ | 5.0 | – | – | Vdc |

# MC1330A1P
# MC1330A2P

## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC1330A1P | 0°C to +70°C | Plastic DIP |
| MC1330A2P | 0°C to +70°C | Plastic DIP |

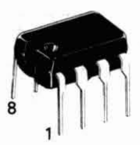
## LOW-LEVEL VIDEO DETECTOR

. . . an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and AFC buffer.

- Conversion Gain – 33 dB (Typ)
- Excellent Differential Phase and Gain
- High Rejection of IF Carrier Feedthrough
- High Video Output – 8.0 V(p-p)
- Fully Balanced Detector
- Output Temperature Compensated
- Improved Versions of the MC1330P

**LOW-LEVEL VIDEO DETECTOR**

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

## CIRCUIT DESCRIPTION

The MC1330A video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector.

The switching carrier has a buffered output for use in providing the AFT function.

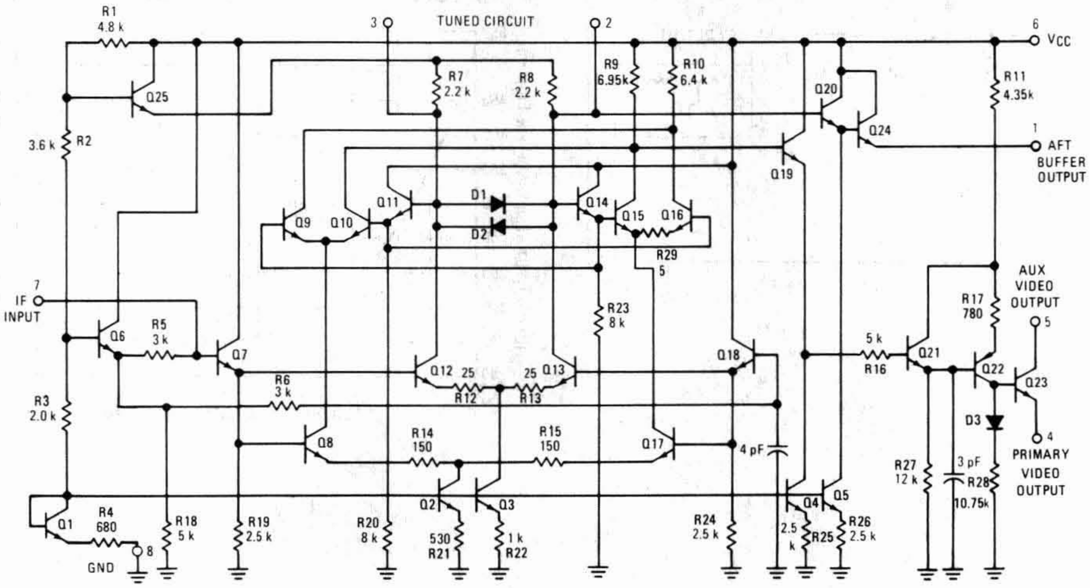
The video amplifier output is an improved design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wide band, > 8.0 MHz, with normal negative polarity. A separate narrow bandwidth, positive video output is also provided.

**OUTPUT VOLTAGE SELECTION**

The MC1330A1P is identical to the MC1330A2P with the following exception:

| | ZERO SIGNAL DC OUTPUT VOLTAGE |
|---|---|
| MC1330A1P | 7.0 to 8.2 Vdc |
| MC1330A2P | 7.8 to 9.0 Vdc |

FIGURE 1 – CIRCUIT SCHEMATIC


R1
4.8 k
3
TUNED CIRCUIT
2
6
VCC
Q25
R7
2.2 k
R8
2.2 k
R9
6.95k
R10
6.4 k
Q20
R11
4.35k
3.6 k
R2
Q24
1
AFT
BUFFER
OUTPUT
Q19
Q11
D1
Q14
Q9
Q10
Q15
Q16
D2
R29
5
AUX
VIDEO
OUTPUT
7
IF
INPUT
R23
8 k
R17
780
5
R5
3 k
Q6
Q7
Q18
5 k
R16
Q21
Q22
Q12
25
25
Q13
Q23
R6
3 k
R12
R13
R3
2.0 k
D3
R14
150
R15
150
Q8
Q17
4 pF
4
PRIMARY
VIDEO
OUTPUT
R27
12 k
3 pF
R28
10.75k
Q2
Q3
Q4
Q5
R4
680
Q1
R18
5 k
R19
2.5 k
R20
8 k
530
R21
1 k
R22
R24
2.5 k
2.5
k
R25
R26
2.5 k
8
GND

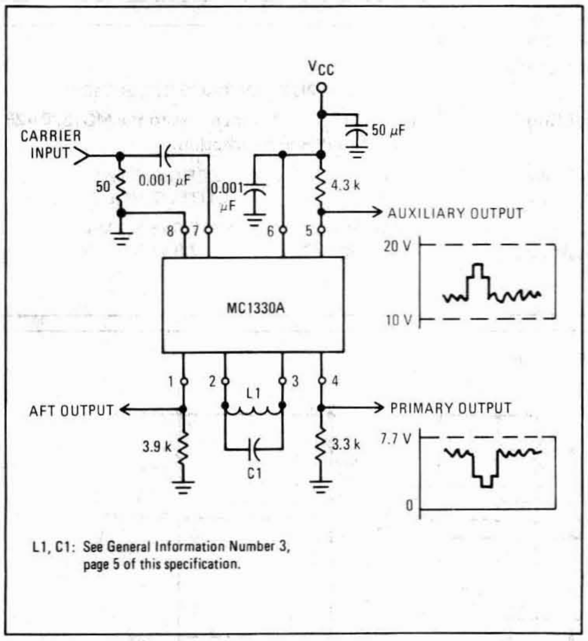
## MAXIMUM RATINGS

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage | 24 | Vdc |
| DC Video Output Current | 5.0 | mAdc |
| DC AFT Output Current | 2.0 | mAdc |
| Junction Temperature | +150 | °C |
| Operating Ambient Temperature Range | 0 to +70 | °C |
| Storage Temperature Range | −65 to +150 | °C |

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = +20 Vdc, Q = 40, fc = 45.75 MHz, $T_A$ = +25°C unless otherwise noted)

| Characteristic | | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Zero Signal dc Output Voltage | MC1330A1P | 4 | 7.0 | – | 8.2 | Vdc |
| | MC1330A2P | 4 | 7.8 | – | 9.0 | Vdc |
| Supply Current | | 5, 6 | 11 | 17.5 | 20 | mA |
| Maximum Signal dc Output Voltage | | 4 | – | 0 | 0.5 | Vdc |
| Conversion Gain for 1.0 Vp-p Output (30% Modulation) | | 7 | 25 | 36 | 65 | mVrms |
| AFT Buffer Output at Carrier Frequency | | 1 | 300 | 475 | 650 | mVp-p |

FIGURE 2 – TEST FIXTURE CIRCUIT


$V_{CC}$
CARRIER INPUT
50
0.001 µF
0.001 µF
50 µF
4.3 k
AUXILIARY OUTPUT
20 V
10 V
8
7
6
5
MC1330A
1
2
3
4
L1
C1
AFT OUTPUT
3.9 k
3.3 k
PRIMARY OUTPUT
7.7 V
0

L1, C1: See General Information Number 3, page 5 of this specification.

FIGURE 3 – INPUT ADMITTANCE

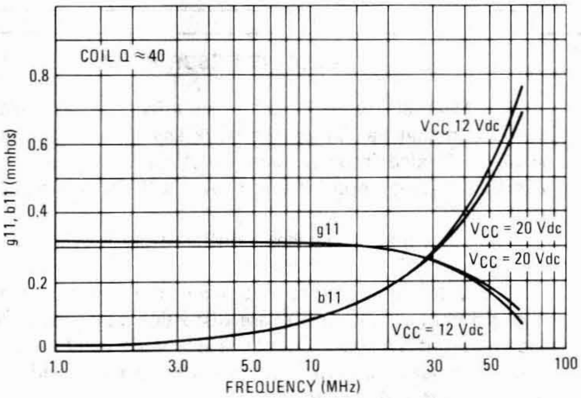
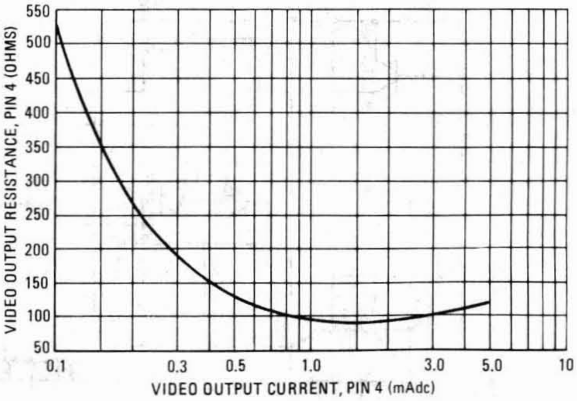


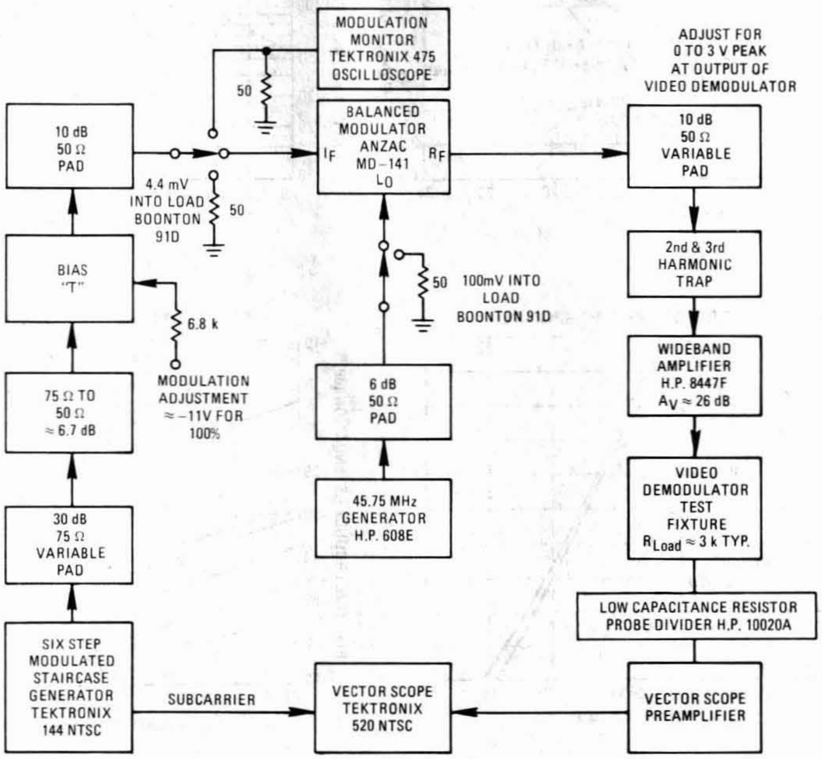
FIGURE 4 – VIDEO DETECTOR OUTPUT RESISTANCE



**DESIGN CHARACTERISTICS** ($V_{CC}$ = +20 Vdc, Q = 40, $f_c$ = 45.75 MHz, $T_A$ = +25°C unless otherwise noted)

| Characteristic | Pin | Typ | Unit |
|---|---|---|---|
| Input Resistance | 7 | 4.9 | kΩ |
| Input Capacitance | 7 | 1.5 | pF |
| Internal Resistance (Across Tuned Circuit) | 2, 3 | 4.4 | kΩ |
| Internal Capacitance (Across Tuned Circuit) | 2, 3 | 1.0 | pF |
| Negative Video Output Bandwidth (Figure 10) | 4 | 10.8 | MHz |
| Positive Video Output Bandwidth (Figure 10) | 5 | 2.2 | MHz |
| Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6 | 4 | 7.0 | Degrees |
| Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6 | 4 | 4.0 | % |
| Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ | 4 | 8.0 | Degrees |
| Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ | 4 | 6.0 | % |
| 920 kHz Beat Output (dB Below 100% Modulated Video, See Figure 11)<br>45.75 MHz = Reference<br>42.17 MHz = - 6 dB<br>41.25 MHz = -20 dB | 4 | −38 | dB |
| Video Output Resistance @ 1 MHz, 2 mA | 4 | 94 | Ω |
| Input Overload (Carrier Level at Input to Caused Detector Output, Pin 4, To Go Positive 0.1 Vdc From Ground.) $V_{CC}$ = 12 Vdc | 7 | 2.0 | Volts |
| $V_{CC}$ = 15 Vdc | | 2.6 | |
| $V_{CC}$ = 20 Vdc | | 3.6 | |
| $V_{CC}$ = 24 Vdc | | 4.6 | |
| Power Supply Voltage Range | 5 | 10 to 24 | Volts |

FIGURE 5 – DIFFERENTIAL PHASE AND GAIN TEST SET UP


MODULATION MONITOR TEKTRONIX 475 OSCILLOSCOPE
50
10 dB 50 Ω PAD
BALANCED MODULATOR ANZAC MD-141
IF
RF
LO
ADJUST FOR 0 TO 3 V PEAK AT OUTPUT OF VIDEO DEMODULATOR
10 dB 50 Ω VARIABLE PAD
4.4 mV INTO LOAD BOONTON 91D
50
BIAS "T"
6.8 k
50
100mV INTO LOAD BOONTON 91D
2nd & 3rd HARMONIC TRAP
WIDEBAND AMPLIFIER H.P. 8447F $A_V$ ≈ 26 dB
75 Ω TO 50 Ω ≈ 6.7 dB
MODULATION ADJUSTMENT ≈ −11V FOR 100%
6 dB 50 Ω PAD
VIDEO DEMODULATOR TEST FIXTURE $R_{Load}$ ≈ 3 k TYP.
30 dB 75 Ω VARIABLE PAD
45.75 MHz GENERATOR H.P. 608E
LOW CAPACITANCE RESISTOR PROBE DIVIDER H.P. 10020A
SIX STEP MODULATED STAIRCASE GENERATOR TEKTRONIX 144 NTSC
SUBCARRIER
VECTOR SCOPE TEKTRONIX 520 NTSC
VECTOR SCOPE PREAMPLIFIER

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +20 Vdc, $T_A$ = +25°C Unless Otherwise Noted)

FIGURE 6 – OUTPUT VOLTAGE TRANSFER FUNCTION

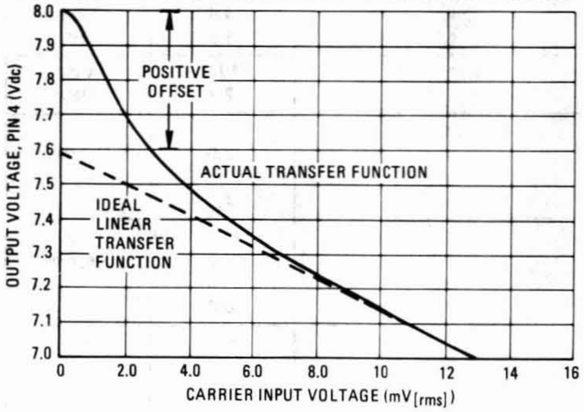


FIGURE 7 – OUTPUT VOLTAGE TRANSFER FUNCTION

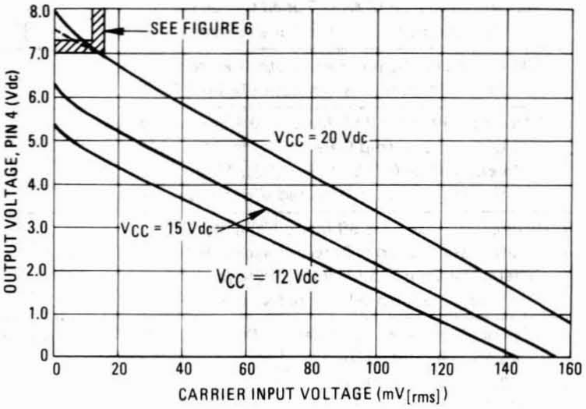


FIGURE 8 – OUTPUT VOLTAGE, SUPPLY CURRENT

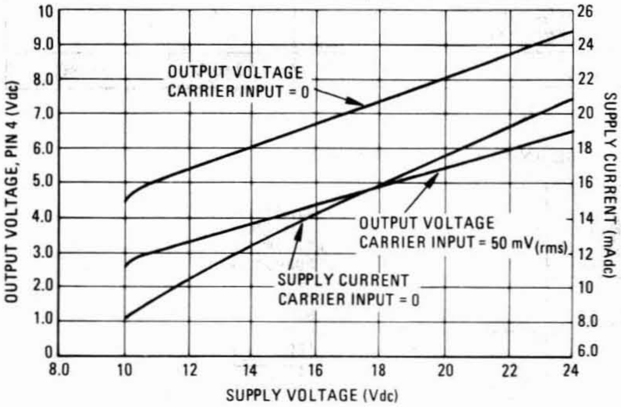


FIGURE 9 – AFT LIMITING

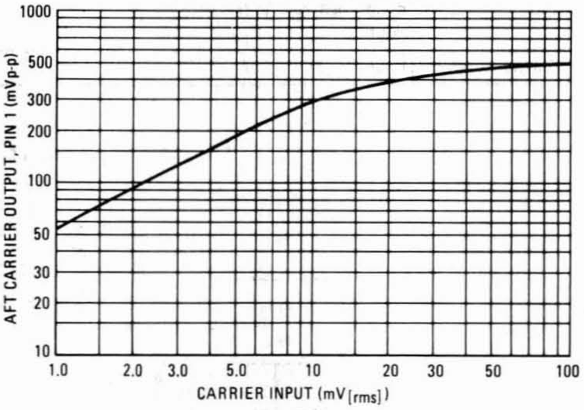


FIGURE 10 – VIDEO OUTPUT RESPONSE

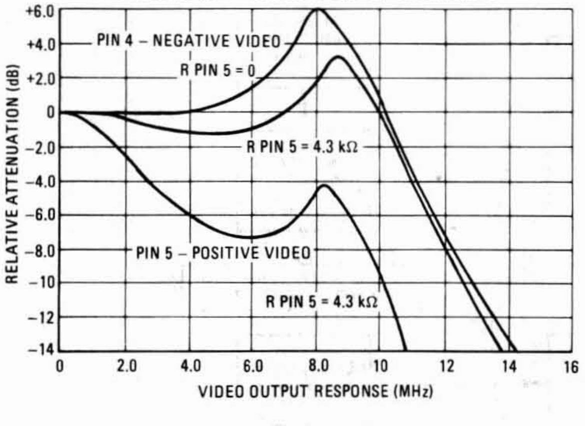
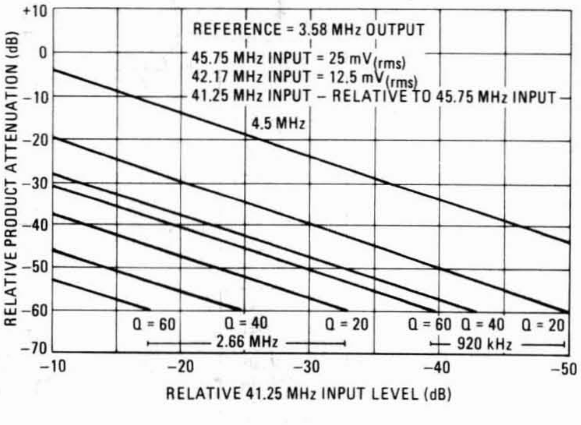


FIGURE 11 – VIDEO OUTPUT PRODUCTS



### TV-IF Amplifier Information

A very compact high performance IF amplifier constructed as shown in Figure 14 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 93 dB voltage gain and can accomodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1349P input.

The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3 volt peak-to-peak output can be varied from 0 to 7.0 V with excellent linearity and freedom from spurious output products.

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate to low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input), next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3 dB greater than the sweep amplitude. See Figures 12 and 13 below. For a more detailed description of the MC1330AP see application note AN-545.

### MC1330A General Information

The MC1330A offers the designer a new approach to an old problem. Now linear detection can be performed at much lower power signal levels than possible with a detector diode.

Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some specific features and information on systems design with this device are given below:

1. The device provides excellent linearity of output versus input, as shown in Figures 6 and 7. These graphs also show that video peak-to-peak amplitude (ac) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)
2. The dc output level does change linearly with supply voltage shown in Figure 8. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.
3. The choice of Q for the tuned circuit of pins 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products but the more critical the tuning accuracy required. See Figure 11. Values of Q from 20 to 50 are recommended. (Note the internal resistance.)
4. A video output with positive-going sync is available at pin 5 if required. This signal has a higher output impedance than pin 4 so it must be handled with greater care. If not used, pin 5 may be connected directly to the supply voltage (pin 6).The video response will be altered somewhat. See Figure 10.
5. An AFT output (pin1) provides 460 mV of IF carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.
6. AGC lockout can occur if the input signal presented in the MC1330A is greater than that shown in the input overload section of the design characteristics shown on Page 3. If these values are exceeded, the turns ratio between the primary and secondary of $T_1$ should be increased. Another solution to the problem is to use an input clamp diode $D_1$ shown in Figure 14.
7. The total I.F. noise figure at high gain reductions can be improved by reflecting ≈ 1 k source impedance to the input of the MC1330AP. This will cause some loss in overall IF voltage gain.

**FIGURE 12 — BANDPASS DISPLAYED BY CONVENTIONAL SWEEP**

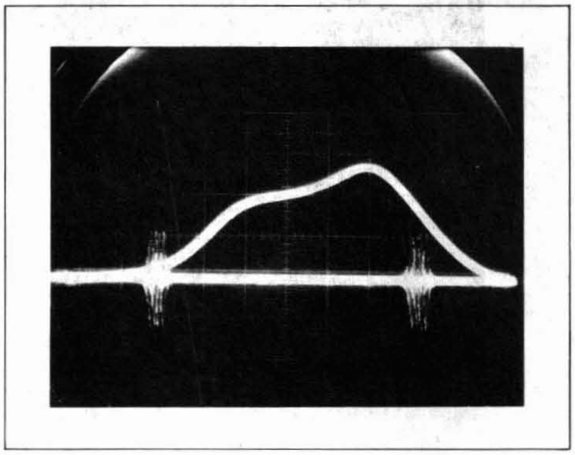


**FIGURE 13 — BANDPASS DISPLAY WITH THE ADDITION OF CARRIER INJECTION**

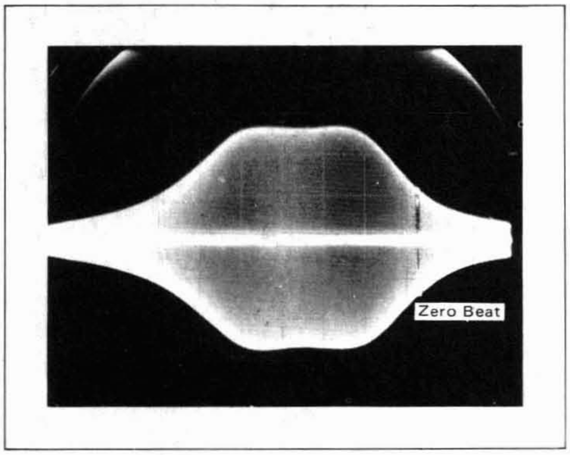
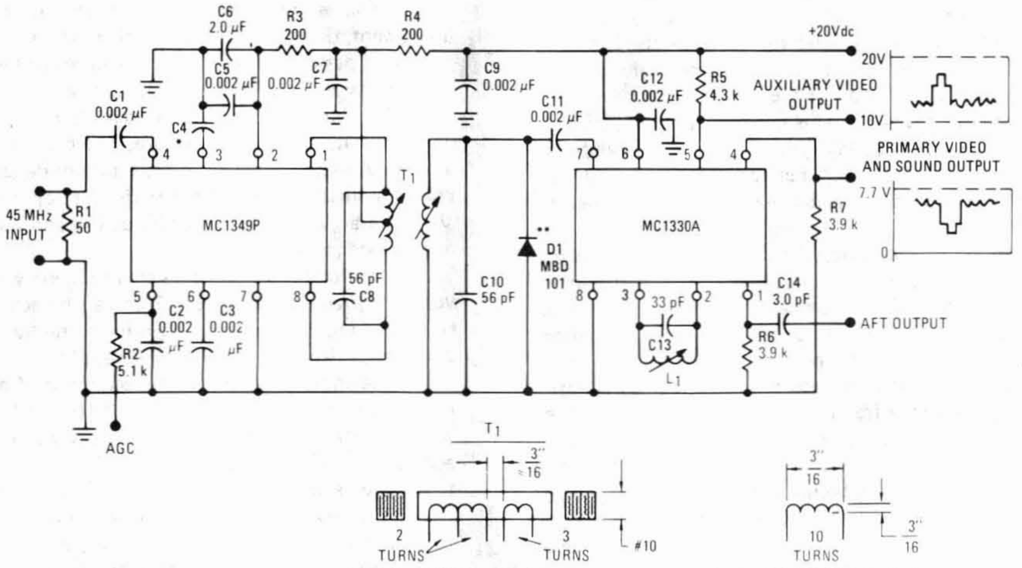


**FIGURE 14 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER and MC1330A LOW-LEVEL VIDEO DETECTOR CIRCUIT**


C6
2.0 μF
R3
200
R4
200
+20Vdc
C5
0.002 μF
C7
0.002 μF
C9
0.002 μF
C1
0.002 μF
C4
C11
0.002 μF
C12
0.002 μF
R5
4.3 k
AUXILIARY VIDEO OUTPUT
20V
10V
PRIMARY VIDEO AND SOUND OUTPUT
7.7 V
0
45 MHz INPUT
R1
50
MC1349P
T1
D1
MBD
101
MC1330A
R7
3.9 k
56 pF
C8
C10
56 pF
C2
0.002 μF
C3
0.002 μF
R2
5.1 k
33 pF
C13
L1
C14
3.0 pF
AFT OUTPUT
R6
3.9 k
AGC
T1
3"/16
2 TURNS
3 TURNS
#10
3"/16
10 TURNS
3"/16

All windings 22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10-32, or equivalent

L1 wound with 26 AWG tinned nylon acetate wire tuned by distorting winding.

*See Note 1 (page 3), and C4, Parts List (page 4) for this specification on the MC1349P Data Sheet.

**See Input Overload Section of the Design Characteristics Page 3, and General Information, Page 5, Note 6.

**FIGURE 15 – PRINTED CIRCUIT BOARD PARTS LAYOUT**

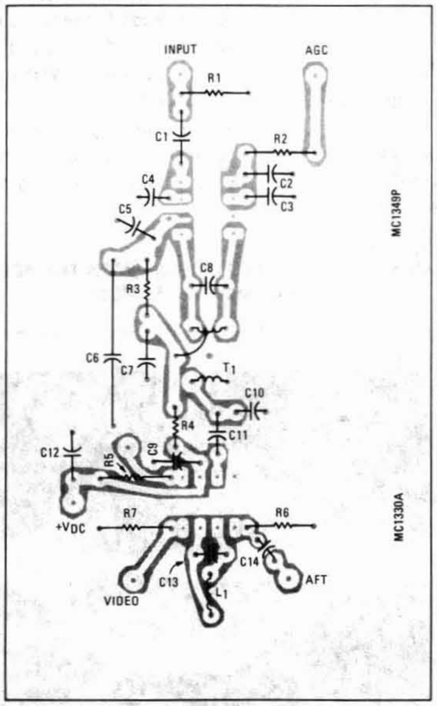
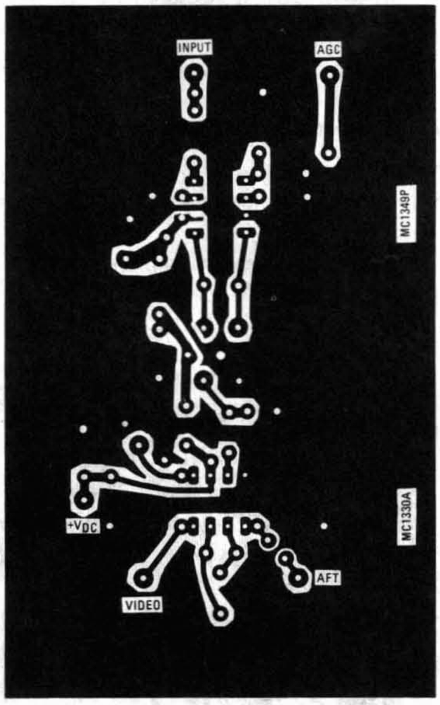

INPUT
AGC
R1
C1
R2
C4
C2
C3
C5
C8
R3
C6
C7
T1
C10
R4
C11
C12
C9
R5
R7
R6
+VDC
C14
C13
AFT
VIDEO
L1
MC1349P
COPPER SIDE UP
MC1330A

**FIGURE 16 – PRINTED CIRCUIT BOARD LAYOUT**


INPUT
AGC
MC1349P
COPPER SIDE UP
+VDC
MC1330A
AFT
VIDEO

**MOTOROLA**

# MC1349P

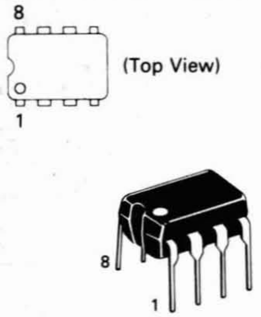
## MONOLITHIC IF AMPLIFIER

. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and television applications over the temperature range 0 to +70°C.

- Power Gain — 60 dB typ at 45 MHz (pin 3 open)
  - — 56 dB typ at 58 MHz (pin 3 open)
  - — 61 dB typ at 45 MHz (pin 3 bypassed)
  - — 59 dB typ at 58 MHz (pin 3 bypassed)
- AGC Range — 80 dB typ, dc to 45 MHz
- High Output Impedance
- Low Reverse Transfer Admittance
- 15-Volt Operation, Single-Polarity Power Supply
- Improved Noise Figure versus AGC

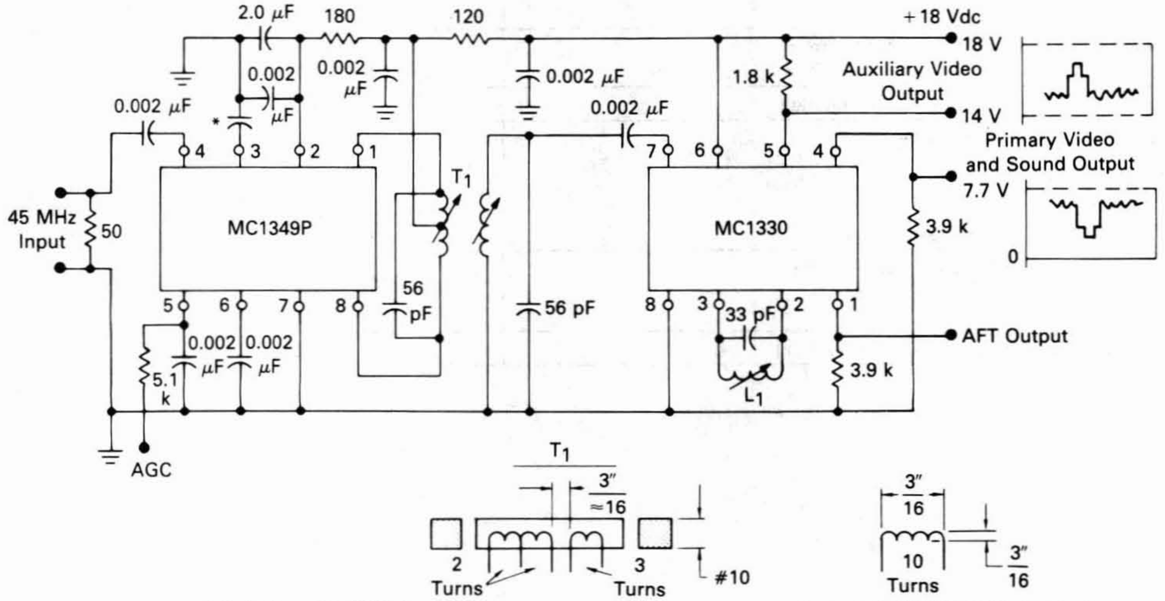
## IF AMPLIFIER

**MONOLITHIC SILICON**
**INTEGRATED CIRCUIT**


8
(Top View)
1
8
1

**N SUFFIX**
PLASTIC PACKAGE
CASE 626-04

**FIGURE 1 — TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER AND MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT**


2.0 μF
180
120
+18 Vdc
18 V
0.002
0.002 μF
0.002 μF
1.8 k
Auxiliary Video Output
0.002 μF
μF
*
0.002 μF
14 V
4
3
2
1
7
6
5
4
Primary Video and Sound Output
T1
7.7 V
45 MHz Input
50
MC1349P
MC1330
3.9 k
0
5
6
7
8
56 pF
56 pF
8
3
33 pF
2
1
AFT Output
0.002 μF
0.002 μF
5.1 k
L1
3.9 k
AGC
T1
3″
≈16
2 Turns
3 Turns
#10
3″
16
10 Turns
3″
16

All windings #22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10-32, or equivalent.

L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

*See Note 1 (page 3), and C4, Parts List (page 4) of this specification.

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted).

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage ($V_{CC1}$) | +18 | Vdc |
| Output Supply Voltage ($V_{CC2}$) | +18 | Vdc |
| AGC Supply Voltage | ≤ $V_{CC1}$ (pin 2) | Vdc |
| Differential Input Voltage | 5.0 | Vdc |
| Power Dissipation (Package Limitation) | | |
| Plastic Package | 625 | mW |
| Derate above $T_A$ = +25°C | 5.0 | mW/°C |
| Operating Temperature Range | 0 to +70 | °C |
| Storage Temperature Range | −65 to +150 | °C |

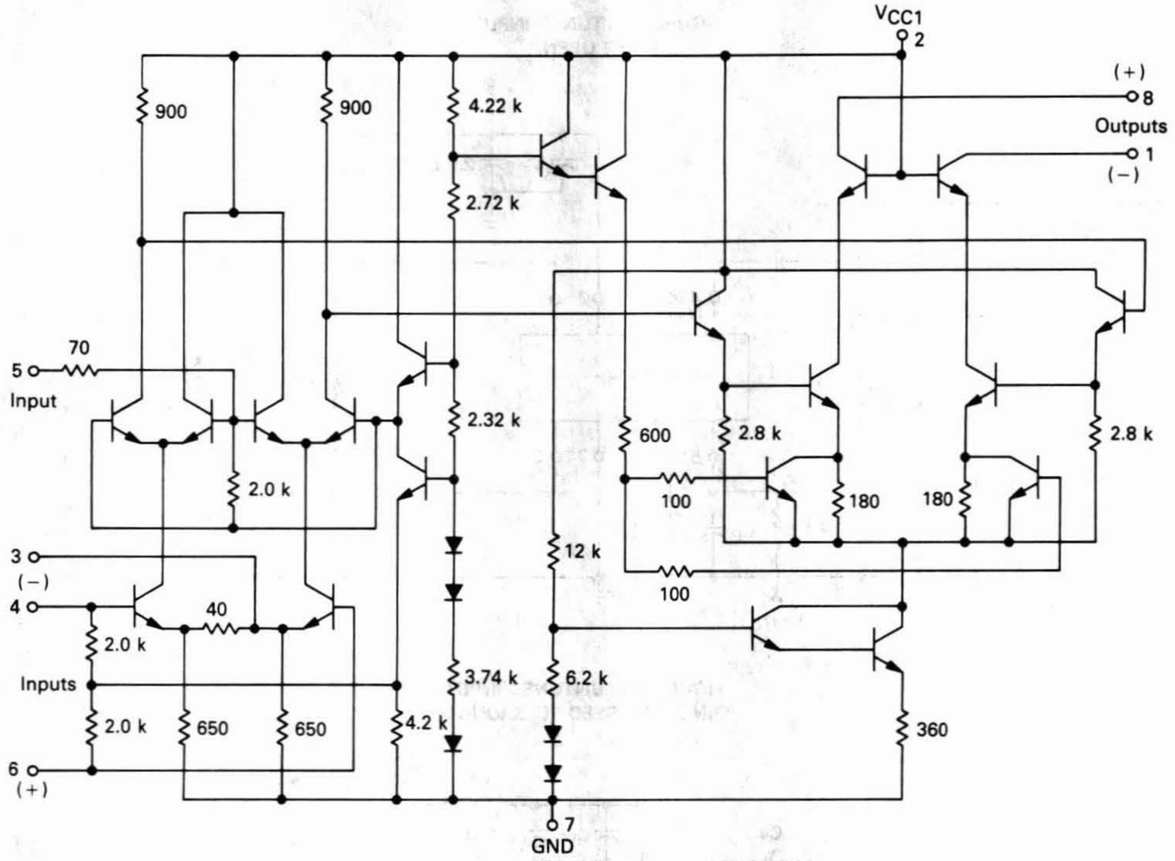
**ELECTRICAL CHARACTERISTICS** ($V_{CC1}$ = +12 Vdc [pin 2], $V_{CC2}$ = +15 Vdc [pins 1 and 8], $T_A$ = +25°C unless otherwise noted.)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| AGC Range, 45 MHz (Figure 3) | 70 | 80 | — | dB |
| Power Gain (Pin 5 grounded via 5.1 kΩ resistor, input pin 4) | | | | dB |
| f = 45 MHz, BW (3 dB) = 4.5 MHz, Tuned Input, pin 3 open | 52 | 60 | — | |
| Untuned Input, pin 3 bypassed | — | 61 | — | |
| f = 58 MHz, BQ (3 dB) = 4.5 MHz, Tuned Input, pin 3 open | — | 56 | — | |
| Untuned Input, pin 3 bypassed | — | 59 | — | |
| Maximum Differential Output Voltage Swing | — | 6.0 | — | $V_{p-p}$ |
| Output Stage Current (pins 1 and 8) | — | 9.0 | — | mA |
| Amplifier Current (pin 2) | — | 15 | 20 | mAdc |
| Power Dissipation | — | 315 | 400 | mW |
| Noise Figure<br>f = 45 MHz, Tuned Input, pin 3 open, Gain Reduction = 15 dB | — | 8.5 | — | dB |

**DESIGN PARAMETERS** ($V_{CC1}$ = +12 Vdc, [pin 2], $V_{CC2}$ = +15 Vdc, [pins 1 and 8], $T_A$ = +25°C unless otherwise noted.)

| Parameter | Symbol | Frequency | | Unit |
|---|---|---|---|---|
| | | 45 MHz | 58 MHz | |
| Single-Ended Input Admittance, input pin 4, AGC min | | | | mmhos |
| Pin 3 open | g11 | 0.74 | 0.95 | |
| Pin 3 open | b11 | 1.9 | 2.4 | |
| Pin 3 bypassed | g11 | 4.1 | 5.4 | |
| Pin 3 bypassed | b11 | 6.5 | 6.9 | |
| Differential Output Admittance, AGC max | g22 | 5.5 | 8.3 | μmhos |
| | b22 | 270 | 360 | |
| Reverse Transfer Admittance (magnitude) | | 1.5 | 2.0 | μmhos |
| Forward Transfer Admittance | | | | |
| Magnitude, pin 3 open | | 520 | 400 | mmhos |
| Angle (0 dB AGC), pin 3 open | | 100 | 130 | degrees |
| Magnitude, pin 3 bypassed | | 1020 | 800 | mmhos |
| Angle (0 dB AGC), pin 3 bypassed | | 120 | 400 | degrees |
| Single-Ended Input Capacitance, AGC min | | | | pF |
| Pin 3 open | | 6.8 | 6.7 | |
| Pin 3 bypassed | | 2.3 | 20 | |
| Differential Output Capacitance (AGC max) | | 1.0 | 1.0 | pF |

FIGURE 2 — CIRCUIT SCHEMATIC



**GENERAL INFORMATION**

The MC1349P is an improved version of the MC1350P. Featuring higher gain, a lower noise figure, and greater AGC range; in addition, an emitter of the input amplifier is available for bypassing. This provides a low input impedance with good gain, useful for untuned input configurations.

Both input and output IF amplifier sections are gain-controlled in the MC1349P, with the input amplifier also serving as an AGC amplifier for the output section. During the initial part of AGC gain reduction, the gain of the input amplifier decreases only a few dB while the output section decreases 15 dB; further AGC acts upon the input section. Although the gain reduction curve was taken with 5.1 kilohms at pin 5, higher series resistance can be used to reduce the voltage and temperature sensitivity of the AGC. Pin 5 currents are shown on the AGC curve, see Figure 10.

In use, it is important to bypass pin 2, both for IF frequencies and for low frequencies, (as shown in the test circuits). This is due to the dual function of the input amplifier. If replacing MC1350P take precaution not to ground pin 3, (not used in the MC1350P). Due to the significantly higher gain of the MC1349P, extra care in layout should be exercised.

**NOTE 1:** The references to bypasses at pin 3 do not give specific values (C4, see Figures 1 and 4). In all cases, measurements were taken with a bypass at a standard value as near as possible to series resonance. The values are dependent on test frequency and circuit layout. Fully bypassing pin 3 reduces the input signal handling capability before distortion from over 100 mV(RMS) to approximately 25 mV(RMS). C4 = 0.002 μF at f = 45 MHz is a typical value for printed circuit applications.

## TEST CIRCUITS

FIGURE 3 — TUNED INPUT
(PIN 3 OPEN)

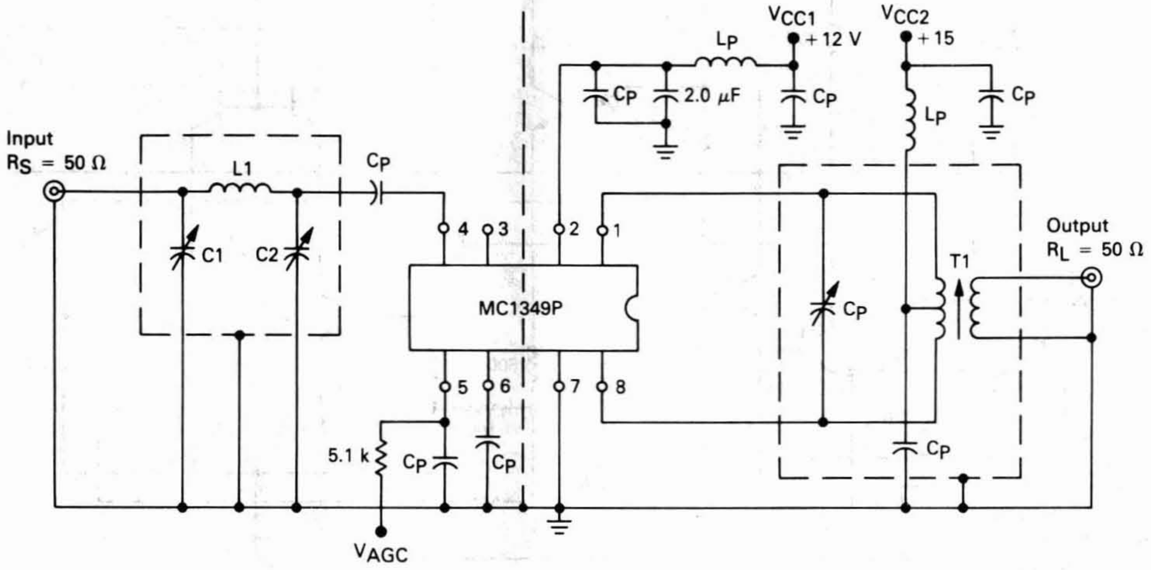
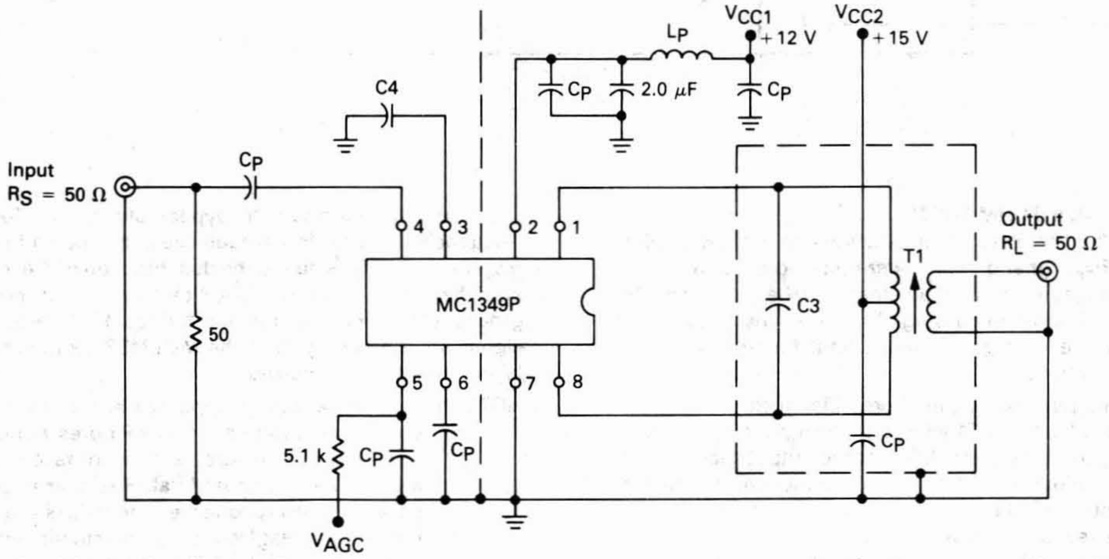

VCC1
VCC2
LP
+12 V
+15
CP
2.0 μF
CP
LP
CP
Input
RS = 50 Ω
L1
CP
C1
C2
4
3
2
1
MC1349P
CP
T1
Output
RL = 50 Ω
5
6
7
8
5.1 k
CP
CP
CP
VAGC

FIGURE 4 — UNTUNED INPUT
(PIN 3 BYPASSED TO GROUND)


VCC1
VCC2
LP
+12 V
+15 V
CP
2.0 μF
CP
C4
Input
RS = 50 Ω
CP
4
3
2
1
MC1349P
50
C3
T1
Output
RL = 50 Ω
5
6
7
8
5.1 k
CP
CP
CP
VAGC

**PARTS LIST**

| Component | 45 MHz | 58 MHz |
|---|---|---|
| C1 | 8–60 pF | 50–100 pF |
| C2 | 3–35 pF | 3–35 pF |
| C3 | 1–7.0 pF | 1–7.0 pF |
| C4 | 82–470 pF | 82–470 pF |
| $C_P$ | 0.0015 μF | 0.001 μF |
| L1 | 0.84 μH | 0.33 μH |
| $L_P$ | 10 μH | 10 μH |

| | | |
|---|---|---|
| T1 | Primary | 14 turns center-tapped |
| | Secondary | 2-1/2 turns (45 MHz tuned input pin #3 open) 1-1/2 turns (all other fixtures) wound over primary |
| | Wire: | #26 AWG tinned nylcon acetate wound on 1/4″ diameter coil form |
| | Core: | Carbonyl E or J, 1/2″ long or equivalent. |

## TYPICAL CHARACTERISTICS

FIGURE 5 — SINGLE-ENDED INPUT ADMITTANCE (PIN 3 OPEN)

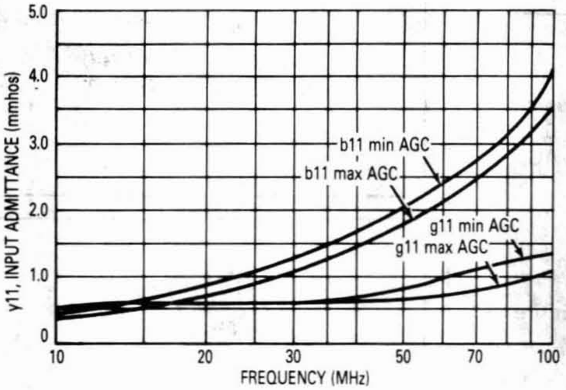


FIGURE 6 — SINGLE-ENDED INPUT ADMITTANCE (PIN 3 BYPASSED TO GROUND)

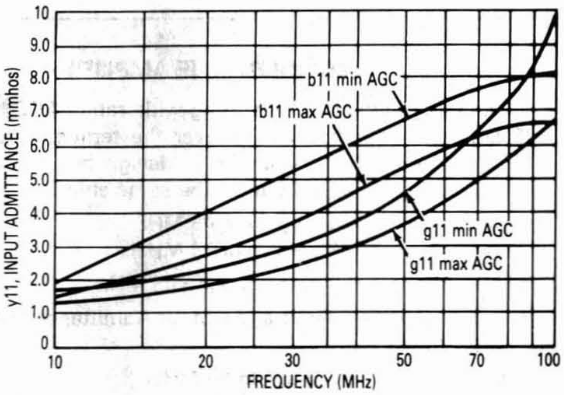


FIGURE 7 — SINGLE-ENDED FORWARD TRANSFER ADMITTANCE

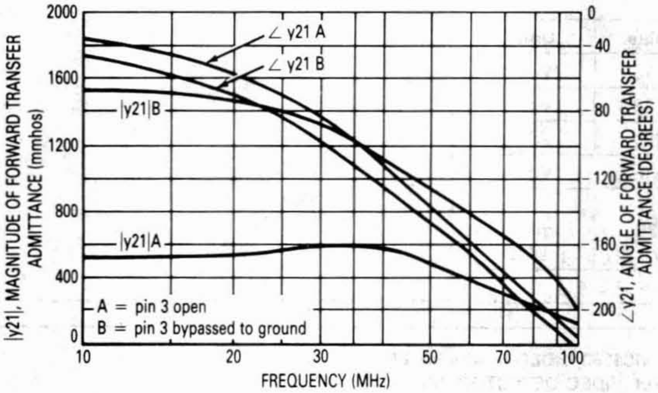


FIGURE 8 — DIFFERENTIAL OUTPUT ADMITTANCE (MAXIMUM AGC)

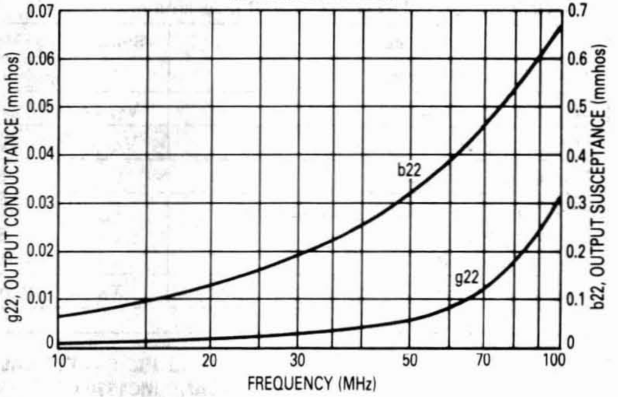


FIGURE 9 — NOISE FIGURE

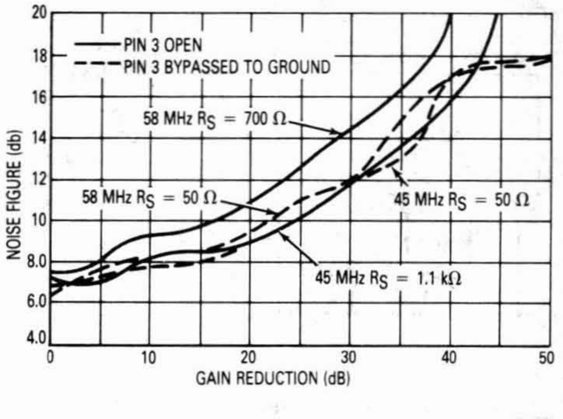
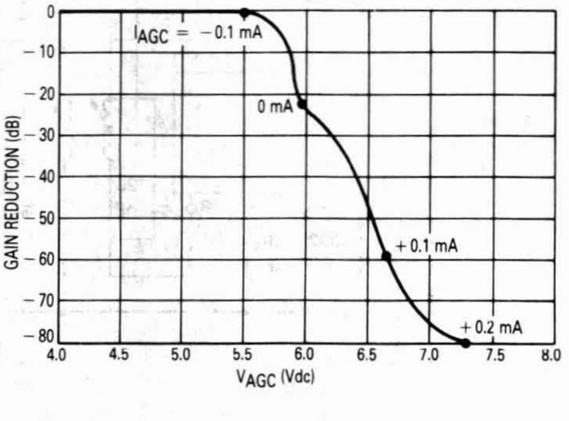


FIGURE 10 — GAIN REDUCTION

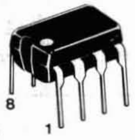


**MOTOROLA**

# MC1350P

## IF AMPLIFIER

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



**P1 SUFFIX**
PLASTIC
PACKAGE
CASE 626-04

**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SO-8

## MONOLITHIC IF AMPLIFIER

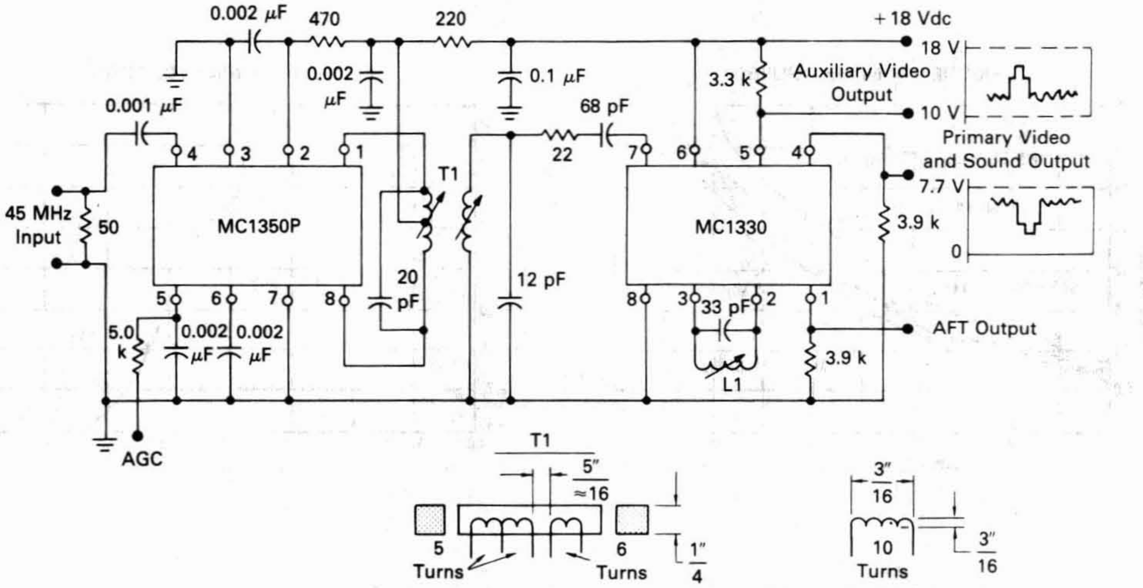
. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over the temperature range 0 to +75°C. The MC1352 is similar in design but has a keyed-AGC amplifier as an integral part of the same chip.

- Power Gain — 50 dB Typ at 45 MHz
  — 48 dB Typ at 58 MHz
- AGC Range — 60 dB Min, dc to 45 MHz
- Nearly Constant Input and Output Admittance Over the Entire AGC Range
- $y_{21}$ Constant (−3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance — << 1.0 μmho Typ
- 12-Volt Operation, Single-Polarity Power Supply

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V^+$ | +18 | Vdc |
| Output Supply Voltage | $V_1$, $V_8$ | +18 | Vdc |
| AGC Supply Voltage | $V_{AGC}$ | $V^+$ | Vdc |
| Differential Input Voltage | $V_{in}$ | 5.0 | Vdc |
| Power Dissipation (Package Limitation)<br>Plastic Package<br>Derate above 25°C | $P_D$ | <br>625<br>5.0 | <br>mW<br>mW/°C |
| Operating Temperature Range | $T_A$ | 0 to +75 | °C |

**FIGURE 1 — TYPICAL MC1350 VIDEO IF AMPLIFIER AND MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT**


0.002 μF
470
220
+18 Vdc
18 V
0.002 μF
0.1 μF
3.3 k
Auxiliary Video Output
10 V
0.001 μF
68 pF
22
Primary Video and Sound Output
T1
7.7 V
45 MHz Input
50
MC1350P
MC1330
3.9 k
0
20 pF
12 pF
33 pF
AFT Output
5.0 k
0.002 μF
0.002 μF
3.9 k
L1
AGC
T1
5″/16
≈16
5 Turns
6 Turns
1″/4
3″/16
10 Turns
3″/16

All windings #30 AWG tinned nylon acetate wire tuned with Carbonyl E or J slugs.

L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

**ELECTRICAL CHARACTERISTICS** ($V^+ = +12$ Vdc; $T_A = +25°C$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1) | | 60 | 68 | — | dB |
| Power Gain (Pin 5 grounded via a 5.1 kΩ resistor)<br>f = 58 MHz, BW = 4.5 MHz See Figure 6(a)<br>f = 45 MHz, BW = 4.5 MHz See Figure 6(a),(b)<br>f = 10.7 MHz, BW = 350 kHz See Figure 7<br>f = 455 kHz, BW = 20 kHz | $A_p$ | <br>—<br>46<br>—<br>— | <br>48<br>50<br>58<br>62 | <br>—<br>—<br>—<br>— | dB |
| Maximum Differential Voltage Swing<br>0 dB AGC<br>−30 dB AGC | $V_o$ | <br>—<br>— | <br>20<br>8.0 | <br>—<br>— | $V_{p-p}$ |
| Output Stage Current (Pins 1 and 8) | $I_1 + I_8$ | — | 5.6 | — | mA |
| Total Supply Current (Pins 1, 2 and 8) | $I_S$ | — | 14 | 17 | mAdc |
| Power Dissipation | $P_D$ | — | 168 | 204 | mW |

**DESIGN PARAMETERS,** Typical Values ($V^+ = +12$ Vdc, $T_A = +25°C$ unless otherwise noted)

| Parameter | Symbol | Frequency | | | | Unit |
|---|---|---|---|---|---|---|
| | | 455 kHz | 10.7 MHz | 45 MHz | 58 MHz | |
| Single-Ended Input Admittance | $g_{11}$<br>$b_{11}$ | 0.31<br>0.022 | 0.36<br>0.50 | 0.39<br>2.30 | 0.5<br>2.75 | mmhos |
| Input Admittance Variations with AGC (0 to 60 dB) | $\Delta g_{11}$<br>$\Delta b_{11}$ | —<br>— | —<br>— | 60<br>0 | —<br>— | μmhos |
| Differential Output Admittance | $g_{22}$<br>$b_{22}$ | 4.0<br>3.0 | 4.4<br>110 | 30<br>390 | 60<br>510 | μmhos |
| Output Admittance Variations with AGC (0 to 60 dB) | $\Delta g_{22}$<br>$\Delta b_{22}$ | —<br>— | —<br>— | 4.0<br>90 | —<br>— | μmhos |
| Reverse Transfer Admittance (Magnitude) | $\|y_{12}\|$ | <<1.0 | <<1.0 | <<1.0 | <<1.0 | μmho |
| Forward Transfer Admittance<br>Magnitude<br>Angle (0 dB AGC)<br>Angle (−30 dB AGC) | <br>$\|y_{21}\|$<br>$< y_{21}$<br>$< y_{21}$ | <br>160<br>−5.0<br>−3.0 | <br>160<br>−20<br>−18 | <br>200<br>−80<br>−69 | <br>180<br>−105<br>−90 | <br>mmhos<br>degrees<br>degrees |
| Single-Ended Input Capacitance | $C_{in}$ | 7.2 | 7.2 | 7.4 | 7.6 | pF |
| Differential Output Capacitance | $C_o$ | 1.2 | 1.2 | 1.3 | 1.6 | pF |

**FIGURE 2 — TYPICAL GAIN REDUCTION**
(Figures 6 and 7)

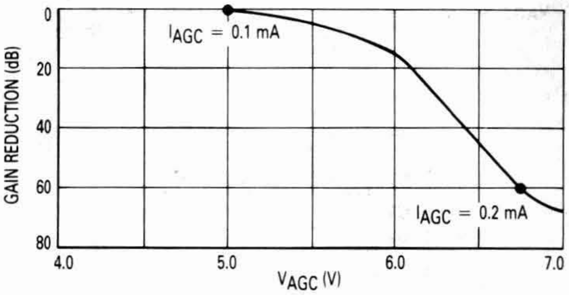
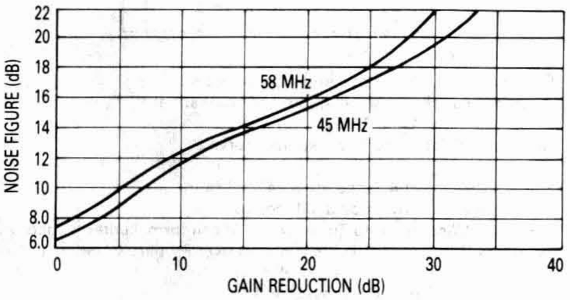


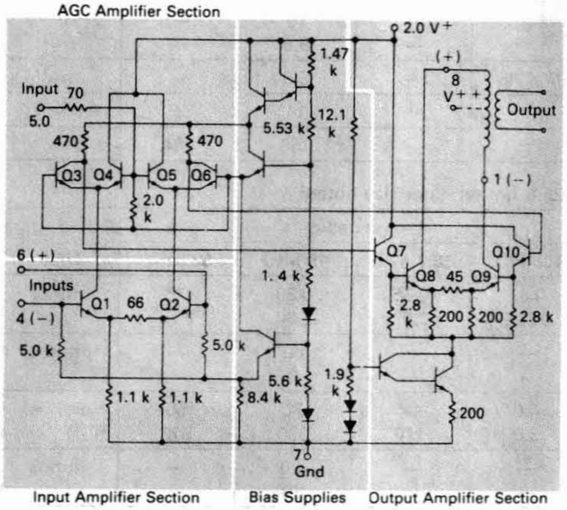
**FIGURE 3 — NOISE FIGURE**
(Figure 6)



## GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

FIGURE 4 — CIRCUIT SCHEMATIC


AGC Amplifier Section
2.0 V+
1.47 k
(+)
8
V++
Output
Input 70
5.0
470
470
5.53 k
12.1 k
Q3
Q4
Q5
Q6
1 (−)
2.0 k
6 (+)
Inputs
4 (−)
Q1
66
Q2
1.4 k
Q7
Q10
Q8
45
Q9
2.8 k
200
200
2.8 k
5.0 k
5.0 k
5.6 k
1.9 k
8.4 k
1.1 k
1.1 k
200
7
Gnd
Input Amplifier Section
Bias Supplies
Output Amplifier Section

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V++) is used, because the base voltage on the output amplifier varies with AGC bias.

FIGURE 5 — TEST CIRCUIT RESPONSE CURVE
(45 and 58 MHz)

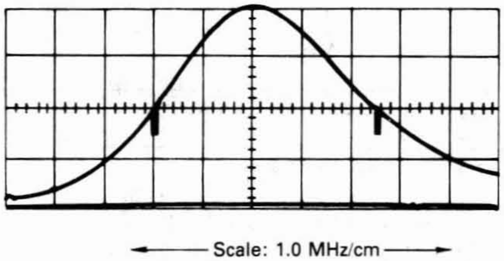
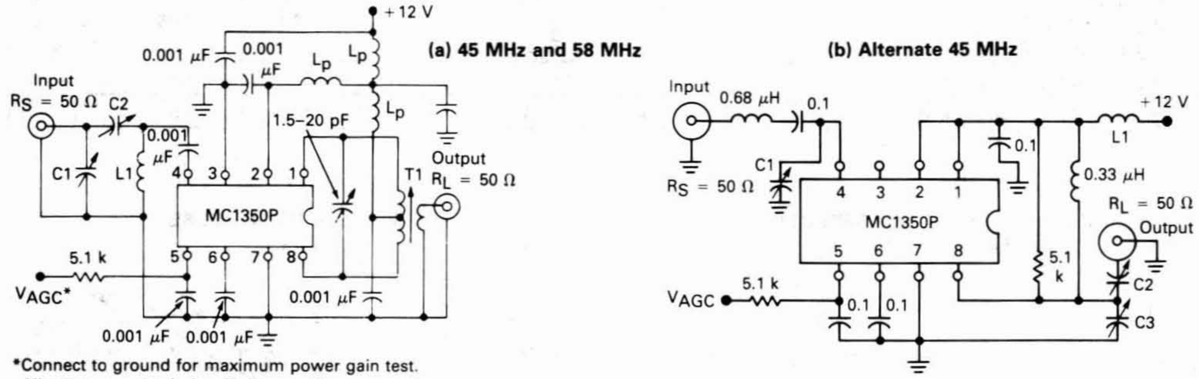


FIGURE 6 — POWER GAIN, AGC AND NOISE FIGURE TEST CIRCUITS


(a) 45 MHz and 58 MHz

(b) Alternate 45 MHz

+12 V
0.001 μF
0.001 μF
Lp
Lp
Input
RS = 50 Ω
C2
C1
L1
0.001 μF
1.5–20 pF
Lp
Output
T1
RL = 50 Ω
4
3
2
1
MC1350P
5
6
7
8
5.1 k
VAGC*
0.001 μF
0.001 μF
0.001 μF
Input
0.68 μH
0.1
+12 V
L1
0.1
C1
RS = 50 Ω
0.33 μH
RL = 50 Ω
Output
MC1350P
5.1 k
VAGC
0.1
0.1
5.1 k
C2
C3

*Connect to ground for maximum power gain test.
All power-supply chokes ($L_p$), are self-resonant at input frequency. $L_p \geq 20$ kΩ
See Figure 5 for frequency response curve.

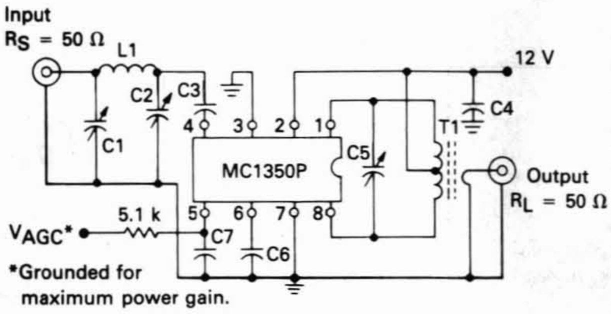
L1 @ 45 MHz = 7 1/4 Turns on a 1/4″ coil form.
@ 58 MHz = 6 Turns on a 1/4″ coil form
T1 Primary Winding = 18 Turns on a 1/4″ coil form, center-tapped, #26 AWG
Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
= 1 Turn @ 58 MHz
Slug = Carbonyl E or J

| L1 | Ferrite Core<br>14 Turns 28 S.W.G |
|---|---|
| C1 | 5–25 pF |
| C2 | 5–25 pF |
| C3 | 5–25 pF |

| | 45 MHz | | 58 MHz | |
|---|---|---|---|---|
| L1 | 0.4 μH | Q ≥ 100 | 0.3 μH | Q ≥ 100 |
| T1 | 1.3–3.4 μH | Q ≥ 100 @ 2.0 μH | 1.2–3.8 μH | Q ≥ 100 @ 2.0 μH |
| C1 | 50–160 pF | | 8–60 pF | |
| C2 | 8–60 pF | | 3–35 pF | |

## GENERAL OPERATING INFORMATION (continued)

FIGURE 7 — POWER GAIN AND AGC TEST CIRCUIT
(455 kHz and 10.7 MHz)



*Grounded for maximum power gain.

| Component | Frequency 455 kHz | Frequency 10.7 MHz |
|---|---|---|
| C1 | — | 80–450 pF |
| C2 | — | 5.0–80 pF |
| C3 | 0.05 μF | 0.001 μF |
| C4 | 0.05 μF | 0.05 μF |
| C5 | 0.001 μF | 36 pF |
| C6 | 0.05 μF | 0.05 μF |
| C7 | 0.05 μF | 0.05 μF |
| L1 | — | 4.6 μH |
| T1 | Note 1 | Note 2 |

Note 1. Primary: 120 μH (center-tapped)
$Q_u$ = 140 at 455 kHz
Primary: Secondary turns ratio ≈ 13

Note 2. Primary: 6.0 μH
Primary winding = 24 turns #36 AWG
(close-wound on 1/4" dia. form)
Core = Carbonyl E or J
Secondary winding = 1-1/2 turns #36 AWG, 1/4" dia.
(wound over center-tap)

## TYPICAL CHARACTERISTICS
($V^+$ = 12 V, $T_A$ = +25°C)

FIGURE 8 — SINGLE-ENDED INPUT ADMITTANCE

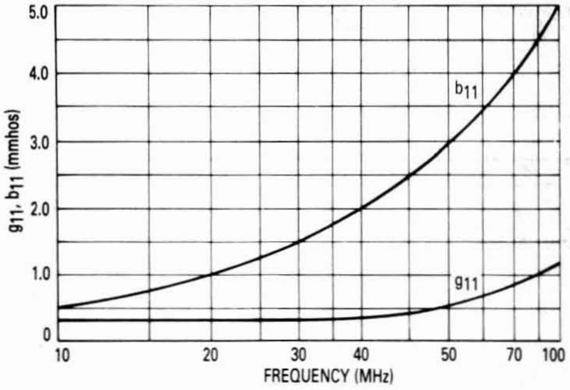


FIGURE 9 — FORWARD TRANSFER ADMITTANCE

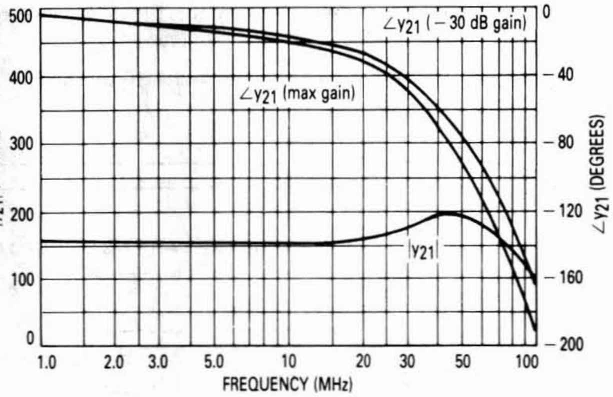


FIGURE 10 — DIFFERENTIAL OUTPUT ADMITTANCE

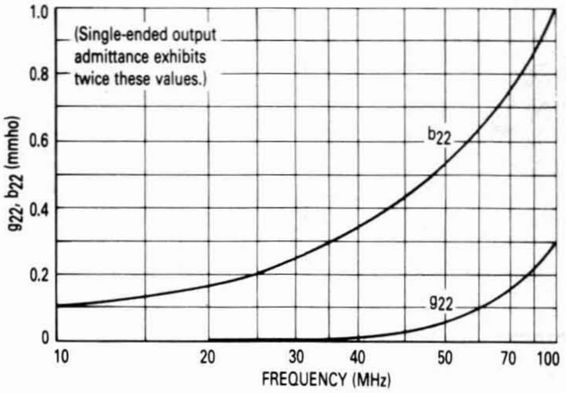
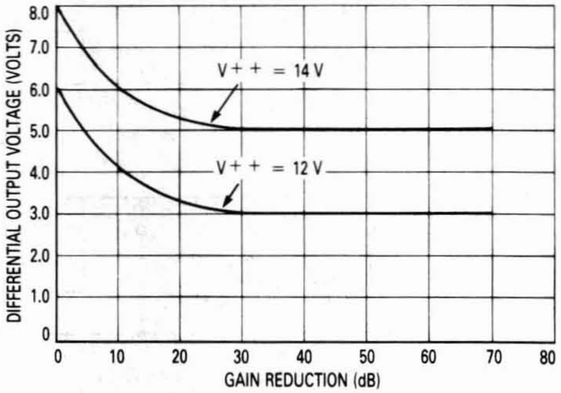


FIGURE 11 — DIFFERENTIAL OUTPUT VOLTAGE



For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control," by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC1352P | 0°C to +70°C | Plastic DIP |

# MC1352

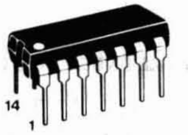
## TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

. . . a monolithic IF amplifier with a complete gated wide-range AGC system for use as the 1st and 2nd IF stages and AGC keyer and amplifier in color or monochrome TV receivers.

- Power Gain at 45 MHz, 52 dB typ
- Extremely Low Reverse-Transfer Admittance – << 1.0 μmho typ
- Nearly Constant Input and Output Admittance Over AGC Range
- Single-Polarity Power-Supply Operation
- High-Gain Gated AGC System for Either Positive or Negative-Going Video Signals
- Control Signal Available for Delayed AGC of Tuner

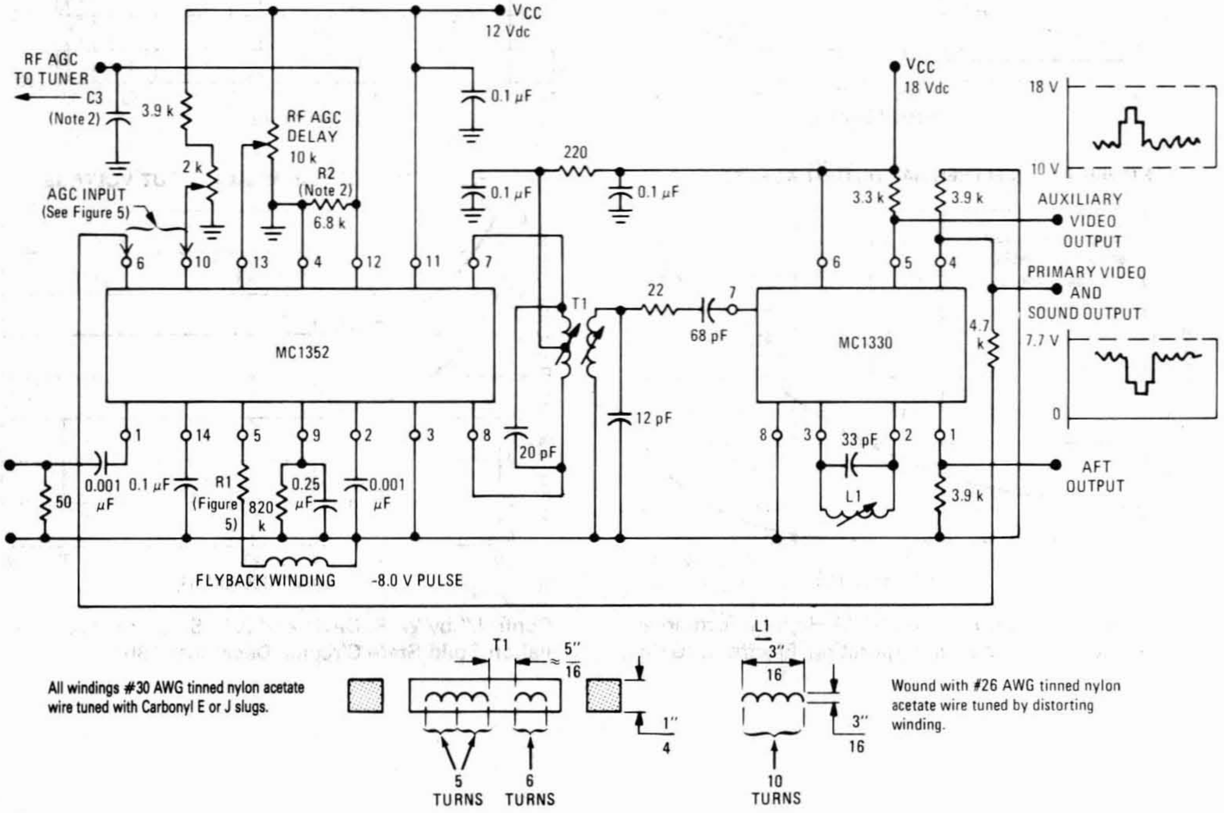
### TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

FIGURE 1 – TYPICAL VIDEO IF AMPLIFIER APPLICATION


VCC
12 Vdc
RF AGC
TO TUNER
C3
(Note 2)
3.9 k
RF AGC
DELAY
10 k
R2
(Note 2)
6.8 k
2 k
AGC INPUT
(See Figure 5)
0.1 μF
220
0.1 μF
0.1 μF
6
10
13
4
12
11
7
MC1352
1
14
5
9
2
3
8
0.001 μF
0.1 μF
R1
(Figure 5)
820 k
0.25 μF
0.001 μF
50
20 pF
FLYBACK WINDING
-8.0 V PULSE
T1
22
7
68 pF
12 pF
VCC
18 Vdc
3.3 k
3.9 k
6
5
4
MC1330
4.7 k
8
3
33 pF
2
1
L1
3.9 k
18 V
10 V
AUXILIARY
VIDEO
OUTPUT
PRIMARY VIDEO
AND
SOUND OUTPUT
7.7 V
0
AFT
OUTPUT
T1
5"/16
1"/4
5
TURNS
6
TURNS
L1
3"/16
3"/16
10
TURNS

All windings #30 AWG tinned nylon acetate wire tuned with Carbonyl E or J slugs.

Wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

**MAXIMUM RATINGS** (Voltages referenced to Pin 4, ground; $T_A$ = +25°C unless otherwise noted)

| Rating | Value | Unit |
|---|---|---|
| Power Supply (Pin 11) | +18 | Vdc |
| Output Supply (Pins 7 and 8) | +18 | Vdc |
| Signal Input Voltage (Pin 1 or 2, other pin ac grounded) | 10 | $V_{p-p}$ |
| AGC Input Voltage (Pin 6 or 10, other pin ac grounded) | +6.0 | Vdc |
| Gating Voltage, Pin 5 | +10, -20 | Vdc |
| Power Dissipation<br>Derate above $T_A$ = +25°C | 625<br>5.0 | mW<br>mW/°C |
| Operating Temperature Range | 0 to +70 | °C |
| Storage Temperature Range | -55 to +150 | °C |

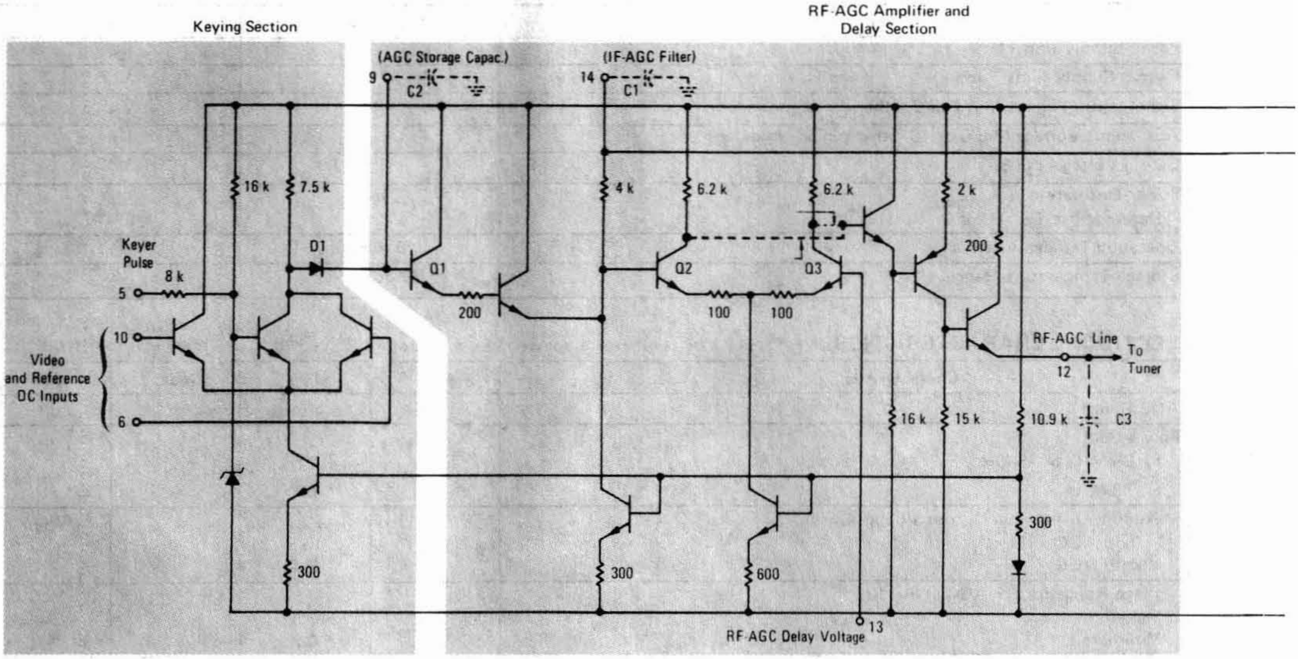
**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +12 Vdc, Voltages referenced to pin 4, ground; $T_A$ = +25°C unless otherwise noted.)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| AGC Range | – | 75 | – | dB |
| Power Gain | | | | dB |
| f = 35 MHz or 45 MHz | – | 52 | – | |
| f = 58 MHz | – | 50 | – | |
| Maximum Differential Output Voltage Swing | | | | $V_{p-p}$ |
| 0 dB AGC | – | 16.8 | – | |
| -30 dB AGC | – | 8.4 | – | |
| Voltage Range for RF-AGC at Pin 12 | | | | Vdc |
| Maximum | – | 7.0 | – | |
| Minimum | – | 0.2 | – | |
| IF Gain Change Over RF-AGC Range | – | 10 | – | dB |
| Output Stage Current ($I_7 + I_8$) | – | 5.7 | – | mAdc |
| Total Supply Current ($I_7 + I_8 + I_{11}$) | – | 27 | 35 | mAdc |

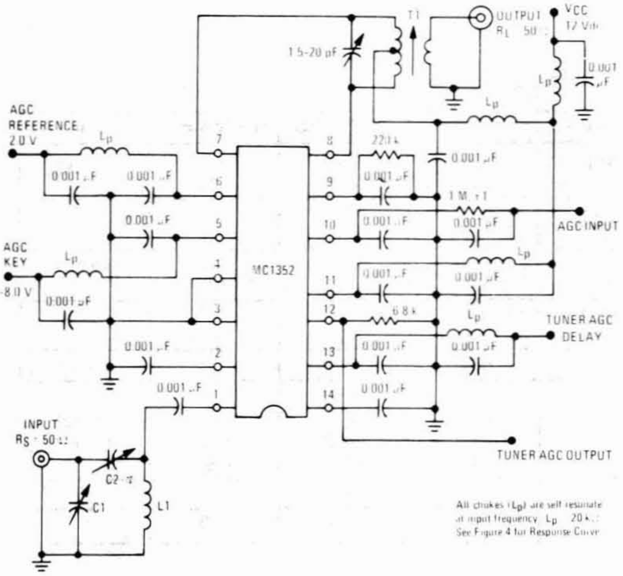
**DESIGN PARAMETERS, TYPICAL VALUES** ($V_{CC}$ = 12 Vdc, $T_A$ = +25°C unless otherwise noted.)

| Parameters | Symbol | f = 35 MHz | f = 45 MHz | f = 58 MHz | Unit |
|---|---|---|---|---|---|
| Single-Ended Input Admittance | $g_{11}$<br>$b_{11}$ | 0.55<br>2.25 | 0.70<br>2.80 | 1.1<br>3.75 | mmhos |
| Input Admittance Variations with AGC (0 to 60 dB) | $\Delta g_{11}$<br>$\Delta b_{11}$ | 50<br>0 | 60<br>0 | –<br>– | µmhos |
| Differential Output Admittance | $g_{22}$<br>$b_{22}$ | 20<br>430 | 40<br>570 | 75<br>780 | µmhos |
| Output Admittance Variations with AGC (0 to 60 dB) | $\Delta g_{22}$<br>$\Delta b_{22}$ | 3.0<br>80 | 4.0<br>100 | –<br>– | µmhos |
| Reverse Transfer Admittance | $\lvert y_{12} \rvert$ | $\ll 1.0$ | $\ll 1.0$ | $\ll 1.0$ | µmho |
| Forward Transfer Admittance | | | | | |
| Magnitude | $\lvert y_{12} \rvert$ | 260 | 240 | 210 | mmhos |
| Angle (0 dB AGC) | $\angle y_{21}$ | -73 | -100 | -135 | degrees |
| Angle (-30 dB AGC) | $\angle y_{21}$ | -52 | -72 | -96 | |
| Single-Ended Input Capacitance | – | 9.5 | 10 | 10.5 | pF |
| Differential Output Capacitance | – | 2.0 | 2.0 | 2.5 | pF |

### FIGURE 2 – CIRCUIT SCHEMATIC
KEYER AND AGC AMPLIFIER


Keying Section
RF-AGC Amplifier and Delay Section
(AGC Storage Capac.)
9
C2
(IF-AGC Filter)
14
C1
16 k
7.5 k
4 k
6.2 k
6.2 k
2 k
Keyer Pulse
8 k
5
D1
Q1
200
Q2
100
100
Q3
200
10
Video and Reference DC Inputs
6
RF-AGC Line
12
To Tuner
16 k
15 k
10.9 k
C3
300
300
300
600
300
RF-AGC Delay Voltage
13

### FIGURE 3 – POWER GAIN, AGC AND NOISE TEST CIRCUIT


T1
OUTPUT
$R_L$ 50 Ω
VCC
12 Vdc
1.5-20 pF
$L_p$
0.001 µF
AGC REFERENCE
2.0 V
$L_p$
0.001 µF
0.001 µF
0.001 µF
AGC KEY
8.0 V
$L_p$
0.001 µF
0.001 µF
0.001 µF
7
6
5
4
3
2
1
8
9
10
11
12
13
14
MC1352
22 k
0.001 µF
0.001 µF
1 M
0.001 µF
0.001 µF
AGC INPUT
0.001 µF
0.001 µF
6.8 k
$L_p$
TUNER AGC DELAY
0.001 µF
0.001 µF
0.001 µF
TUNER AGC OUTPUT
INPUT
$R_S$ = 50 Ω
C2
C1
L1

All chokes ($L_p$) are self resonate at input frequency. $L_p$ ≈ 20 kΩ
See Figure 4 for Response Curve

| | 35 and 45 MHz | | 58 MHz | |
|---|---|---|---|---|
| L1 | 0.4 µH | Q · 100 | 0.3 µH | Q · 100 |
| T1 | 1.3-3.4 µH | Q · 100 @ 2 µH | 1.2-3.8 µH | Q · 100 @ 2 µH |
| C1 | 48-100 pF | | 40-80 pF | |
| C2 | 8-60 pF | | 12-45 pF | |

L1 and T1 = #26 AWG Tinned Nylon Acetate Wire.

L1 @ 35 or 45 MHz = 7-1/4 Turns on a 1/4" coil form
@ 58 MHz = 6 Turns on a 1/4" coil form
T1 Primary Winding = 18 Turns on a 1/4" coil form
Secondary Winding = 2 Turns Wound Evenly over Primary Winding for 35 or 45 MHz and 1 Turn for 58 MHz
Slug = Carbonyl E or J

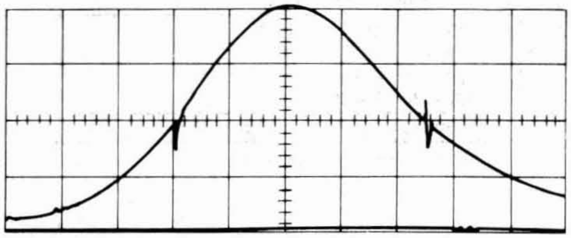
## GENERAL OPERATING INFORMATION

The MC1352, consists of an AGC section and an IF signal amplifier (Figure 2) subdivided into different functions as indicated by the illustration.

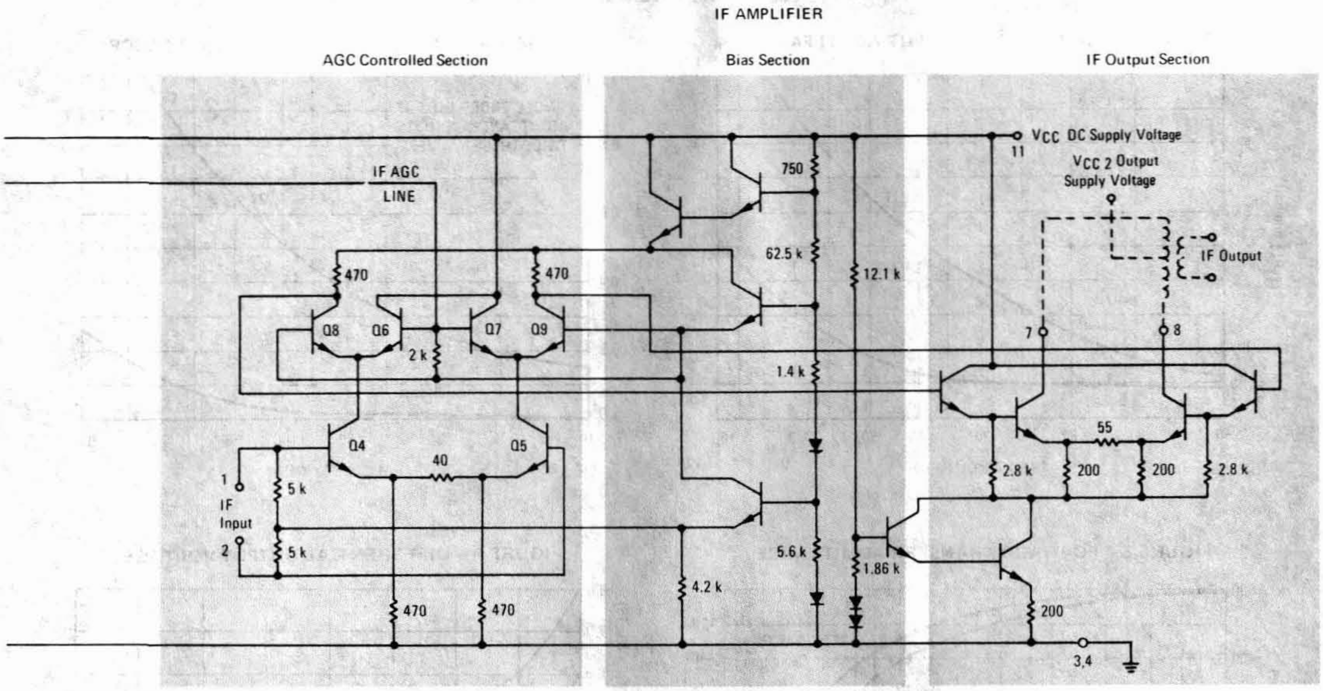
A gating pulse, a reference level, and a composite video signal are required for proper operation of the AGC section. Either positive or negative-going video may be used; necessary connections and signal levels are shown in Figure 1. The essential difference is that the video is fed into Pin 10 and AGC reference level is applied to Pin 6 for a video signal with positive-going sync while the input connections are reversed for negative-going sync.

The action of the gating section is such that the proper voltage, $V_C$,

### FIGURE 4 – TEST CIRCUIT RESPONSE CURVE
(45 and 58 MHz)



Scale: 1 MHz/cm



is maintained across the external capacitor, C2, for a particular video level and dc reference setting. The voltage $V_C$, is the result of the charge delivered through D1 and the charge drained by Q1. The charge delivered occurs during the time of the gating pulse, and its magnitude is determined by the amplitude of the video signal relative to the dc reference level. The voltage $V_C$ is delivered via the IF-AGC amplifier and applied to the variable gain stage of the IF signal amplifier and is also applied to the RF-AGC amplifier, where it is compared to the fixed RF-AGC delay voltage reference by the differential amplifier, Q2 and Q3. The following stages amplify the output signal of Q2 and shift the dc levels causing the RF-AGC voltage to vary.

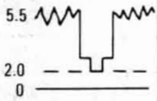
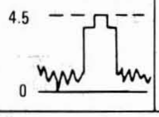
The input amplifiers (Q4 and Q5) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac). Terminals 1 and 2 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q6 and Q7 causing those transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q8 and Q9. The output amplifiers are fed from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant.

**NOTES:**

1. The 12-V supply must have a low ac impedance to prevent low-frequency instability in the RF-AGC loop. This can be achieved by a 12-V zener diode and a large decoupling capacitor. (5 μF).
2. Choices of C1, C2 and C3 depend somewhat on the set designers' preference concerning AGC stability versus AGC recovery speed. Typical values are C1 = 0.1 μF, C2 = 0.25 μF, C3 = 10 μF.
3. To set a fixed IF-AGC operating point (e.g., for receiver alignment) connect a 22 kΩ resistor from pin 9 to pin 11 to give minimum gain, then bias pin 14 to give the correct operating point using a 200 kΩ variable resistor to ground.
4. Although the unit will normally be operating with a very high power gain, the pin configuration has been carefully chosen so that shielding between input and output terminals will not normally be necessary even when a standard socket is used.

FIGURE 5 – TYPICAL AGC APPLICATION CHART

| Video Polarity | Pin 6 Voltage | Pin 10 Voltage | Pin 5 R1 (Ω) |
|---|---|---|---|
| Negative-Going Sync. |  | Adj. 1.0–4.0 Vdc<br>Nom 2.0 V | 0 |
| Positive-Going Sync. | Adj. 1.0–8.0 Vdc<br>Nom 4.5 V |  | 3.9 k |

## TYPICAL CHARACTERISTICS

($V_{CC}$ = +12 Vdc, $T_A$ = +25°C unless otherwise noted.)

FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE

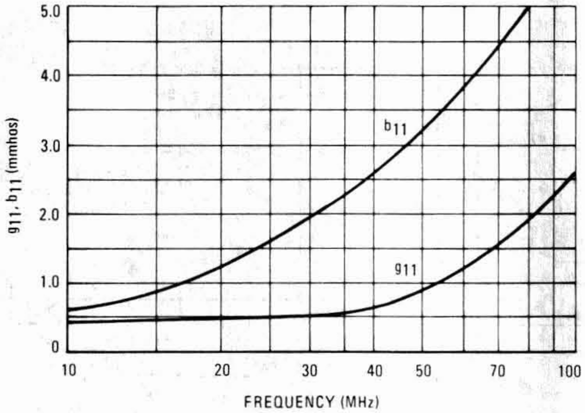


FIGURE 7 – DIFFERENTIAL OUTPUT ADMITTANCE

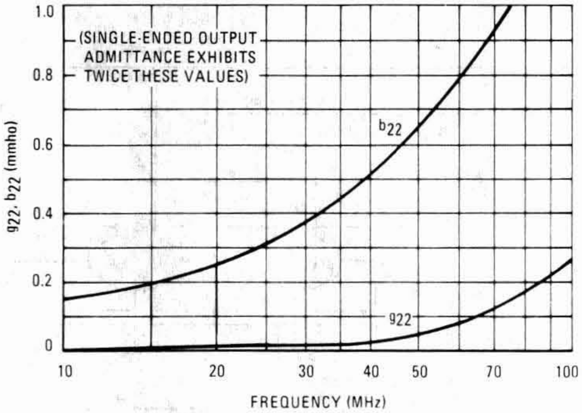


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

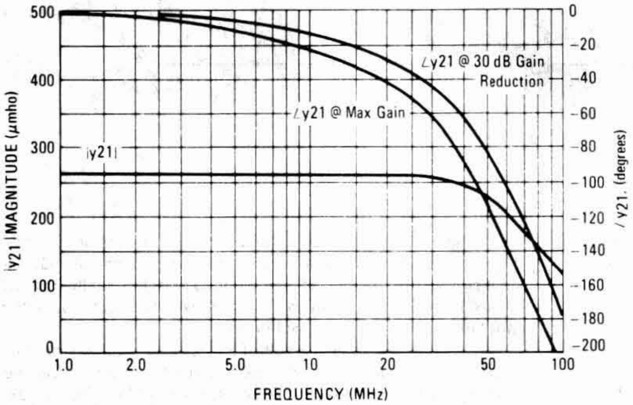


FIGURE 9 – DIFFERENTIAL OUTPUT VOLTAGE

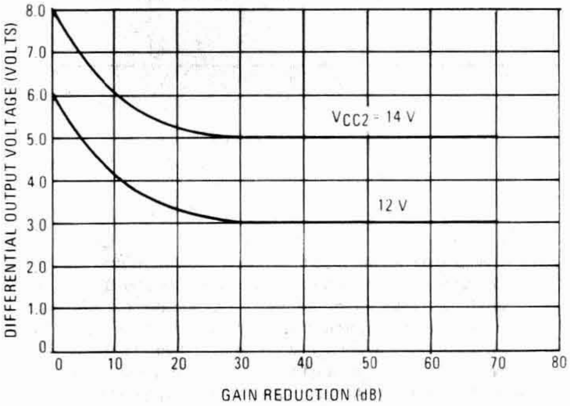


FIGURE 10 – AGC CHARACTERISTICS

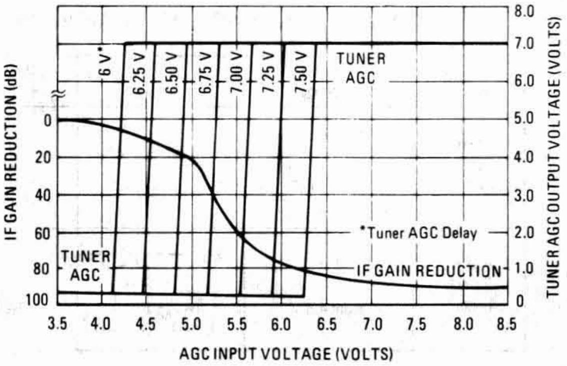
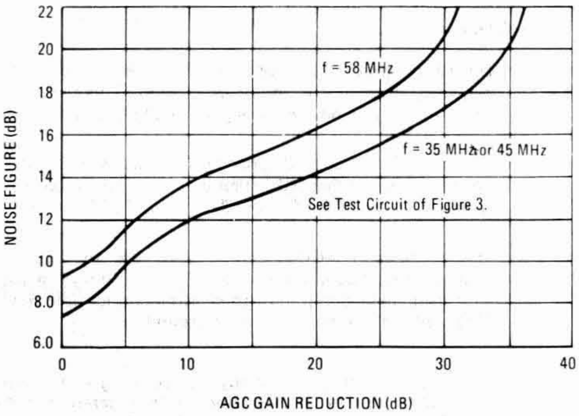


FIGURE 11 – TYPICAL NOISE FIGURE



## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC1355P | 0°C to +70°C | Plastic DIP |

# MC1355

## BALANCED FOUR-STAGE HIGH-GAIN FM/IF AMPLIFIER

. . . designed for use with Foster-Seeley discriminator or ratio detector in high quality FM systems.

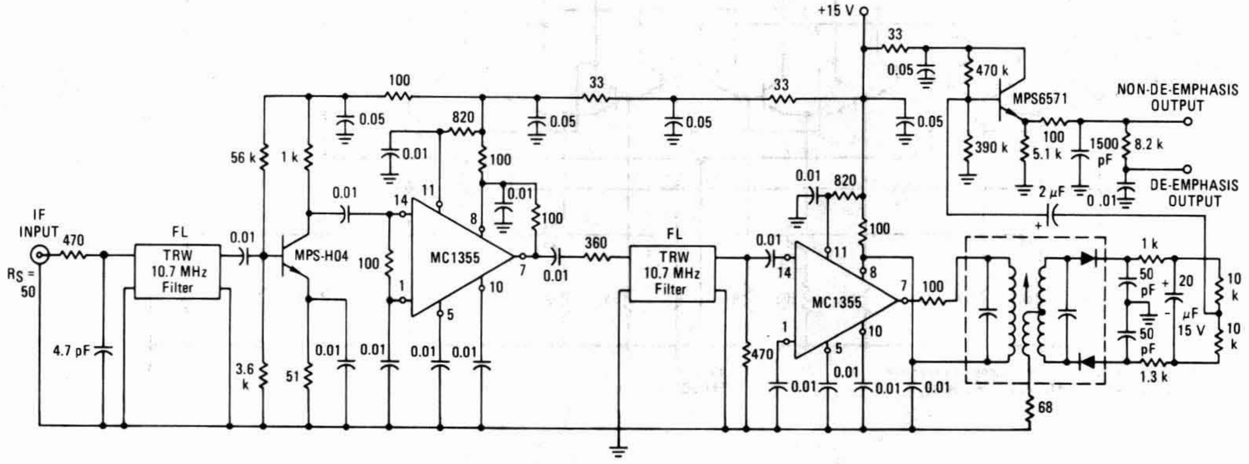
- High AM Rejection (60 dB typ)
- Wide Range of Supply Voltages (8 to 18 Vdc)
- Low Distortion (0.5% typ)

## LIMITING FM IF AMPLIFIER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

FIGURE 1 – DUAL MC1355 FM IF APPLICATION


+15 V
33
0.05
470 k
MPS6571
NON-DE-EMPHASIS OUTPUT
100
33
33
0.05
0.05
0.05
0.05
820
0.01
100
56 k
1 k
390 k
5.1 k
100
1500 pF
8.2 k
2 µF
0.01
DE-EMPHASIS OUTPUT
0.01
820
0.01
100
IF INPUT
470
$R_S$ = 50
FL
TRW 10.7 MHz Filter
0.01
MPS-H04
100
MC1355
14
11
8
7
1
10
5
0.01
360
FL
TRW 10.7 MHz Filter
0.01
14
11
8
7
1
10
5
MC1355
100
1 k
50 pF
20 µF 15 V
10 k
10 k
50 pF
1.3 k
4.7 pF
3.6 k
51
0.01
0.01
0.01
0.01
470
0.01
0.01
0.01
0.01
68
+

*All other pins grounded
T-Ratio Detector (input impedance ≅ 1.5 k) G.I. ≠36231 or equivalent

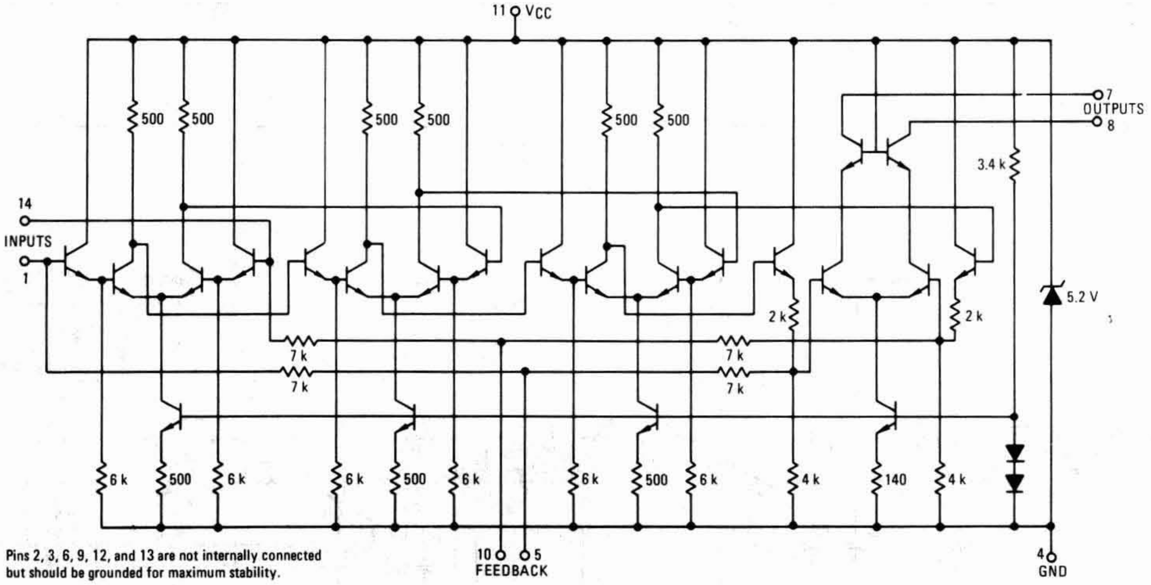
**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Value | Unit |
|---|---|---|
| Output Voltage (Pins 7 & 8) | 40 | Vdc |
| Supply Current to Pin 11 | 20 | mA |
| Input Signal Voltage (single-ended) | 5.0 | Vp-p |
| Input Signal Voltage (differential) | 10 | Vp-p |
| Power Dissipation (package limitation)<br>Derate above $T_A$ = +25°C | 625<br>5.0 | mW<br>mW/°C |
| Operating Temperature Range (Ambient) | 0 to +70° | °C |
| Storage Temperature Range | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 15 Vdc, f = 10.7 MHz, $T_A$ = +25°C)

| Characteristic | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Power Supply Voltage Range | | 8.0 | 15 | 18 | Vdc |
| Total Circuit Current | | – | 16 | – | mAdc |
| Total Output Stage Current | | – | 4.2 | – | mA |
| Device Dissipation | | – | 125 | – | mW |
| Internal Zener Voltage | | – | 5.2 | – | Vdc |
| Input Signal for 3 dB Limiting | | – | 175 | 250 | μV(rms) |
| Output Current Swing | | 3.1 | 4.2 | 5.4 | mA p-p |
| AM Rejection (10 mv to 1.0 v (rms) input, FM @ 100%, AM @ 80%, Foster Seeley detector) | | – | 60 | – | dB |
| Admittance Parameters | $Y_{11}$ | – | 120 + j320 | – | μmhos |
| | $Y_{12}$ | – | j0.6 | – | μmho |
| | $Y_{21}$ | – | 8 + j5.9 | – | mhos |
| | $Y_{22}$ | – | 15 + j230 | – | μmhos |

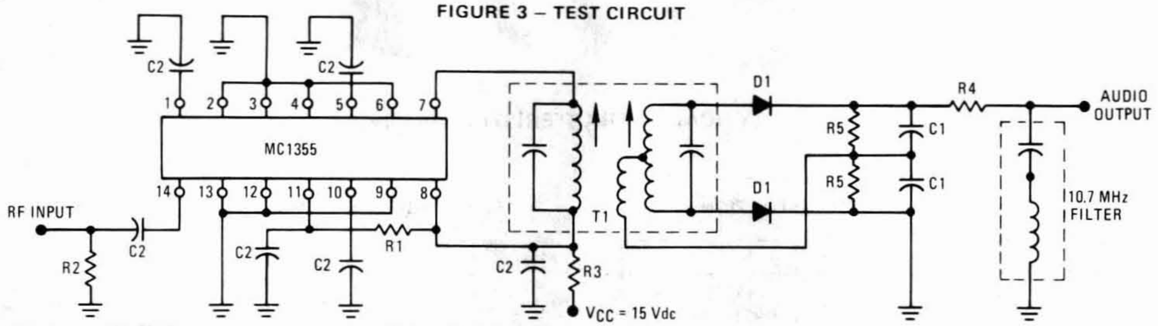
FIGURE 2 – CIRCUIT SCHEMATIC


11 VCC
500
500
500
500
500
500
7
OUTPUTS
8
3.4 k
14
INPUTS
1
5.2 V
2 k
2 k
7 k
7 k
7 k
7 k
6 k
500
6 k
6 k
500
6 k
6 k
500
6 k
4 k
140
4 k
10
5
FEEDBACK
4
GND

Pins 2, 3, 6, 9, 12, and 13 are not internally connected but should be grounded for maximum stability.

## TYPICAL CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT


C2
C2
MC1355
1
2
3
4
5
6
7
14
13
12
11
10
9
8
RF INPUT
R2
C2
C2
C2
R1
C2
R3
VCC = 15 Vdc
T1
D1
D1
R5
R5
C1
C1
R4
AUDIO OUTPUT
10.7 MHz FILTER

| | |
|---|---|
| R1 | 820 ohms |
| R2 | 50 ohms |
| R3 | 100 ohms |
| R4 | 5 kilohms |
| R5 | 12 kilohms |
| C1 | 50 pF |
| C2 | 0.01 μF |
| T1 | 10.7 MHz Foster-Seeley Discriminator,<br>Primary Impedance = 3.9 k,<br>Peak-to-Peak Separation = 600 kHz |
| D1 | Small Signal Germanium Diode<br>(1N542 or equiv) |

Specifications are given for a Foster-Seeley discriminator. Improved AM rejection at low signal levels can be obtained with a ratio detector.

For optimum circuit stability it is important to ground pins 2, 3, 4, 6, 9, 12, and 13.

FIGURE 4 – AM REJECTION TEST BLOCK DIAGRAM

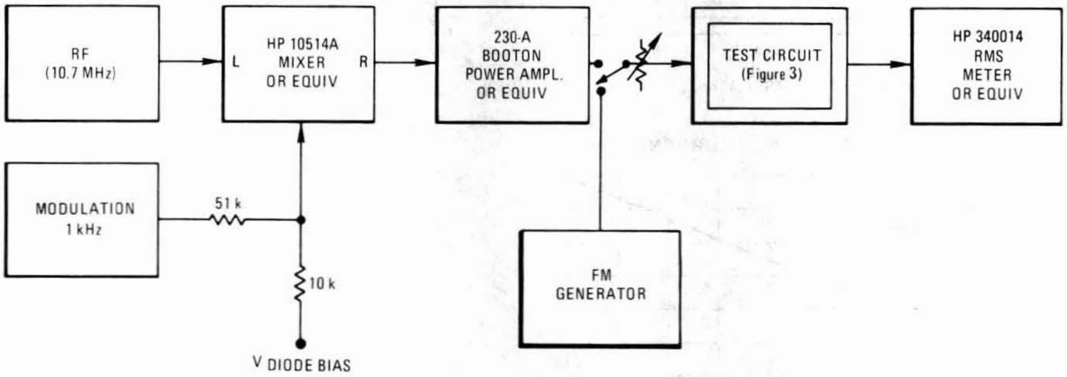

RF
(10.7 MHz)
HP 10514A
MIXER
OR EQUIV
L
R
230-A
BOOTON
POWER AMPL.
OR EQUIV
TEST CIRCUIT
(Figure 3)
HP 340014
RMS
METER
OR EQUIV
MODULATION
1 kHz
51 k
10 k
V DIODE BIAS
FM
GENERATOR

FIGURE 5 – LIMITING

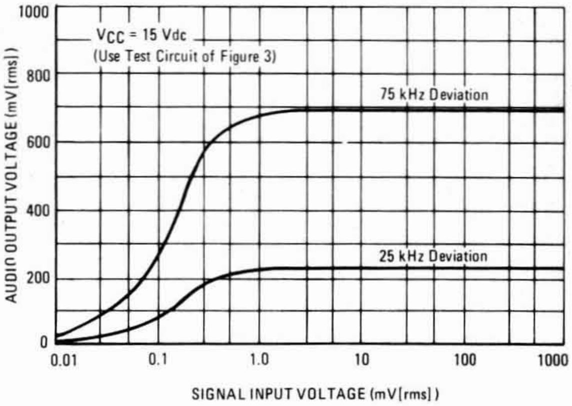
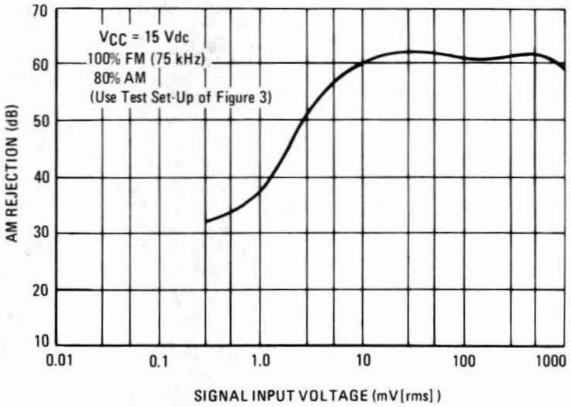


FIGURE 6 – AM REJECTION



## TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OUTPUT DISTORTION

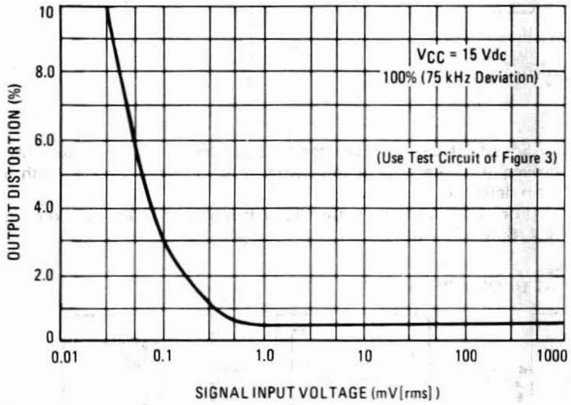


FIGURE 8 – SIGNAL-TO-NOISE RATIO SIGNAL

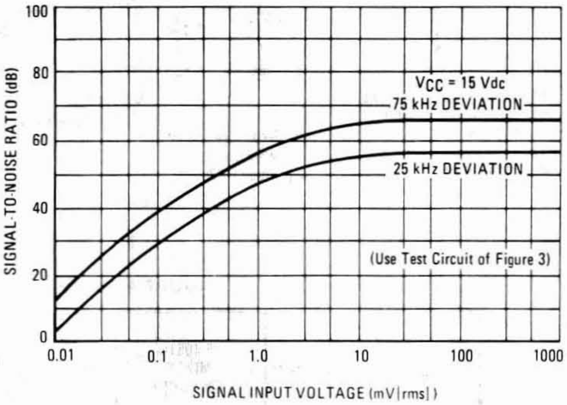
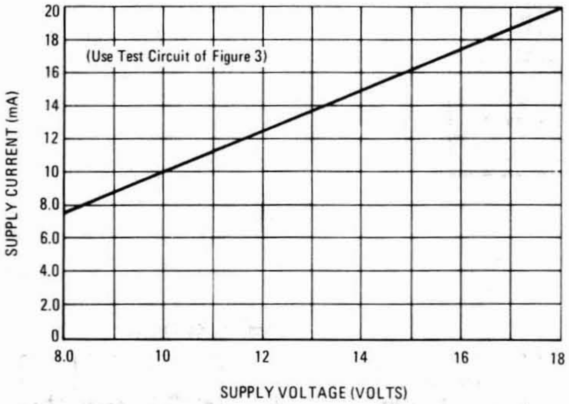


FIGURE 9 – TOTAL SUPPLY CURRENT



6

## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC1357P | 0°C to +70°C | Plastic DIP |

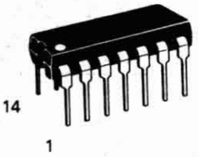
# MC1357

## IF AMPLIFIER AND QUADRATURE DETECTOR

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

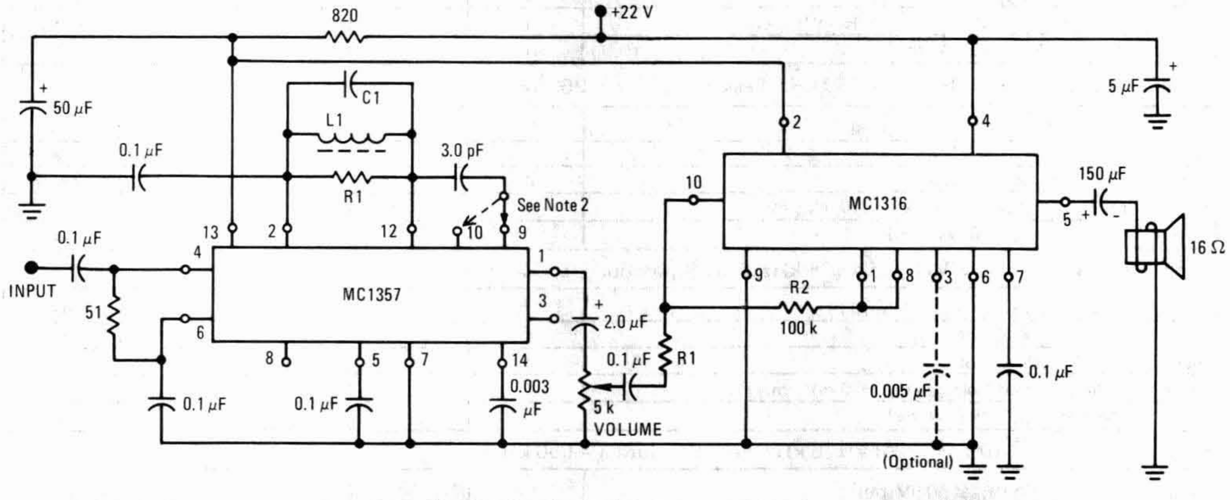
## TV SOUND IF OR FM IF AMPLIFIER WITH QUADRATURE DETECTOR

- A Direct Replacement for the ULN2111A
- Greatly Simplified FM Demodulator Alignment
- Excellent Performance at $V_{CC}$ = 8.0 Vdc



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

**FIGURE 1 – TV TYPICAL APPLICATION CIRCUIT**


820
+22 V
+
50 µF
C1
L1
0.1 µF
3.0 pF
R1
See Note 2
13
2
12
10
9
0.1 µF
4
INPUT
51
6
MC1357
1
3
8
5
7
14
0.1 µF
0.1 µF
0.003 µF
+
2.0 µF
0.1 µF
R1
5 k
VOLUME
10
MC1316
2
4
9
1
8
3
6
7
R2
100 k
0.005 µF
(Optional)
0.1 µF
5 µF
+
150 µF
5
+
16 Ω

Typical Performance:
2 Watts Output
2% Distortion
250 µV Sensitivity (3 dB Lim.)

C1 = 120 pF
L1 = 14 µH
R1 = 20 kΩ
Q = 30

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage | 16 | Vdc |
| Input Voltage (Pin 4) | 3.5 | $V_p$ |
| Power Dissipation (Package Limitation)<br>Plastic Packages<br>Derate above $T_A$ = +25°C | 625<br><br>5.0 | mW<br><br>mW/°C |
| Operating Temperature Range (Ambient) | 0 to +70° | °C |
| Storage Temperature Range | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 12 Vdc, $T_A$ = +25°C unless otherwise noted.)

| Characteristic | | Pin | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Drain Current | $V_{CC}$ = 8 V<br>$V_{CC}$ = 12 V | 13 | 10<br>– | 12<br>15 | 19<br>21 | mA |
| Amplifier Input Reference Voltage | | 6 | – | 1.45 | – | Vdc |
| Detector Input Reference Voltage | | 2 | – | 3.65 | – | Vdc |
| Amplifier High Level Output Voltage | | 10 | 1.25 | 1.45 | 1.65 | Vdc |
| Amplifier Low Level Output Voltage | | 9 | – | 0.145 | 0.2 | Vdc |
| Detector Output Voltage | $V_{CC}$ = 8 V<br>$V_{CC}$ = 12 V | 1 | –<br>– | 3.7<br>5.4 | –<br>– | Vdc |
| Amplifier Input Resistance | | 4 | – | 5.0 | – | kΩ |
| Amplifier Input Capacitance | | 4 | – | 11 | – | pF |
| Detector Input Resistance | | 12 | – | 70 | – | kΩ |
| Detector Input Capacitance | | 12 | – | 2.7 | – | pF |
| Amplifier Output Resistance | | 10 | – | 60 | – | ohms |
| Detector Output Resistance | | 1 | – | 200 | – | ohms |
| De-Emphasis Resistance | | 14 | – | 8.8 | – | kΩ |

**DYNAMIC CHARACTERISTICS** (FM Modulation Freq. = 1.0 kHz, Source Resistance = 50 ohms, $T_A$ = +25°C for all tests.)

($V_{CC}$ = 12 Vdc, $f_o$ = 4.5 MHz, Δf = ±25 kHz, Peak Separation = 150 kHz)

| Characteristics | Pin | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Amplifier Voltage Gain ($V_{in} \leq$ 50 μV[rms]) | 10 | – | 60 | – | dB |
| AM Rejection* ($V_{in}$ = 10 mV[rms]) | 1 | – | 36 | – | dB |
| Input Limiting Threshold Voltage | 4 | – | 250 | – | μV(rms) |
| Recovered Audio Output Voltage ($V_{in}$ = 10 mV[rms]) | 1 | – | 0.72 | – | V(rms) |
| Output Distortion ($V_{in}$ = 10 mV[rms]) | 1 | – | 3 | – | % |

($V_{CC}$ = 12 Vdc, $f_o$ = 5.5 MHz, Δf = ±50 kHz, Peak Separation = 260 kHz)

| | | | | | |
|---|---|---|---|---|---|
| Amplifier Voltage Gain ($V_{in} \leq$ 50 μV[rms]) | 10 | – | 60 | – | dB |
| AM Rejection* ($V_{in}$ = 10 mV[rms]) | 1 | – | 40 | – | dB |
| Input Limiting Threshold Voltage | 4 | – | 250 | – | μV(rms) |
| Recovered Audio Output Voltage ($V_{in}$ = 10 mV[rms]) | 1 | – | 1.2 | – | V(rms) |
| Output Distortion ($V_{in}$ = 10 mV[rms]) | 1 | – | 5 | – | % |

($V_{CC}$ = 8.0 Vdc, $f_o$ = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

| | | | | | |
|---|---|---|---|---|---|
| Amplifier Voltage Gain ($V_{in} \leq$ 50 μV[rms]) | 10 | – | 53 | – | dB |
| AM Rejection* ($V_{in}$ = 10 mV[rms]) | 1 | – | 37 | – | dB |
| Input Limiting Threshold Voltage | 4 | – | 600 | – | μV(rms) |
| Recovered Audio Output Voltage ($V_{in}$ = 10 mV[rms]) | 1 | – | 0.30 | – | V(rms) |
| Output Distortion ($V_{in}$ = 10 mV[rms]) | 1 | – | 1.4 | – | % |

($V_{CC}$ = 12 Vdc, $f_o$ = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

| | | | | | |
|---|---|---|---|---|---|
| Amplifier Voltage Gain ($V_{in} \leq$ 50 μV[rms]) | 10 | – | 53 | – | dB |
| AM Rejection* ($V_{in}$ = 10 mV[rms]) | 1 | – | 45 | – | dB |
| Input Limiting Threshold Voltage | 4 | – | 600 | – | μV(rms) |
| Recovered Audio Output Voltage ($V_{in}$ = 10 mV[rms]) | 1 | – | 0.48 | – | V(rms) |
| Output Distortion ($V_{in}$ = 10 mV[rms]) | 1 | – | 1.4 | – | % |

*100% FM, 30% AM Modulation

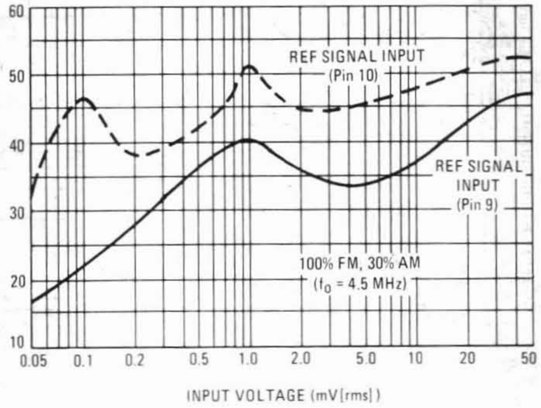
## TYPICAL CHARACTERISTICS

($V_{CC}$ = 12 V, $T_A$ = +25°C unless otherwise noted)

(Use Test Circuit of Figure 13)

($f_o$ = 4.5 MHz)

FIGURE 2 – AM REJECTION



($f_o$ = 5.5 MHz)

FIGURE 3 – AM REJECTION

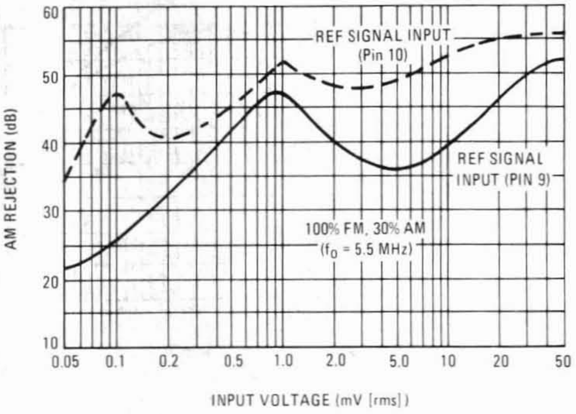


FIGURE 4 – DETECTED AUDIO OUTPUT

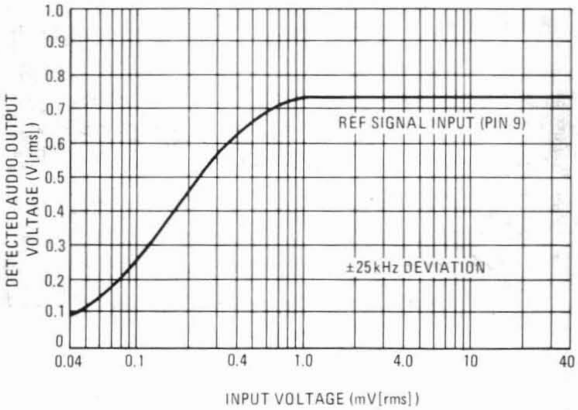


FIGURE 5 – DETECTED AUDIO OUTPUT

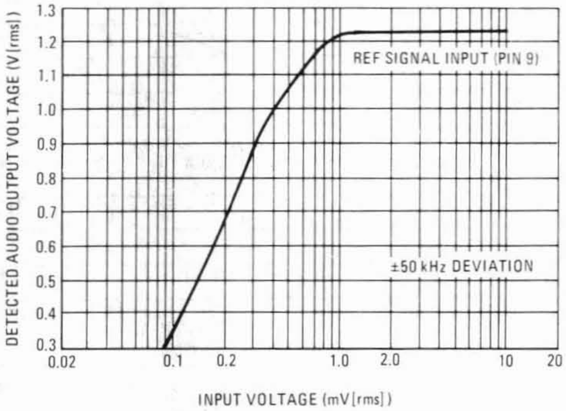


FIGURE 6 – DETECTOR TRANSFER CHARACTERISTIC

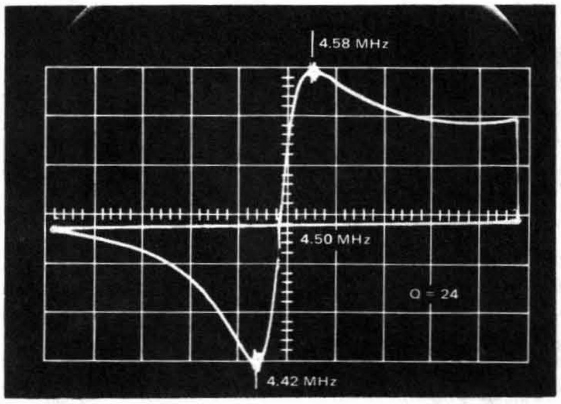
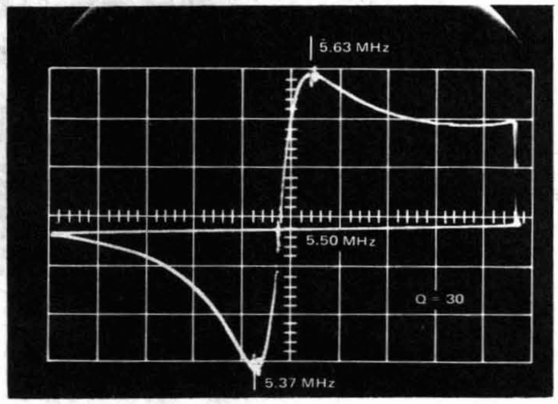


FIGURE 7 – DETECTOR TRANSFER CHARACTERISTIC



## TYPICAL CHARACTERISTICS (continued)

($f_o$ = 10.7 MHz, $T_A$ = +25°C unless otherwise noted.)
(Use Test Circuit of Figure 13)

FIGURE 8 – AM REJECTION

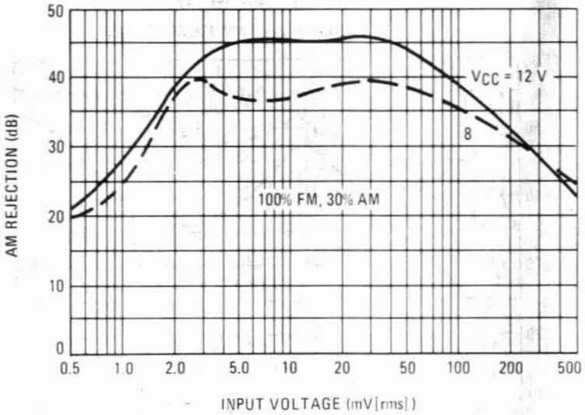


FIGURE 9 – AFC VOLTAGE DRIFT
(1.0 mV INPUT CARRIER @ 10.7 MHz)

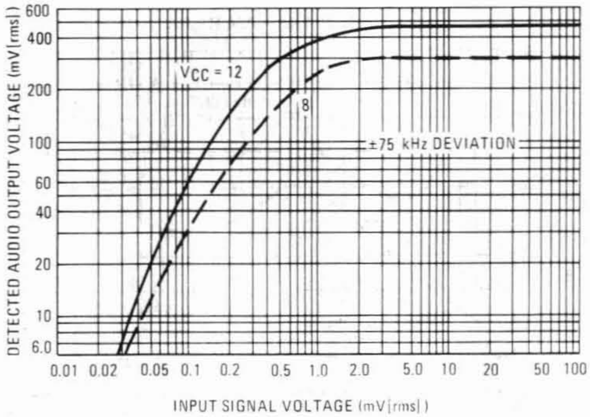


FIGURE 10 – LIMITING

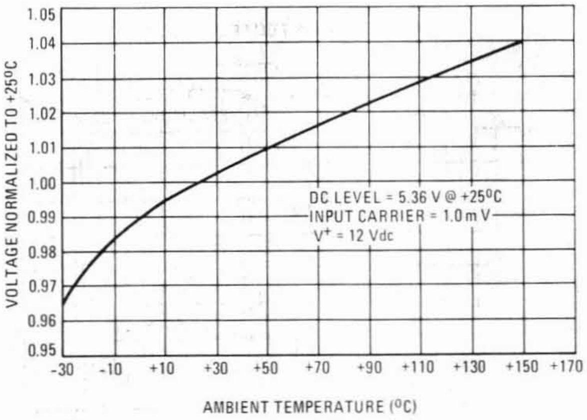


FIGURE 11 – SIGNAL-TO-NOISE RATIO

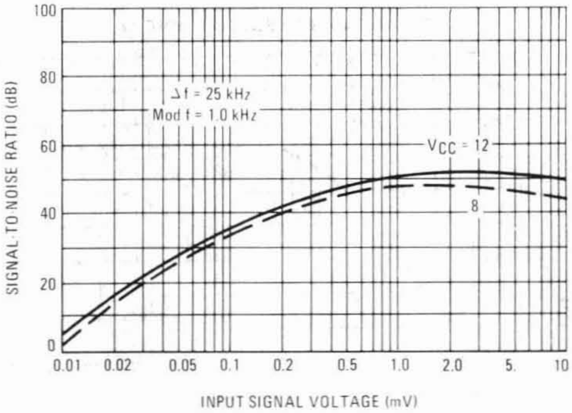


FIGURE 12 – DETECTOR TRANSFER CHARACTERISTIC

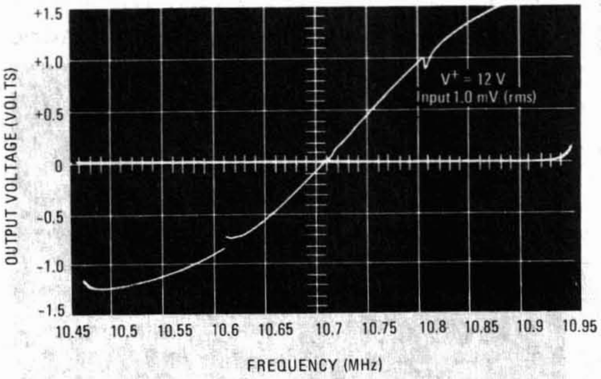
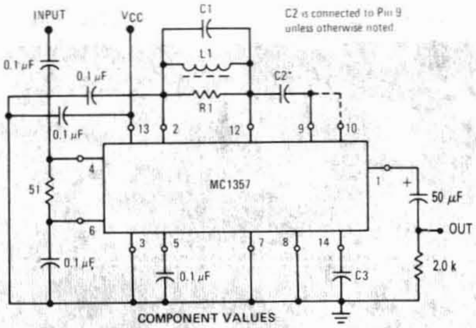


FIGURE 13 – TEST CIRCUIT

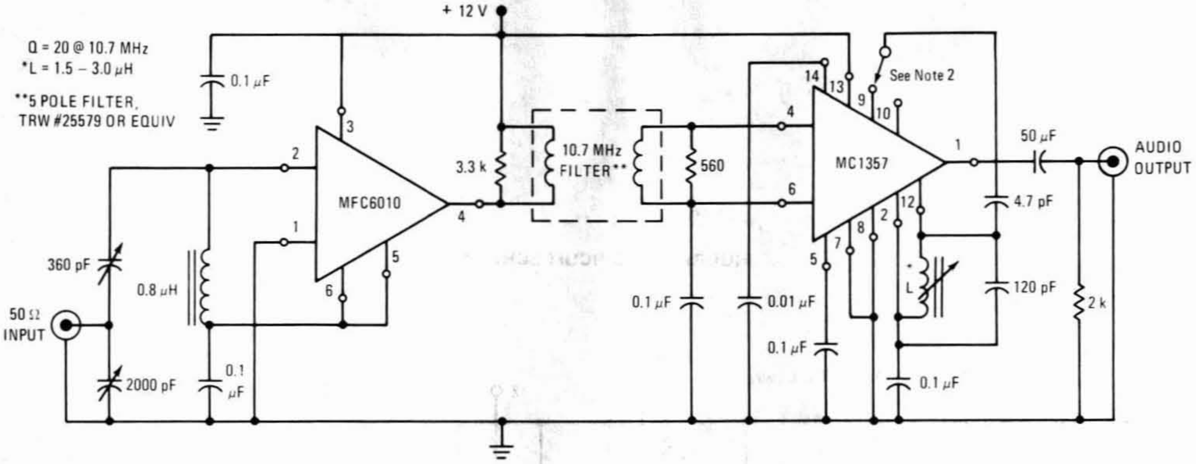

INPUT
VCC
C1
L1
R1
C2*
0.1 µF
0.1 µF
0.1 µF
0.1 µF
0.1 µF
51
13
2
12
9
10
4
6
1
3
5
7
8
14
MC1357
+
50 µF
OUT
2.0 k
C3

*C2 is connected to Pin 9 unless otherwise noted.

COMPONENT VALUES

| f | L1 | C1 | R1 | Q(R1, L1) | C2 | C3 |
|---|---|---|---|---|---|---|
| MHz | µH | pF | kΩ |  | pF | µF |
| 4.5 | 14 | 120 | 20 | 30 | 3.0 | 0.003 |
| 5.5 | 8.0 | 100 | 20 | 30 | 3.0 | 0.003 |
| 10.7 | 2.0 | 120 | 3.9 | 20 | 4.7 | 0.01 |

FIGURE 14 – FM RADIO TYPICAL APPLICATION CIRCUIT


+ 12 V
Q = 20 @ 10.7 MHz
*L = 1.5 – 3.0 μH
**5 POLE FILTER, TRW #25579 OR EQUIV
0.1 μF
MFC6010
3.3 k
10.7 MHz FILTER**
560
MC1357
See Note 2
50 μF
AUDIO OUTPUT
4.7 pF
120 pF
2 k
L
0.1 μF
0.01 μF
0.1 μF
0.1 μF
360 pF
0.8 μH
50 Ω INPUT
2000 pF
0.1 μF
1
2
3
4
5
6
7
8
9
10
12
13
14

Note 1:

Information shown in Figures 15, 16, and 17 was obtained using the circuit of Figure 14.

Note 2:

Optional input to the quadrature coil may be from either pin 9 or pin 10 in the applications shown. Pin 9 has commonly been used on this type of part to avoid overload with various tuning techniques. For this reason, pin 9 is used in tests on the preceding pages (except as noted). However, a significant improvement of limiting sensitivity can be obtained using pin 10, see Figure 17, and no overload problems have been incurred with this tuned circuit configuration.

FIGURE 15 – OUTPUT DISTORTION

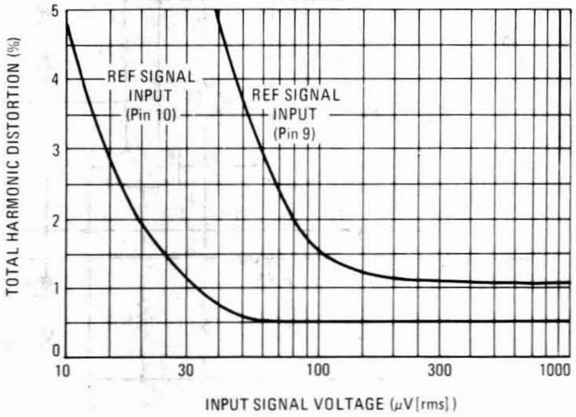


FIGURE 16 – SIGNAL-TO-NOISE RATIO

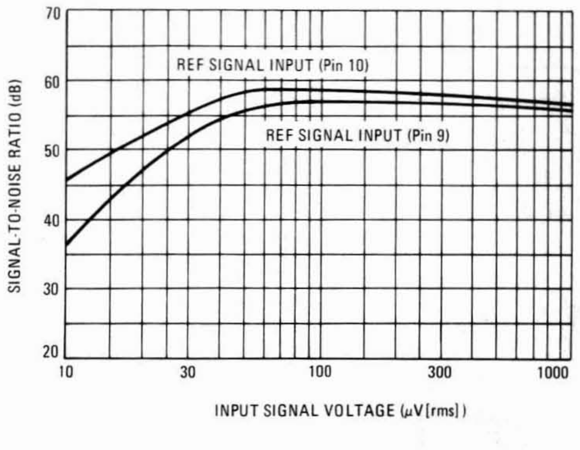


FIGURE 17 – RECOVERED AUDIO OUTPUT

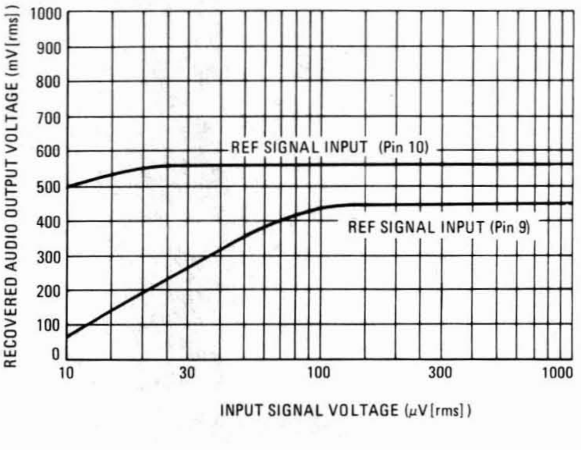
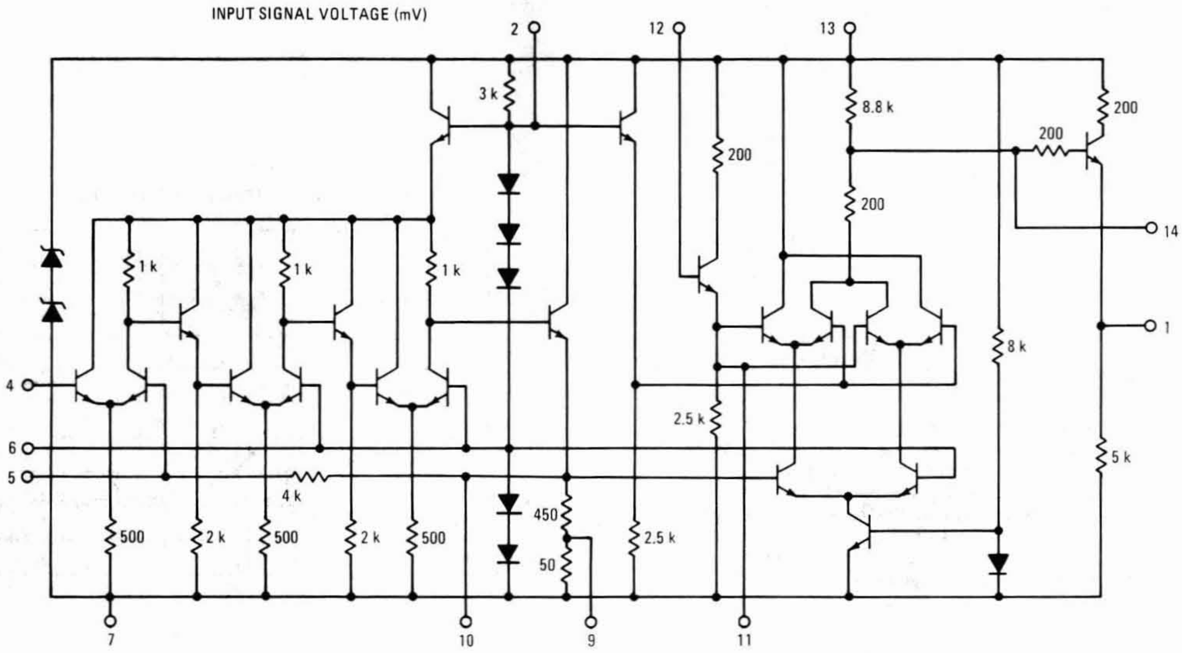


FIGURE 18 – CIRCUIT SCHEMATIC


INPUT SIGNAL VOLTAGE (mV)
2
12
13
3 k
8.8 k
200
200
200
200
1 k
1 k
1 k
14
1
8 k
4
6
5
2.5 k
5 k
4 k
450
500
2 k
500
2 k
500
50
2.5 k
7
10
9
11

# MC1358

## IF AMPLIFIER, LIMITER, FM DETECTOR, AUDIO DRIVER, ELECTRONIC ATTENUATOR

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC1358P | −20°C to +75°C | Plastic DIP |

## TV SOUND IF AMPLIFIER

. . . a versatile monolithic device incorporating IF limiting, detection, electronic attenuation, audio amplifier, and audio driver capabilities.

- Direct Replacement for the CA3065
- Differential Peak Detector Requiring a Single Tuned Circuit
- Electronic Attenuator Replaces Conventional ac Volume Control − Range > 60 dB
- Excellent AM Rejection @ 4.5 and 5.5 MHz
- High Stability
- Low Harmonic Distortion
- Audio Drive Capability − 6.0 mAp-p
- Minimum Undesirable Output Signal @ Maximum Attenuation

**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

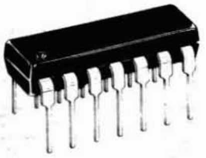
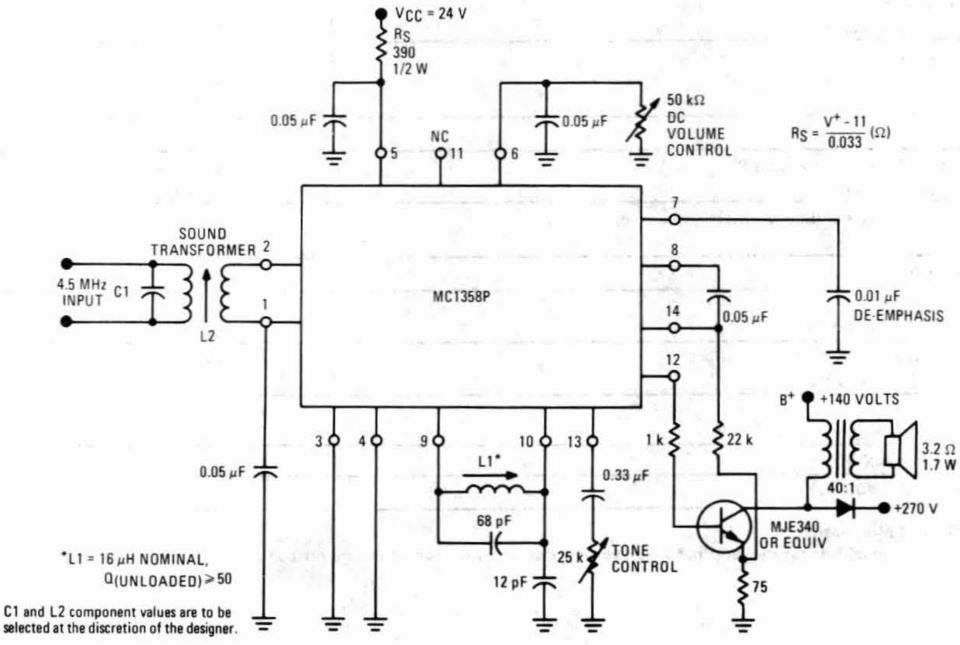


FIGURE 1 – TYPICAL TV APPLICATION CIRCUIT



$V_{CC}$ = 24 V
$R_S$
390
1/2 W
0.05 μF
0.05 μF
50 kΩ
DC
VOLUME
CONTROL
$R_S = \frac{V^+ - 11}{0.033}$ (Ω)
NC
5
11
6
7
8
14
12
SOUND
TRANSFORMER
2
1
4.5 MHz
INPUT
C1
L2
MC1358P
0.01 μF
DE-EMPHASIS
0.05 μF
B+
+140 VOLTS
3
4
9
10
13
1 k
22 k
3.2 Ω
1.7 W
40:1
+270 V
L1*
0.33 μF
0.05 μF
68 pF
MJE340
OR EQUIV
25 k
TONE
CONTROL
12 pF
75
*L1 = 16 μH NOMINAL,
Q(UNLOADED) ≥ 50
C1 and L2 component values are to be selected at the discretion of the designer.

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Value | Unit |
|---|---|---|
| Input Signal Voltage (Pins 1 and 2) | ±3.0 | Vdc |
| Power Supply Current | 50 | mA |
| Power Dissipation (Package Limitation) | | |
| Plastic Packages | 625 | mW |
| Derate above $T_A$ = +25°C | 5.0 | mW/°C |
| Operating Temperature Range (Ambient) | -20 to +75 | °C |
| Storage Temperature Range | -65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 24 Vdc, $T_A$ = +25°C unless otherwise noted).

| Characteristic | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Regulated Voltage | 5 | 10.3 | 11 | 12.2 | Vdc |
| DC Supply Current ($V^+$ = 9 Vdc, $R_S$ = 0) | 5 | 10 | 16 | 24 | mA |
| Quiescent Output Voltage | 12 | – | 5.1 | – | Vdc |

**DYNAMIC CHARACTERISTICS** ($V_{CC}$ = 24 Vdc, $T_A$ = +25°C unless otherwise noted).

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **IF AMPLIFIER AND DETECTOR** | | | | |
| **$f_o$ = 4.5 MHz, Δf = ±25 kHz** | | | | |
| AM Rejection* ($V_{in}$ = 10 mV [rms]) | 40 | 51 | – | dB |
| Input Limiting Threshold Voltage | – | 200 | 400 | μV(rms) |
| Recovered Audio Output Voltage ($V_{in}$ = 10 mV[rms]) | 0.5 | 0.70 | – | V(rms) |
| Output Distortion ($V_{in}$ = 10 mV [rms]) | – | 0.4 | 2.0 | % |
| **$f_o$ = 5.5 MHz, Δf = ±50 kHz** | | | | |
| AM Rejection* ($V_{in}$ = 10 mV [rms]) | 40 | 53 | – | dB |
| Input Limiting Threshold Voltage | – | 200 | 400 | μV(rms) |
| Recovered Audio Output Voltage ($V_{in}$ = 10 mV [rms]) | 0.5 | 0.91 | – | V(rms) |
| Output Distortion ($V_{in}$ = 10 mV [rms]) | – | 0.9 | – | % |
| Input Impedance Components (f = 4.5 MHz, measurement between Pins 1 and 2) | | | | |
| Parallel Input Resistance | – | 17 | – | kΩ |
| Parallel Input Capacitance | – | 4.0 | – | pF |
| Output Impedance Components (f = 4.5 MHz, measurement between Pin 9 and Gnd) | | | | |
| Parallel Output Resistance | – | 3.25 | – | kΩ |
| Parallel Output Capacitance | – | 3.6 | – | pF |
| Output Resistance, Detector | | | | |
| Pin 7 | – | 7.5 | – | kΩ |
| Pin 8 | – | 250 | – | Ω |
| **ATTENUATOR** | | | | |
| Volume Reduction Range (See Figure 8) (dc Volume Control = ∞) | 60 | – | – | dB |
| Maximum Undesirable Signal (See Note 1) (dc Volume Control = ∞) | – | 0.07 | 1.0 | mV |
| **AUDIO AMPLIFIER** | | | | |
| Voltage Gain ($V_{in}$ = 0.1 V(rms), f = 400 Hz) | 17.5 | 20 | – | dB |
| Total Harmonic Distortion ($V_o$ = 2.0 V(rms), f = 400 Hz) | – | 2.0 | – | % |
| Output Voltage (THD = 5%, f = 400 Hz) | 2.0 | 3.0 | – | V(rms) |
| Input Resistance (f = 400 Hz) | – | 70 | – | kΩ |
| Output Resistance (f = 400 Hz) | – | 270 | – | Ω |

*100% FM, 30% AM Modulation.

Note 1. Undesirable signal is measured at pin 8 when volume control is set for minimum output.

## TYPICAL CHARACTERISTICS

($V_{CC}$ = 24 Vdc, $T_A$ = +25°C unless otherwise noted)

**($f_o$ = 4.5 MHz)**

**FIGURE 2 – AM REJECTION**

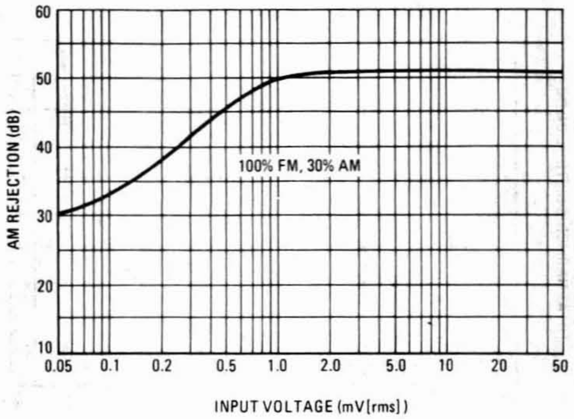


**FIGURE 4 – DETECTED AUDIO OUTPUT**

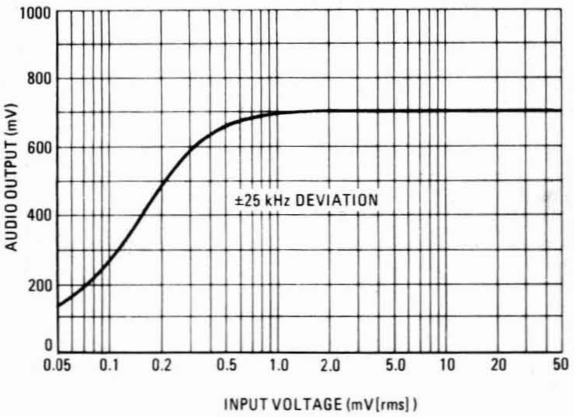
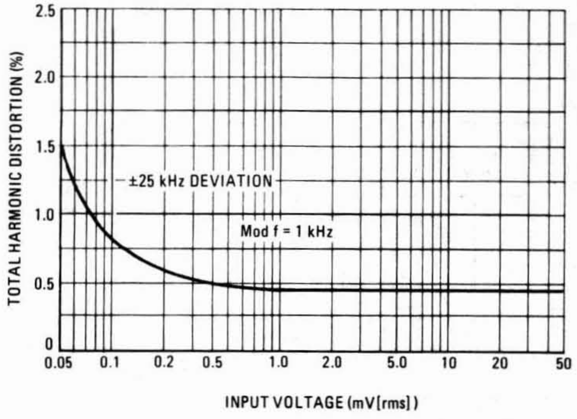


**FIGURE 6 – IF AMPLIFIER AND DETECTOR THD**



**($f_o$ = 5.5 MHz)**

**FIGURE 3 – AM REJECTION**

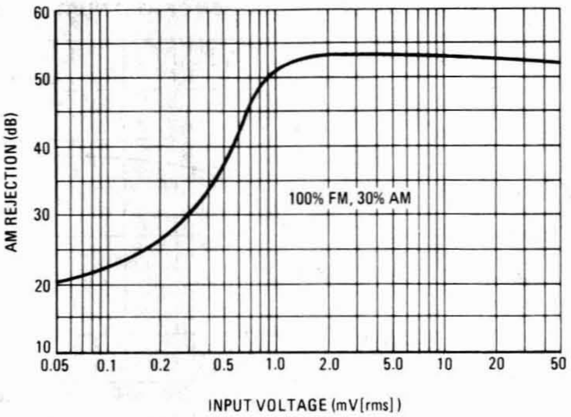


**FIGURE 5 – DETECTED AUDIO OUTPUT**

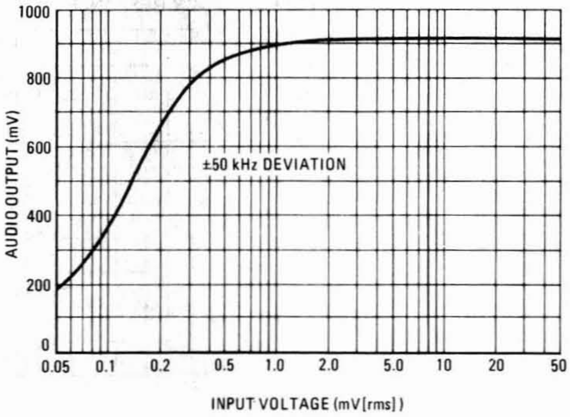
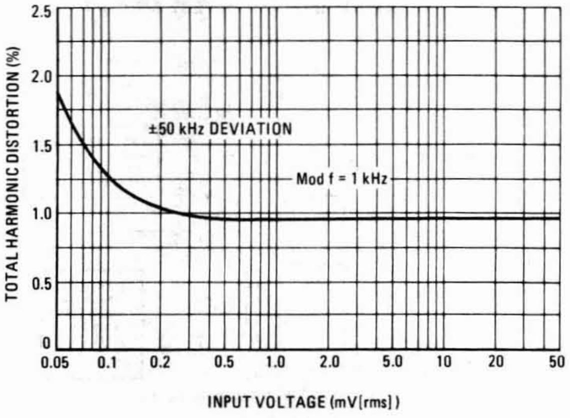


**FIGURE 7 – IF AMPLIFIER AND DETECTOR THD**



## TYPICAL CHARACTERISTICS (continued)

**FIGURE 8 – GAIN REDUCTION OF ATTENUATOR**

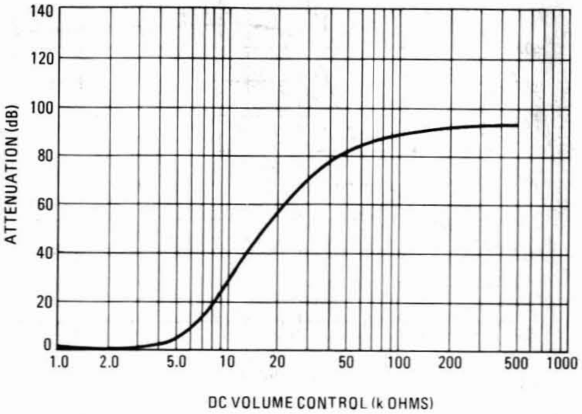


**FIGURE 9 – AUDIO AMPLIFIER THD**

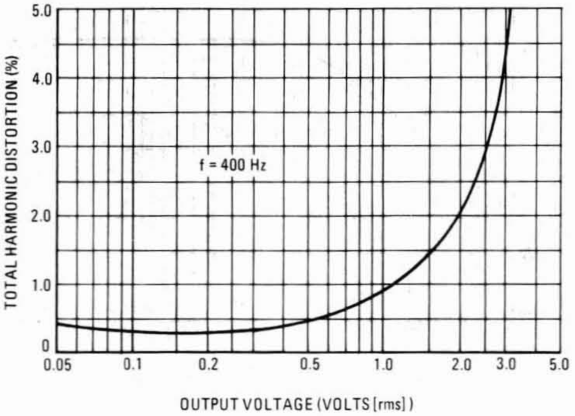


**FIGURE 10 – IF FREQUENCY RESPONSE**

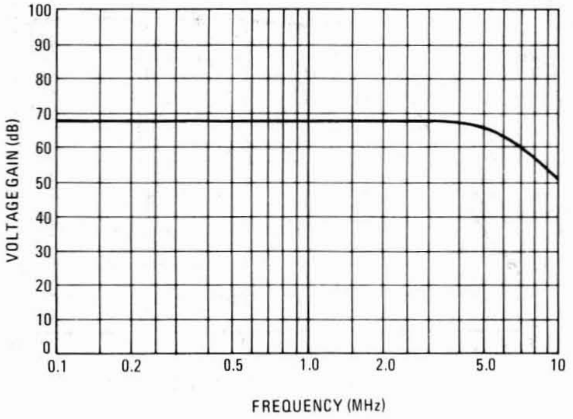
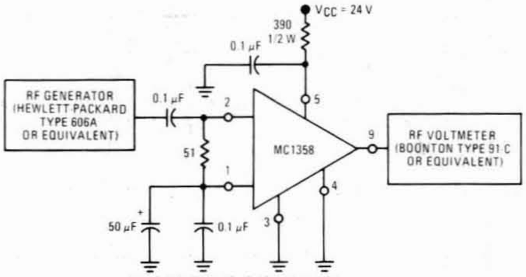
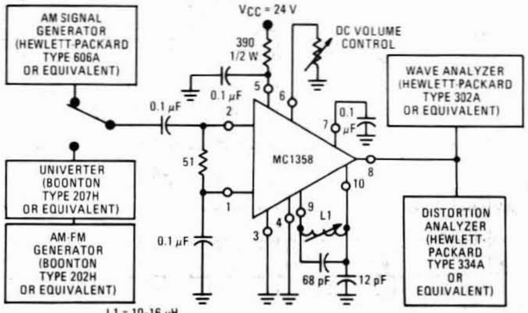


**FIGURE 11 – IF FREQUENCY RESPONSE TEST CIRCUIT**


VCC = 24 V
390
1/2 W
0.1 µF
RF GENERATOR
(HEWLETT-PACKARD
TYPE 606A
OR EQUIVALENT)
0.1 µF
2
5
MC1358
9
RF VOLTMETER
(BOONTON TYPE 91-C
OR EQUIVALENT)
51
1
4
50 µF
0.1 µF
3

Pins 6, 7, 8, 10, 11, 12, 13, 14 no connection.

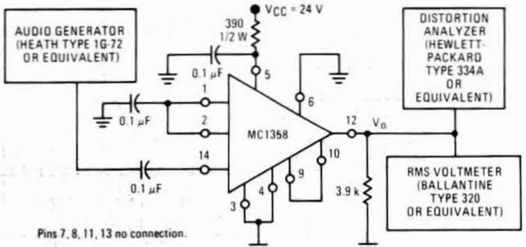
**FIGURE 12 – AM REJECTION, DETECTED AUDIO, THD, ATTENUATION TEST CIRCUIT**


AM SIGNAL
GENERATOR
(HEWLETT-PACKARD
TYPE 606A
OR EQUIVALENT)
VCC = 24 V
390
1/2 W
DC VOLUME
CONTROL
WAVE ANALYZER
(HEWLETT-PACKARD
TYPE 302A
OR EQUIVALENT)
0.1 µF
5
6
0.1 µF
2
0.1
µF
7
UNIVERTER
(BOONTON
TYPE 207H
OR EQUIVALENT)
51
MC1358
8
10
1
9
L1
AM-FM
GENERATOR
(BOONTON
TYPE 202H
OR EQUIVALENT)
0.1 µF
3
4
68 pF
12 pF
DISTORTION
ANALYZER
(HEWLETT-
PACKARD
TYPE 334A
OR
EQUIVALENT)

L1 = 10-16 µH
Q(unloaded) ≥ 50

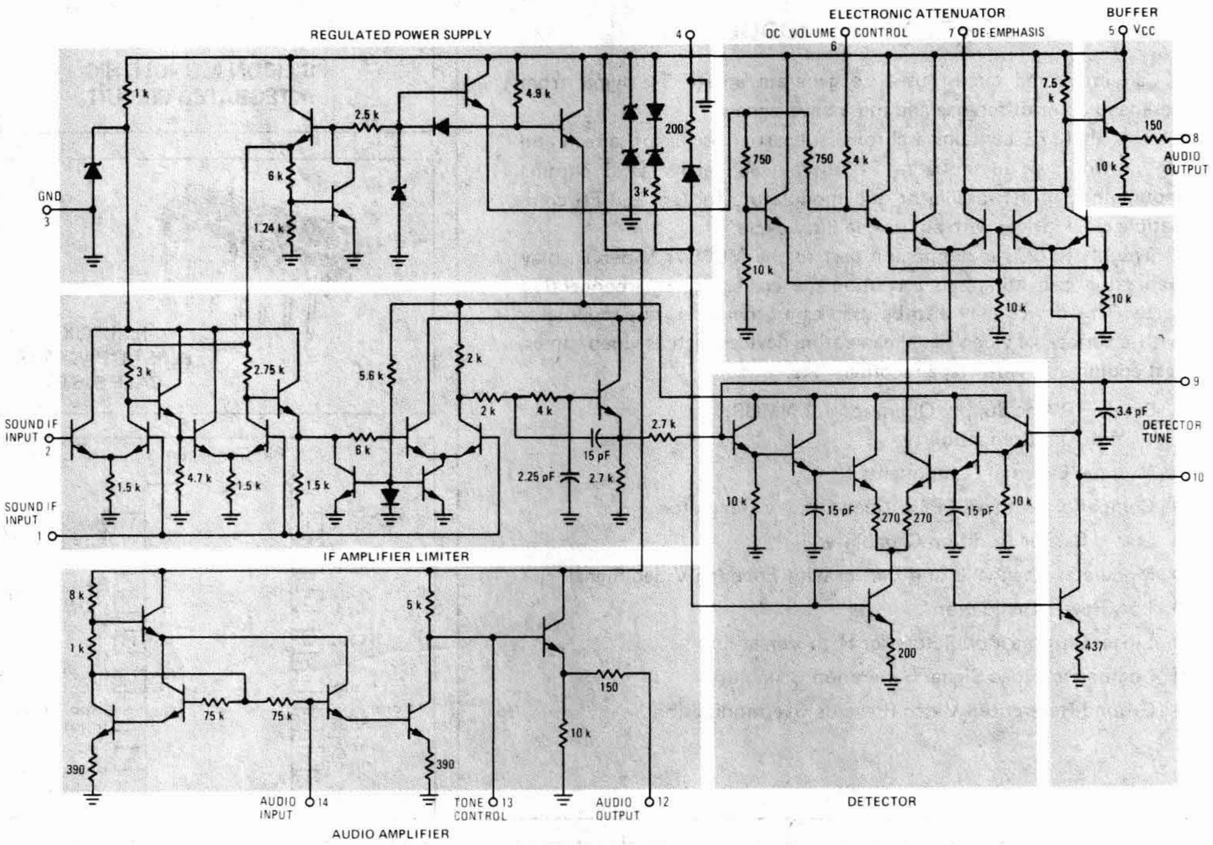
Pins 11, 12, 13, 14 no connection.

**FIGURE 13 – AUDIO VOLTAGE GAIN, AUDIO THD TEST CIRCUIT**


AUDIO GENERATOR
(HEATH TYPE 1G-72
OR EQUIVALENT)
VCC = 24 V
390
1/2 W
0.1 µF
5
DISTORTION
ANALYZER
(HEWLETT-
PACKARD
TYPE 334A
OR
EQUIVALENT)
1
6
0.1 µF
2
MC1358
12
Vo
14
10
0.1 µF
9
4
3
3.9 k
RMS VOLTMETER
(BALLANTINE
TYPE 320
OR EQUIVALENT)

Pins 7, 8, 11, 13 no connection.

FIGURE 14 – CIRCUIT SCHEMATIC


REGULATED POWER SUPPLY
ELECTRONIC ATTENUATOR
BUFFER
4
DC VOLUME CONTROL 6
7 DE-EMPHASIS
5 VCC
1 k
2.5 k
4.9 k
6 k
1.24 k
200
3 k
GND 3
750
750
4 k
7.5 k
150
8 AUDIO OUTPUT
10 k
10 k
10 k
10 k
3 k
2.75 k
5.6 k
2 k
2 k
4 k
SOUND IF INPUT 2
1.5 k
4.7 k
1.5 k
1.5 k
6 k
15 pF
2.25 pF
2.7 k
2.7 k
SOUND IF INPUT 1
IF AMPLIFIER LIMITER
9
3.4 pF
DETECTOR TUNE
10
10 k
15 pF
270
270
15 pF
10 k
200
437
8 k
1 k
5 k
75 k
75 k
150
10 k
390
390
AUDIO INPUT 14
TONE CONTROL 13
AUDIO OUTPUT 12
AUDIO AMPLIFIER
DETECTOR

**MOTOROLA**

# MC1372

## COLOR TV VIDEO MODULATOR CIRCUIT

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

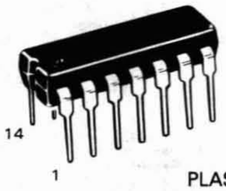
## COLOR TV VIDEO MODULATOR

. . . an integrated circuit used to generate an RF TV signal from baseband color-difference and luminance signals.

The MC1372 contains a chroma subcarrier oscillator, a lead and lag network, a quasi-quadrature suppressed carrier DSB chroma modulator, an RF oscillator and modulator, and an LSTTL compatible clock driver with adjustable duty cycle.

The MC1372 is a companion part to the MC6847 Video Display Generator, providing and accepting the correct dc interconnection levels. This device may also be used as a general-purpose modulator with a variety of video signal generating devices such as video games, test equipment, video tape recorders, etc.

- Single 5.0 Vdc Supply Operation for NMOS and TTL Compatibility
- Minimal External Components
- Compatible with MC6847 Video Display Generator
- Sound Carrier Addition Capability
- Modulates Channel 3 or 4 Carrier with Encoded Video Signal
- Low Power Dissipation
- Linear Chroma Modulators for High Versatility
- Composite Video Signal Generation Capability
- Ground-Referenced Video Prevents Overmodulation



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

**Pin Connections**

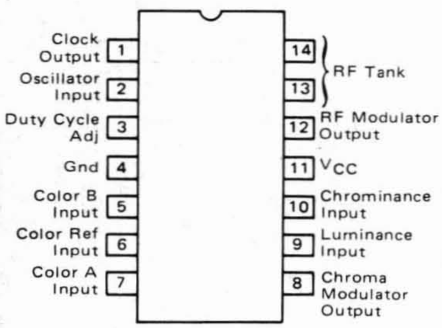
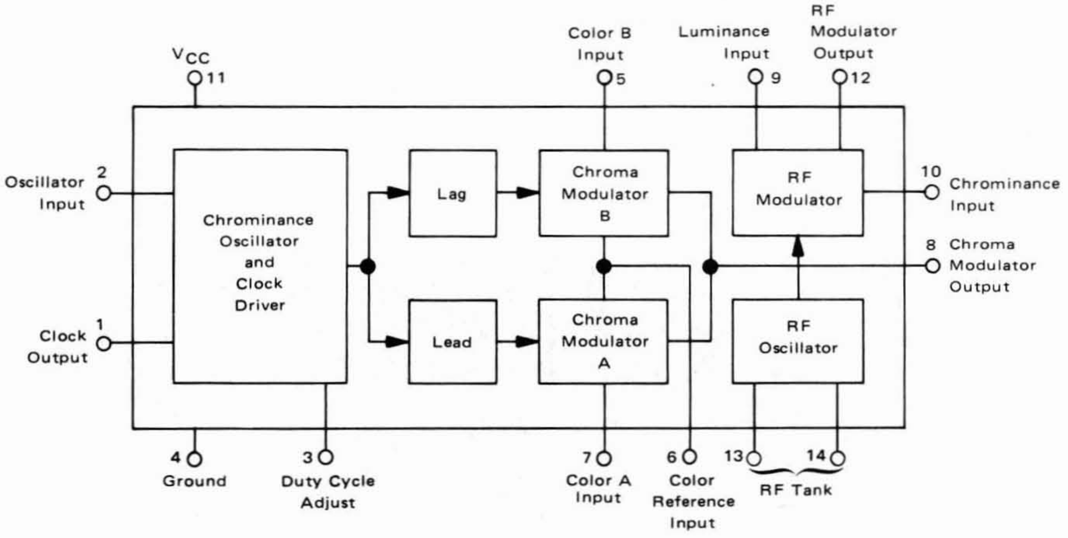

Clock Output 1
Oscillator Input 2
Duty Cycle Adj 3
Gnd 4
Color B Input 5
Color Ref Input 6
Color A Input 7
8 Chroma Modulator Output
9 Luminance Input
10 Chrominance Input
11 VCC
12 RF Modulator Output
13
14
RF Tank

**FIGURE 1 – BLOCK DIAGRAM**


VCC 11
Color B Input 5
Luminance Input 9
RF Modulator Output 12
Oscillator Input 2
Clock Output 1
Chrominance Oscillator and Clock Driver
Lag
Lead
Chroma Modulator B
Chroma Modulator A
RF Modulator
RF Oscillator
10 Chrominance Input
8 Chroma Modulator Output
4 Ground
3 Duty Cycle Adjust
7 Color A Input
6 Color Reference Input
13
14
RF Tank

## MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| Rating | Value | Unit |
|---|---|---|
| Supply Voltage | 8.0 | Vdc |
| Operating Ambient Temperature Range | 0 to +70 | °C |
| Storage Temperature Range | −65 to +150 | °C |
| Junction Temperature | 150 | °C |
| Power Dissipation, Package<br>Derate above 25°C | 1.25<br>13 | Watts<br>mW/°C |

## RECOMMENDED OPERATING CONDITIONS

| | | |
|---|---|---|
| Supply Voltage | 5.0 | Vdc |
| Luma Input Voltage – Sync Tip<br>Peak White | 1.0<br>0.35 | Vdc |
| Color Reference Voltage | 1.5 | Vdc |
| Color A, B Input Voltage Range | 1.0 to 2.0 | Vdc |

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = +5 Vdc, $T_A$ = 25°C, Test Circuit 1 unless otherwise noted)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Operating Supply Voltage | 4.75 | 5.0 | 5.25 | Volts |
| Supply Current | – | 25 | – | mA |
| **CHROMA OSCILLATOR/CLOCK DRIVER** (Measured at Pin 1 unless otherwise noted) | | | | |
| Output Voltage ($V_{OL}$) | – | – | 0.4 | Vdc |
| ($V_{OH}$) | 2.4 | – | – | |
| Rise Time (V1 = 0.4 to 2.4 Vdc) | – | – | 50 | ns |
| Fall Time (V1 = 2.4 to 0.4 Vdc) | – | – | 50 | ns |
| Duty Cycle Adjustment Range (V3 = 5.0 Vdc)<br>(Measured at V1 = 1.4 V) | 70 | – | 30 | % |
| Inherent Duty Cycle (No connection to Pin 3) | – | 50 | – | % |
| **CHROMA MODULATOR** (V5 = V6 = V7 = 1.5 Vdc unless otherwise noted) | | | | |
| Input Common Mode Voltage Range (Pins 5, 6, 7) | 0.8 | – | 2.3 | Vdc |
| Oscillator Feedthrough (Measured at Pin 8) | – | 15 | 31 | mV(p-p) |
| Modulation Angle [θ8(V7 = 2.0 Vdc) – θ8(V5 = 2.0 Vdc)] | 85 | 100 | 115 | degrees |
| Conversion Gain [V8/(V7 – V6); V8/(V5 – V6)] | – | 0.6 | – | V(p-p)/Vdc |
| Input Current (Pins 5, 6, 7) | – | – | −20 | µA |
| Input Resistance (Pins 5, 6, 7) | 100 | – | – | kΩ |
| Input Capacitance (Pins 5, 6, 7) | – | – | 5.0 | pF |
| Chroma Modulator Linearity<br>(V5 = 1.0 to 2.0 V; V7 = 1.0 to 2.0 V) | – | 4.0 | – | % |
| **RF MODULATOR** | | | | |
| Luma Input Dynamic Range (Pin 9, Test Circuit 2) | 0 | – | 1.5 | Volts |
| RF Output Voltage (f = 67.25 MHz, V9 = 1.0 V) | – | 15 | – | mVrms |
| Luma Conversion Gain<br>(ΔV12/ΔV9; V9 = 0.1 to 1.0 Vdc) Test Circuit 2 | – | 0.8 | – | V/V |
| Chroma Conversion Gain<br>(ΔV12/ΔV10; V10 = 1.5 Vp-p; V9 = 1.0 Vdc) Test Circuit 2 | – | 0.95 | – | V/V |
| Chroma Linearity (Pin 12, V10 = 1.5 Vp-p) Test Circuit 2 | – | 1.0 | – | % |
| Luma Linearity (Pin 12, V9 = 0 to 1.5 Vdc) Test Circuit 2 | – | 2.0 | – | % |
| Input Current (Pin 9) | – | – | −20 | µA |
| Input Resistance (Pin 10) | – | 800 | – | Ω |
| Input Resistance (Pin 9) | 100 | – | – | kΩ |
| Input Capacitance (Pins 9, 10) | – | – | 5.0 | pF |
| Residual 920 kHz (Measured at Pin 12) See Note 1 | – | 50 | – | dB |
| Output Current (Pin 12, V9 = 0 V) Test Circuit 2 | – | 1.0 | – | mA |
| **TEMPERATURE CHARACTERISTICS** ($V_{CC}$ = 5 Vdc, $T_A$ = 0 to 70°C, IC only) | | | | |
| Chroma Oscillator Deviation ($f_o$ = 3.579545 MHz) | – | ±50 | – | Hz |
| RF Oscillator Deviation ($f_o$ = 67.25 MHz) | – | ±250 | – | kHz |
| Clock Drive Duty Cycle Stability | ±5.0 | – | – | % |

NOTE 1. V9 = 1.0 Vdc, $V_C$ = 300 mV(p-p) @ 3.58 MHz,
$V_S$ = 250 mV(p-p) @ 4.5 MHz, Source Impedance = 75 Ω.

FIGURE 2 – TEST CIRCUIT 1

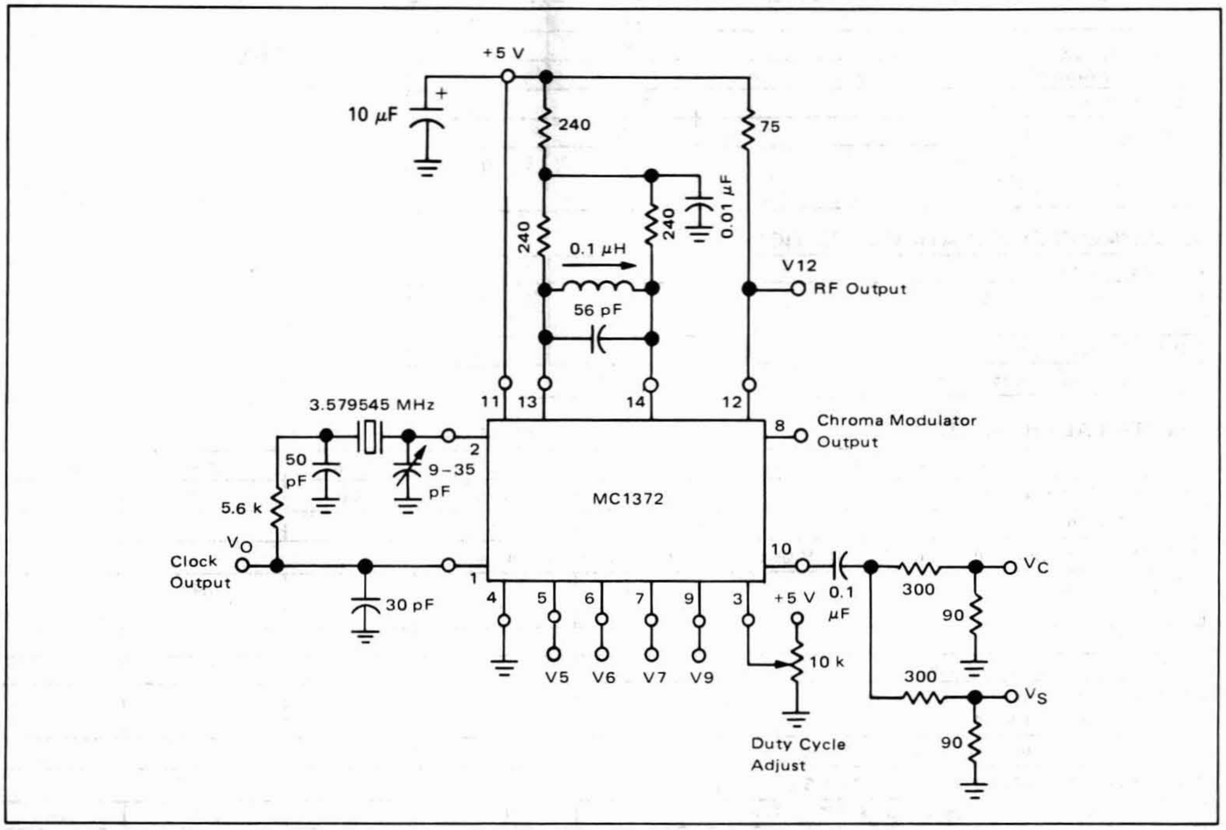

+5 V
10 µF
240
75
240
240
0.01 µF
0.1 µH
56 pF
V12
RF Output
3.579545 MHz
11
13
14
12
8
Chroma Modulator Output
2
50 pF
9–35 pF
5.6 k
MC1372
VO
Clock Output
1
30 pF
10
0.1 µF
300
VC
90
4
5
6
7
9
3
+5 V
10 k
V5
V6
V7
V9
300
VS
90
Duty Cycle Adjust

FIGURE 3 – TEST CIRCUIT 2

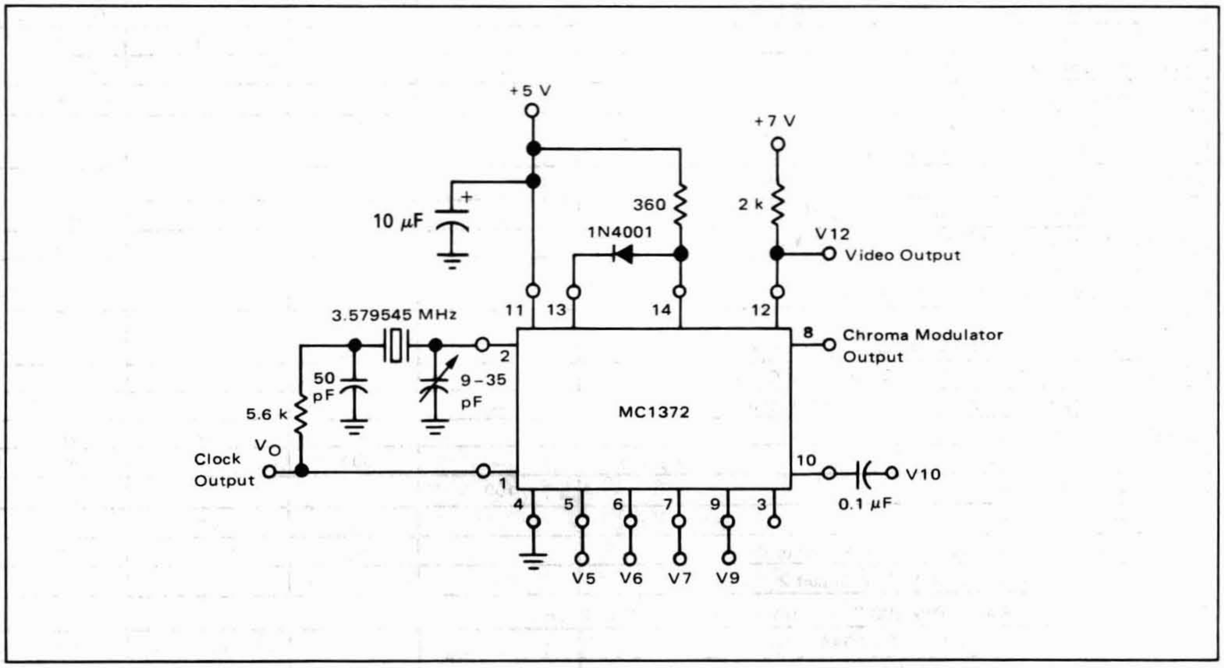
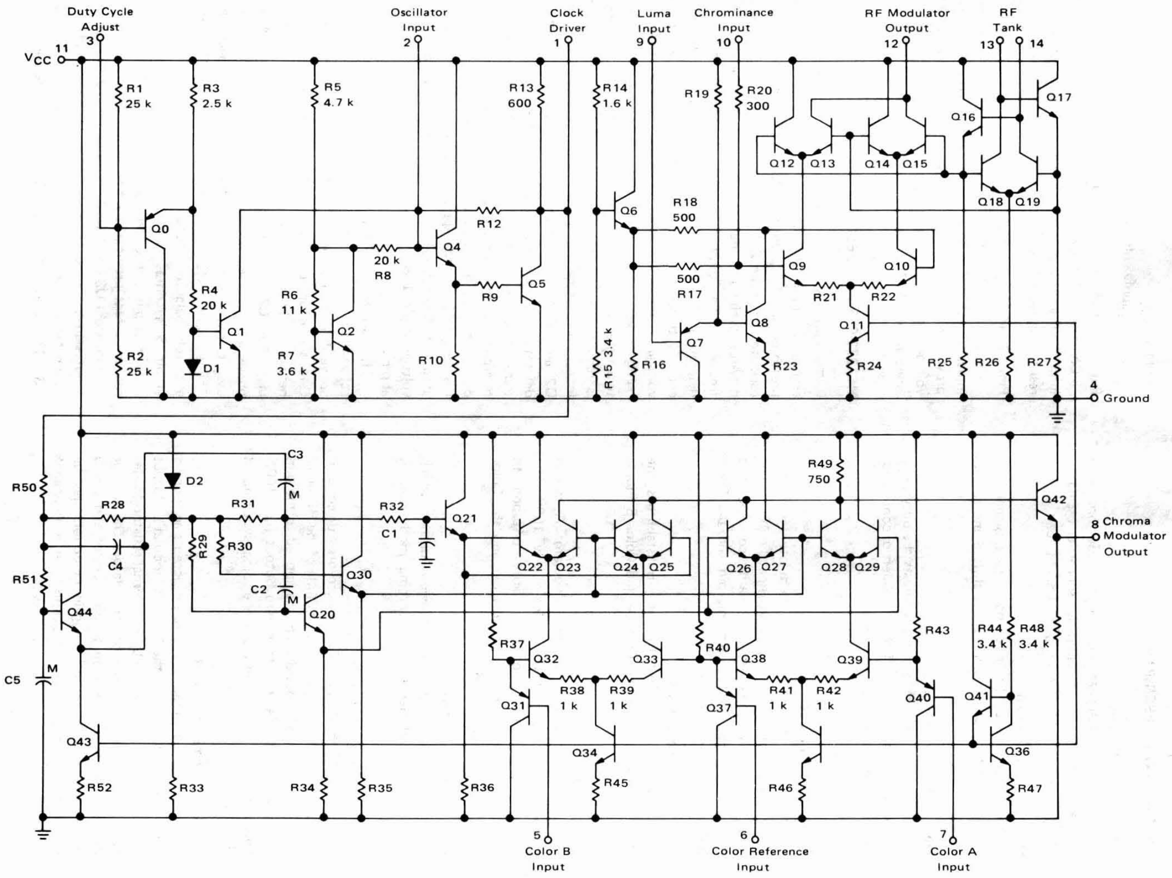

+5 V
+7 V
10 µF
360
2 k
1N4001
V12
Video Output
11
13
14
12
3.579545 MHz
8
Chroma Modulator Output
2
50 pF
9–35 pF
5.6 k
MC1372
VO
Clock Output
1
10
V10
0.1 µF
4
5
6
7
9
3
V5
V6
V7
V9

FIGURE 4 – SCHEMATIC DIAGRAM


Duty Cycle Adjust 3
Oscillator Input 2
Clock Driver 1
Luma Input 9
Chrominance Input 10
RF Modulator Output 12
RF Tank 13 14
VCC 11
R1 25 k
R3 2.5 k
R5 4.7 k
R13 600
R14 1.6 k
R19
R20 300
Q0
Q1
Q2
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
R12
20 k R8
R9
R18 500
500 R17
R21
R22
R4 20 k
R6 11 k
R7 3.6 k
R2 25 k
D1
R10
R15 3.4 k
R16
R23
R24
R25
R26
R27
4 Ground
R50
R28
R31
R32
C1
C3
M
D2
Q21
R29
R30
C4
C2
M
Q30
Q20
R51
Q44
C5
M
Q43
R52
R33
R34
R35
R36
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
R49 750
Q42
8 Chroma Modulator Output
R37
Q32
Q33
R38 1 k
R39 1 k
Q31
Q34
R45
R40
Q38
Q39
R41 1 k
R42 1 k
Q37
R46
R43
Q40
Q41
R44 3.4 k
R48 3.4 k
Q36
R47
5 Color B Input
6 Color Reference Input
7 Color A Input

## OPERATIONAL DESCRIPTION

**Pin 1 – Clock Output**

Provides a rectangular pulse output waveform with frequency equal to the chrominance subcarrier oscillator. This output is capable of driving one LS-TTL load.

**Pin 2 – Oscillator Input**

Color subcarrier oscillator feedback input. Signal from the clock output is externally phase shifted and ac coupled to this pin.

**Pin 3 – Duty Cycle Adjust**

A dc voltage applied to this pin adjusts the duty cycle of the clock output signal. If the pin is left unconnected, the duty cycle is approximately 50%.

**Pin 4 – Ground**

**Pin 5 – Color B Input**

Dc coupled input to Chroma Modulator B, whose phase leads modulator A by approximately 100°. The modulator output amplitude and polarity correspond to the voltage difference between this pin and the Color Reference Voltage at Pin 6.

**Pin 6 – Color Reference Input**

The dc voltage applied to this pin establishes the reference voltage to which Color A and Color B inputs are compared.

**Pin 7 – Color A Input**

Dc coupled input to Chroma Modulator A, whose phase lags modulator B by approximately 100°. The modulator output amplitude and polarity correspond to the voltage difference between this pin and the Color Reference Voltage at Pin 6.

**Pin 8 – Chroma Modulator Output**

Low impedance (emitter follower) output which provides the vectorial sum of chroma modulators A and B.

**Pin 9 – Luminance Input**

Input to RF modulator. This pin accepts a dc coupled luminance and sync signal. The amplitude of the RF signal output increases with positive voltage applied to the pin, and ground potential results in zero output (i.e., 100% modulation). A signal with positive-going sync should be used.

**Pin 10 – Chrominance Input**

Input to the RF modulator. This pin accepts ac coupled chrominance provided by the Chroma Modulator Output (pin 8). The signal is reduced by an internal resistor divider before being applied to the RF modulator. The resistor divider consists of a 300 ohm series resistor and a 500 ohm shunt resistor. Additional gain reduction may be obtained by the addition of external series resistance to pin 10.

**Pin 11 – $V_{CC}$**

Positive supply voltage

**Pin 12 – RF Modulator Output**

Common collector of output modulator stage. Output impedance and stage gain may be selected by choice of resistor connected between this pin and dc supply.

**Pins 13 and 14 – RF Tank**

A tuned circuit connected between these pins determines the RF oscillator frequency. The tuned circuit must provide a low dc resistance shunt. Applying a dc offset voltage between these pins results in baseband composite video at the RF Modulator Output.

## MC1372 CIRCUIT DESCRIPTION

The chrominance oscillator and clock driver consist of emitter follower Q4 and inverting amplifier Q5. Signal presented at clock driver output pin 1 is coupled to oscillator input pin 2 through an external RC and crystal network, which provides 180° phase shift at the resonant frequency. The duty cycle of the output waveform is determined by the dc component at pin 1 internally coupled through R12 to the base of Q4. As pin 1 dc voltage increases, a smaller portion of the sinusoidal feedback signal at pin 2 exceeds the Q4 base voltage of two times $V_{BE}$ required for conduction. As the dc level is reduced, device Q4 and thus Q5 is turned on for a longer percentage of the cycle. Transistors Q0, Q1, Q2 and diode D1 provide the biasing network which determines the dc operating level of the oscillator. The transistor Q2 and resistors R5, R6, and R7 form a voltage reference of four times $V_{BE}$ at the collector of Q2. The dc voltage at pin 1 is determined by the values of R4, R8, and R12 and the applied duty cycle adjust voltage at pin 3. Since these resistors are nominally equal, the voltage at pin 1 will always approximate the dc voltage at pin 3.

The oscillator signal at pin 1 is internally coupled to active filter Q44. This filter reduces the frequency content above 4 MHz. The output of the filter at the emitter of Q44 is ac coupled through C3 to the input of the lead/lag network. R32 and C1 provide approximately 50° of phase lag, while C2 and R29 provide approximately 50° of phase lead. These two quasi-quadrature waveforms are used to switch chroma modulators B and A, respectively. The transistors Q22 through Q25 and Q32–Q33 form a doubly balanced modulator. The input signal applied at pin 5 is compared to the color dc reference voltage applied at pin 6 in differential amplifier Q32–Q33. The source current provided by transistor Q34 is partitioned in transistors Q32 and Q33 according to the differential input signal. The bases of transistors Q23 and Q24 are connected to the dc reference voltage at the emitter of Q30. The bases of transistors Q22 and Q25 are connected to the phase delayed oscillator signal at the emitter of buffer transistor Q21. The differential signal currents provided by Q32 and Q33 are switched in transistors Q22 through Q25 and the resultant signal voltage is developed across R49. This signal has the phase and frequency of the oscillator signal at the emitter of Q21. The amplitude is proportional to the differential input signal applied between pins 5 and 6. Transistors Q26 through Q29 and Q38–Q39 form chroma modulator B. This modulator develops a signal voltage which is proportional to the differential voltage applied between pins 7 and 6. The phase and frequency of the output is equal to the phase advanced chroma oscillator at the emitter of buffer transistor Q20. Both chroma modulators A and B share the same output resistor, R49, so the output signal presented at the emitter of Q42 (pin 8) is the algebraic sum of modulators A and B.

The RF oscillator consists of differential amplifier Q18 and Q19 cross-coupled through emitter followers Q16 and Q17. The oscillator will operate at the parallel resonant frequency of the network connected between pins 13 and 14. The oscillator output is used to switch the doubly balanced RF modulator, Q9 through Q15. Transistors Q7 and Q8 provide level shifting and a high input impedance to the luminance input pin 9. The bases of transistors Q9 and Q10 are both biased through resistors R17 and R18, respectively, to the same dc reference voltage at Q6 emitter. The base voltage at Q10 may only be offset in a negative direction by luminance signal current source Q8. This design insures that overmodulation due to the luminance signal will never occur. The chrominance signal developed at pin 8 is externally ac coupled to pin 10 where it is reduced by resistor dividers R20 and R17, and added to the luminance signal in Q9. The resultant differential composite video currents are switched at the appropriate RF frequency in Q12 through Q15. The output signal current is presented at pin 12.

Transistors Q36, Q41 and resistors R44, R47 provide a highly stable voltage reference for biasing current sources Q43, Q34, Q35, and Q11.

## MC1372 APPLICATION INFORMATION

### Chrominance Oscillator

The oscillator is used as a clock signal for driving associated external circuitry, in addition to providing a switching signal for the chroma modulators. The IC uses an external crystal in a Colpitts configuration, as shown in Figure 5. Resistor R1 provides current limiting to reduce the signal swing. Capacitor C2 is adjusted for the exact frequency desired (3.579545 MHz).

In some applications, the duty cycle of the clock signal at pin 1 must be modified to overcome gate delays in associated equipment. The duty cycle may be adjusted by varying the dc voltage applied to pin 3. This adjustment may be made with the use of a potentiometer (10 kΩ) between supply and ground. With no connection to pin 3, the duty cycle is approximately 50%.

### Chroma Modulator

The chrominance oscillator is internally phase shifted and applied to chroma modulators A and B. No external lead/lag networks are necessary. The phase relationship between the modulators is approximately 100°, which was chosen to provide the best rendition of colors using equal amplitude color-difference signals. The voltage applied to pin 5, 6, or 7 must always be within the Input Common Mode Voltage Range. Since the amplitude of chrominance output is proportional to the voltage difference between pins 5 and 6 or 7 and 6, it is desirable to select the Color Reference Voltage applied to pin 6 to be midway between $V5_{max}$ and $V5_{min}$ (which should be $V7_{max}$ and $V7_{min}$). The Chroma B Modulator will be defined as a (B-Y) modulator if a burst flag signal is applied to the Color B Input (pin 5) at the appropriate time. This voltage should be negative with respect to the Color Reference Voltage, and typically has an amplitude equal to $1/2[V6-V5_{min}]$. Since the phase of burst is always defined as −(B-Y), the Chroma A Modulator approximates an (R-Y) modulator; however, the phase is offset by 10° from the nominal 90°, to provide the 100° phase shift as discussed previously.

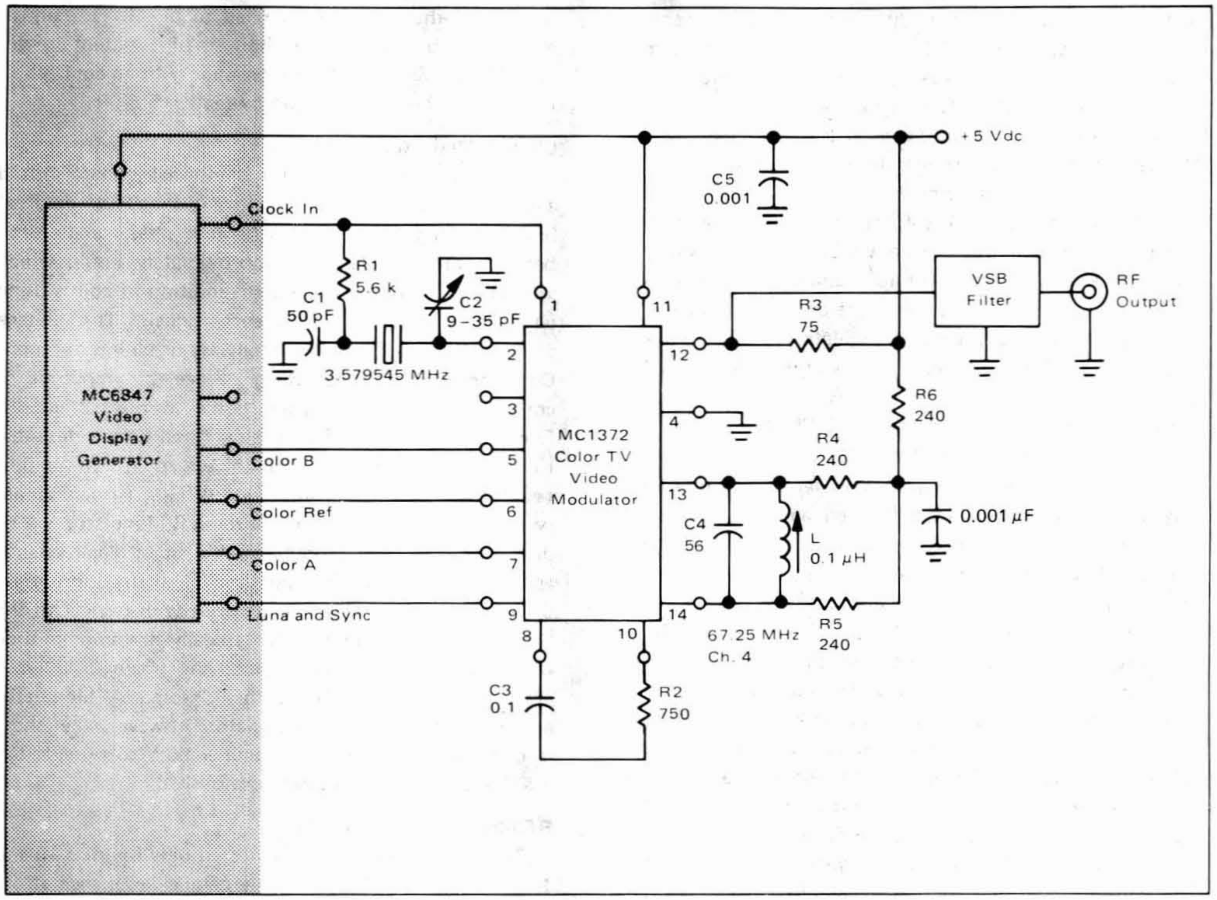
### RF Modulator and Oscillator

The coil and capacitor connected between pins 13 and 14 should be selected to have a parallel resonance at the carrier frequency of the desired TV channel. The values of 56 pF and 0.1 μH shown in Figure 5 were chosen for a Channel 4 carrier frequency of 67.25 MHz. For Channel 3 operation, the resonant frequency should be 61.25 MHz (C = 75 pF, L = 0.1 μH). Resistors R4 and R5 are chosen to provide an adequate amplitude of switching voltage, whereas R6 is used to lower the maximum dc level of switching voltage below $V_{CC}$, thus preventing saturation within the IC.

Composite Luminance and Sync should be dc coupled to Luminance Input, pin 9. This signal must be within the Luma Input Dynamic Range to insure linearity. Since an increase in dc voltage applied to pin 9 results in an increase in RF output, the input signal should have positive-going sync to generate an NTSC compatible signal. As long as the input signal is positive, overmodulation is prevented by the integrated circuit.

Chrominance information should be ac coupled to Chrominance Input, pin 10. This pin is internally connected to a resistor divider consisting of a series 300 ohms and a shunt 500 ohms resistor. The input impedance is thus 800 ohms, and a coupling capacitor should be appropriately chosen.

FIGURE 5 – TYPICAL APPLICATION CIRCUIT


+5 Vdc
C5
0.001
Clock In
R1
5.6 k
C1
50 pF
C2
9–35 pF
3.579545 MHz
MC6847
Video
Display
Generator
Color B
Color Ref
Color A
Luma and Sync
MC1372
Color TV
Video
Modulator
1
2
3
5
6
7
9
8
10
11
12
4
13
14
VSB
Filter
RF
Output
R3
75
R6
240
R4
240
0.001 μF
C4
56
L
0.1 μH
R5
240
67.25 MHz
Ch. 4
C3
0.1
R2
750

The Luminance to Chrominance ratio (L:C) may be modified with the addition of an external resistor in series with pin 10 (as shown in Figure 5). The unmodified L:C ($A_O$) is determined by the ratio of the respective Conversion Gain for equal amplitude signals (typically, 0.883 = −1.6 dB). The modified L:C will be governed by the equation $A_O(1 + R_{ext}/800)$ for equal amplitude input signals.

The internal chrominance modulators are not internally connected to the RF modulator; therefore, the user has the option of connecting an externally generated chrominance signal to the RF modulator. In addition, the RF modulator is wideband, and a 4.5 MHz FM audio signal may be added to the chrominance input at pin 10. This may be accomplished by selecting an appropriate series input resistor to provide the correct Luminance:Sound ratio.

The modulated RF signal is presented as a current at RF Modulator Output, pin 12. Since this pin represents a current source, any load impedance may be selected for matching purposes and gain selection, as long as the voltage at pin 12 is high enough to prevent the output devices from reaching saturation (approximately 4.5 V with components in Figure 5). The peak current out of pin 12 is typically 2 mA. Hence, a load resistance of up to 250 ohms may be safely used with a 5 V supply.

**Composite Video Signal Generation**

The RF modulator may be easily used as a composite video generator by replacing the RF oscillator tank circuit with a diode as shown in Figure 3. This results in the output modulator being biased so the summation of luminance and chrominance appears unswitched at pin 12. The polarity of the output waveform is controlled by the direction of the diode. *Inverted video:* Anode to pin 14, cathode to pin 13. *Non-inverted video:* Anode to pin 13, cathode to pin 14. Note that the supply resistor must always be connected to the anode of the diode.

The amplitude of signal may be increased by increasing the load resistor on pin 12 and returning it to a higher supply voltage. Any voltage up to the Absolute Maximum Rating may be used.

### Applications with MC6847 Video Display Generator

The MC1372 may be easily interfaced to the MC6847 as shown in Figure 5. The dc levels generated and required by the VDG are compatible with the MC1372, so that pins 1, 5, 6, 7, and 9 may be directly coupled to the appropriate MC6847 pins. Both integrated circuits as well as any associated NMOS MPU may be driven from a common 5 Vdc supply.

### Recommended Chroma-Luma Signals

A chroma modulation angle of 100° was chosen to facilitate a desirable selection of colors with a minimum number of input signal levels. The following table demonstrates applicable signal levels for a variety of colors.

RECOMMENDED CHROMA-LUMA SIGNALS

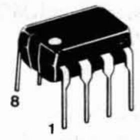
| | Pin #9 Luminance Input (Vdc) | Pin #7 Color A (Vdc) | Pin #6 Color Ref. (Vdc) | Pin #5 Color B (Vdc) |
|---|---|---|---|---|
| **Sync** | 1.0 | 1.5 | 1.5 | 1.5 |
| **Blanking** | 0.75 | 1.5 | 1.5 | 1.5 |
| **Burst** | 0.75 | 1.5 | 1.5 | 1.25 |
| **Black** | 0.70 | 1.5 | 1.5 | 1.5 |
| **Green** | 0.50 | 1.0 | 1.5 | 1.0 |
| **Yellow** | 0.38 | 1.5 | 1.5 | 1.0 |
| **Blue** | 0.62 | 1.5 | 1.5 | 2.0 |
| **Red** | 0.62 | 2.0 | 1.5 | 1.5 |
| **Cyan** | 0.50 | 1.0 | 1.5 | 1.5 |
| **Magenta** | 0.50 | 2.0 | 1.5 | 2.0 |
| **Orange** | 0.50 | 2.0 | 1.5 | 1.0 |
| **Buff** | 0.38 | 1.5 | 1.5 | 1.5 |

**MOTOROLA**

# MC1373

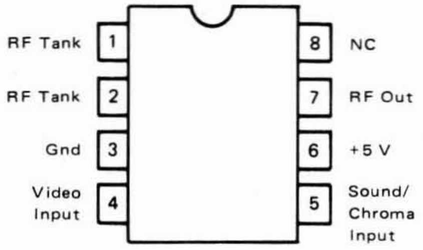
## TV VIDEO MODULATOR CIRCUIT

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

**PIN CONNECTIONS**


RF Tank 1
RF Tank 2
Gnd 3
Video Input 4
8 NC
7 RF Out
6 +5 V
5 Sound/ Chroma Input

## TV VIDEO MODULATOR

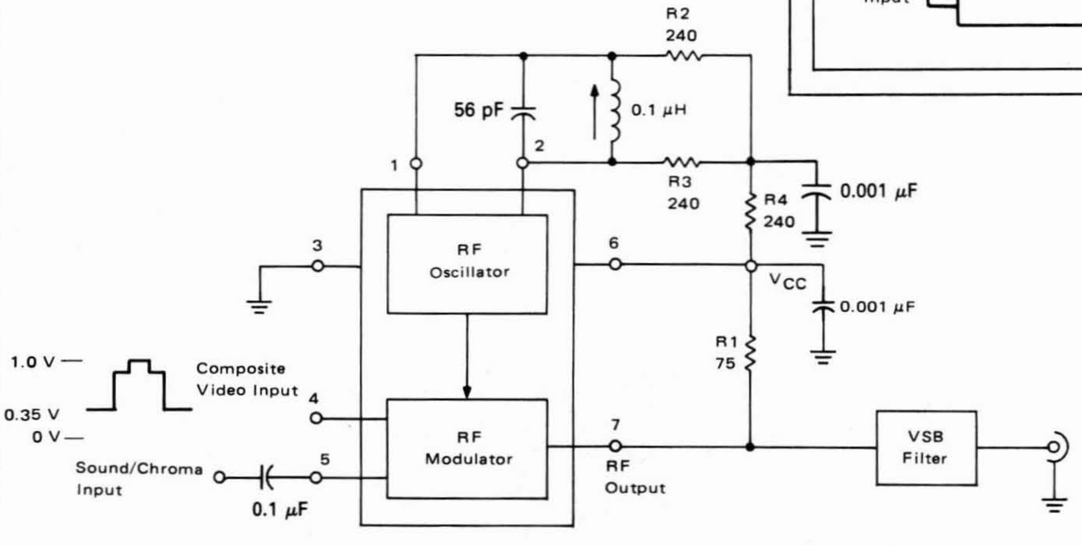
. . . an RF oscillator and dual-input modulator to generate a TV signal from baseband video inputs.

Applications include video games, home computer display, video tape recorders, and test equipment.

The very low level of intermodulation products, compact package and small external component count make this device superior to simple discrete circuits.

- Single 5.0 Vdc Supply
- Channel 3 or 4 Operation
- Excellent Oscillator Stability to 100 MHz
- Color and Sound Compabitility
- Dual Input Modulator for Ease of Signal Handling
- Low Intermodulation (−50 dB 920 kHz Beat)
- Overmodulation Protection

FIGURE 1 — BLOCK DIAGRAM AND APPLICATION CIRCUIT


R2
240
56 pF
0.1 µH
1
2
R3
240
R4
240
0.001 µF
3
RF Oscillator
6
VCC
0.001 µF
R1
75
1.0 V
0.35 V
0 V
Composite Video Input
4
RF Modulator
7
Sound/Chroma Input
5
0.1 µF
RF Output
VSB Filter

## MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| Rating | Value | Unit |
|---|---|---|
| Supply Voltage | 8.0 | Vdc |
| Operating Ambient Temperature Range | 0 to +70 | °C |
| Storage Temperature Range | −65 to +150 | °C |
| Junction Temperature | 150 | °C |
| Power Dissipation, Package<br>Derate above 25°C | 1.25<br>10 | Watts<br>mW/°C |

## RECOMMENDED OPERATING CONDITIONS

| | | |
|---|---|---|
| Supply Voltage | 5.0 | Vdc |
| Luma Input Voltage — Sync Tip<br>Peak White | 1.0<br>0.35 | Vdc |

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = +5 Vdc, $T_A$ = 25°C, Test Circuit 1 unless otherwise noted)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Operating Supply Voltage | 4.75 | 5.0 | 5.25 | Volts |
| Supply Current | — | 12 | — | mA |
| **RF MODULATOR** | | | | |
| Luma Input Dynamic Range (Pin 4, Test Circuit 2) | 0 | — | 1.5 | Volts |
| RF Output Voltage (f = 67.25 MHz, V4 = 1.0 V) | — | 15 | — | mVrms |
| Luma Conversion Gain ($\Delta V7/\Delta V4$, V4 = 0.1 to 1.0 Vdc) Test Circuit 2 | — | 0.8 | — | V/V |
| Chroma Conversion Gain ($\Delta V7/\Delta V5$; V5 = 1.5 Vp-p;V4 = 1.0 Vdc) Test Circuit 2 | — | 0.95 | — | V/V |
| Chroma Linearity (Pin 7, V5 = 1.5 Vp-p) Test Circuit 2 | — | 1.0 | — | % |
| Luma Linearity (Pin 7, V4 = 0 to 1.5 Vdc) Test Circuit 2 | — | 2.0 | — | % |
| Input Current (Pin 4) | — | — | −20 | µA |
| Input Resistance (Pin 5) | — | 800 | — | Ω |
| Input Resistance (Pin 4) | 100 | — | — | kΩ |
| Input Capacitance (Pins 4, 5) | — | — | 5.0 | pF |
| Residual 920 kHz (Measured at Pin 7) See Note 1 | — | 60 | — | dB |
| Output Current (Pin 7, V4 = 0 V) Test Circuit 2 | — | 1.5 | — | mA |
| **TEMPERATURE CHARACTERISTICS** ($V_{CC}$ = 5 Vdc, $T_A$ = 0 to 70°C, IC only) | | | | |
| RF Oscillator Deviation ($f_o$ = 67.25 MHz) | — | ±250 | — | kHz |

NOTE 1. RF Reference Level = 6.0 mV @ Pin 7. Load Impedance = 75 Ω.
RF + 4.5 MHz = −13 dB.
RF + 3.58 MHz = −20 dB.

FIGURE 2 — TEST CIRCUIT 1

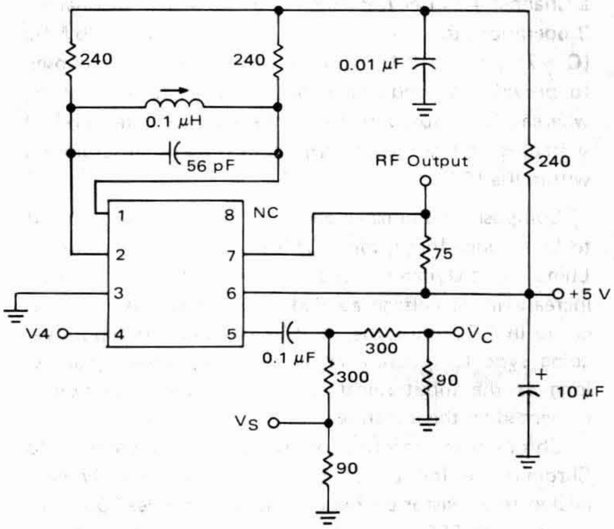


FIGURE 3 — TEST CIRCUIT 2

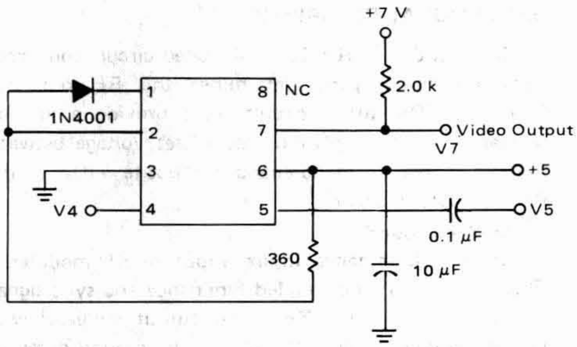
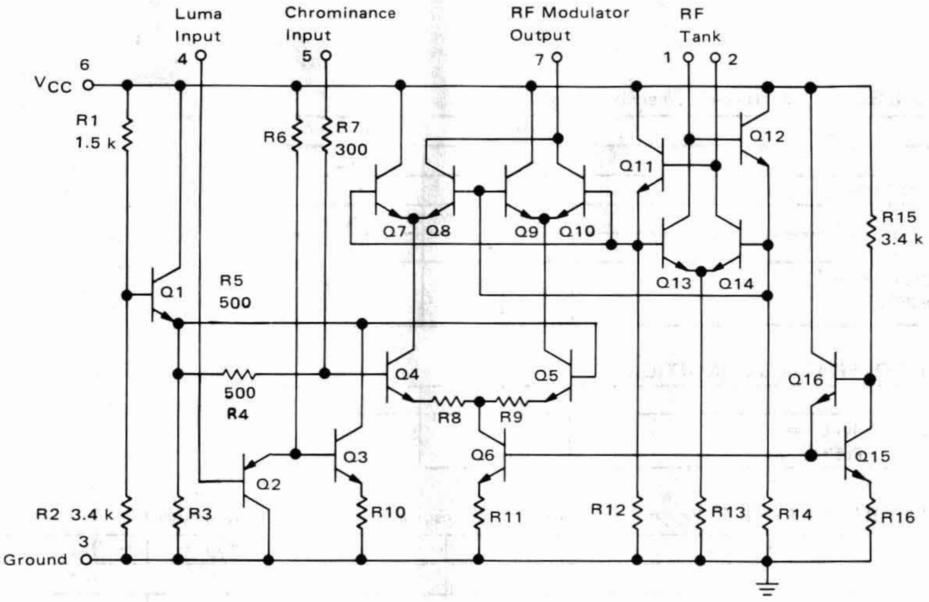


FIGURE 4 – SCHEMATIC DIAGRAM



## SCHEMATIC DESCRIPTION

The RF oscillator consists of differential amplifier Q13 and Q14 cross-coupled through emitter followers Q11 and Q12. The oscillator will operate at the parallel resonant frequency of the network connected between pins 1 and 2. The oscillator output is used to switch the doubly balanced RF modulator, Q4 through Q10. Transistors Q2 and Q3 provide level shifting and a high input impedance to the luminance input pin 4. The bases of transistors Q4 and Q5 are both biased through resistors R4 and R5, respectively, to the same dc reference voltage at Q1 emitter. The base voltage at Q5 may only be offset in a negative direction by luminance signal current source Q3. This design insures that overmodulation due to the luminance signal will never occur. The chrominance signal is externally ac coupled to pin 5 where it is reduced by resistor dividers R7 and R4, and added to the luminance signal in Q4. The resultant differential composite video currents are switched at the appropriate RF frequency in Q7 through Q10. The output signal current is presented at pin 7.

Transistors Q15, Q16 and resistors R15, R16 provide a highly stable voltage reference for biasing the current source Q6.

## OPERATIONAL DESCRIPTION

**Pins 1 and 2 – RF Tank.** A tuned circuit connected between these pins determines the RF oscillator frequency. The tuned circuit must provide a low dc resistance shunt. Applying a dc offset voltage between these pins results in baseband composite video at the RF Modulator Output.

**Pin 3 – Ground.**

**Pin 4 – Luminance Input.** Input to RF modulator. This pin accepts a dc coupled luminance and sync signal. The amplitude of the RF signal output increases with positive voltage applied to the pin, and ground potential results in zero output (i.e., 100% modulation). A signal with positive-going sync should be used.

**Pin 5 – Chrominance/Sound Input.** Input to the RF modulator. This pin accepts an ac coupled chrominance signal. The signal is reduced by an internal resistor divider before being applied to the RF modulator. The resistor divider consists of a 300 ohm series resistor and a 500 ohm shunt resistor. A 4.5 MHz FM audio signal may be added to the input by selecting an appropriate series input resistor to provide the correct Luminance:Sound ratio.

**Pin 6 – $V_{CC}$.** Positive supply voltage.

**Pin 7 – RF Modulator Output.** Common collector of output modulator stage. Output impedance and stage gain may be selected by choice of resistor connected between this pin and dc supply.

**Pin 8 – No Connection.**

## APPLICATIONS INFORMATION (Refer to Figure 1)

### RF Modulator and Oscillator

The coil and capacitor connected between pins 1 and 2 should be selected to have a parallel resonance at the carrier frequency of the desired TV channel. The values of 56 pF and 0.1 μH shown in Figure 1 were chosen for a Channel 4 carrier frequency of 67.25 MHz. For Channel 3 operation, the resonant frequency should be 61.25 MHz (C = 75 pF, L = 0.1 μH). Resistors R2 and R3 are chosen to provide an adequate amplitude of switching voltage, whereas R4 is used to lower the maximum dc level of switching voltage below $V_{CC}$, thus preventing saturation within the IC.

Composite Luminance and Sync should be dc coupled to Luminance Input, pin 4. This signal must be within the Luma Input Dynamic Range to insure linearity. Since an increase in dc voltage applied to pin 4 results in an increase in RF output, the input signal should have positive-going sync to generate an NTSC compatible signal. As long as the input signal is positive, overmodulation is prevented by the integrated circuit.

Chrominance information should be ac coupled to Chrominance Input, pin 5. This pin is internally connected to a resistor divider consisting of a series 300 ohms and a shunt 500 ohms resistor. The input impedance is thus 800 ohms, and a coupling capacitor should be appropriately chosen.

**MOTOROLA**

# MC1374

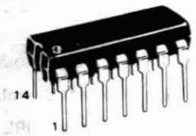
## TV MODULATOR CIRCUIT

The MC1374 includes an FM audio modulator, sound carrier oscillator, RF oscillator, and RF dual input modulator. It is designed to generate a TV signal from audio and video inputs. The MC1374's wide dynamic range and low distortion audio make it particularly well suited for applications such as video tape recorders, video disc players, T.V. games and subscription decoders.

- Single Supply, 5 V to 12 V
- Channel 3 or 4 Operation
- Variable Gain RF Modulator
- Wide Dynamic Range
- Low Intermodulation Distortion
- Positive or Negative Sync
- Low Audio Distortion
- Few External Components

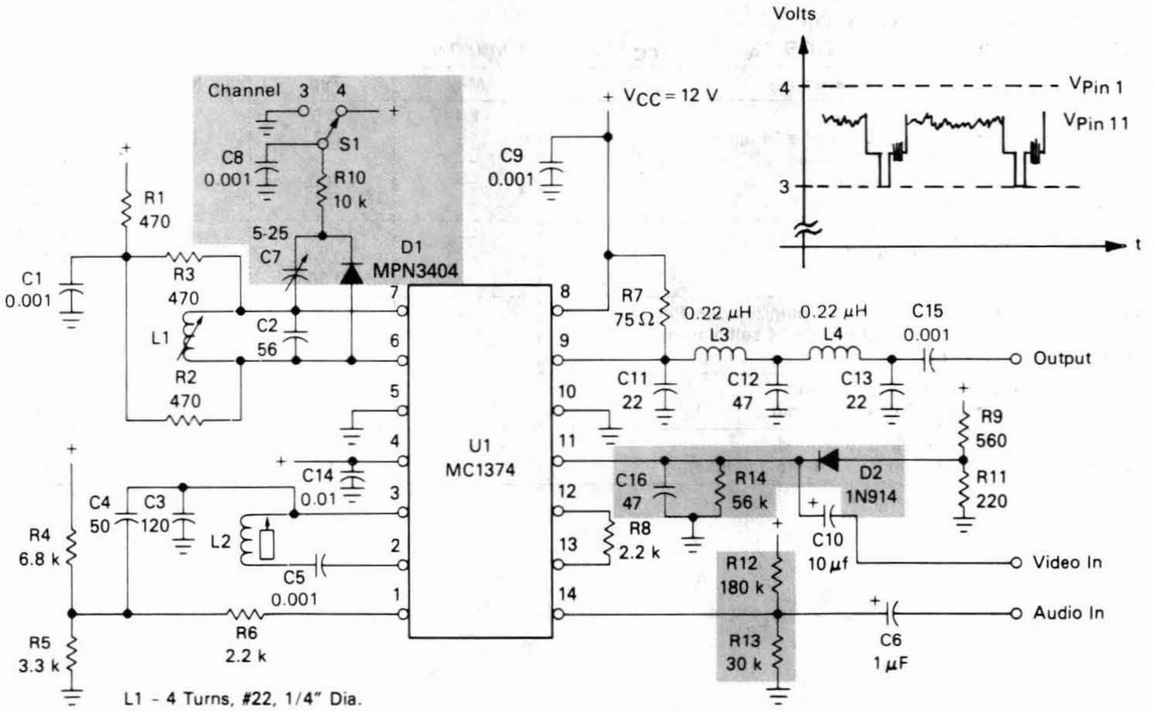
## TV MODULATOR CIRCUIT

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

FIGURE 1 — TYPICAL APPLICATION


Volts
4
3
VPin 1
VPin 11
t
Channel 3 4
S1
C8
0.001
R10
10 k
5-25
C7
D1
MPN3404
+ VCC = 12 V
C9
0.001
R1
470
C1
0.001
R3
470
L1
C2
56
R2
470
7
6
5
4
3
2
1
8
9
10
11
12
13
14
U1
MC1374
R7
75 Ω
0.22 µH
L3
0.22 µH
L4
C15
0.001
Output
C11
22
C12
47
C13
22
R9
560
R11
220
C16
47
R14
56 k
D2
1N914
R8
2.2 k
C10
10 µf
Video In
R12
180 k
R13
30 k
C6
1 µF
Audio In
C14
0.01
C4
50
C3
120
L2
C5
0.001
R4
6.8 k
R5
3.3 k
R6
2.2 k

L1 - 4 Turns, #22, 1/4" Dia.
L2 - 40 Turns, #36, 3/16" Dia.

**Shaded Parts Optional**

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Value | Unit |
|---|---|---|
| Supply Voltage | 14 | Vdc |
| Operating Ambient Temperature Range | 0 to +70 | °C |
| Storage Temperature Range | -65 to +150 | °C |
| Junction Temperature | 150 | °C |
| Power Dissipation, Package<br>Derate above 25°C | 1.25<br>10 mW/°C | Watts |

## AM OSCILLATOR/MODULATOR ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 12 Vdc, $T_A$ = 25°C, $f_c$ = 67.25 MHz, Figure 4 circuit, unless noted)

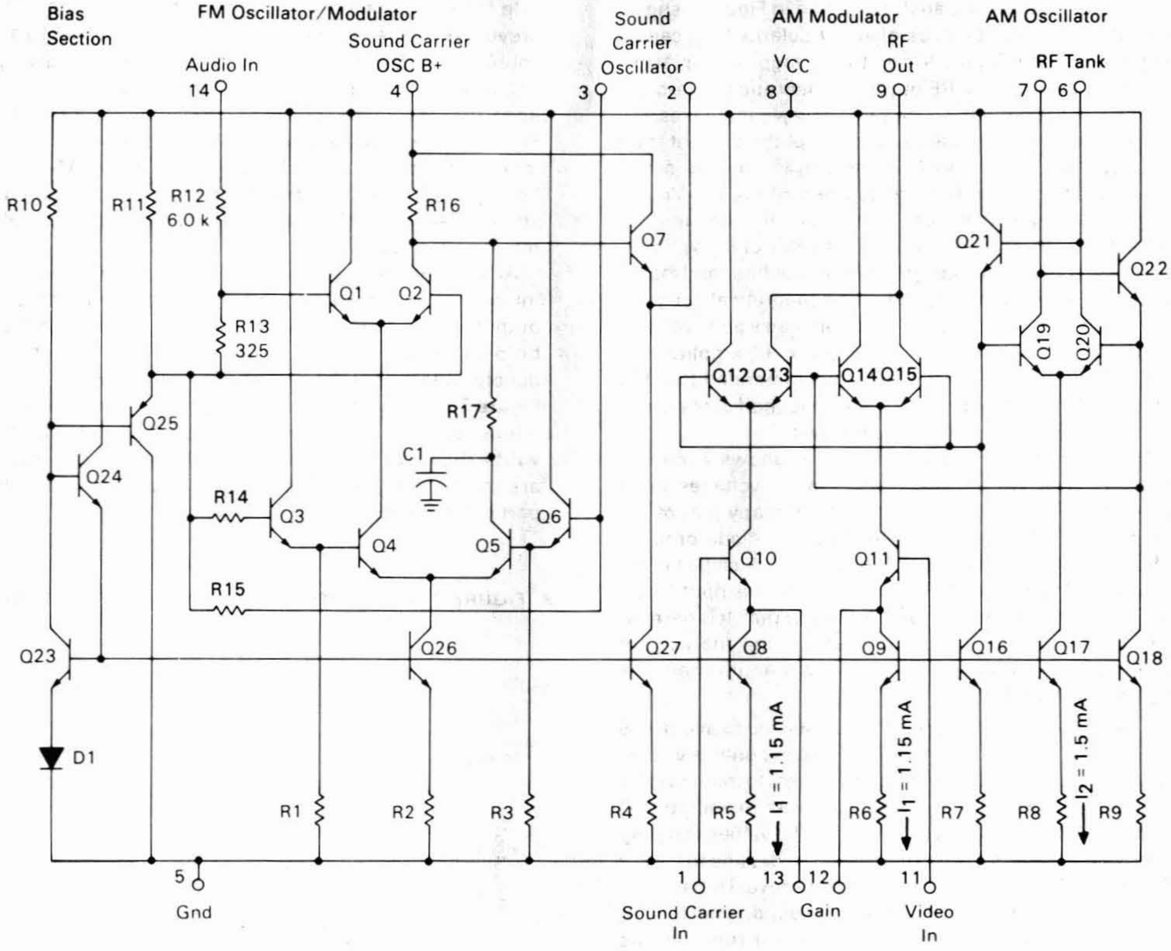
| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Operating Supply Voltage | 5.0 | 12 | 12 | V |
| Supply Current (Figure 1) | — | 13 | — | mA |
| Video Input Dynamic Range (Sync Amplitude) | 0.25 | 1.0 | 1.0 | V Pk |
| RF Output (Pin 9, R7 = 75 Ω, No External Load) | — | 170 | — | mV pp |
| Carrier Suppression | 36 | 40 | — | dB |
| Linearity (75% to 12.5% Carrier, 15 kHz to 3.58 MHz) | — | — | 2.0 | % |
| Differential Gain Distortion (IRE Test Signal) | 5.0 | 7.0 | 10 | % |
| Differential Phase Distortion (3.58 MHz IRE Test Signal) | — | 1.5 | 2.0 | Degrees |
| 920 kHz Beat (3.58 MHz @ 30%, 4.5 MHz @ 25%) | — | -57 | — | dB |
| Video Bandwidth (75 Ω Input Source) | 30 | — | — | MHz |
| Oscillator Frequency Range | — | 105 | — | MHz |
| Internal Resistance across Tank (Pin 6 to Pin 7) | — | 1.8 | — | kΩ |
| Internal Capacitance across Tank (Pin 6 to Pin 7) | — | 4.0 | — | pF |

## FM OSCILLATOR/MODULATOR ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C, $V_{CC}$ = 12 Vdc, 4.5 MHz, Test circuit of Figure 11 unless noted)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Frequency Range of Modulator | 1.4 | 4.5 | 14 | MHz |
| Frequency Shift versus Temperature (Pin 14 open) | — | 0.2 | 0.3 | kHz/°C |
| Frequency Shift versus $V_{CC}$ (Pin 14 open) | — | — | 4.0 | kHz/V |
| Output Amplitude (Pin 3 not loaded) | — | 900 | — | mVp-p |
| Output Harmonics, Unmodulated | — | — | -40 | dB |
| Modulation Sensitivity 1.7 MHz | — | 0.20 | — | MHz/V |
| 4.5 MHz | — | 0.24 | — | MHz/V |
| 10.7 MHz | — | 0.80 | — | MHz/V |
| Audio Distortion (±25 kHz Deviation ,Optimized Bias Pin 14) | — | 0.6 | 1.0 | % |
| Audio Distortion (±25 kHz Deviation, Pin 14 self biased) | — | 1.4 | — | |
| Incidental AM (±25 kHz FM) | — | 2.0 | — | |
| Audio Input Resistance (Pin 14 to ground) | — | 6.0 | — | kΩ |
| Audio Input Capacitance (Pin 14 to ground) | — | 5.0 | — | pF |
| Stray Tuning Capacitance (Pin 3 to ground) | — | 5.0 | — | pF |
| Effective Oscillator Source Impedance (Pin 3 to load) | — | 2.0 | — | kΩ |

FIGURE 2 — TV MODULATOR


Bias Section
FM Oscillator/Modulator
Audio In
14
Sound Carrier OSC B+
4
Sound Carrier Oscillator
3
2
AM Modulator
VCC
8
RF Out
9
AM Oscillator
RF Tank
7
6
R10
R11
R12 6.0 k
R13 325
R16
R17
C1
R14
R15
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
D1
R1
R2
R3
R4
R5
R6
R7
R8
R9
I1 = 1.15 mA
I1 = 1.15 mA
I2 = 1.5 mA
5
Gnd
1
Sound Carrier In
13
12
Gain
11
Video In

## GENERAL DESCRIPTION

The MC1374 contains an RF oscillator, RF modulator, and a phase-shift type FM modulator, arranged to permit good printed circuit layout of a complete T.V. modulation system. The RF oscillator is similar to the one used in MC1372 and MC1373, and is coupled internally in the same way. It's frequency is controlled by an external tank on Pins 6 and 7, or by a crystal circuit, and will operate to approximately 105 MHz. The video modulator is a balanced type as used in the well known MC1496. Modulated sound carrier and composite video information can be put in separately on pins 1 and 11 to minimize unwanted crosstalk. A single resistor on Pins 12 and 13 is selected to set the modulator gain. The RF output at Pin 9 is a current source which drives a load connected from Pin 9 to $V_{CC}$.

The FM system was designed specifically for the T.V. intercarrier function. For circuit economy, one phase shift circuit was built into the chip. Still, it will operate from 1.4 MHz to 14 MHz, low enough to be used in a cordless telephone base station (1.76 MHz), and high enough to be used as an FM IF test signal source (10.7 MHz). At 4.5 MHz, a deviation of ±25 kHz can be achieved with 0.6% distortion (typical).

In the circuit above devices Q1 through Q7 are active in the oscillator function. Differential amplifier Q3, Q4, Q5, and Q6 acts as a gain stage, sinking current from input section Q1, Q2 and the phase shift network R17, C1. Input amplifier Q1, Q2 can vary the amount of "in phase" Q4 current to be combined with phase shifter current in load resistor R16. The R16 voltage is applied to emitter follower Q7 which drives an external L-C circuit. Feedback from the center of the L-C circuit back to the base of Q6 closes the loop. As audio input is applied which would offset the stable oscillatory phase, the frequency changes to counteract. The input to Pin 14 can include a dc feedback current for AFC over a limited range.

The modulated FM signal from Pin 3 is coupled to Pin 1 of the RF modulator and is then modulated onto the AM carrier.

## THE AM SECTION

The AM modulator transfer function in Figure 3 shows that the video input can be of either polarity (and can be applied at either input). When the voltages on Pin 1 and Pin 11 are equal, the RF output is theoretically zero. As the difference between $V_{Pin\ 11}$ and $V_{Pin\ 1}$ increases, the RF output increases linearly until all of the current from both $I_1$ current sources (Q8 and Q9) is flowing in one side of the modulator. This occurs when $\pm(V_{Pin\ 11} - V_{Pin\ 1}) = I_1 R_G$, where $I_1$ is typically 1.15 mA. The peak-to-peak RF output is then $2I_1 R_L$. Usually the value of $R_L$ is chosen to be 75Ω to ease the design of the output filter and match into T.V. distribution systems. The theoretical range of input voltage and $R_G$ is quite wide, but noise and available sound level limit the useful video (sync tip) amplitude to between 0.25 and 1.0 Vpk. It is recommended that the value of $R_G$ be chosen so that only about half of the dynamic range will be used at sync tip level.

The operating window of Figure 5 shows a cross--hatched area where Pin 1 and Pin 11 voltages must always be in order to avoid saturation in any part of the modulator. (The letter $\phi$ represents one diode drop, or about 0.75 V.) The oscillator Pins 6 and 7 must be biased to a level of $V_{CC} - \phi - 2I_1 R_L$ (or lower) and the input Pins 1 and 11 must always be at least $2\phi$ below that. It is permissible to operate down to 1.6 V, saturating the current sources, but whenever possible, the minimum should be $3\phi$ above ground.

The oscillator will operate dependably up to about 105 MHz with a broad range of tank circuit components values. It is desirable to use a small L and a large C to minimize the dependence on I.C. internal capacitance. An operating Q between 10 and 20 is recommended. The values of $R_1$, $R_2$ and $R_3$ are chosen to produce the desired Q and to set the Pin 6 and 7 d.c. voltage as discussed above. Unbalanced operation; i.e., Pin 6 or 7 bypassed to ground, is not recommended. Although the oscillator will still run, and the modulator will produce a useable signal, this mode causes substantial base-band video feedthrough. Bandswitching, as Figure 1 shows, can still be accomplished economically without using the unbalanced method.

The oscillator frequency with respect to temperature in the test circuit shows less than ±20 kHz total shift from 0°C to 50°C as shown in Figure 7. At higher temperatures the slope approaches 2.0 kHz/°C. Improvement in this region would require a temperature compensating tuning capacitor of the N75 family.

Crystal control is feasible using the circuit shown in Figure 21. The crystal is a 3rd overtone series type, used in series resonance. The L1, C2 resonance is adjusted well below the crystal frequency and is sufficiently tolerant to permit fixed values. A frequency shift versus temperature of less than 1.0 Hz/°C can be expected from this approach. The resistors Ra and Rb are to suppress parasitic resonances.

Coupling of output RF to wiring and components on Pins 1 and 11 can cause as much as 300 kHz shift in carrier (at 67 MHz) over the video input range. A careful layout can keep this shift below 10 kHz. Oscillator may also be inadvertently coupled to the RF output, with the undesired effect of preventing a good null when $V_{11} = V_1$. Reasonable care will yield carrier rejection ratios of 36 to 40 dB below sync tip level carrier.

In television, one of the most serious concerns is the prevention of the intermodulation of color (3.58 MHz) and sound (4.5 MHz) frequencies, which causes a 920 kHz signal to appear in the spectrum. Very little (3rd order) nonlinearity is needed to cause this problem. The results in Figure 6 are unsatisfactory, and demonstrate that too much of the available dynamic range of the MC1374 has been used. Figures 8 and 10 show that by either reducing standard signal level, or reducing gain, acceptable results may be obtained.

At VHF frequencies, small imbalances within the device introduce substantial amounts of 2nd harmonic in the RF output. At 67 MHz, the 2nd harmonic is only 6 to 8 dB below the maximum fundamental. For this reason a double pi low pass filter is shown in the test circuit of Figure 3 and works well for channel 3 and 4 lab work. For a fully commercial application, a vestigial sideband filter will be required. The general form and approximate values are shown in Figure 19. It must be exactly aligned to the particular channel.

FIGURE 3 — AM MODULATOR TRANSFER FUNCTION

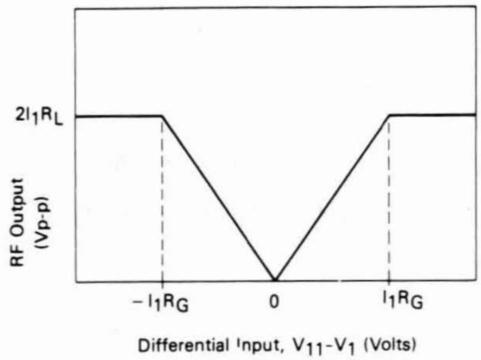


FIGURE 4 — AM TEST CIRCUIT

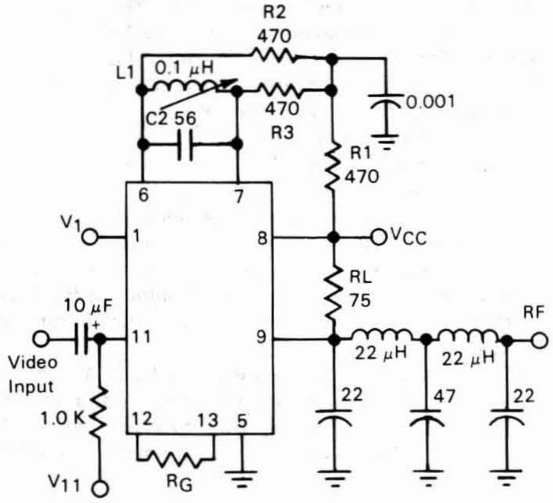


FIGURE 5 — THE OPERATING WINDOW

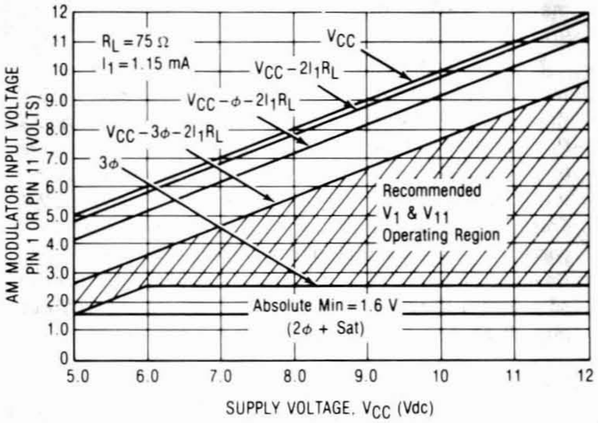


FIGURE 6 — 920 kHz BEAT

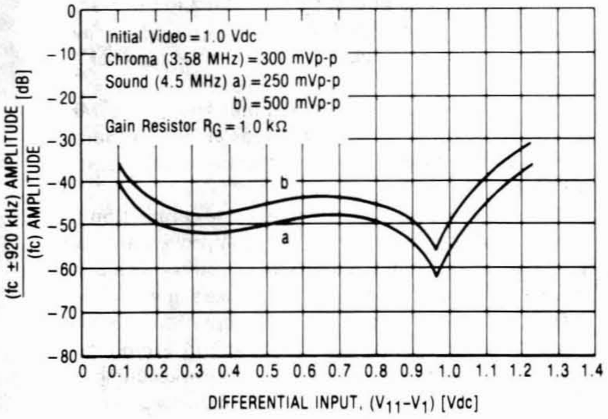


FIGURE 7 — RF OSCILLATOR FREQUENCY versus TEMPERATURE

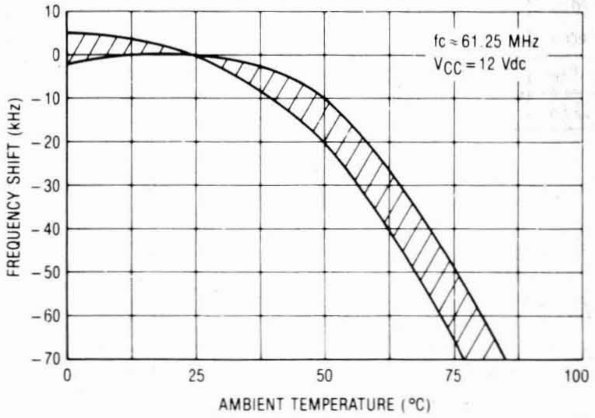


FIGURE 8 — 920 kHz BEAT

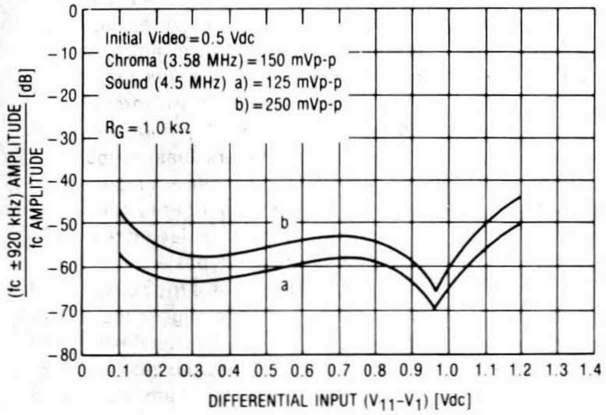


FIGURE 9 — RF OSCILLATOR FREQUENCY versus SUPPLY VOLTAGE

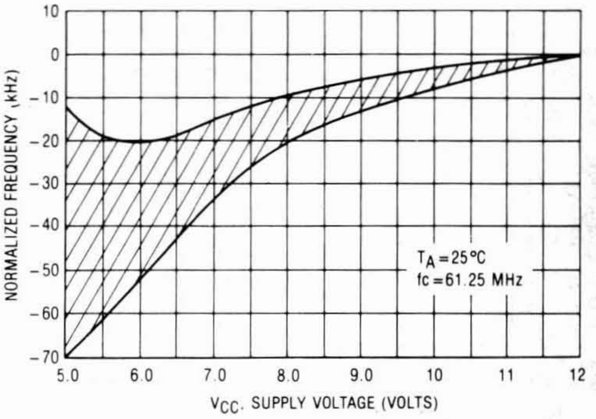
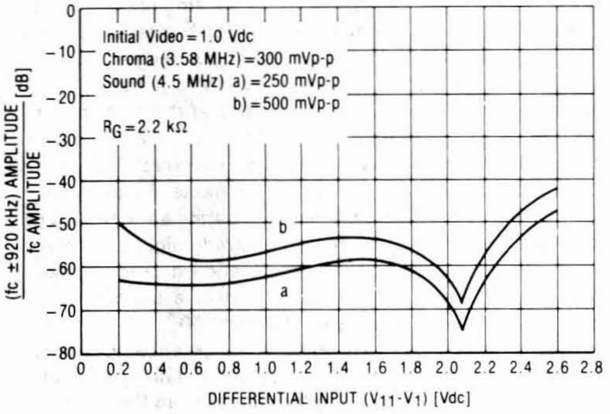


FIGURE 10 — 920 kHz BEAT



## FM SECTION

The oscillator center frequency is approximately the resonance of the inductor $L_2$ from Pin 2 to Pin 3 and the effective capacitance $C_3$ from Pin 3 to ground. For overall oscillator stability, it is best to keep $X_L$ in the range of 300 Ω to 1.0 kΩ.

The modulator transfer characteristic at 4.5 MHz is shown in Figure 15. Transfer curves at other frequencies have a very similar shape, but differ in deviation per input volt, as shown in Figures 13 and 17.

Most applications will not require dc connection to the audio input, Pin 14. However, some improvements can be achieved by the addition of biasing circuitry. The unaided device will establish its own Pin 14 bias at 4 $\theta$, or about 3.0 V. This bias is a little too high for optimum modulation linearity. Figure 14 shows better than 2-to-1 improvement in distortion between the unaided device and pulling Pin 14 down to 2.6 to 2.7 V. This can be accomplished by a simple divider, if the supply voltage is relatively constant.

The impedance of the divider has a bearing on the frequency versus temperature stability of the FM system. A divider of 180 kΩ and 30 kΩ (for $V_{CC}$ = 12 V) will give good temperature stabilization results. However, as Figure 18 shows, a divider is not a good method if the supply voltage varies. The designer must make the decisions here, based on considerations of economy, distortion and temperature requirements and power supply capability. If the distortion requirements are not stringent, then no bias components are needed. If, in this case, the temperature compensation needs to be improved in the high ambient area, the tuning capacitor from Pin 3 to ground can be selected from N75 or N150 temperature compensation types.

Another reason for dc input to Pin 14 is the possibility of automatic frequency control. Where high accuracy of intercarrier frequency is required, it may be desirable to feed back the dc output of an AFC or phase detector for nominal carrier frequency control. Only limited control range could be used without adversely affecting the distortion performance, but very little frequency compensation will be needed.

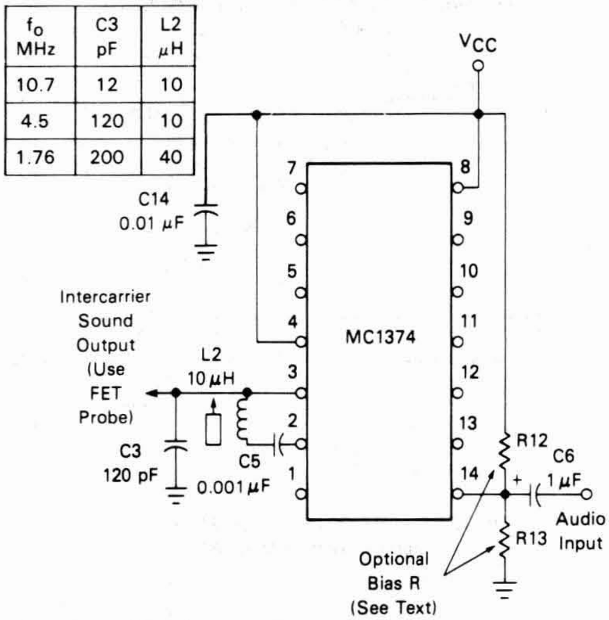
One added convenience in the FM section is the separate Pin "oscillator B+" which permits disabling of the sound system during alignment of the AM section. Usually it can be hard wired to the $V_{CC}$ source without decoupling.

Standard practice in television is to provide pre-emphasis of higher audio frequencies at the transmitter and a matching de-emphasis in the T.V. receiver audio amplifier. The purpose of this is to counteract the fact that less energy is usually present in the higher frequencies, and also that fewer modulation sidebands are within the deviation window. Both factors degrade signal to noise ratio. Pre-emphasis of 75 μs is standard practice. For cases where it has not been provided, a suitable pre-emphasis network is covered in Figure 20.

It would seem natural to take the FM system output from Pin 2, the emitter follower output, but this output is high in harmonic content. Taking the output from Pin 3 sacrifices somewhat in source impedance but results in a clean output fundamental, with all harmonics more than 40 dB down. This choice removes the need for additional filtering components. The source impedance of Pin 3 is approximately 2.0 kΩ, and the open circuit amplitude is about 900 mV p-p for the test circuit shown in Figure 11.

The application circuit of Figure 1 shows the recommended approach to coupling the FM output from Pin 3 to the AM modulator input, Pin 1. The input impedance at Pin 1 is very high, so the intercarrier level is determined by the source impedance of Pin 3 driving through C4 into the video bias circuit impedance of R4 and R5, about 2.2 K. This provides an intercarrier level of 500 mV p-p, which is correct for the 1.0 V peak video level chosen in this design. Resistor R6 and the input capacitance of Pin 1 provide some decoupling of stray pickup of RF oscillator or AM output which may be coupled to the sound circuitry.

FIGURE 11 — FM TEST CIRCUIT



| $f_o$ MHz | C3 pF | L2 μH |
|---|---|---|
| 10.7 | 12 | 10 |
| 4.5 | 120 | 10 |
| 1.76 | 200 | 40 |

FIGURE 12 — MODULATOR SENSITIVITY

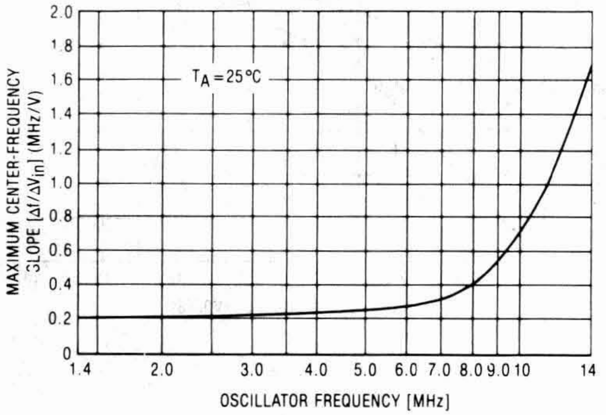


FIGURE 13 — MODULATOR TRANSFER FUNCTION (1.76 MHz)

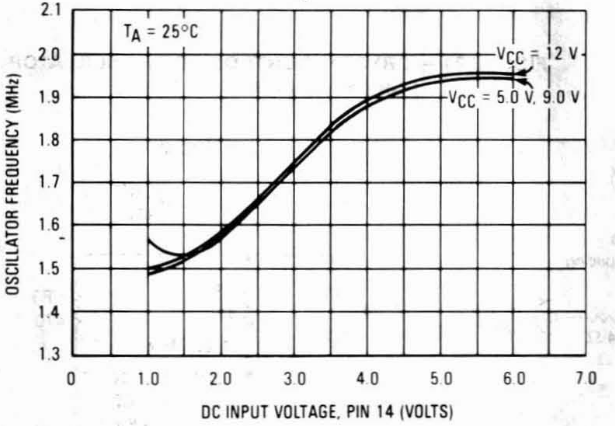


FIGURE 14 — DISTORTION versus MODULATION DEPTH

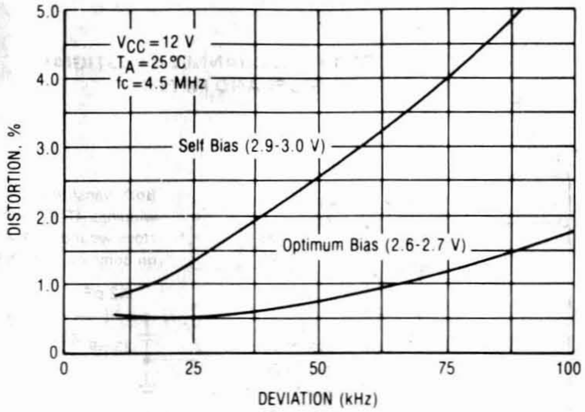


FIGURE 15 — MODULATOR TRANSFER FUNCTION (4.5 MHz)

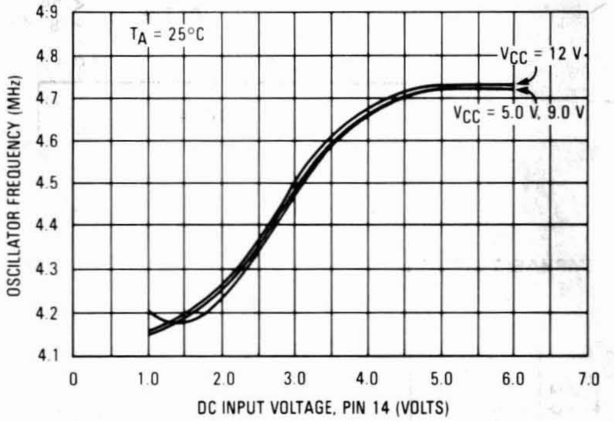


FIGURE 16 — FM SYSTEM FREQUENCY versus TEMPERATURE

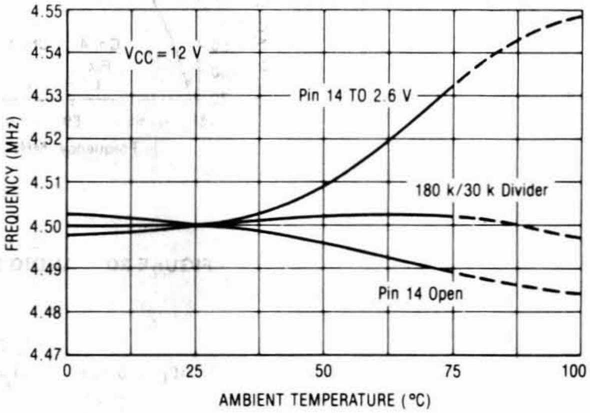


FIGURE 17 — MODULATOR TRANSFER FUNCTION (10.7 MHz)

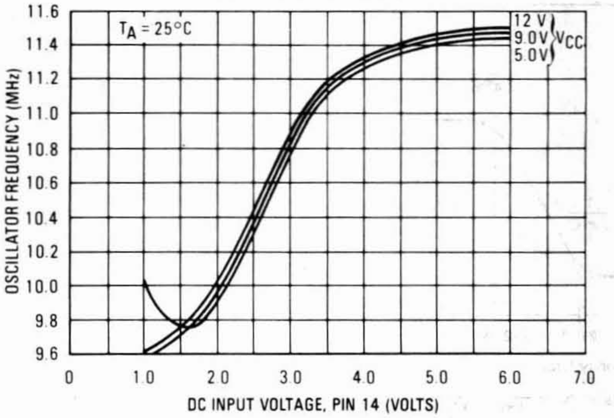


FIGURE 18 — FM SYSTEM FREQUENCY versus $V_{CC}$

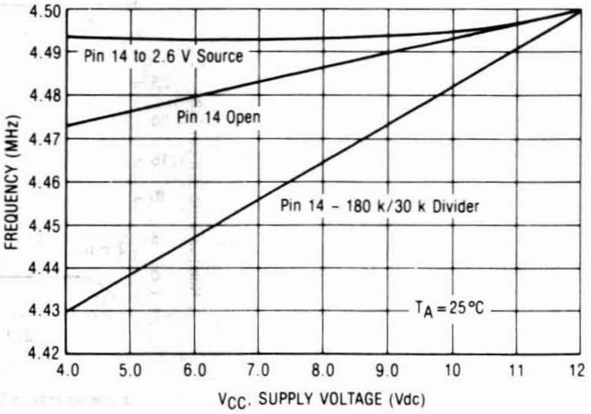


FIGURE 19 — A CHANNEL 4 VESTIGIAL SIDEBAND FILTER

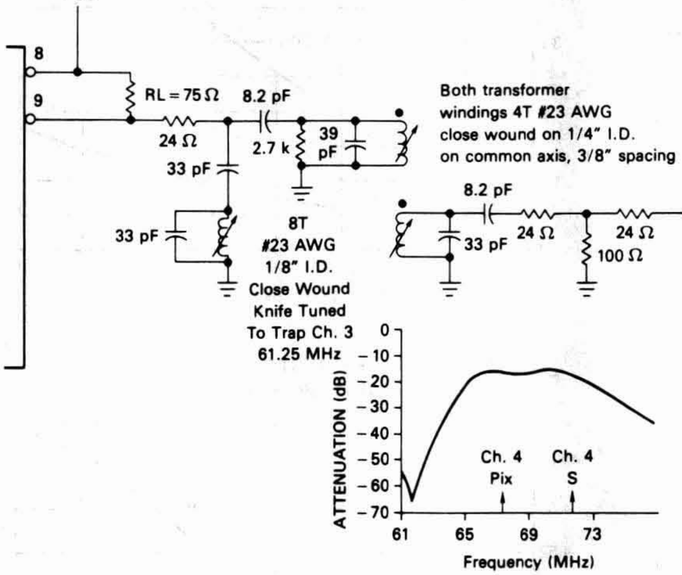

VCC
8
9
RL = 75 Ω
8.2 pF
24 Ω
33 pF
2.7 k
39 pF
Both transformer windings 4T #23 AWG close wound on 1/4" I.D. on common axis, 3/8" spacing
8.2 pF
24 Ω
24 Ω
100 Ω
33 pF
Output 75 Ω
33 pF
8T #23 AWG 1/8" I.D. Close Wound Knife Tuned To Trap Ch. 3 61.25 MHz
ATTENUATION (dB)
0
−10
−20
−30
−40
−50
−60
−70
61
65
69
73
Ch. 4 Pix
Ch. 4 S
Frequency (MHz)

FIGURE 21 — CRYSTAL CONTROLLED RF OSCILLATOR FOR CHANNEL 3, 61.25 MHz

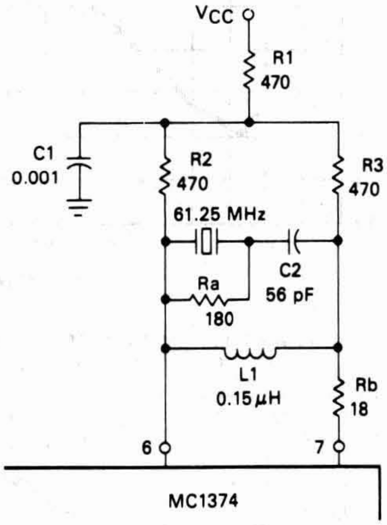
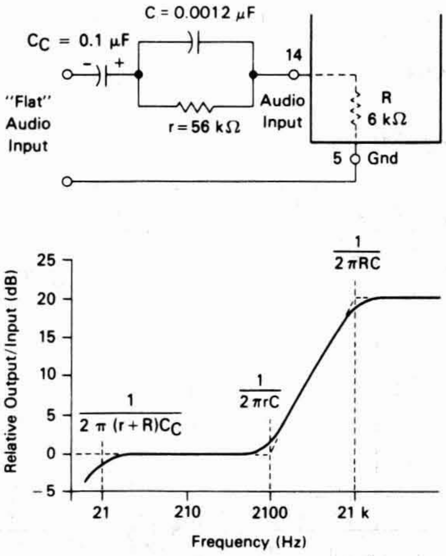

VCC
R1 470
C1 0.001
R2 470
R3 470
61.25 MHz
C2 56 pF
Ra 180
L1 0.15 μH
Rb 18
6
7
MC1374

FIGURE 20 — AUDIO PRE-EMPHASIS CIRCUIT


C = 0.0012 μF
CC = 0.1 μF
−
+
"Flat" Audio Input
r = 56 kΩ
14
Audio Input
R 6 kΩ
5
Gnd
Relative Output/Input (dB)
25
20
15
10
5
0
−5
1/(2π(r + R)CC)
1/(2πrC)
1/(2πRC)
21
210
2100
21 k
Frequency (Hz)

$$\text{pre-emphasis} = 75\ \mu s = rC = \frac{1}{2\pi(2100\text{ Hz})}$$

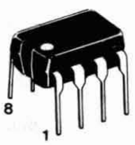
**See Application Note AN829 for further information.**

**MOTOROLA**

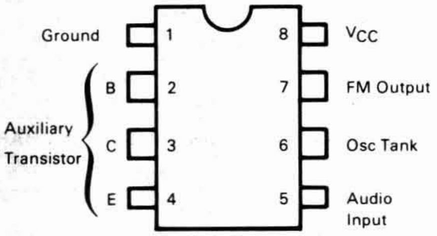
# MC1376

## FM MODULATOR CIRCUIT

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

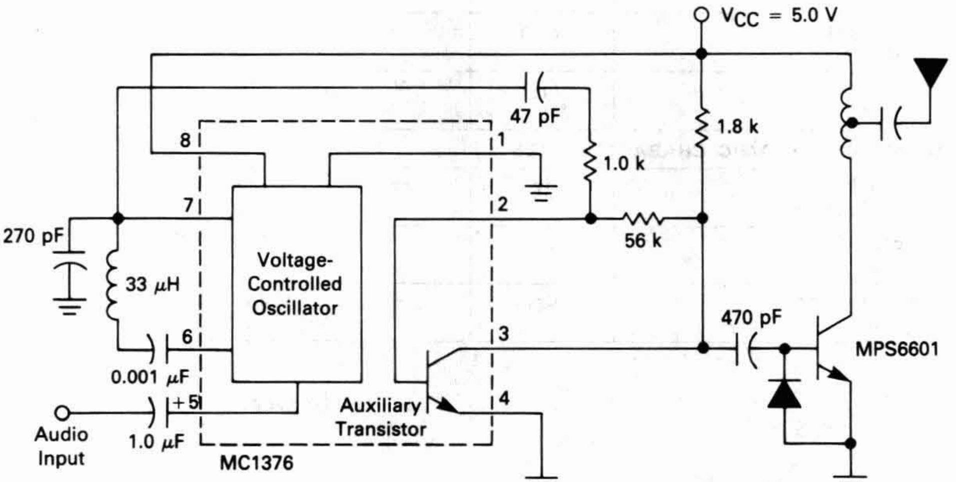

Ground
1
8
VCC
Auxiliary Transistor
B
2
7
FM Output
C
3
6
Osc Tank
E
4
5
Audio Input

## FM MODULATOR CIRCUIT

. . . a voltage-controlled oscillator/modulator ideally suited to cordless telephone and television intercarrier applications.

- Wide Supply Range (5.0–12 Vdc)
- Useful Frequency Range (1.4–14 MHz)
- Low Distortion (<1%)
- Excellent Oscillator Stability
- Output RF Driver Transistor Included
- Low Cost, Low Component Count Circuit
- Wide Deviation Capability

**FIGURE 1 — CORDLESS TELEPHONE BASE STATION TRANSMITTER (1.76 MHz)**


VCC = 5.0 V
47 pF
1.8 k
1.0 k
56 k
8
1
7
2
270 pF
33 μH
Voltage-Controlled Oscillator
6
0.001 μF
470 pF
3
MPS6601
+5
4
Audio Input
1.0 μF
Auxiliary Transistor
MC1376

**MAXIMUM RATINGS** ($T_A$ 25°C unless otherwise noted)

| Rating | Value | Unit |
|---|---|---|
| Modulator Supply Voltage | 13 | Vdc |
| Transistor Collector-Emitter Voltage | 10 | Vdc |
| Transistor Collector-Base Voltage | 15 | Vdc |
| Operating Ambient Temperature Range | 0 to +70° | °C |
| Storage Temperature Range | -65 to +150 | °C |
| Junction Temperature | 150 | °C |
| Power Dissipation, Package<br>Derate above 25°C | 1.2<br>10 | Watts<br>mW/°C |

**MODULATOR ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, $V_{CC}$ = 12 Vdc, Test Circuit of Figure 2 unless otherwise noted)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Operating Supply Voltage<br>Supply Current, $V_{CC}$ = 12 Vdc (excluding transistor) | 5.0<br>— | —<br>5.0 | 12<br>8.0 | Vdc<br>mAdc |
| Frequency Range of Modulator<br>Frequency Shift versus Temperature (R1 = ∞)<br>Frequency Shift versus $V_{CC}$ (R1 = ∞)<br>Output Amplitude<br>Output Harmonics, Unmodulated | —<br>—<br>—<br>80<br>— | 1.4–14<br>0.25<br>3.3<br>150<br>−43 | —<br>—<br>—<br>—<br>— | MHz<br>kHz/°C<br>kHz/V<br>mVp-p<br>dB |
| Modulation Sensitivity 1.7 MHz<br>4.5 MHz<br>10.7 MHz | —<br>—<br>— | 0.20<br>0.24<br>0.80 | —<br>—<br>— | MHz/V<br>MHz/V<br>MHz/V |
| Audio Distortion (±25 kHz, Deviation, R1 = 27 k, $f_o$ = 4.5 MHz)<br>Incidental AM (±25 kHz FM, 4.5 MHz) | —<br>— | 0.55<br>2.0 | —<br>— | %<br>% |
| Audio Input Resistance (Pin 5 to ground)<br>Audio Input Capacitance (Pin 5 to ground) | —<br>— | 6.0<br>5.0 | —<br>— | kΩ<br>pF |
| Stray Tuning Capacitance (Pin 7 to ground)<br>Effective Oscillator Source Impedance (Pin 7) | —<br>— | 6.0<br>2.0 | —<br>— | pF<br>kΩ |

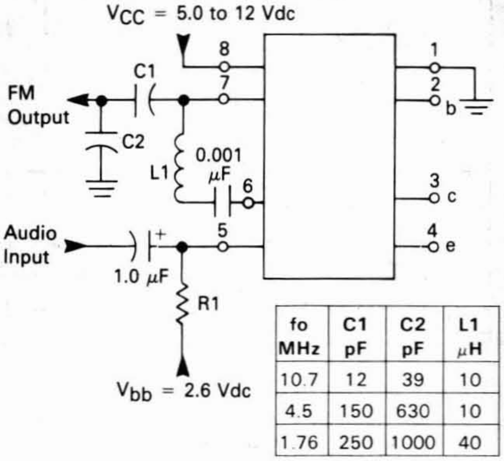
**AUXILIARY TRANSISTOR STATIC CHARACTERISTICS**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Collector-Base Breakdown Voltage<br>($I_C$ = 10 μAdc) | $V_{(BR)CBO}$ | 15 | 40 | — | Vdc |
| Collector-Emitter Breakdown Voltage<br>($I_C$ = 1.0 μAdc) | $V_{(BR)CEO}$ | 10 | — | — | Vdc |
| Collector-Substrate Breakdown Voltage<br>($I_C$ = 10 μAdc) | $V_{(BR)CIO}$ | — | 40 | — | Vdc |
| Emitter-Base Breakdown Voltage<br>($I_E$ = 10 μAdc) | $V_{(BR)EBO}$ | — | 6.50 | — | Vdc |
| Collector-Base Cutoff Current<br>($I_{BE}$ = 10 Vdc, $I_E$ = 0) | $I_{CBO}$ | — | — | 200 | nAdc |
| DC Current Gain<br>($I_C$ = 10 mAdc, $V_{CE}$ = 3.0 Vdc) | $h_{FE}$ | 40 | 90 | — | — |

**AUXILIARY TRANSISTOR DYNAMIC CHARACTERISTICS**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Current-Gain-Bandwidth Product<br>($V_{CE}$ = 3.0 Vdc, $I_C$ = 3.0 mAdc) | $f_T$ | — | 500 | — | MHz |
| Collector-Base Capacitance<br>($V_{CB}$ = 3.0 Vdc, $I_C$ = 0) | $C_{cb}$ | — | 1.0 | — | pF |
| Collector-Substrate Capacitance<br>($V_{CS}$ = 3.0 Vdc, $I_C$ = 0) | $C_{CI}$ | — | 3.0 | — | pF |

FIGURE 2 — TEST CIRCUIT



| fo MHz | C1 pF | C2 pF | L1 µH |
|---|---|---|---|
| 10.7 | 12 | 39 | 10 |
| 4.5 | 150 | 630 | 10 |
| 1.76 | 250 | 1000 | 40 |

## MC1376 GENERAL INFORMATION

This device was initially designed for the base station transmitter of a cordless telephone, the 1.76 MHz FM modulator shown in Figure 1. It also contains a "separate" transistor suitable for service as an output buffer or amplifier for up to 50 mA. Though the oscillator contains internal phase shift components which are not accessible, the MC1376 still has an operating frequency range of 1.4 to 14 MHz, making it a good companion to MC1372 or MC1373 as a 4.5 or 5.5 MHz intercarrier sound modulator for television signal generation. Also, the device can be used as a low cost FM IF (10.7 MHz) signal source for the production line or lab. Although not suitable for true high fidelity distortion measurements, it can handle quite wide deviation with very modest distortion, compared to other oscillator configurations. The modulator section is identical to the FM portion of the MC1374, TV modulator.

FIGURE 3 — MODULATOR TRANSFER FUNCTION (1.76 MHz)

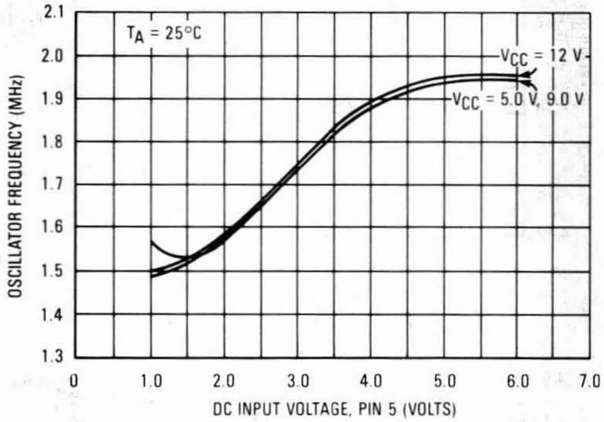


FIGURE 5 — MODULATOR TRANSFER FUNCTION (10.7 MHz)

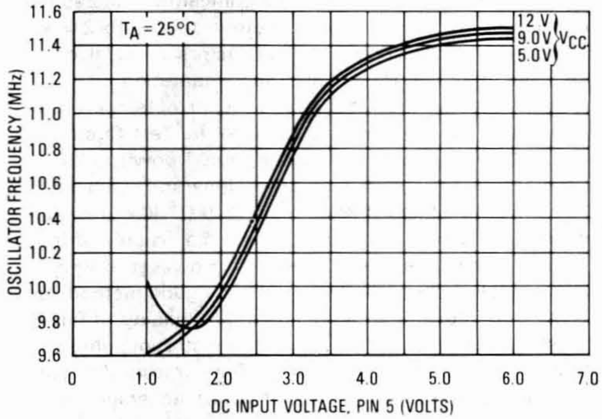


FIGURE 4 — MODULATOR TRANSFER FUNCTION (4.5 MHz)

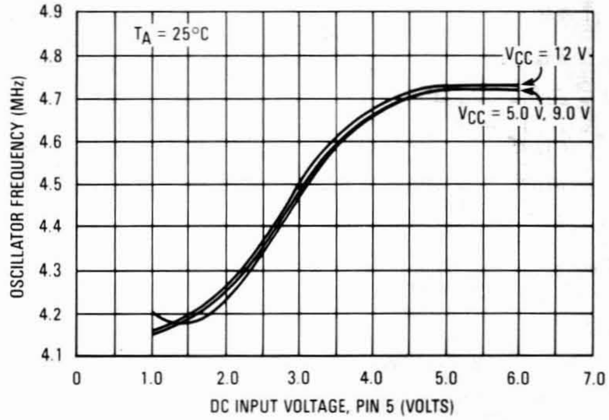
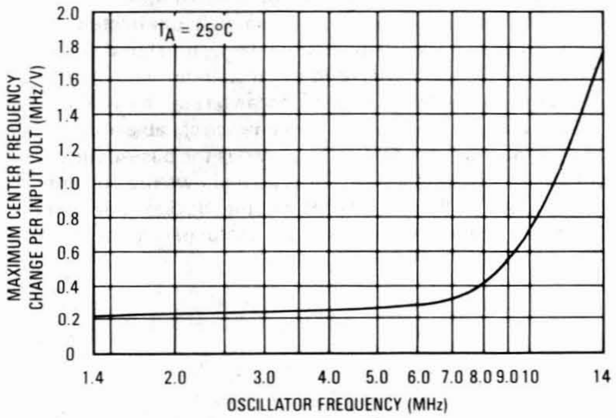


FIGURE 6 — MODULATOR SENSITIVITY



## APPLICATIONS INFORMATION

The oscillator center frequency is approximately the resonance of the inductor (Pin 6 to Pin 7) and the total capacitance from Pin 7 to ground. Include 6.0 pF (internal) and the circuit strays in the resonant frequency calculations for the higher frequency applications. For overall oscillator stability, it is best to keep the $X_L$ and $X_C$ in the range of 300 Ω to 1.0 kΩ.

The modulator transfer characteristics for three test frequencies are shown in Figures 3, 4 and 5. Although the horizontal axes of these curves are labelled "dc input voltage, Pin 5", they are valid transfer functions relating instantaneous Pin 5 voltage to output frequency.

Figure 6 is a plot of the maximum deviation per input volt over the usable frequency range of the part.

Most applications will require no dc connection at the audio input, Pin 5. However, some performance improvements can be achieved by addition of biasing circuitry. The unaided device will usually establish its own Pin 5 bias at 2.9 to 3.0 V. A brief study of Figures 3, 4, and 5 shows that this bias is a little high for optimum modulation linearity. This is verified by taking distortion measurments using a high quality FM detector (see Figure 7). Note that the distortion readings can be significantly reduced by externally pulling Pin 5 bias down to 2.6 to 2.7 V. Temperature and supply voltage factors must also be considered in determining bias implementation.

Figure 8 shows frequency as a function of temperature for several biasing methods (refer to the Test Circuit in Figure 2). This shows that pulling Pin 5 down to 2.6 V through 27 kΩ greatly improves the temperature stability. If $V_{CC}$ is well regulated, then a simple 180 kΩ/30 kΩ resistor divider is a good choice for optimum distortion and frequency stability versus temperature. However, if $V_{CC}$ is not regulated, then the divider is not a good method, as shown in Figure 9. To summarize, the biasing of Pin 5 must be done with considerations of distortion, ambient temperature, and supply stability. Temperature drift can also be compensated by means of controlled temperature coefficient capacitors, which are very common and inexpensive in this range of values. An N150 type used for C1 will nearly flatten the R1 = ∞ case in Figure 8.

The FM output at Pin 7 is usually about 600 mVp-p and has low harmonic content and high (2 kΩ) output impedance. The oscillator behavior is relatively unaffected by loading above 1.0 kΩ. If lower impedance must be driven, the capacitive divider used in the test circuit is a useful technique, or the "extra" transistor can be used as a buffer.

The transistor is a large geometry device capable of operating at over 50 mA. Figure 11 provides the base-emitter voltage characteristics and Figure 12 shows the current gain versus collector current for the device. See the Electrical Characteristics for other useful parameters.

FIGURE 7 — DISTORTION versus MODULATION DEPTH

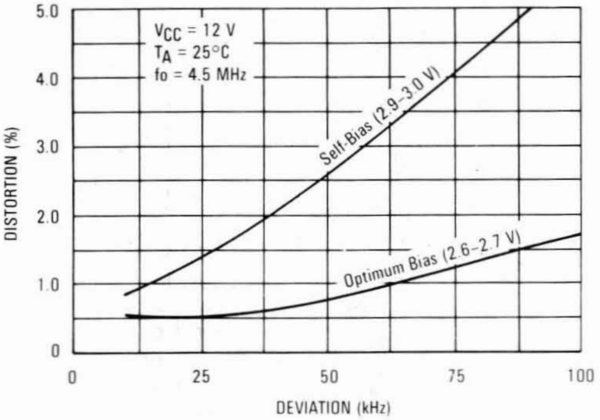


FIGURE 8 — FREQUENCY STABILITY versus TEMPERATURE

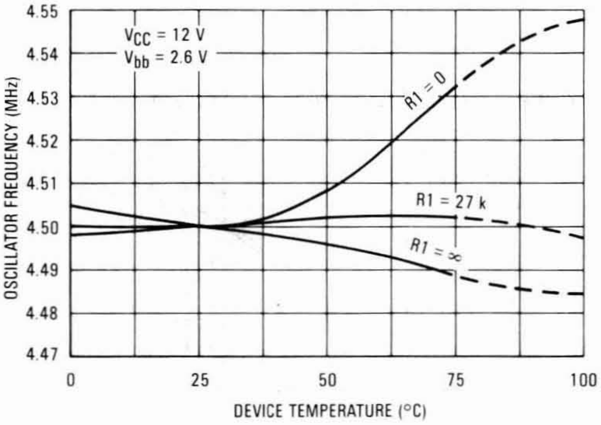


FIGURE 9 — FREQUENCY STABILITY versus SUPPLY VOLTAGE

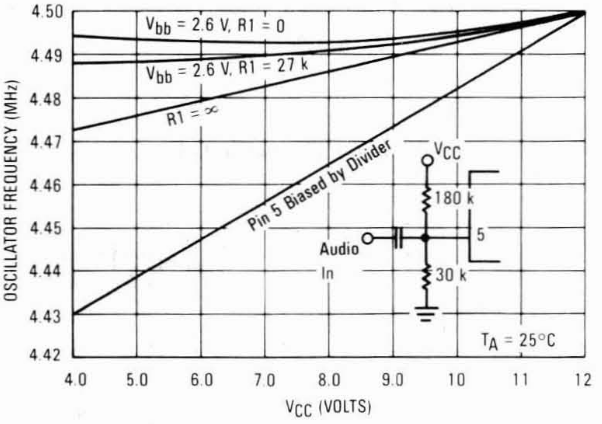
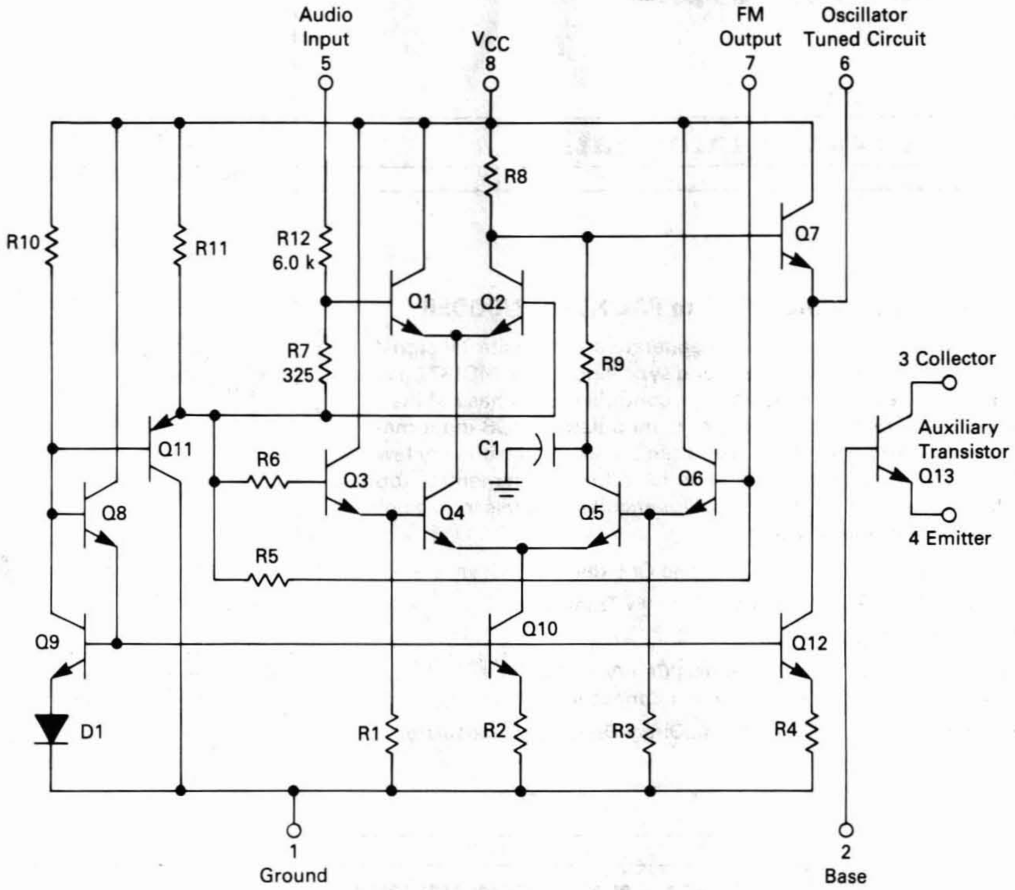


FIGURE 10 — INTERNAL SCHEMATIC


Audio
Input
5
VCC
8
FM
Output
7
Oscillator
Tuned Circuit
6
R8
Q7
R10
R11
R12
6.0 k
Q1
Q2
R7
325
R9
3 Collector
Auxiliary
Transistor
Q13
4 Emitter
Q11
R6
Q3
C1
Q6
Q8
Q4
Q5
R5
Q10
Q9
Q12
D1
R1
R2
R3
R4
1
Ground
2
Base

6

FIGURE 11 — BASE-EMITTER VOLTAGE

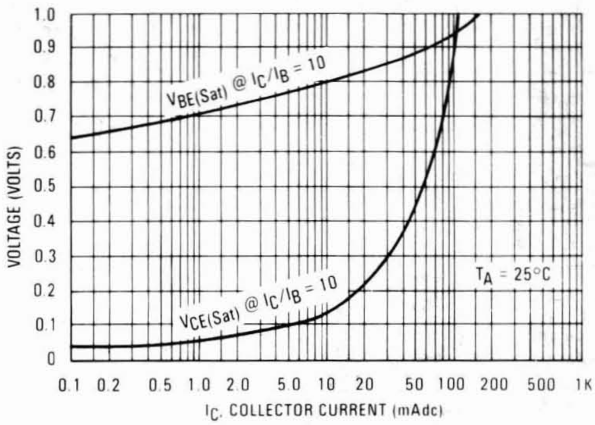
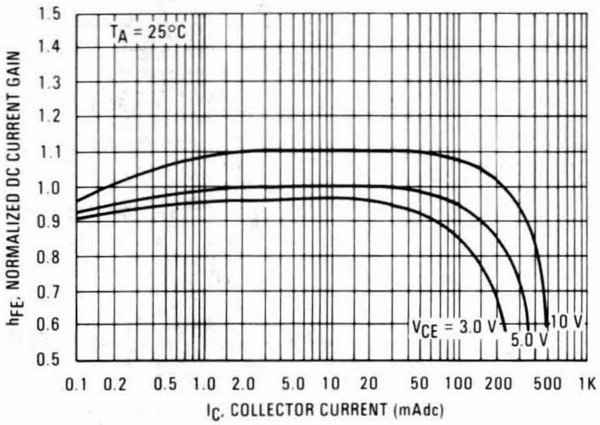


FIGURE 12 — NORMALIZED DC CURRENT GAIN



# MOTOROLA

# MC1377

## Advance Information

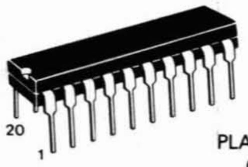
**COLOR TELEVISION RGB to PAL/NTSC ENCODER**

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

### COLOR TELEVISION RGB to PAL/NTSC ENCODER

. . . an integrated circuit used to generate a composite TV signal from baseband red, blue, green and sync inputs. The MC1377 has color subcarrier oscillator, voltage controlled 90° phase shifter, two DSB suppressed carrier chroma modulators, RGB input matrices and blanking level clamps. It can be operated with very few external parts, but has the pinouts for a fully implemented, top quality composite signal. It is ideal for encoding signals from color cameras and graphics generators.

- Reference Oscillator Self-Contained Or Externally Driven
- Nominal 90° ±3.0° Axes Are Optionally Trimmable
- Simple PAL/NTSC Switch
- Luminance And Chroma Channels Can Accept Delay Line/Bandpass Elements Or Direct Connection
- Provides dc Reference To Permit Direct Drive To RF Modulator

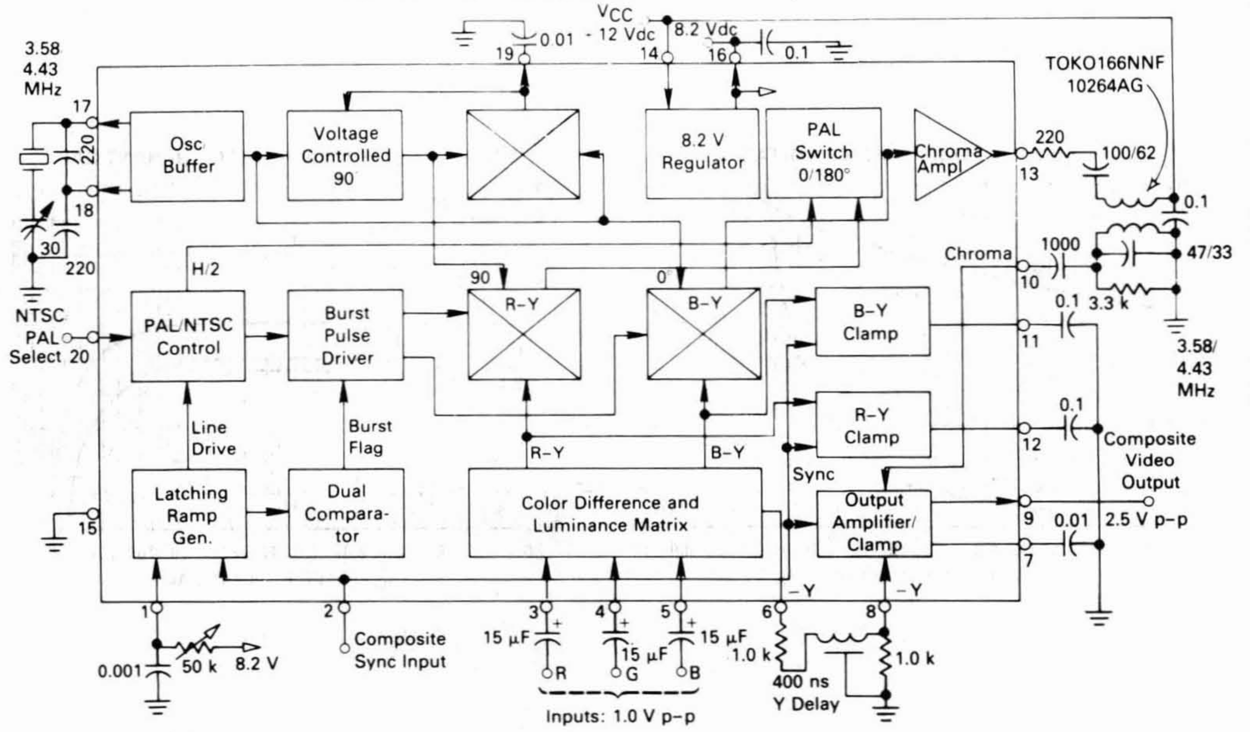


**P SUFFIX**
PLASTIC PACKAGE
CASE 738-02

**FN SUFFIX**
PLASTIC PACKAGE
CASE 775-01
PLCC-20

| ORDERING INFORMATION | | |
|---|---|---|
| **Device** | **Temperature Range** | **Package** |
| MC1377P | 0–70°C | Plastic DIP |

**FIGURE 1 — BLOCK DIAGRAM AND APPLICATION CIRCUIT**


VCC
0.01
- 12 Vdc
8.2 Vdc
0.1
19
14
16
3.58
4.43
MHz
17
220
18
30
220
NTSC
PAL
Select 20
15
Osc Buffer
Voltage Controlled 90
8.2 V Regulator
PAL Switch 0/180°
Chroma Ampl
TOKO166NNF
10264AG
220
100/62
13
0.1
Chroma
1000
10
47/33
0.1
3.3 k
3.58/
4.43
MHz
H/2
90
0°
R–Y
B–Y
PAL/NTSC Control
Burst Pulse Driver
B–Y Clamp
11
R–Y Clamp
12
0.1
Composite Video Output
Line Drive
Burst Flag
R–Y
B–Y
Sync
Latching Ramp Gen.
Dual Comparator
Color Difference and Luminance Matrix
Output Amplifier/ Clamp
9
0.01
2.5 V p–p
7
–Y
–Y
1
2
3
4
5
6
8
0.001
50 k
8.2 V
Composite Sync Input
15 µF
15 µF
15 µF
R
G
B
Inputs: 1.0 V p–p
1.0 k
1.0 k
400 ns
Y Delay

This document contains information on a new product. Specifications and information herein are subject to change without notice.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 15 | Vdc |
| 8.2 Vdc Regulator Output Current | $I_{REG}$ | 10 | mAdc |
| Operating Temperature | $T_{AMB}$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature | $T_{J(max)}$ | 150 | °C |
| Power Dissipation, package<br>Derate above 25°C | $P_D$ | 1.25<br>10 | W<br>mW/°C |

## RECOMMENDED OPERATING CONDITIONS

| | | |
|---|---|---|
| Supply Voltage | 12 ± 1.2 | Vdc |
| Sync Tip Level<br>Sync, Blanking Level | −0.5 to +1.0<br>+1.7 to +8.2 | Vdc |
| Red, Green, Blue Inputs (Saturated) | 1.0 | $V_{p-p}$ |

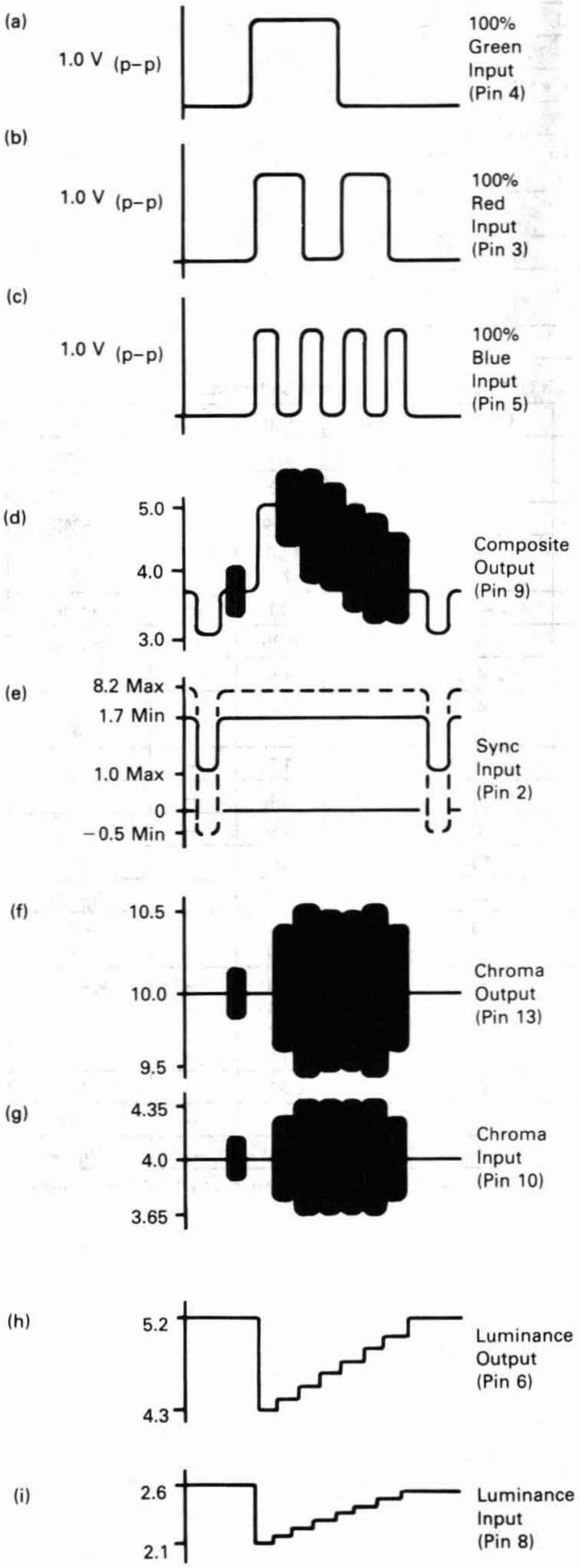
## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 12 Vdc, $T_A$ = 25°C, Circuit Of Figure 1 Unless Otherwise Noted.)

| Characteristic | Pin No. | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Current | 14 | 20 | 32 | 40 | mAdc |
| Oscillator Amplitude | 18 | — | 0.5 | — | $V_{(p-p)}$ |
| External Subcarrier Input (Oscillator Components Removed) | 17 | — | 0.25 | — | $V_{RMS}$ |
| Subcarrier Input: Resistance<br>Capacitance | 17 | —<br>— | 5.0<br>2.0 | —<br>— | k Ω<br>pF |
| Modulation Angle (R–Y) to (B–Y) | — | 85 | 90 | 95 | Degrees |
| (R–Y) Angle Adjustment | 19 | — | 0.25 | — | Deg/μA |
| R, G, B Input For 100% Color Saturation | 3, 4, 5 | — | 1.0 | — | $V_{(p-p)}$ |
| R, G, B Input: Resistance<br>Capacitance | 3, 4, 5 | —<br>— | 10<br>2.0 | — | kΩ<br>pF |
| Sync Threshold (See Figure 2e) | 2 | — | 1.7 | — | V |
| Sync Input Resistance (Input > 1.7 V) | 2 | — | 10 | — | kΩ |
| Chroma Output Level At 100% Saturation | 13 | — | 1.0 | — | $V_{(p-p)}$ |
| Chroma Output Resistance | 13 | — | 50 | — | Ω |
| Chroma Input Level For 100% Saturation | 10 | — | 0.7 | — | $V_{(p-p)}$ |
| Chroma Input: Resistance<br>Capacitance | 10 | —<br>— | 10<br>2.0 | —<br>— | kΩ<br>pF |
| Composite Output, 100% Saturation (See Figure 2d): Sync<br>Luminance<br>Chroma<br>Burst | 9 | —<br>—<br>—<br>— | 0.6<br>1.4<br>1.7<br>0.6 | —<br>—<br>—<br>— | $V_{(p-p)}$ |
| Output Impedance (See Note 1) | 9 | — | 50 | — | Ω |
| Luminance Bandwidth (3 dB), Less Delay Line | 9 | — | 8.0 | — | MHz |
| Subcarrier Leakage In Output | 9 | — | 20 | — | $mV_{(p-p)}$ |

Note 1: Output Impedance can be reduced to less than 10Ω by using a 150Ω output load from Pin 9 to ground. Power supply current will increase to about 60 mA.

**See Application Note AN932 for further information.**

FIGURE 2 — SIGNAL VOLTAGES
(CIRCUIT VALUES OF FIGURE 1)



## APPLICATION NOTES

**R.G.B. Inputs** should be set up to be 1.0 V p–p for fully saturated levels. This is not arbitrary, since sync and burst levels are internally fixed. The large (15 µF) input capacitors of Figure 1 are needed for the 50/60 Hz vertical component.

**Subcarrier Oscillator.** The internal common-collector Colpitts can be free run or it can easily be pulled in by a lightly coupled signal from a "master" into Pin 17. Also, it can be disabled entirely and a 0.25 $V_{RMS}$ signal driven into Pin 17.

**Modulator Phase Angles** are quite accurately established internally. Taking (B–Y) as 0°, burst is at 180°, and the angle of (R–Y) is 90° ± 3.0°. The (R–Y) angle can be "tweaked." For example, 470 kΩ from Pin 19 to ground will increase the (R–Y) to (B–Y) angle about 3.0°. Pulling Pin 19 up will decrease the angle.

**Composite Output** is dc referenced and can be direct coupled to an RF modulator as shown in Figure 3. In this case, the 8.2 V regulator output of the MC1377 is divided down to 5.8 V to provide the zero carrier reference to Pin 1 of the MC1374.

**Burst Generation** is provided by a sync triggered ramp on Pin 1 and two internal level sensors. Since the early part of this ramp is used, it is quite accurate. Fixed R–C values are feasible, as shown in Figure 3.

**Sync Input** can be varied over a wide latitude but neverless must be applied correctly. The typical ac coupled sync signal has very little positive value and will require a pull-up resistor to 8.2 Vdc at the input. The sync input is a 10 kΩ/10 kΩ divider in the base of a common emitter stage. For PAL operation, the correctly serrated vertical sync interval must be used, in order to continuously trigger the PAL flip-flop. "Block" vertical sync can be used for NTSC.

**(R–Y)(B–Y)(–Y)** signals are generated to NTSC values (±5.0%) in the input matrices. They are dc clamped at black level by a sync driven clamp. Burst amplitude is internally fixed to correspond to sync level, allowing for 3.0 dB loss in the chroma bandpass filter. If the filter is not used, as shown in Figure 3, a resistor divider should be inserted between Pin 13 and Pin 10 to provide the proper chroma level. When the chroma bandpass is not used, the (–Y) delay line should also be removed, but the 1.0 k/1.0 k divider from Pin 6 to Pin 8 should be retained.

FIGURE 3 — COUPLING THE MC1377 TO THE MC1374 RF MODULATOR

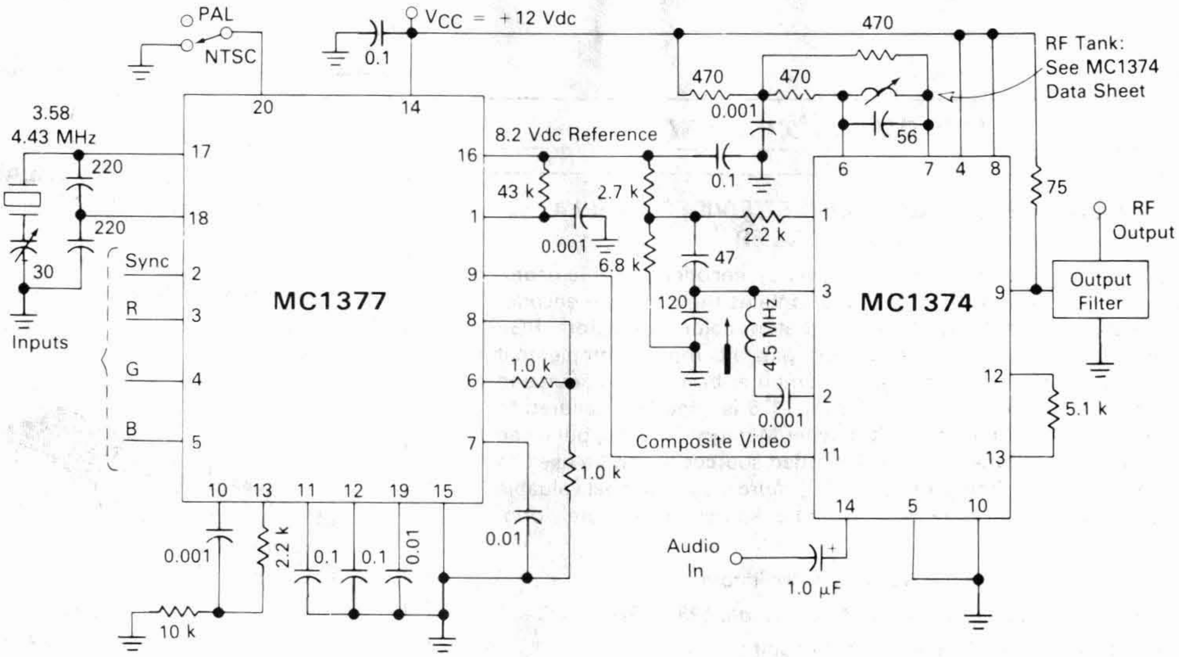

PAL
NTSC
VCC = +12 Vdc
0.1
470
470
470
0.001
56
RF Tank: See MC1374 Data Sheet
3.58
4.43 MHz
220
220
30
Inputs
Sync
R
G
B
20
14
17
18
2
3
4
5
16
1
9
8
6
7
10
13
11
12
19
15
MC1377
8.2 Vdc Reference
43 k
2.7 k
0.1
0.001
6.8 k
2.2 k
47
120
4.5 MHz
0.001
1.0 k
1.0 k
0.01
Composite Video
0.001
2.2 k
0.1
0.1
0.01
10 k
MC1374
6
7
4
8
1
3
2
9
12
13
11
14
5
10
75
RF Output
Output Filter
5.1 k
Audio In
1.0 μF

FIGURE 4 — VECTORSCOPE DISPLAY OF 100% SATURATED NTSC COLOR BARS

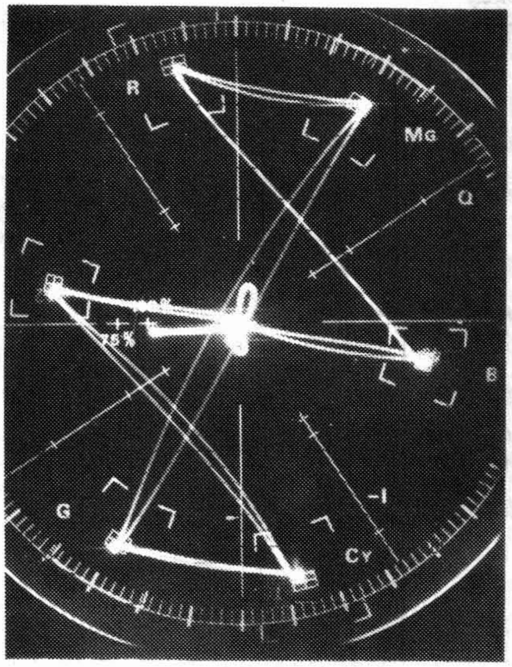
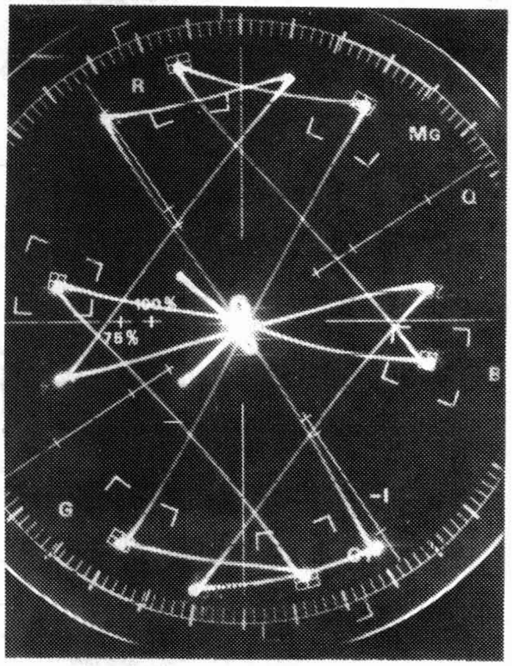


FIGURE 5 — 100% SATURATED PAL COLOR BARS ON NTSC VECTORSCOPE



**MOTOROLA**

# MC1378

## Product Preview

### COLOR TELEVISION COMPOSITE VIDEO OVERLAY SYNCHRONIZER

. . . a bipolar composite video overlay encoder and microcomputer synchronizer. The MC1378 contains the complete encoder function of the MC1377, i.e. quadrature color modulators, RGB matrix, and blanking level clamps, plus a complete complement of synchronizers to lock a microcomputer-based video source to any remote video source. The MC1378 is especially tailored to work with the Motorola RMS (Raster Memory System), but it can be applied to other controllable video sources. It can be used as a local system timing and encoding source, but it is most valuable when used to lock the microcomputer source to a remotely originated video signal.

- Contains All Needed Reference Oscillators
- Can Be Operated in PAL or NTSC Mode, 625 or 525 Line
- Wideband, Full-Fidelity Color Encoding
- Local or Remote Modes of Operation
- Minimal External Components
- Designed to Operate from 5.0 V Supply
- Will Work with Non-standard Video

**COLOR TELEVISION COMPOSITE VIDEO OVERLAY SYNCHRONIZER**

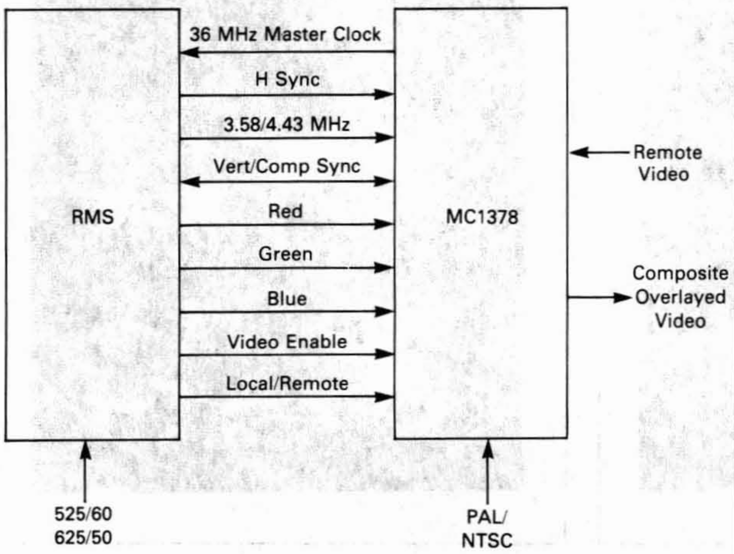
**SILICON MONOLITHIC INTEGRATED CIRCUIT**

**P SUFFIX**
PLASTIC PACKAGE
CASE 711-03

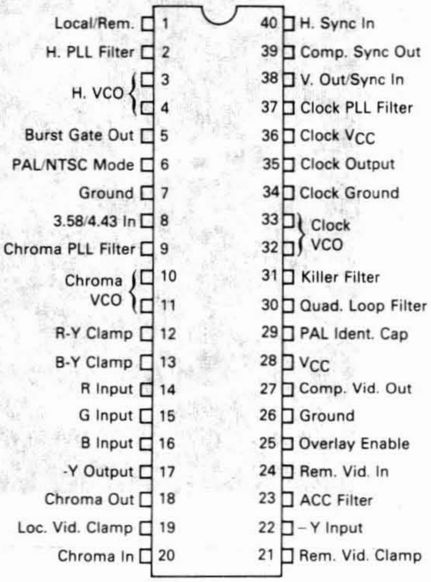
**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC1378P | 0–70°C | Plastic DIP |

**FIGURE 1 — BLOCK DIAGRAM TYPICAL APPLICATION**


RMS
MC1378
36 MHz Master Clock
H Sync
3.58/4.43 MHz
Vert/Comp Sync
Red
Green
Blue
Video Enable
Local/Remote
Remote Video
Composite Overlayed Video
525/60
625/50
PAL/ NTSC

**PIN ASSIGNMENTS**


Local/Rem. 1
H. PLL Filter 2
H. VCO 3
4
Burst Gate Out 5
PAL/NTSC Mode 6
Ground 7
3.58/4.43 In 8
Chroma PLL Filter 9
Chroma VCO 10
11
R-Y Clamp 12
B-Y Clamp 13
R Input 14
G Input 15
B Input 16
-Y Output 17
Chroma Out 18
Loc. Vid. Clamp 19
Chroma In 20
40 H. Sync In
39 Comp. Sync Out
38 V. Out/Sync In
37 Clock PLL Filter
36 Clock VCC
35 Clock Output
34 Clock Ground
33 Clock VCO
32
31 Killer Filter
30 Quad. Loop Filter
29 PAL Ident. Cap
28 VCC
27 Comp. Vid. Out
26 Ground
25 Overlay Enable
24 Rem. Vid. In
23 ACC Filter
22 – Y Input
21 Rem. Vid. Clamp

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 6.0 | Vdc |
| Operating Temperature | $T_A$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature | $T_{J(max)}$ | 150 | °C |
| Power Dissipation (Package)<br>Derate above 25°C | $P_D$ | 1.25<br>10 | W<br>mW/°C |

## RECOMMENDED OPERATING CONDITIONS

| Condition | Pin No. | Value | Unit |
|---|---|---|---|
| Supply Voltage | 28, 36 | 5.0 ± 0.25 | Vdc |
| RGB Input for 100% Saturation | 14, 15, 16 | 1.0 | $V_{p\text{-}p}$ |
| Color Oscillator Input Level | 8 | 0.5 | $V_{p\text{-}p}$ |
| Video Input, Positive | 24 | 1.0 | $V_{p\text{-}p}$ |

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0 V, $T_A$ = 25°C Circuit of Figure 4 or 5)

| Characteristic | Pin No. | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Current | 28, 36 | — | 100 | — | mAdc |
| Video Output, Open Circuit, Positive | 27 | — | 2.0 | — | $V_{p\text{-}p}$ |
| Modulation Angle (R − Y) to (B − Y) | — | 87 | 90 | 93 | Degrees |
| RGB Input Impedance | 14, 15, 16 | — | 10 | — | kΩ |
| Local/Remote Switch (TTL) High<br>Low | 1 | — | Remote<br>Local | — | — |
| Horizontal Sync Input, Negative Going (TTL) | 40 | — | 4.3 | — | $V_{p\text{-}p}$ |
| Vertical Sync Output, Negative Going, Remote Mode (TTL) | 38 | — | 4.3 | — | $V_{p\text{-}p}$ |
| Composite Sync Output, Negative Going (TTL) | 39 | — | 4.3 | — | $V_{p\text{-}p}$ |
| Burst Gate Output, Positive Going (TTL) | 5 | — | 4.3 | — | $V_{p\text{-}p}$ |

## DESCRIPTION OF OPERATION — Refer to Figures 3, 4

### REMOTE MODE

The incoming remote video signal (Pin 24) supplies all synchronizing information. A discussion of the function of the phase detectors helps to clarify the lockup method:

PD1 — locks the internally counted-down 4 MHz horizontal VCO to the incoming horizontal sync. It is fast acting, to follow VCR source fluctuations.

PD2 — locks the 36 MHz clock VCO, which is divided down by the RMS, to the divided down horizontal VCO.

PD3 — is a gated phase detector which locks the 14 MHz crystal oscillator, divided by 4, to the incoming color burst.

PD4 — controls an internal phase shifter to assure that the outgoing color burst is the same phase as incoming burst at PD3.

PD5 — not used in REMOTE MODE

Vertical lock is obtained by continuously resetting the sync generator in the RMS with separated vertical sync from the MC1378, Pin 38. This signal is TTL level vertical block sync, negative going. The horizontal sync from the RMS to Pin 40 is also TTL level with sync negative going. The local/remote switch, Pin 1, is in local mode when grounded, remote mode when taken to 5.0 V. The overlay control, Pin 25, has an analog characteristic, centered about 1.0 V, which allows fading from local to remote.

### LOCAL MODE

The MC1378 and RMS combine to provide a fully synchronized standard signal source. In this case, composite sync must be supplied by the RMS or other time base system. In the MC1378 the phase detectors operate as follows:

PD1 — locks the internally counted-down 4 MHz horizontal VCO to a Horizontal Sync signal (at Pin 40) from the RMS (counted down from 36 MHz).

PD2 — not used in LOCAL MODE.

PD3 — not used in LOCAL MODE.

PD4 — active, but providing an arbitrary phase shift setting between the color oscillator and the output burst phase.

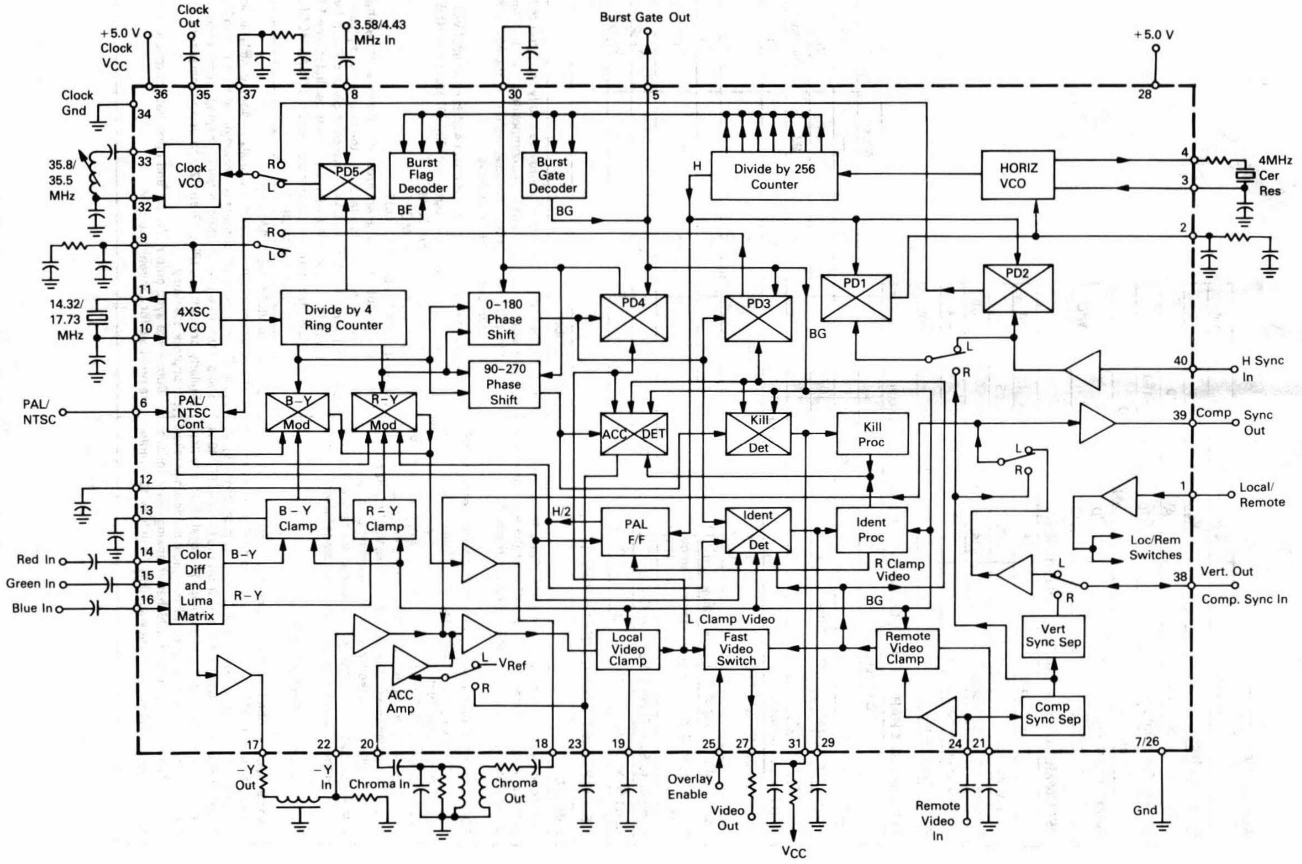
PD5 — locks the 36 MHz clock VCO (which is divided down by the RMS) to the 14 MHz (crystal) color oscillator. The 14 MHz is, therefore, the system standard in LOCAL MODE, and it is not dc controlled.

### COMPOSITE VIDEO GENERATION

The color encoding at the RGB signals is done exactly as in the MC1377. Composite chroma is looped out at Pins 18 and 20 to allow the designer to choose band shaping. Luminance is similarly brought out (Pins 17 and 22) to permit installation of the appropriate delay.

Composite sync output, Pin 39, and burst gate output, Pin 5, are provided for convenience only.

FIGURE 2 — MC1378 INTERNAL BLOCK DIAGRAM


+5.0 V
Clock
VCC
Clock
Out
3.58/4.43
MHz In
Burst Gate Out
+5.0 V
Clock
Gnd
35.8/
35.5
MHz
14.32/
17.73
MHz
PAL/
NTSC
Red In
Green In
Blue In
Clock
VCO
PD5
Burst
Flag
Decoder
BF
Burst
Gate
Decoder
BG
Divide by 256
Counter
H
HORIZ
VCO
4MHz
Cer
Res
4XSC
VCO
Divide by 4
Ring Counter
0–180
Phase
Shift
90–270
Phase
Shift
PD4
PD3
PD1
PD2
BG
H Sync
In
PAL/
NTSC
Cont
B–Y
Mod
R–Y
Mod
ACC DET
Kill
Det
Kill
Proc
Comp
Sync
Out
Local/
Remote
Loc/Rem
Switches
B – Y
Clamp
R – Y
Clamp
H/2
PAL
F/F
Ident
Det
Ident
Proc
R Clamp
Video
Vert. Out
Comp. Sync In
Color
Diff
and
Luma
Matrix
B–Y
R–Y
BG
L Clamp Video
Vert
Sync Sep
Local
Video
Clamp
Fast
Video
Switch
Remote
Video
Clamp
Comp
Sync Sep
ACC
Amp
VRef
R
L
–Y
Out
–Y
In
Chroma In
Chroma
Out
Overlay
Enable
Video
Out
VCC
Remote
Video
In
Gnd
36
35
37
8
30
5
28
34
33
32
9
11
10
6
12
13
14
15
16
4
3
2
40
39
1
38
17
22
20
18
23
19
25
27
31
29
24
21
7/26

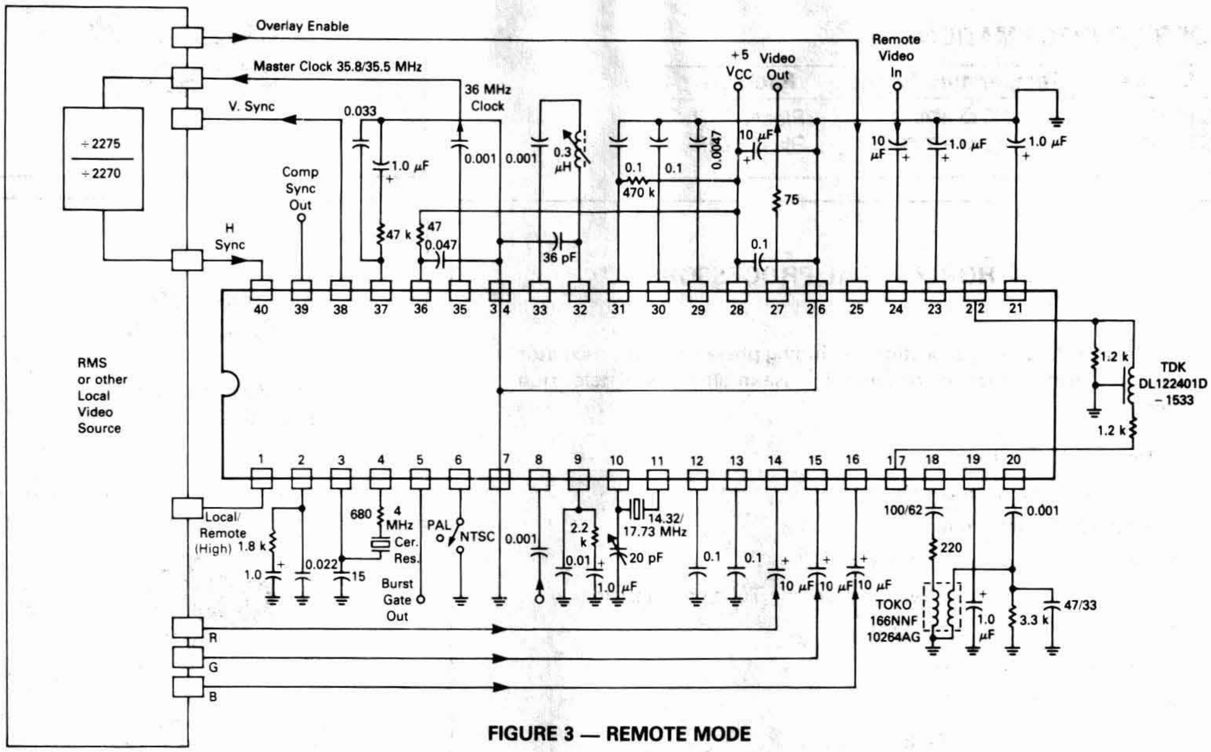

Overlay Enable
Master Clock 35.8/35.5 MHz
V. Sync
÷ 2275
÷ 2270
H Sync
Comp Sync Out
0.033
36 MHz Clock
1.0 μF
47 k
47
0.047
0.001
0.001
0.3 μH
36 pF
0.1
0.1
470 k
0.0047
+5 VCC
Video Out
10 μF
75
0.1
Remote Video In
10 μF
1.0 μF
1.0 μF
40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
RMS or other Local Video Source
1.2 k
TDK DL122401D − 1533
1.2 k
Local/ Remote (High)
1.8 k
1.0
0.022
15
680
4 MHz Cer. Res.
PAL
NTSC
Burst Gate Out
0.001
2.2 k
0.01
1.0 μF
14.32/ 17.73 MHz
20 pF
0.1
0.1
10 μF
10 μF
10 μF
100/62
220
0.001
TOKO 166NNF 10264AG
1.0 μF
3.3 k
47/33
R
G
B

FIGURE 3 — REMOTE MODE

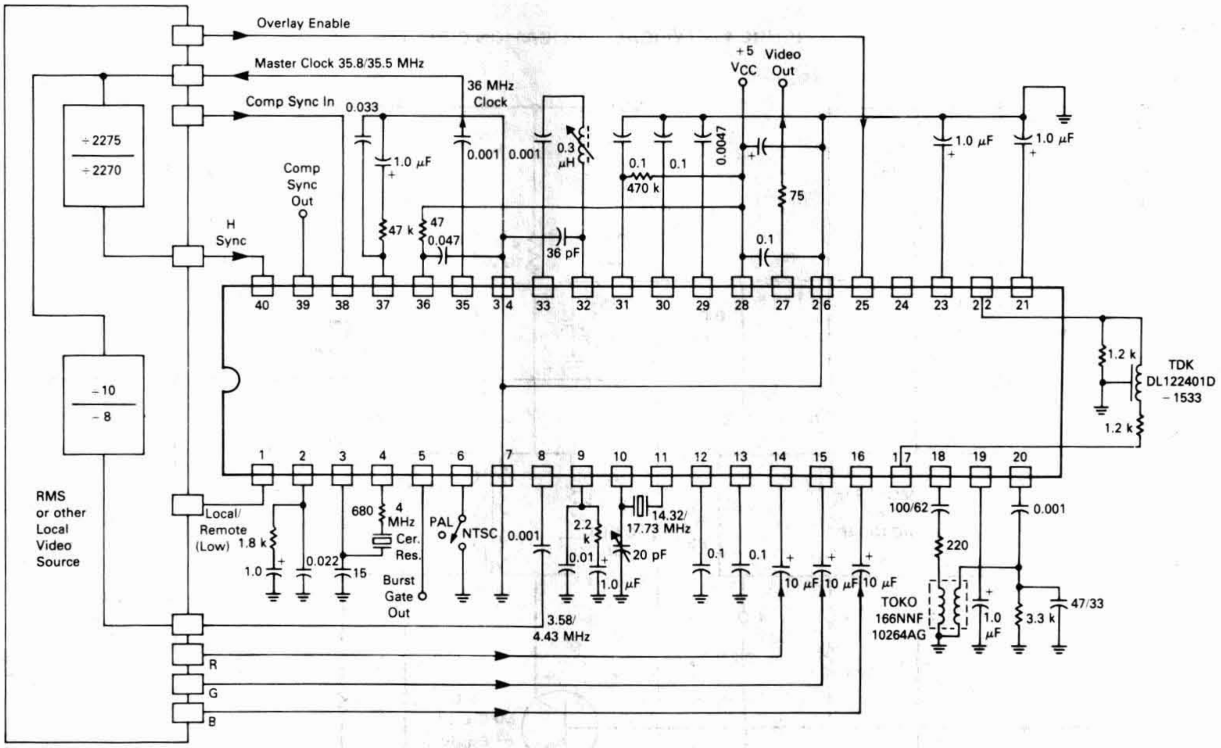

Overlay Enable
Master Clock 35.8/35.5 MHz
Comp Sync In
0.033
36 MHz Clock
÷ 2275
÷ 2270
Comp Sync Out
1.0 μF
0.001
0.001
0.3 μH
0.1
0.1
470 k
0.0047
+5 VCC
Video Out
75
H Sync
47 k
47
0.047
36 pF
0.1
1.0 μF
1.0 μF
40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
÷ 10
÷ 8
1.2 k
TDK DL122401D − 1533
1.2 k
RMS or other Local Video Source
Local/ Remote (Low)
1.8 k
1.0
0.022
15
680
4 MHz Cer. Res.
PAL
NTSC
Burst Gate Out
0.001
2.2 k
0.01
1.0 μF
14.32/ 17.73 MHz
20 pF
0.1
0.1
10 μF
10 μF
10 μF
100/62
220
0.001
TOKO 166NNF 10264AG
1.0 μF
3.3 k
47/33
3.58/ 4.43 MHz
R
G
B

FIGURE 4 — LOCAL MODE

## ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC1391P | 0°C to +70°C | Plastic DIP |
| MC1394P | 0°C to +70°C | Plastic DIP |

# MC1391P
# MC1394P

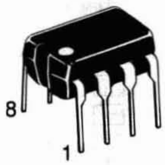
## TV HORIZONTAL PROCESSOR

. . . low-level horizontal sections including phase detector, oscillator and pre-driver — a device designed for use in all types of television receivers.

- Internal Shunt Regulator
- Preset Hold Control Capability
- ±300 Hz Typical Pull-In
- Linear Balanced Phase Detector
- Variable Output Duty Cycle for Driving Tube or Transistor
- Low Thermal Frequency Drift
- Small Static Phase Error
- Adjustable dc Loop Gain
- MC1391P — Positive Flyback Inputs
- MC1394P — Negative Flyback Inputs

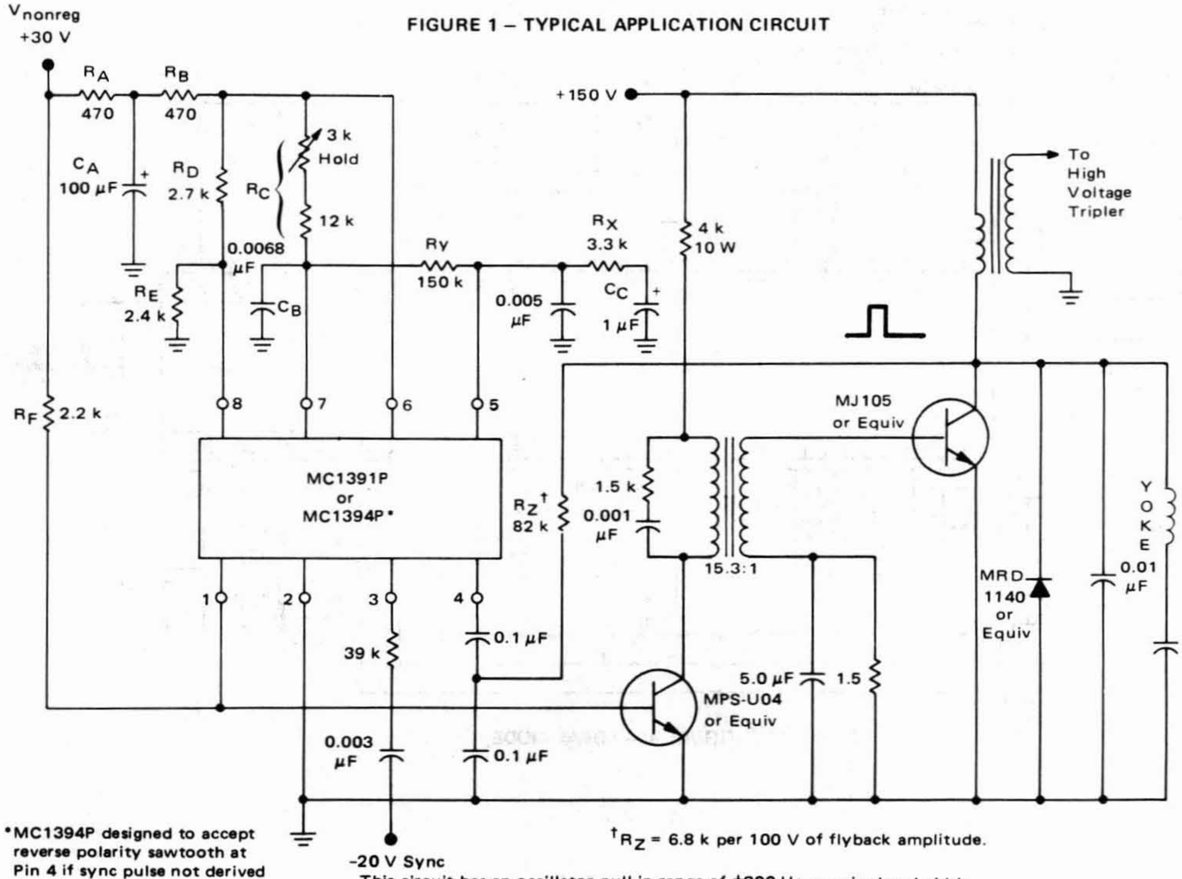
**TV HORIZONTAL PROCESSOR**

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

FIGURE 1 — TYPICAL APPLICATION CIRCUIT


Vnonreg
+30 V
RA
470
RB
470
CA
100 µF
RD
2.7 k
RC
3 k
Hold
12 k
0.0068 µF
RE
2.4 k
CB
Ry
150 k
Rx
3.3 k
0.005 µF
CC
1 µF
+150 V
4 k
10 W
To High Voltage Tripler
RF 2.2 k
8
7
6
5
MC1391P or MC1394P*
Rz†
82 k
1.5 k
0.001 µF
15.3:1
MJ105 or Equiv
Y O K E
0.01 µF
MRD-1140 or Equiv
0.2 µF
1
2
3
4
39 k
0.1 µF
5.0 µF
1.5
MPS-U04 or Equiv
0.003 µF
0.1 µF
-20 V Sync

*MC1394P designed to accept reverse polarity sawtooth at Pin 4 if sync pulse not derived from MJ105 collector.

†$R_Z$ = 6.8 k per 100 V of flyback amplitude.

This circuit has an oscillator pull-in range of ±300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Value | Unit |
|---|---|---|
| Supply Current | 40 | mAdc |
| Output Voltage | 40 | Vdc |
| Output Current | 30 | mAdc |
| Sync Input Voltage (Pin 3) | 5.0 | $V_{(p-p)}$ |
| Flyback Input Voltage (Pin 4) | 5.0 | $V_{(p-p)}$ |
| Power Dissipation (Package Limitation)<br>Plastic Package<br>Derate above $T_A$ = +25°C | <br>625<br>5.0 | <br>mW<br>mW/°C |
| Operating Temperature Range (Ambient) | 0 to +70° | °C |
| Storage Temperature Range | -65 to +150 | °C |

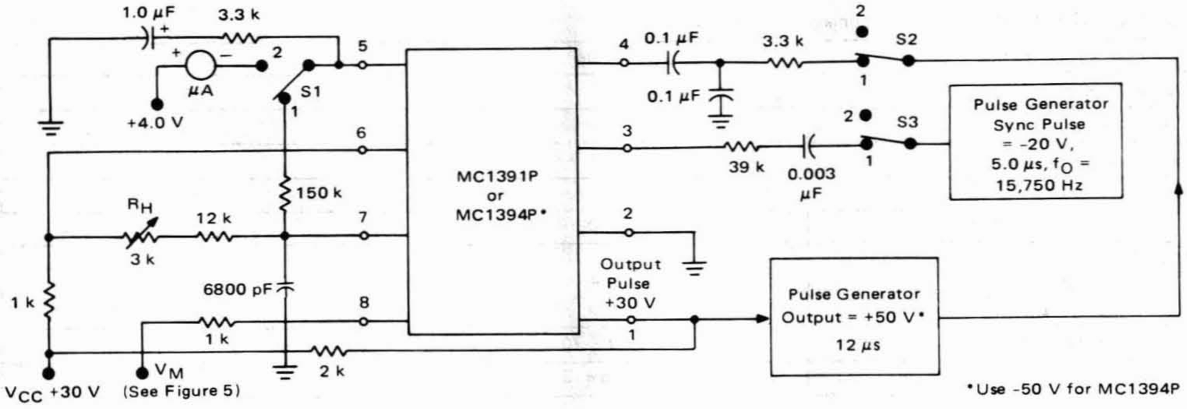
**ELECTRICAL CHARACTERISTICS** ($T_A$ = +25°C unless otherwise noted.) (See Test Circuit of Figure 2, all switches in position 1.)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Regulated Voltage (Pin 6) | 8.0 | 8.6 | 9.0 | Vdc |
| Supply Current (Pin 6) | – | 20 | – | mAdc |
| Collector-Emitter Saturation Voltage (Output Transistor Q1 in Figure 6) ($I_C$ = 20 mA, Pin 1) Vdc | – | 0.15 | 0.25 | Vdc |
| Voltage (Pin 4) | – | 2.0 | – | Vdc |
| Oscillator Pull-in Range (Adjust $R_H$ in Figure 2) | – | ±300 | – | Hz |
| Oscillator Hold-in Range (Adjust $R_H$ in Figure 2) | – | ±900 | – | Hz |
| Static Phase Error ($\Delta f$ = 300 Hz) | – | 0.5 | – | μs |
| Free-running Frequency Supply Dependance (S1 in position 2) | – | ±3.0 | – | Hz/Vdc |
| Phase Detector Leakage (Pin 5) (All switches in position 2) | – | – | ±1.0 | μA |
| Sync Input Voltage (Pin 3) | 2.0 | – | 5.0 | V(p-p) |
| Sawtooth Input Voltage (Pin 4) | 1.0 | – | 3.0 | V(p-p) |

## TYPICAL CHARACTERISTICS

($T_A$ = +25°C unless otherwise noted.)

FIGURE 2 – TEST CIRCUIT


1.0 µF
3.3 k
µA
+4.0 V
S1
150 k
RH
3 k
12 k
6800 pF
1 k
1 k
2 k
VCC +30 V
VM
(See Figure 5)
MC1391P
or
MC1394P*
0.1 µF
0.1 µF
3.3 k
S2
39 k
0.003 µF
S3
Pulse Generator
Sync Pulse
= -20 V,
5.0 µs, fO =
15,750 Hz
Output Pulse +30 V
Pulse Generator
Output = +50 V*
12 µs

*Use -50 V for MC1394P

FIGURE 3 – FREQUENCY versus TEMPERATURE

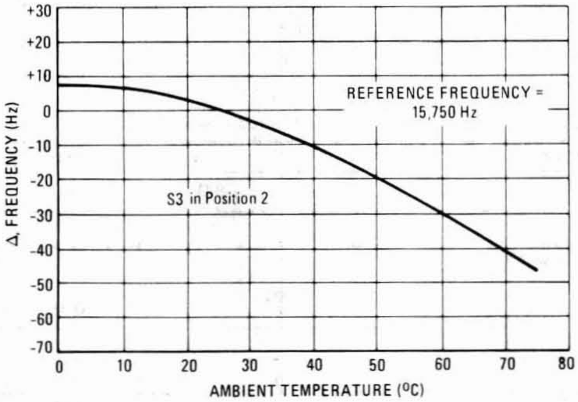


FIGURE 4 – FREQUENCY DRIFT versus WARM-UP TIME

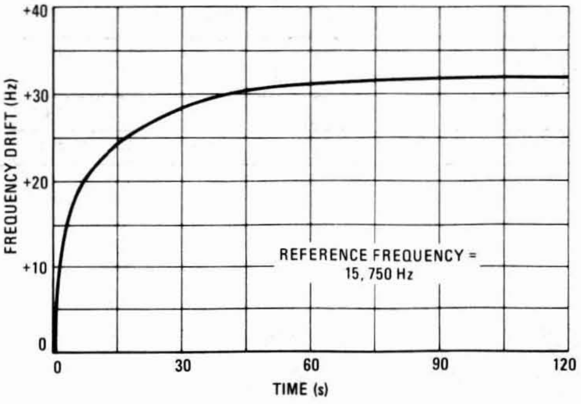


FIGURE 5 – MARK-SPACE RATIO

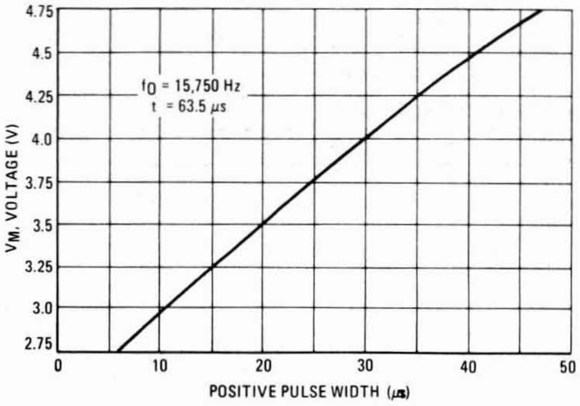
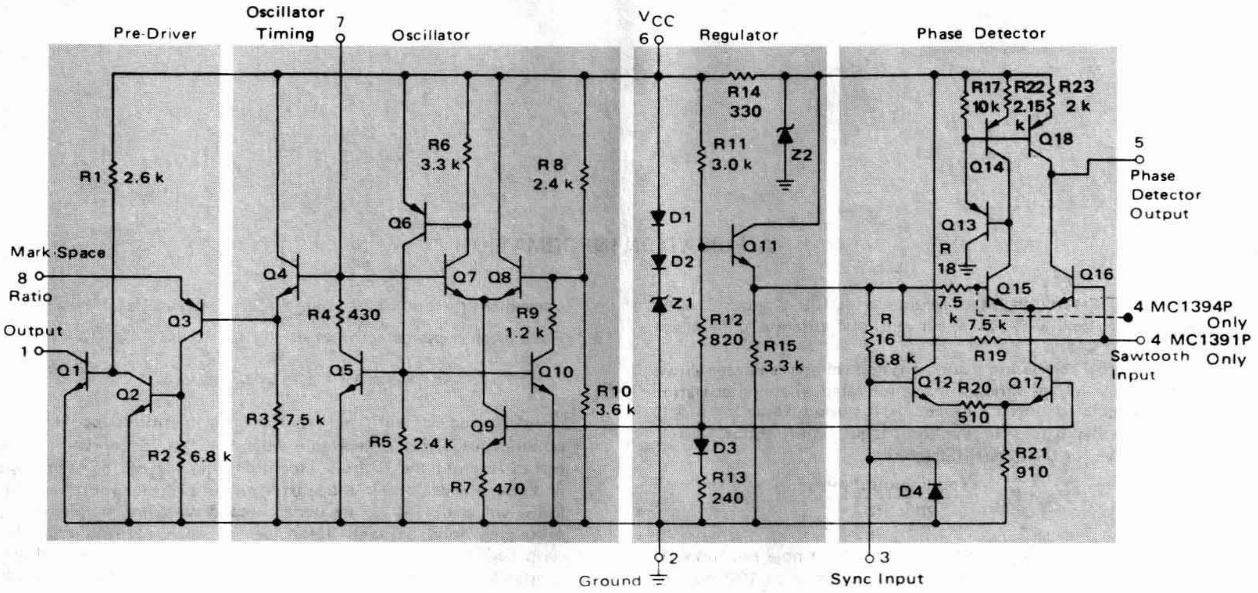


FIGURE 6 – CIRCUIT SCHEMATIC


Pre-Driver
Oscillator Timing 7
Oscillator
VCC 6
Regulator
Phase Detector
R1 2.6 k
Mark-Space 8 Ratio
Output 1
Q1
Q2
Q3
R2 6.8 k
Q4
R4 430
R3 7.5 k
Q5
R5 2.4 k
Q6
R6 3.3 k
Q7
Q8
R8 2.4 k
R9 1.2 k
Q9
R7 470
Q10
R10 3.6 k
D1
D2
Z1
R14 330
R11 3.0 k
Z2
Q11
R12 820
R15 3.3 k
D3
R13 240
R17 10 k
R22 2.15 k
R23 2 k
Q18
Q14
Q13
R18 7.5 k
Q15
Q16
5 Phase Detector Output
4 MC1394P Only
4 MC1391P Only
Sawtooth Input
R16 6.8 k
R19 7.5 k
Q12
R20 510
Q17
R21 910
D4
2 Ground
3 Sync Input

## CIRCUIT OPERATION

The MC1391P and MC1394P contain the oscillator, phase detector and predriver sections needed for a television horizontal APC loop.

The oscillator is an RC type with one pin (Pin 7) used to control the timing. The basic operation can be explained easily. If it is assumed that Q7 is initially off, then the capacitor connected from Pin 7 to ground will be charged by an external resistor ($R_C$) connected to Pin 6. As soon as the voltage at Pin 7 exceeds the potential set at the base of Q8 by resistors R8 and R10, Q7 will turn on and Q6 will supply base current to Q5 and Q10. Transistor Q10 will set a new, lower potential at the base of Q8 determined by R8, R9 and R10. Then, transistor Q5 will discharge the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time Q7 will turn off and the cycle repeats.

The sawtooth generated at the base of Q4 will appear across R3 and turn off Q3 whenever it exceeds the bias set on Pin 8. By adjusting the potential at Pin 8, the duty cycle (MSR) at the predriver output pin (Pin 1) can be changed to accommodate either tube or transistor horizontal output stages.

The phase detector is isolated from the remainder of the circuit by R14 and Z2. The phase detector consists of the comparator Q15, Q16 and the gated current source Q17. Negative going sync pulses at Pin 3 turn off Q12 and the current division between Q15 and Q16 will be determined by the phase relationship of the sync and the sawtooth waveform at Pin 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents will flow in the collectors of Q15 and Q16 each for half the sync pulse period. The current in Q15 is turned around by Q18 so that there is no net output current at Pin 5 for balanced conditions. When a phase offset occurs, current will flow either in or out of Pin 5. This pin is connected via an external low-pass filter to Pin 7, thus controlling the oscillator.

Shunt regulation for the circuit is obtained with a zero temperature coefficient from the series combination of D1, D2 and Z1.

## APPLICATION INFORMATION

Although it is an integrated circuit, the MC1391P and MC1394P have all the flexibility of a conventional discrete component horizontal APC loop.

The internal temperature compensated voltage regulator allows a wide supply voltage variation to be tolerated, enabling operation from nonregulated power supplies. A minimum value for supply current into Pin 6 to maintain zener regulation is about 18 mA. Allowing 2mA for the external dividers

$$R_A + R_B = \frac{V_{nonreg(min)} - 8.8}{20 \times 10^{-3}}$$

Components $R_A$, $R_B$ and $C_A$ are used for ripple rejection. If the supply voltage ripple is expected to be less than 100 mV (for a 30 Volt supply) then $R_A$ and $R_B$ can be combined and $C_A$ omitted.

The output pulse width can be varied from 6 µs to 48 µs by changing the voltage at Pin 8 (see Figure 5). However, care should be taken to keep the lead lengths to Pin 8 as short as possible to prevent ringing which can result in erroneous output pulses at Pin 1. The parallel impedance of $R_D$ and $R_E$ should be close to 1 kΩ to ensure stable pulse widths.

For 15 mA drive at saturation

$$R_F = \frac{V_{nonreg} - 0.3}{15 \times 10^{-3}}$$

The oscillator free-running frequency is set by $R_C$ and $C_B$ connected to Pin 7. For values of $R_C \gg R_{discharge}$ (R4 in Figure 6), a useful approximation for the free-running frequency is

$$f_O = \frac{1}{0.6\, R_C C_B}$$

Proper choice of $R_C$ and $C_B$ will give a wide range of oscillator frequencies – operation at 31.5 kHz for count-down circuits is possible for example. As long as the product $R_C C_B \approx 10^{-4}$ many combinations of values of $R_C$ and $C_B$ will satisfy the free-running frequency requirement of 15.734 kHz. However, the sensitivity of the oscillator ($\beta$) to control-current from the phase detector is directly dependent on the magnitude of $R_C$, and this provides a convenient method of adjusting the dc loop gain (fc).

For a given phase detector sensitivity ($\mu$) = $1.60 \times 10^{-4}$ A/rad

$$f_c = \mu\beta \text{ and } \beta = 3.15 \times R_C \text{ Hz/mA}$$

Increasing $R_C$ will raise the dc loop gain and reduce the static phase error (S.P.E.) for a given frequency offset. Secondary effects are to increase the natural resonant frequency of the loop ($\omega_n$) and give a wider pull-in range from an out-of-lock condition. The loop will also tend to be underdamped with fast pull-in times, producing good airplane flutter performance. However, as the loop becomes more underdamped impulse noise can cause shock excitation of the loop. Unlimited increase in the dc loop gain will also raise the noise bandwidth excessively causing horizontal jitter with thermal noise. Once the dc loop gain has been selected for adequate S.P.E. performance, the loop filter can be used to produce the balance between other desirable characteristics. Damping of the loop is achieved most directly by changing the resistor $R_X$ with respect to $R_Y$ which modifies the ac/dc gain ratio (m) of the loop. Lowering this ratio will reduce the pull-in range and noise bandwidth (fnn). (Note: very large values of $R_Y$ will limit the control capability of the phase detector with a corresponding reduction in hold-in range).

Static phasing can be adjusted simply by adding a small resistor between the flyback pulse integrating capacitor and ground. The sync coupling capacitor should not be too small or it can charge during the vertical pulse and this may result in picture bends at the top of the CRT.

NOTE:

In adjusting the loop parameters, the following equations may prove useful:

$$f_{nn} = \frac{1 + \chi^2 T\omega_c}{4\chi T} \qquad \chi = \frac{R_X}{R_Y}$$

$$\omega_n = \sqrt{\frac{\omega_c}{(1+\chi)\,T}} \qquad \omega_c = 2\pi f_c$$

$$T = R_Y C_C$$

$$K = \frac{\chi^2 T\omega_c}{4}$$

where:

K = loop damping coefficient

**MOTOROLA**

# MC3320P
# MC3321P

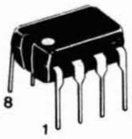
## CLASS B AUDIO DRIVERS

. . . designed as preamplifiers and driver circuits for complementary output transistors.

- Driver for Auto Radios – and up to 10-Watt Amplifiers
- High Gain – 7.0 mV for 1.0 Watt, $R_L$ = 3.2 Ohms
- High Input Impedance – 500-Kilohm Capability
- Output Biasing Diodes Included
- No Special $h_{FE}$ Matching of Outputs Required
- Formerly MFC8020A and MFC8021A in Case 644A Package

## CLASS B AUDIO DRIVERS

**SILICON MONOLITHIC**
**INTEGRATED CIRCUIT**

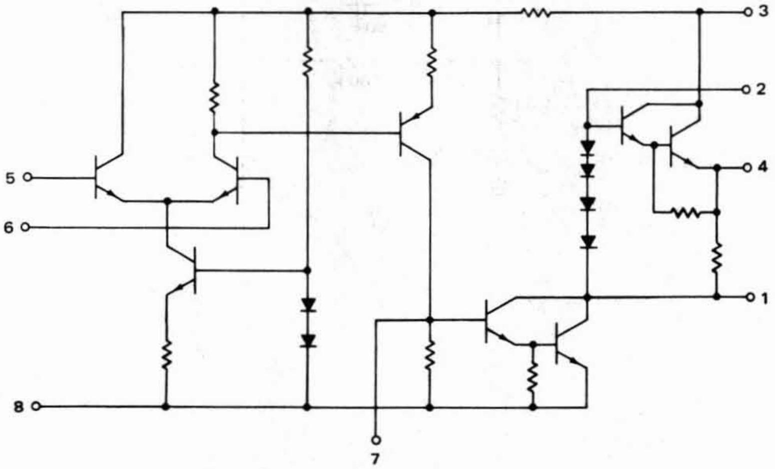


PLASTIC PACKAGE
CASE 626-04

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Symbol | MC3320P | MC3321P | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 35 | 20 | Vdc |
| Peak Output Current (Pins 4 and 1) | $I_P$ | 150 | | mA |
| Operating Ambient Temperature Range | $T_A$ | -10 to +75 | | °C |
| Storage Temperature Range | $T_{stg}$ | -55 to +125 | | °C |
| Junction Temperature | $T_J$ | 150 | | °C |

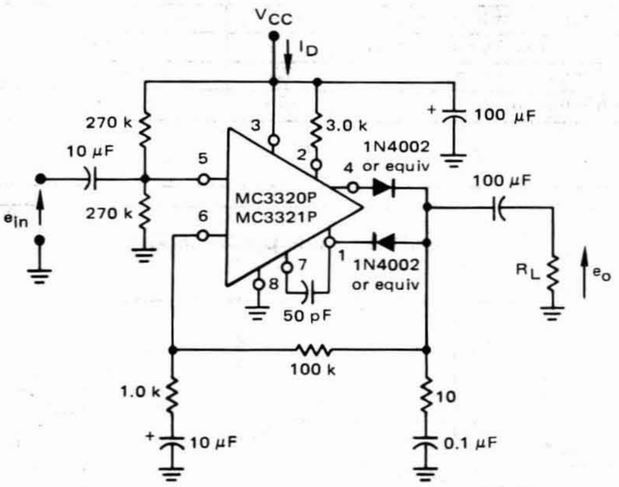
**FIGURE 1 – CIRCUIT SCHEMATIC**



**ELECTRICAL CHARACTERISTICS** ($T_A$ = +25°C unless otherwise noted) (See Figure 2)

| Characteristic | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Drain Current ($e_{in}$ = 0) | | | | | mA |
| ($V_{CC}$ = 30 Vdc) | MC3320P | – | 10 | 30 | |
| ($V_{CC}$ = 14 Vdc) | MC3321P | – | 7.0 | 30 | |
| Sensitivity ($P_O$ = 1.0 Watt, f = 1.0 kHz) | | | | | mV |
| ($e_o$ = 8.95 V(RMS), $R_L$ = 165 Ω) | MC3320P | – | 89 | 112 | |
| ($e_o$ = 3.2 V(RMS), $R_L$ = 65 Ω) | MC3321P | – | 32 | 40 | |
| Total Harmonic Distortion (f = 1.0 kHz) | | | | | % |
| ($V_{CC}$ = 30 V, $e_o$ = 8.95 V(RMS), $R_L$ = 165 Ω) | MC3320P | – | 0.7 | 5.0 | |
| ($V_{CC}$ = 14 V, $e_o$ = 3.2 V(RMS), $R_L$ = 65 Ω) | MC3321P | – | 1.0 | 5.0 | |
| Open-Loop Gain | | | | | dB |
| ($V_{CC}$ = 30 V, $R_L$ = 165 Ω) | MC3320P | – | 89 | – | |
| ($V_{CC}$ = 14 V, $R_L$ = 65 Ω) | MC3321P | – | 87 | – | |
| Ripple Rejection (f = 60 Hz, $A_V$ = 100, $e_{in}$ = 0, Power Supply Ripple = 1.0 V(RMS)) | | – | 27 | – | dB |
| Equivalent Input Noise ($e_{in}$ = 0, $R_S$ = 1.0 kΩ, BW = 100 Hz – 10 Hz) | | – | 18 | – | µV |
| Quiescent Output Voltage ($e_{in}$ = 0) | | | | | Vdc |
| ($V_{CC}$ = 30 V) | MC3320P | – | 15 | – | |
| ($V_{CC}$ = 14 V) | MC3321P | – | 7.0 | – | |

FIGURE 2 – TEST CIRCUIT

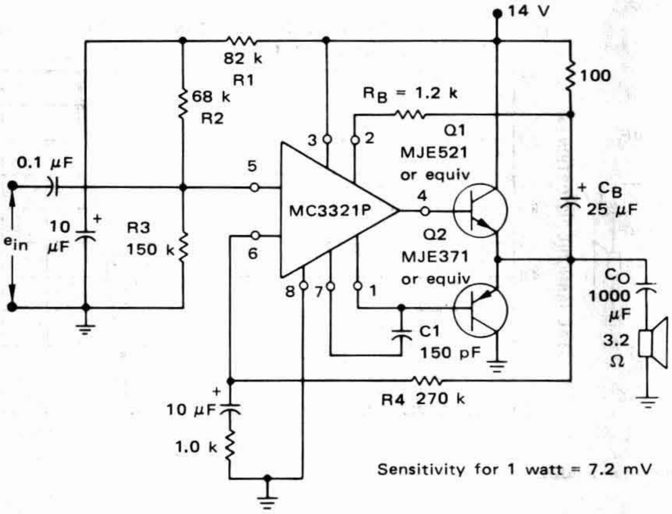


VCC
ID
270 k
10 µF
270 k
ein
3
3.0 k
2
5
6
MC3320P
MC3321P
1N4002
4 or equiv
100 µF
100 µF
1
1N4002
or equiv
7
8
50 pF
RL
eo
100 k
1.0 k
10 µF
10
0.1 µF

## TYPICAL AUTO RADIO AUDIO APPLICATIONS and CHARACTERISTICS

($T_A$ = +25° unless otherwise noted.)

FIGURE 3 – APPLICATION CIRCUIT FOR MC3321P*



Sensitivity for 1 watt = 7.2 mV

FIGURE 4–TOTAL HARMONIC DISTORTION versus OUTPUT POWER

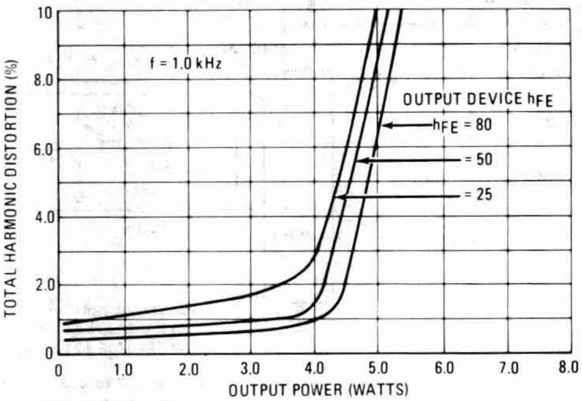


FIGURE 5 – TOTAL HARMONIC DISTORTION versus FREQUENCY

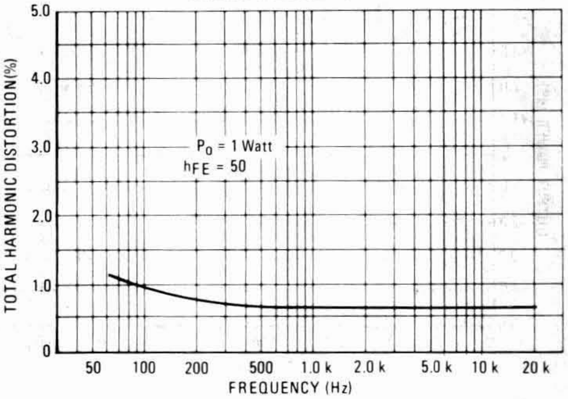
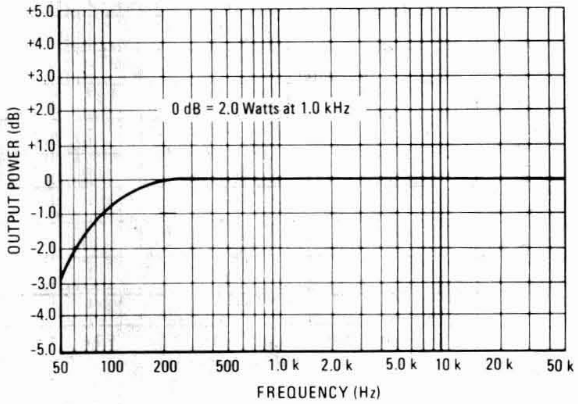


FIGURE 6 – FREQUENCY RESPONSE



## APPLICATIONS INFORMATION for MC3321P (AUTO RADIO AUDIO)

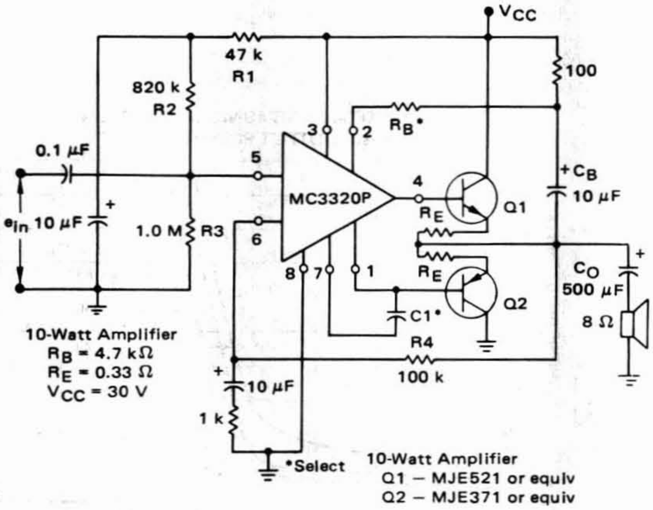
The MC3321P combines all the voltage gain required for an automotive radio audio amplifier into one package reducing the circuit-board area requirement. The circuit shown in Figure 3 has an input sensitivity of approximately 7.2 millivolts for a one-watt output. Sensitivity can be adjusted by changing the value of $R_4$. The circuit performance is a function of the output device $h_{FE}$, as shown in Figure 4. Figure 4 can be used to determine the minimum $h_{FE}$ of the output transistors. The bandwidth of the amplifier is determined by the capacitor, $C_1$. If $C_1$ is increased to 390 pF the high frequency 3.0 dB point is typically 20 kHz.

* Differences may be found in idle current when matching this device to various output transistor types. It is suggested that a 10k potentiometer be placed between Pins 1 and 4 in series with a 100 Ohm resistor. This will allow for a reduction in quiescent current. Care should be taken not to allow the idle current to fall below 1 mA to avoid crossover distortion.

## TYPICAL 10-WATT AMPLIFIER APPLICATION AND CHARACTERISTICS

($T_A$ = +25°C unless otherwise noted.)

FIGURE 7 – APPLICATION CIRCUIT*



$V_{CC}$
47 k
R1
100
820 k
R2
0.1 µF
3
2
$R_B$*
5
4
+$C_B$
10 µF
MC3320P
Q1
$R_E$
$e_{in}$ 10 µF
1.0 M
R3
6
8
7
1
$R_E$
$C_O$
500 µF
Q2
C1*
8 Ω
R4
100 k
10 µF
1 k
*Select
10-Watt Amplifier
$R_B$ = 4.7 kΩ
$R_E$ = 0.33 Ω
$V_{CC}$ = 30 V
10-Watt Amplifier
Q1 – MJE521 or equiv
Q2 – MJE371 or equiv

(Select C1 to provide desired bandwidth. C1 = 47 pF minimum)

FIGURE 8 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER

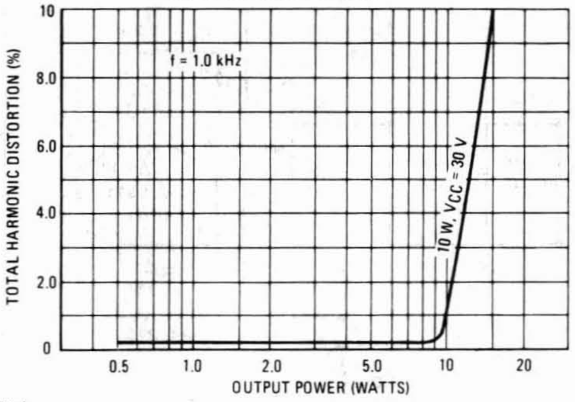


FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY

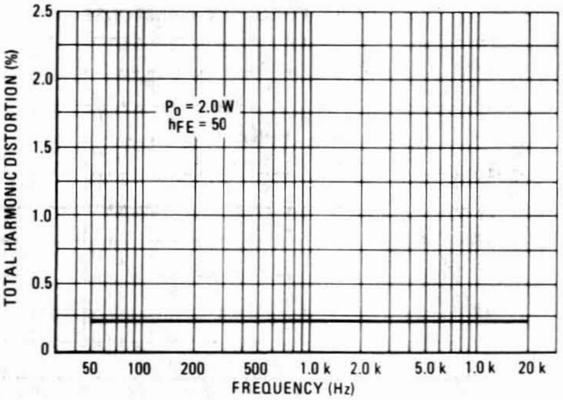
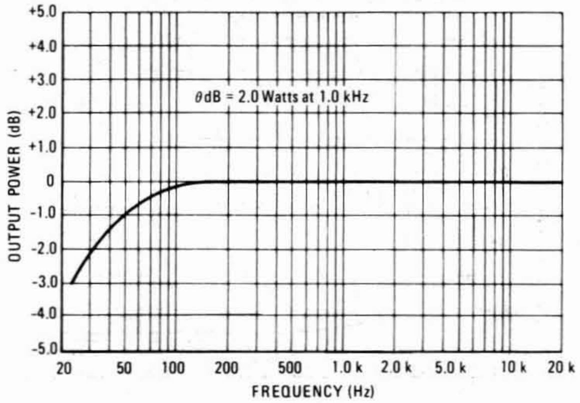


FIGURE 10 – FREQUENCY RESPONSE



### APPLICATIONS INFORMATION for MC3320P (10 Watt Amplifiers)

The MC3320P is a high-voltage device capable of driving 10 Watt audio amplifiers. The gain of the circuit shown in Figure 7 changes when the value of R4 is varied and the bandwidth is determined by C1. Emitter resistors are required at the higher voltages used for 10 Watt audio amplifiers to provide thermal stability. The value of $R_E$ is a function of the heatsink thermal resistance and supply voltage. The heatsink requirements for operation at +65°C (with both devices mounted on the same heatsink) is about 14°C/W for the 10-Watt amplifier. If the maximum ambient operating temperature is reduced then the heatsink can be reduced in size as calculated by

$$\theta SA = \frac{T_J - (\theta JS)\, P_D - T_A}{P_D}$$

where

θSA = Heatsink thermal resistance

$T_J$ = Maximum junction operating temperature

θJS = Junction to heatsink thermal resistance (includes all surface interface components for thermal resistance such as the insulating washer)

$P_D$ = Maximum power dissipation of transistors (This occurs at about 60% of maximum output power) 6.0 W for 10 W, 7.2 W for 12 W

$T_A$ = Maximum ambient temperature

* Differences may be found in idle current when matching this device to various output transistor types. It is suggested that a 10k potentiometer be placed between Pins 1 and 4 in series with a 100 Ohm resistor. This will allow for a reduction in quiescent current. Care should be taken not to allow the idle current to fall below 1 mA to avoid crossover distortion.

**MOTOROLA**

# MC3325

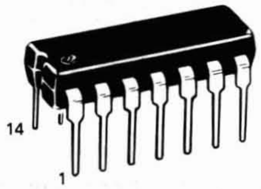
## AUTOMOTIVE VOLTAGE REGULATOR

### SILICON MONOLITHIC INTEGRATED CIRCUIT

## AUTOMOTIVE VOLTAGE REGULATOR

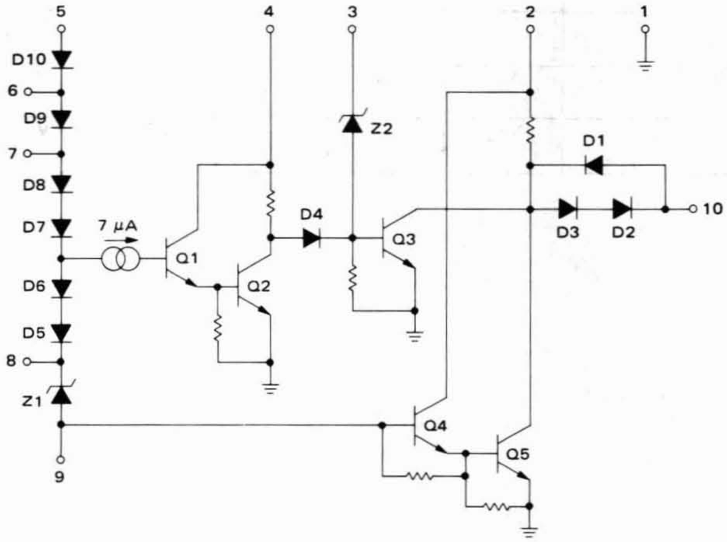
. . . designed for use in conjunction with an NPN Darlington transistor in a floating field alternator charging system.

- Overvoltage Protection
- Shut-Down on Loss of Battery Sense
- Selectable Temperature Coefficient
- Available in Chip Form for Hybrid Assembly

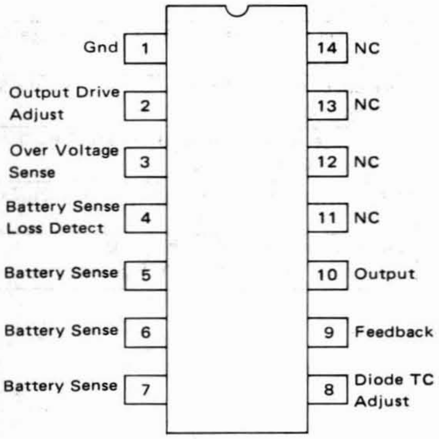


**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

### CIRCUIT SCHEMATIC


5
4
3
2
1
D10
6
D9
7
D8
D7
7 µA
Q1
Q2
D4
Z2
Q3
D1
D3
D2
10
D6
D5
8
Z1
Q4
Q5
9

### PIN CONNECTIONS


Gnd 1
Output Drive Adjust 2
Over Voltage Sense 3
Battery Sense Loss Detect 4
Battery Sense 5
Battery Sense 6
Battery Sense 7
14 NC
13 NC
12 NC
11 NC
10 Output
9 Feedback
8 Diode TC Adjust

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC3325P | -40 to +85°C | Plastic DIP |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Current Into Pins 5, 6, and 7 | $I_{5,6,\text{ or }7}$ | 50 | mA |
| Current Into Pin 3 | $I_3$ | 20 | mA |
| Current Into Pin 4 | $I_4$ | 20 | mA |
| Current Into Pin 2 | $I_2$ | 120 | mA |
| Current Into Pin 8 | $I_8$ | 50 | mA |
| Current Into Pin 9 | $I_9$ | 50 | mA |
| Current Into Pin 10 | $I_{10}$ | 50 | mA |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Temperature Range | $T_A$ | -40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise specified.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Diode TC Adjust: Threshold Voltage on Pin 8 (Figure 1) | $V_8$ | 7.9 | – | 8.95 | V |
| Battery Sense: Threshold Voltage on Pin 5 (Figure 1) | $V_5$ | 11.8 | – | 13.45 | V |
| Battery Sense: Threshold Voltage on Pin 6 (Figure 1) | $V_6$ | 11.1 | – | 12.75 | V |
| Battery Sense: Threshold Voltage on Pin 7 (Figure 1) | $V_7$ | 10.5 | – | 11.9 | V |
| Battery Sense Loss Detect: Threshold Current Into Pin 4 (Figure 2) | $I_4$ | – | – | 600 | μA |
| Battery Sense Loss Detect: Threshold Voltage at Pin 4 ($I_4 \leq 400\ \mu A$, Figure 2) | $V_4$ | 1.3 | – | 1.7 | V |
| Overvoltage Sense: Threshold Current Into Pin 3 (Figure 2) | $I_3$ | – | – | 600 | μA |
| Overvoltage Sense: Threshold Voltage at Pin 3 ($I_3 \leq 400\ \mu A$, Figure 2) | $V_3$ | 6.7 | – | 9.0 | V |
| Output Drive Adjust: Voltage Drop from Pin 2 to Pin 10 ($I_2$ = 10 mA, Figure 3) | $V_2$ | 1.9 | – | 2.4 | V |
| Low State Output Voltage at Pin 10 ($I_3$ = 12 mA, $I_2$ = 120 mA, Figure 4) | $V_{10}$ | – | – | 0.7 | V |

## TEST CIRCUITS

FIGURE 1

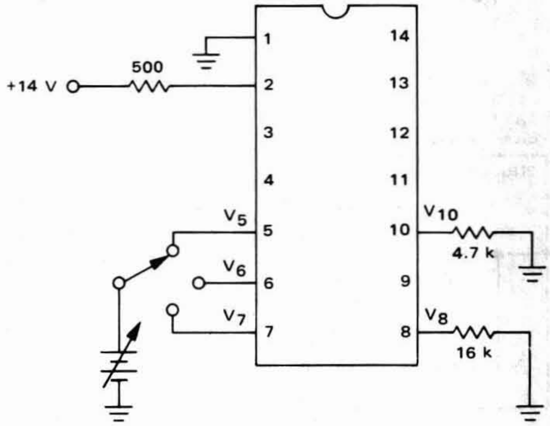

+14 V
500
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V5
V6
V7
V10
4.7 k
V8
16 k

FIGURE 2

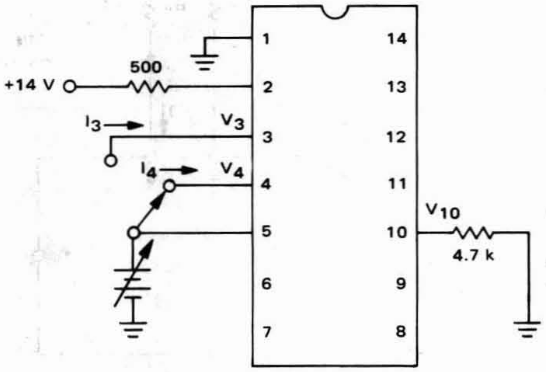

+14 V
500
I3
V3
I4
V4
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V10
4.7 k

FIGURE 3

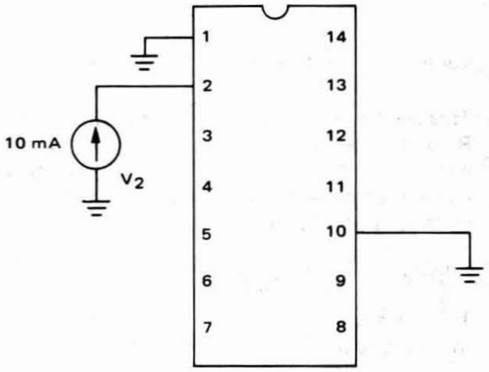

10 mA
V2
1
2
3
4
5
6
7
14
13
12
11
10
9
8

FIGURE 4

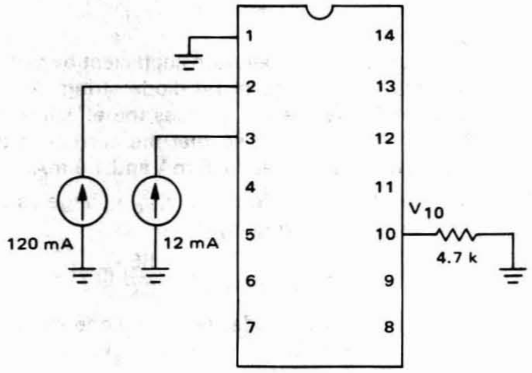
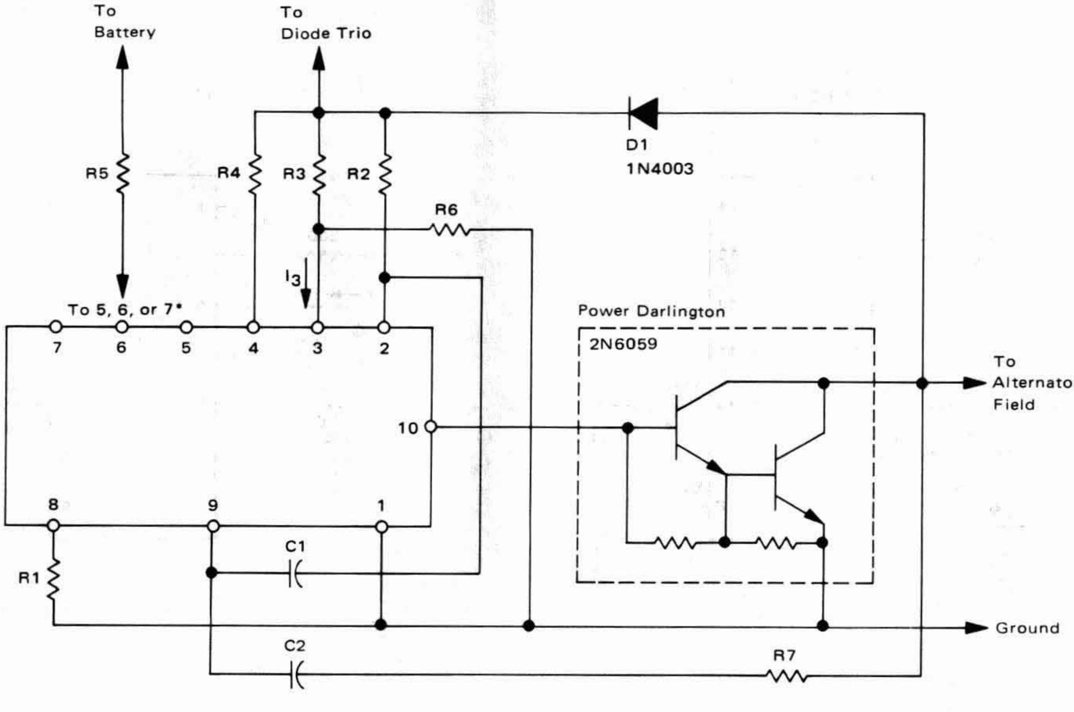

120 mA
12 mA
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V10
4.7 k

**FIGURE 5 — APPLICATION CIRCUIT**



*Note: The temperature coefficient of the battery voltage sense terminal is determined by the number of diodes used in the diode string (i.e., whether Pin 5, 6, or 7 is used). The approximate temperature coefficient for a diode at 1.0 mA is −2.0 mV/°C, and for a zener diode it is +3.0 mV/°C. Counting from ground (see circuit schematic) we have −2.0 mV for Q5, −2.0 mV for Q4, +3.0 mV for Z1, −8.0 mV for D5 thru D8, and an additional −2.0 mV each for D9 and D10 if used. The total temperature coefficient can be varied from approximately −9.0 mV/°C to −13 mV/°C depending on the number of the diodes in the diode string that are utilized.

## APPLICATIONS CIRCUIT INFORMATION

**(See Figure 5)**

R1 Determines the temperature coefficient by setting the value of current in the diode string. As the value of R1 decreases, so does the effective TC. R1 should be chosen so that the current in the diode string is between 0.5 mA and 1.0 mA.

R5 This resistor determines the $V_{reg}$ voltage as defined by the following equation:

$$V_{reg} = (1 + \frac{R5}{R1})\ 8.4 + (n + \frac{R5}{5K})\ (0.7)$$

n = number of diodes used in diode string $(4 \leq n \leq 6)$

R4 Used as a current limiting resistor on Pin 4 in case of an open battery voltage sense lead.

R3 Used as a current limiting resistor on Pin 3 in case of overvoltage at the diode trio. Voltage at Pin 3 will run approximately 7.5 volts. R3 should be chosen so that the current ($I_3$) at maximum overvoltage is between 2.0 mA and 6.0 mA.

R2 This resistor determines the output drive current. Refer to specifications for the darlington driver and select the value for R2 that will provide enough drive to the output when the diode trio voltage is at a minimum.

$$I_{Drive} \cong \frac{V_{min} - 2.8\ V}{R2 + 50\ \Omega}$$

R6 This resistor in conjunction with R3 is used to set the threshold of overvoltage action.

$$\text{Threshold} \cong \frac{R3 + R6}{R6}\ (7.5)$$

R7 Used for compensation (Approximately 3.0 kΩ)

C1, C2 Used for compensation (Approximately 0.01 μF)

**MOTOROLA**

# MC3334P
# MCC3334
# MCCF3334

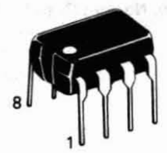
## HIGH ENERGY IGNITION CIRCUIT

. . . designed to use the signal from a reluctor type ignition pickup to produce a well controlled output from a power Darlington output transistor.

- Very Low Peripheral Component Count
- No Critical System Resistors
- Wide Supply Voltage Operating Range (4.0–24 V)
- Overvoltage Shutdown (30 V)
- Dwell Automatically Adjusts To Produce Optimum Stored Energy Without Waste
- Externally Adjustable Peak Current
- Available in Chip and Flip Chip Form
- Transient Protected Inputs and Outputs

## HIGH ENERGY IGNITION CIRCUIT

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

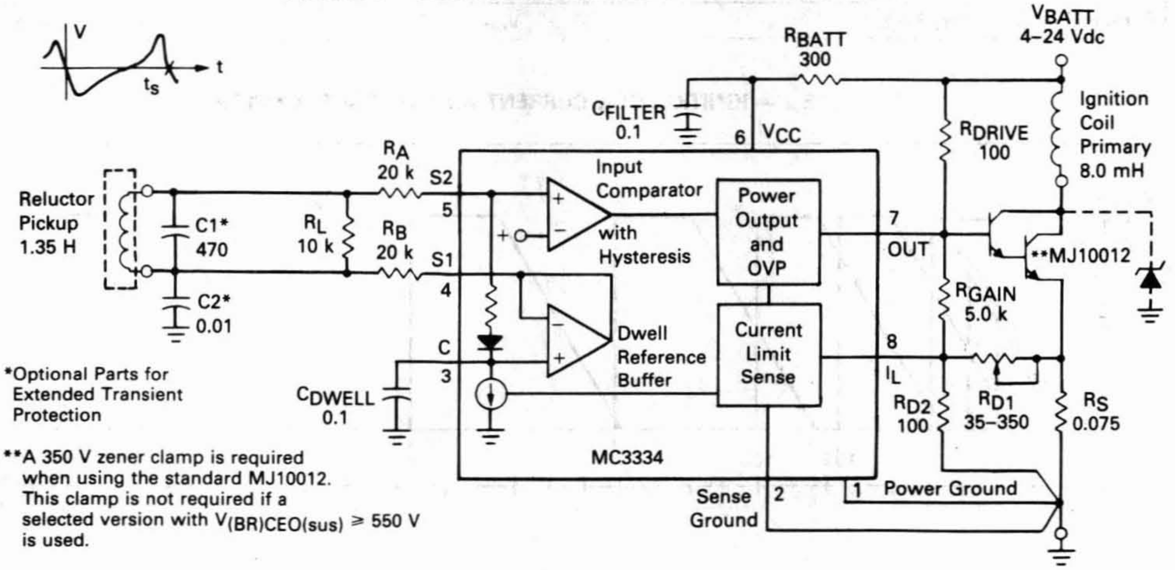
### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage — Steady State<br>Transient 300 ms or less | $V_{BATT}$ | 24<br>90 | Volts |
| Output Sink Current — Steady State<br>Transient 300 ms or less | $I_{out}$ | 300<br>1.0 | mA<br>Amps |
| Junction Temperature | $T_{J(max)}$ | 150 | °C |
| Operating Temperature Range | $T_A$ | −40 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Power Dissipation, Package<br>Derate above 25°C | $P_D$ | 1.25<br>10 | Watts<br>mW/°C |

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC3334P | −40 to +125 | Plastic DIP |
| MCC3334 | −40 to +125 | Chip |
| MCCF3334 | −40 to +125 | Flip-Chip |

FIGURE 1 — BLOCK DIAGRAM AND TYPICAL APPLICATION


V
t
$t_s$
$R_{BATT}$
300
$V_{BATT}$
4–24 Vdc
$C_{FILTER}$
0.1
6
$V_{CC}$
Ignition
Coil
Primary
8.0 mH
$R_{DRIVE}$
100
$R_A$
20 k
S2
5
Input
Comparator
with
Hysteresis
Power
Output
and
OVP
7
OUT
**MJ10012
Reluctor
Pickup
1.35 H
C1*
470
$R_L$
10 k
$R_B$
20 k
S1
4
C2*
0.01
$R_{GAIN}$
5.0 k
C
3
Dwell
Reference
Buffer
Current
Limit
Sense
8
$I_L$
$C_{DWELL}$
0.1
$R_{D2}$
100
$R_{D1}$
35–350
$R_S$
0.075
MC3334
Sense
Ground
2
1
Power Ground

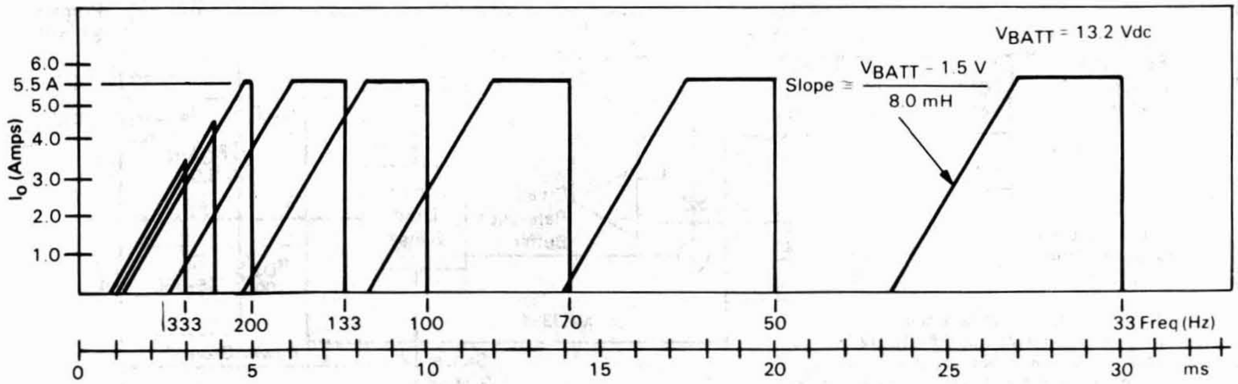
*Optional Parts for Extended Transient Protection

**A 350 V zener clamp is required when using the standard MJ10012. This clamp is not required if a selected version with $V_{(BR)CEO(sus)} \geq 550$ V is used.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = −40 to +125°C, $V_{BATT}$ = 13.2 Vdc, circuit of Figure 1, unless noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Internal Supply Voltage, Pin 6 | $V_{CC}$ | | | | Vdc |
| $V_{BATT}$ = 4.0 Vdc | | — | 3.5 | — | |
| 8.0 Vdc | | — | 7.2 | — | |
| 12.0 | | — | 10.4 | — | |
| 14.0 | | — | 11.8 | — | |
| Ignition Coil Current Peak, Cranking RPM 2.0 - 27 Hz | $I_{o(pk)}$ | | | | A pk |
| $V_{BATT}$ = 4.0 Vdc | | 3.0 | 3.4 | — | |
| 6.0 | | 4.0 | 5.2 | — | |
| 8.0 | | 4.6 | 5.3 | — | |
| 10.0 | | 5.1 | 5.4 | — | |
| Ignition Coil Current Peak, Normal RPM | $I_{o(pk)}$ | | | | A pk |
| Freq. = 33 Hz | | 5.1 | 5.5 | — | |
| 133 Hz | | 5.1 | 5.5 | — | |
| 200 Hz | | 4.2 | 5.4 | — | |
| 267 Hz | | 3.4 | 4.4 | — | |
| 333 Hz | | 2.7 | 3.4 | — | |
| Ignition Coil On-Time, Normal RPM Range | $t_{on}$ | | | | ms |
| Freq. = 33 Hz | | — | 7.5 | 14.0 | |
| 133 Hz | | — | 5.0 | 5.9 | |
| 200 Hz | | — | 4.0 | 4.6 | |
| 267 Hz | | — | 3.0 | 3.6 | |
| 333 Hz | | — | 2.3 | 2.8 | |
| Shutdown Voltage | $V_{BATT}$ | 25 | 30 | 35 | Vdc |
| Input Threshold (Static Test) | $V_{S2}$-$V_{S1}$ | | | | mVdc |
| Turn-on | | — | 360 | — | |
| Turn-off | | — | 90 | — | |
| Input Threshold Hysteresis | $V_{S2}$-$V_{S1}$ | 75 | — | — | mVdc |
| Input Threshold (Active Operation) | $V_{S2}$ | | | | Vdc |
| Turn-on | | — | 1.8 | — | |
| Turn-off | | — | 1.5 | — | |
| Total Circuit Lag from $t_s$ (Figure 1) until Ignition Coil Current Falls to 10% | | — | 60 | 120 | µs |
| Ignition Coil Current Fall Time (90%-10%) | | — | 4.0 | — | µs |
| Saturation Voltage I.C. Output (Pin 7) ($R_{DRIVE}$ = 100 Ω) | $V_{CE(sat)}$ | | | | mVdc |
| $V_{BATT}$ = 10 Vdc | | — | 120 | — | |
| 30 Vdc | | — | 280 | — | |
| 50 Vdc | | — | 540 | — | |
| Current Limit Reference, Pin 8 | $V_{ref}$ | 120 | 160 | 190 | mVdc |

**FIGURE 2 — IGNITION COIL CURRENT versus FREQUENCY/PERIOD**



The MC3334 high energy ignition circuit was designed to serve aftermarket Delco five terminal ignition applications. This device, driving a high voltage Darlington transistor, offers an ignition system which optimizes spark energy at minimum power dissipation. The IC is pinned out to permit thick film or printed circuit module design without any crossovers.

## CIRCUIT DESCRIPTION

The basic function of an ignition circuit is to permit build-up of current in the primary of a spark coil, and then to interrupt the flow at the proper firing time. The resulting flyback action in the ignition coil induces the required high secondary voltage needed for the spark. In the simplest systems, fixed dwell angle produces a fixed duty cycle, which can result in too little stored energy at high RPM, and/or wasted power at low RPM. The MC3334 uses a variable dc voltage reference, stored on $C_{DWELL}$, and buffered to the bottom end of the reluctor pickup (S1) to vary the duty cycle at the spark coil. At high RPM, the MC3334 holds the output "off" for approximately 1.0 ms to permit full energy discharge from the previous spark; then it switches the output Darlington transistor into full saturation. The current ramps up at a slope dictated by $V_{BATT}$ and the coil L. At very high RPM the peak current may be less than desired, but it is limited by the coil itself.

As the RPM decreases, the ignition coil current builds up and would be limited only by series resistance losses. The MC3334 provides adjustable peak current regulation sensed by $R_S$ and set by $R_{D1}$, in this case at 5.5 A, as shown in Figure 2. As the RPM decreases further, the coil current is held at 5.5 A for a short period. This provides a reserve for sudden acceleration, when discharge may suddenly occur earlier than expected. The peak hold period is about 20% at medium RPM, decreasing to about 10% at very low RPM. (Note: 333 Hz = 5000 RPM for an eight cylinder four stroke engine.) At lower $V_{BATT}$, the "on" period automatically stretches to accommodate the slower current build-up. At very low $V_{BATT}$ and low RPM, a common condition during cold starting, the "on" period is nearly the full cycle to permit as much coil current as possible.

The output stage of the IC is designed with an OVP circuit which turns it on at $V_{BATT} \approx 30$ V ($V_{CC} \approx 22$ V), holding the output Darlington off. This protects the IC and the Darlington from damage due to load dump or other causes of excessive $V_{BATT}$.

## COMPONENT VALUES

PICKUP — series resistance = 800 Ω ± 10% @ 25°C
inductance = 1.35 H @ 1.0 kHz @ 15 Vrms.

COIL — leakage L = 0.6 mH
primary R = 0.43 Ω ± 5% @ 25°C
primary L = 7.5 to 8.5 mH @ 5.0 A

$R_L$ — load resistor for pick-up = 10 kΩ ± 20%

$R_A$, $R_B$ — input buffer resistors, provide additional transient protection to the already clamped inputs = 20 k ± 20%

C1, C2 — for reduction of high frequency noise and spark transients induced in pick-up and leads; optional and non-critical

$R_{BATT}$ — provides load dump protection (but small enough to allow operation at $V_{BATT}$ = 4.0 V) = 300 Ω ± 20%

$C_{FILTER}$ — transient filter on $V_{CC}$, non-critical

$C_{DWELL}$ — stores reference, circuit designed for 0.1 μF ± 20%

$R_{GAIN}$ — $R_{GAIN}/R_{D1}$ sets the dc gain of the current regulator = 5.0 k ± 20%

$R_{D2}$ — $R_{D2}/R_{D1}$ set up voltage feedback from $R_S$

$R_S$ — sense resistor (PdAg in thick film techniques) = 0.075 Ω ± 30%

$R_{DRIVE}$ — low enough to supply drive to the output Darlington, high enough to keep $V_{CE(sat)}$ of the IC below Darlington turn-on during load dump = 100 Ω ± 20%, 5.0 W

$R_{D1}$ — starting with 35 Ω assures less than 5.5 A, increasing as required to set 5.5 A

$$R_{D1} = \frac{I_{o(pk)}\, R_S - V_{ref}}{\frac{V_{ref}}{R_{D2}} - \frac{1.4}{R_{GAIN}}} - \approx 100\ \Omega\ \text{(nom)}$$

## GENERAL LAYOUT NOTES

The major concern in the substrate design should be to reduce ground resistance problems. The first area of concern is the metallization resistance in the power ground to module ground and the output to the $R_{DRIVE}$ resistor. This resistance directly adds to the $V_{CE(sat)}$ of the IC power device and if not minimized could cause failure in load dump. The second concern is to reference the sense ground as close to the ground end of the sense resistor as possible in order to further remove the sensitivity of ignition coil current to ground I.R. drops.

All versions were designed to provide the same pin-out order viewed from the top (component side) of the board or substrate. This was done to eliminate conductor cross-overs. The standard MC3334 plastic device is numbered in the industry convention, counter-clockwise viewed from the top. The MCC3334 chip version is made from the same die artwork, so it is also counter-clockwise viewed from the top, or bonding pad side. The MCCF3334 "flip" or "bump" chip is made from reversed artwork, so it is numbered clockwise viewed from its bump side. Since this chip is mounted face down, the resulting assembly still has the same counter-clockwise order viewed from above the component surface. All chips have the same size and bonding pad spacing. See Figure 4 for dimensions.

FIGURE 3 — INTERNAL SCHEMATIC

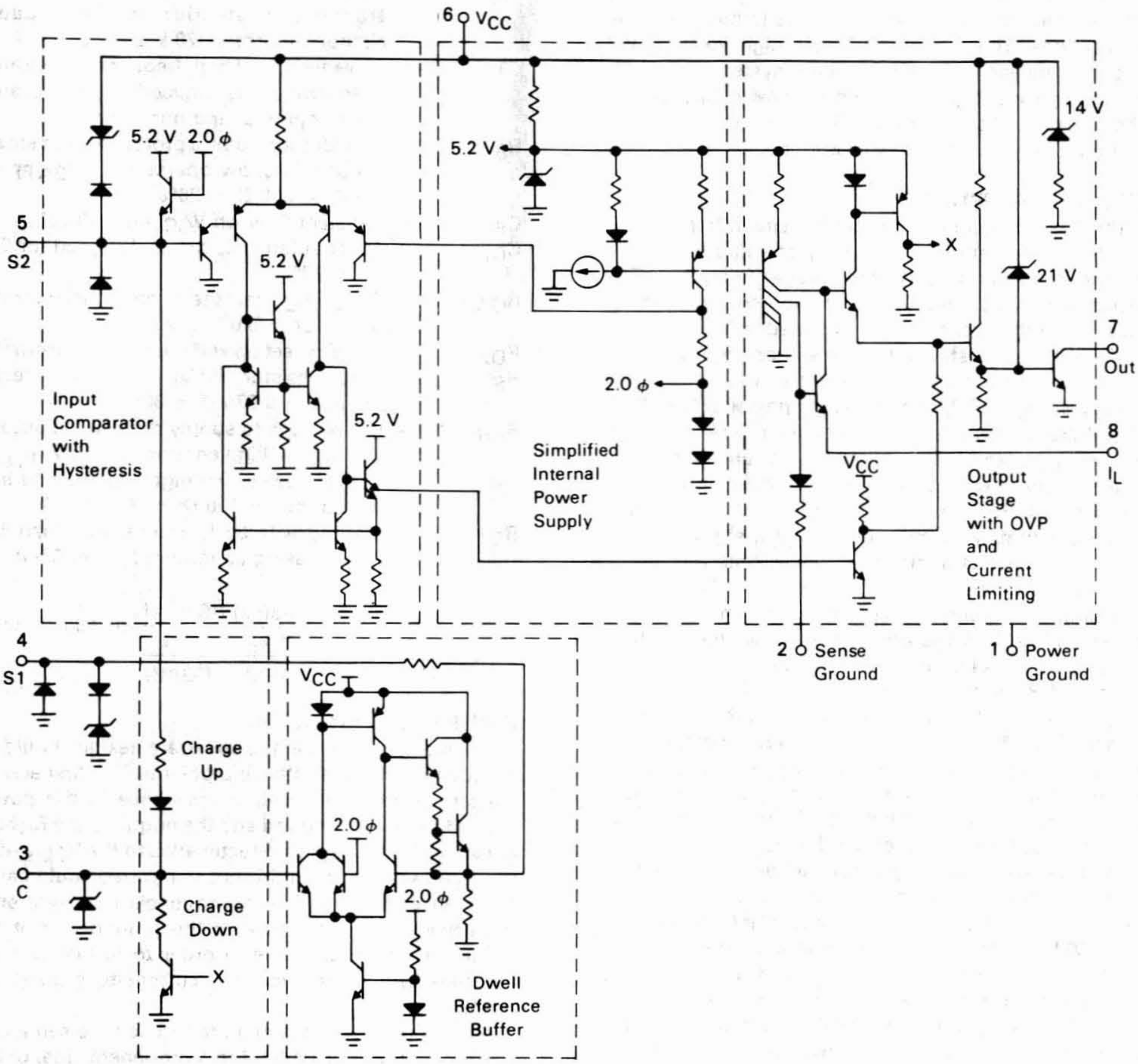
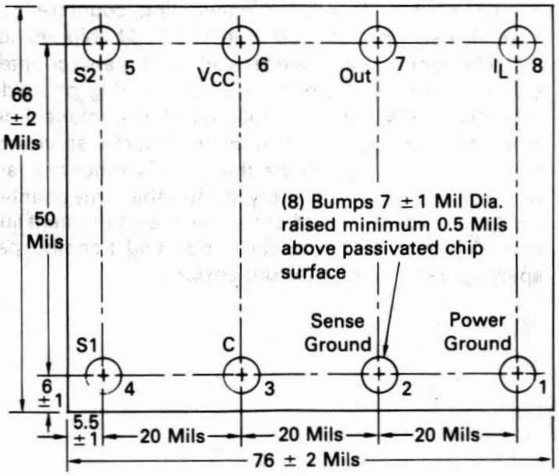

6 VCC
5.2 V
2.0 ϕ
5
S2
5.2 V
5.2 V
Input
Comparator
with
Hysteresis
5.2 V
Simplified
Internal
Power
Supply
2.0 ϕ
X
14 V
21 V
7
Out
8
IL
VCC
Output
Stage
with OVP
and
Current
Limiting
2 Sense
Ground
1 Power
Ground
4
S1
Charge
Up
3
C
Charge
Down
X
VCC
2.0 ϕ
2.0 ϕ
Dwell
Reference
Buffer

FIGURE 4 — MCCF3334 IGNITION CIRCUIT BUMP SIDE VIEW


S2 5
VCC 6
Out 7
IL 8
66
±2
Mils
50
Mils
(8) Bumps 7 ±1 Mil Dia.
raised minimum 0.5 Mils
above passivated chip
surface
S1
C
Sense
Ground
Power
Ground
4
3
2
1
6
±1
5.5
±1
20 Mils
20 Mils
20 Mils
76 ± 2 Mils

# MC3340P

## ELECTRONIC ATTENUATOR

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

**ORDERING INFORMATION**

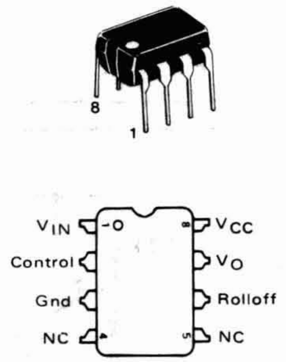
| Device | Temperature Range | Package |
|---|---|---|
| MC3340P | 0°C to +70°C | Plastic DIP |

## ELECTRONIC ATTENUATOR

- Designed for use in:
  - DC Operated Volume Control
  - Compression and Expansion Amplifier Applications
- Controlled by DC Voltage or External Variable Resistor
- Economical 8-Pin Dual In-Line Package
- Formerly MFC6040 in Case 643A Package

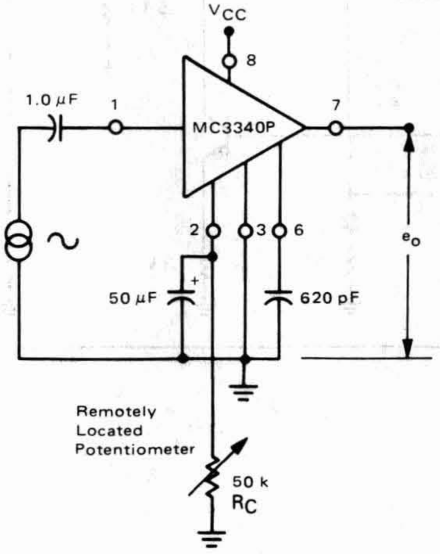
**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted.)

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage | 20 | Vdc |
| Power Dissipation @ $T_A$ = 25°C<br>Derate above $T_A$ = 25°C | 1.2<br>10 | Watts<br>mW/°C |
| Operating Ambient Temperature Range | 0 to +70 | °C |


8
1
VIN
Control
Gnd
NC
VCC
VO
Rolloff
NC

**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

FIGURE 1 – TYPICAL DC "REMOTE" VOLUME CONTROL


VCC
8
1.0 µF
1
7
MC3340P
2
3
6
eo
50 µF
620 pF
Remotely Located Potentiometer
50 k
RC

**ELECTRICAL CHARACTERISTICS** ($e_{in}$ = 100 mV (RMS), f = 1.0 kHz, $V_{CC}$ = 16 Vdc, $T_A$ = +25°C unless otherwise noted.)

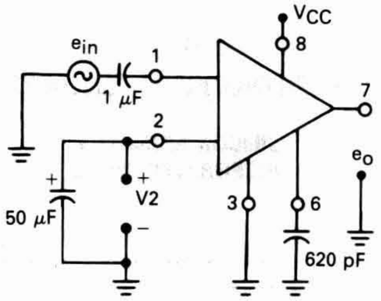
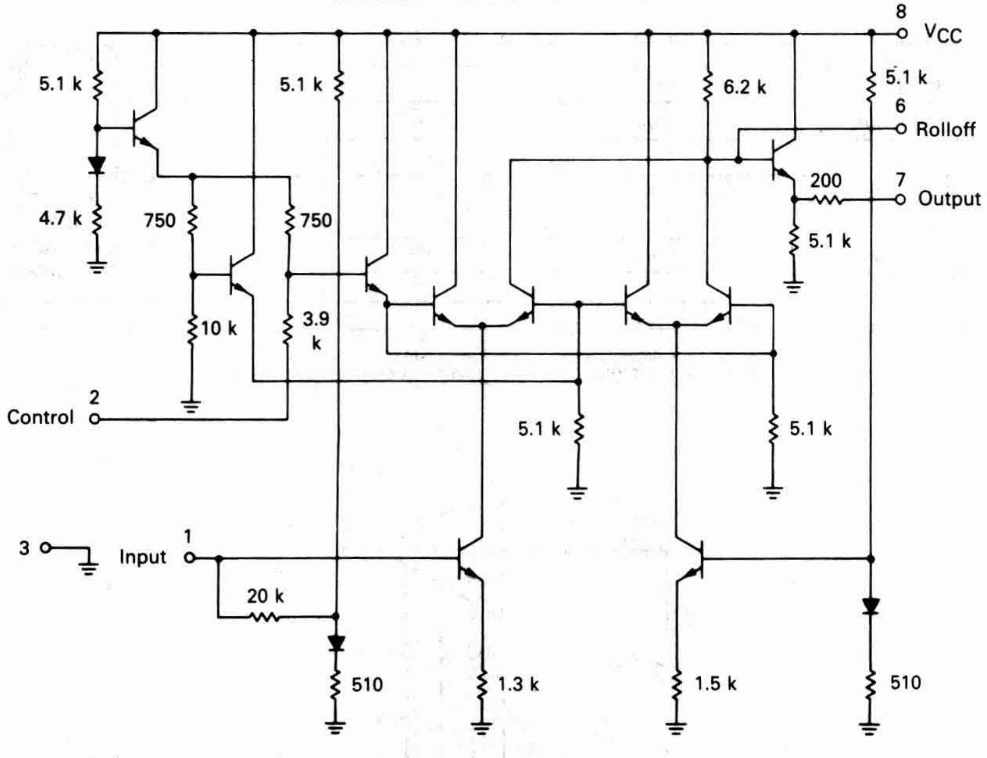
| Circuit | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
|  VCC<br>8<br>e<sub>in</sub><br>1<br>1 µF<br>7<br>2<br>e<sub>o</sub><br>+<br>+<br>V2<br>–<br>50 µF<br>3<br>6<br>620 pF | Operating Power Supply Voltage | 8.0 | — | 18 | Vdc |
| | Control Terminal Sink Current, Pin 2 ($e_{in}$ = 0) | — | — | 2.0 | mAdc |
| | Maximum Input Voltage | — | — | 0.5 | V(RMS) |
| | Voltage Gain | 11 | 13 | — | dB |
| | **Attenuation Range from Max Gain (V2 = 6.5 Vdc)** | 70 | 80 | — | dB |
| | Total Harmonic Distortion (Pin 2 Gnd) ($e_{in}$ = 100 mV (RMS), $e_o$ = $A_v$ x $e_{in}$) | — | 0.6 | 1.0 | % |

**FIGURE 2 — CIRCUIT SCHEMATIC**


8
VCC
5.1 k
5.1 k
6.2 k
5.1 k
6
Rolloff
200
7
Output
4.7 k
750
750
5.1 k
3.9 k
10 k
2
Control
5.1 k
5.1 k
3
Input
1
20 k
510
1.3 k
1.5 k
510

## TYPICAL ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 16 Vdc, $T_A$ = +25°C unless otherwise noted.)

FIGURE 3 – ATTENUATION versus DC CONTROL VOLTAGE

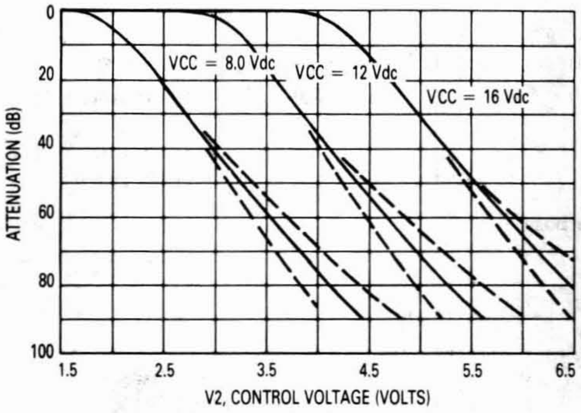


FIGURE 4 – ATTENUATION versus CONTROL RESISTOR

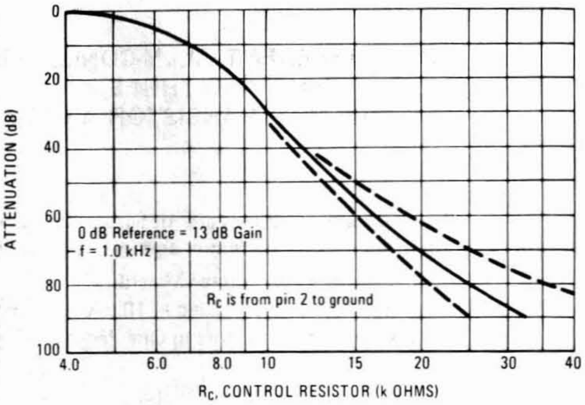


FIGURE 5 – FREQUENCY RESPONSE

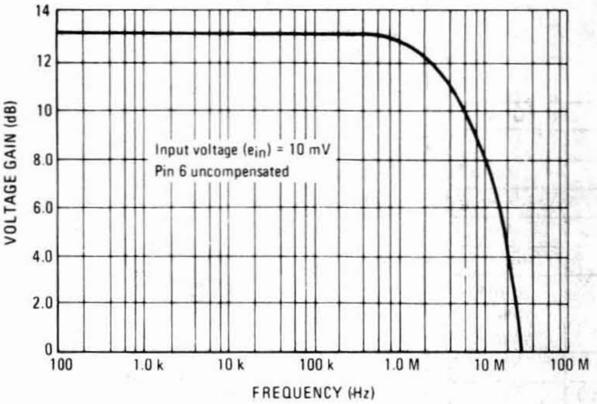


FIGURE 6 – OUTPUT VOLTAGE SWING

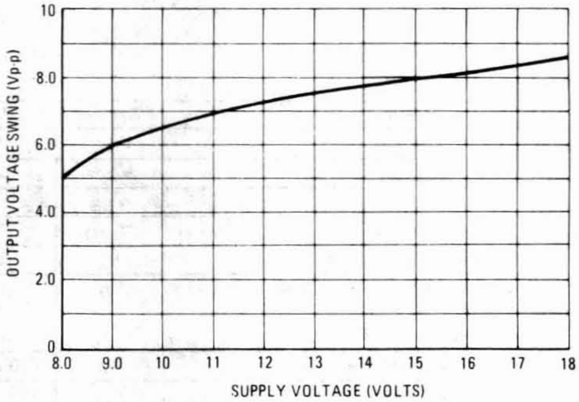
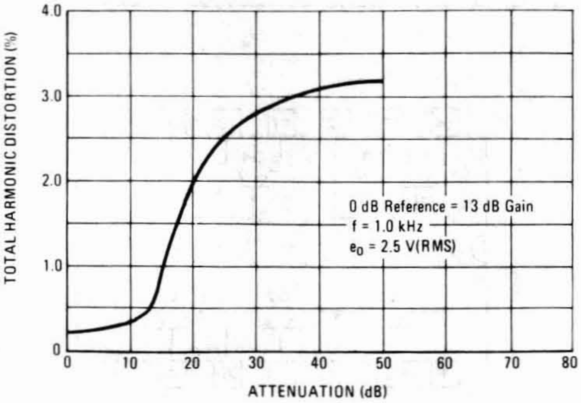


FIGURE 7 – TOTAL HARMONIC DISTORTION



# MC3346
# MC3386

**ORDERING INFORMATION**

| Device | Temperature Range | Package |
|---|---|---|
| MC3346D | −40°C to +85°C | SO-14 |
| MC3346P | −40°C to +85°C | Plastic DIP |
| MC3386D | −40°C to +85°C | SO-14 |
| MC3386P | −40°C to +85°C | Plastic DIP |

## ONE DIFFERENTIALLY-CONNECTED PAIR AND THREE ISOLATED TRANSISTOR ARRAY

The MC3346 and MC3386 are designed for general-purpose, low power applications for consumer and industrial designs.

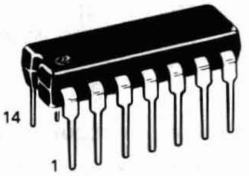
- Guaranteed Base-Emitter Voltage Matching
- Operating Current Range Specified — 10 μA to 10 mA
- Five General-Purpose Transistors in One Package

## GENERAL PURPOSE TRANSISTOR ARRAY

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

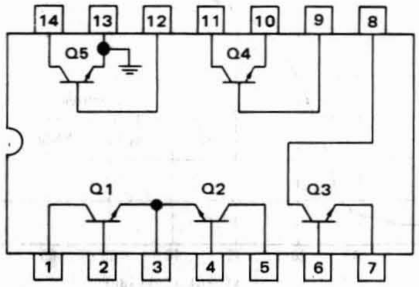
**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector-Emitter Voltage | $V_{CEO}$ | 15 | Vdc |
| Collector-Base Voltage | $V_{CBO}$ | 20 | Vdc |
| Emitter-Base Voltage | $V_{EB}$ | 5.0 | Vdc |
| Collector-Substrate Voltage | $V_{CIO}$ | 20 | Vdc |
| Collector Current — Continuous | $I_C$ | 50 | mAdc |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C<br>Derate Each Transistor @ 25°C | $P_D$ | 1.2<br>10<br>300 | Watts<br>mW/°C<br>mW/°C |
| Operating Temperature Range | $T_A$ | −40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

**D SUFFIX**
PLASTIC PACKAGE
CASE 751A-01
SO-14



Pin 13 is connected to substrate and must remain at the lowest circuit potential.

## ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | MC3346P |  |  | MC3386P |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| **STATIC CHARACTERISTICS** |  |  |  |  |  |  |  |  |
| Collector-Base Breakdown Voltage ($I_C$ = 10 μAdc) | $V_{(BR)CBO}$ | 20 | 60 | – | 20 | 60 | – | Vdc |
| Collector-Emitter Breakdown Voltage ($I_C$ = 1.0 mAdc) | $V_{(BR)CEO}$ | 15 | – | – | 15 | – | – | Vdc |
| Collector-Substrate Breakdown Voltage ($I_C$ = 10 μA) | $V_{(BR)CIO}$ | 20 | 60 | – | 20 | 60 | – | Vdc |
| Emitter-Base Breakdown Voltage ($I_E$ = 10 μAdc) | $V_{(BR)EBO}$ | 5.0 | 7.0 | – | 5.0 | 7.0 | – | Vdc |
| Collector-Base Cutoff Current ($V_{CB}$ = 10 Vdc, $I_E$ = 0) | $I_{CBO}$ | – | – | 40 | – | – | 100 | nAdc |
| DC Current Gain | $h_{FE}$ |  |  |  |  |  |  | – |
| ($I_C$ = 10 mAdc, $V_{CE}$ = 3.0 Vdc) |  | – | 140 | – | – | – | – |  |
| ($I_C$ = 1.0 mAdc, $V_{CE}$ = 3.0 Vdc) |  | 40 | 130 | – | 40 | 130 | – |  |
| ($I_C$ = 10 μAdc, $V_{CE}$ = 3.0 Vdc) |  | – | 60 | – | – | – | – |  |
| Base-Emitter Voltage | $V_{BE}$ |  |  |  |  |  |  | Vdc |
| ($V_{CE}$ = 3.0 Vdc, $I_E$ = 1.0 mAdc) |  | – | 0.72 | – | – | 0.72 | – |  |
| ($V_{CE}$ = 3.0 Vdc, $I_E$ = 10 mAdc) |  | – | 0.80 | – | – | 0.80 | – |  |
| Input Offset Current for Matched Pair Q1 and Q2 ($V_{CE}$ = 3.0 Vdc, $I_C$ = 1.0 mAdc) | $\|I_{IO1}-I_{IO2}\|$ | – | 0.3 | 2.0 | – | 0.3 | – | μAdc |
| Magnitude of Input Offset Voltage ($V_{CE}$ = 3.0 Vdc, $I_C$ = 1.0 mAdc) | – | – | 0.5 | 5.0 | – | 0.5 | – | mVdc |
| Temperature Coefficient of Base-Emitter Voltage ($V_{CE}$ = 3.0 Vdc, $I_C$ = 1.0 mAdc) | $\frac{\Delta V_{BE}}{\Delta T}$ | – | -1.9 | – | – | -1.9 | – | mV/°C |
| Temperature Coefficient | $\frac{\|\Delta V_{IO}\|}{\Delta T}$ | – | 1.0 | – | – | 1.0 | – | μV/°C |
| Collector-Emitter Cutoff Current ($V_{CE}$ = 10 Vdc, $1_B$ = 0) | $I_{CEO}$ | – | – | 0.5 | – | – | 5.0 | μAdc |
| **DYNAMIC CHARACTERISTICS** |  |  |  |  |  |  |  |  |
| Low Frequency Noise Figure ($V_{CE}$ = 3.0 Vdc, $I_C$ = 100 μAdc, $R_S$ = 1.0 kΩ, f = 1.0 kHz) | NF | – | 3.25 | – | – | 3.25 | – | dB |
| Forward Current Transfer Ratio ($V_{CE}$ = 3.0 Vdc, $I_C$ = 1.0 mAdc, f = 1.0 kHz) | $h_{FE}$ | – | 110 | – | – | 110 | – | – |
| Short-Circuit Input Impedance ($V_{CE}$ = 3.0 Vdc, $I_C$ = 1.0 mAdc) | $h_{ie}$ | – | 3.5 | – | – | 3.5 | – | kΩ |
| Open-Circuit Output Impedance ($V_{CE}$ = 3.0 Vdc, $I_C$ = 1.0 mAdc) | $h_{oe}$ | – | 15.6 | – | – | 15.6 | – | μmhos |
| Reverse Voltage Transfer Ratio ($V_{CE}$ = 3.0 Vdc, $I_C$ = 1.0 mAdc) | $h_{re}$ | – | 1.8 | – | – | 1.8 | – | $\times 10^{-4}$ |
| Forward Transfer Admittance ($V_{CE}$ = 3.0 Vdc, $I_C$ = 1.0 mAdc, f = 1.0 MHz) | $y_{fe}$ | – | 31-j1.5 | – | – | 31-j1.5 | – | – |
| Input Admittance ($V_{CE}$ = 3.0 Vdc, $I_C$ = 1.0 mAdc, f = 1.0 MHz) | $y_{ie}$ | – | 0.3+j0.04 | – | – | 0.3+j0.04 | – | – |
| Output Admittance ($V_{CE}$ = 3.0 Vdc, $I_C$ = 1.0 mAdc, f = 1.0 MHz) | $y_{oe}$ | – | 0.001+j0.03 | – | – | 0.001+j0.03 | – | – |
| Current-Gain — Bandwidth Product ($V_{CE}$ = 3.0 Vdc, $I_C$ = 3.0 mAdc) | $f_T$ | 300 | 550 | – | – | 550 | – | MHz |
| Emitter-Base Capacitance ($V_{EB}$ = 3.0 Vdc, $I_E$ = 0) | $C_{eb}$ | – | 0.6 | – | – | 0.6 | – | pF |
| Collector-Base Capacitance ($V_{CB}$ = 3.0 Vdc, $I_C$ = 0) | $C_{cb}$ | – | 0.58 | – | – | 0.58 | – | pF |
| Collector-Substrate Capacitance ($V_{CS}$ = 3.0 Vdc, $I_C$ = 0) | $C_{CI}$ | – | 2.8 | – | – | 2.8 | – | pF |

## TYPICAL CHARACTERISTICS

**FIGURE 1 – COLLECTOR CUTOFF CURRENT versus TEMPERATURE (Each Transistor)**

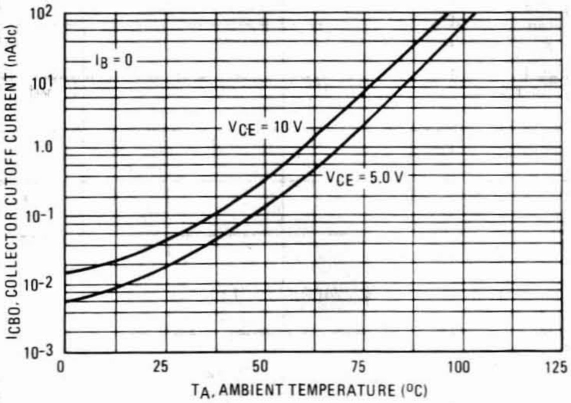


**FIGURE 2 – COLLECTOR CUTOFF CURRENT versus TEMPERATURE (Each Transistor)**

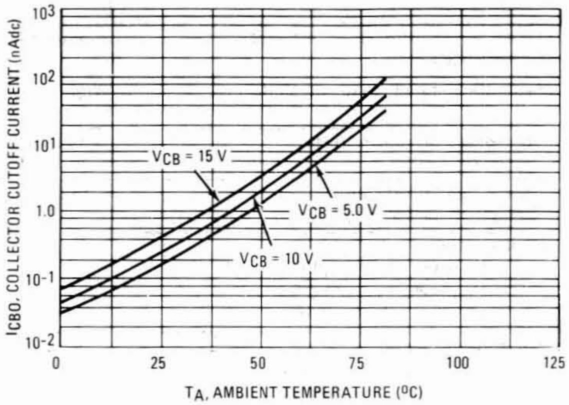


**FIGURE 3 – INPUT OFFSET CHARACTERISTICS FOR Q1 and Q2**

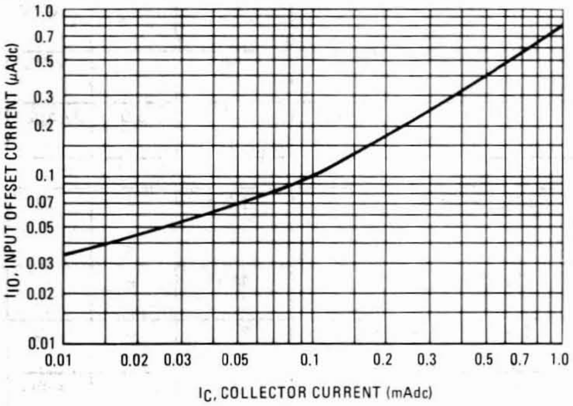


**FIGURE 4 – BASE-EMITTER AND INPUT OFFSET VOLTAGE CHARACTERISTICS**

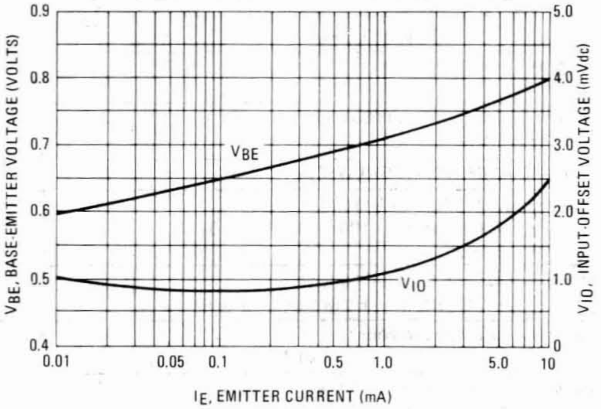
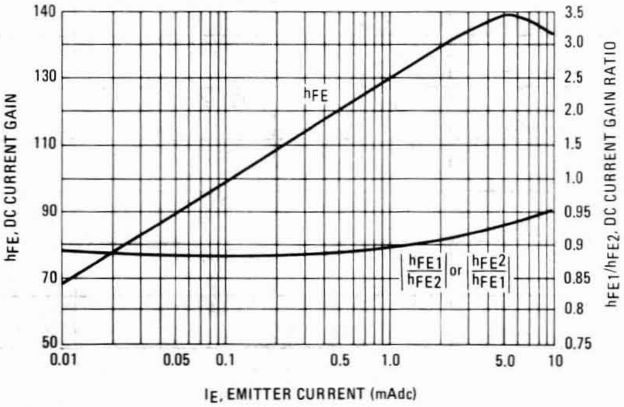


**FIGURE 5 – DC CURRENT GAIN**



**MOTOROLA**

# MC3350

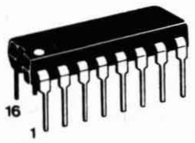
## TRIPLE INDEPENDENT DIFFERENTIAL AMPLIFIER

The MC3350 consists of three independent differential amplifiers on a common monolithic substrate. The construction technique provides close electrical and thermal matching of the amplifiers which makes this device particularly useful in multiple channel applications.

- Three Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Useful from dc to 120 MHz
- Economical Configuration

## GENERAL PURPOSE TRANSISTOR ARRAY

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

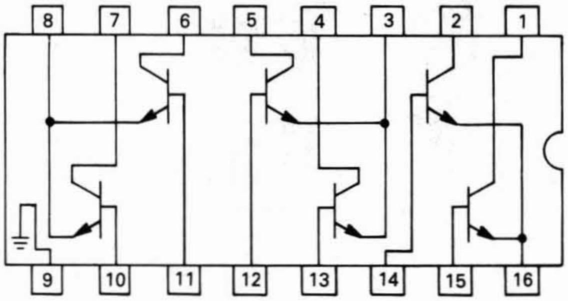
### MAXIMUM RATINGS

| Rating | | Value | Unit |
|---|---|---|---|
| Collector-Emitter Voltage | $V_{CEO}$ | 35 | Vdc |
| Collector-Base Voltage | $V_{CBO}$ | 40 | Vdc |
| Emitter-Base Voltage | $V_{EB}$ | 5.0 | Vdc |
| Collector-Substrate Voltage | $V_{CIO}$ | 40 | Vdc |
| Collector Current — Continuous | $I_C$ | 50 | mAdc |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Temperature Range | $T_A$ | −40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC3350P | 0 to 70°C | Plastic DIP |

### PIN CONNECTIONS

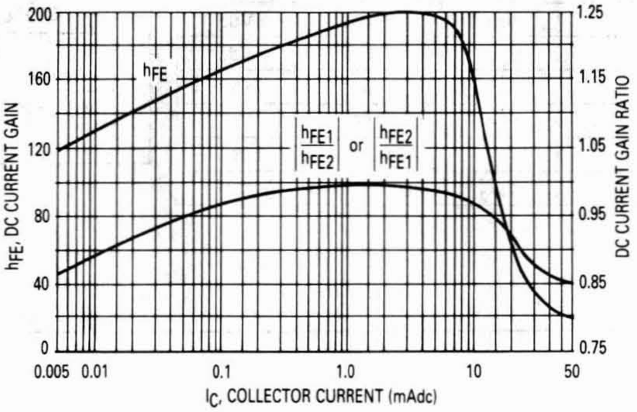


Pin 9 is connected to substrate and must remain at the lowest circuit potential.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER** | | | | | |
| Input Offset Voltage<br>$V_{CE}$ = 2.0 Vdc; $I_C$ = 1.0 mAdc | $V_{IO}$ | — | — | 5.0 | mVdc |
| **STATIC CHARACTERISTICS FOR EACH TRANSISTOR** | | | | | |
| Collector-Emitter Breakdown Voltage<br>$I_C$ = 5.0 mAdc | $V_{(BR)CEO}$ | 30 | — | — | Vdc |
| Collector-Emitter Cutoff Current<br>$V_{CE}$ = 25 Vdc | $I_{CES}$ | — | — | 100 | nAdc |
| Emitter Cutoff Current<br>$V_{EB}$ = 5.0 Vdc; $I_C$ = 0 | $I_{EBO}$ | — | — | 100 | nAdc |
| DC Current Gain ($V_{CE}$ = 2.0 Vdc)<br>$I_C$ = 100 μAdc<br>$I_C$ = 10 mAdc | $h_{FE}$ | <br>30<br>75 | <br>165<br>140 | <br>—<br>— | — |

FIGURE 1 — DC CURRENT GAIN AND RATIO versus COLLECTOR CURRENT



**MOTOROLA**

# MC3356

## WIDEBAND FSK RECEIVER

. . . includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communications equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: −3 dB Limiting Sensitivity
  30 μVrms @ 100 MHz
- Highly versatile, full-function device, yet few external parts are required

**WIDEBAND**
**FSK**
**RECEIVER**

**SILICON MONOLITHIC**
**INTEGRATED CIRCUIT**

**P SUFFIX**
PLASTIC PACKAGE
CASE 738-02

**FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM**

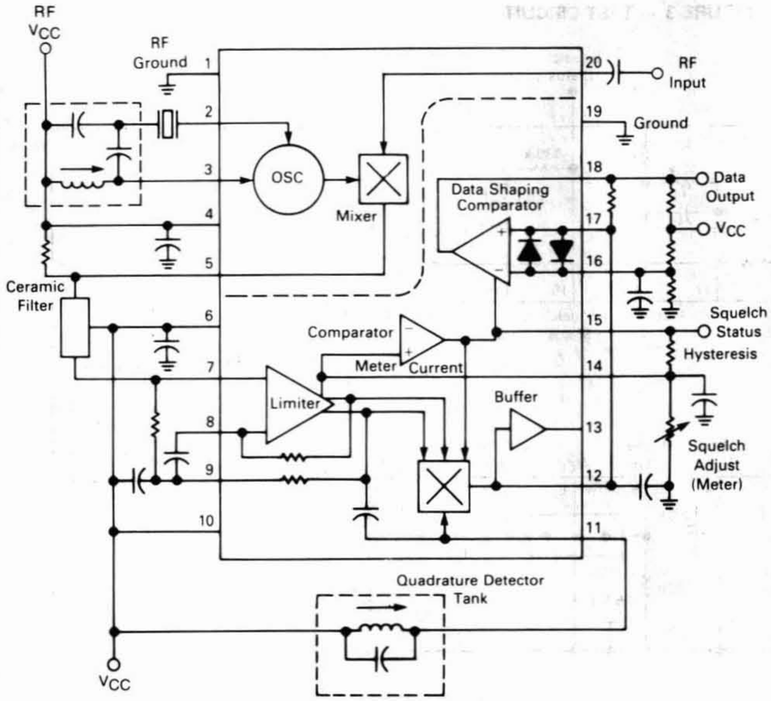
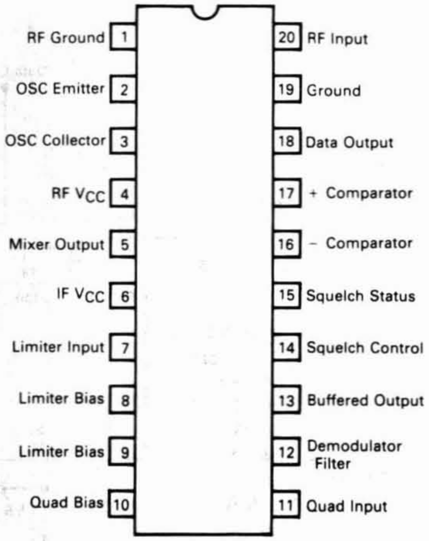

RF
VCC
RF
Ground
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
RF
Input
Ground
OSC
Mixer
Data Shaping
Comparator
Data
Output
VCC
Squelch
Status
Hysteresis
Comparator
Meter
Current
Limiter
Buffer
Ceramic
Filter
Squelch
Adjust
(Meter)
Quadrature Detector
Tank
VCC

**FIGURE 2 — PIN CONNECTIONS**


RF Ground 1
OSC Emitter 2
OSC Collector 3
RF VCC 4
Mixer Output 5
IF VCC 6
Limiter Input 7
Limiter Bias 8
Limiter Bias 9
Quad Bias 10
20 RF Input
19 Ground
18 Data Output
17 + Comparator
16 − Comparator
15 Squelch Status
14 Squelch Control
13 Buffered Output
12 Demodulator Filter
11 Quad Input

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC(max)}$ | 15 | Vdc |
| Operating Power Supply Voltage Range (Pins 6, 10) | $V_{CC}$ | 3.0 to 9.0 | Vdc |
| Operating R.F. Supply Voltage Range (Pin 4) | R.F. $V_{CC}$ | 3.0 to 12.0 | Vdc |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | −40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Power Dissipation, Package Rating | $P_D$ | 1.25 | W |

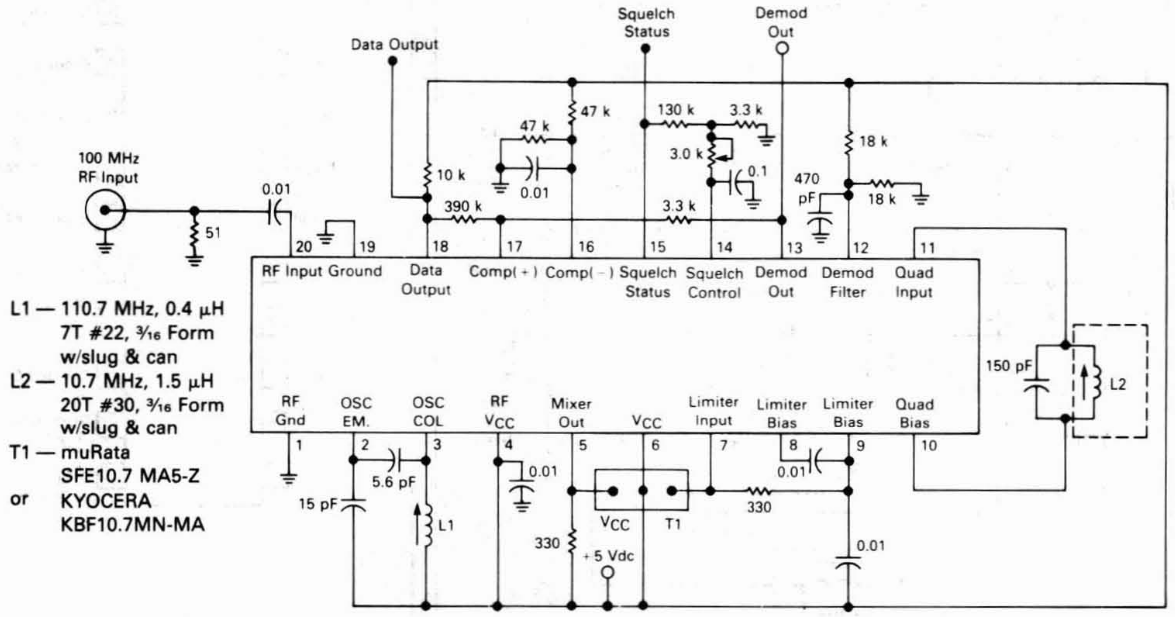
## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5.0 Vdc, $f_o$ = 100 MHz, $f_{osc}$ = 110.7 MHz, Δf = ±75 kHz, $f_{mod}$ = 1.0 kHz, 50 Ω source, $T_A$ = 25°C, test circuit of Figure 3, unless otherwise noted.)

| Characteristics | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Drain Current Total, RF $V_{CC}$ and $V_{CC}$ | — | 20 | 25 | mAdc |
| Input for −3 dB limiting | — | 30 | — | μVrms |
| Input for 50 dB quieting $\left(\frac{S+N}{N}\right)$ | — | 60 | — | μVrms |
| Mixer Voltage Gain, Pin 20 to Pin 5 | 2.5 | — | — | |
| Mixer Input Resistance, 100 MHz | — | 260 | — | Ω |
| Mixer Input Capacitance, 100 MHz | — | 5.0 | — | pF |
| Mixer/Oscillator Frequency Range (Note 1) | — | 0.2 to 150 | — | MHz |
| IF/Quadrature Detector Frequency Range (Note 1) | — | 0.2 to 50 | — | MHz |
| AM Rejection (30% AM, RF $V_{in}$ = 1.0 mVrms) | — | 50 | — | dB |
| Demodulator Output, Pin 13 | — | 0.5 | — | Vrms |
| Meter Drive | — | 7.0 | — | μA/dB |
| Squelch Threshold | — | 0.8 | — | Vdc |

Note 1: Not taken in Test Circuit of Figure 3; new component values required.

FIGURE 3 — TEST CIRCUIT


Squelch Status
Demod Out
Data Output
100 MHz RF Input
51
0.01
47 k
47 k
0.01
10 k
390 k
130 k
3.3 k
3.0 k
0.1
3.3 k
470 pF
18 k
18 k
20
19
18
17
16
15
14
13
12
11
RF Input
Ground
Data Output
Comp(+)
Comp(−)
Squelch Status
Squelch Control
Demod Out
Demod Filter
Quad Input
RF Gnd
OSC EM.
OSC COL
RF VCC
Mixer Out
VCC
Limiter Input
Limiter Bias
Limiter Bias
Quad Bias
1
2
3
4
5
6
7
8
9
10
150 pF
L2
5.6 pF
15 pF
L1
0.01
0.01
330
330
VCC
T1
+5 Vdc
0.01

L1 — 110.7 MHz, 0.4 μH
7T #22, 3/16 Form
w/slug & can
L2 — 10.7 MHz, 1.5 μH
20T #30, 3/16 Form
w/slug & can
T1 — muRata
SFE10.7 MA5-Z
or KYOCERA
KBF10.7MN-MA

FIGURE 4 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

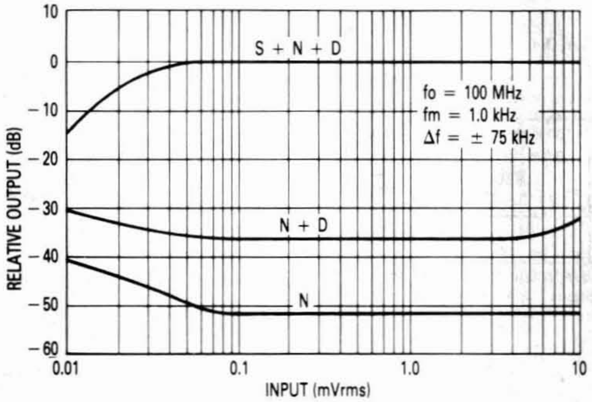
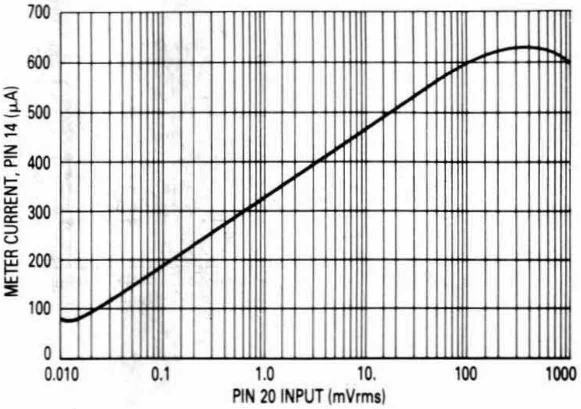


FIGURE 5 — METER CURRENT versus SIGNAL INPUT



## General Description

This device is intended for single and double conversion VHF receiver systems, primarily for FSK data transmission up to 500 K baud (250 kHz). It contains an oscillator, mixer, limiting IF, quadrature detector, signal strength meter drive, and data shaping amplifier.

The oscillator is a common base Colpitts type which can be crystal controlled, as shown in Figure 1, or L-C controlled as shown in the other figures. At higher $V_{CC}$, it has been operated as high as 200 MHz. A mixer/oscillator voltage gain of 2 up to approximately 150 MHz, is readily achievable.

The mixer functions well from an input signal of 10 μVrms, below which the squelch is unpredictable, up to about 10 mVrms, before any evidence of overload. Operation up to 1.0 Vrms input is permitted, but nonlinearity of the meter output is incurred, and some oscillator pulling is suspected. The AM rejection above 10 mVrms is degraded.

The limiting IF is a high frequency type, capable of being operated up to 50 MHz. It is expected to be used at 10.7 MHz in most cases, due to the availability of standard ceramic resonators. The quadrature detector is internally coupled to the IF, and a 5.0 pF quadrature capacitor is internally provided. The −3dB limiting sensitivity of the IF itself is approximately 50 μV (at Pin 7), and the IF can accept signals up to 1.0 Vrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 state limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 10 μV to 100 mVrms. (See Figure 5.)

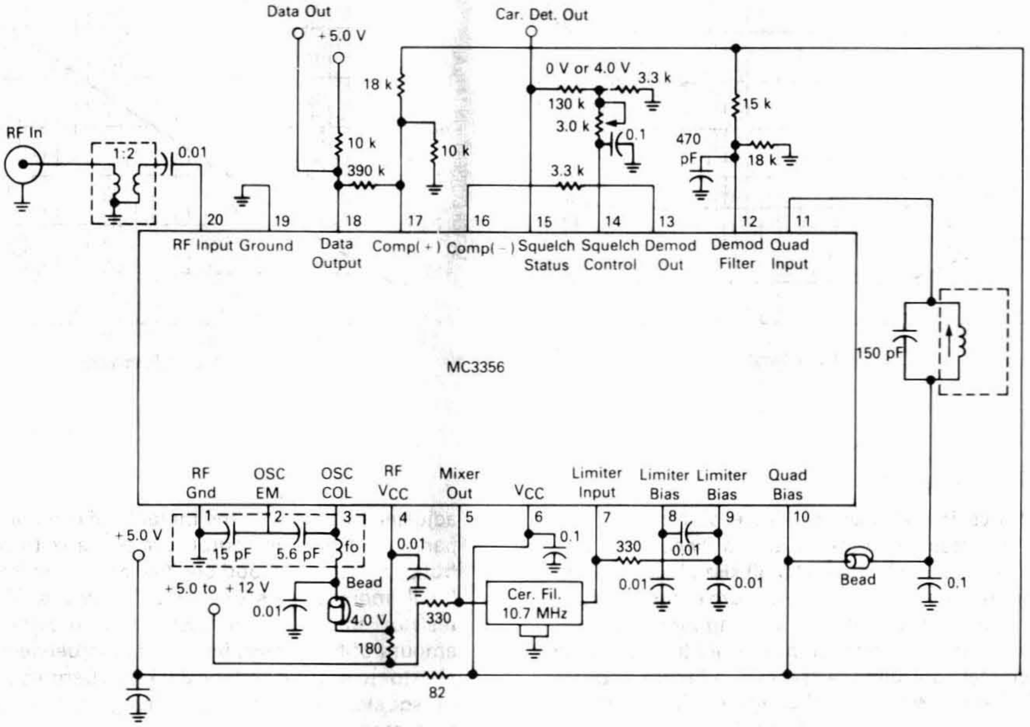
A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator(+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 30 μVrms. The 130 kΩ resistor shown in the test circuit provides a small amount of hysteresis. Its connection between the 3.3 k resistor to ground and the 3.0 k pot, permits adjustment of squelch level without changing the amount of hysteresis.

The squelch is internally connected to both the quadrature detector and the data shaper. The quadrature detector output, when squelched, goes to a dc level approximately equal to the zero signal level, unsquelched. The squelch causes the data shaper to produce a high ($V_{CC}$) output.

The data shaper is a complete "floating" comparator, with back to back diodes across its inputs. The output of the quadrature detector can be fed directly to either input of this amplifier to produce an output that is either at $V_{CC}$ or $V_{EE}$, depending upon the received frequency. The impedance of the biasing can be varied to produce an amplifier which "follows" frequency detuning to some degree, to prevent data pulse width changes.

When the data shaper is driven directly from the demodulator output, Pin 13, there may be distortion at Pin 13 due to the diodes, but this is not important in the data application. A useful note in relating high/low input frequency to logic state: low IF frequency corresponds to low demodulator output. If the oscillator is above the incoming RF frequency, then high RF frequency will produce a logic low. (Input to (+)input of Data Shaper as shown in figures 1 and 3.)

FIGURE 6 — APPLICATION WITH FIXED BIAS ON DATA SHAPER


Data Out
+5.0 V
Car. Det. Out
0 V or 4.0 V
3.3 k
130 k
3.0 k
0.1
3.3 k
18 k
10 k
390 k
10 k
15 k
470 pF
18 k
RF In
1:2
0.01
20
19
18
17
16
15
14
13
12
11
RF Input
Ground
Data Output
Comp(+)
Comp(−)
Squelch Status
Squelch Control
Demod Out
Demod Filter
Quad Input
150 pF
MC3356
RF Gnd
OSC EM
OSC COL
RF VCC
Mixer Out
VCC
Limiter Input
Limiter Bias
Limiter Bias
Quad Bias
1
2
3
4
5
6
7
8
9
10
+5.0 V
15 pF
5.6 pF
fo
0.01
0.1
330
0.01
+5.0 to +12 V
0.01
Bead
4.0 V
330
Cer. Fil. 10.7 MHz
0.01
0.01
Bead
0.1
180
82

## Application Notes

The MC3356 is a high frequency/high gain receiver that requires following certain layout techniques in designing a stable circuit configuration. The objective is to minimize or eliminate, if possible, any unwanted feedback.

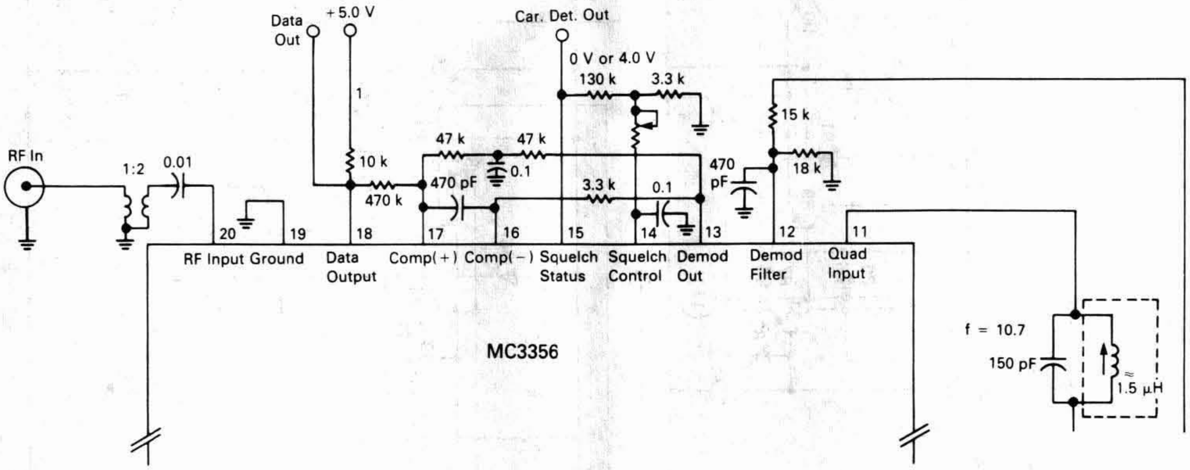
Shielding, which includes the placement of input and output components, is important in minimizing electrostatic or electromagnetic coupling. The MC3356 has its pin connections such that the circuit designer can place the critical input and output circuits on opposite ends of the chip. Shielding is normally required for inductors in tuned circuits.

The MC3356 has separate $V_{CC}$'s and grounds for the RF and IF sections which allows good external circuit isolation by minimizing common ground paths.

Note that the circuits of figures 1 and 3 have RF, oscillator, and IF circuits predominantly referenced to the plus supply rails. Figure 6, on the other hand, shows a suitable means of ground referencing. The two methods produce identical results when carefully executed. It is important to treat Pin 19 as a ground node for either approach. The RF input should be "grounded" to Pin 1 and then the input and the mixer/oscillator grounds (or RF $V_{CC}$ bypasses) should be connected by a low inductance path to Pin 19. IF and detector sections should also have their bypasses returned by a *separate* path to Pin 19. $V_{CC}$ and RF $V_{CC}$ can be decoupled to minimize feedback, although the configuration of Figure 3 shows a successful implementation on a common 5.0 supply. Once again, the message is: define a supply node and a ground node and return each section to those nodes by separate, low impedance paths.

The test circuit of Figure 3 has a 3 db limiting level of 30 μV which can be lowered 6 db by a 1:2 untuned transformer at the input as shown in figures 6 and 7. For applications that require additional sensitivity, an RF amplifier can be added, but with no greater than 20 db gain. This will give a 2.0 to 2.5 μV sensitivity and any additional gain will reduce receiver dynamic range without improving its sensitivity. Although the test circuit operates at +5.0 V, the mixer/oscillator optimum performance is at +8.0 V to 12 V. A minimum of +8.0 V is recommended in high frequency applications (above 150 MHz), or in PLL applications where the oscillator drives a prescaler.

FIGURE 7 — APPLICATION WITH SELF-ADJUSTING BIAS ON DATA SHAPER

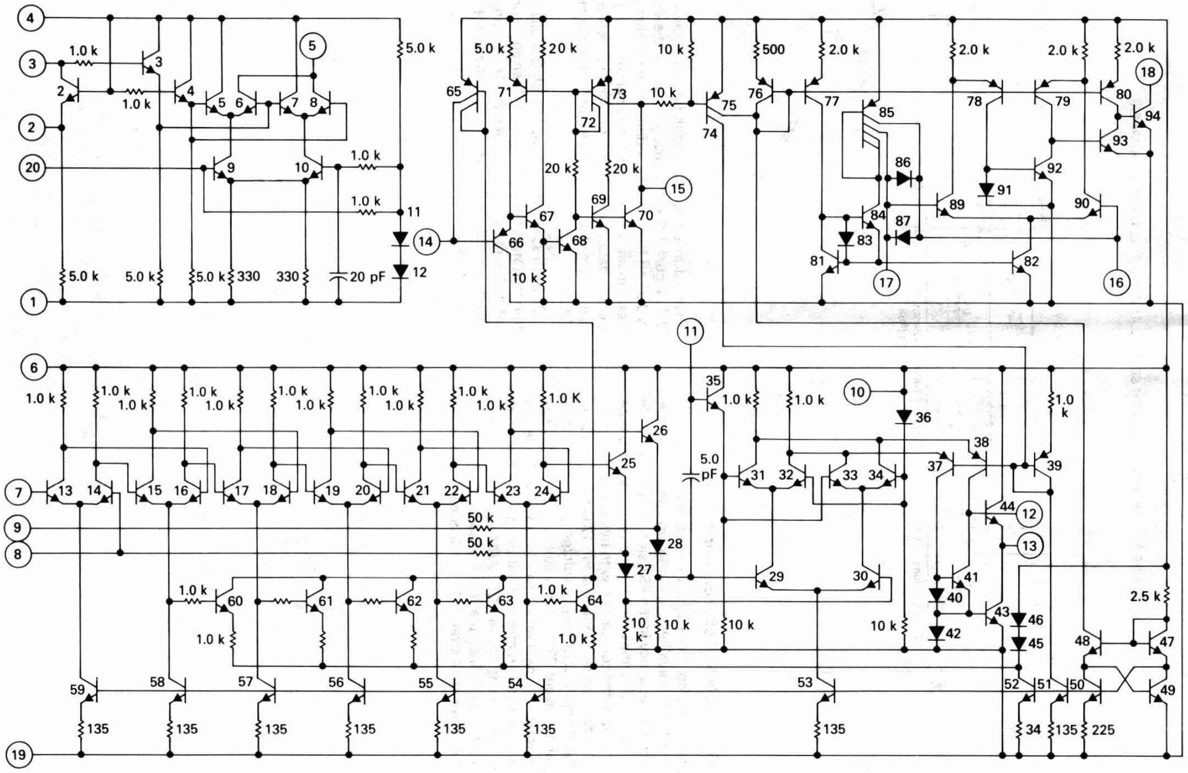

Data Out
+5.0 V
Car. Det. Out
0 V or 4.0 V
130 k
3.3 k
1
15 k
47 k
47 k
RF In
1:2
0.01
10 k
0.1
470
18 k
470 pF
pF
470 k
3.3 k
0.1
20
19
18
17
16
15
14
13
12
11
RF Input Ground
Data Output
Comp(+)
Comp(−)
Squelch Status
Squelch Control
Demod Out
Demod Filter
Quad Input
f = 10.7
150 pF
≈ 1.5 μH
MC3356

## APPLICATION NOTES, continued

Depending on the external circuit, inverted or non-inverted data is available at Pin 18. Inverted data makes the higher frequency in the FSK signal a 'one' when the local oscillator is above the incoming RF. Figure 6 schematic shows the comparator with hysteresis. In this circuit the dc reference voltage at Pin 17 is about the same as the demodulated output voltage (Pin 13) when no signal is present. This type circuit is preferred for systems where the data rates can drop to zero. Some systems have a low frequency limit on the data rate, such as systems using the MC3850 ACIA that has a start or stop bit. This defines the low frequency limit that can appear in the data stream. Figure 6 circuit can then be changed to a circuit configuration as shown in Figure 7. In Figure 7 the reference voltage for the comparator is derived from the demodulator output through a low pass circuit where $\tau$ is much lower than the lowest frequency data rate. This and similar circuits will compensate for small tuning changes (or drift) in the quadrature detector.

Squelch status (Pin 15) goes high (squelch off) when the input signal becomes greater than some preset level set by the resistance between Pin 14 and ground. Hysteresis is added to the circuit externally by the resistance from Pin 14 to Pin 15.

FIGURE 8 — INTERNAL SCHEMATIC


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
1.0 k
5.0 k
330
20 pF
20 k
10 k
500
2.0 k
50 k
5.0 pF
135
34
225
2.5 k
1.0 K
10 k

**MOTOROLA**

# MC3357

## Advance Information

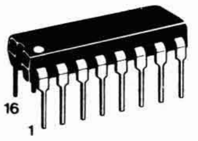
## LOW POWER NARROW BAND FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typ) @ $V_{CC}$ = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage — (-3.0 dB) = 5.0 $\mu$V (Typ)
- Low Number of External Parts Required

## LOW POWER FM IF

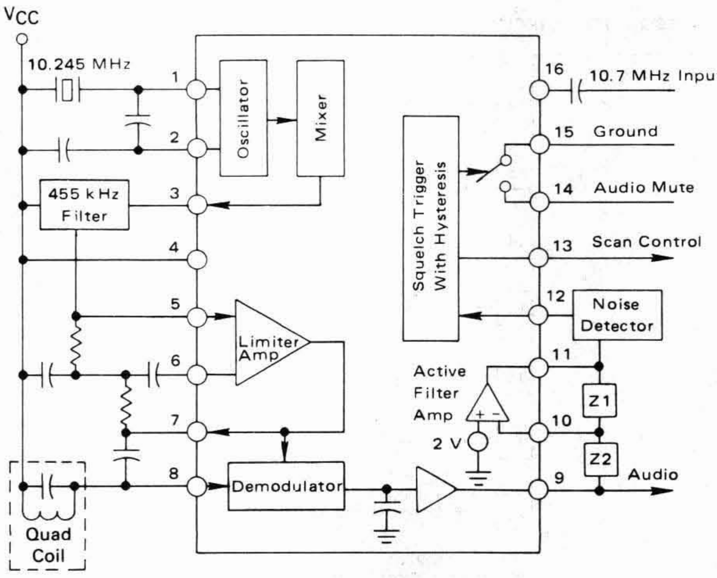
**SILICON MONOLITHIC INTEGRATED CIRCUIT**



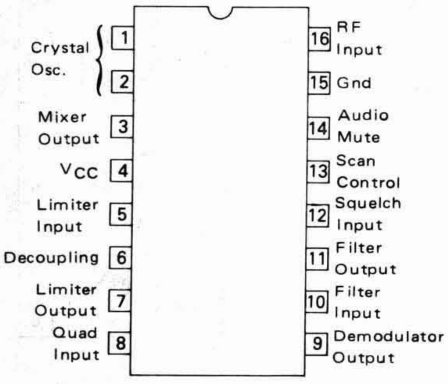
**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

**D SUFFIX**
PLASTIC PACKAGE
CASE 751B-01
SO-16

**FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM**


VCC
10.245 MHz
1
2
3
4
5
6
7
8
455 kHz Filter
Oscillator
Mixer
Limiter Amp
Demodulator
Quad Coil
Squelch Trigger With Hysteresis
Noise Detector
Active Filter Amp
2 V
Z1
Z2
16
10.7 MHz Input
15
Ground
14
Audio Mute
13
Scan Control
12
11
10
9
Audio

**PIN CONNECTIONS**


Crystal Osc.
1
2
Mixer Output
3
VCC
4
Limiter Input
5
Decoupling
6
Limiter Output
7
Quad Input
8
RF Input
16
Gnd
15
Audio Mute
14
Scan Control
13
Squelch Input
12
Filter Output
11
Filter Input
10
Demodulator Output
9

This document contains information on a new product. Specifications and information herein are subject to change without notice.

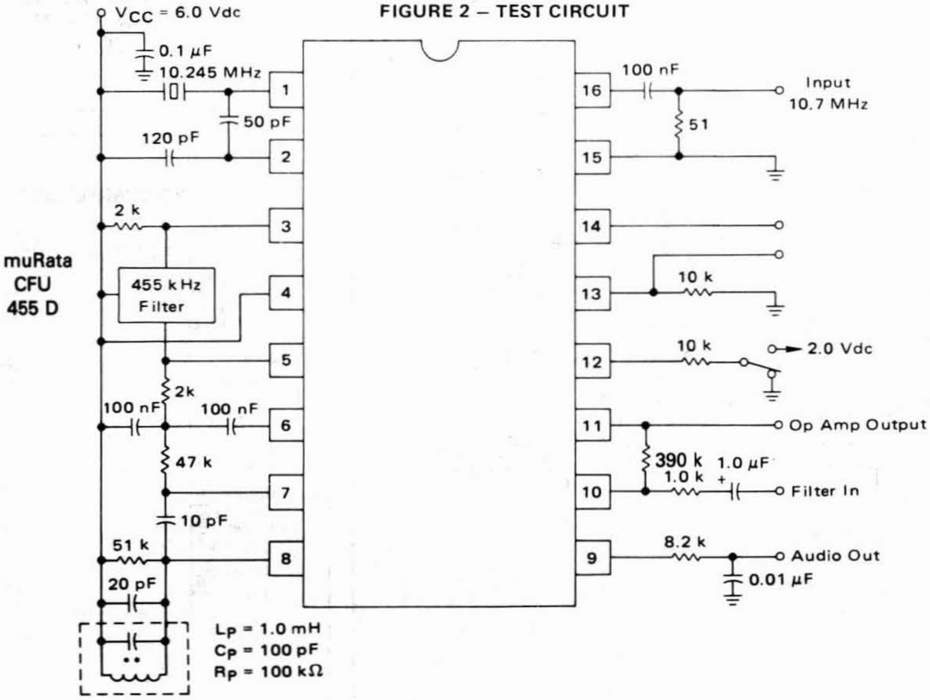
**MAXIMUM RATINGS** ($T_A$ = 25°C, unless otherwise noted)

| Rating | Pin | Symbol | Value | Unit |
|---|---|---|---|---|
| Power Supply Voltage | 4 | $V_{CC}$(max) | 12 | Vdc |
| Operating Supply Voltage Range | 4 | $V_{CC}$ | 4 to 8 | Vdc |
| Detector Input Voltage | 8 | – | 1.0 | Vp-p |
| Input Voltage ($V_{CC} \geqslant 6.0$ Volts) | 16 | $V_{16}$ | 1.0 | $V_{RMS}$ |
| Mute Function | 14 | $V_{14}$ | -0.5 to 5.0 | $V_{pk}$ |
| Junction Temperature | – | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | – | $T_A$ | −30 to +70 | °C |
| Storage Temperature Range | – | $T_{stg}$ | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 6.0 Vdc, fo = 10.7 MHz, Δf = ± 3.0 kHz, $f_{mod}$ = 1.0 kHz, $T_A$ = 25°C unless otherwise noted.)

| Characteristic | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Drain Current | 4 | | | | mA |
| Squelch Off | | – | 2.0 | – | |
| Squelch On | | – | 3.0 | 5.0 | |
| Input Limiting Voltage (−3 dB Limiting) | 16 | – | 5.0 | 10 | μV |
| Detector Output Voltage | 9 | – | 3.0 | – | Vdc |
| Detector Output Impedance | – | – | 400 | – | Ω |
| Recovered Audio Output Voltage ($V_{in}$ = 10 mV) | 9 | 200 | 350 | – | mVrms |
| Filter Gain (10 kHz) ($V_{in}$ = 5 mV) | – | 40 | 46 | – | dB |
| Filter Output Voltage | 11 | 1.8 | 2.0 | 2.5 | Vdc |
| Trigger Hysteresis | – | – | 100 | – | mV |
| Mute Function Low | 14 | – | 15 | 50 | Ω |
| Mute Function High | 14 | 1.0 | 10 | – | MΩ |
| Scan Function Low (Mute Off) ($V_{12}$ = 2 Vdc) | 13 | – | 0 | 0.5 | Vdc |
| Scan Function High (Mute On) ($V_{12}$ = Gnd) | 13 | 5.0 | – | – | Vdc |
| Mixer Conversion Gain | 3 | – | 20 | – | dB |
| Mixer Input Resistance | 16 | – | 3.3 | – | kΩ |
| Mixer Input Capacitance | 16 | – | 2.2 | – | pF |

FIGURE 2 – TEST CIRCUIT


VCC = 6.0 Vdc
0.1 μF
10.245 MHz
50 pF
120 pF
2 k
muRata
CFU
455 D
455 kHz
Filter
2k
100 nF
100 nF
47 k
10 pF
51 k
20 pF
Lp = 1.0 mH
Cp = 100 pF
Rp = 100 kΩ
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
100 nF
Input
10.7 MHz
51
10 k
10 k
2.0 Vdc
Op Amp Output
390 k
1.0 μF
1.0 k
+
Filter In
8.2 k
Audio Out
0.01 μF

## CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer-oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

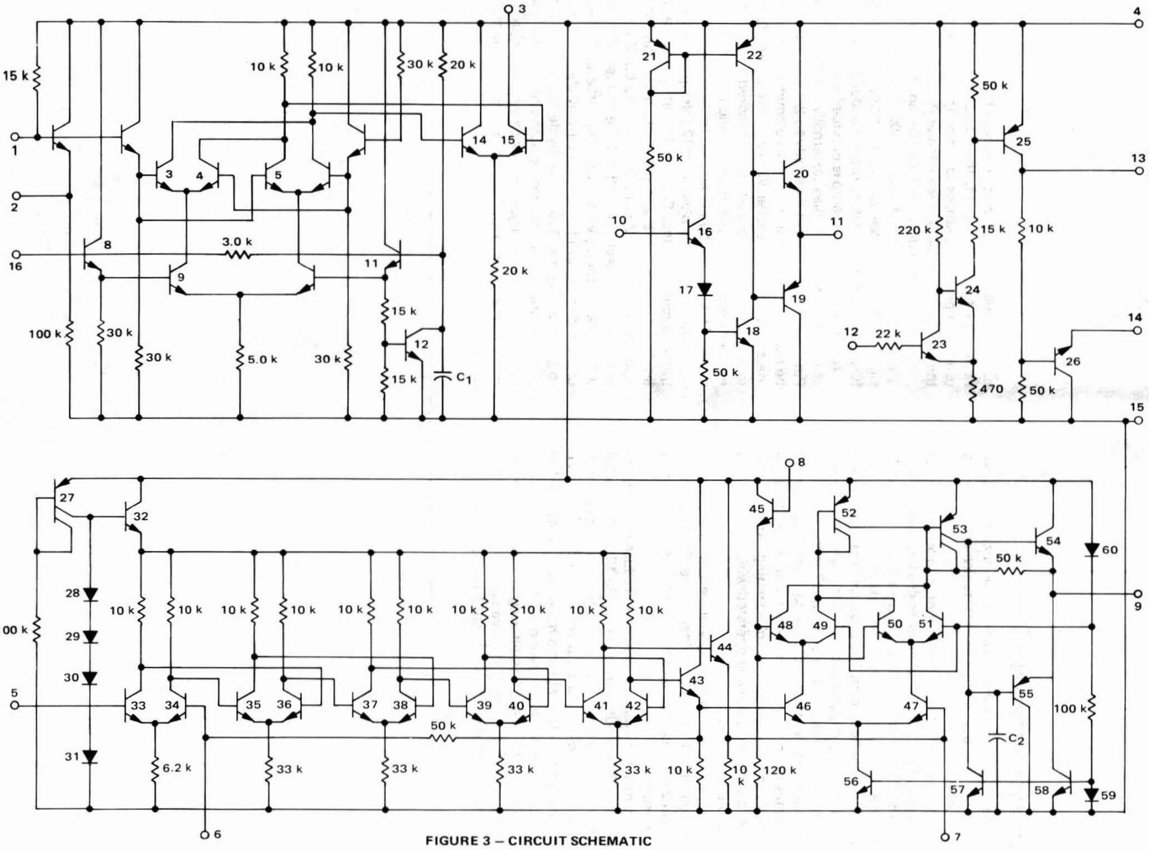
The mixer is doubly-balanced to reduce spurious responses. The input impedance at Pin 16 is set by a 3.0 kΩ internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at Pin 3 must be dc connected to B+, below which it can swing 0.5 V.

After suitable bandpass filtering (ceramic or LC) the signal goes to the input of a five-stage limiter at Pin 5. The output of the limiter at Pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at Pin 7 is also used to supply dc feedback to Pin 5. The other side of the first limiter stage is decoupled at Pin 6.

The recovered audio is partially filtered, then buffered giving an impedance of around 400 Ω at Pin 9. The signal still requires de-emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at Pin 11 providing dc bias (externally) to the input at Pin 10 which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that Pin 13 is low at an impedance level of around 60 kΩ, and the audio mute (Pin 14) is open circuit. If Pin 12 is pulled down to 0.7 V by the noise or tone detector, Pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 μA and Pin 14 is internally short-circuited to ground. There is 100 mV of hysteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to a high-impedance ground-reference point in the audio path between Pin 9 and the audio amplifier.


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
15 k
10 k
10 k
30 k
20 k
3.0 k
100 k
30 k
30 k
5.0 k
30 k
15 k
15 k
C1
20 k
50 k
50 k
50 k
220 k
15 k
10 k
22 k
470
50 k
100 k
10 k
6.2 k
33 k
33 k
33 k
33 k
50 k
120 k
50 k
100 k
C2
3
4
5
8
9
11
12
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
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49
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51
52
53
54
55
56
57
58
59
60

FIGURE 3 — CIRCUIT SCHEMATIC

**MOTOROLA**

# MC3359

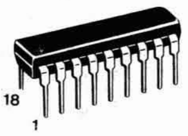
## HIGH-GAIN LOW-POWER FM IF

**SILICON MONOLITHIC INTEGRATED CIRCUIT**

## LOW-POWER NARROW-BAND FM IF

. . . includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrow-band FM signals using a 455 kHz ceramic filter for use in FM dual conversion communications equipment. The MC3359 is similar to the MC3357 except that the MC3359 has an additional limiting IF stage, an AFC output, and an opposite polarity Broadcast Detector. The MC3359 also requires fewer external parts.

- Low Drain Current (3.6 mA (Typ) @ $V_{CC}$ = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage — (−3.0 dB) = 2.0 μV (Typ)
- Low Number of External Parts Required



**P SUFFIX**
PLASTIC PACKAGE
CASE 707-02

**FN SUFFIX**
PLASTIC PACKAGE
CASE 775-01
PLCC-20*

***Surface Mount pin-out is different than standard package pin-out for this device. Please refer to Chapter 7 for details.**

**FIGURE 1 — TYPICAL APPLICATION IN A SCANNER RECEIVER**

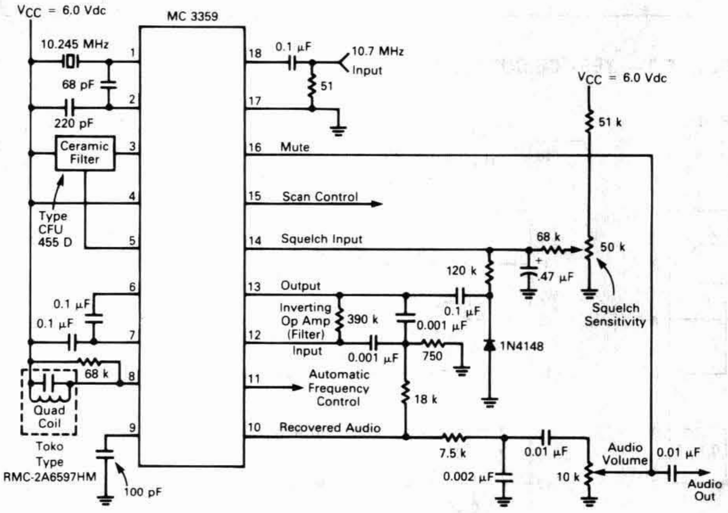
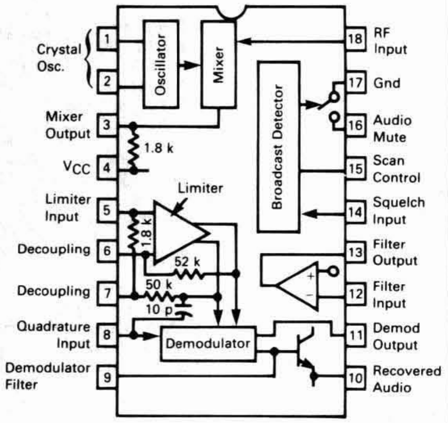

$V_{CC}$ = 6.0 Vdc
MC 3359
10.245 MHz
68 pF
220 pF
Ceramic Filter
Type CFU 455 D
0.1 μF
0.1 μF
68 k
Quad Coil
Toko Type RMC-2A6597HM
100 pF
1
2
3
4
5
6
7
8
9
18
17
16 Mute
15 Scan Control
14 Squelch Input
13 Output
12
11
10 Recovered Audio
0.1 μF
10.7 MHz Input
51
$V_{CC}$ = 6.0 Vdc
51 k
68 k
50 k
120 k
47 μF
Squelch Sensitivity
Inverting Op Amp (Filter) Input
390 k
0.1 μF
0.001 μF
0.001 μF
750
1N4148
Automatic Frequency Control
18 k
7.5 k
0.01 μF
0.002 μF
Audio Volume
10 k
0.01 μF
Audio Out

**FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM**


Crystal Osc.
1
2
Mixer Output
3
$V_{CC}$
4
Limiter Input
5
Decoupling
6
Decoupling
7
Quadrature Input
8
Demodulator Filter
9
Oscillator
Mixer
1.8 k
Limiter
1.8 k
52 k
50 k
10 p
Demodulator
Broadcast Detector
18 RF Input
17 Gnd
16 Audio Mute
15 Scan Control
14 Squelch Input
13 Filter Output
12 Filter Input
11 Demod Output
10 Recovered Audio

**MAXIMUM RATINGS** ($T_A$ = 25°C, unless otherwise noted)

| Rating | Pin | Symbol | Value | Unit |
|---|---|---|---|---|
| Power Supply Voltage | 4 | $V_{CC}(max)$ | 12 | Vdc |
| Operating Supply Voltage Range | 4 | $V_{CC}$ | 4 to 9 | Vdc |
| Input Voltage ($V_{CC} \geq 6.0$ Volts) | 18 | $V_{18}$ | 1.0 | $V_{rms}$ |
| Mute Function | 16 | $V_{16}$ | −0.7 to 12 | $V_{pk}$ |
| Junction Temperature | — | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | — | $T_A$ | −30 to +70 | °C |
| Storage Temperature Range | — | $T_{stg}$ | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 6.0 Vdc, fo = 10.7 MHz, Δf = ±3.0 kHz, $f_{mod}$ = 1.0 kHz, 50 Ω source, $T_A$ = 25° C test circuit of Figure 3, unless otherwise noted)

| Characteristics | Min | Typ | Max | Units |
|---|---|---|---|---|
| Drain Current (pins 4 and 8) Squelch Off<br>Squelch On | —<br>— | 3.6<br>5.4 | 6.0<br>7.0 | mA |
| Input for 20 dB Quieting | — | 8.0 | — | μVrms |
| Input for −3dB Limiting | — | 2.0 | — | μVrms |
| Mixer Voltage Gain (Pin 18 to Pin 3, Open) | — | 46 | — | |
| Mixer Third Order Intercept, 50 Ω Input | — | −1.0 | — | dBm |
| Mixer Input Resistance | — | 3.6 | — | kΩ |
| Mixer Input Capacitance | — | 2.2 | — | pF |
| Recovered Audio, Pin 10 (Input Signal 1.0 mVrms) | 450 | 700 | — | mVrms |
| Detector Center Frequency Slope, Pin 10 | — | 0.3 | — | V/kHz |
| AFC Center Slope, Pin 11, Unloaded | — | 12 | — | V/kHz |
| Filter gain (test circuit of Fig. 3) | 40 | 51 | — | dB |
| Squelch Threshold, Through 10K to Pin 14 | — | 0.62 | — | Vdc |
| Scan Control Current, Pin 15 Pin 14 – High<br>– Low | —<br>2.0 | 0.01<br>2.4 | 1.0<br>— | μA<br>mA |
| Mute Switch Impedance Pin 16 to Ground Pin 14 – High<br>– Low | — | 5.0<br>1.5 | 10<br>— | Ω<br>MΩ |

**FIGURE 3 — TEST CIRCUIT**

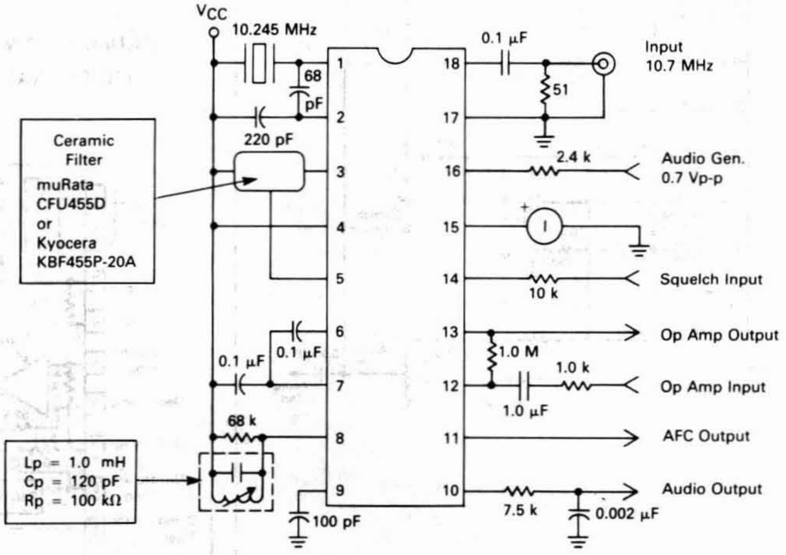

VCC
10.245 MHz
68 pF
220 pF
Ceramic Filter muRata CFU455D or Kyocera KBF455P-20A
0.1 μF
0.1 μF
68 k
Lp = 1.0 mH
Cp = 120 pF
Rp = 100 kΩ
100 pF
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
0.1 μF
51
Input 10.7 MHz
2.4 k
Audio Gen. 0.7 Vp-p
+
I
10 k
Squelch Input
1.0 M
Op Amp Output
1.0 k
1.0 μF
Op Amp Input
AFC Output
7.5 k
0.002 μF
Audio Output

**FIGURE 4 — MIXER VOLTAGE GAIN**

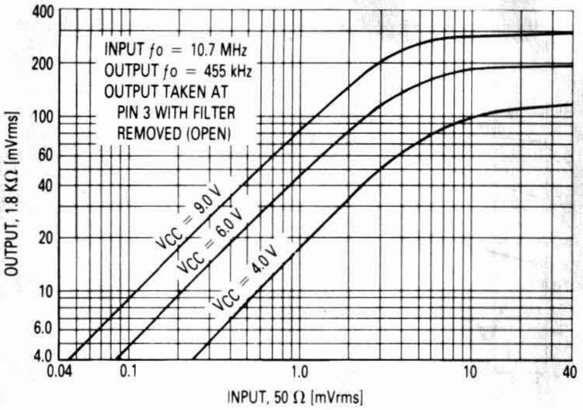


**FIGURE 5 — LIMITING I.F. FREQUENCY RESPONSE**

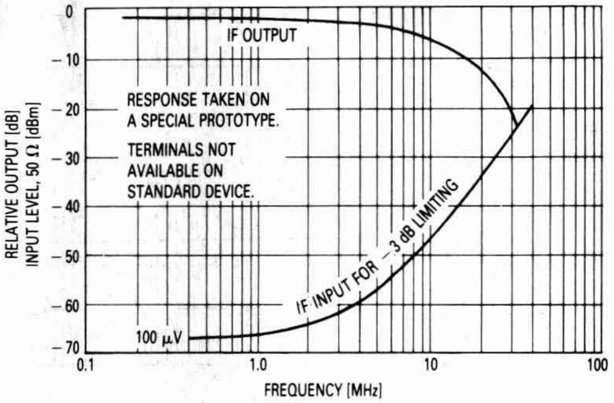


**FIGURE 6 — MIXER THIRD ORDER INTERMODULATION PERFORMANCE**

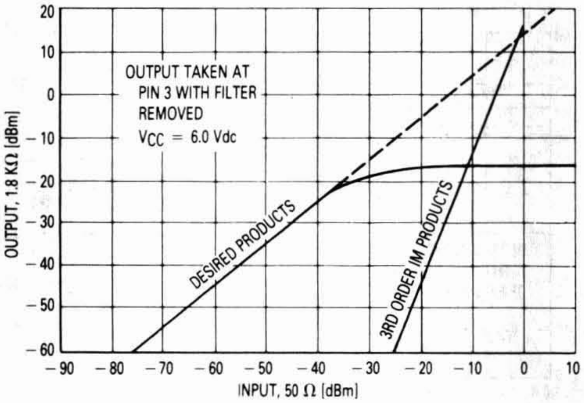


**FIGURE 7 — DETECTOR AND AFC RESPONSES**

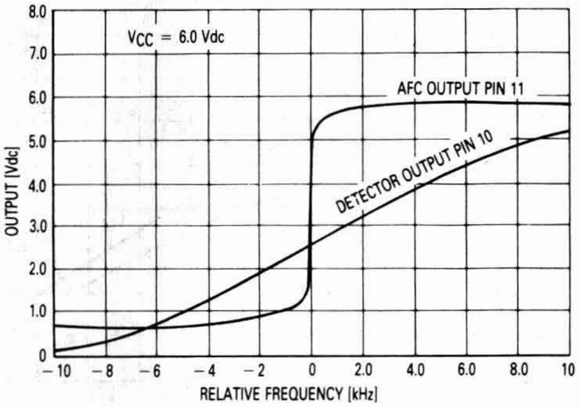


**FIGURE 8 — RELATIVE MIXER GAIN**

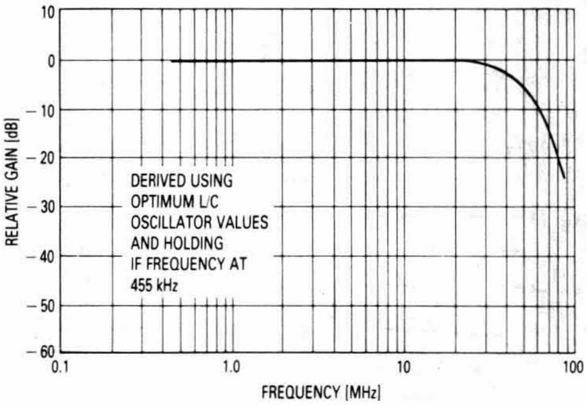
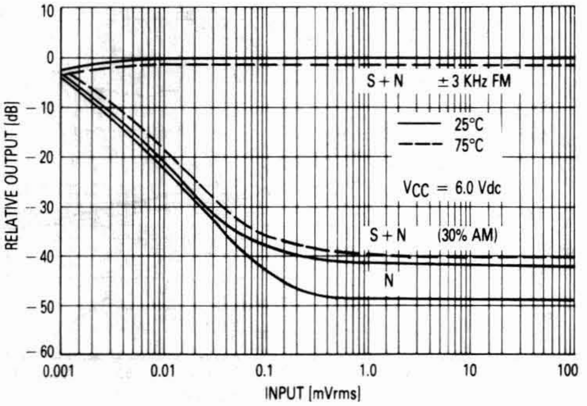
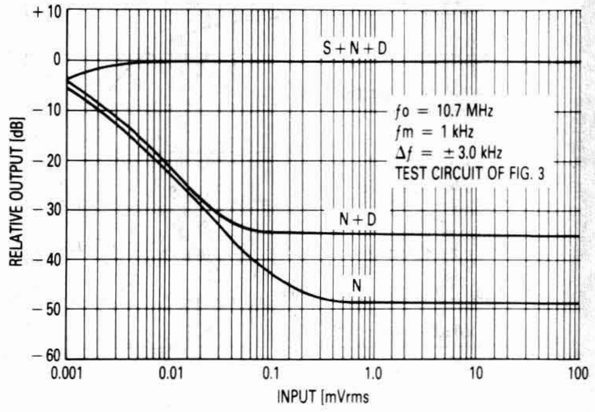


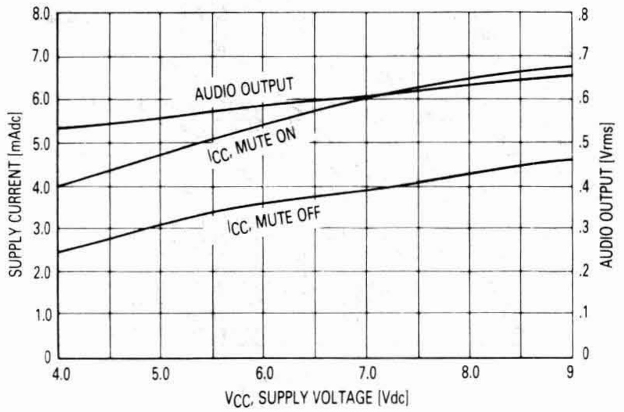
**FIGURE 9 — OVERALL GAIN, NOISE, AND A.M. REJECTION**



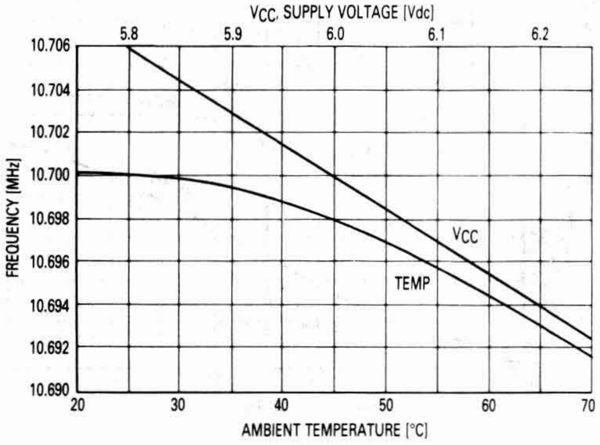
### FIGURE 10 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION



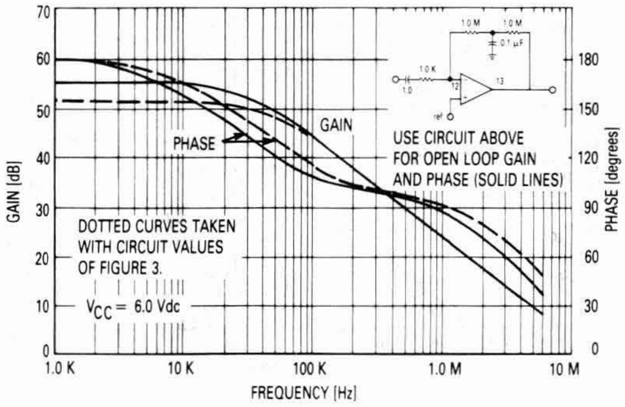
### FIGURE 11 — AUDIO OUTPUT AND TOTAL CURRENT DRAIN versus SUPPLY VOLTAGE



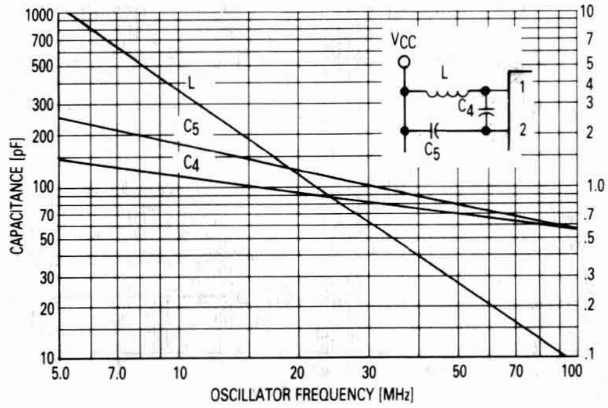
### FIGURE 12 — L/C OSCILLATOR, TEMPERATURE AND POWER SUPPLY SENSITIVITY



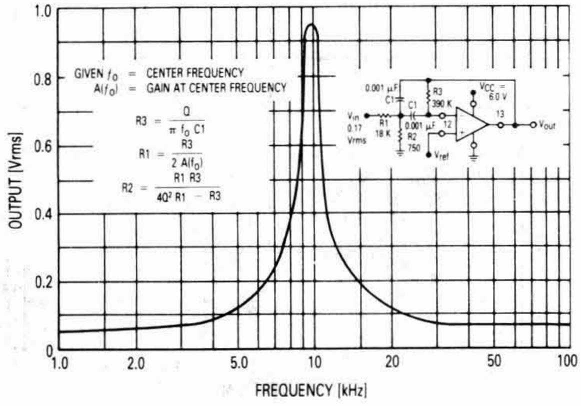
### FIGURE 13 — OP AMP GAIN AND PHASE RESPONSE



### FIGURE 14 — L/C OSCILLATOR RECOMMENDED COMPONENT VALUES



### FIGURE 15 — THE OP AMP AS A BANDPASS FILTER



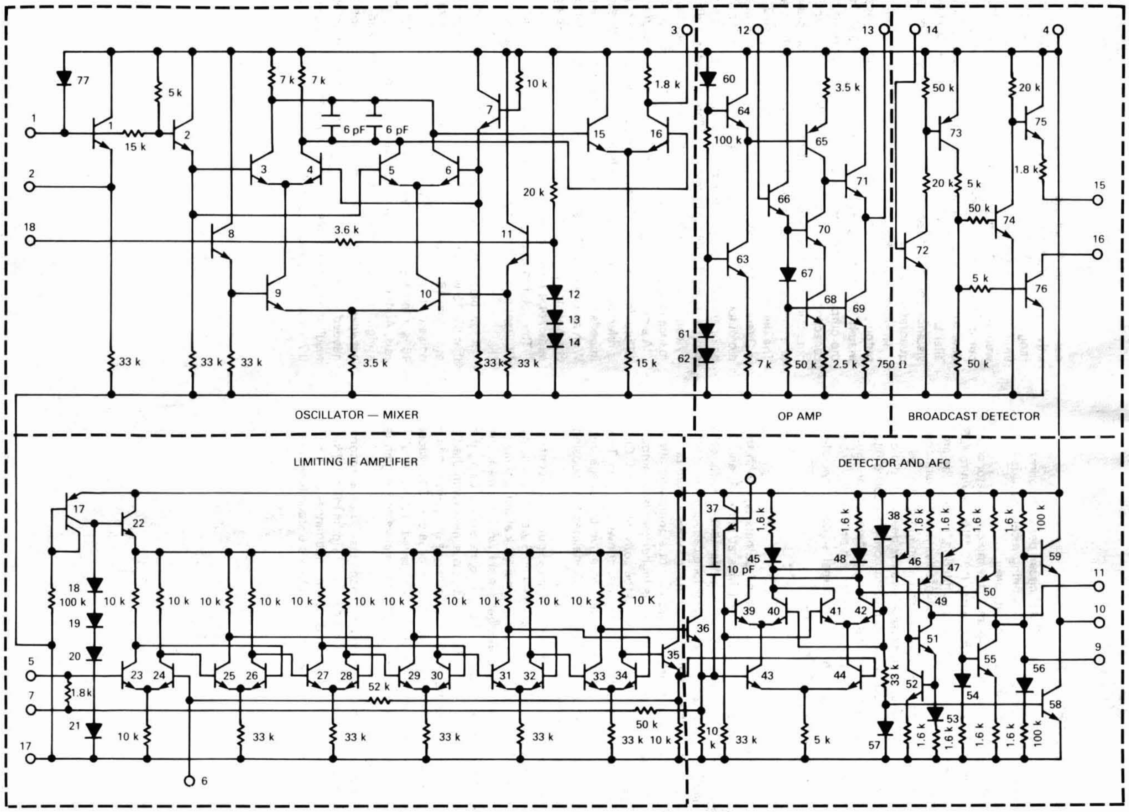

OSCILLATOR — MIXER
OP AMP
BROADCAST DETECTOR
LIMITING IF AMPLIFIER
DETECTOR AND AFC
1
2
3
4
5
6
7
9
10
11
12
13
14
15
16
17
18
5 k
15 k
7 k
6 pF
3.6 k
10 k
20 k
1.8 k
100 k
3.5 k
50 k
33 k
3.5 k
15 k
7 k
2.5 k
750 Ω
10 k
10 K
52 k
1.8 k
10 pF
1.6 k
5 k

FIGURE 16 — CIRCUIT SCHEMATIC

## CIRCUIT DESCRIPTION

The MC3359 is a low-power FM IF circuit designed primarily for use in voice-communication scanning receivers. It is also finding a place in narrow-band data links.

In the typical application (Figure 1), the mixer-oscillator combination converts the input frequency (10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch-trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

## APPLICATION

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at pin 4, 1, and 2, respectively. The crystal is used in fundamental mode, calibrated for parallel resonance at 32 pF load capacitance. In theory this means that the two capacitors in series should be 32 pF, but in fact much larger values do not significantly affect the oscillator frequency, and provide higher oscillator output.

The oscillator can also be used in the conventional L/C Colpitts configuration without loss of mixer conversion gain. This oscillator is, of course, much more sensitive to voltage and temperature as shown in Figure 12. Guidelines for choosing L and C values are given in Figure 14.

The mixer is doubly balanced to reduce spurious responses. The mixer measurements of Figure 4 and 6 were made using an external 50 Ω source and the internal 1.8 k at pin 3. Voltage gain curves at several Vcc voltages are shown in Figure 4. The Third Order Intercept curves of Figure 6 are shown using the conventional dBm scales. Measured power gain (with the 50 Ω input) is approximately 18 dB but the useful gain is much higher because the mixer input impedance is over 3 kΩ. Most applications will use a 330 Ω 10.7 MHz crystal filter ahead of the mixer. For higher frequencies, the relative mixer gain is given in Figure 8.

Following the mixer, a ceramic bandpass filter is recommended. The 455 kHz types come in bandwidths from ±2 kHz to ±15 kHz and have input and output impedances of 1.5 k to 2.0 k. For this reason, the pin 5 input to the 6 stage limiting IF has an internal 1.8 k resistor. The IF has a 3 dB limiting sensitivity of approximately 100 μV at pin 5 and a useful frequency range of about 5 MHz as shown in Figure 5. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector, including the 10 pF quadrature capacitor. Only a parallel L/C is needed externally from pin 8 to Vcc. A shunt resistance can be added to widen the peak separation of the quadrature detector.

The detector output is amplified and buffered to the audio output, pin 10, which has an output impedance of approximately 300 Ω. Pin 9 provides a high impedance (50 k) point in the output amplifier for application of a filter or deemphasis capacitor. Pin 11 is the AFC output, with high gain and high output impedance (1 M). If not needed, it should be grounded, or it can be connected to pin 9 to double the recovered audio. The detector and AFC responses are shown in Figure 7.

Overall performance of the MC3359 from mixer input to audio output is shown in Figure 9 and 10. The MC3359 can also be operated in "single conversion" equipment; i.e., the mixer can be used as a 455 kHz amplifier. The oscillator is disabled by connecting pin 1 to pin 2. In this mode the overall performance is identical to the 10.7 MHz results of Figure 9.

A simple inverting op amp is provided with an output at pin 13 providing dc bias (externally) to the input at pin 12, which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of either noise above the normal audio, or a tone signal.

The open loop response of this op amp is given in Figure 13. Bandpass filter design information is provided in Figure 15.

A low bias to pin 14 sets up the squelch-trigger circuit such that pin 15 is high, a source of at least 2.0 mA, and the audio mute (pin 16) is open-circuit. If pin 14 is raised to 0.7 V by the noise or tone detector, pin 15 becomes open-circuit and pin 16 is internally short-circuited to ground. There is no hysteresis. Audio muting is accomplished by connecting pin 16 to a high-impedance ground-reference point in the audio path between pin 10 and the audio amplifier. No dc voltage is needed, in fact it is not desirable because audio "thump" would result during the muting function. Signal swing greater than 0.7 V below ground on pin 16 should be avoided.

**MOTOROLA**

# MC3361

## Advance Information

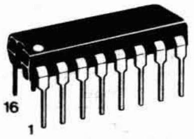
### LOW POWER NARROW BAND FM IF

. . . includes Ocillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3361 is designed for use in FM dual conversion communications equipment.

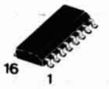
- Operates From 1.8 V to 7.0 V
- Low Drain Current 4.0 mA Typ @ $V_{CC}$ = 4.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage — −3.0 dB = 2.0 μV Typ
- Low Number of External Parts Required

**LOW POWER**
**FM IF**

**SILICON MONOLITHIC**
**INTEGRATED CIRCUIT**

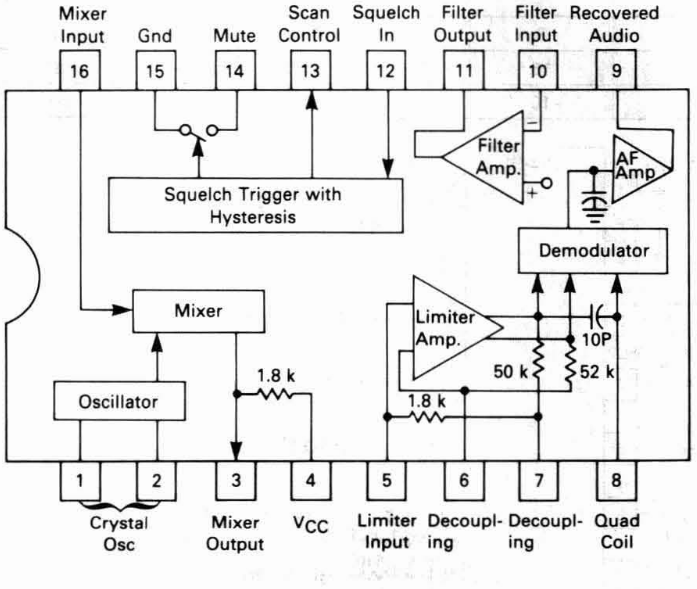


**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05



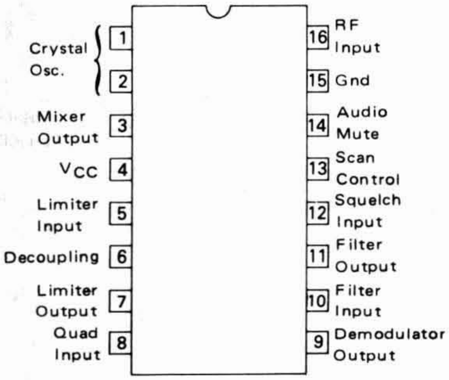
**D SUFFIX**
PLASTIC PACKAGE
CASE 751B-01
SO-16

**FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM**



Mixer Input
Gnd
Mute
Scan Control
Squelch In
Filter Output
Filter Input
Recovered Audio
16
15
14
13
12
11
10
9
Filter Amp.
AF Amp
Squelch Trigger with Hysteresis
Demodulator
Mixer
Limiter Amp.
10P
50 k
52 k
1.8 k
1.8 k
Oscillator
1
2
3
4
5
6
7
8
Crystal Osc
Mixer Output
$V_{CC}$
Limiter Input
Decoupling
Decoupling
Quad Coil

**PIN CONNECTIONS**



Crystal Osc.
1
2
Mixer Output
3
$V_{CC}$
4
Limiter Input
5
Decoupling
6
Limiter Output
7
Quad Input
8
16
RF Input
15
Gnd
14
Audio Mute
13
Scan Control
12
Squelch Input
11
Filter Output
10
Filter Input
9
Demodulator Output

This document contains information on a new product. Specifications and information herein are subject to change without notice.

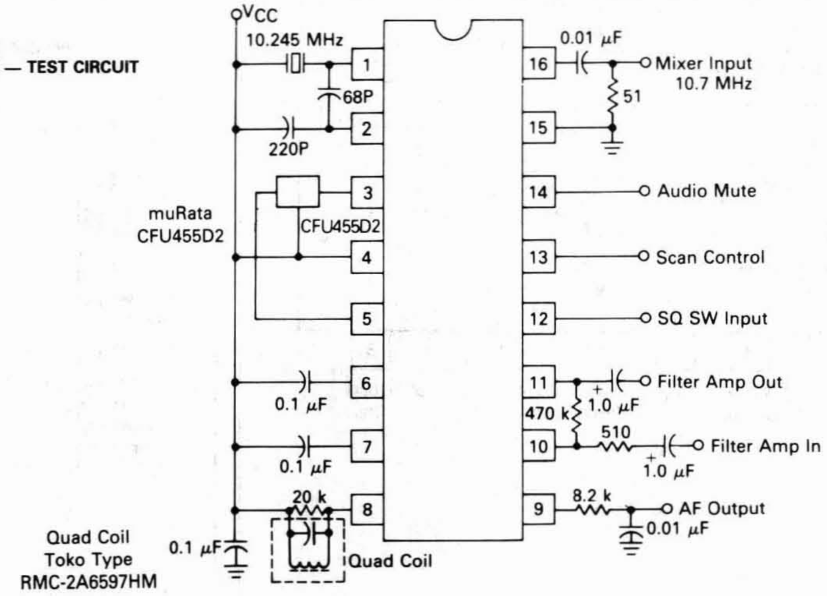
**MAXIMUM RATINGS** ($T_A$ = 25°C, unless otherwise noted)

| Rating | Pin | Symbol | Value | Unit |
|---|---|---|---|---|
| Power Supply Voltage | 4 | $V_{CC}(max)$ | 8.0 | Vdc |
| Operating Supply Voltage Range | 4 | $V_{CC}$ | 1.8 to 7.0 | Vdc |
| Detector Input Voltage | 8 | — | 1.0 | Vp-p |
| Input Voltage ($V_{CC} \geq 4.0$ Volts) | 16 | $V_{16}$ | 1.0 | $V_{RMS}$ |
| Mute Function | 14 | $V_{14}$ | −0.5 to 5.0 | $V_{pk}$ |
| Junction Temperature | — | $T_J$ | 150 | °C |
| Operating Ambient Temperature Range | — | $T_A$ | −30 to +70 | °C |
| Storage Temperature Range | — | $T_{stg}$ | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 4.0 Vdc, fo = 10.7 MHz, Δf = ±3.0 kHz, $f_{mod}$ = 1.0 kHz, $T_A$ = 25°C unless otherwise noted.)

| Characteristic | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Drain Current<br>Squelch Off<br>Squelch On | 4 | <br>—<br>— | <br>4.0<br>6.0 | <br>—<br>— | mA |
| Input Limiting Voltage<br>(−3.0 dB Limiting) | 16 | — | 2.0 | — | μV |
| Detector Output Voltage | 9 | — | 2.0 | — | Vdc |
| Detector Output Impedance | — | — | 400 | — | Ω |
| Recovered Audio Output Voltage<br>($V_{in}$ = 10 mV) | 9 | 100 | 150 | — | mVrms |
| Filter Gain (10 kHz)<br>($V_{in}$ = 5.0 mV) | — | 40 | 48 | — | dB |
| Filter Output Voltage | 11 | — | 1.5 | — | Vdc |
| Trigger Hysteresis | — | — | 50 | | mV |
| Mute Function Low | 14 | — | 10 | — | Ω |
| Mute Function High | 14 | — | 10 | — | MΩ |
| Scan Function Low (Mute Off)<br>($V_{12}$ = 2.0 Vdc) | 13 | — | — | 0.5 | Vdc |
| Scan Function High (Mute On)<br>($V_{12}$ = Gnd) | 13 | 3.0 | — | — | Vdc |
| Mixer Conversion Gain | 3 | — | 24 | — | dB |
| Mixer Input Resistance | 16 | — | 3.3 | — | kΩ |
| Mixer Input Capacitance | 16 | — | 2.2 | — | pF |

**FIGURE 2 — TEST CIRCUIT**



VCC
10.245 MHz
68P
220P
muRata
CFU455D2
CFU455D2
0.1 μF
0.1 μF
20 k
Quad Coil
Toko Type
RMC-2A6597HM
0.1 μF
Quad Coil
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
0.01 μF
Mixer Input
10.7 MHz
51
Audio Mute
Scan Control
SQ SW Input
Filter Amp Out
470 k
1.0 μF
510
Filter Amp In
1.0 μF
8.2 k
AF Output
0.01 μF

**MOTOROLA**

# MC3393P

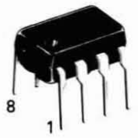
## TWO MODULUS PRESCALER

The MC3393P can divide by 15 and 16, and can be used with Motorola CMOS frequency synthesizers MC145146, 52, 56 for commercial AM-FM radio, land mobile and marine two-way radios, avionic radios, and scanner receivers.

- 140 MHz (typ) Toggle Frequency
- ÷15/16
- TTL and CMOS Compatible Output
- Active Pullup and Pulldown
- +5.0 V Supply
- Buffered Clock Input
- 100–400 mV (typ) Input Sensitivity
- 200 Milliwatts (typ)

**TWO MODULUS PRESCALER**

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

**FIGURE 1 — LOGIC DIAGRAM**

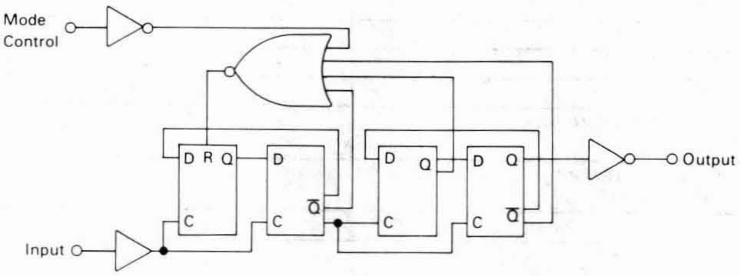
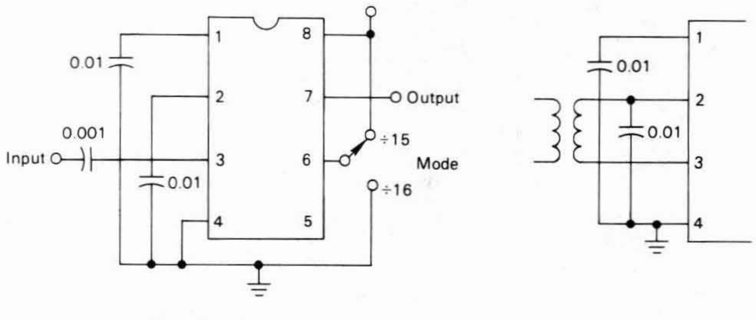

Mode Control
Input
D R Q
C
D
C
Q̄
D Q
C
D Q
C Q̄
Output

**FIGURE 2 — TEST CIRCUITS**


0.01
0.001
Input
0.01
1
2
3
4
8
7
6
5
Output
÷15
Mode
÷16
0.01
0.01
1
2
3
4

Capacitor Coupled Input

Link Coupled Input

Pin Outs
1. Bias Decouple
2. Bias Decouple
3. Input
4. Ground
5. NC
6. Input
7. Output
8. $V_{CC}$

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 6.0 | Vdc |
| Input Mode Control Voltage | $V_{ICR}$ | 10 | Vdc |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Temperature Range | $T_A$ | -40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

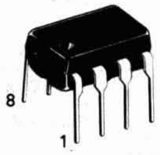
## PRELIMINARY ELECTRICAL CHARACTERISTICS (Unless otherwise noted $V_{CC}$ = +5.0 Vdc, $T_A$ = 25°C, $f_{in}$ = 100 MHz)

| Characteristics | Min | Typ | Max | Units |
|---|---|---|---|---|
| Power Supply Voltage | 4.5 | — | 5.5 | Vdc |
| Current Drain | — | 40 | — | mA |
| Input Voltage | 100 | — | 400 | mV(rms) |
| Input Impedance: Real Part<br>Capacitance | —<br>— | 900<br>6.0 | —<br>— | Ohms<br>pF |
| Mode Control Voltage for 15 Count | 2.7 | — | 10 | Vdc |
| Mode Control Voltage for 16 Count | 0 | — | 0.8 | Vdc |
| Output High at 30 μA Source | 2.7 | 4.3 | — | Vdc |
| Output Low at 1.6 mA Sink | — | 0.3 | 0.8 | Vdc |
| Propagation Delay Time | — | 25 | — | ns |
| Set up Time (16 to 15 Count) Measured before Rising Edge of Clock on Count 15 | — | 20 | — | ns |
| Release Time (15 to 16 Count) Measured before Falling Edge of Clock Preceding Count 15 | — | 15 | — | ns |
| Thermal Resistance, $R_{\theta JC}$ | — | 100 | — | °C/W |

# MC3396P

## DIVIDE BY 20 PRESCALER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 626-04

## DIVIDE BY 20 PRESCALER

The MC3396P is a fixed ÷20 prescaler for use in frequency synthesizers and similar applications.

- 200 MHz (typ) Toggle Frequency
- Single 5.0 Volt Supply
- Buffered Clock Input
- 100 mV — 400 mV RMS Input Sensitivity
- Open-Collector Saturating Output is Capable of Driving TTL and CMOS.

FIGURE 1 — LOGIC DIAGRAM

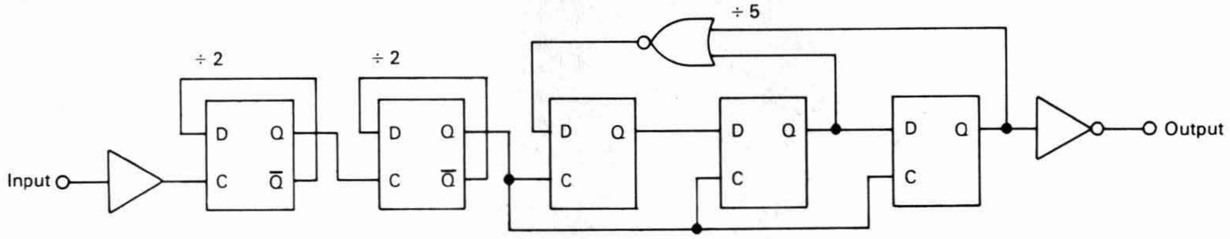
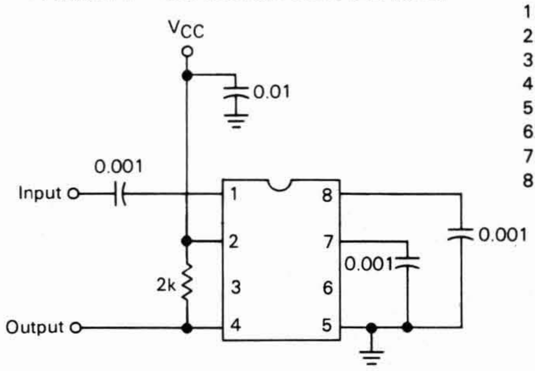

÷ 5
÷ 2
÷ 2
D
Q
C
Q̄
D
Q
C
Q̄
D
Q
C
D
Q
C
D
Q
C
Input
Output

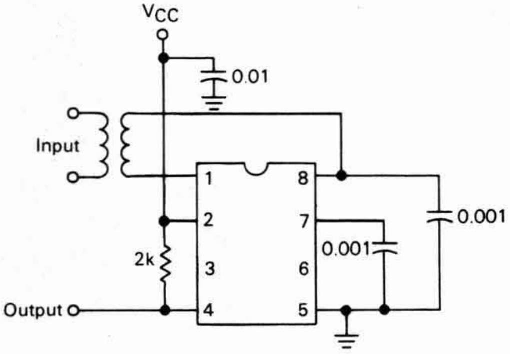
FIGURE 2 — CAPACITOR-COUPLED INPUT


VCC
0.01
0.001
Input
1
2
3
4
8
7
6
5
0.001
0.001
2k
Output

**PIN CONNECTIONS**

1. Input
2. $V_{CC}$
3. NC
4. Output
5. Ground
6. NC
7. Bias Decouple
8. Bias Decouple

FIGURE 3 — LINK-COUPLED INPUT


VCC
0.01
Input
1
2
3
4
8
7
6
5
0.001
0.001
2k
Output

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 8.0 | Vdc |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Temperature Range | $T_A$ | −40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** (Unless otherwise noted $V_{CC}$ = 5 Vdc, $T_A$ = 25°C, $f_{in}$ = 125 MHz measured in the circuit of Figure 2)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Operating Power Supply Voltage Range | 4.5 | — | 5.5 | Vdc |
| Current Drain | — | 30 | — | mA |
| Operating Input Voltage Range | 100 | — | 400 | mV(rms) |
| Input Impedance: | | | | |
| Real Part | — | 600 | — | Ohms |
| Capacitance | — | 6.0 | — | pF |
| Output Voltage | 3.0 | 4.5 | — | $V_{p-p}$ |
| Thermal Resistance — $\theta_{JA}$ | — | 100 | — | °C/W |

# MC13001XP
# MC13002XP

## Advance Information

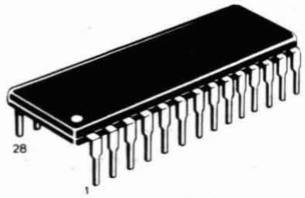
### MONOMAX BLACK-AND-WHITE TV SUBSYSTEM

The MONOMAX is a single-chip IC that will perform the electronic functions of a monochrome TV receiver, with the exception of the tuner, sound channel, and power output stages. The MC13001XP and MC13002XP will function as drop-in replacements for MC13001P and MC13002P, but some external IF components can be removed for maximum benefit. IF AGC range has been increased, video output impedance lowered, and horizontal driver output current capability increased.

- Full Performance Monochrome Receiver with Noise and Video Processing — Black Level Clamp, DC Contrast, Beam Limiter
- Video IF Detection on Chip — No Coils, No Pins, except Inputs
- Noise Filtering on Chip — Minimum Pins and Externals
- Oscillator Components on Chip — No Precision Capacitors Required
- MC13001XP for 525 Line NTSC and MC13002XP for 625 Line CCIR
- Low Dissipation in All Circuit Sections
- High-Performance Vertical Countdown
- 2-Loop Horizontal System with Low Power Start-Up Mode
- Noise Protected Sync and Gated AGC System
- Designed to work with TDA1190P or TDA3190P Sound IF and Audio Output Devices
- Reverse RF AGC Types are Available: MC13008XP, MC13009XP

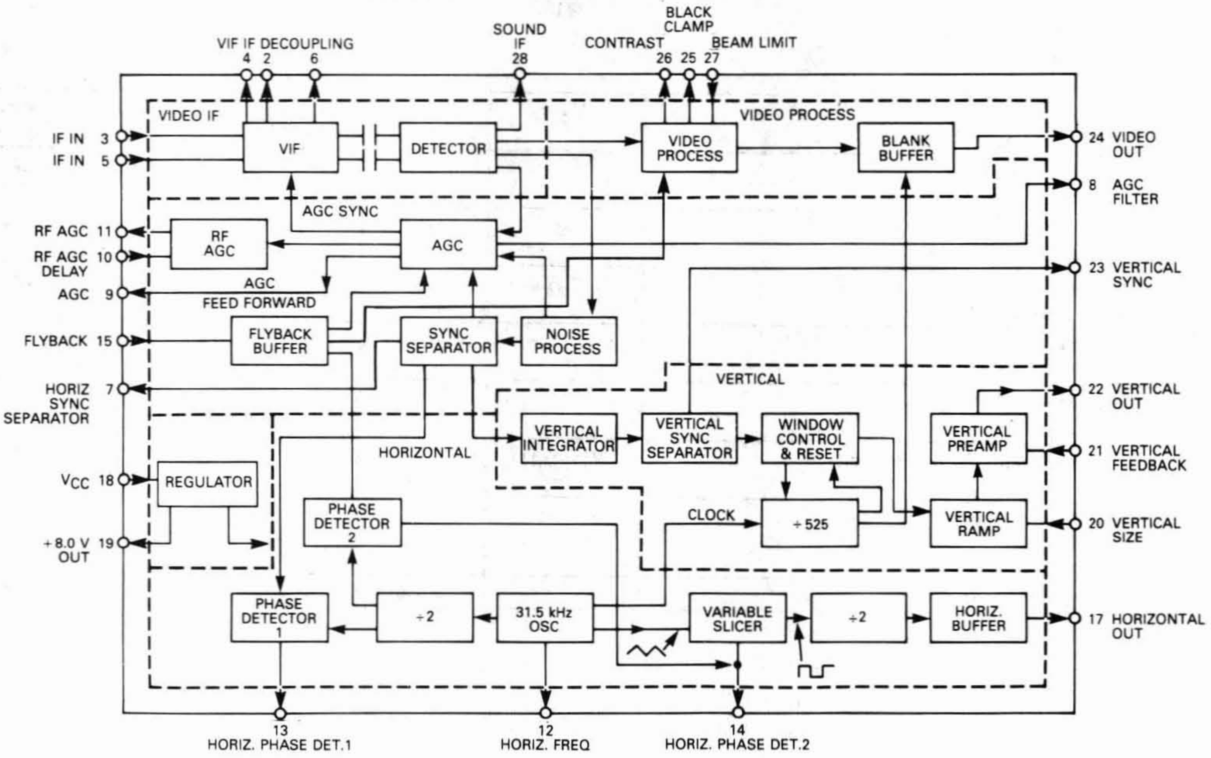
**MONOMAX**
**BLACK-AND-WHITE TV**
**SUBSYSTEM**

**SILICON MONOLITHIC**
**INTEGRATED CIRCUITS**



**P SUFFIX**
PLASTIC PACKAGE
CASE 710-02

**FIGURE 1 — BASIC ELEMENTS OF THE SYSTEM**


VIF IF DECOUPLING
4
2
6
SOUND IF
28
CONTRAST
BLACK CLAMP
BEAM LIMIT
26
25
27
VIDEO IF
VIF
DETECTOR
VIDEO PROCESS
VIDEO PROCESS
BLANK BUFFER
IF IN 3
IF IN 5
24 VIDEO OUT
8 AGC FILTER
AGC SYNC
RF AGC 11
RF AGC 10 DELAY
AGC 9
RF AGC
AGC
AGC FEED FORWARD
23 VERTICAL SYNC
FLYBACK 15
FLYBACK BUFFER
SYNC SEPARATOR
NOISE PROCESS
HORIZ SYNC SEPARATOR 7
VERTICAL
22 VERTICAL OUT
VERTICAL INTEGRATOR
VERTICAL SYNC SEPARATOR
WINDOW CONTROL & RESET
VERTICAL PREAMP
21 VERTICAL FEEDBACK
HORIZONTAL
VCC 18
REGULATOR
+8.0 V 19 OUT
PHASE DETECTOR 2
CLOCK
÷525
VERTICAL RAMP
20 VERTICAL SIZE
PHASE DETECTOR 1
÷2
31.5 kHz OSC
VARIABLE SLICER
÷2
HORIZ. BUFFER
17 HORIZONTAL OUT
13 HORIZ. PHASE DET.1
12 HORIZ. FREQ
14 HORIZ. PHASE DET.2

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage — Pin 18 | $V_{CC}$ | +16 | Vdc |
| Power Dissipation | $P_D$ | 1.0 | Watts |
| Horizontal Driver Current — Pin 17 | $I_{HOR}$ | −20 | mA |
| RF AGC Current — Pin 11 | $I_{RFAGC}$ | 20 | mA |
| Video Detector Current — Pin 24 | $I_{VID}$ | 5.0 | mA |
| Vertical Driver Current — Pin 22 | $I_{VERT}$ | 5.0 | mA |
| Auxiliary Regulator Current — Pin 19 | $I_{REG}$ | 35 | mA |
| Thermal Resistance Junction-to-Case | $R_{\theta JC}$ | 60 | °C/W |
| Maximum Junction Temperature | $T_J$ | 150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Operating Temperature Range | $T_A$ | 0° to +70 | °C |

**RECOMMENDED OPERATING CONDITIONS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Horizontal Output Drive Current | $I_{HOR}$ | ≤10 | mA |
| RF AGC Current | $I_{RFAGC}$ | ≤10 | mA |
| Regulator Current | $I_{REG}$ | ≤20 | mA |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 11.3 V, $T_A$ = 25°C)

| Characteristics | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply Current | Pins 18 & 19 | $I_{CC}$ | 44 | — | 76 | mA |
| Regulator Voltage | Pin 19 | $V_{REG}$ | 7.2 | 8.2 | 8.8 | Vdc |
| **HORIZONTAL SPECIFICATIONS** | | | | | | |
| Oscillator Frequency (Nominal) | Pin 12 | $f_{HOR(NOM)}$ | 13 | — | 19 | kHz |
| Oscillator Sensitivity | | | — | 230 | — | Hz/μA |
| Start-Up Frequency<br>($I_{18}$ = 4.0 mA) | | $f_{HOR}$ | −10 | — | +10 | % |
| Oscillator Temperature Stability<br>(0 ≤ TA ≤ 75°C) | | $f_{HOR}$ | — | 50 | — | Hz |
| Phase Detector 1<br>(Charge/Discharge Current)<br>(Non Standard Frame)<br>(Standard Frame) | | $I_{\phi 1}$ | | ±900<br>±400 | | μA |
| Phase Detector 1<br>(Output Voltage Limits) | | $V_{\phi 1}$ | — | 7.5 (Max)<br>2.5 (Min) | — | Vdc |
| Phase Detector 1<br>(Leakage Current) | | | — | — | 2.0 | μA |
| Phase Detector 2<br>(Charge/Discharge Current) | | $I_{\phi 2}$ | — | +1.0<br>−0.6 | | mA |
| Phase Detector 2<br>(Output Voltage Limits) | | $V_{\phi 2}$ | | 7.7 (Max)<br>1.5 (Min) | | Vdc |
| Phase Detector 2<br>(Leakage Current) | | | — | — | 3.0 | μA |
| Horizontal Delay Range<br>(Sync to Flyback) | | | | 18 (Max)<br>5.0 (Min) | | μs |
| Horizontal Output Saturation Voltage<br>($I_{17}$ = 15 mA) | | $V_{17(SAT)}$ | — | — | 0.3 | Vdc |
| Phase Detector 1 (Gain Constant)<br>(Out-of-Lock)<br>(In-Lock) | | | — | 5.0<br>10 | — | μA/μs |
| Horizontal Pull-In Range | | | ±500 | ±750 | | Hz |

**VERTICAL SPECIFICATIONS**

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Current Pin 22 | $I_{22}$ | −0.6 | — | — | mA |
| Feedback Leakage Current Pin 21 | $I_{21}$ | — | — | 6.0 | μA |
| Ramp Retrace Current Pin 20 | $I_{20}$ | 500 | — | 900 | μA |
| Ramp Leakage Current Pin 20 | | — | — | 0.3 | μA |
| Feedback Maximum Voltage | $V_{21}$ | — | 5.1 | — | Vdc |

**IF SPECIFICATIONS**

| | | | | | |
|---|---|---|---|---|---|
| Regulator Voltage | $V_4$ | — | 7.5 | — | Vdc |
| Input Bias Voltage | $V_{2,6}$ | — | 4.2 | — | Vdc |
| Input Resistance<br>Input Capacitance<br>($V_{AGC}$ Pin 8 = 4.0 V) | $R_{IN}$<br>$C_{IN}$ | | 6.0<br>2.0 | | kΩ<br>pF |
| Sensitivity<br>($V_8$ = 0 V, 400 Hz 30% MOD, $V_{28}$ = 0.8 $V_{pp}$) | | — | 80 | — | $\mu V_{RMS}$ |
| Bandwidth | | — | 75 | — | MHz |

**VIDEO SPECIFICATIONS**

| | | | | | |
|---|---|---|---|---|---|
| Zero Carrier Voltage (See Figure 5) Pin 28 | | — | 7.0 | — | Vdc |
| Output Voltage (See Figure 6) Pin 24<br>White to Back Porch | | — | 1.4 | — | V |
| Differential Gain<br>Differential Phase<br>(IRE Test Method) | | — | 6<br>4 | — | %<br>Degrees |
| Contrast Bias Current Pin 26 | $I_{26}$ | — | 10 | — | μA |
| Contrast Control Range | | — | 14:1 | — | |
| Beam Limiting Voltage Pin 27 | $V_{27}$ | — | 1.0 | — | Vdc |

**AGC & SYNC**

| | | | | | |
|---|---|---|---|---|---|
| R.F. (Tuner) AGC Output Current<br>($V_{11}$ = 5.5 V) | $I_{11}$ | 5.0 | — | — | mA |
| AGC Delay Bias Current | $I_{10}$ | — | −10 | — | μA |
| AGC Feedforward Current | $I_9$ | — | 1.0 | — | mA |
| AGC Threshold<br>(Sync Tip at Pin 28) | $V_{28}$ | 4.7 | — | 5.1 | Vdc |
| Sync Separator Operating Point | $V_7$ | — | 4.2 | — | Vdc |
| Sync Separator Charge Current | $I_7$ | — | 5.0 | — | mA |

FIGURE 2 — MONOMAX AGC CHARACTERISTICS

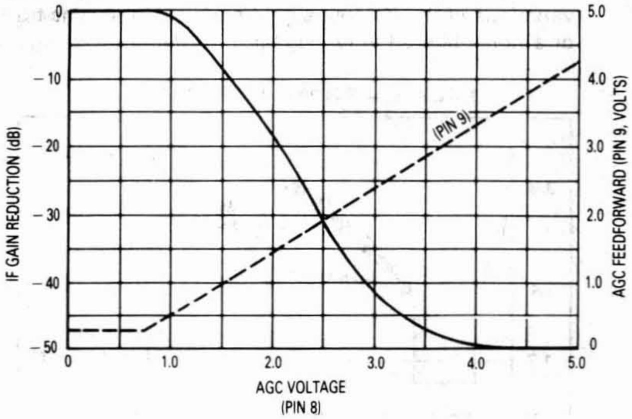


FIGURE 3 — VIDEO OUTPUT RESPONSE

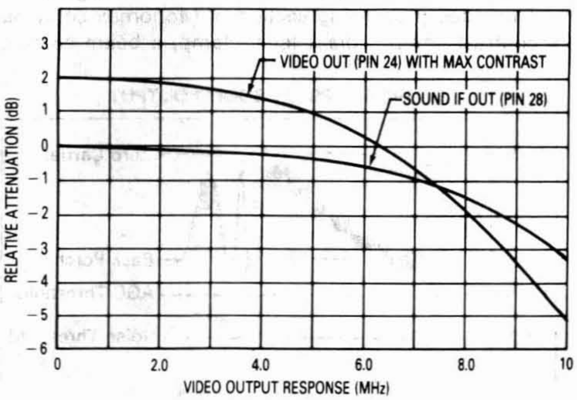
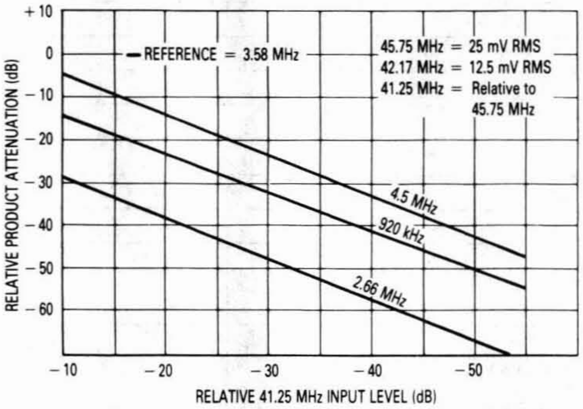


FIGURE 4 — DETECTOR PRODUCTS



## GENERAL DESCRIPTION

The Video IF Amplifier is a four-stage design with 80 μV sensitivity. It uses a 6.2 V supply decoupled at Pin 4. The first two stages are gain controlled, and to ensure optimum noise performance, the first stage control is delayed until the second stage has been gain reduced by 15 dB. To bias the amplifier, balanced dc feedback is used which is decoupled at Pins 2 and 6 and then fed to the input Pins 3 and 5 by internal 3.9 k resistors. The nominal bias voltage at these input pins is approximately 4.2 Vdc. The input, because of the high IF gain, should be driven from a balanced differential source. For the same reason, care must be taken with the IF decoupling.

The IF output is rectified in a full wave envelope detector and detector nonlinearity is compensated by using a similar nonlinear element in a feedback output buffer amplifier. The detected 1.9 $V_{p-p}$ video at Pin 28 contains the sound intercarrier signal, and Pin 28 is normally used as the sound takeoff point. The video frequency response, detector to Pin 28, is shown in Figure 3 and the detector intermodulation performance can be seen by reference to Figure 4. Typical Pin 28 video waveforms and voltage levels are shown in Figure 5.

The video processing section of Monomax contains a contrast control, black level clamp, a beam current limiter and composite blanking. The video signal first passes through the contrast control. This has a range of 14:1 for a 0 V to 5.0 V change of voltage on Pin 26, which corresponds to a change of video amplitude at Pin 24 of 1.4 V to 0.1 V (black to white level). The beam current limiter operates on the contrast control, reducing the video signal when the beam current exceeds the limit set by external components. As the beam current increases, the voltage at Pin 27 moves negatively from its normal value of 1.5 V, and at 1.0 V operates the contrast control, thus initiating beam limiting action. After the contrast control, the video is passed through a buffer amplifier and dc restored by the black level clamp circuit before being fed to Pin 24 where it is blanked. The black level clamp, which is gated "on" during the second half of the flyback, maintains the video black level at 2.4 V ± 0.1 V under all conditions, including changes in contrast, temperature and power supply. The loop integrating capacitor is at Pin 25 and is normally at a voltage of 3.3 V. The frequency response of the video at Pin 24 is shown in Figure 3 and it is blanked to within 0.5 V of ground.

The AGC loop is a gated system, and for all normal variations of the IF input signal maintains the sync tip of a noise filtered video signal at a reference voltage

FIGURE 5 — PIN 28 SOUND OUTPUT

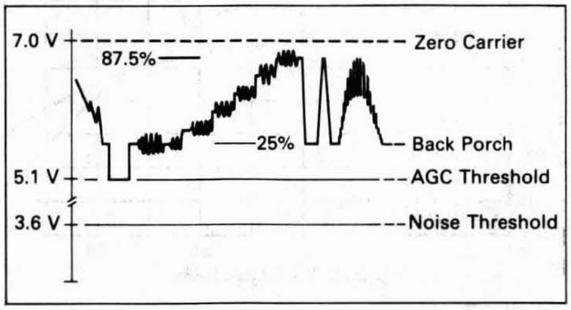
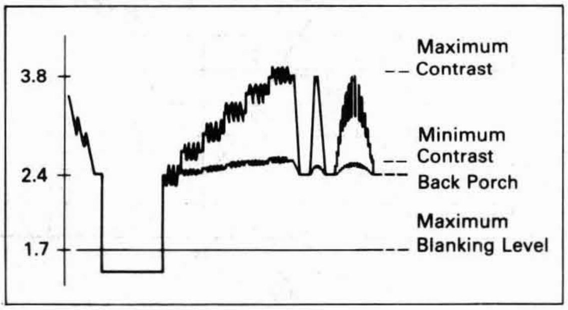


FIGURE 6 — PIN 24 — VIDEO OUTPUT



(5.1 V Pin 28). The strobe for the AGC error amplifier is formed by gating together the flyback pulse with the separated sync pulse. Integration of the error signal is performed by the capacitor at Pin 8, which forms the dominant AGC time constant. Improved noise performance is obtained by the use of a gated AGC system, noise protected by a dc coupled noise canceling circuit. The false AGC lock conditions, which can result from this combination, are prevented by an anti lockout circuit connected to the sync separator at Pin 7. AGC lockout conditions, which occur due to large rapid changes of signal level are detected at Pin 7 and recovery is ensured under these conditions by changing the AGC into a mean level system. The voltage at Pin 10 sets the point at which tuner AGC takeover occurs and positive going tuner control, suitable for an NPN RF transistor, is available at Pin 11. The maximum output is 5.5 V at 5.0 mA. A feed-forward output is provided at Pin 9. This enables the AGC control voltage to be ac coupled into the tuner takeover control at Pin 10. The coupling allows additional IF gain reduction during signal transient conditions, thus compensating for variations of AGC loop gain at the tuner AGC takeover point. In this way the AGC system stability and response are not degraded.

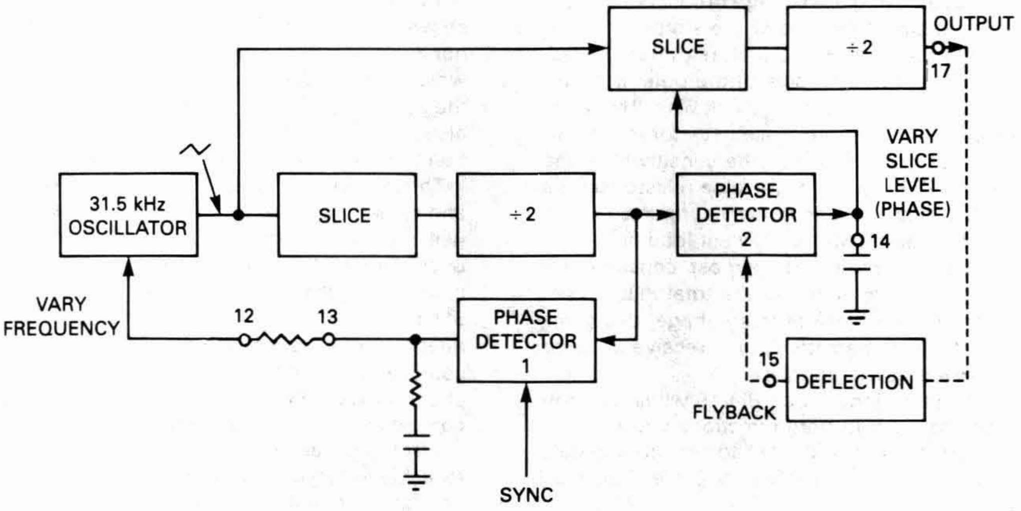
The previously mentioned noise protection is effected by detecting negative-going noise spikes at the video detector output. A dc coupled detector is used which turns on when a noise spike exceeds the video sync tip by 1.4 V. This pulse is then stretched and used to cancel the noise present on the delayed video at the input to the sync separator. Cancellation is performed by blanking the video to ground. Complete cancellation of the noise spike results from the stretching of the blanking pulse and the delay of the noise spike at the input to the sync separator. Protection of both the horizontal PLL and the AGC stems from the fact that both circuits use the noise cancelled sync for gating.

The composite sync is stripped from a delayed and filtered video in a peak detecting type of sync separator. The components connected to Pin 7 determine the slice and tilt levels of the sync separator. For ideal horizontal sync separation and to ensure correct operation of AGC anti-lockup circuit, a relatively short time constant is required at Pin 7. This time constant is less than optimum for good noise free vertical separation, giving rise to a vertical slice level near sync tip. An additional, longer, time-constant is therefore coupled to the first via a diode. With the correct choice of time constants, the diode is non conducting during the horizontal sync period, but conducts during the longer vertical period. This connects the longer time constant to the sync separator for the vertical period and stops the slice level from moving up to the sync tip. The separated composite sync is integrated internally, and the time constant is such that only the longer period vertical pulses produce a significant output pulse. The output is then fed to the vertical sync separator, which further processes the vertical pulse and provides increased noise protection. The selection of the external components connected to the vertical separator at Pin 23 permits a wide range of performance options. A simple resistor divider from the 8.2 V regulated supply gives adequate performance for most conditions. The addition of an RC network will make the slice level adapt to varying sync amplitude and give improved weak signal performance. A resistor to the AGC voltage on Pin 9 enables the sync slice level to be changed as a function of signal level. This further improves the low signal level separation while at the same time giving increased impulse noise protection on strong signals.

## HORIZONTAL OSCILLATOR

The horizontal PLL (see Figure 7) is a 2-loop system using a 31.5 kHz oscillator which after a divider stage is locked to the sync pulse using phase detector 1. The control signal derived from this phase detector on Pin 13 is fed via a high-value resistor to the frequency-control point on Pin 12. The same divided oscillator

FIGURE 7 — HORIZONTAL OSCILLATOR SYSTEMS



frequency is also fed to phase detector 2, where the flyback pulse is compared with it and the resulting error used to change a variable slice level on the oscillator ramp waveform. This therefore changes the timing of the output square wave from the slicer and hence the timing of the buffered horizontal output on Pin 17 (see Figure 8). The error on phase detector 2 is reduced until the phasing of the flyback pulse is correct with respect to the divided oscillator waveform, and hence with respect to the sync pulse.

To improve the pull-in and noise characteristics of the first PLL, the phase detector current is increased when the vertical lock indicator signals an unlocked condition and is decreased when locked. This increases the loop bandwidth and pull-in range when out of lock and decreases the loop bandwidth when in lock, thus improving the noise performance. In addition, the phase detector current during the vertical period is reduced in order to minimize the disturbance to the horizontal caused by the longer period vertical phase detector pulses.

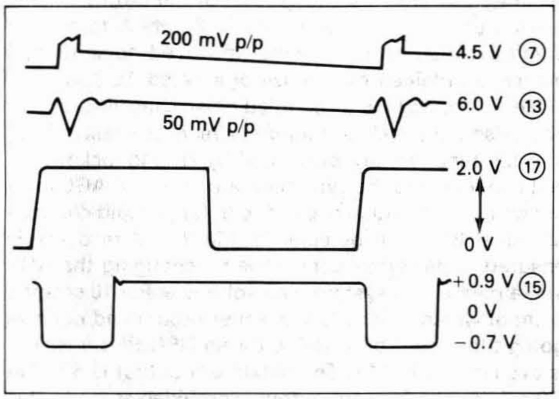
The oscillator itself is a novel design using an on-chip 50 pF silicon nitride capacitor which has a temperature drift of only 70 ppm/°C and negligible long term drift. This, in conjunction with an external resistor, gives a drift of horizontal frequency of less than 1Hz/°C — i.e., less than 100 Hz over the full operating temperature range of the chip. The pull-in range of the PLL is about ± 750 Hz, so normally this would eliminate the need for any customer adjustment of the frequency.

The second significant feature of this design is the use of a virtual ground at the frequency control point which floats at a potential derived from a divider across the power supply and this is the same divider which determines the end-points of the oscillator ramp. The frequency adjustment which is necessary to take up tolerances in the on-chip capacitor is fed in as a current to this virtual ground and when this adjustment current is derived from an external potentiometer across the same supply there is no frequency variation with supply voltage. Moreover, using the voltage from a potentiometer for the adjustment instead of the simple variable resistor normally used in RC oscillators makes the frequency independent of the value of the potentiometer and hence its temperature coefficient. The frequency control current from the first phase detector is fed into this same virtual ground and as the sensitivity of the control is about 230 Hz/μA a high value resistor can be used (680 kΩ) and this can be directly connected to the phase detector filter without significant loading.

This oscillator operates with almost constant frequency to below 4.0 volts and as the total PLL system consumes less than 4.0 mA at this voltage, this gives an ideal start-up characteristic for receivers using deflection-derived power supplies.

The flyback gating input is on Pin 15 which is internally clamped to 0.7 V in both directions and requires a negative input current of 0.6 mA to operate the gate circuit. This input can be a raw flyback pulse simply fed via a suitable resistor.

**FIGURE 8 — HORIZONTAL WAVEFORMS**



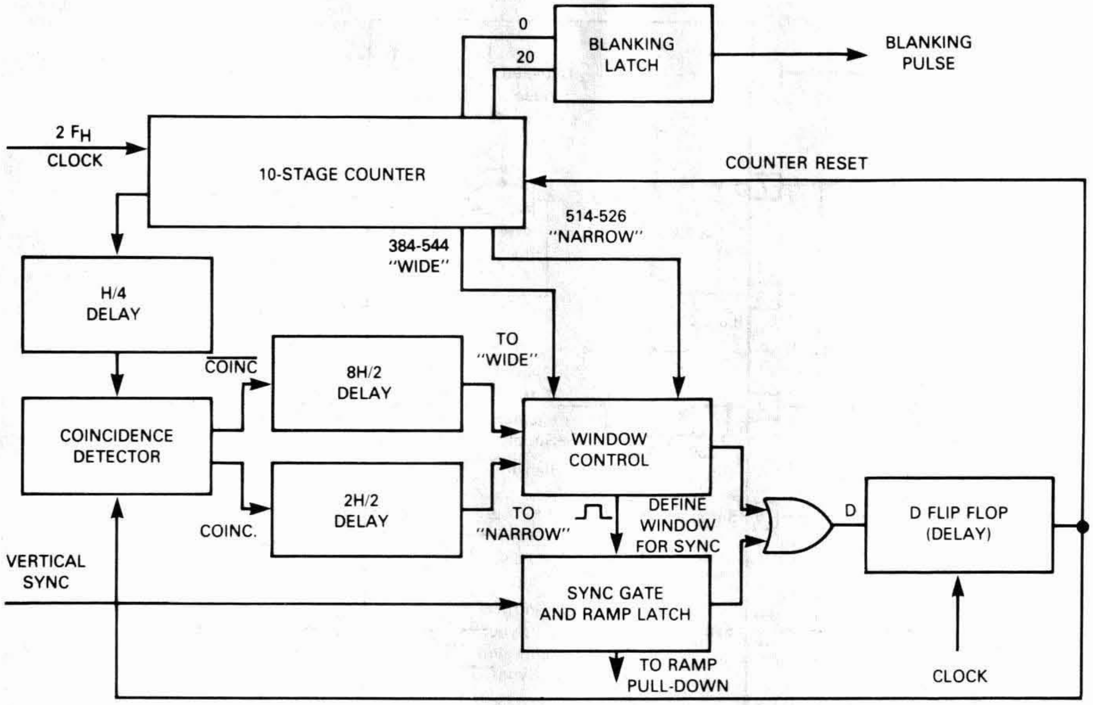
## VERTICAL SYSTEM

An output switching signal is taken from the 31.5 kHz oscillator to clock the vertical counter which is used in place of a conventional vertical oscillator circuit. The counter is reset by the vertical sync pulse but the period during which it is permitted to reset is controlled by the window control. Normally, when the counter is running synchronously, the window is narrow to give some protection against spurious noise pulses in the sync signal. If the counter output is not coincident with sync however, after a short period the window opens to give reset over a much wider count range, leading to a fast picture roll towards lock. At weak signal, i.e., less than 200 μV IF input, the vertical system is forced to narrow mode to give a steadier picture for commonly occurring types of noise. The vertical sync, gated by the counter, then resets a ramp generator on Pin 20 and the 1.5 volt p-p ramp is buffered to Pin 22 by the vertical preamplifier. A differential input to the preamp on Pin 21 compares the signal generated across the resistor in series with the deflection coils with the generated ramp and thus controls shape and amplitude of the coil current.

The basic block diagram of the countdown system is shown in Figure 9. The 31.5 kHz (2 F$^{H}$) clock from the horizontal oscillator drives a 10-stage counter circuit which is normally reset by the vertical sync pulse via the sync gate, OR gate and D flip-flop. This D input is also used to initiate discharge of the ramp capacitor and hence causes picture flyback.

The period during which sync can reset the counter and cause flyback is determined by the window control which defines a count range during which the gate is open. One of two ranges is selected according to the condition of the signal. The normal "narrow" range is 514 to 526 counts for a 525 line system and is selected after the coincidence detector indicates that the reset is coincident, twice in succession, with the 525 count from the counter. When the detector indicates non-coincidence 8 times in succession, then the window control switches to the "wide" mode (384 to 544 counts) to achieve rapid re-synchronization. For the 625 line version the counts are 614 to 626 for narrow mode and

FIGURE 9 — MONOMAX VERTICAL COUNTDOWN

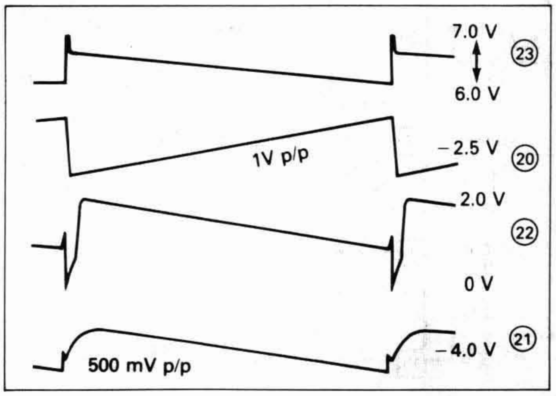

0
20
BLANKING LATCH
BLANKING PULSE
2 $F_H$ CLOCK
10-STAGE COUNTER
COUNTER RESET
514-526 "NARROW"
384-544 "WIDE"
H/4 DELAY
TO "WIDE"
$\overline{\text{COINC}}$
8H/2 DELAY
COINCIDENCE DETECTOR
WINDOW CONTROL
2H/2 DELAY
COINC.
TO "NARROW"
DEFINE WINDOW FOR SYNC
D
D FLIP FLOP (DELAY)
VERTICAL SYNC
SYNC GATE AND RAMP LATCH
TO RAMP PULL-DOWN
CLOCK

484 to 644 for wide mode. Note that the OR gate after the sync gate is used to terminate the count at the end of the respective window if a sync pulse has not appeared.

This method accepts non-standard signals almost in the same way as a conventional triggered RC oscillator and has a similar fast lock-in time. However, the use of a window control on the counter reset ensures that when locked with a normal standard broadcast signal the counter will reject most spurious noise pulses.

The blanking output is provided from a latch which is set by the counter reset pulse and terminated by count 20 from the counter chain.

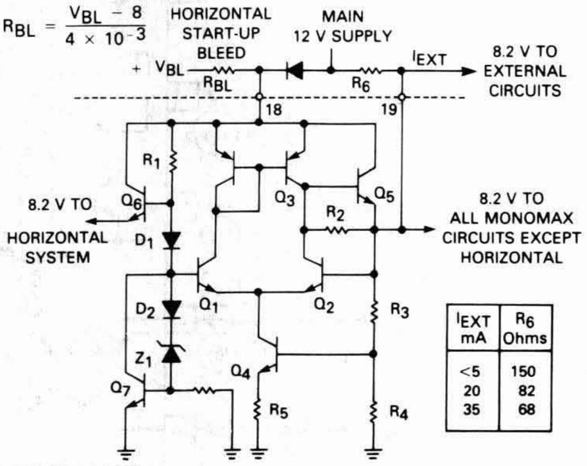
FIGURE 10 — VERTICAL WAVEFORMS



## POWER SUPPLY

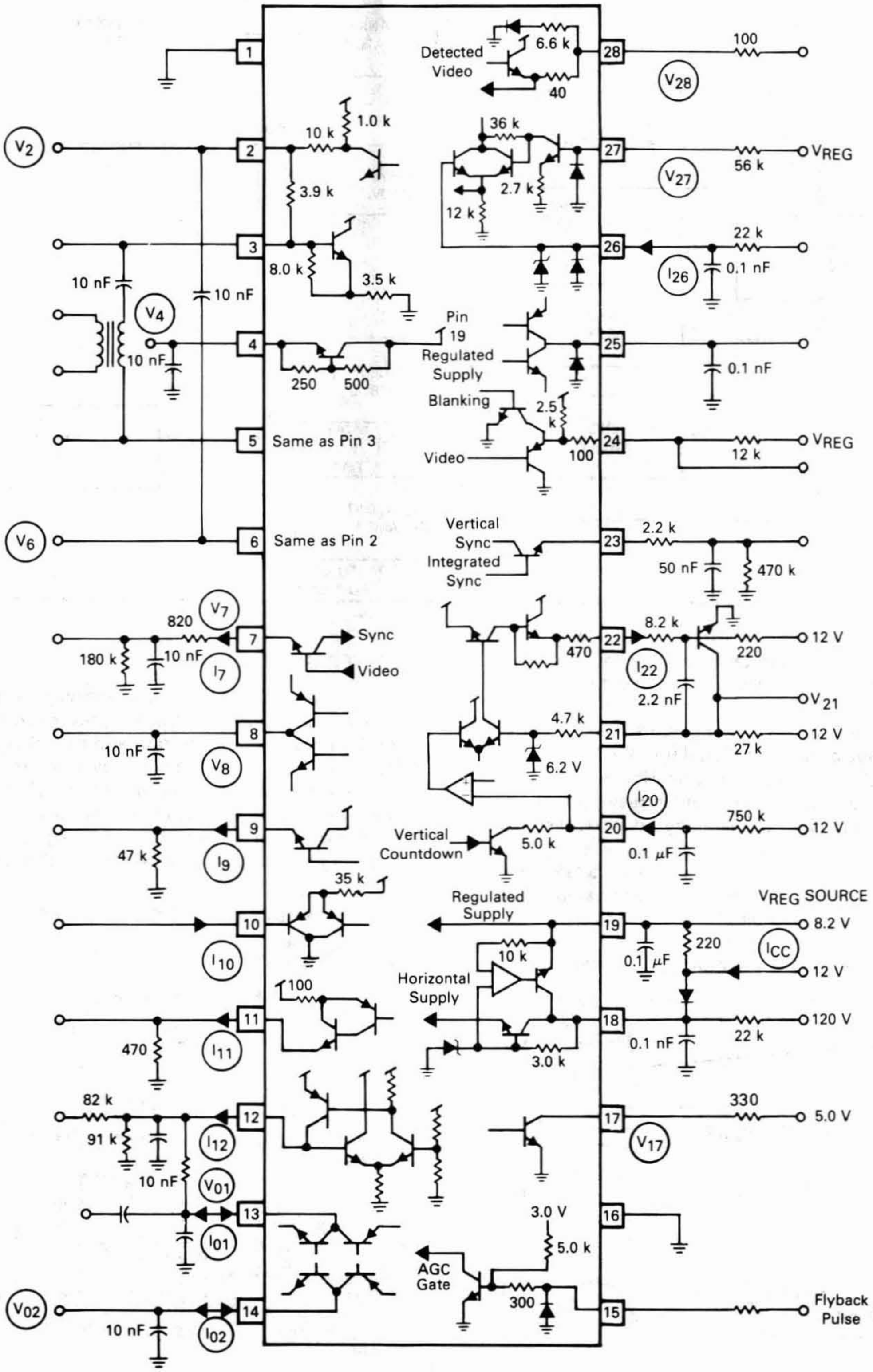
The power supply regulator, although of simple design, provides two independent power supplies — one for the horizontal PLL section and the other for the remainder of the chip. The supplies share the same reference voltage but the design of the main regulator is such that it can be switched on independently to give minimum loading on the "bleed" voltage source during start-up phase of a deflection-derived supply system.

FIGURE 11 — POWER SUPPLY CIRCUIT

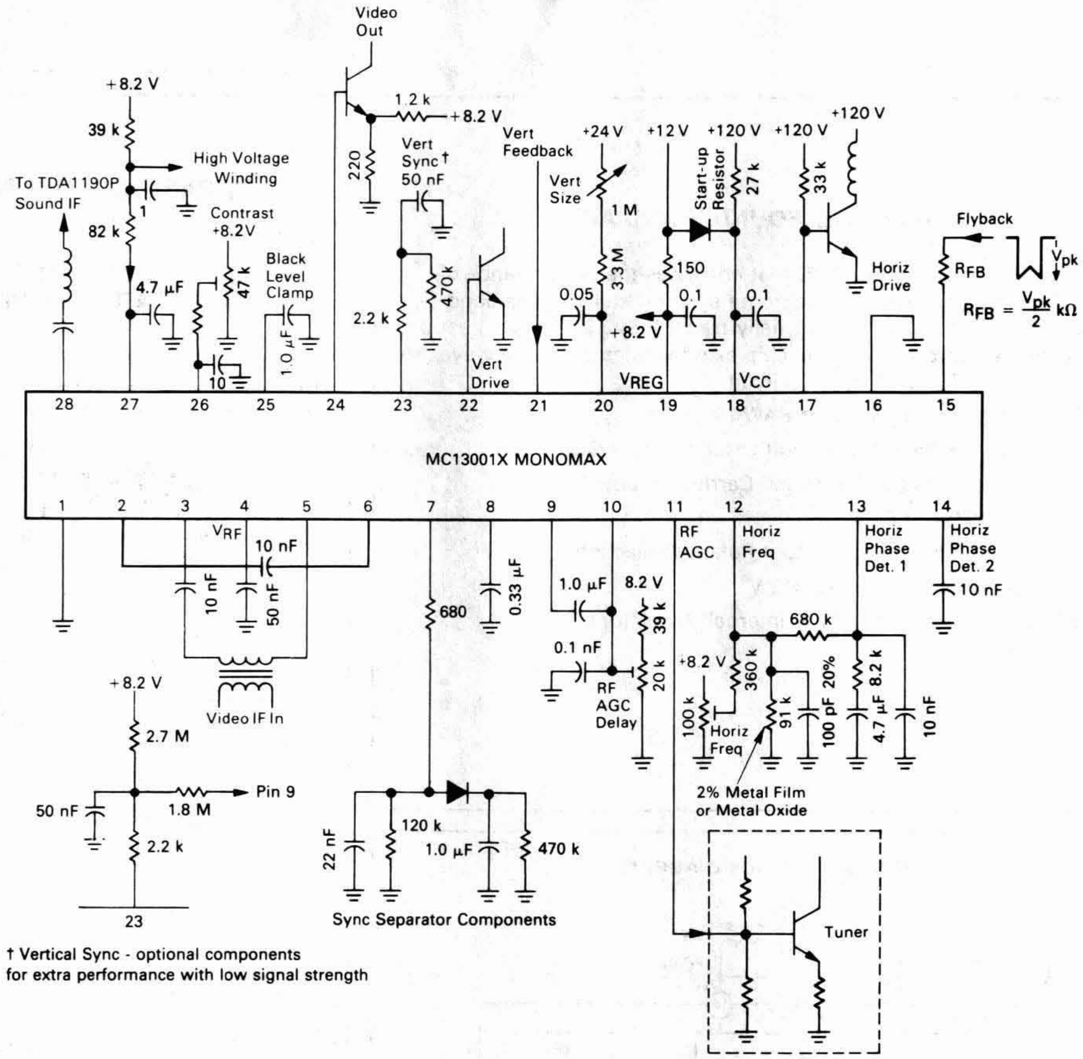

$R_{BL} = \frac{V_{BL} - 8}{4 \times 10^{-3}}$
HORIZONTAL START-UP BLEED
MAIN 12 V SUPPLY
+ $V_{BL}$
$R_{BL}$
$R_6$
$I_{EXT}$
8.2 V TO EXTERNAL CIRCUITS
18
19
$R_1$
$Q_6$
$Q_3$
$Q_5$
$R_2$
8.2 V TO HORIZONTAL SYSTEM
$D_1$
8.2 V TO ALL MONOMAX CIRCUITS EXCEPT HORIZONTAL
$D_2$
$Q_1$
$Q_2$
$R_3$
$Z_1$
$Q_4$
$Q_7$
$R_5$
$R_4$

| $I_{EXT}$ mA | $R_6$ Ohms |
|---|---|
| <5 | 150 |
| 20 | 82 |
| 35 | 68 |

FIGURE 12 — TEST CIRCUIT DIAGRAM


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
Detected Video
6.6 k
40
100
V28
36 k
2.7 k
12 k
56 k
VREG
V27
22 k
0.1 nF
I26
V2
10 k
1.0 k
3.9 k
8.0 k
3.5 k
10 nF
10 nF
V4
10 nF
250
500
Pin 19 Regulated Supply
0.1 nF
Blanking
2.5 k
Video
100
Same as Pin 3
12 k
VREG
V6
Same as Pin 2
Vertical Sync
Integrated Sync
2.2 k
50 nF
470 k
820
V7
180 k
10 nF
I7
Sync
Video
8.2 k
470
220
12 V
I22
2.2 nF
V21
4.7 k
6.2 V
27 k
12 V
10 nF
V8
I20
Vertical Countdown
5.0 k
750 k
12 V
0.1 μF
47 k
I9
35 k
Regulated Supply
VREG SOURCE
8.2 V
0.1 μF
220
ICC
12 V
10 k
Horizontal Supply
I10
100
470
I11
3.0 k
0.1 nF
22 k
120 V
82 k
91 k
10 nF
I12
V01
330
5.0 V
V17
3.0 V
5.0 k
I01
AGC Gate
300
V02
10 nF
I02
Flyback Pulse

### FIGURE 13 — TYPICAL APPLICATION


Video Out
+8.2 V
39 k
High Voltage Winding
To TDA1190P Sound IF
1
82 k
Contrast +8.2V
4.7 µF
47 k
Black Level Clamp
10
1.0 µF
1.2 k
+8.2 V
220
Vert Sync†
50 nF
2.2 k
470 k
Vert Drive
Vert Feedback
Vert Size
+24 V
1 M
3.3 M
0.05
+8.2 V
+12 V
Start-up Resistor
+120 V
27 k
150
0.1
0.1
+120 V
33 k
+120 V
Horiz Drive
Flyback
RFB
Vpk
RFB = Vpk/2 kΩ
VREG
VCC
28
27
26
25
24
23
22
21
20
19
18
17
16
15
MC13001X MONOMAX
1
2
3
4
5
6
7
8
9
10
11
12
13
14
VRF
10 nF
10 nF
50 nF
Video IF In
680
0.33 µF
1.0 µF
8.2 V
39 k
0.1 nF
20 k
RF AGC Delay
RF AGC
Horiz Freq
Horiz Phase Det. 1
Horiz Phase Det. 2
10 nF
680 k
+8.2 V
360 k
100 k
Horiz Freq
91 k
100 pF 20%
8.2 k
4.7 µF
10 nF
2% Metal Film or Metal Oxide
+8.2 V
2.7 M
50 nF
1.8 M
Pin 9
2.2 k
23
22 nF
120 k
1.0 µF
470 k
Sync Separator Components
Tuner

† Vertical Sync - optional components for extra performance with low signal strength

**See Application Note AN879 for further information.**

**MOTOROLA**

# MC13010P

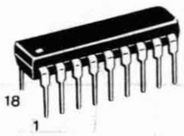
## TV PARALLEL SOUND IF AND AFT

The PSIF is a single-chip IC that enhances the performance of a color TV, audio and video/chroma system. It eliminates bandpass compromises which normally tradeoff 920 kHz video beat with sound performance. The chip also includes a surface wave filter preamplifier and an AFT circuit.

- Low Noise Preamplifier for SAW Filter
- Wideband IF Amplification with Mean Level AGC
- Intercarrier Detector for Sound Carrier Output
- Reduces 920 kHz Beat
- AFT Discriminator with Output Polarity Selection
- Internal Voltage Regulator 8.2 V
- 30 mA Available from 8.2 V Internal Regulator

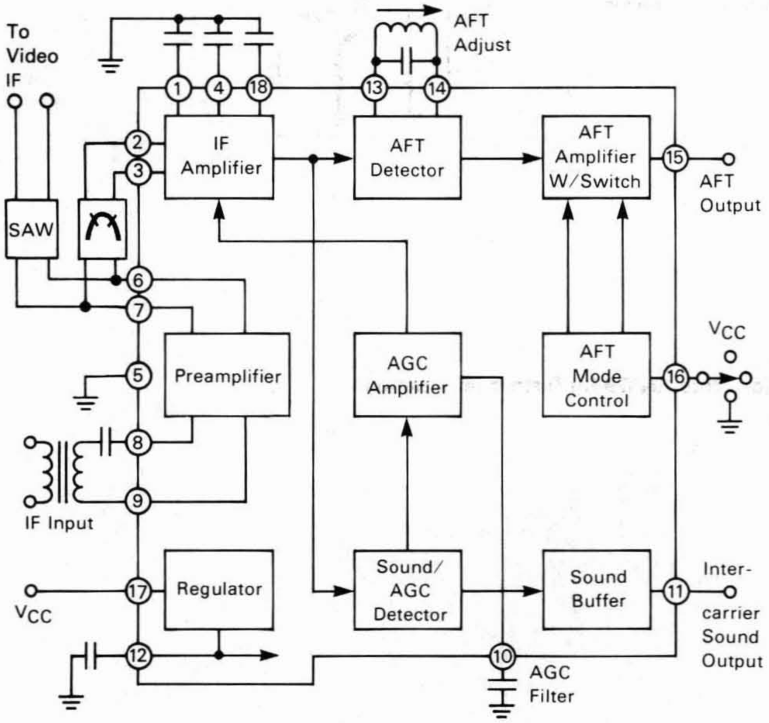
### TV PARALLEL SOUND IF/AFT

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



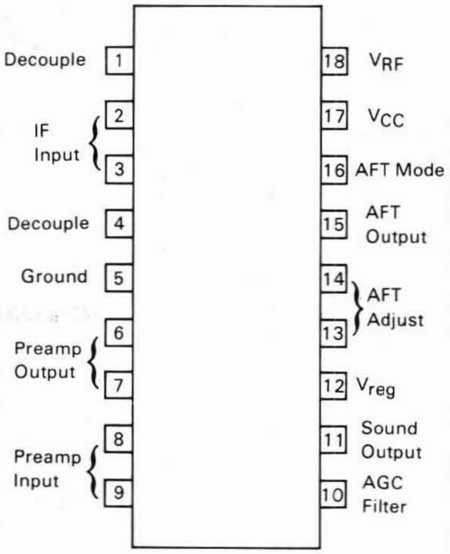
**P SUFFIX**
PLASTIC PACKAGE
CASE 707-02

FIGURE 1 — BLOCK DIAGRAM



To Video IF
AFT Adjust
1
4
18
13
14
2
3
IF Amplifier
AFT Detector
AFT Amplifier W/Switch
15
AFT Output
SAW
6
7
5
Preamplifier
AGC Amplifier
AFT Mode Control
VCC
16
8
9
IF Input
17
Regulator
Sound/ AGC Detector
Sound Buffer
11
Inter-carrier Sound Output
VCC
12
10
AGC Filter

PIN CONNECTIONS



Decouple 1
IF Input 2
3
Decouple 4
Ground 5
Preamp Output 6
7
Preamp Input 8
9
18 VRF
17 VCC
16 AFT Mode
15 AFT Output
14 AFT Adjust
13
12 Vreg
11 Sound Output
10 AGC Filter

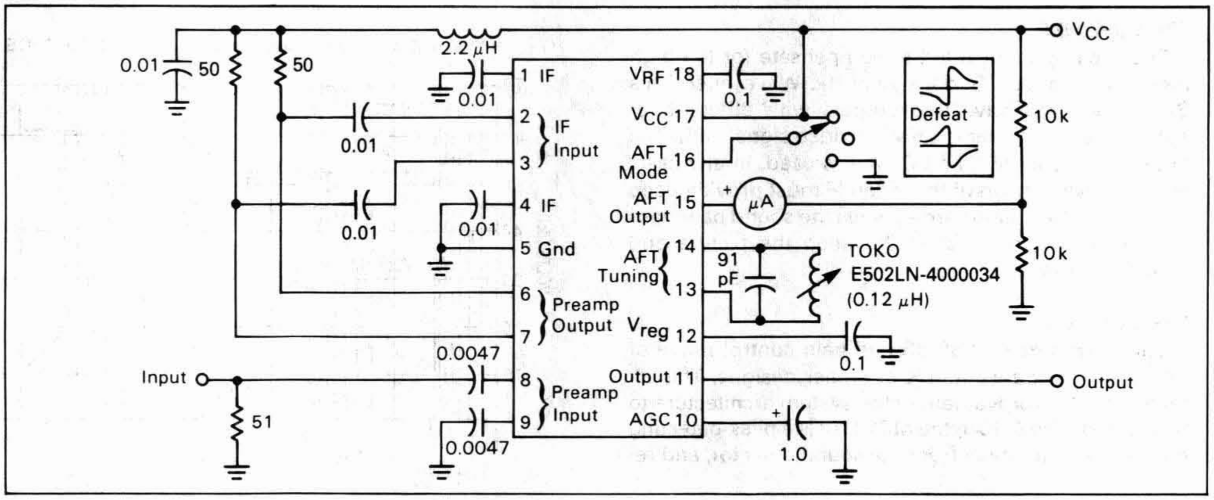
## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CCC}$ | 16 | Vdc |
| Regulator Output Current | $I_{reg}$ | 30 | mAdc |
| Thermal Resistance | $R_{\theta JA}$ | 70 | °C/W |
| Power Dissipation (Package Limitation) | $P_D$ | 1.1 | W |
| Maximum Junction Temperature | $T_{J(max)}$ | 150 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 12 V, $T_A$ = 25°C, Test Circuit of Figure 2, unless otherwise noted)

| Static Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Current | $I_{CC}$ | 30 | — | 60 | mAdc |
| Regulator Voltage, Pin 12 | $V_{reg}$ | 7.6 | 8.2 | 8.8 | Vdc |
| RF Supply Voltage, Pin 18 | $V_{RF}$ | 5.8 | 6.5 | 7.2 | Vdc |
| Preamplifier Current, Pins 6, 7 | | 4.0 | 6.6 | 7.5 | mAdc |
| **Dynamic Characteristics** | | | | | |
| Preamp Gain (Differential Output, 50 Ω Loads) | Av | — | −3.0 | — | dB |
| IF Sensitivity, Output 1.5 $V_{pp}$ Input 45.75 MHz, 30% AM @ 1.0 kHz Differential Pins 2, 3 | | — | 80 | — | $\mu V_{rms}$ |
| AGC Range, Input CW for Output Change of ±0.25 Vdc | | — | 48 | — | dB |
| Intercarrier Sound Output (Beat), Input 45.75 MHz, 7.0 $mV_{rms}$; 41.25 MHz, 2.2 $mV_{rms}$ | | 100 | 200 | 400 | $mV_{rms}$ |
| IF Bandwidth (3.0 dB) | $f_{max}$ | — | 80 | — | MHz |
| Preamplifier Input Resistance<br>Preamplifier Input Capacitance | $R_{in}$<br>$C_{in}$ | —<br>— | 1.5<br>11.5 | —<br>— | kΩ<br>pF |
| IF Input Resistance<br>IF Input Capacitance | $R_{in}$<br>$C_{in}$ | —<br>— | 2.2<br>4.0 | —<br>— | kΩ<br>pF |
| Preamplifier Max Input Signal (Single Ended) | $V_{in}$ | — | 50 | — | $mV_{rms}$ |
| IF Max Input Signal (Differential) | $V_{in}$ | — | 50 | — | $mV_{rms}$ |
| Noise Figure IF, Max Gain<br>Noise Figure Preamplifier | | —<br>— | 6.0<br>5.0 | —<br>— | dB |
| AFT Center-Frequency Slope | | — | 4.0 | — | μA/kHz |
| AFT Output Max, 1.0 MHz Detuning | | — | ±300 | — | μA |

FIGURE 2 — TEST CIRCUIT


0.01
50
50
2.2 μH
0.01
1 IF
2
IF Input
3
0.01
0.01
4 IF
0.01
5 Gnd
6
Preamp Output
7
0.0047
Input
8
Preamp Input
9
51
0.0047
$V_{RF}$ 18
0.1
$V_{CC}$ 17
AFT Mode 16
AFT Output 15
μA
AFT Tuning 14
13
91 pF
TOKO
E502LN-4000034
(0.12 μH)
$V_{reg}$ 12
0.1
Output 11
Output
AGC 10
1.0
Defeat
10k
10k
$V_{CC}$

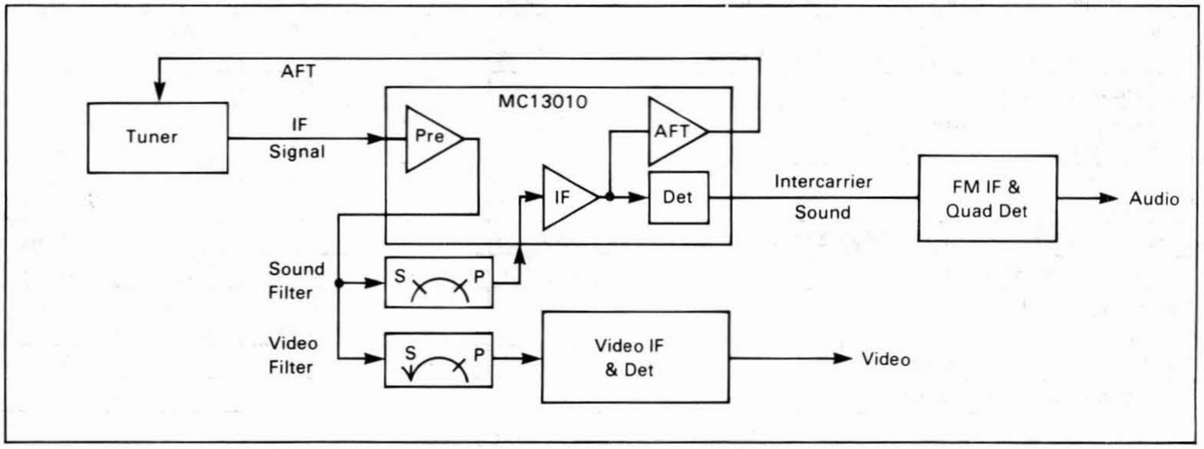
## DESCRIPTION

The MC13010 TV Parallel Sound IF/AFT is designed to be part of a high performance color television system. Its primary function is to provide a complete separate IF amplifier for sound, leaving the normal IF to be concerned only with video. Secondary functions include an AFT detector and a SAW preamp.

In most present day color television receivers, sound and video are processed by the same IF amplifier and, in many cases, the same synchronous or pseudosynchronous detector. This imposes undesirable compromises in video and sound performance. Particularly in the U.S., the avoidance of a color/sound beat product (920 kHz) can only be achieved at the expense of sound quieting and sensitivity. Earlier solutions involved a single IF amplifier driving two detectors, with numerous interstage alignments required.

A method of solving these problems is to process the sound and video separately, directly from the tuner output. The MC13010 provides the second complete IF channel, with its own wideband detector and AGC. This permits both video IF and sound IF to be free of tuned elements, except at their inputs. (See Figure 3.)

FIGURE 3 — BLOCK DIAGRAM OF T.V. APPLICATION OF MC13010



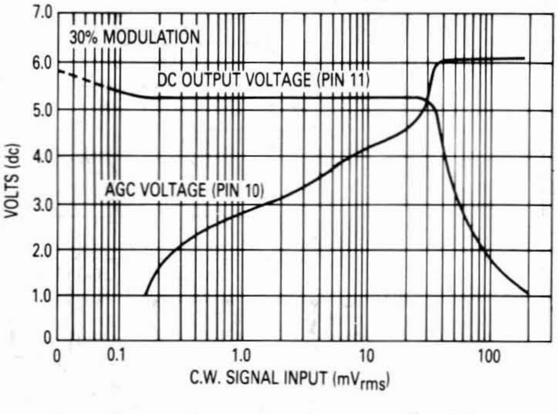
## PREAMPLIFIER

The preamp is included to compensate for the high insertion loss of a Surface Acoustic Wave filter. This SAW filter may have two outputs with different responses, or it may serve only the video signal path. The preamp is optional if an LC filter is used. In any case, the selectivity ahead of the video IF must provide deep trapping of the sound carrier, while the sound bandpass is relatively broad and flat between the picture and sound carriers.

## THE SOUND IF

The overall gain of 80 dB and gain control range of 48 dB equals the video IF's of earlier designs. This allows the full improvement of the system architecture to be realized. The AGC in the MC13010 is a peak-detecting type, driven internally from the sound detector, and requiring only one external filter. The general characteristic of the IF gain and gain control are given in Figure 4. The intercarrier sound output (Pin 11) is typically about 200 $mV_{rms}$, which easily overcomes a lossy intercarrier filter and meets the input needs of even the least sensitive FM sound IF ICs.

FIGURE 4 — GAIN AND AGC CHARACTERISTICS



## AFT

The AFT detector is a quadrature type operating at the picture IF frequency, with only one external L-C to be aligned. The polarity of the AFT output may be changed by taking the mode control (Pin 16) high or low. If the control pin is left open, the AFT is defeated.

## ADDITIONAL APPLICATIONS

The MC13010 is an ideal part for stand-alone AFT. It contains the entire active system to provide a tuner with "self control". (See Figure 6.)

This device performs AM detection at the intercarrier sound output. Therefore, AM modulated digital data may be recovered. This function may be useful in cable systems where digital coding is employed.

FIGURE 5(A) — TYPICAL TV APPLICATION

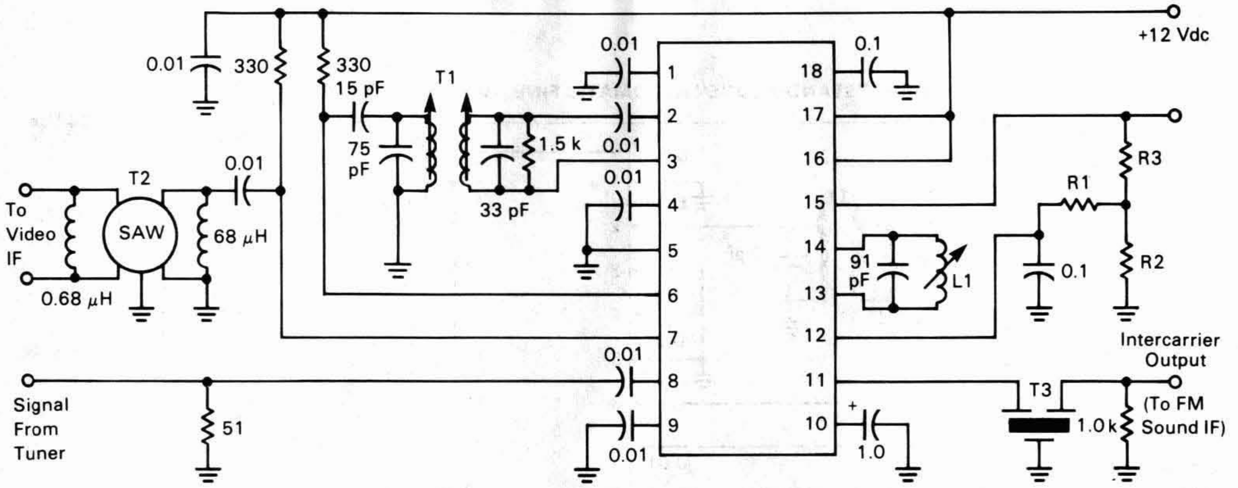
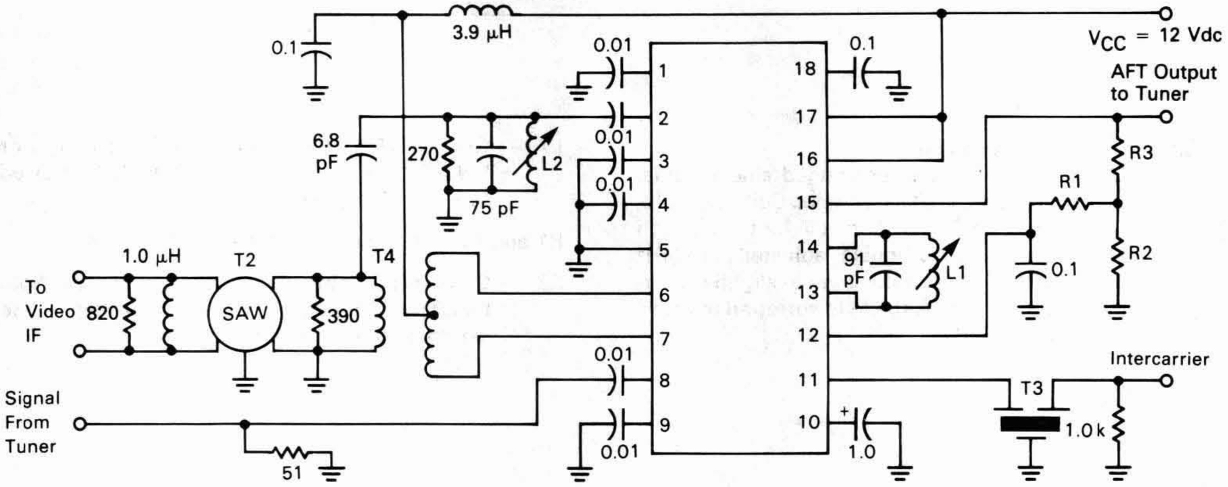

+12 Vdc
0.01
330
330
15 pF
T1
75 pF
1.5 k
0.01
0.01
33 pF
0.01
T2
To Video IF
SAW
68 µH
0.68 µH
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
0.1
R3
R1
0.1
R2
91 pF
L1
Intercarrier Output
0.01
Signal From Tuner
51
T3
1.0 k
(To FM Sound IF)
0.01
+
1.0

FIGURE 5(B) — TYPICAL APPLICATION


3.9 µH
0.1
VCC = 12 Vdc
AFT Output to Tuner
0.01
0.01
0.01
6.8 pF
270
75 pF
L2
R3
R1
R2
0.1
91 pF
L1
1.0 µH
T2
T4
To Video IF
820
SAW
390
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
Intercarrier
0.01
Signal From Tuner
51
0.01
+
1.0
T3
1.0 k

Shown above are two approaches to using the MC13010 in TV designs. The simpler circuit 5(a) offers the lowest cost, but the 12 dB of preamp gain does not overcome the 20 to 25 dB of SAW filter loss. (Bearing in mind that discrete L/C approaches also incur some loss at this point, the 5(a) circuit is probably about equal in gain.) The transformer T4 in Figure 5(b) takes advantage of the high impedance current source nature of the preamp outputs, Pins 6 and 7, to pick up another 6.0 dB of gain. Even more may be possible with more primary turns. When using the coil information given at the right, note that it is based on very limited experience and is offered only as a general guideline.

Experimental values for 45 MHz IF:

T1 — Primary: TOKO E502LN-4000034
Secondary: TOKO E502LN-7000037 in shield case

T2 — Video IF Surface Acoustic Wave (SAW) Filter: muRata, SAF 45MC02Z

T3 — Ceramic Intercarrier Output Filter: muRata SFE 4.5 MB

T4 — TOKO KANAS-K7060EK

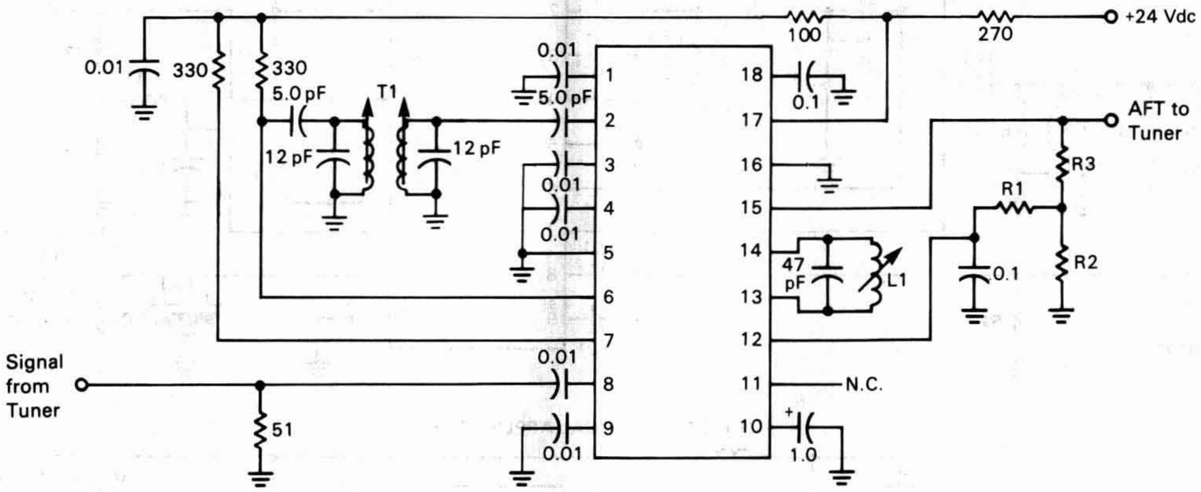
L1 — TOKO E502LN-4000034 J.W. Miller 48A147MPC with shield case, tuned to 45.75, L ≈ 0.12 µH.

L2 — Same part as L1, except tuned to 44 MHz and loaded with 270 Ω

R1 and R2 — Adjust for nominal tuning voltage

R3 — Chosen for tuning voltage swing required. Note that Pin 15 can source or sink 300 µA (typ) at the extremes of control range

FIGURE 6 — "STAND-ALONE" AUTOMATIC FINE TUNING (AFT) APPLICATION


100
270
+24 Vdc
0.01
330
330
5.0 pF
T1
0.01
5.0 pF
12 pF
12 pF
0.01
0.01
0.1
AFT to Tuner
R3
R1
47 pF
L1
0.1
R2
Signal from Tuner
0.01
51
0.01
N.C.
1.0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18

**Channel 3 Component Values**

T1 — Made from two coils positioned side by side, without shields, on 0.38″ centers. Coils are COILCRAFT part no. T7-142 (violet 7-1/2 turns), each with its own slug, Carbonal E, adjusted to 63 MHz (≈0.4 μH). This should give a slightly over-coupled response. A sheild to surround the coils may be required.

L1 — COILCRAFT UNI-7/150 (blue 6-1/2 turns) or UNI-10/144 (green 5-1/2 turns) shielded, adjusted to 61.25 MHz (≈ 0.14 μH)

R1 and R2 — Adjust for nominal tuning voltage

R3 — Chosen for tuning voltage swing required. Note that Pin 15 can source or sink 300 μA (typ) at the extremes of control range

**MOTOROLA**

# MC13020P

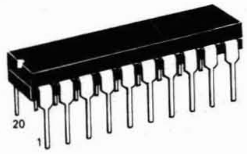
## MOTOROLA C-QUAM® AM STEREO DECODER

This circuit is a complete one-chip full-feature AM stereo decoding and pilot detection system. It employs full-wave envelope signal detection at all times for the L + R signal, and decodes L − R signals only in the presence of valid stereo transmission.

- No Adjustments, No Coils
- Few Peripheral Components
- True Full-Wave Envelope Detection for L + R
- PLL Detection For L − R
- 25 Hz Pilot Presence Required To Receive L − R
- Pilot Acquisition Time 300 ms For Strong Signals, Time Extended For Noise Conditions To Prevent "Falsing"
- Internal Level Detector Can Be Used As AGC Source

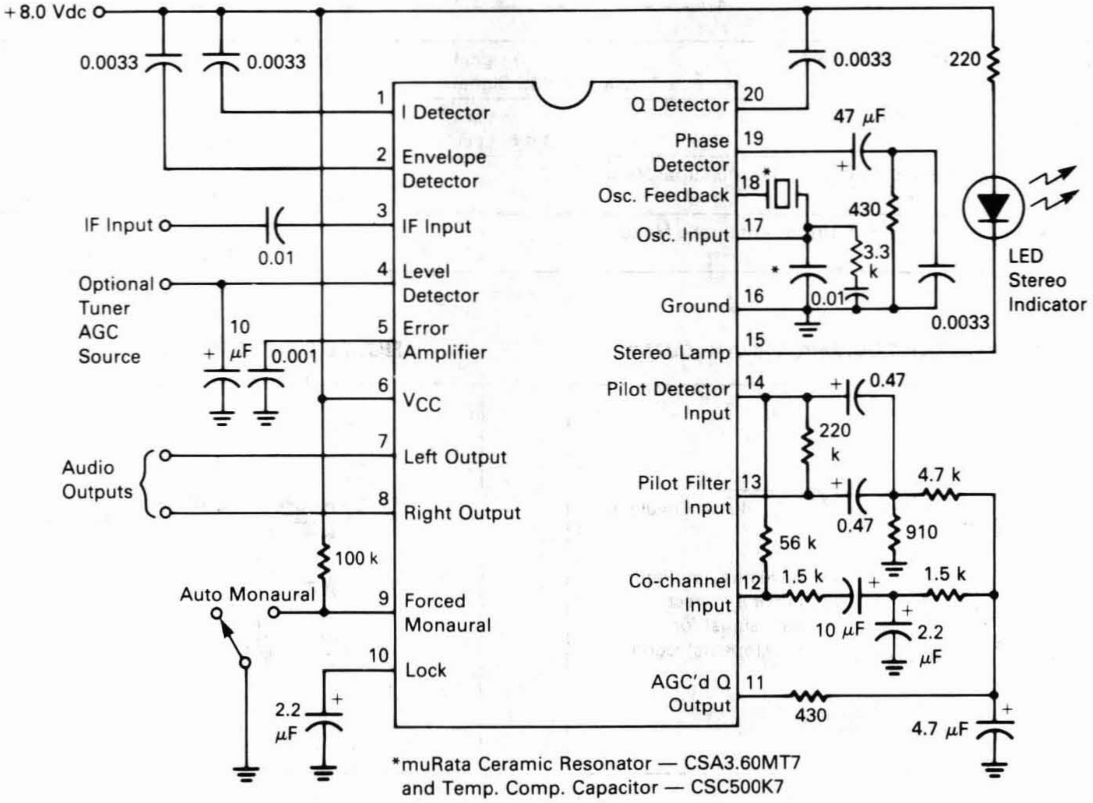
## MOTOROLA C-QUAM® AM STEREO DECODER

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 738-02

**FIGURE 1 — TYPICAL APPLICATION**


+8.0 Vdc
0.0033
0.0033
0.0033
220
1
I Detector
Q Detector
20
47 μF
2
Envelope Detector
Phase Detector
19
18*
Osc. Feedback
430
3
IF Input
IF Input
Osc. Input
17
0.01
3.3 k
LED Stereo Indicator
4
Level Detector
Optional Tuner AGC Source
Ground
16
0.01
0.0033
10 μF
0.001
5
Error Amplifier
Stereo Lamp
15
6
VCC
Pilot Detector Input
14
0.47
220 k
7
Left Output
Audio Outputs
8
Right Output
Pilot Filter Input
13
0.47
4.7 k
910
56 k
100 k
Auto Monaural
9
Forced Monaural
Co-channel Input
12
1.5 k
1.5 k
10 μF
2.2 μF
10
Lock
AGC'd Q Output
11
430
2.2 μF
4.7 μF

*muRata Ceramic Resonator — CSA3.60MT7
and Temp. Comp. Capacitor — CSC500K7

C-QUAM is a trademark of Motorola Inc.

The purchase of the Motorola C-QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

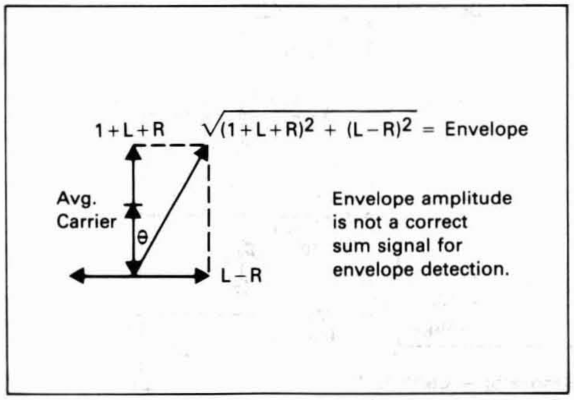
**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 14 | Vdc |
| Pilot Lamp Current, Pin 15 | | 50 | mAdc |
| Operating Temperature | $T_A$ | −40 to +85 | °C |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature | $T_{J(max)}$ | 150 | °C |
| Power Dissipation<br>Derate above 25°C | $P_D$ | 1.25<br>10 | W<br>mW/°C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 8.0 Vdc, $T_A$ = 25°C, Input Signal = 200 mVRMS (Unmodulated Carrier, Circuit Of Figure 1 Unless Otherwise Noted.)

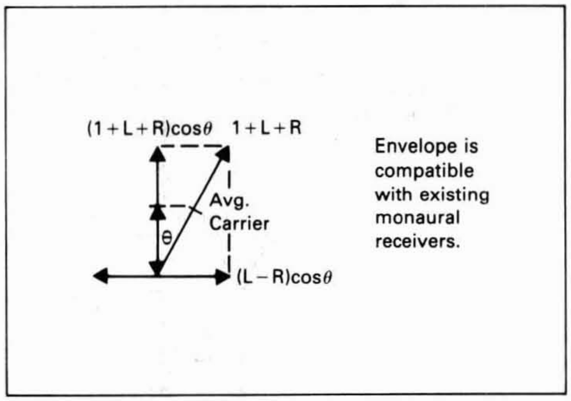
| Characteristic | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Operating Range | | — | 6.0 to 10 | — | Vdc |
| Supply Line Current Drain, Pin 6 | | 20 | 30 | 40 | mAdc |
| Input Signal Level, Unmodulated, Pin 3, for Full Operation | | 100 | 200 | 357 | mVRMS |
| Audio Output Level, 50% Modulation, L only or R only | | 160 | 220 | 280 | mVRMS |
| Audio Output Level, 50% Modulation, Monaural | | 80 | 110 | 140 | mVRMS |
| Output THD, 50% Modulation | Monaural<br>Stereo | —<br>— | 0.5<br>1.0 | —<br>— | % |
| Channel Separation, L only or R only, 50% Modulation | | — | 30 | — | dB |
| Pilot Acquisition Time, VCO locked, after release of forced monaural | | — | 300 | — | ms |
| Input Impedance | $R_{in}$<br>$C_{in}$ | 20<br>— | 27<br>6.0 | —<br>— | kΩ<br>pF |
| Output Impedance | | — | 100 | 150 | Ω |
| Level Detector Filter Voltage, Pin 4, | 0 signal<br>200 mVRMS Signal | 1.4<br>— | 1.7<br>2.5 | 2.0<br>— | Vdc |
| Lock Detector Filter Voltage, Pin 10 | In Lock<br>Out of Lock | —<br>— | 7.8<br>0.8 | —<br>— | Vdc |
| Force to Monaural, Pin 9, Pull Down for Monaural Mode | | 2.0<br>— | 2.5<br>0.15 | —<br>1.0 | Vdc<br>μA |
| Force to Monaural, Pin 9, Pull Up for Automatic Mode | | —<br>— | 3.5<br><0.001 | 3.7<br>1.0 | Vdc<br>μA |

**FIGURE 2 — BASIC QUADRATURE AM (QUAM)**



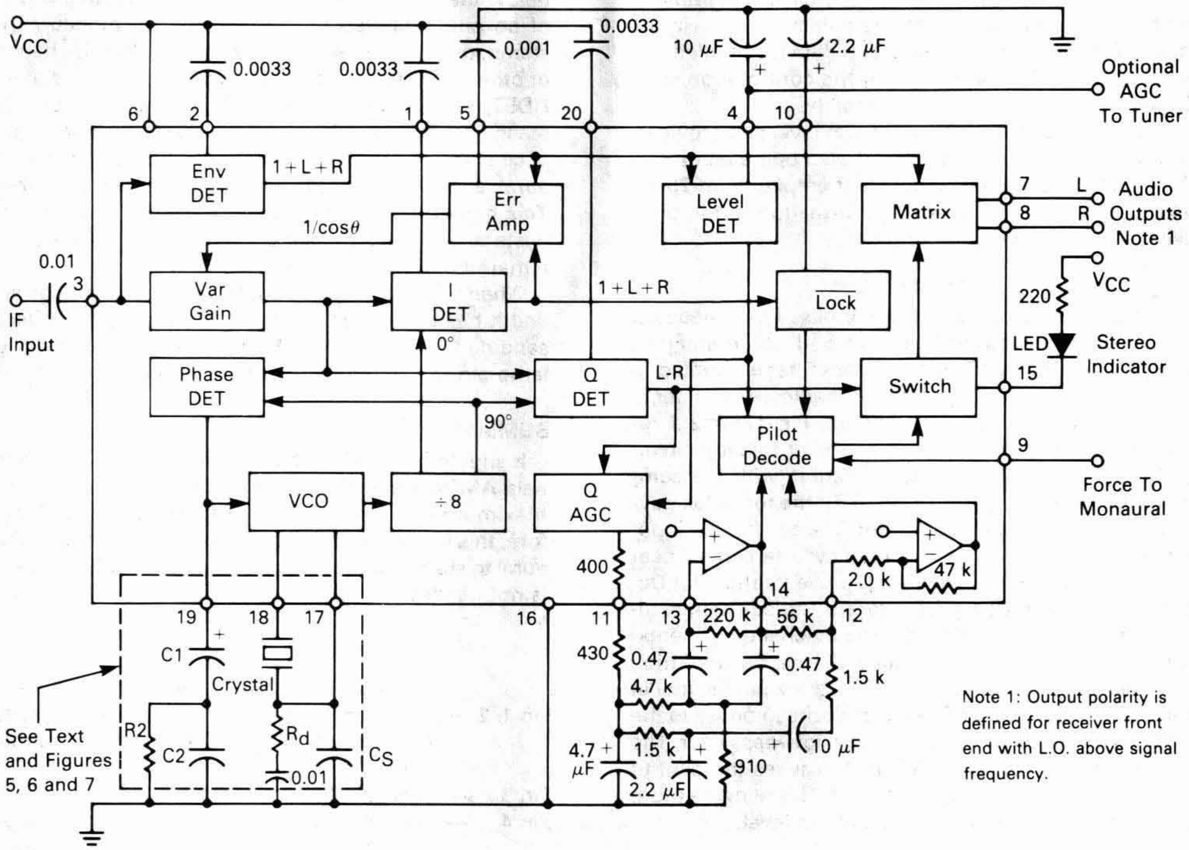
Envelope amplitude is not a correct sum signal for envelope detection.

**FIGURE 3 — MOTOROLA C-QUAM®**



Envelope is compatible with existing monaural receivers.

FIGURE 4 — BLOCK DIAGRAM


VCC
0.0033
0.0033
0.001
0.0033
10 μF
2.2 μF
Optional
AGC
To Tuner
6
2
1
5
20
4
10
Env DET
1+L+R
Err Amp
Level DET
Matrix
7
8
L
R
Audio
Outputs
Note 1
1/cosθ
0.01
3
IF Input
Var Gain
I DET
0°
1+L+R
Lock
220
VCC
LED
Stereo Indicator
15
Phase DET
Q DET
L-R
Switch
90°
Pilot Decode
9
Force To Monaural
VCO
÷8
Q AGC
400
2.0 k
47 k
14
19
18
17
16
11
13
220 k
56 k
12
C1
Crystal
430
0.47
0.47
1.5 k
4.7 k
See Text and Figures 5, 6 and 7
R2
C2
Rd
CS
0.01
4.7 μF
1.5 k
10 μF
910
2.2 μF

Note 1: Output polarity is defined for receiver front end with L.O. above signal frequency.

## MOTOROLA C-QUAM® — COMPATIBLE QUADRATURE AM STEREO

### INTRODUCTION

In C-QUAM®, conventional quadrature amplitude modulation has been modified by multiplying each axis by cosθ as shown in Figures 2 and 3. The resulting carrier envelope is 1+L+R, i.e., a correct sum signal for monaural receivers and for stereo receivers operating in monaural mode. A 25 Hz pilot signal is added to the L–R information at a 4% modulation level.

### THE DECODER

The MC13020P takes the output of the AM IF amplifier and performs the complete C-QUAM® decoding function. In the absence of a good stereo signal, it produces an undegraded monaural output. Note in Figure 4 that the L+R information delivered to the output always comes from the envelope detector (Env DET).

The MC13020P decodes the stereo information by first converting the C-QUAM® signal to QUAM, and then detecting QUAM. The conversion is accomplished by comparing the output of the Env DET and the I DET in the Err AMP. This provides the 1/cosθ correction factor, which is then multiplied by the C-QUAM® incoming signal in the Var Gain block. Thus, the output of the Var Gain block is a QUAM signal, which can then be synchronously detected by conventional means. The I and Q detectors are held at 0° and 90° relative demodulation angles by reference signals from the phase-locked, divided-down VCO. The output of the I DET is 1+L+R, with the added benefit (over the Env DET) of being able to produce a negative output on strong co-channel or noise interference. This is used to tell the Lock circuit to go to monaural operation. The output of the Q DET is the L−R and pilot information.

### THE VCO

The VCO operates at 8 times the IF input frequency, which ensures that it is out-of-band, even when a 260 kHz IF frequency is used. Typically a 450 kHz IF frequency is used with synthesized front ends. This places the VCO at 3.6 MHz, which permits economic crystal and ceramic resonators. A crystal VCO is very stable, but cannot be pulled very far to follow front-end mistuning. Pull-in capability of ±100 Hz at 450 kHz is typical, and de-Q-ing with a resistor (see Figure 7) can increase the range only slightly. Therefore, the crystal approach can only be used with very accurate, stable front-ends. By comparison, ceramic and L−C VCO circuits offer pull-in range in the order of ±2.5 kHz (at 450 kHz). Ceramic devices accurate enough to avoid trimming adjustment can be obtained with a matched capacitor for Cs (see Figures 1 and 5).

In the PLL filter circuit on Pin 19, C1 is the primary factor in setting a loop corner frequency of 8–10 Hz, in-lock. An internally controlled fast pull-in is provided. R2 is selected to slightly overdamp the control loop, and C2 prevents high frequency instability.

The Level DET block senses carrier level and provides an optional tuner AGC source. It also operates on the Q AGC block to provide a constant amplitude of 25 Hz pilot at Pin 11, and it delivers information to the pilot decoder regarding signal strength.

### PILOT AND CO-CHANNEL FILTERS

The Q AGC output drives a low pass filter, made up of 400 Ω internal, and 430 Ω and 5 $\mu$F external. From this point, an active 25 Hz band-pass filter is coupled to the Pilot Decoder, Pin 14, and another low-pass filter is connected to the Co-channel Input, Pin 12. A 2:1 reduction of 25 Hz pilot level to the Pilot Decode circuit will cause the system to go monaural, with the components shown. Refer to Figure 8 for the formulas governing the active band-pass filter. The co-channel input signal contains any low frequency intercarrier beat notes, and, at the selected level, prevents the Pilot Decode circuit from going into stereo. The co-channel input, Pin 12, gain can be adjusted by changing the external 1.5 k resistor. The values shown set the "trip" level at about 7% modulation. The 25 Hz pilot signal at the output of the active filter is opposite in phase to the pilot signal coming from the second low-pass filter. The 56 k resistor from Pin 14 to Pin 12 causes the pilot to be cancelled at the co-channel input. This allows a more sensitive setting of the co-channel trip level.

### THE PILOT DECODER

The Pilot Decoder has two modes of operation. When signal conditions are good, the decoder will switch to stereo after 7 consecutive cycles of the 25 Hz pilot tone. When signal conditions are bad, the detected interference changes the pilot counter so as to require 37 consecutive cycles of pilot to go to stereo. In a frequency synthesized radio, the logic that mutes the audio when tuning can be connected to Pin 9. When this pin is held low it holds the decoder in monaural mode and switches it to the short count. This pin should be held low until the synthesizer and decoder have both locked onto a new station. A 300 ms delay should be sufficient. If the synthesizer logic does not provide sufficient delay, the circuit shown in Figure 9 may be added. Once Pin 9 goes high, the Pilot Decoder starts counting. If no pilot is detected for seven consecutive counts, it is assumed to be a good monaural station and the decoder is switched to the long count. This reduces the possibility of false stereo triggering due to signal level fluctuation or noise. If the PLL goes out of lock, or interference is detected by the co-channel protection circuit before seven cycles are counted, the decoder goes into the long count mode. Each disturbance will reset the counter to zero. The Level Detector will keep the decoder from going into stereo if the IF input level drops 10 dB, but will not change the operation of the pilot counter.

Once the decoder has gone into the stereo mode, it will go instantly back to monaural if either the lock detector on Pin 10 goes low, or if the carrier level drops below the preset threshold. Seven consecutive counts of no pilot will also put the decoder in monaural. In stereo, the co-channel input is disabled, and co-channel or other noise is detected by negative excursions of the I DET, as mentioned earlier. When these excursions reach a level caused by approximately 20% modulation of co-channel, the lock detector puts the system in monaural, even though the PLL may still actually be locked. This higher level of co-channel tolerance provides the hysteresis to prevent chattering in and out of stereo on a marginal signal.

When all inputs to the Pilot Decode block are correct, and it has completed its count, it turns on the Switch, sending the L – R to the Matrix, and switches the pilot lamp pin to a low impedance to ground.

### SUMMARY

It should be noted that in C-QUAM®, with both channels AM modulated, the noise increase in stereo is a maximum of 3.0 dB, less on program material. Therefore, this is not the major concern in the choice of monaural to stereo switching point as it was in FM, and blend is not needed.

## PIN DESCRIPTIONS

Pin 1, 2 — Detector Filters, $R_{out}$ = 4.3 k, recommend 0.0033 $\mu$F to $V_{CC}$ to filter 450 kHz components.
Pin 3 — IF Signal Input
Pin 4 — Level Detector filter pin, $R_{out}$ = 8.2 k, 10 $\mu$F to ground sets the AGC time constant. High impedance output, needs buffer.
Pin 5 — Error Amp compensation to stabilize the Var Gain feedback loop
Pin 6 — $V_{CC}$, 6-10 Vdc, suitable for low $V_{batt}$ automotive operation, but must be protected from "high line" condition.
Pin 7, 8 — Left and Right Outputs, NPN emitter followers
Pin 9 — Forced Monaural, MOS or TTL controllable
Pin 10 — Lock detector filter, $R_{out}$ = 27 k, recommend 2.2 $\mu$F to ground.
Pin 11 — AGC'd Q output, NPN emitter follower with 400 Ω from emitter to Pin 11
Pin 12 — Co-channel Input, 2.0 k series in and 47 k feedback
Pin 13 — Pilot Filter Input to op amp, see Figure 8
Pin 14 — Pilot Decode Input (op amp output) emitter follower, $R_{out}$ = 100 Ω
Pin 15 — Stereo Lamp, open-collector of an NPN common emitter stage, can sink 50 mA, $V_{sat}$ = 0.3 V at 5.0 mA
Pin 16 — Ground
Pin 17 — Oscillator input, $R_{in}$ = 10 k, do not dc connect to Pin 18 or ground
Pin 18 — Oscillator feedback, NPN emitter, $R_{out}$ = 100 Ω
Pin 19 — Phase Detector Output, current source to filter
Pin 20 — Detector Filter, $R_{out}$ = 4.3 k, recommend 0.0033 $\mu$F to $V_{CC}$ to filter 450 kHz

FIGURE 5 — CERAMIC VCO

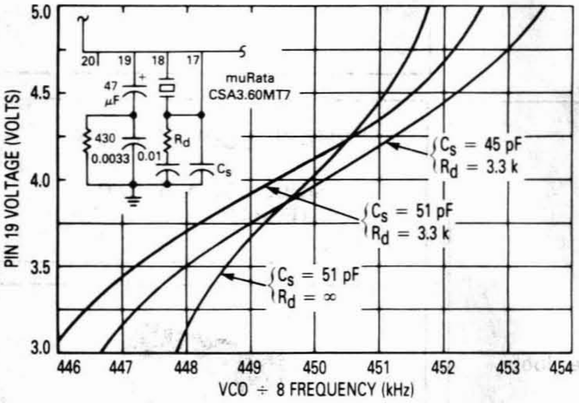


FIGURE 6 — L-C VCO

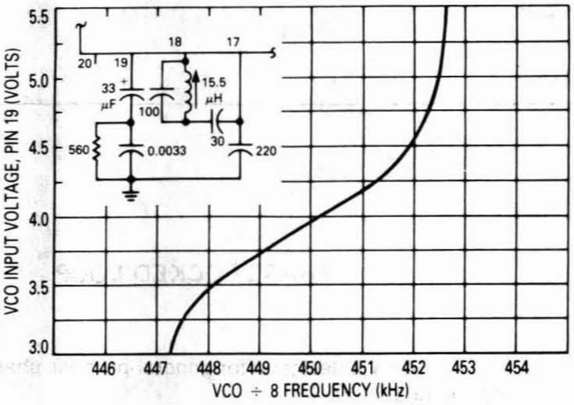


FIGURE 7 — CRYSTAL VCO

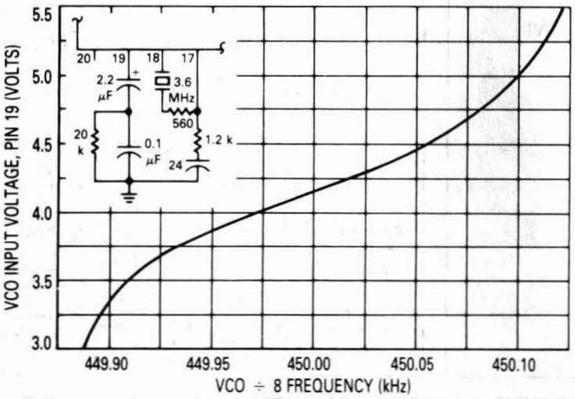
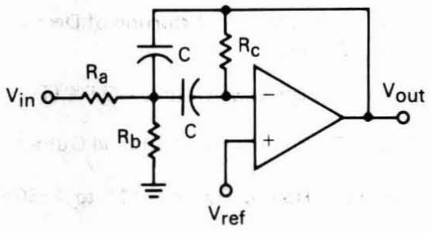


FIGURE 8 — ACTIVE BAND-PASS FILTER



C
Rc
Ra
Vin
C
Rb
Vout
Vref

$$R_c = \frac{Q}{\pi f_o C}$$

$$R_a = \frac{R_c}{2 A_o}$$

$$R_b = \frac{R_a R_c}{4Q^2 R_a - R_c}$$

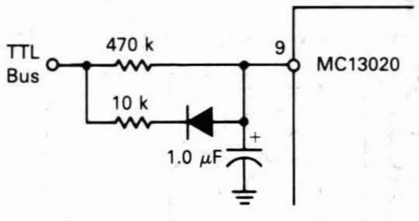
where, in this application:
$f_o$ = center frequency = 25 Hz
$A_o$ = gain at $f_o \leq 25$
$Q \leq 10$

Choose values for $f_o$, $A_o$, Q, and convenient C, solve for resistors

| C ± 5% | $R_a$ ± 5% | $R_b$ ± 1% | $R_c$ ± 1% |
|---|---|---|---|
| 0.47 μF | 4.7 k | 910 | 220 k |
| 0.33 μF | 8.2 k | 1.3 k | 330 k |

Note: Capacitor C should be a good grade, low ESR.

FIGURE 9 — FORCED MONAURAL OPTIONAL DELAY CIRCUIT



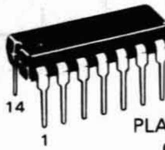
TTL Bus
470 k
9
MC13020
10 k
1.0 μF

**MOTOROLA**

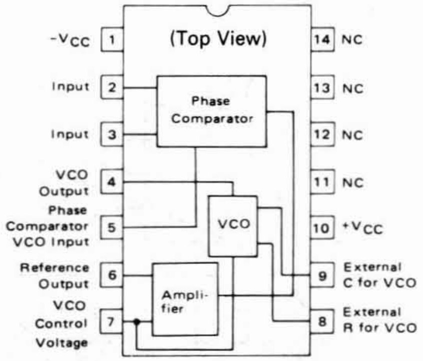
# NE565A

## PHASE-LOCKED LOOP

**SILICON MONOLITHIC INTEGRATED CIRCUITS**



**P SUFFIX**
PLASTIC PACKAGE
CASE 646-05

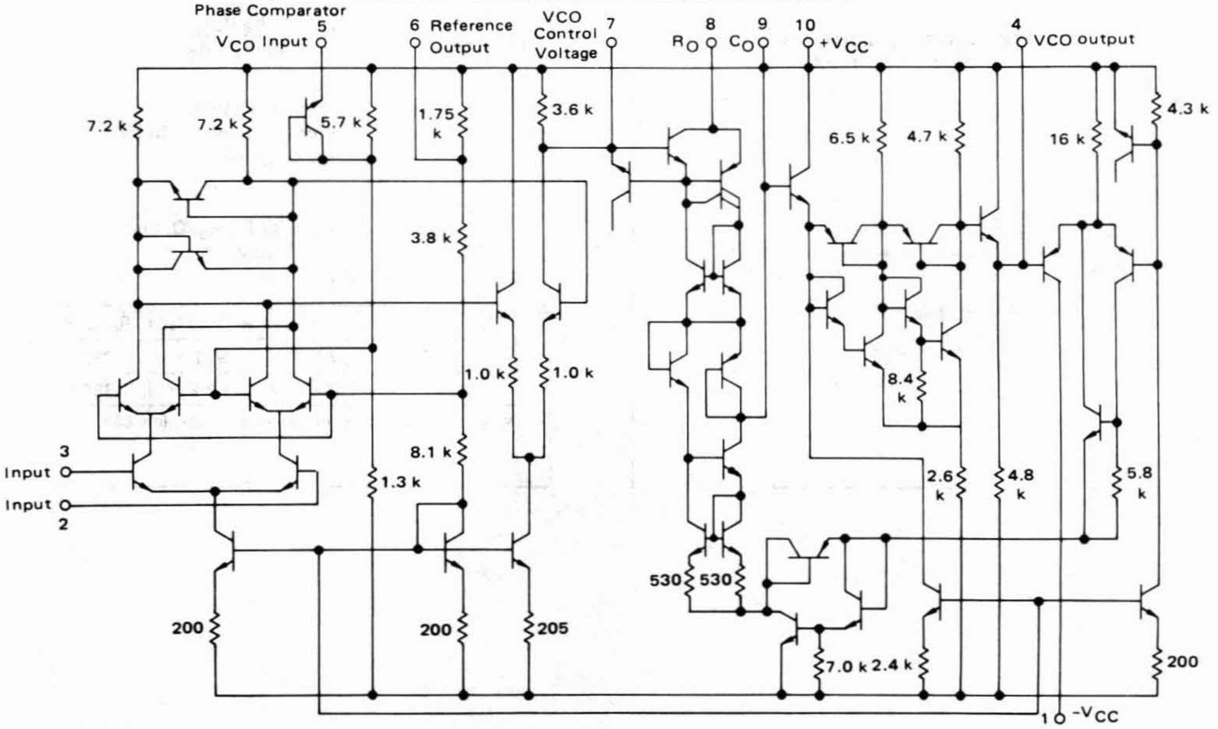

(Top View)
-VCC 1
Input 2
Input 3
VCO Output 4
Phase Comparator VCO Input 5
Reference Output 6
VCO Control Voltage 7
External R for VCO 8
External C for VCO 9
+VCC 10
NC 11
NC 12
NC 13
NC 14
Phase Comparator
VCO
Amplifier

## PHASE-LOCKED LOOP

The NE565A is designed for general-purpose phase-locked loop applications to 500 kHz.

- Stable Center Frequency – 200 ppm/°C (Typ)
- Flexible Power Supply Range – ±5 to ±12 Volts with Small Frequency Drift – 100 ppm/% (Typ)
- Low Total Harmonic Distortion of Demodulator Output – 1.5% (Max)
- Linear Triangle Wave Output – 0.5% (Typ)
- TTL, DTL Compatible Inputs and Outputs
- Adjustable Hold In Range – ±1% to >±60%.

FIGURE 1 – REPRESENTATIVE CIRCUIT SCHEMATIC


Phase Comparator VCO Input 5
6 Reference Output
VCO Control Voltage 7
8 RO
9 CO
10 +VCC
4 VCO output
7.2 k
7.2 k
5.7 k
1.75 k
3.6 k
6.5 k
4.7 k
16 k
4.3 k
3.8 k
1.0 k
1.0 k
8.4 k
3 Input
Input 2
8.1 k
1.3 k
2.6 k
4.8 k
5.8 k
530
530
200
200
205
7.0 k
2.4 k
200
1 -VCC

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | ±12 | Vdc |
| Power Dissipation (Package Limitation)<br>Derate above 25°C | $P_D$ | 8.25<br>6.6 | mW<br>mW/°C |
| Operating Ambient Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |

### ELECTRICAL CHARACTERISTICS (Test Circuit Figure 2, $T_A$ = 25°C, $V_{CC}$ = ±6.0 Vdc unless otherwise noted.)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Power Supply Current | – | 8.0 | 12.5 | mA |
| Input Impedance (Pins 2, 3)<br>-4.0 V < V2, V3 < 0 V | – | 5.0 | – | kΩ |
| Input Level Required for Tracking<br>$f_o$ = 10 kHz, ±10% Frequency Deviation | 10 | – | – | mVrms |
| VCO Maximum Operating Frequency<br>$C_o$ = 2.7 pF | – | 500 | – | kHz |
| Operating Frequency Temperature Coefficient | – | 200 | – | ppm/°C |
| Frequency Drift with Supply Voltage | – | 200 | – | ppm/% |
| Triangle Wave Ouptut Voltage | 2.0 | 2.4 | 3.0 | Vp-p |
| Triangle Wave Output Linearity | – | 0.5 | – | % |
| Square Wave Output Level | 4.7 | 5.4 | – | Vp-p |
| VCO Output Impedance (Pin 4) | – | 5.0 | – | kΩ |
| Square Wave Duty Cycle | 40 | 50 | 60 | % |
| Square Wave Rise Time | – | 20 | – | ns |
| Square Wave Fall Time | – | 50 | – | ns |
| Output Current Sink (Pin 4) | 0.6 | 1.0 | – | mA |
| VCO Sensitivity | – | 6600 | – | Hz/V |
| Demodulated Output Voltage (Pin 7)<br>$f_o$ = 10 kHz, ±10% Frequency Deviation | 200 | 300 | – | mVp-p |
| Total Harmonic Distortion<br>$f_o$ = 10 kHz, ±10% Frequency Deviation | – | 0.2 | 1.5 | % |
| Output Impedance (Pin 7) | – | 3.5 | – | kΩ |
| DC Output Voltage Level (Pin 7) | 4.0 | 4.5 | 5.0 | V |
| Output Offset Voltage (Input = 0)<br>/V7-V6/ | – | 50 | 200 | mV |
| Temperature Drift of /V7-V6/ | – | 500 | – | µV/°C |
| AM Rejection | – | 40 | – | dB |
| Phase Detector Sensitivity $K_D$ | – | 0.68 | – | V/radian |

FIGURE 2 – TEST CIRCUIT SCHEMATIC

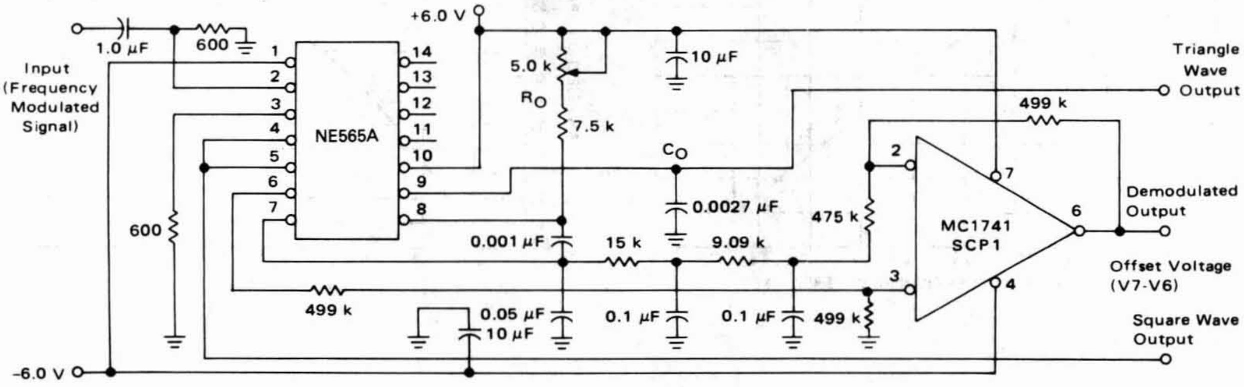

+6.0 V
1.0 µF
600
Input (Frequency Modulated Signal)
1
2
3
4
5
6
7
14
13
12
11
10
9
8
NE565A
5.0 k
$R_O$
7.5 k
10 µF
$C_O$
0.0027 µF
0.001 µF
15 k
9.09 k
475 k
499 k
2
3
7
6
4
MC1741 SCP1
Triangle Wave Output
Demodulated Output
Offset Voltage (V7-V6)
Square Wave Output
600
499 k
0.05 µF
10 µF
0.1 µF
0.1 µF
499 k
-6.0 V

FIGURE 3 – POWER SUPPLY CHARACTERISTICS

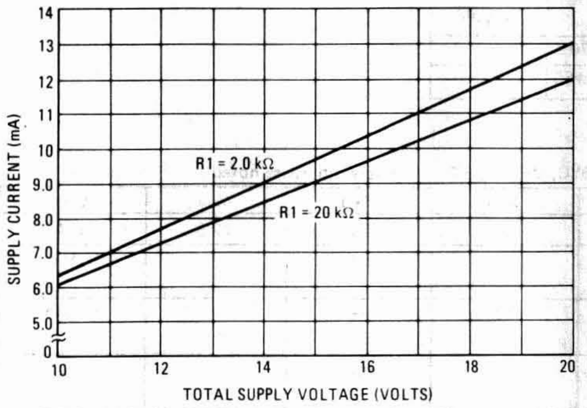


FIGURE 4 – VCO CONVERSION GAIN

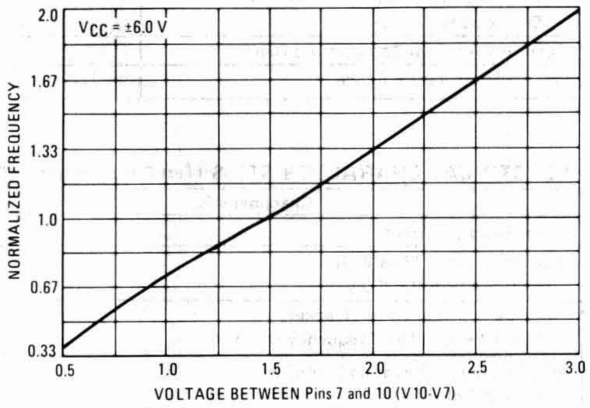


FIGURE 5 – LOCK RANGE versus INPUT VOLTAGE

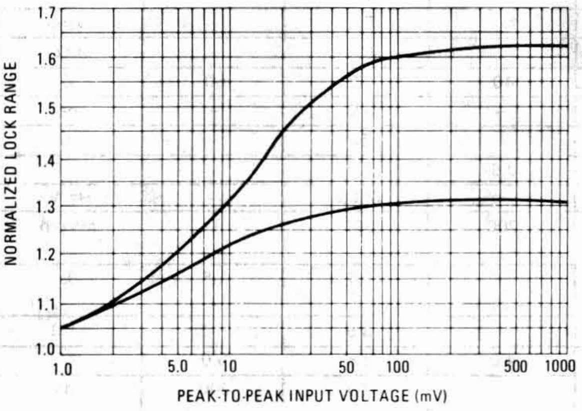


FIGURE 6 – OSCILLATOR OUTPUT WAVEFORMS

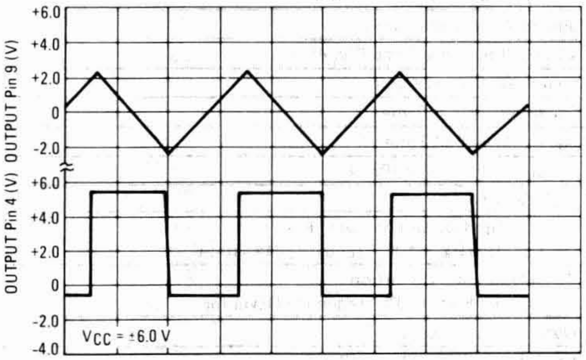


FIGURE 7 – LOCK RANGE
(As a Function of Gain Setting Resistance)

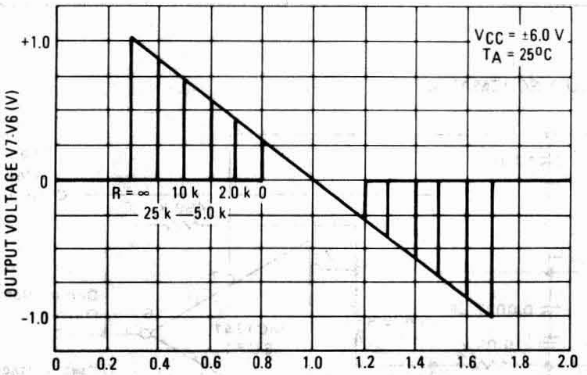
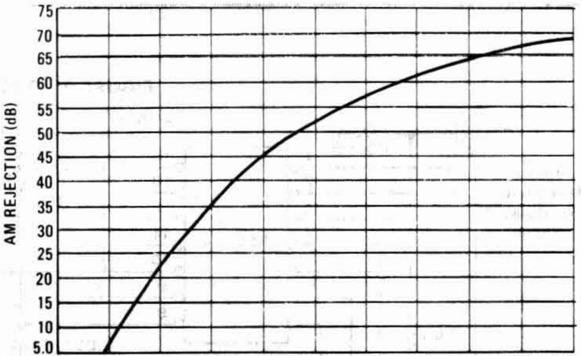


FIGURE 8 – AM REJECTION CHARACTERISTICS



## GENERAL APPLICATIONS INFORMATION

The following formulas are useful when designing with the NE565A:

1. Center Frequency – $f_O \approx \frac{1}{3.7\, R_O C_O}$

   Where: $f_O$ is the frequency of the VCO without input signal. For $R_O$, $C_O$ circuit location see Figure 2.

2. Loop Gain – $K_O K_D A$

   Definitions:

   $K_O$ – VCO Conversion Gain – the conversion factor between VCO frequency and control voltage.
   $K_O = 4.12\, f_O$ (units are in radians/sec/volt)
   Example: for VCO Sensitivity @ 10 kHz (in Hz/volt)

   $$K_O = \frac{4.12 \times 10^4}{2\pi \text{ radians}} = 6600 \text{ Hz/Volt}$$

   $K_D$ – Phase Detector Gain Factor – the conversion factor between the phase detector output voltage and the phase difference between input and VCO signals. Units are in volts/radian.

   $$K_D = \frac{8.1 \bullet A}{V_{CC}}$$

   Where: $A = f(R6 \text{ to } R7)$

   Hence: $K_D = \frac{8.1}{V_{CC}}\,[f(R6\text{-}R7)]$

   Where: $V_{CC}$ is total system supply voltage, f(R6-R7) is internal amplifier gain (See Figure 9). $V_{CC}$ - total supply voltage to the circuit.

3. Lock Range – $f_L = \pm \frac{8 f_O}{V_{CC}}$

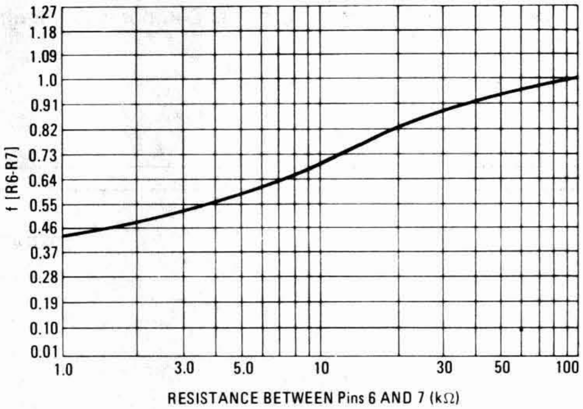
   Where: $f_L$ is the range of frequencies in the area of $f_O$ over which the VCO, once locked to the input signal, will remain locked.

4. Capture Range – $f_C \approx \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

   Where: $f_C$ is that range of frequencies around $f_O$ over which the loop will acquire lock with an input signal initially starting out of lock.

   ($\tau$ = Time Constant at Pin 7)

**FIGURE 9 – INTERNAL AMPLIFIER GAIN CHARACTERISTICS**



**MOTOROLA**

# TBA120C

## FM IF AMPLIFIER, LIMITER AND DETECTOR

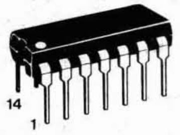
An integrated circuit specifically designed for use in the sound section of TV receivers and the FM/IF portion of radio receivers.

The TBA120C is pin for pin and function compatible with the proelectron type TBA120S but includes an improved dc volume control, which makes "grouping" or selection unnecessary.

- Excellent 3.0 dB Limiting
- High A.M. Rejection
- Wide Supply Voltage Range
- Auxiliary Zener Diode & Transistor
- Minimum Number of External Components Required

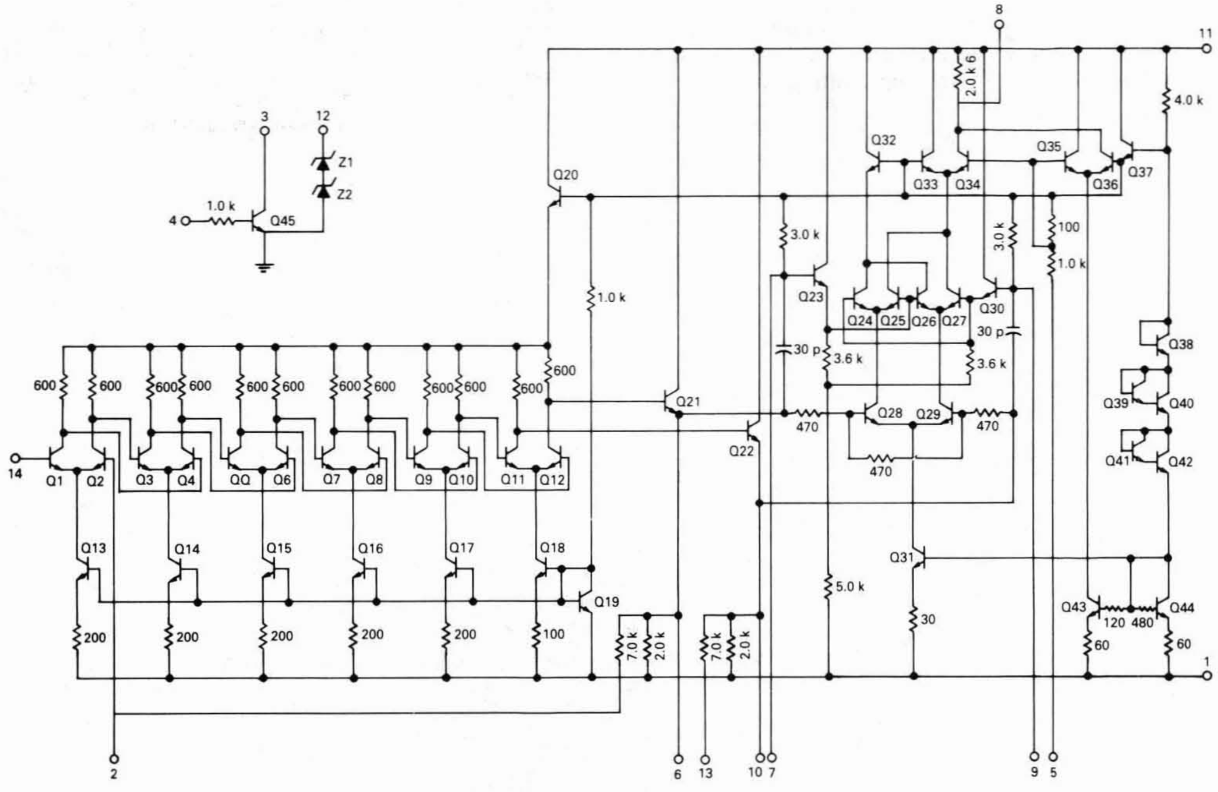
**FM IF AMPLIFIER,**
**LIMITER, FM DETECTOR**
**AND**
**AUDIO PREAMPLIFIER**

**SILICON MONOLITHIC**
**INTEGRATED CIRCUIT**



PLASTIC PACKAGE
CASE 646-05

**CIRCUIT SCHEMATIC**


8
11
2.0 k 6
4.0 k
3
12
Z1
Z2
1.0 k
4
Q45
Q20
Q32
Q33
Q34
Q35
Q36
Q37
3.0 k
3.0 k
100
1.0 k
1.0 k
Q23
Q24
Q25
Q26
Q27
Q30
30 p
30 p
3.6 k
3.6 k
Q38
600
600
600
600
600
600
600
600
600
600
600
600
600
Q21
470
Q28
Q29
470
470
Q22
Q39
Q40
Q41
Q42
14
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q31
Q19
5.0 k
Q43
Q44
120
480
200
200
200
200
200
100
7.0 k
2.0 k
7.0 k
2.0 k
30
60
60
1
2
6
13
10
7
9
5

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage | +18 | Vdc |
| Power Dissipation (Package Limitation)<br>Plastic Package<br>Derate above $T_A$ = +25°C | <br>625<br>5.0 | <br>mW<br>mW/°C |
| Operating Temperature Range | 0 to +75 | °C |
| Storage Temperature Range | −65 to +150 | °C |

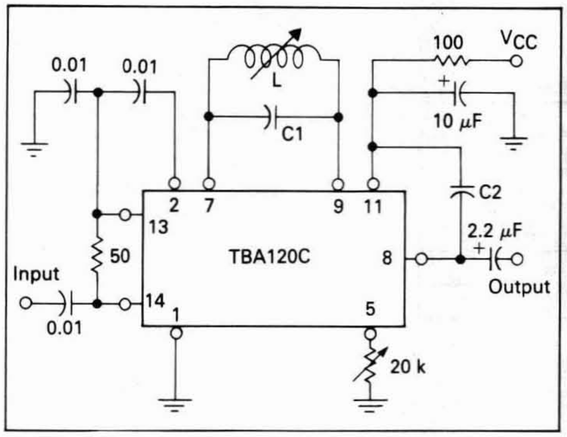
**ELECTRICAL CHARACTERISTICS** ($T_A$ = +25°C, $V_{CC}$ = 12 V, R = 20 k, Test circuit: Figure 1)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Supply Voltage Range | 6.0 | — | 18 | Volts |
| Supply Current | 10 | 14 | 18 | mA |
| Audio Output ($f_O$ = 5.5 MHz, Δf = 50 kHz, Q = 45) | — | 1.0 | — | Volts RMS |
| Audio Output ($f_O$ = 10.7 MHz, Δf = 75 kHz, Q = 35) | — | 0.38 | — | Volts RMS |
| 3.0 dB Limiting ($f_O$ = 5.5 MHz, Δf = 50 kHz, Q = 45) | — | 30 | 60 | μVRMS |
| 3.0 dB Limiting ($f_O$ = 10.7 MHz, Δf = 75 kHz, Q = 35) | — | 40 | — | μVRMS |
| A.M. Rejection ($f_O$ = 5.5 MHz, RF Input: 500 μV) | 45 | — | — | dB |
| A.M. Rejection ($f_O$ = 10.7 MHz, RF Input: 500 μV) | 40 | — | — | dB |
| Volume Control Range | 65 | 75 | — | dB |
| Output Impedance | — | 2.6 | — | kΩ |

**ELECTRICAL CHARACTERISTICS OF AUXILIARY Z DIODE AND TRANSISTOR Q45** ($T_A$ = +25°)

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Z-Voltage @ 5.0 mA (Pin 12) | 11.2 | — | 13.2 | Volts |
| Z-Resistance (Pin 12) @ 1.0 kHz, 5.0 mA | — | 15 | — | Ω |
| Q45 Breakdown Voltage $V_{CEO}$ | 13 | — | — | Volts |
| Q45 Current Gain @ $I_C$ = 1.0 mA, $V_{CE}$ = 5.0 V | 40 | 100 | — | — |

FIGURE 1 — TEST CIRCUIT


0.01
0.01
L
100
VCC
+
10 μF
C1
C2
2
7
9
11
13
2.2 μF
+
50
TBA120C
8
Input
Output
14
1
5
0.01
20 k

**COMPONENT VALUES:**

| | L | $C_1$ | Q |
|---|---|---|---|
| 5.5 MHz | 0.55 μH | 1.5 nF | 45 |
| 6.0 MHz | 0.55 μH | 1.2 nF | 45 |
| 10.7 MHz | 2.2 μH | 100 pF | 35 |

C2 = 0.022 μF, together with the integrated resistor of 2.6 kΩ (Pin 8) gives the deemphasis and can be reduced if required. For stereo 470 pF should be used to provide H.F. decoupling.

FIGURE 2 — AUDIO OUTPUT AND S/N versus INPUT SIGNAL LEVEL AT 5.5 AND 6.0 MHz

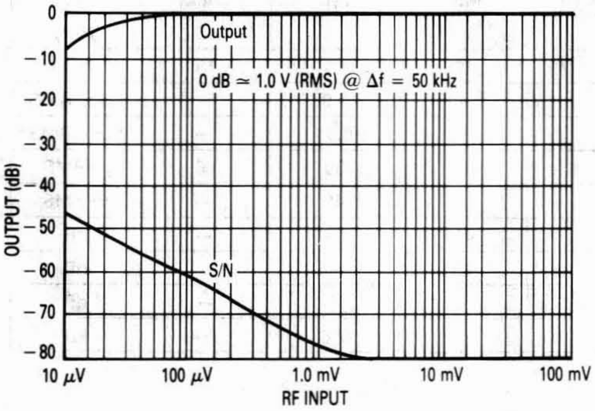


FIGURE 3 — AUDIO OUTPUT AND S/N versus INPUT SIGNAL LEVEL AT 10.7 MHz

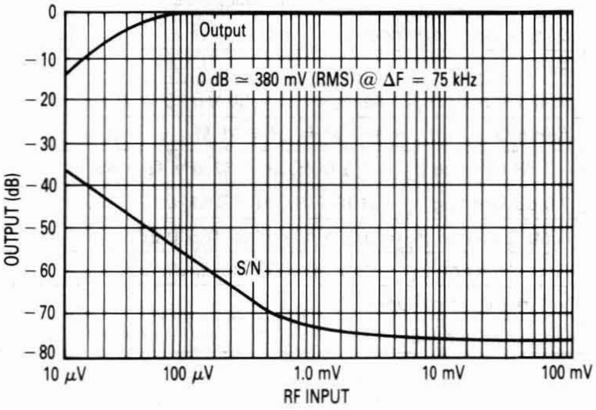


FIGURE 4 — A.M. REJECTION versus INPUT SIGNAL LEVEL AT 5.5 AND 6.0 MHz (30% A.M., 50 kHz F.M.)

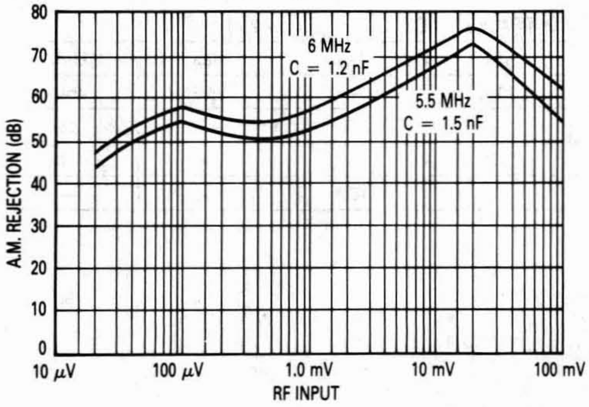


FIGURE 5 — A.M. REJECTION versus INPUT SIGNAL LEVEL AT 10.7 MHz (30% A.M., 75 kHz FM)

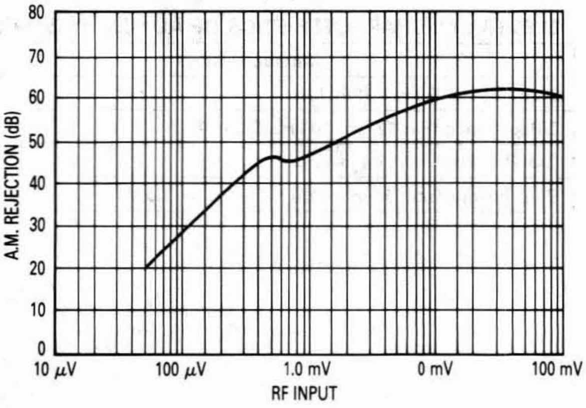


FIGURE 6 — OUTPUT VOLTAGE versus SUPPLY VOLTAGE

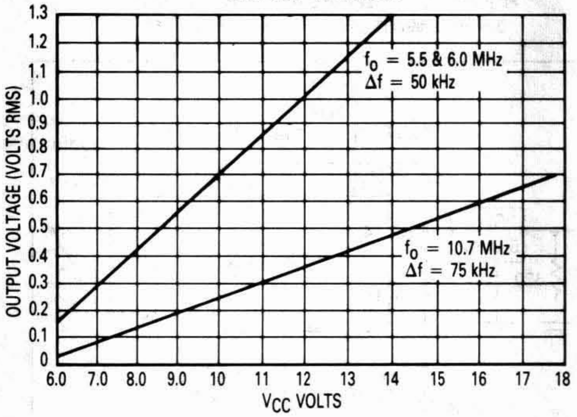


FIGURE 7 — T.H.D. + NOISE versus ATTENUATION (D.C. VOLUME CONTROL)

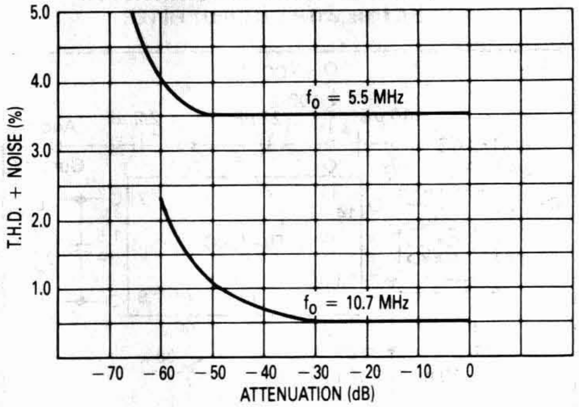


FIGURE 8 — OUTPUT SIGNAL ATTENUATION versus VOLUME CONTROL RESISTANCE

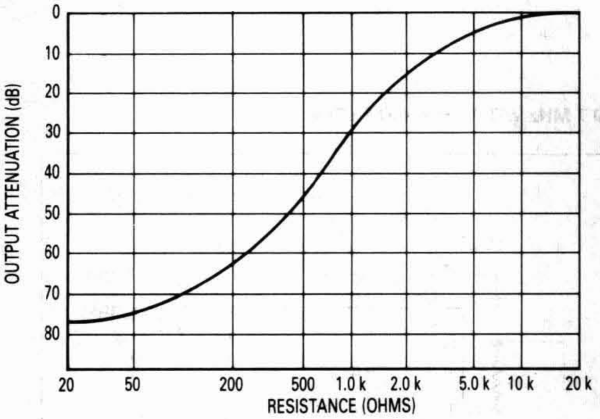


FIGURE 9 — OUTPUT SIGNAL ATTENUATION versus D.C. VOLTAGE AT PIN 5

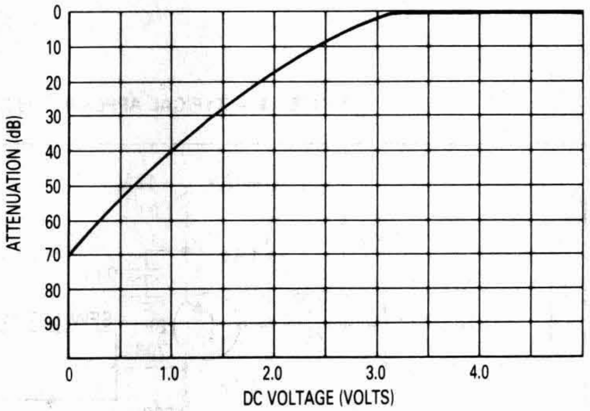


FIGURE 10 — AUDIO PREAMPLIFIER TEST CIRCUIT

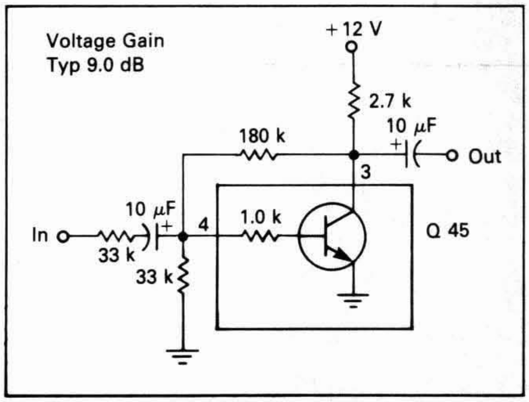

Voltage Gain
Typ 9.0 dB
+12 V
2.7 k
180 k
10 µF
+
Out
3
10 µF
+
In
33 k
4
1.0 k
Q 45
33 k

FIGURE 11 — T.H.D. versus OUTPUT VOLTAGE FOR AUDIO PREAMPLIFIER SHOWN IN FIGURE 10

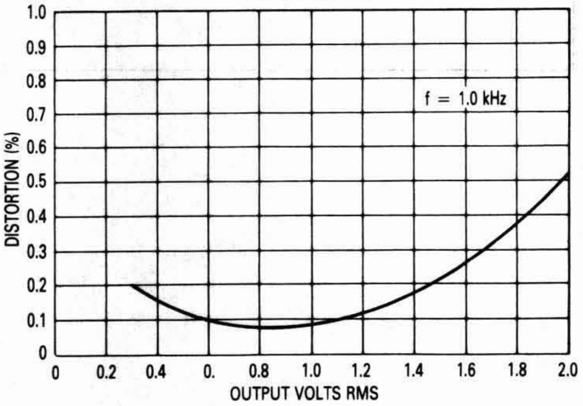


FIGURE 12 — TYPICAL APPLICATION FOR 5.5 MHz WITH L-C INPUT FILTER

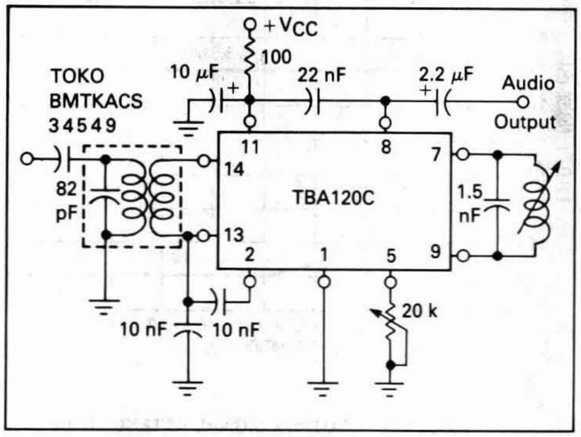

+VCC
100
TOKO
BMTKACS
34549
10 μF
22 nF
2.2 μF
Audio
Output
82
pF
TBA120C
11
8
7
14
13
2
1
5
9
1.5
nF
20 k
10 nF
10 nF

FIGURE 13 — TYPICAL APPLICATION FOR 5.5 MHz WITH CERAMIC INPUT FILTER

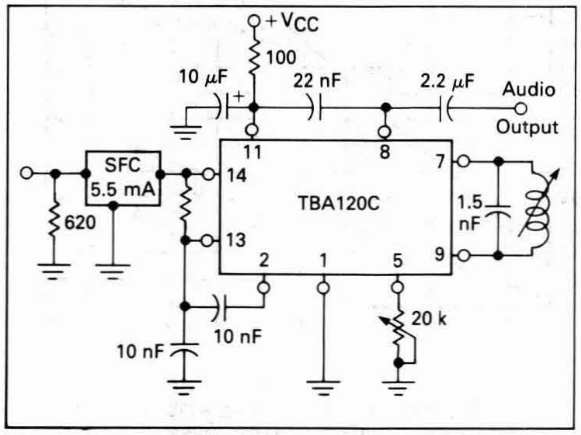
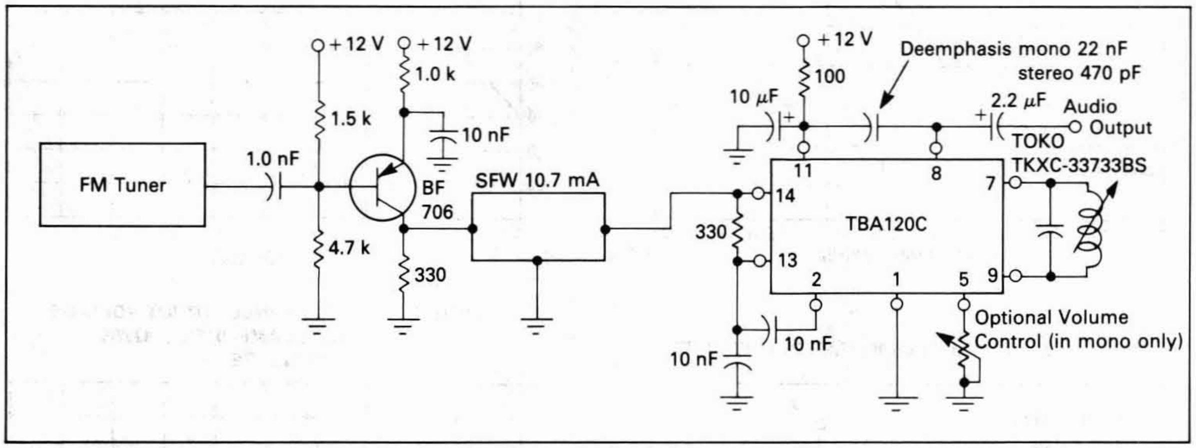

+VCC
100
10 μF
22 nF
2.2 μF
Audio
Output
SFC
5.5 mA
620
TBA120C
11
8
7
14
13
2
1
5
9
1.5
nF
20 k
10 nF
10 nF

FIGURE 14 — TYPICAL APPLICATION FOR 10.7 MHz WITH CERAMIC FILTER


+12 V
+12 V
1.0 k
1.5 k
10 nF
FM Tuner
1.0 nF
BF
706
SFW 10.7 mA
4.7 k
330
+12 V
100
Deemphasis mono 22 nF
stereo 470 pF
10 μF
2.2 μF
Audio
Output
TOKO
TKXC-33733BS
TBA120C
11
8
7
14
13
2
1
5
9
330
10 nF
10 nF
Optional Volume
Control (in mono only)

**MOTOROLA**

# TCA4500A

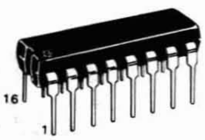
## Advance Information

### FM STEREO DEMODULATOR DESIGNED FOR USE IN HI-FI STEREO RECEIVERS AND CAR RADIOS

- Wide Supply Range: 8 – 16 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range (Fixed or Adjustable)
- Variable Blend Control
- Low Distortion: 0.3% THD at 2.5 Vp-p Composite Input Signal
- Excellent Rejection of ARI Subcarrier (57 kHz)
- Excellent Rejection of Pilot Tone Harmonics including 114 kHz
- Wide Dynamic Range: 0.5 – 2.5 Vp-p Composite Input Signal
- Up to 6 dB Gain (Monaural)
- Low Output Impedance
- Transient-free Mono/Stereo Switching
- 50 dB Supply Ripple Rejection
- Integrated Stereo/Monaural Switch – 100 mA Lamp Driving Capability
- Requires No Inductors

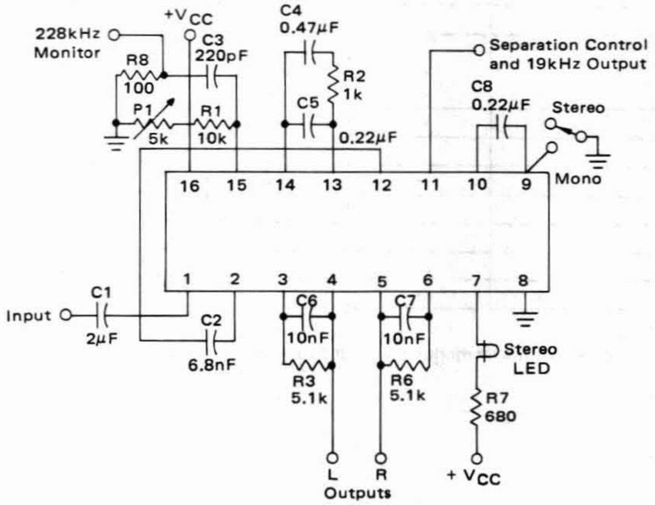
## FM STEREO DEMODULATOR

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



PLASTIC PACKAGE
CASE 648-05

FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT


228kHz Monitor
+VCC
C3 220pF
R8 100
P1 5k
R1 10k
C4 0.47μF
R2 1k
C5 0.22μF
Separation Control and 19kHz Output
C8 0.22μF
Stereo
Mono
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
Input
C1 2μF
C2 6.8nF
C6 10nF
R3 5.1k
C7 10nF
R6 5.1k
Stereo LED
R7 680
L
R
Outputs
+ VCC

**PIN FUNCTIONS**

1 – Input
2 – Preamplifier output
3 – Left amplifier input
4 – Left channel output
5 – Right channel output
6 – Right amplifier input
7 – Stereo indicator Lamp
8 – Ground
9 – Stereo switch filter
10 – Stereo switch filter
11 – 19 kHz output/blend
12 – Modulator input
13 – Loop filter
14 – Loop filter
15 – Oscillator RC network
16 – $V_{CC}$

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise noted)

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage | 16 | Volts |
| Power Dissipation (Package limitation) | 1800 | mW |
| Derate above $T_A$ = +25°C | 15 | mW/°C |
| Operating Temperature Range (Ambient) | −40 to +85 | °C |
| Storage Temperature Range | −65 to +150 | °C |
| Lamp Drive Voltage (Max. voltage at Pin 7 with lamp "off") | 30 | Volts |
| Lamp Current | 100 | mA |
| Blend Control Input Voltage (Pin 11) | 10 | Volts |

**ELECTRICAL CHARACTERISTICS** Unless otherwise noted: $V_{CC}$ = +12 Vdc, $T_A$ = 25°C, 2.5 Vp-p standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 10% pilot level, using circuit of Figure 1.

| Characteristic | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Stereo Channel Separation: Unadjusted | 30 | – | – | dB |
| Optimised on other channel[1] | 40 | – | – | |
| Monaural Voltage Gain[1] | 0.8 | 1.0 | 1.2 | |
| THD at 2.5 Vp-p Composite Input Signal | – | – | 0.3 | % |
| at 1.5 Vp-p Composite Input Signal | – | 0.2 | – | |
| Signal/Noise Ratio<br>RMS 20 Hz - 15 kHz | – | 90 | – | dB |
| Ultrasonic Frequency Rejection 19 kHz | – | 31 | – | dB |
| 38 kHz | – | 50 | – | |
| Stereo Switch Level (19 kHz input level for lamp "on") | 12 | 16 | 20 | mVrms |
| Hysteresis | – | 6.0 | – | dB |
| Quiescent Output Voltage Change with Mono/Stereo Switching | – | 5.0 | 20 | mVdc |
| Stereo Blend Control Voltage (Pin 11) 3 dB Separation | – | 0.7 | – | V |
| (see Figure 2) 30 dB Separation | – | 1.7 | – | V |
| Minimum Separation (Pin 11 at 0 V) | – | – | 1.0 | dB |
| Monaural Channel Imbalance (pilot tone off) | – | – | 0.3 | dB |
| ARI 57 kHz Pilot Tone Influence on THD[2] | – | – | 0.5 | % |
| Sub-carrier Harmonic Rejection 76 kHz | – | 45 | – | dB |
| 114 kHz | – | 50 | – | |
| 152 kHz | – | 50 | – | |
| Supply Ripple Rejection | – | 50 | – | dB |
| Input Impedance | – | 50 | – | KΩ |
| Output Impedance | – | 100 | – | Ω |
| Blend Control Current[1] | – | – | -300 | μA |
| Capture Range | – | ±5.0 | – | % |
| Operating Supply Voltage | 8.0 | – | 16 | V |
| Current Drain (lamp off) | – | 35 | – | mA |

Notes: [1] See Applications Information and Circuit Description

[2] ARI Test – Input signal: 1.5 Vp-p standard composite signal, 1 kHz modulation added to a CW 50 mVrms signal at 57.3 kHz.

## TYPICAL CHARACTERISTICS

Unless otherwise noted $V_{CC}$ = +12 V, $T_A$ = +25°C, Input Signal is Modulated L or R with 10% Pilot Level. (See Fig. 16.)

——— : High Loop Gain Circuit

– – – : Normal Circuit

**FIGURE 2 – CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL**

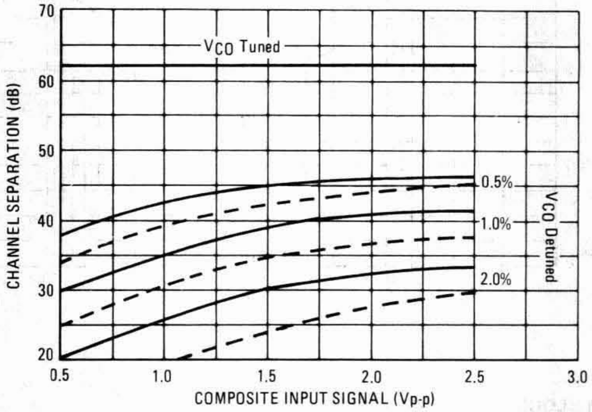


**FIGURE 3 – VCO FREE-RUNNING FREQUENCY versus TEMPERATURE**

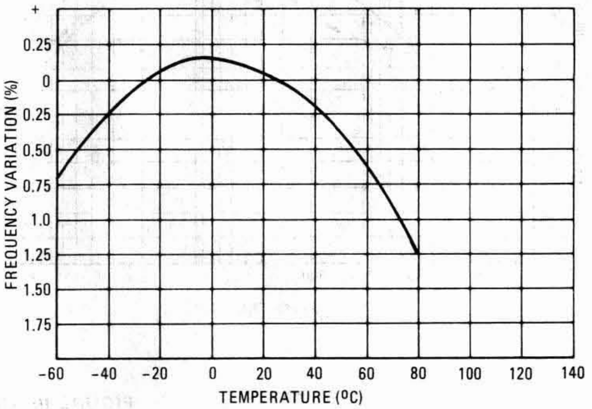


**FIGURE 4 – STEREO SWITCH LEVEL versus VCO FREE-RUNNING FREQUENCY**

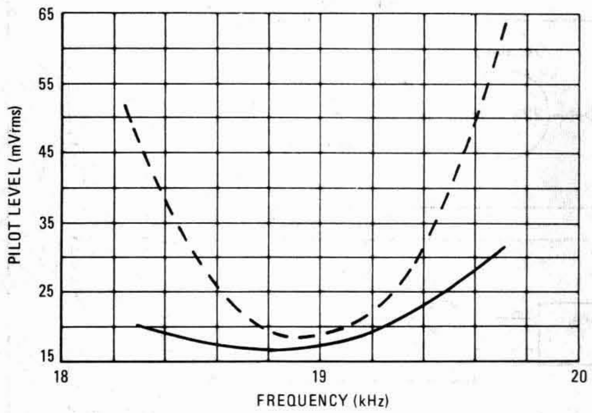


**FIGURE 5 – SUPPLY RIPPLE REJECTION versus SUPPLY VOLTAGE**

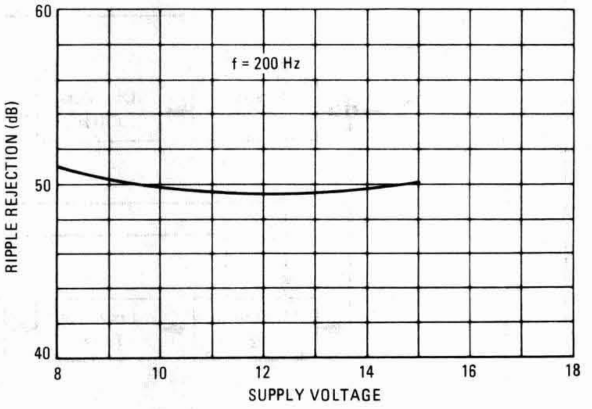


**FIGURE 6 – THD versus COMPOSITE INPUT LEVEL**

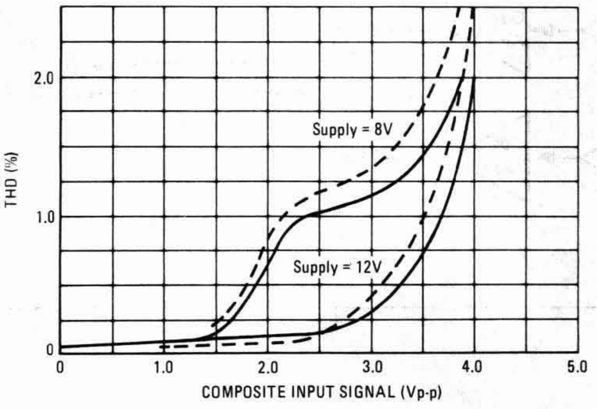
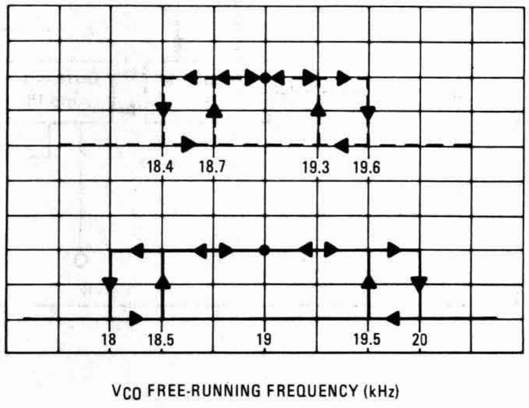


**FIGURE 7 – CAPTURE and HOLDING RANGE WITH 20 mV PILOT LEVEL**



6

**FIGURE 8 – CHANNEL SEPARATION versus FREQUENCY**

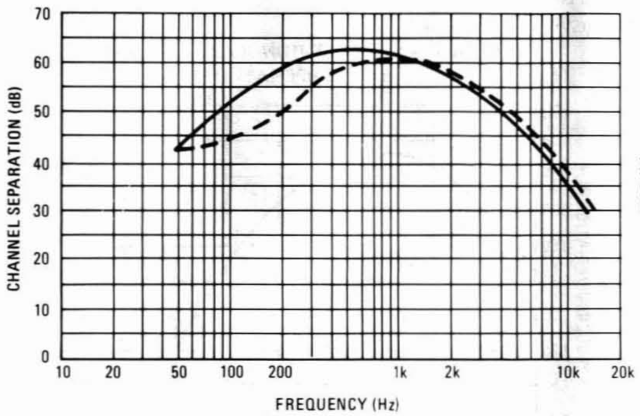


**FIGURE 9 – THD versus FREQUENCY**

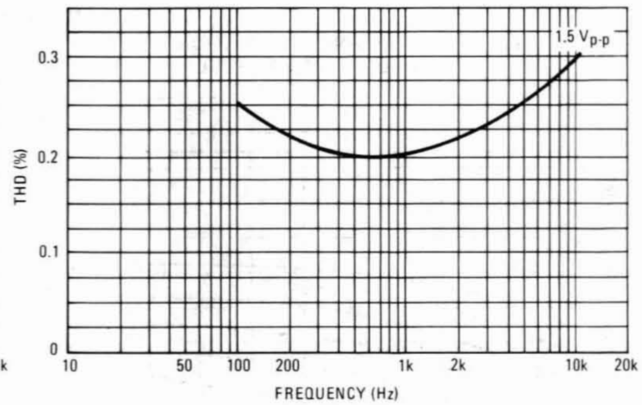
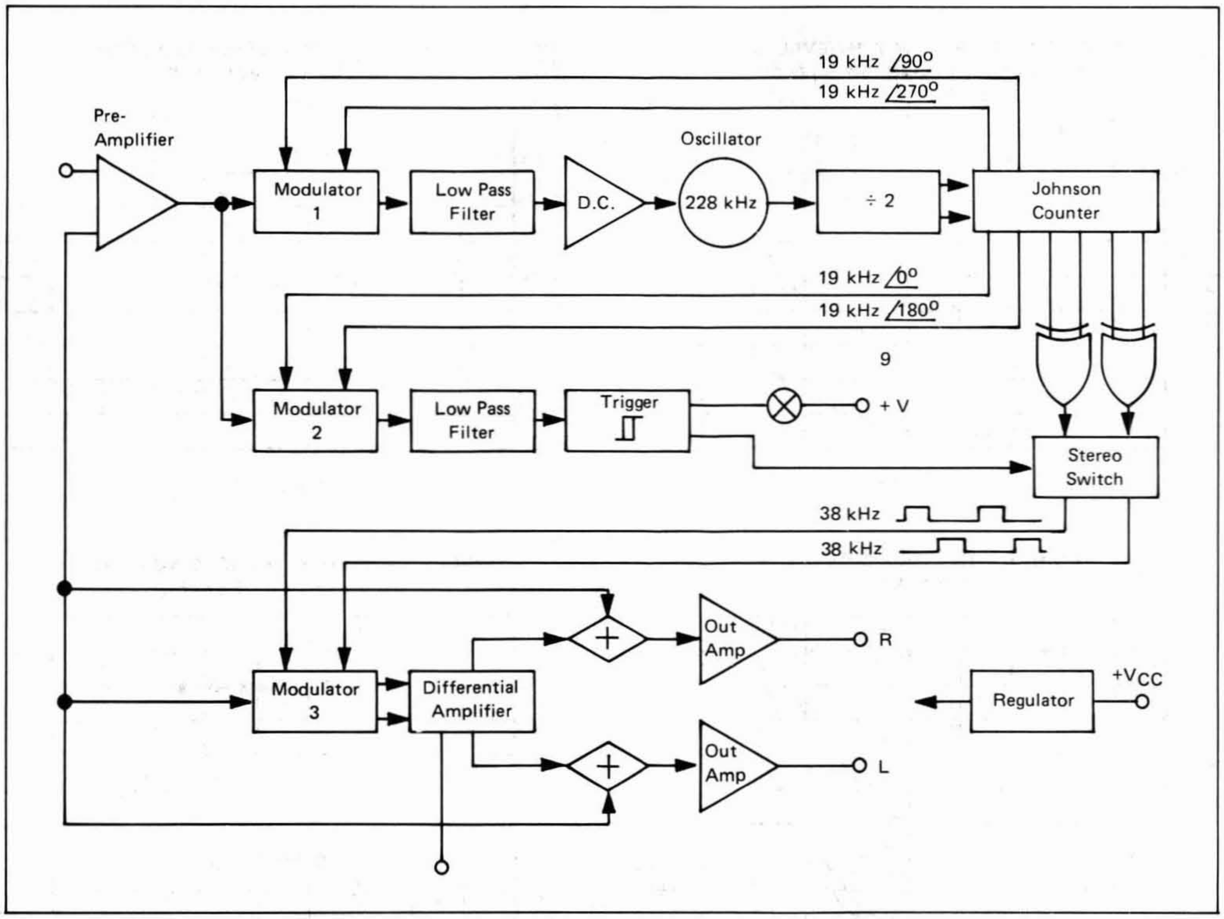


**FIGURE 10 – SYSTEM BLOCK DIAGRAM**


19 kHz ∠90°
19 kHz ∠270°
Pre-Amplifier
Modulator 1
Low Pass Filter
D.C.
Oscillator
228 kHz
÷ 2
Johnson Counter
19 kHz ∠0°
19 kHz ∠180°
9
Modulator 2
Low Pass Filter
Trigger
+ V
Stereo Switch
38 kHz
38 kHz
+
Out Amp
R
+$V_{CC}$
Modulator 3
Differential Amplifier
Regulator
+
Out Amp
L

## CIRCUIT DESCRIPTION

### INTRODUCTION

The TCA4500A is a phase-lock-loop stereo decoder which incorporates a variable separation control, and in which sensitivity to the third harmonics of both the pilot and sub-carrier frequencies has been eliminated by the use of appropriate, digitally generated, waveforms in the phase-lock-loop and decoder sections.

The variable separation control may be operated manually, or by a receiver's AGC or S meter signals, to provide smooth transitions between monaural and stereo reception. It operates only during stereo reception: the circuit switches automatically to monaural if the 19 kHz pilot tone is absent.

The elimination of sensitivity to the third harmonic (114 kHz) of the sub-carrier (38 kHz) excludes interference from the 100 kHz (European Spacing) spaced side bands of adjacent transmitters, while elimination of sensitivity to the third harmonic (57 kHz) of the pilot tone (19 kHz) excludes interference from the ARI* system employed in Europe.

*Auto Radio Information.

### CIRCUIT OPERATION

The block diagram of the circuit, shown in Fig. 10, consists of three sections: the phase-lock-loop, including the digital waveform generator: the stereo switch: and the decoder, in which the composite stereo signal is demodulated and matrixed to separate L and R channels.

In the phase-lock-loop the internal RC oscillator, operating at 228 kHz, feeds a 3 stage Johnson counter, via a binary divider, to generate a series of 19 kHz square waves. By the use of suitably connected NAND and EXCLUSIVE OR gates, the waveforms shown in Fig. 11, which are used to drive the various modulators in the circuit, are developed.

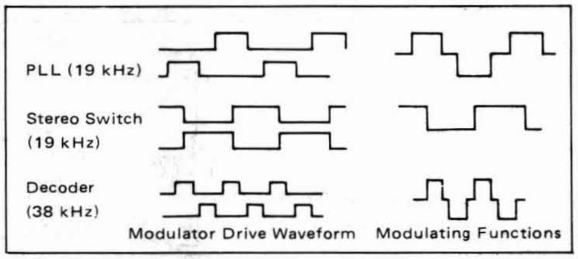
The use of such drive waveforms produces the modulating functions also shown in Fig. 11. The usual square-waveforms have been replaced in the PLL and decoder sections by 3-level forms which contain no third harmonic (actually no harmonics which are multiples of 2 or 3 are present). This eliminates the frequency translation of interference from these bands into the low frequency region. Such translation may produce audible components in the decoder section from the sidebands of adjacent channel FM signals, and may produce phase jitter, and consequent intermodulation distortion, in the PLL, from the modulated 57 kHz tones of the ARI system. The TCA 4500A is inherently free from these effects.

The stereo switch section is of conventional form (e.g. MC1310).

The decoder section consists of a modulator (driven by the waveforms shown in Fig. 11) whose outputs are the inverted and non-inverted channel difference signals. These signals pass to the output amplifiers via the variable blend circuit in which they are partially combined , and hence mutually attenuated, according to the control voltage applied.

Matrixing occurs at the inputs of the output amplifiers, where the unmodified composite signal is added to the blended channel difference signals. The stereo separation may be progressively reduced from maximum to zero, dependent on the blending. The control law has been made non-linear, as the major redistribution of sound energy occurs at very low separation levels. For monaural, or very weak stereo signals, the modulator in the decoder section is disactivated by the stereo switch circuit. The variable separation control is thus, also, automatically disabled.

FIGURE 11 – DIGITAL WAVEFORM



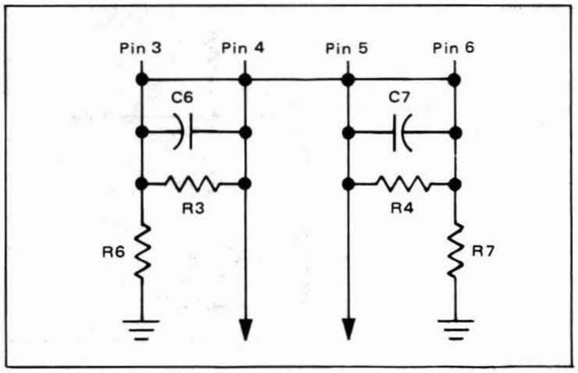
## APPLICATION INFORMATION

### GAIN AND DE-EMPHASIS

The gain and de-emphasis characteristics of the circuit are defined by shunt feedback via the external RC networks (R3, C6, R4, C7 of Fig. 1) around the output amplifiers. The gain is unity when resistors of 5.1 kΩ are used. Higher gains may be obtained by using networks of the form shown in Fig. 12.

The resistors R6, R7 are added to correct the output quiescent voltage levels which are optimized for R3, R4 = 5.1 kΩ and which would, if uncorrected, become too low with higher value resistors. Suitable network values are as follows:

FIGURE 12 – OUTPUT AMPLIFIER FEEDBACK NETWORKS



## APPLICATION INFORMATION (continued)

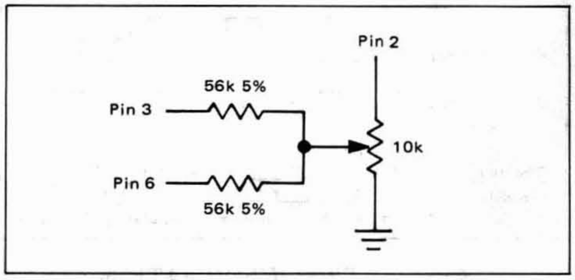
| Gain (dB) | R3, R4 | C6, C7 | | R6, R7 |
|---|---|---|---|---|
| | | 50 µs | 75 µs | |
| 0 | 5.1kΩ | 10 nF | 15 nF | |
| 3 | 6.8kΩ | 6.8 nF | 10 nF | 47k ±10% |
| 6 | 10k | 4.7 nF | 6.8 nF | 27k ±10% |

The maximum output level is 1 Vrms; consequently the max. input is limited to 1.4 Vp-p if the gain is set to 6 dB.

### SEPARATION ADJUSTMENT

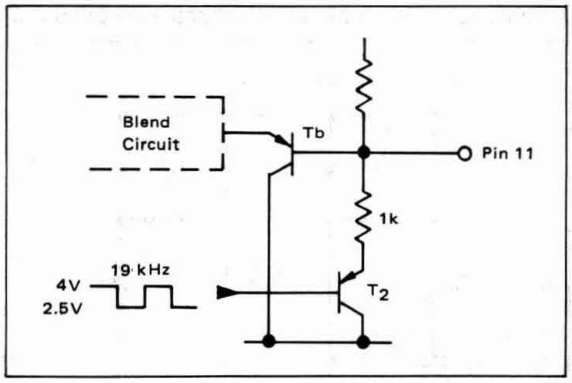
A separation adjustment may be added, as shown below, (Fig. 13), to compensate for the receiver's IF characteristics.

FIGURE 13 – NETWORK PROVIDING ADJUSTABLE SEPARATION



This network reduces the amplification of the channel sum signal in the decoder, to compensate the attenuation of the channel difference signal in the receiver's IF section. The network shown will compensate for up to 2 dB attenuation at 38 kHz. The decoder gain is, obviously, reduced by an amount equal to the compensation required. When used as described, the adjustment also corrects the inherent separation of the decoder, which may be optimized on one channel. Optimization of both channels is possible if separate potentiometers are used to feed each output amplifier.

FIGURE 14 – BLEND CONTROL INPUT CIRCUIT



### VARIABLE SEPARATION (BLEND) CONTROL AND 19 kHz OUTPUT

To retain the 16-pin package, the blend control has been combined with the 19 kHz output on pin 11. The internal circuit providing this combination is shown in Fig.14.

If pin 11 is left open-circuit, the 19 kHz signal appears at a mean dc level of 4 V. The blend circuit is inoperative at this level and the decoder provides full separation. The 19 kHz signal can be used to tune the internal oscillator.

To reduce the separation, the voltage on pin 11 is lowered. At 3.2 V, T2 ceases conduction and the 19 kHz signal disappears.

At 2.3 V, the blend circuit comes into operation and the separation decreases according to the curve shown in Fig. 15.

FIGURE 15 – SEPARATION CONTROL VOLTAGE

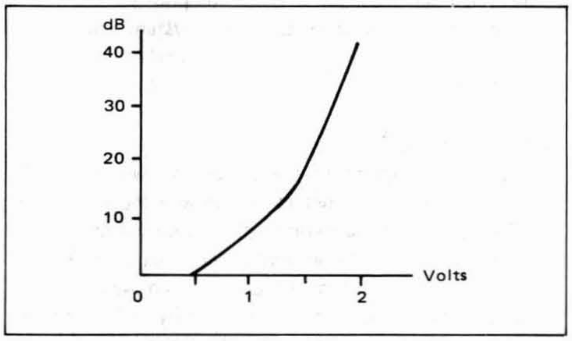
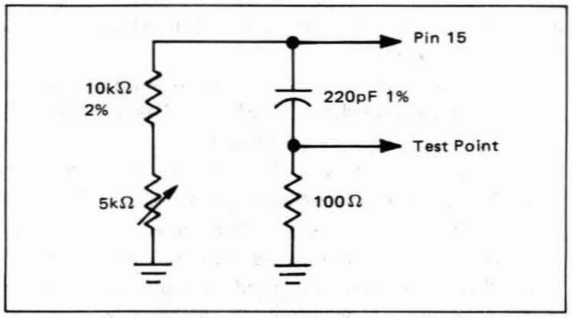


FIGURE 16 – OSCILLATOR NETWORK FOR DIRECT FREQUENCY MEASUREMENT



### OSCILLATOR TUNING

If the variable separation facility is not required, pin 11 is left open-circuit and the 19 kHz signal which then appears may be used to indicate the oscillator frequency. If the variable separation is used, and the drive circuit prevents access to the 19 kHz signal, then the oscillator frequency must be measured directly. A test point should be obtained by modifying the oscillator RC network as shown in Fig. 16.

The output is a pulse train of approximately 1.5 Volts amplitude. Connecting frequency counters of up to 300 pF input capacitance produces less than 0.3% change of the oscillator frequency, which should be set to 228 kHz.

**HIGH LOOP GAIN COMPONENTS**

For applications demanding operation under low pilot level (e.g., car radio) the following component changes to Fig. 1 are recommended.

R1 = 12k
R2 = 1.5k
R8 = 330
P1 = 10k

C3 = 150 pF
C4 = 330 nF
C5 = 150 nF

**EXTERNAL MONO-STEREO SWITCHING AND OSCILLATOR KILLING**

If required, the TCA 4500A can be forced into mono mode simply by grounding pin 9 (see Fig. 1). The 228 kHz oscillator will be automatically killed.

The conditions governing Mono/Stereo switching on pin 9 are the following:

- Quiescent voltage: +2.3 Vdc
- Current required to ensure mono operaton (with 100 mVrms pilot level): 10 $\mu$A (from pin 9 to ground) Hysteresis: 0.7$\mu$A
- Stereo/mono switching and oscillator killing: less than +500 mV
- Maximum stray capacitance between pin 9 and ground: 100 pF

**EXTERNAL COMPONENT FUNCTIONS**

P1 – 19 kHz frequency adjustment
P2 – channel separation adjustment and compensation for IF roll-off.
R3, R6 – gain fixing resistors. The values shown in the schematic are for unity gain.
C6, C7 – de-emphasis capacitors. Value to give: RC = 50 $\mu$s.

Values shown in Fig. 1 are recommended for applications with input level higher than 1.0 Vrms.

**MOTOROLA**

# TCA5550

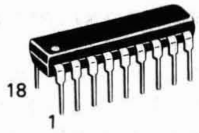
## STEREO SOUND CONTROL SYSTEM

The TCA5550 is a single chip stereo balance, volume, bass and treble control circuit designed for use in car radios, TV, and audio systems. Simple dc inputs allow the control to be effected by four inexpensive potentiometers or a remote control system. The bass and treble responses are defined by a single capacitor per control per channel.

- Four High Impedance dc Controls — Vol, Bass, Treble, Balance
- A Single External Capacitor Defines Each Tone Control Characteristic
- Low Distortion, 0.1% at Nominal Input Level, Unity Gain with the Tone Controls Flat
- Channel Separation Better Than 45 dB
- Wide Power Supply Tolerance, 10 to 16 Vdc
- ± 14 dB of Tone Control
- More Than 75 dB of Volume Control
- Wide Dynamic Range: 100 mV to 500 $mV_{rms}$ Input Signal
- Low Output Impedance

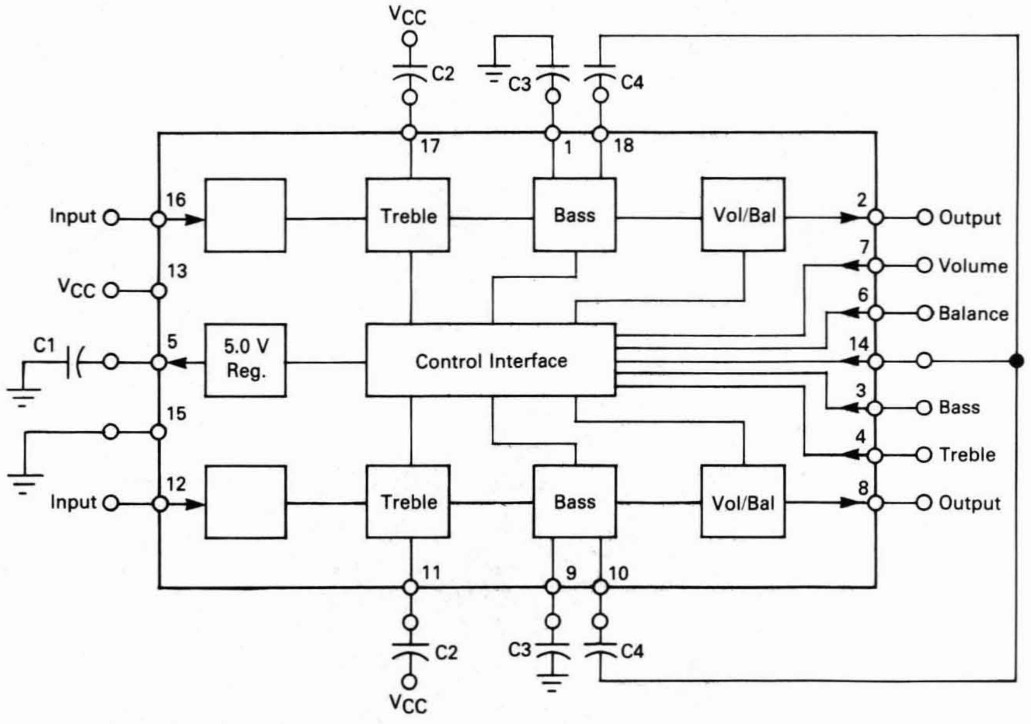
## STEREO SOUND CONTROL SYSTEM

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 707-02

**FIGURE 1 — BLOCK DIAGRAM**


VCC
C2
C3
C4
17
1
18
Input
16
Treble
Bass
Vol/Bal
2
Output
7
Volume
6
Balance
13
VCC
C1
5
5.0 V Reg.
Control Interface
14
3
Bass
15
4
Treble
Input
12
Treble
Bass
Vol/Bal
8
Output
11
9
10
C2
C3
C4
VCC

**MAXIMUM RATINGS** ($T_A = +25°C$)

| Rating | Value | Unit |
|---|---|---|
| Power Supply Voltage | 18 | Volts |
| Power Dissipation (Package Limitation) | 1250 | mW |
| Derate above $T_A = +25°C$ | 10 | mW/°C |
| Operating Temperature Range (Ambient) | −40 to +85 | °C |
| Storage Temperature Range | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A = 25°C$, $V_{CC} = 12$ Vdc)

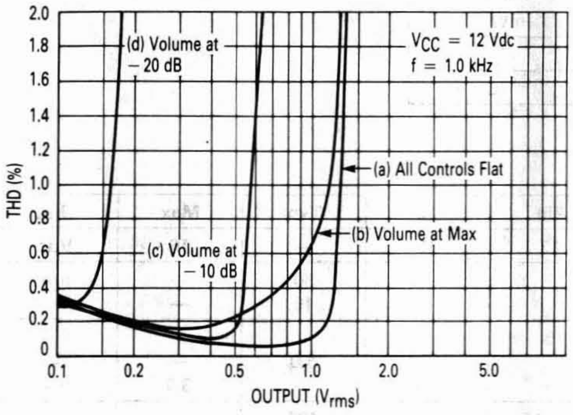
| Characteristic | | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | | 13 | 10 | — | 16 | Vdc |
| Supply Current | Min Gain | | — | 30 | — | mA |
| | Max Gain | | — | 15 | — | |
| Regulated Output | | 5 | | | | |
| Voltage[1] | | | — | 5.0 | — | V |
| Current | | | — | — | 3.0 | mA |
| Input Levels | Max Gain | 12, 16 | — | 100 | — | $mV_{rms}$ |
| | With Reduced Gain[3] | | — | — | 500 | |
| Input Impedance | | 12, 16 | — | 100 | — | kΩ |
| Output Impedance | | 2, 8 | — | 300 | — | Ω |
| Tone Control Range (at 70 Hz & 10 kHz)[2] | | 3,4 | | | | dB |
| With Pins 3 & 4 @ 0.5 V | | | — | −14 | — | |
| With Pins 3 & 4 @ 2.3 V | | | — | 0 | — | |
| With Pins 3 & 4 @ 4.1 V | | | — | +14 | — | |
| Balance Control Range | Min Gain | 6 | — | −35 | — | dB |
| (Constant Power Law) | Max Gain | | — | +3.0 | — | dB |
| Voltage on Pin 6 for Balanced Gain | | | — | 2.3 | — | V |
| Volume Control Range | | 7 | — | 80 | — | dB |
| With Pin 7 @ 0 V | | | — | +10 | — | |
| With Pin 7 @ 3.1 V | | | — | −20 | — | |
| With Pin 7 @ $V_{PIN\ 5}$ | | | — | −70 | — | |
| Control Input Currents | | 3, 4, 6, 7 | — | — | ±1.0 | µA |
| Channel Separation | | | 45 | — | — | dB |
| Distortion (at 1.0 kHz) at 300 $mV_{rms}$ Output[3] | | | — | 0.1 | — | % |
| Signal : Noise Ratio<br>50 Hz to 15 kHz, 10 dB Gain, Tone Controls Flat | | | — | 70 | — | dB |
| Noise Level<br>50 Hz to 15 kHz, Min Gain | | | — | 50 | — | $\mu V_{rms}$ |

**NOTES:**

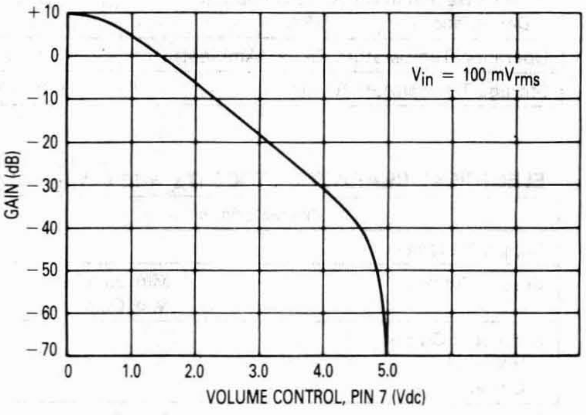
1. The control potentiometers to this point, see Figure 7.
2. These figures are functions of the capacitors on Pins 1, 9, 10, 11, 17 & 18. See the application diagram, Figure 7.
3. The input level may be increased to 500 $mV_{rms}$ but the user controls must be adjusted to ensure that the output level does not exceed 300 $mV_{rms}$.

## PERFORMANCE CHARACTERISTICS, FIGURES 2–7, TAKEN IN CIRCUIT OF FIGURE 8, $V_{CC}$ = 12 V

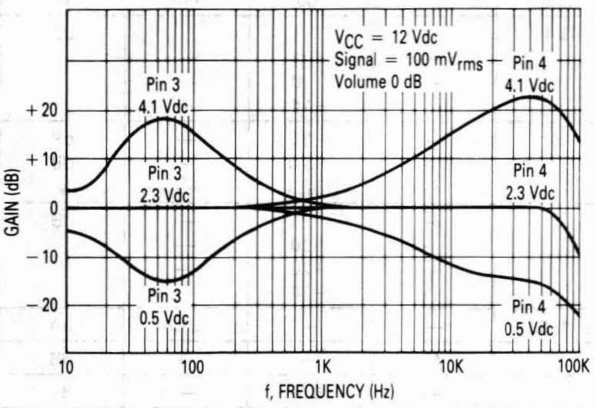
### FIGURE 2 — MIDBAND DISTORTION



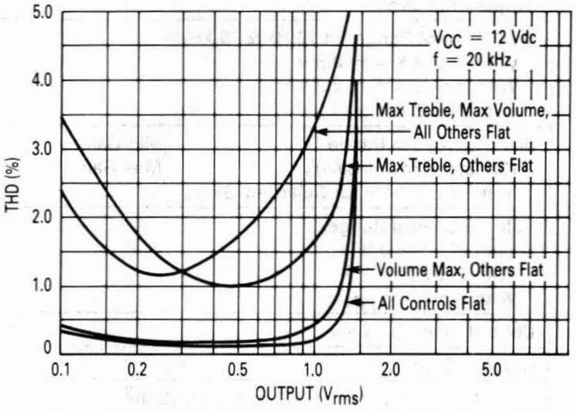
### FIGURE 3 — VOLUME CONTROL CHARACTERISTICS



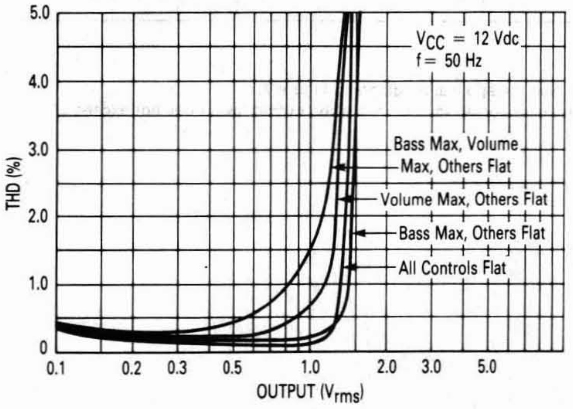
### FIGURE 4 — TONE CONTROL CHARACTERISTICS



### FIGURE 5 — HIGH FREQUENCY DISTORTION



### FIGURE 6 — LOW FREQUENCY DISTORTION



### FIGURE 7 — BALANCE CONTROL CHARACTERISTIC

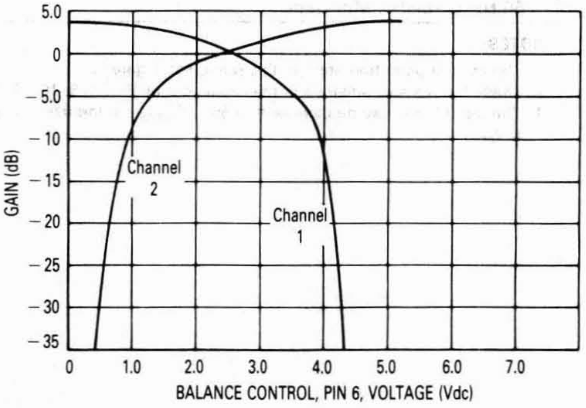
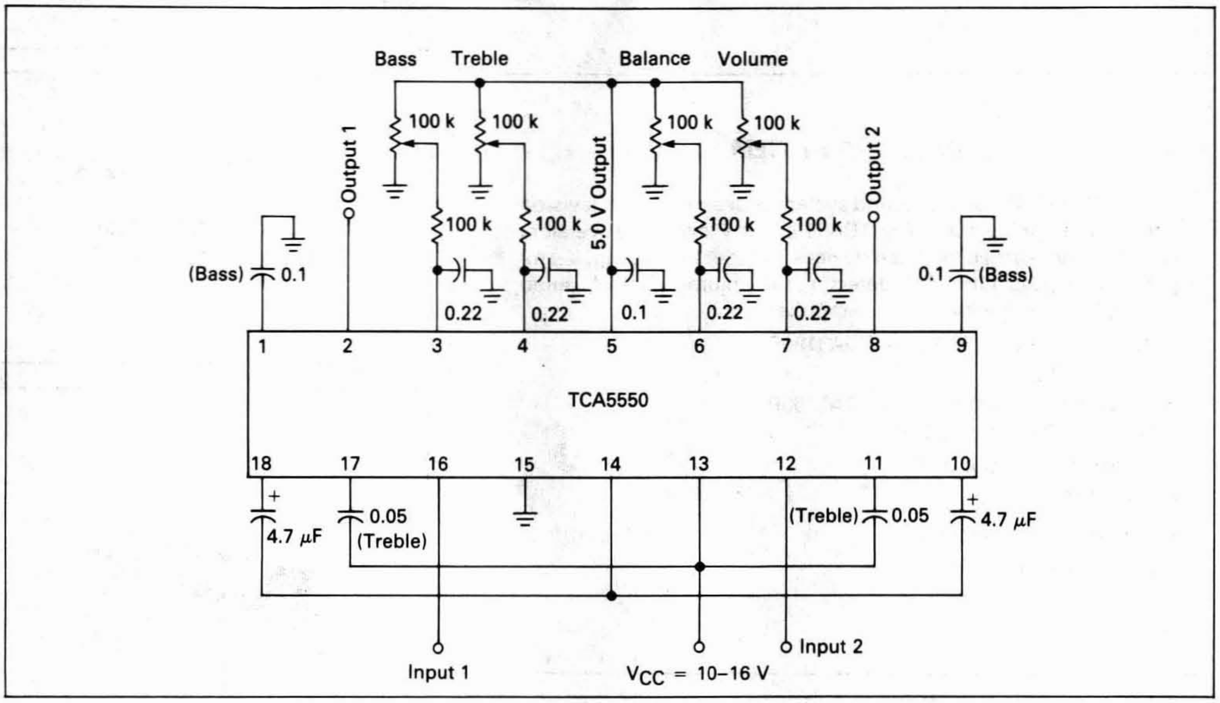


**FIGURE 8 — APPLICATION CIRCUIT**


Bass
Treble
Balance
Volume
100 k
100 k
100 k
100 k
Output 1
5.0 V Output
Output 2
100 k
100 k
100 k
100 k
(Bass)
0.1
0.22
0.22
0.1
0.22
0.22
0.1
(Bass)
1
2
3
4
5
6
7
8
9
TCA5550
18
17
16
15
14
13
12
11
10
+
4.7 μF
0.05
(Treble)
(Treble)
0.05
+
4.7 μF
Input 1
VCC = 10–16 V
Input 2

**MOTOROLA**

# TDA1190P
# TDA3190P

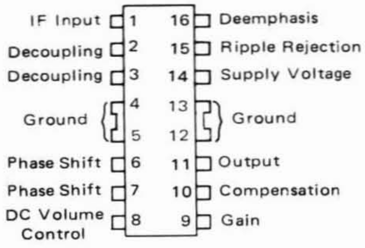
## TV SOUND SYSTEM

The TDA3190P 4.2-watt sound system is designed for television and related applications. The TDA1190P is a low-power version. Functions performed by these devices include: IF Limiting, IF amplifier, low pass filter, FM detector, DC volume control, audio preamplifier, and audio power amplifier.

- 4.2 Watts Output Power — TDA3190P
  ($V_{CC}$ = 24 V, $R_L$ = 16 Ω)
- 1.3 Watts Output Power — TDA1190P
  ($V_{CC}$ = 18 V, $R_L$ = 32 Ω)
- Linear Volume Control
- High AM Rejection
- Low Harmonic Distortion
- High Sensitivity

## TV SOUND SYSTEM

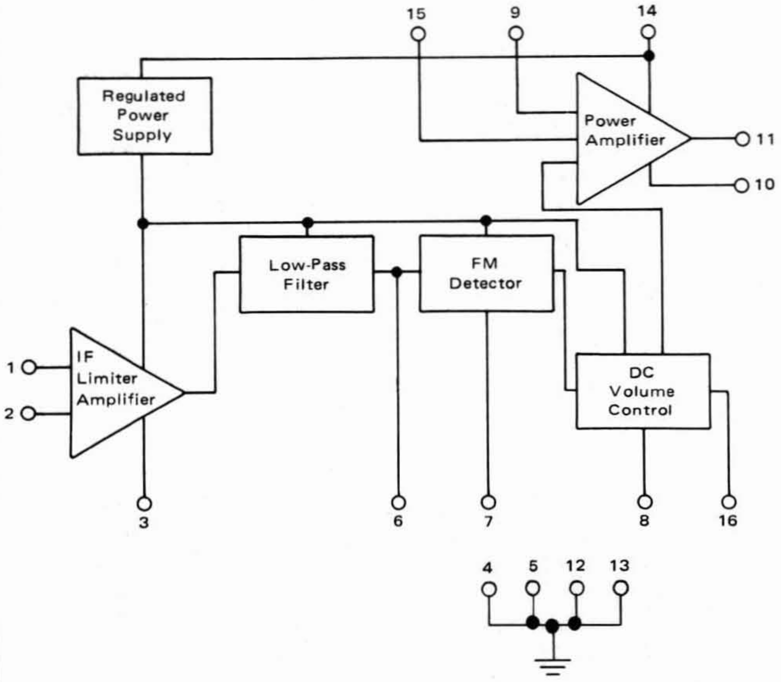
**SILICON MONOLITHIC**
**INTEGRATED CIRCUIT**



IF Input 1
Decoupling 2
Decoupling 3
Ground 4 5
Phase Shift 6
Phase Shift 7
DC Volume Control 8
16 Deemphasis
15 Ripple Rejection
14 Supply Voltage
13 12 Ground
11 Output
10 Compensation
9 Gain

**PLASTIC PACKAGE**
**CASE 648C-01**

### BLOCK DIAGRAM



15
9
14
Regulated Power Supply
Power Amplifier
11
10
Low-Pass Filter
FM Detector
IF Limiter Amplifier
1
2
DC Volume Control
3
6
7
8
16
4
5
12
13

### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| Both Devices | 0 to +75°C | Plastic |

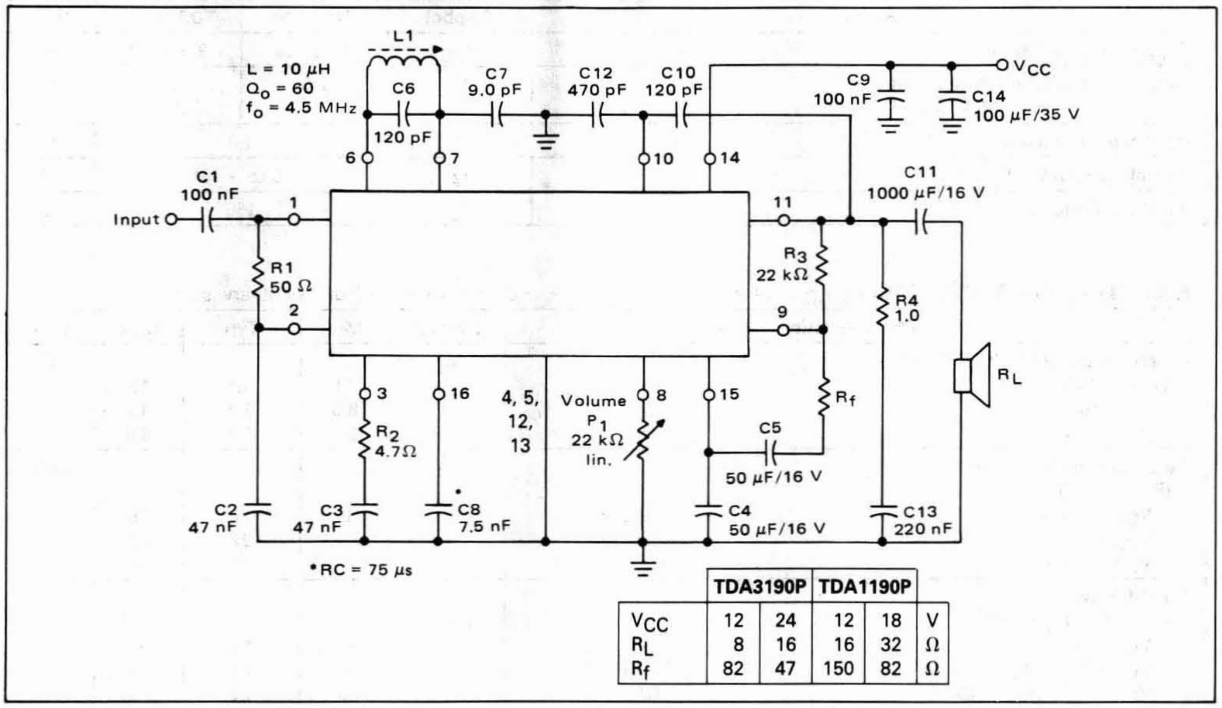
### MAXIMUM RATINGS

| Rating | Symbol | TDA3190P | TDA1190P | Unit |
|---|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | 9.0 to 28 | 9.0 to 22 | V |
| Output Peak Current (Nonrepetitive) | $I_o$ | 2.0 | 1.5 | A |
| (Repetitive) | | 1.5 | 1.0 | |
| Input Signal Voltage | $V_I$ | 1.0 | | V |
| Operating Temperature Range | $T_A$ | 0 to +75 | | °C |
| Junction Temperature | $T_J$ | 150 | | °C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 24 V, $f_o$ = 4.5 MHz, Δf = ±25 kHz, $T_A$ = 25°C unless otherwise noted.)

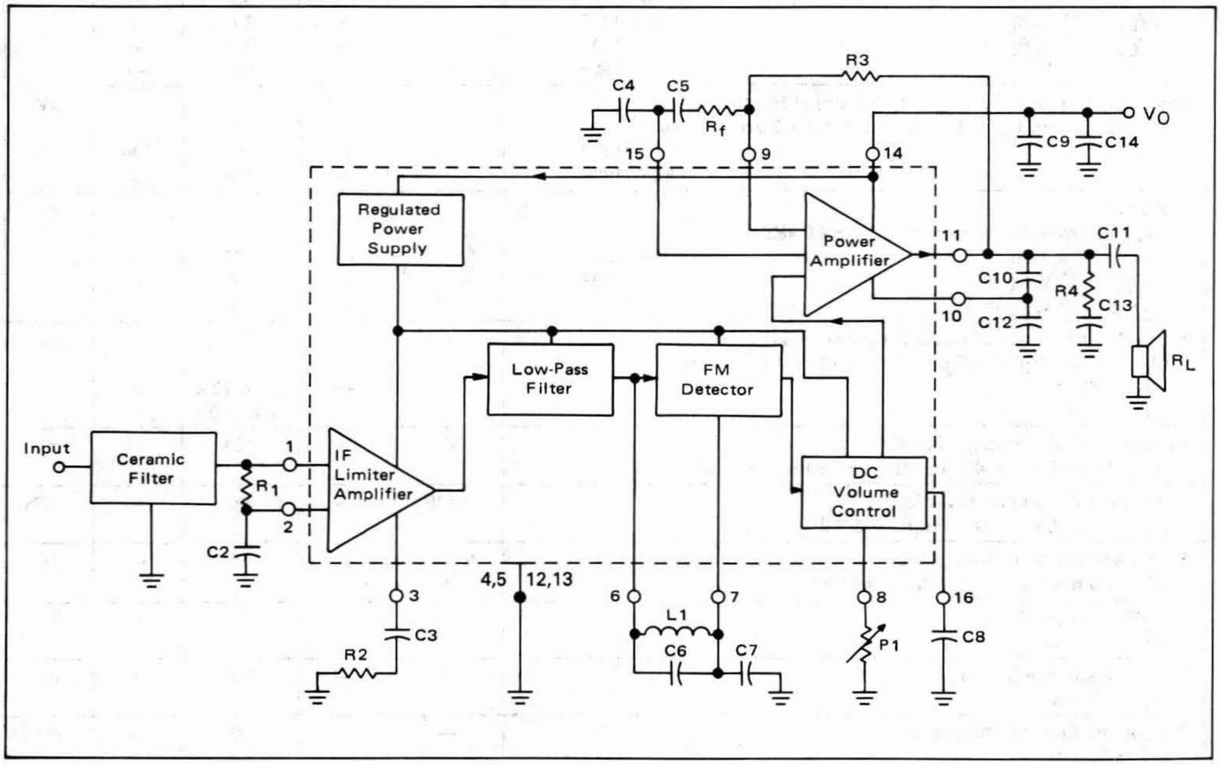
| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Quiescent Output Voltage (Pin 11) | | $V_O$ | | | | V |
| $V_{CC}$ = 24 V | TDA3190P | | 11 | 12 | 13 | |
| $V_{CC}$ = 18 V | TDA1190P | | 8.0 | 9.0 | 10 | |
| $V_{CC}$ = 12 V | Both | | 5.1 | 6.0 | 6.9 | |
| Quiescent Drain Current<br>(P1 = 22 kΩ) | | $I_D$ | | | | mA |
| $V_{CC}$ = 24 V | TDA3190P | | 11 | 22 | 35 | |
| $V_{CC}$ = 18 V | TDA1190P | | 11 | 22 | 35 | |
| $V_{CC}$ = 12 V | Both | | — | 19 | — | |
| Output Power<br>(d = 10%, $f_m$ = 400 Hz) | | $P_O$ | | | | W |
| $V_{CC}$ = 24 V, $R_L$ = 16 Ω | TDA3190P | | — | 4.2 | — | |
| $V_{CC}$ = 12 V, $R_L$ = 8.0 Ω | TDA3190P | | — | 1.5 | — | |
| $V_{CC}$ = 18 V, $R_L$ = 32 Ω | TDA1190P | | 1.0 | 1.3 | — | |
| $V_{CC}$ = 12 V, $R_L$ = 16 Ω | TDA1190P | | 0.7 | 0.9 | — | |
| (d = 2%, $f_m$ = 400 Hz) | | | | | | |
| $V_{CC}$ = 24 V, $R_L$ = 16 Ω | TDA3190P | | — | 3.5 | — | |
| $V_{CC}$ = 12 V, $R_L$ = 8.0 Ω | TDA3190P | | — | 1.4 | — | |
| $V_{CC}$ = 18 V, $R_L$ = 32 Ω | TDA1190P | | — | 1.0 | — | |
| $V_{CC}$ = 12 V, $R_L$ = 16 Ω | TDA1190P | | — | 0.7 | — | |
| Input Limiting Threshold Volts (−3.0 dB) at Pin 1<br>Δf = ±7.5 kHz, $f_m$ = 400 Hz, Set P1 for 2.0 Vrms on Pin 11 | | $V_I$ | | | | µV |
| | TDA3190P | | — | 40 | 100 | |
| | TDA1190P | | — | 60 | 100 | |
| Distortion<br>($P_O$ = 50 mW, $f_m$ = 400 Hz, Δf = ±7.5 kHz) | | | | | | % |
| $V_{CC}$ = 24 V, $R_L$ = 16 Ω | TDA3190P | | — | 0.75 | — | |
| $V_{CC}$ = 18 V, $R_L$ = 32 Ω | TDA1190P | | — | 1.0 | — | |
| $V_{CC}$ = 12 V, $R_L$ = 16 Ω | Both | | — | 1.0 | — | |
| Frequency Response of Audio Amplifier (−3.0 dB)<br>($R_L$ = 16 Ω, $C_{10}$ = 120 pF, $C_{12}$ = 470 pF, $P_1$ = 22 kΩ) | | B | | | | Hz |
| $R_f$ = 82 Ω | | | — | 70 to 12 k | — | |
| $R_f$ = 47 Ω | | | — | 70 to 7.0 k | — | |
| Recovered Audio Voltage (Pin 16)<br>($V_I \geq$ 1.0 mV, $f_m$ = 400 Hz, Δf = ±7.5 kHz, $P_1$ = 0) | | $V_o$ | — | 120 | — | mV |
| Amplitude Modulation Rejection<br>($V_I \geq$ 1.0 mV, $f_m$ = 400 Hz, m = 30%) | | AMR | — | 55 | — | dB |
| Signal and Noise to Noise Ratio<br>($V_I \geq$ 1.0 mV, $V_o$ = 4.0 V, $f_m$ = 400 Hz) | | $\frac{S+N}{N}$ | 50 | 65 | — | dB |
| Input Resistance (Pin 1)<br>($V_I$ = 1.0 mV) | | $r_i$ | — | 30 | — | kΩ |
| Input Capacitance (Pin 1)<br>($V_I$ = 1.0 mV) | | $C_i$ | — | 5.0 | — | pF |
| DC Volume Control Attenuation<br>(P1 = 12 kΩ) | | — | — | 90 | — | dB |

## TEST CIRCUIT


L1
L = 10 μH
$Q_o$ = 60
$f_o$ = 4.5 MHz
C6
120 pF
C7
9.0 pF
C12
470 pF
C10
120 pF
C9
100 nF
C14
100 μF/35 V
$V_{CC}$
C1
100 nF
Input
1
2
6
7
10
14
11
9
R1
50 Ω
C11
1000 μF/16 V
R3
22 kΩ
R4
1.0
$R_L$
$R_f$
3
16
4, 5, 12, 13
Volume
$P_1$
22 kΩ
lin.
8
15
C5
50 μF/16 V
$R_2$
4.7Ω
C2
47 nF
C3
47 nF
C8
7.5 nF
C4
50 μF/16 V
C13
220 nF
*RC = 75 μs

| | TDA3190P | | TDA1190P | | |
|---|---|---|---|---|---|
| $V_{CC}$ | 12 | 24 | 12 | 18 | V |
| $R_L$ | 8 | 16 | 16 | 32 | Ω |
| $R_f$ | 82 | 47 | 150 | 82 | Ω |

## TYPICAL CIRCUIT CONFIGURATION


R3
C4
C5
$R_f$
15
9
14
$V_O$
C9
C14
Regulated Power Supply
Power Amplifier
11
10
C11
C10
R4
C13
C12
$R_L$
Low-Pass Filter
FM Detector
Input
Ceramic Filter
$R_1$
1
2
C2
IF Limiter Amplifier
DC Volume Control
3
C3
R2
4,5
12,13
6
7
L1
C6
C7
8
P1
16
C8

**MOTOROLA**

# TDA3301
# TDA3303

## TV COLOR PROCESSOR

These devices will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube. The provision of high bandwidth on-screen display inputs makes them suitable for text display, TV games, cameras, etc. The TDA3301 differs from the TDA3303 in its user control laws, and also a phase shift control which operates in PAL, as well as NTSC.

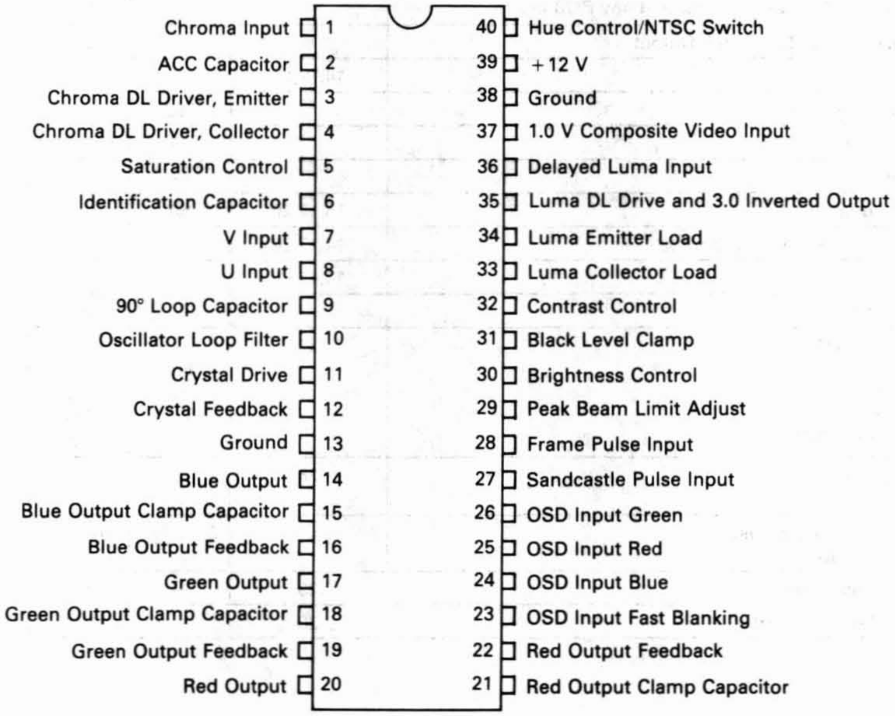
- Automatic Black Level Setup
- Beam Current Limiting
- Uses Inexpensive 4.43/3.58 MHz Crystal
- No Oscillator Adjustment Required
- Three OSD Inputs Plus Fast Blanking Input
- Four DC, High Impedance User Controls
- Interfaces with TDA3030B SECAM Adaptor
- Single 12 V Supply
- Low Dissipation, Typically 600 mW

## TV COLOR PROCESSOR

**SILICON MONOLITHIC**
**INTEGRATED CIRCUIT**

**P SUFFIX**
PLASTIC PACKAGE
CASE 711-03

**FIGURE 1 — PIN ASSIGNMENT**


Chroma Input 1
ACC Capacitor 2
Chroma DL Driver, Emitter 3
Chroma DL Driver, Collector 4
Saturation Control 5
Identification Capacitor 6
V Input 7
U Input 8
90° Loop Capacitor 9
Oscillator Loop Filter 10
Crystal Drive 11
Crystal Feedback 12
Ground 13
Blue Output 14
Blue Output Clamp Capacitor 15
Blue Output Feedback 16
Green Output 17
Green Output Clamp Capacitor 18
Green Output Feedback 19
Red Output 20
40 Hue Control/NTSC Switch
39 +12 V
38 Ground
37 1.0 V Composite Video Input
36 Delayed Luma Input
35 Luma DL Drive and 3.0 Inverted Output
34 Luma Emitter Load
33 Luma Collector Load
32 Contrast Control
31 Black Level Clamp
30 Brightness Control
29 Peak Beam Limit Adjust
28 Frame Pulse Input
27 Sandcastle Pulse Input
26 OSD Input Green
25 OSD Input Red
24 OSD Input Blue
23 OSD Input Fast Blanking
22 Red Output Feedback
21 Red Output Clamp Capacitor

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise stated)

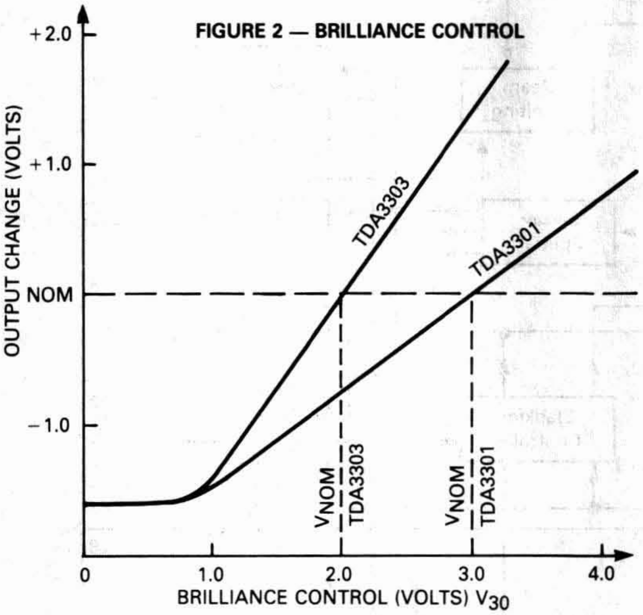
| Rating | Pin | Value | Unit |
|---|---|---|---|
| Supply Voltage | 39 | 14 | Vdc |
| Operating Temperature Range | | 0 to +70 | °C |
| Storage Temperature Range | | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, $V_{CC}$ = 12 V)

| Characteristic | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | 39 | 10.8 | 12 | 13.2 | V |
| Supply Current | | — | 45 | 60 | mA |
| Composite Video Input | 37 | — | 1.0 | — | Vp-p |
| Video Input Resistance | | 13 | 18 | 23 | kΩ |
| Video Gain to Pin 35 | | 2.7 | 3.2 | 3.6 | Vp-p |
| Input Window | | 0.8–3 | 0.7–3.2 | — | V |
| Chroma Input (Burst) | 1 | 10 | 100 | 200 | mVp-p |
| Input Resistance | 1 | — | 5.0 | — | kΩ |
| ACC Effectiveness | 4 | — | 1.2 | 3.0 | dB |
| OSD Input | 24,25,26 | 0.5 | 0.7 | 1.0 | V |
| OSD Drive Impedance | | — | — | 180 | Ω |
| OSD Frequency Response (−3.0 dB) | | 9.0 | — | — | MHz |
| OSD Max Gain | | — | 7.2 | — | MHz |
| Gain Difference Between Any Two | | — | — | 15 | % |
| Beam Current Ref. Threshold | 16,19,22 | 1.7 | 2.0 | 2.3 | V |
| Differential Voltage | | — | — | 20 | mV |
| Beam Current Ref. Input Current | | — | — | +1.5/−0.5 | μA |
| Differential Current | | — | — | 1.0 | μA |
| Luminance Gain Between Pin 36 and Outputs (depends on $R_{33}$ and $R_{34}$) | | — | 4.7 | — | |
| Luminance Bandwidth (−3.0 dB) | 14,17,20 | 9.0 | — | — | MHz |
| Output Resistance | | 120 | 170 | 300 | Ω |
| Residual Carrier (4.43 Mc/s) | | — | 30 | 150 | mVp-p |
| PAL Offset (H/2) | | — | — | 50 | mVp-p |
| Difference in Gain Between Y Input and any RGB o/p | | — | 5.0 | — | % |
| U Input Sensitivity for 5.0 V Blue Output | 8 | — | 340 | — | mVp-p |
| Matrix Error | 14,17,20 | — | — | 10 | % |
| Oscillator Capture Range | | 350 | — | — | Hz |
| U Ref. Phase Error | | — | — | 5.0 | ° |
| V Ref. Phase Error | | — | — | 5.0 | ° |
| Color Kill Attenuation | 14,17,20 | 50 | — | — | dB |
| Contrast Tracking OSD/Luma/Chroma | 14,17,20 | — | — | — | dB |
| OSD Contrast Tracking | 14,17,20 | — | — | ±2.0 | dB |
| OSD Enable Slice Level | 23 | — | 0.7 | — | V |
| Sandcastle Slice Level | 27 | | | | |
| Burst Gate | | 6.5 | 7.2 | 8.0 | V |
| Line Blanking | | 2.0 | 2.6 | 3.0 | V |
| R Input $V_{27} > 7.0$ V | | — | 5.0 | — | kΩ |
| $V_{27} < 7.0$ V | | — | 22 | — | kΩ |
| Frame Slice Level | 28 | 2 | 2.8 | 3.6 | V |
| R Input | | | 15 | — | kΩ |
| Peak Beam Limiter Threshold ($I_{29}$ Min = 250 μA) | | 3.4 x $I_{29}$ | 4 x $I_{29}$ | 4.6 x $I_{29}$ | |
| Pin 29 Input Resistance | 29 | — | 5.0 | — | kΩ |
| Pin 29 Open Circuit Voltage | 29 | — | 10.6 | — | V |

## INPUT/OUTPUT FUNCTIONS

FIGURE 2 — BRILLIANCE CONTROL

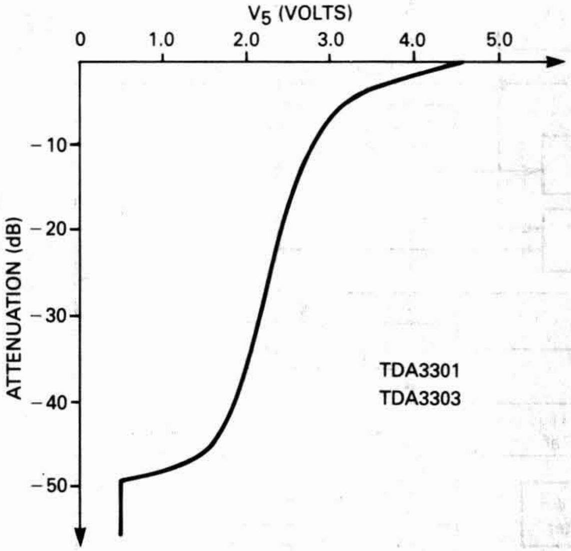


The brilliance control operates by adding a pedestal to the output signals. The amplitude of the pedestal is controlled by Pin 30.

During CRT beam current sampling a standard pedestal is substituted, its value being equivalent to the value given by $V_{30}$ Nom. Brightness at black level with $V_{30}$ Nom is given by the sum of three gun currents at the sampling level, i.e. 3 x 20 μA with 100 k reference resistors on Pins 16, 19, and 22.

During picture blanking the brilliance pedestal is zero; therefore the output voltage during blanking is always the minimum brilliance black level (Note: Signal channels are also gain blanked).

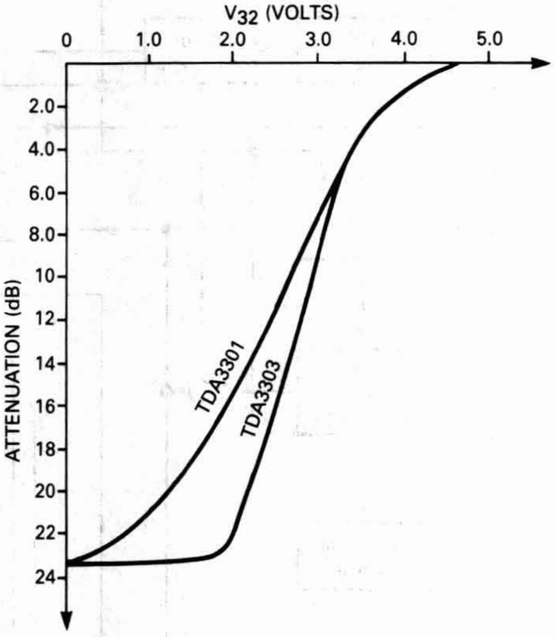
FIGURE 3 — SATURATION CONTROL VOLTAGE



Pin 5 is automatically pulled to ground with a misidentified PAL signal.

Note: Nominal 100% saturation point is given by choice of $R_2$ which sets ACC operating point.

FIGURE 4 — CONTRAST CONTROL



Note: Pin 32 is pulled down by the operation of the peak beam limiter.

FIGURE 5 — BLOCK DIAGRAM

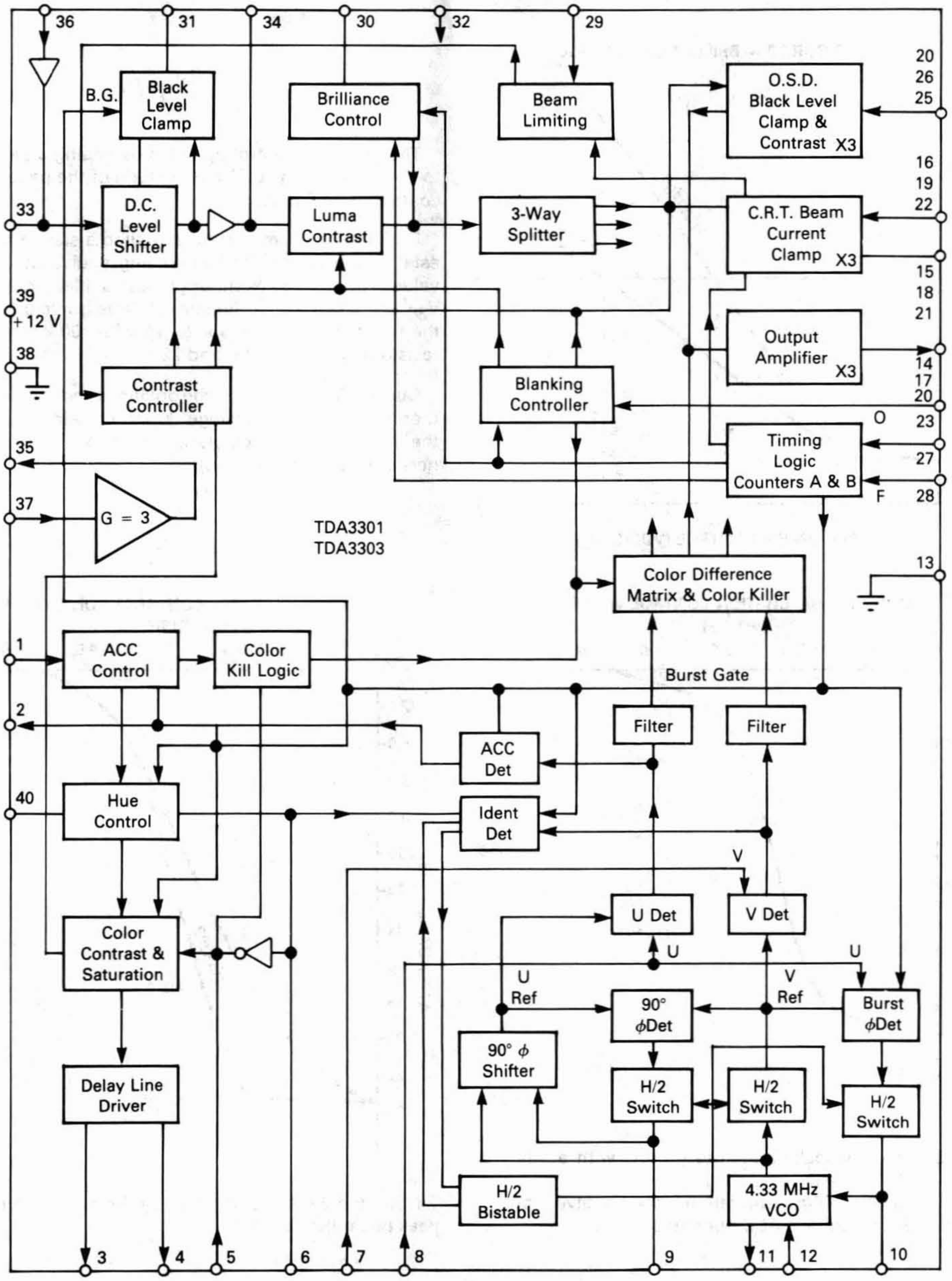
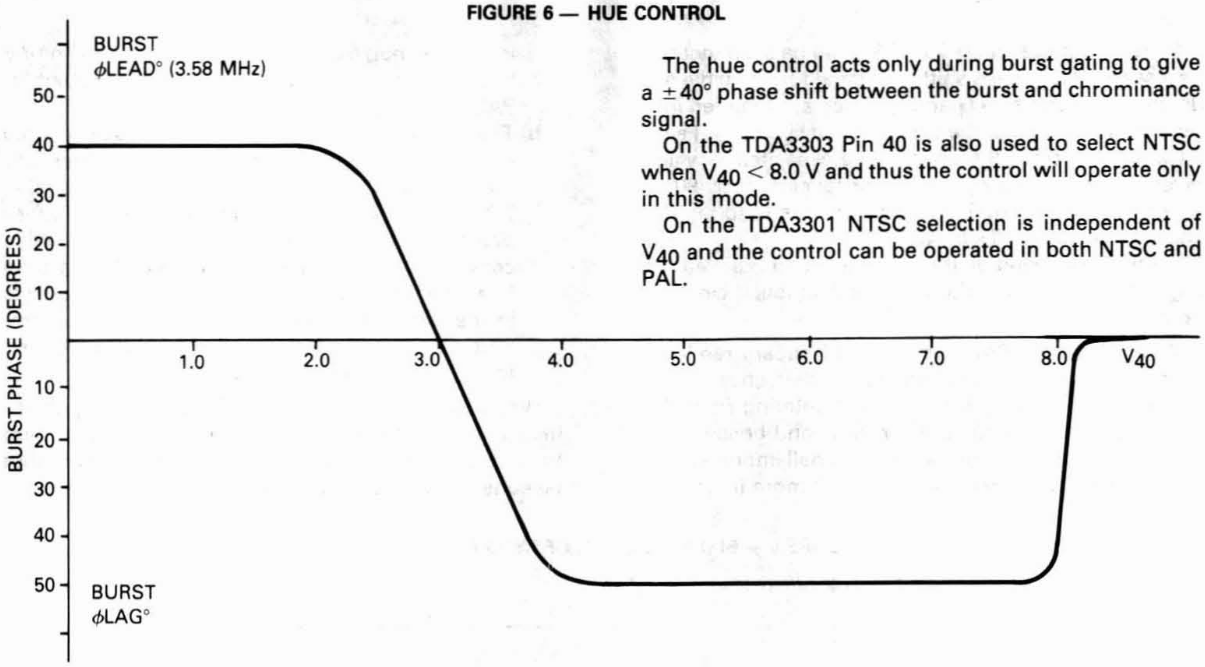

36
31
34
30
32
29
B.G.
Black Level Clamp
Brilliance Control
Beam Limiting
O.S.D. Black Level Clamp & Contrast X3
20
26
25
33
D.C. Level Shifter
Luma Contrast
3-Way Splitter
C.R.T. Beam Current Clamp X3
16
19
22
15
18
21
39
+ 12 V
38
Output Amplifier X3
14
17
20
Contrast Controller
Blanking Controller
O
23
Timing Logic Counters A & B
27
F
28
35
37
G = 3
TDA3301
TDA3303
13
Color Difference Matrix & Color Killer
1
ACC Control
Color Kill Logic
Burst Gate
2
Filter
Filter
ACC Det
40
Hue Control
Ident Det
V
U Det
V Det
U
U
Color Contrast & Saturation
U Ref
90° ϕDet
V Ref
Burst ϕDet
90° ϕ Shifter
H/2 Switch
H/2 Switch
H/2 Switch
Delay Line Driver
H/2 Bistable
4.33 MHz VCO
3
4
5
6
7
8
9
11
12
10

FIGURE 6 — HUE CONTROL



The hue control acts only during burst gating to give a ±40° phase shift between the burst and chrominance signal.

On the TDA3303 Pin 40 is also used to select NTSC when $V_{40} < 8.0$ V and thus the control will operate only in this mode.

On the TDA3301 NTSC selection is independent of $V_{40}$ and the control can be operated in both NTSC and PAL.

## CIRCUIT OPERATION

### CHROMINANCE DECODER SECTION

The chrominance decoder section of the TDA3301 consists of the following blocks:

Phase-locked reference oscillator — Figures 7, 8 and 9
Phase-locked 90 degree servo loop — Figures 9 and 10
U and V axis decoders
ACC detector and identification detector — Figure 11
Identification circuits and PAL bistable — Figure 12
Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

- a minimum number of factory adjustments
- a minimum number of external components
- compatibility with the SECAM adapter TDA3030B
- low dissipation
- use of a standard 4.433618 MHz Crystal rather than a 2.0 fc Crystal with divider.

### REFERENCE REGENERATION

The crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. A great deal of care was taken to ensure that the oscillator loop gain and the crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade crystal (crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

FIGURE 7 — VOLTAGE CONTROLLED OSCILLATOR (VCO)

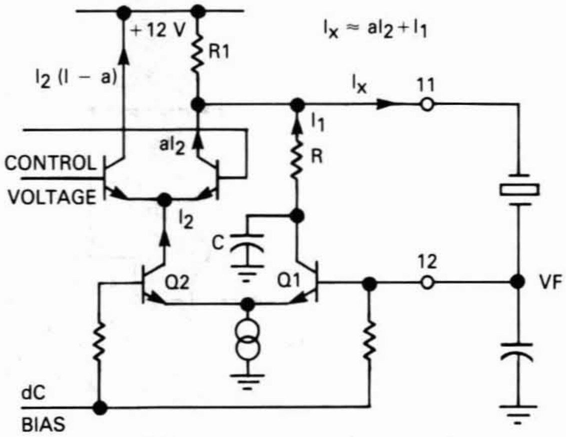
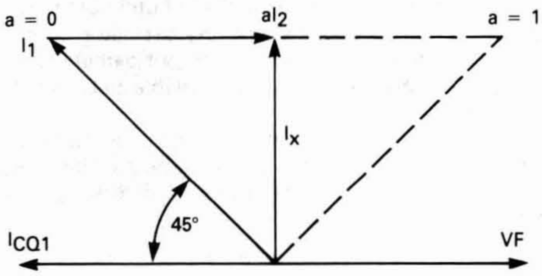


FIGURE 8 — VECTOR DIAGRAM FOR VCO



By referring to Figures 7 and 8 it can be seen that the necessary ±45° phase shift is obtained by variable addition of two currents $I_1$ and $I_2$ which are then fed into the load resistance of the crystal tuned circuit $R_1$. Feedback is taken from the crystal load capacitance which gives a voltage VF lagging the crystal current by 90°.

The RC network in $T_1$ collector causes $I_1$ to lag the collector current of $T_1$ by 45°.

For SECAM operation the currents $I_1$ and $I_2$ are added together in a fixed ratio giving a frequency close to nominal.

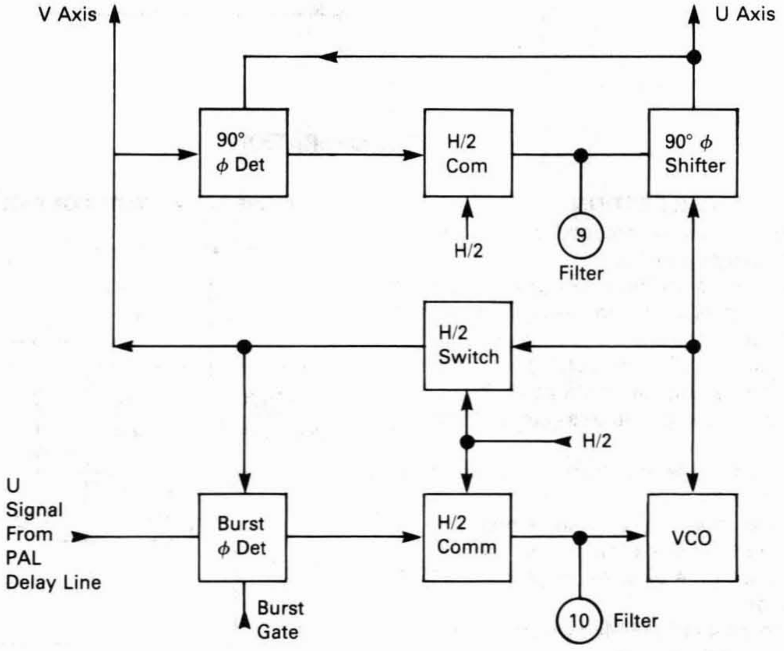
When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not dc. A commutator at the phase detector output also driven from the PAL bistable converts this ac signal to a dc prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC this cannot be considered to be a serious disadvantage.

FIGURE 9 — BLOCK DIAGRAM OF REFERENCE SECTION



## 90° REFERENCE GENERATION

To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the variable all-pass network (see Figure 10).

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B adapter.

FIGURE 10 — VARIABLE ALL-PASS NETWORK

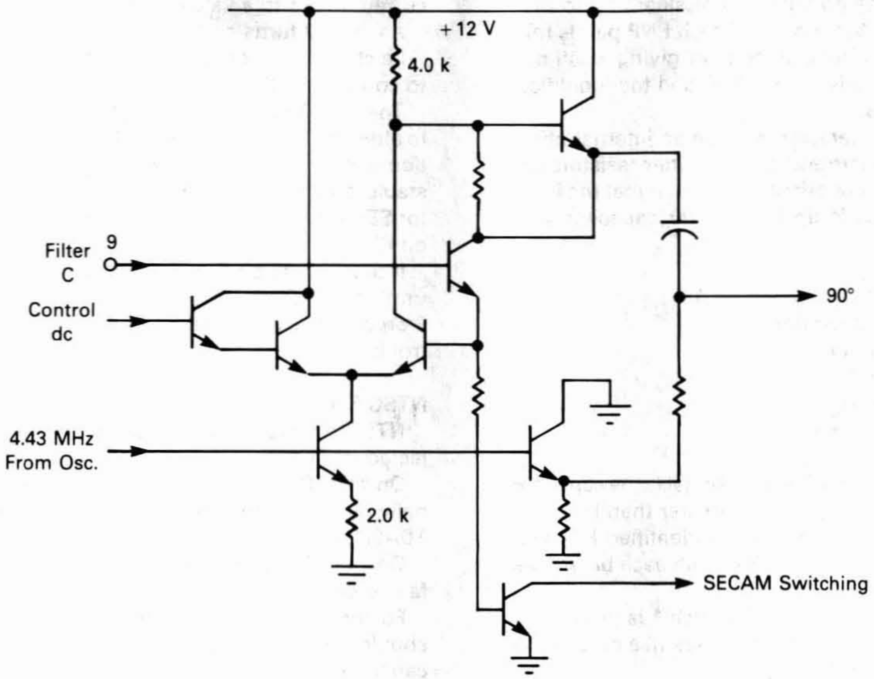
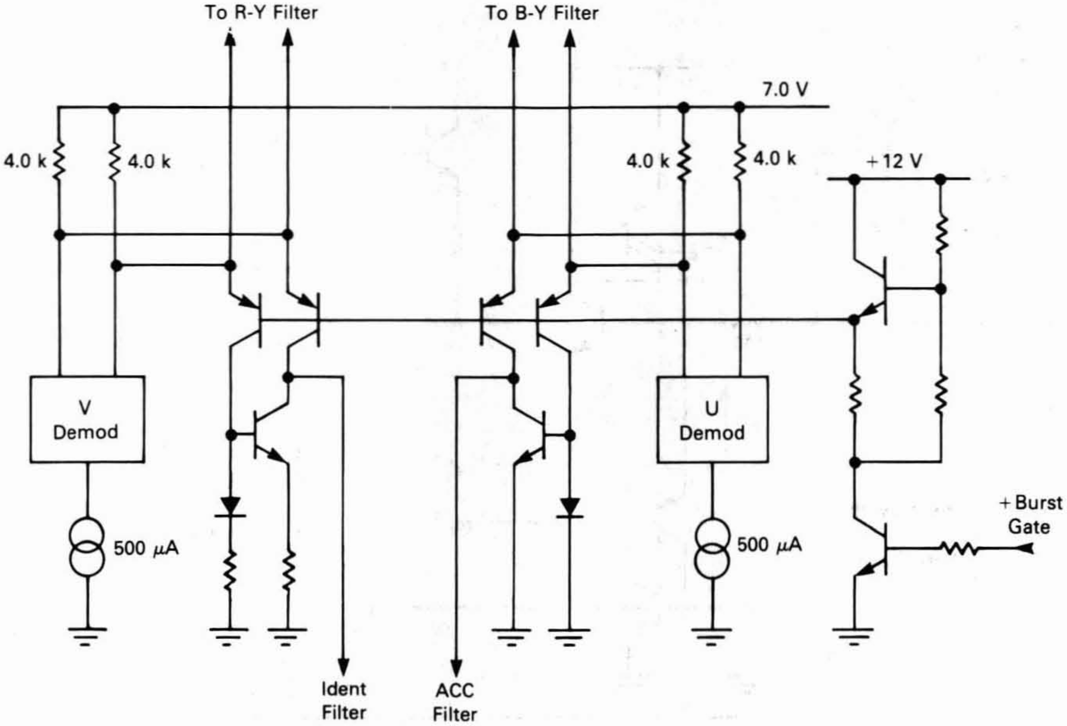

+12 V
4.0 k
Filter C
9
Control dc
4.43 MHz From Osc.
2.0 k
90°
SECAM Switching

FIGURE 11 — ACC AND IDENTIFICATION DETECTORS


To R-Y Filter
To B-Y Filter
7.0 V
4.0 k
4.0 k
4.0 k
4.0 k
+12 V
V Demod
U Demod
500 μA
500 μA
+Burst Gate
Ident Filter
ACC Filter

## ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push-pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

## IDENTIFICATION

See Figure 12 for definitions.

| | |
|---|---|
| Monochrome | $I_1 > I_2$ |
| PAL ident. OK | $I_1 < I_2$ |
| PAL ident. X | $I_1 > I_2$ |
| NTSC | $I_3 > I_2$ |

Only for correctly identified PAL signal is the capacitor voltage held low since $I_2$ is then greater than $I_1$.

For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage $V_{CC}$ rises with each burst gate pulse.

When $V_{ref}$ is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by $R_1$.

When $V_{ref}$ 2 is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current injected on Pin 6.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

## NTSC SWITCH

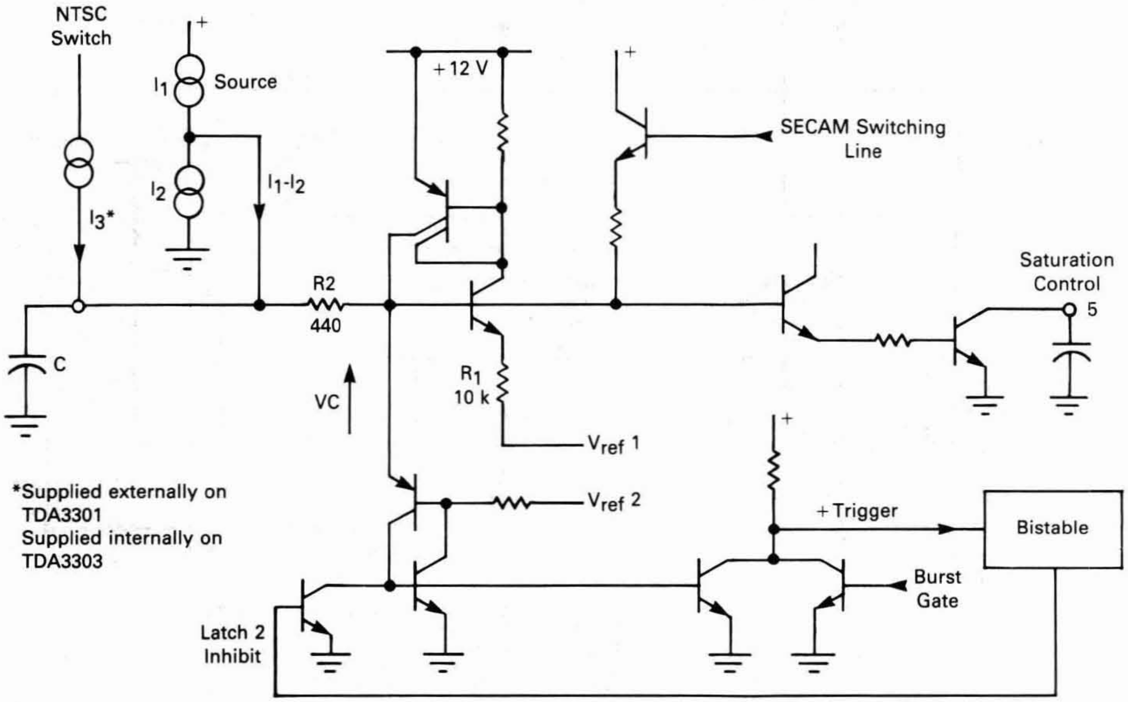
NTSC operation is selected when current ($I_3$) is injected into Pin 6.

On the TDA3301 this current must be derived externally by connecting Pin 6 to + 12 V via a resistor (as on TDA3300B).

On the TDA3303 $I_3$ is supplied internally when $V_{40}$ falls below 8.0 V;

For normal PAL operation on both versions Pin 40 should be connected to + 12 V and Pin 6 to the filter capacitor.

FIGURE 12 — IDENTIFICATION CIRCUIT



*Supplied externally on TDA3301
Supplied internally on TDA3303

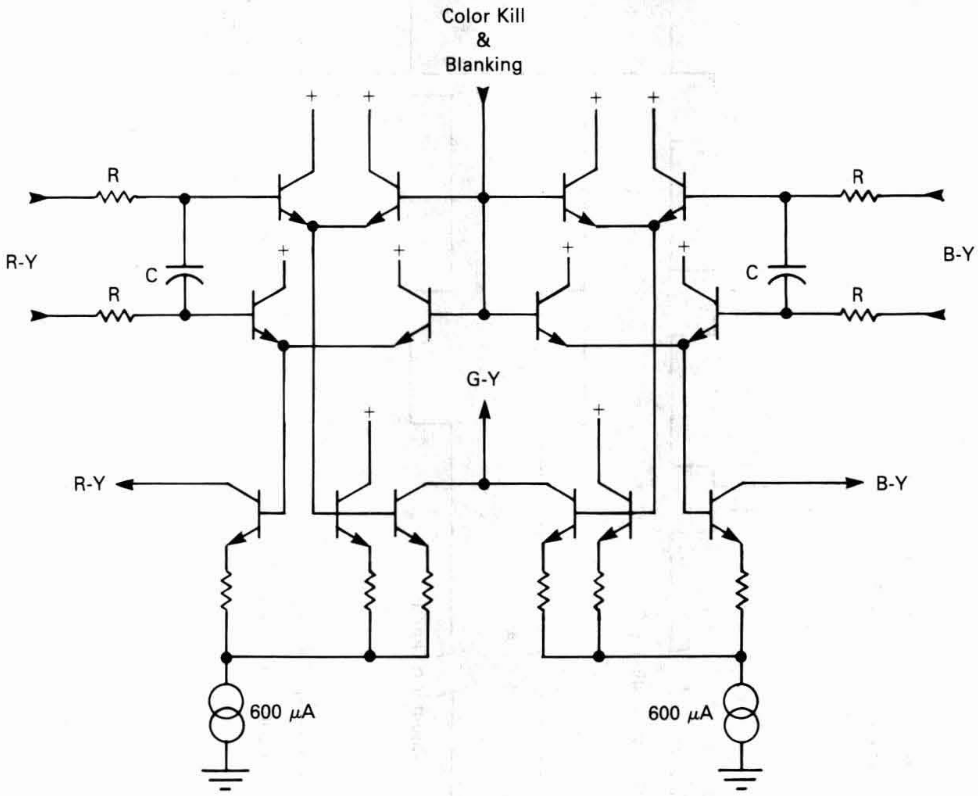
### COLOR DIFFERENCE MATRIXING, COLOR KILLING, AND CHROMA BLANKING

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

The color difference matrixing is performed by 2 differential amplifiers each with one side split to give the correct values of the −(B-Y) and −(R-Y) signals. These are added to give the (G-Y) signal.

The 3 color difference signals are then taken to the virtual earths of the video output stages together with luminance signal.

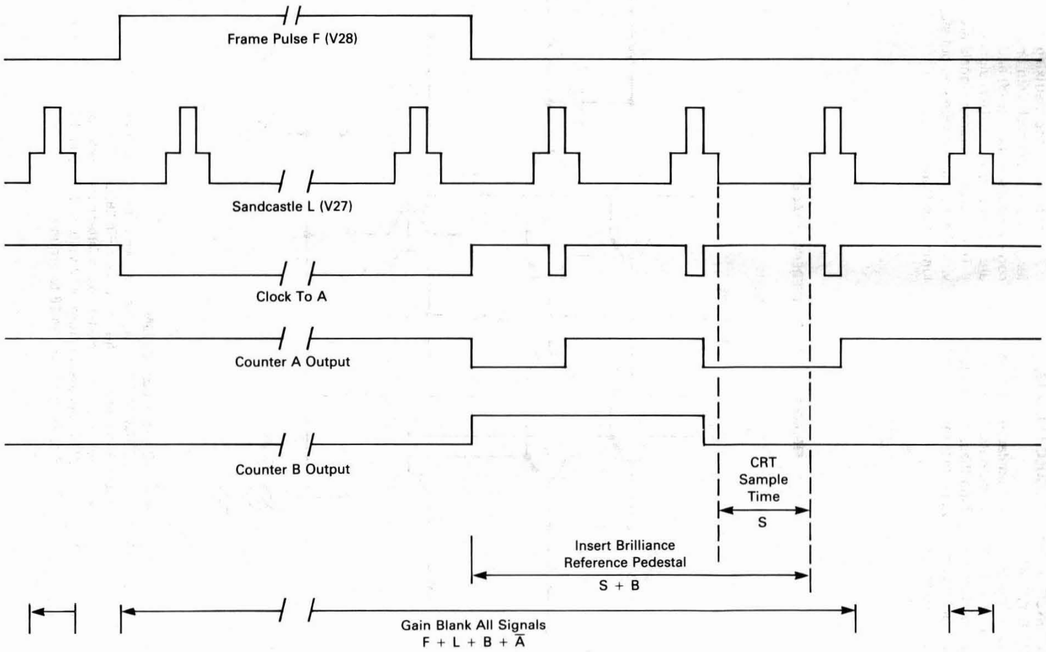
FIGURE 13 — COLOR DIFFERENCE STAGES



### SANDCASTLE SELECTION

The TDA3301/3303 may be used with a two level sandcastle and a separate frame pulse to Pin 28, or with only a 3 level (super) sandcastle. In the latter case a resistor of 1 MΩ is necessary from +12 volts to Pin 28 and a 470 pF capacitor from Pin 28 to ground.

FIGURE 14 — TIMING DIAGRAM


Frame Pulse F (V28)
Sandcastle L (V27)
Clock To A
Counter A Output
Counter B Output
CRT
Sample
Time
S
Insert Brilliance
Reference Pedestal
S + B
Gain Blank All Signals
F + L + B + $\bar{A}$

## TIMING COUNTER FOR SAMPLE CONTROL

In order to control the beam current sampling at the beginning of each frame scan two edge triggered flip-flops are used.

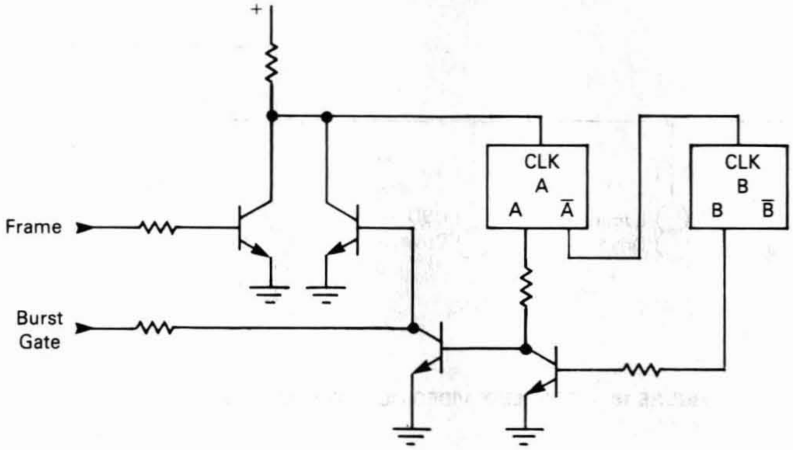
The output $\overline{A}$ of the first flip-flop A is used to clock the second flip-flop B. Clocking of A by the burst gate is inhibited by a count of $A.\overline{B}$.

The count sequence can only by initiated by the trailing edge of the frame pulse. In order to provide control signals for:

Luma/Chroma blanking,
Beam current sampling,
On-screen display blanking,
Brilliance control.

The appropriate flip-flop outputs are matrixed with sandcastle and frame signals by an emitter follower matrix.

FIGURE 15 — TIMING COUNTER



## ON-SCREEN DISPLAY INPUTS

Each section of the OSD stages consists of a common emitter input stage feeding a diversion gate controlled by the contrast control. During burst gate time a feedback loop is activated which clamps the signal at the input coupling capacitor. This ensures that the current in the diversion gate is zero at black level and makes the OSD black level insensitive to contrast control, also the inputs ignore signals below black, e.g. sync, pulses.

FIGURE 16 — OSD STAGE

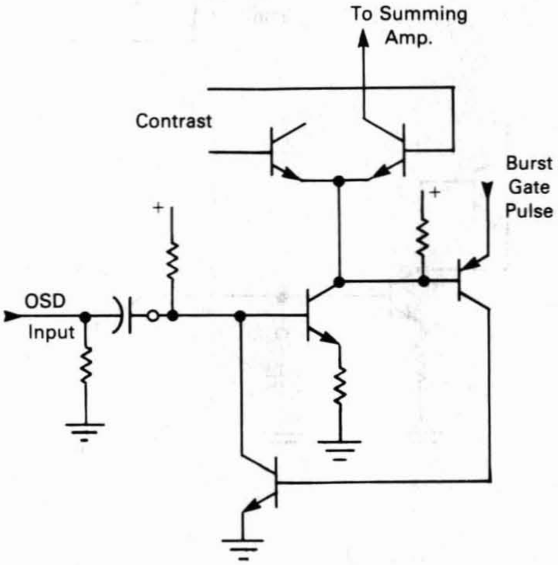


FIGURE 17 — VIDEO OUTPUT SECTION

Each video output stage consists of a feedback amplifier in which the input signal is a current drive to the virtual earth from the luminance, color difference and on-screen display stages.

A further drive current is used to control the dc operating point; this is derived from the sample and hold stage which samples the beam current after frame flyback.

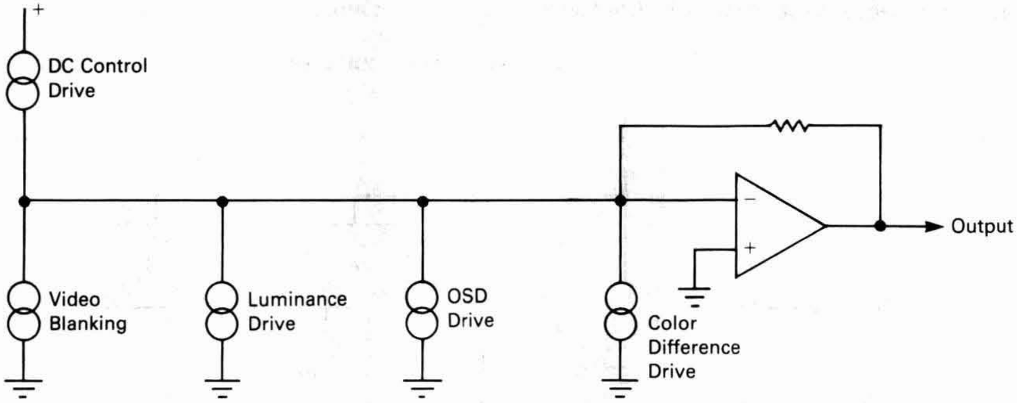

+
DC Control Drive
Video Blanking
Luminance Drive
OSD Drive
Color Difference Drive
−
+
Output

FIGURE 18 — COMPLETE VIDEO OUTPUT SECTIONS

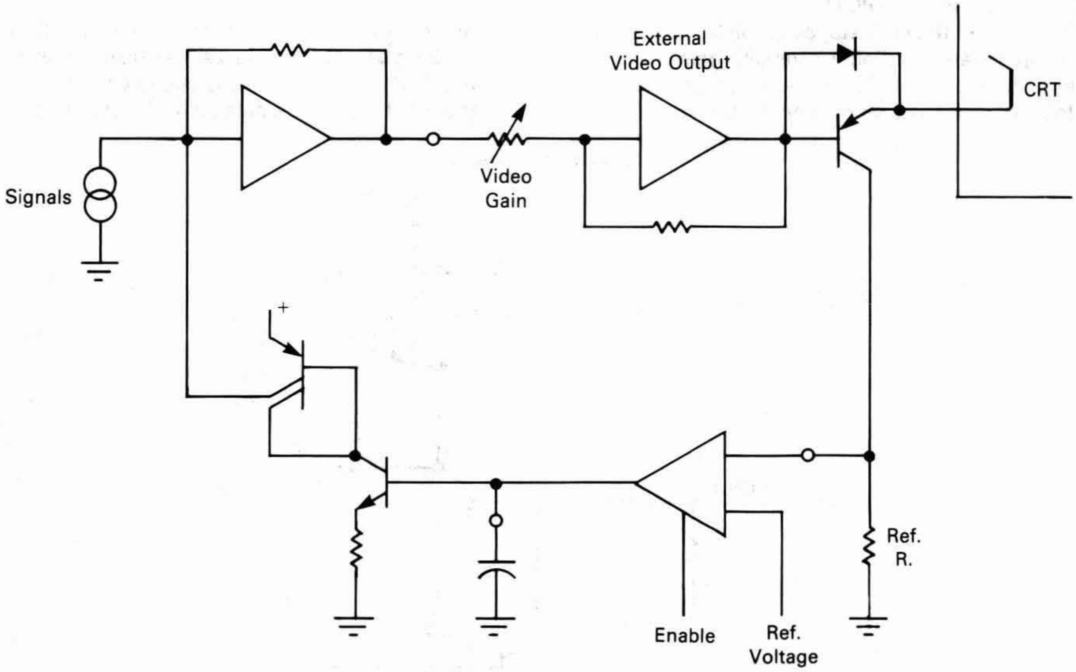
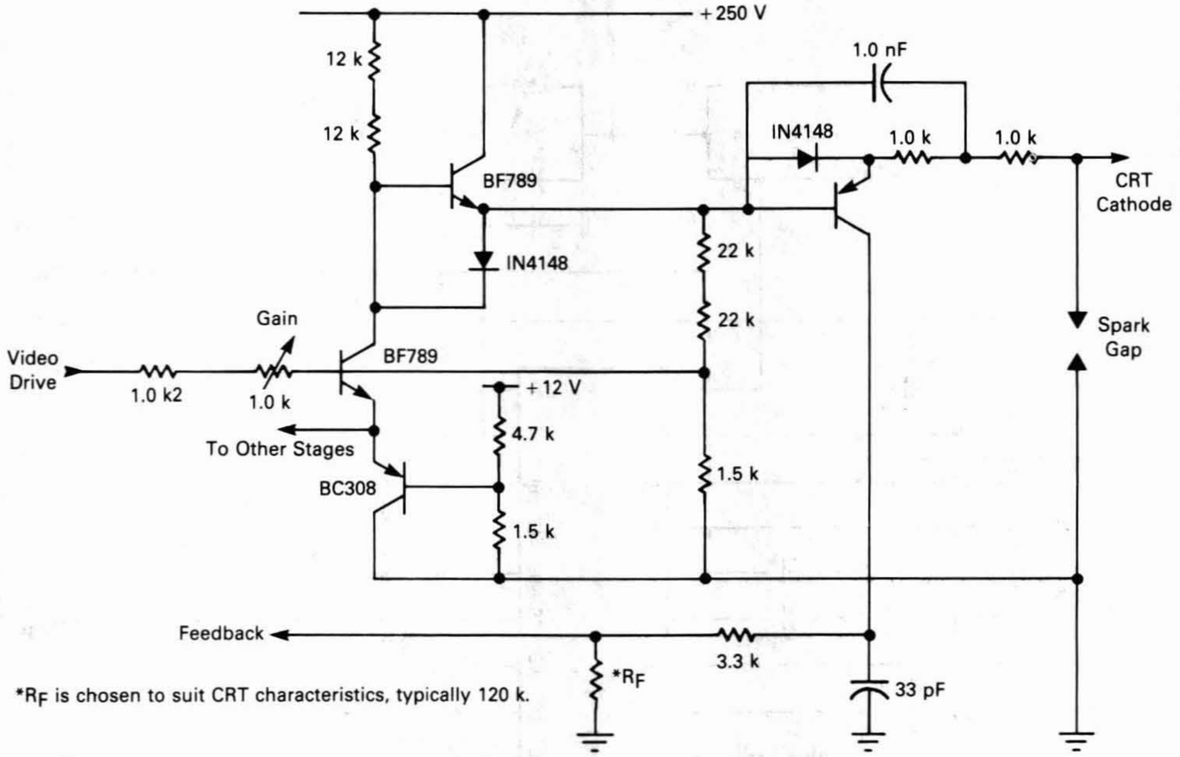

External Video Output
CRT
Signals
Video Gain
+
Ref. R.
Enable
Ref. Voltage

FIGURE 19 — TYPICAL VIDEO OUTPUT STAGE


+250 V
12 k
12 k
BF789
IN4148
1.0 nF
IN4148
1.0 k
1.0 k
CRT Cathode
22 k
22 k
Spark Gap
Gain
Video Drive
1.0 k2
1.0 k
BF789
+12 V
4.7 k
To Other Stages
BC308
1.5 k
1.5 k
Feedback
3.3 k
*RF
33 pF

*$R_F$ is chosen to suit CRT characteristics, typically 120 k.

FIGURE 20 — CLASS A VIDEO OUTPUT STAGE WITH DIRECT FEEDBACK

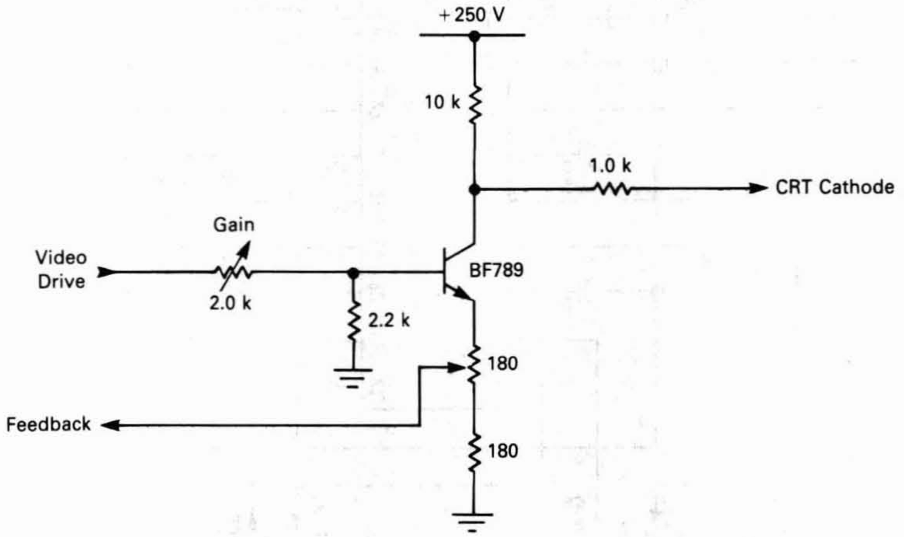
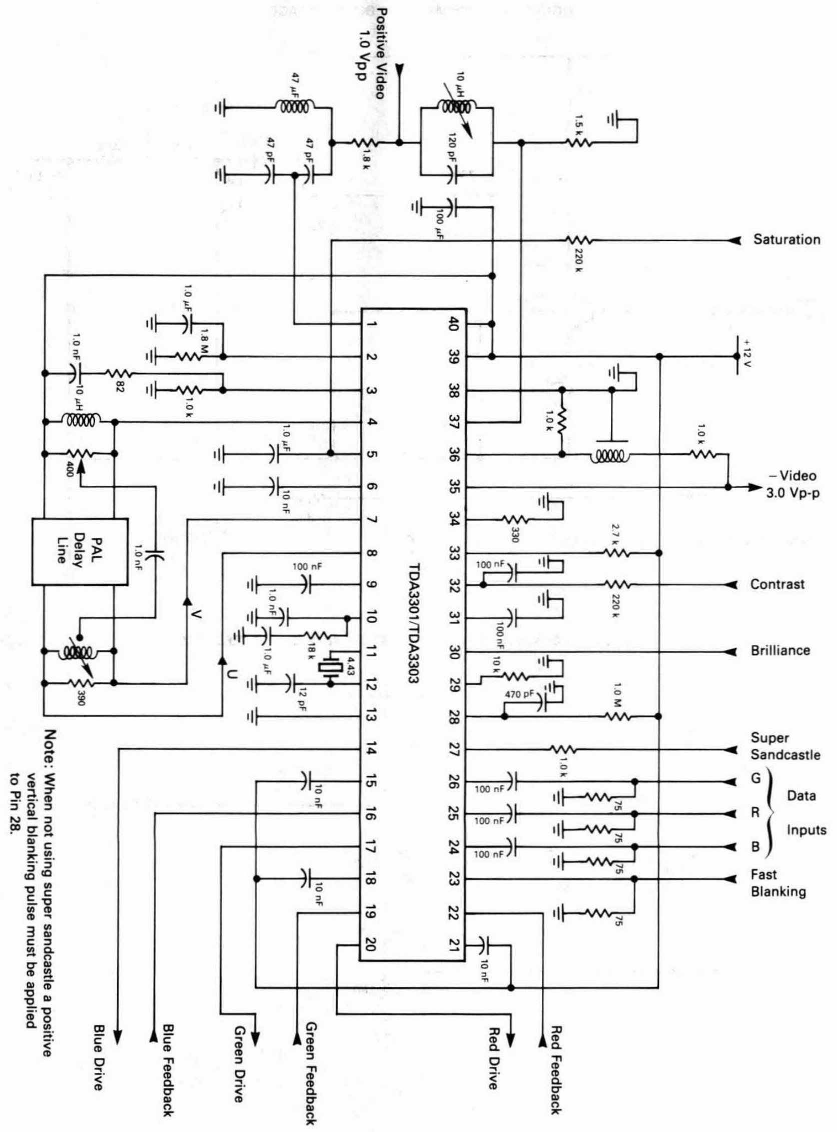

+250 V
10 k
1.0 k
CRT Cathode
Gain
Video Drive
2.0 k
2.2 k
BF789
180
180
Feedback

FIGURE 21 — TYPICAL PAL APPLICATION


TDA3301/TDA3303
Positive Video
1.0 Vpp
Saturation
+12 V
– Video
3.0 Vp-p
Contrast
Brilliance
Super
Sandcastle
G
R
B
Data
Inputs
Fast
Blanking
Red Feedback
Red Drive
Green Feedback
Green Drive
Blue Feedback
Blue Drive
PAL
Delay
Line
U
V
4.43
1.5 k
10 µH
120 pF
1.8 k
47 µF
47 pF
47 pF
100 µF
220 k
1.0 k
1.0 k
2.7 k
220 k
1.0 M
330
100 nF
100 nF
10 k
470 pF
1.0 k
100 nF
100 nF
100 nF
75
75
75
75
10 nF
1.0 µF
10 nF
100 nF
1.0 nF
18 k
1.0 µF
12 pF
10 nF
10 nF
1.0 µF
1.8 M
1.0 k
82
1.0 nF
10 µH
400
1.0 nF
390

**Note:** When not using super sandcastle a positive vertical blanking pulse must be applied to Pin 28.

**MOTOROLA**

# TDA3330

## TV COLOR PROCESSOR

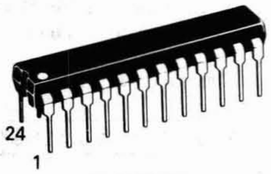
This device will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube.

Its simplified approach makes it particularly suitable for low cost CTV systems.

- No Oscillator Adjustment Required
- Four dc High Impedance User Controls
- Uses Inexpensive 4.43/3.58 MHz Crystals
- Interfaces With TDA3030B SECAM Adaptor
- Uses Horizontal Flyback or Super Sandcastle Pulse
- Single 12 V Supply
- Low Dissipation

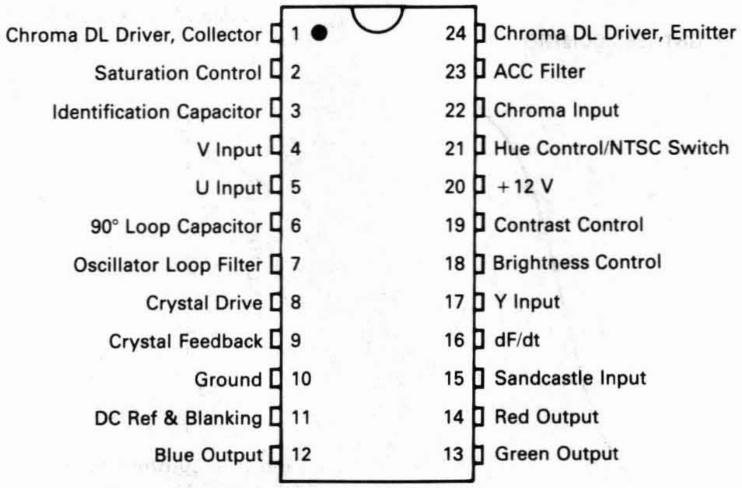
## TV COLOR PROCESSOR

**SILICON MONOLITHIC**
**INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 724-02

**FIGURE 1 — PIN ASSIGNMENT**


Chroma DL Driver, Collector 1
Saturation Control 2
Identification Capacitor 3
V Input 4
U Input 5
90° Loop Capacitor 6
Oscillator Loop Filter 7
Crystal Drive 8
Crystal Feedback 9
Ground 10
DC Ref & Blanking 11
Blue Output 12
24 Chroma DL Driver, Emitter
23 ACC Filter
22 Chroma Input
21 Hue Control/NTSC Switch
20 +12 V
19 Contrast Control
18 Brightness Control
17 Y Input
16 dF/dt
15 Sandcastle Input
14 Red Output
13 Green Output

**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise stated)

| Rating | Pin | Value | Unit |
|---|---|---|---|
| Supply Voltage | 20 | 14 | Vdc |
| Operating Temperature Range | | 0 to +70 | °C |
| Storage Temperature Range | | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, $V_{CC}$ = 12 V)

| Characteristic | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | 20 | 10.8 | 12 | 13.2 | V |
| Supply Current | | — | — | 50 | mA |
| Composite Video Input | 17 | — | 1.0 | — | Vp-p |
| Video Input Resistance | | | | | |
| Burst Gate On | | — | 5.0 | — | kΩ |
| Burst Gate Off | | — | 1.5 | — | MΩ |
| Chroma Input (Burst) | 22 | 10 | 100 | 200 | mVp-p |
| Input Resistance | 22 | — | 5.0 | — | kΩ |
| ACC Effectiveness | 1 | −1.5 | 0 | +1.5 | dB |
| Luminance Gain between Pin 17 and Outputs (Contrast max) | | — | 8.0 | — | |
| Luminance Bandwidth (−3.0 dB) | 12, 13, 14 | — | 5.0 | — | MHz |
| Output Resistance | | — | 170 | — | Ω |
| Residual Carrier (4.43 MHz) | | — | — | 200 | mVp-p |
| PAL Offset (H/2) | | — | — | 50 | mVp-p |
| U Input Sensitivity for 5.0 V Blue Output | 5 | — | 340 | — | mVp-p |
| Matrix Error | 12, 13, 14 | — | — | 10 | % |
| Oscillator Capture Range | | 300 | 500 | — | Hz |
| U Reference Phase Error | | — | — | 5.0 | ° |
| V Reference Phase Error | | — | — | 5.0 | ° |
| Color Kill Attenuation | 12, 13, 14 | 50 | — | — | dB |
| Contrast Tracking Luma/Chroma | 12, 13, 14 | — | 0 | 2.0 | dB |
| Sandcastle Slice Level | 15 | | | | |
| Burst Gate | | — | 7.2 | 8.0 | V |
| Line Blanking | | 0.5 | 1.5 | 2.5 | V |
| R Input $V_{15} > 7.0$ V | | — | 5.0 | — | kΩ |
| $V_{15} < 7.0$ V | | — | 10 | — | kΩ |

## INPUT/OUTPUT FUNCTIONS

**FIGURE 2 — BRIGHTNESS CONTROL**

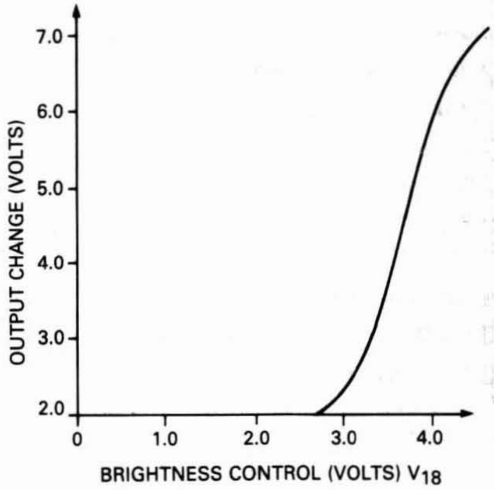
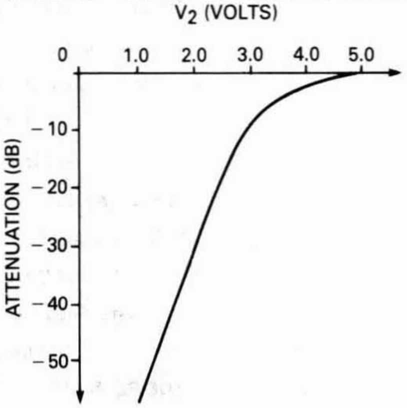


**FIGURE 3 — SATURATION CONTROL VOLTAGE**



Pin 2 is automatically pulled to ground with a mis-identified PAL signal.

Note: Nominal 100% saturation point is given by choice of $R_{pin\ 23}$ which sets ACC operating point.

FIGURE 4 — CONTRAST CONTROL

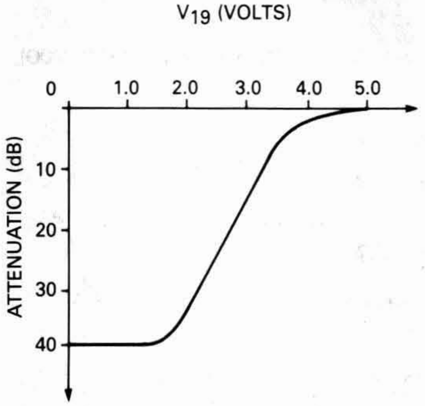
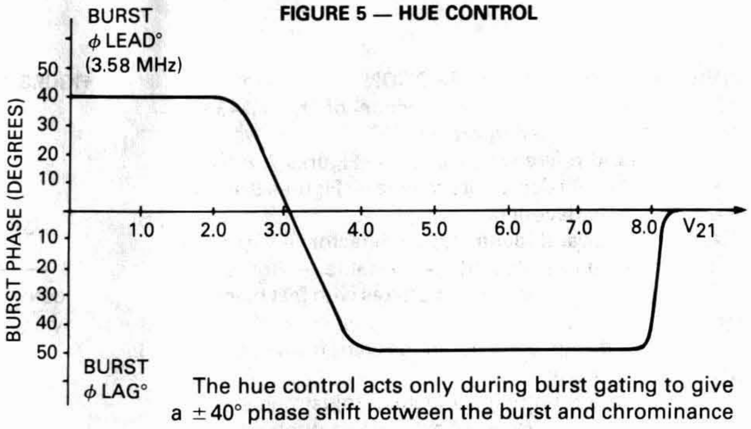


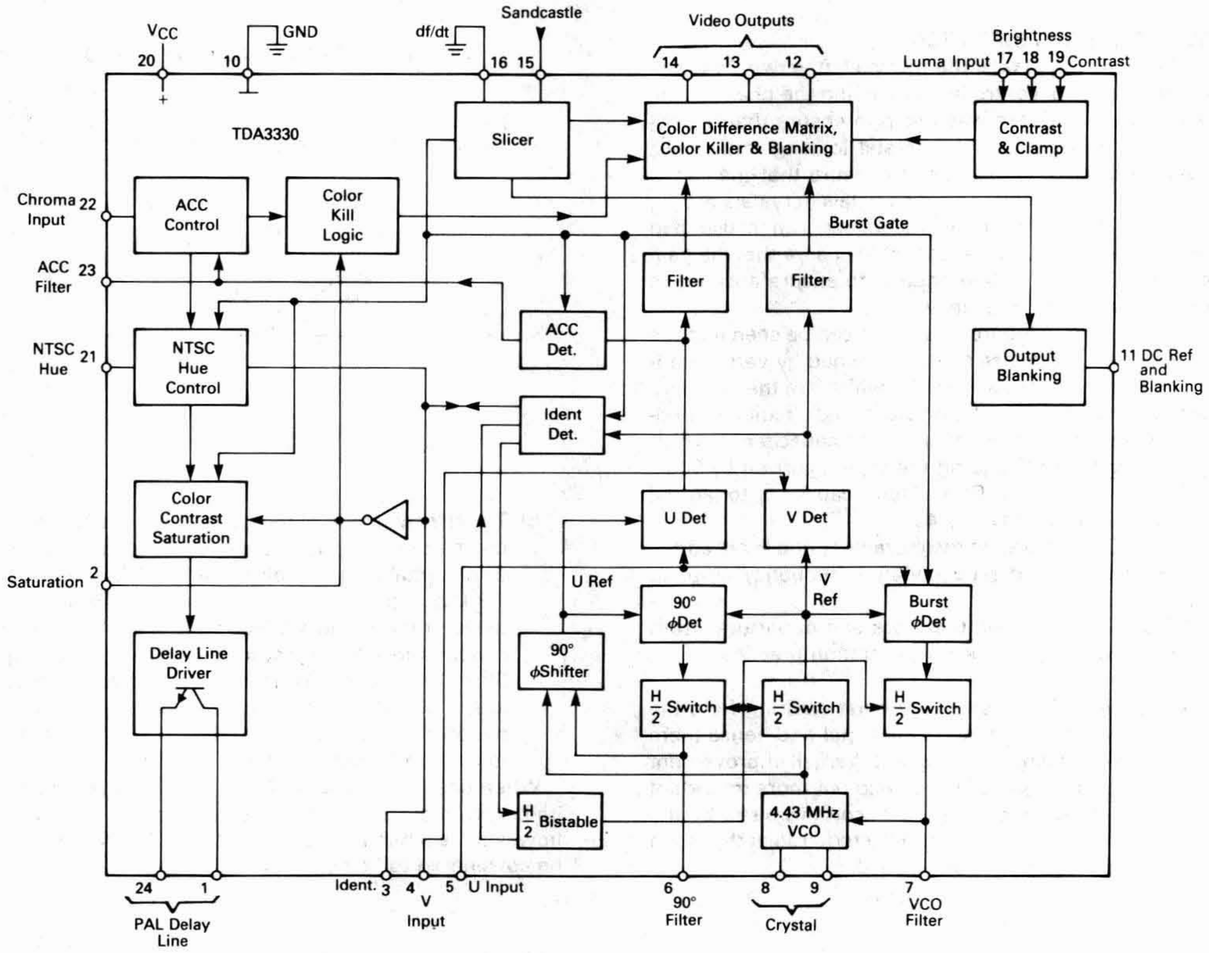
FIGURE 5 — HUE CONTROL



The hue control acts only during burst gating to give a ±40° phase shift between the burst and chrominance signal.

Pin 21 is also used to select NTSC when $V_{21} < 8.0$ V and thus the control will operate only in this mode. NTSC selection means the PAL phase switching is turned off. Delay-line and filter switching must be implemented externally.

FIGURE 6 — BLOCK DIAGRAM


Sandcastle
Video Outputs
VCC
GND
df/dt
Brightness
20
10
16
15
14
13
12
Luma Input
17
18
19
Contrast
TDA3330
Slicer
Color Difference Matrix, Color Killer & Blanking
Contrast & Clamp
Chroma Input 22
ACC Control
Color Kill Logic
Burst Gate
ACC Filter 23
Filter
Filter
ACC Det.
NTSC Hue 21
NTSC Hue Control
Output Blanking
11 DC Ref and Blanking
Ident Det.
Color Contrast Saturation
U Det
V Det
Saturation 2
U Ref
V Ref
90° φDet
Burst φDet
Delay Line Driver
90° φShifter
H/2 Switch
H/2 Switch
H/2 Switch
H/2 Bistable
4.43 MHz VCO
24
1
PAL Delay Line
Ident. 3
4 V Input
5 U Input
6 90° Filter
8
9
Crystal
7 VCO Filter

## CIRCUIT OPERATION

### CHROMINANCE DECODER SECTION

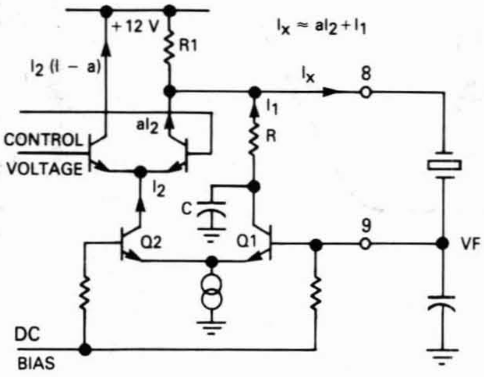
The chrominance decoder section of the TDA3330 consists of the following blocks:

Phase-locked reference oscillator — Figures 7, 8 and 9
Phase-locked 90 degree servo loop — Figures 9 and 10
U and V axis decoders
ACC detector and identification detector — Figure 11
Identification circuits and PAL bistable — Figure 12
Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

- a minimum number of factory adjustments
- a minimum number of external components
- compatibility with the SECAM adapter TDA3030B
- low dissipation
- use of a standard 4.433618 MHz crystal rather than a 2.0 fc crystal with divider, (or standard 3.579545 MHz for NTSC).

FIGURE 7 — VOLTAGE CONTROLLED OSCILLATOR (VCO)



### REFERENCE REGENERATION

The crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. Much care was taken to ensure that the oscillator loop gain and the crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade crystals ( crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

By referring to Figures 7 and 8 it can be seen that the necessary ±45° phase shift is obtained by variable addition of two currents $I_1$ and $I_2$ which are then fed into the load resistance of the crystal tuned circuit $R_1$. Feedback is taken from the crystal load capacitance which gives a voltage VF lagging the crystal current by 90°.

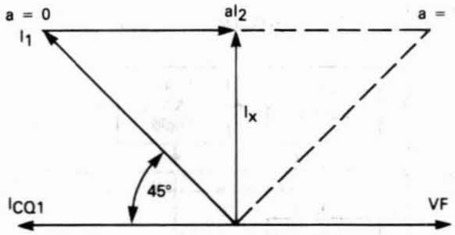
The RC network in Q1 collector causes $I_1$ to lag the collector current of Q1 by 45°.

For SECAM operation the currents $I_1$ and $I_2$ are added together in a fixed ratio giving a frequency close to nominal.

When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

FIGURE 8 — VECTOR DIAGRAM FOR VCO



b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not DC. A commutator at the phase detector output also driven from the PAL bistable converts this AC signal to a DC prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC this cannot be considered to be serious disadvantage.

## 90° REFERENCE GENERATION

To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the variable all-pass network. (See Figure 10.)

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation with TDA3030B the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B adapter.

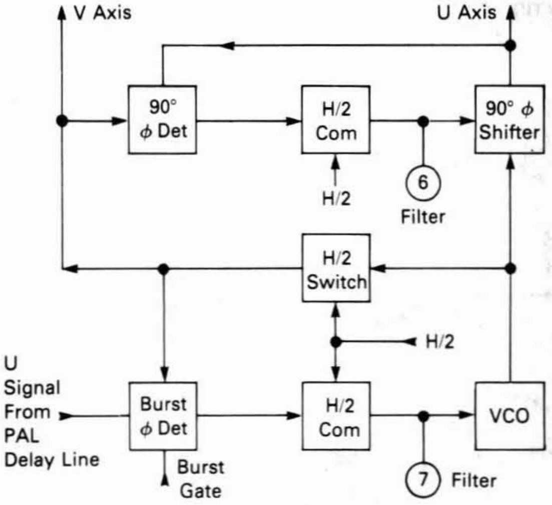


FIGURE 9 — BLOCK DIAGRAM OF REFERENCE SECTION

## ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

## IDENTIFICATION

See Figure 12 for definitions.

| | |
|---|---|
| Monochrome | $I_1 > I_2$ |
| PAL ident. OK | $I_1 < I_2$ |
| PAL ident. X | $I_1 > I_2$ |
| NTSC | $I_3 > I_2$ |

Only for correctly identified PAL signal is the capacitor voltage held low since $I_2$ is then greater than $I_1$.

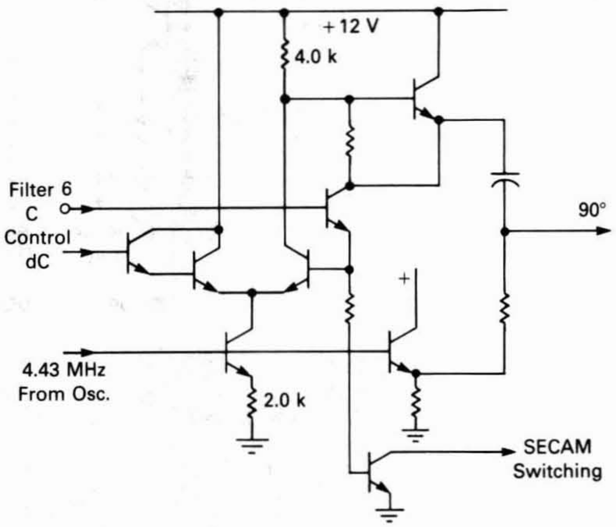


FIGURE 10 — VARIABLE ALL-PASS NETWORK

For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage $V_C$ rises with each burst gate pulse.

When $V_{ref}1$ is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by $R_1$.

When $V_{ref}2$ is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current ($I_3$) injected into Pin 3 by the NTSC switch. This is supplied internally when $V_{21}$ falls below 8.0 V.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

FIGURE 11 — ACC AND IDENTIFICATION DETECTORS

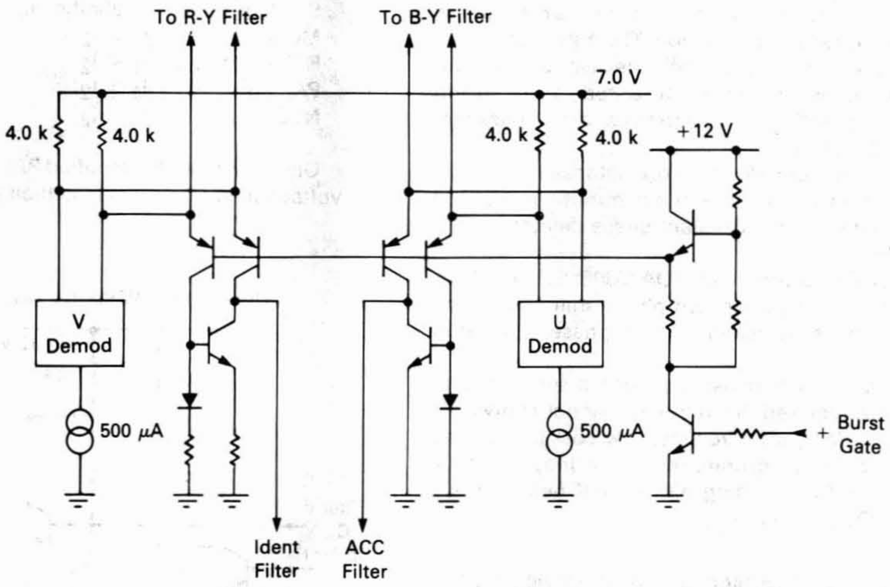
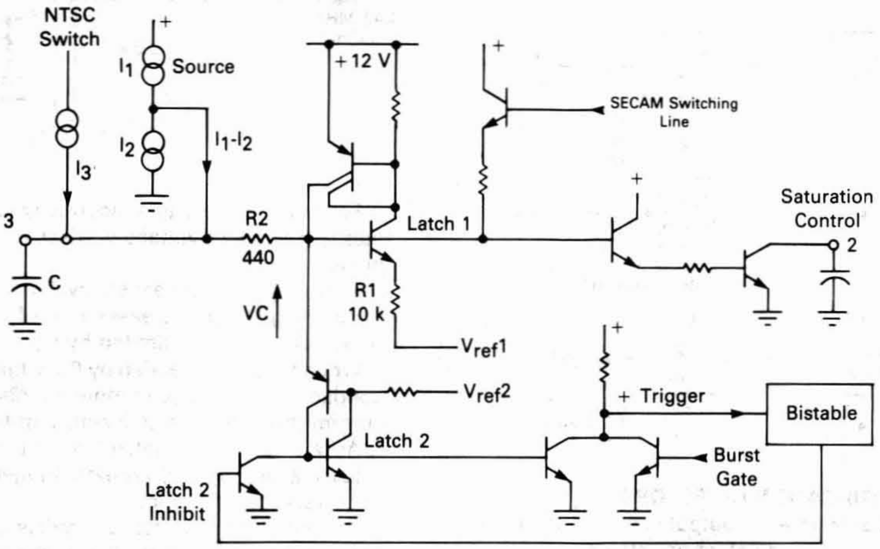

To R-Y Filter
To B-Y Filter
7.0 V
4.0 k
4.0 k
4.0 k
4.0 k
+12 V
V
Demod
U
Demod
500 μA
500 μA
Burst
Gate
Ident
Filter
ACC
Filter

FIGURE 12 — IDENTIFICATION CIRCUIT


NTSC
Switch
I1
Source
I2
I1-I2
I3
3
C
R2
440
VC
+12 V
Latch 1
R1
10 k
Vref1
Vref2
SECAM Switching
Line
Saturation
Control
2
+ Trigger
Bistable
Latch 2
Latch 2
Inhibit
Burst
Gate

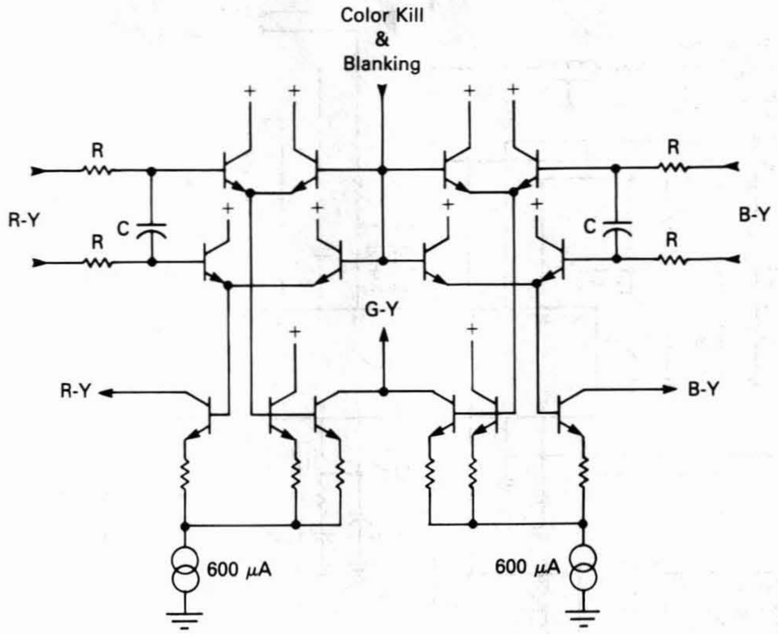
## COLOR DIFFERENCE MATRIXING, COLOR KILLING, AND CHROMA BLANKING

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

The color difference matrixing is performed by 2 differential amplifiers each with one side split to give the correct values of the −(B-Y) and −(R-Y) signals. These are added to give the (G-Y) signal.

The 3 color difference signals are then taken to the virtual earths of the video output stages together with luminance signal.

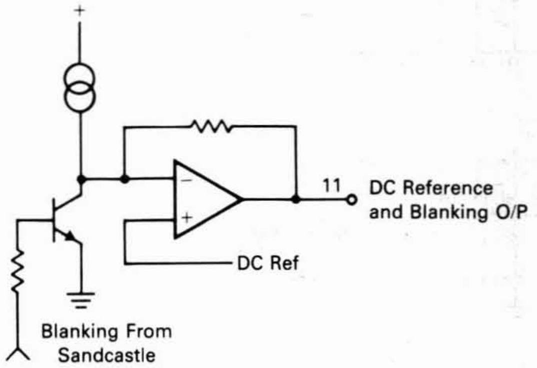
FIGURE 13 — COLOR DIFFERENCE STAGES


Color Kill
&
Blanking
R
R
R-Y
C
R
C
R
B-Y
G-Y
R-Y
B-Y
600 μA
600 μA

## SANDCASTLE SECTION

The input signal is sliced at 2 levels, 1.5 V and 7.2 V. Above 1.5 V is used for blanking, above 7.2 V for burst gating provided level on Pin 16 is below 0.7 V. If a normal Sandcastle is used, it is recommended to ground the Pin 16. This input is used to inhibit the burst gate. This is used if a true Sandcastle is not available; in this case horizontal flyback may be used instead and differentiated flyback applied to the $\frac{df}{dt}$ pin (input resistance 1.0 kΩ).

FIGURE 14 — DC REFERENCE AND BLANKING SECTION


11
DC Reference
and Blanking O/P
DC Ref
Blanking From
Sandcastle

The DC Reference and Blanking section is used to bias the Video output stages. The temperature coefficient is arranged to be a $V_{BE}$ drift less than the Red, Green and Blue outputs.

FIGURE 15 — TYPICAL PAL APPLICATION

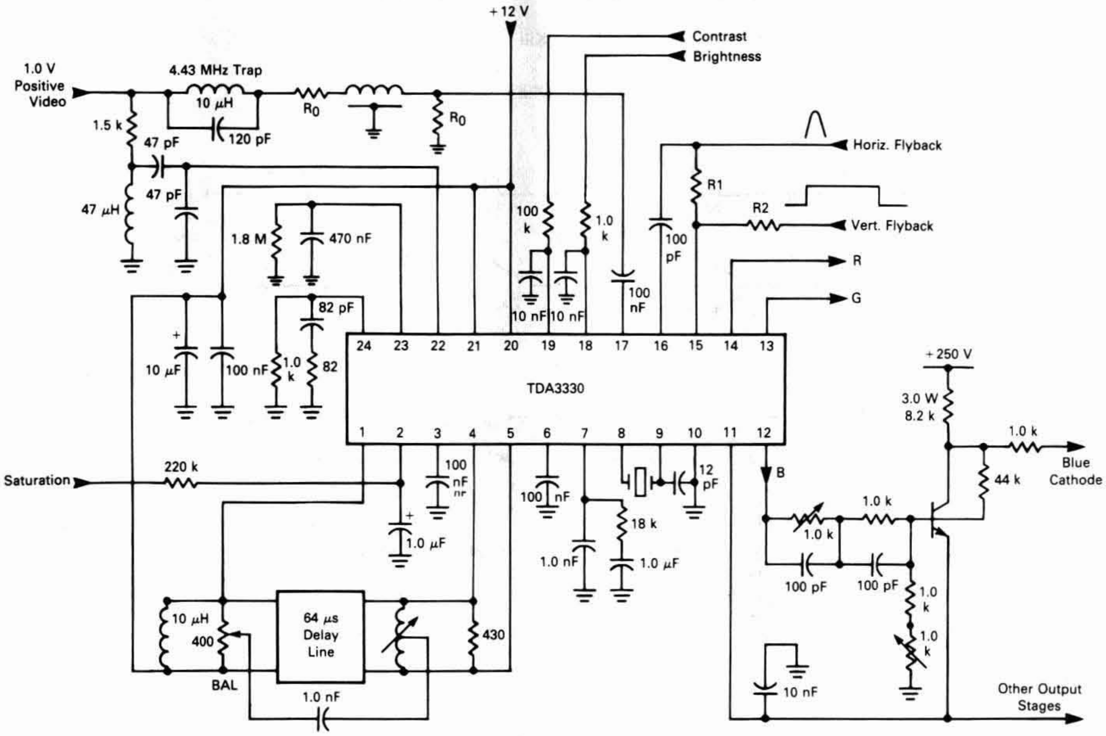
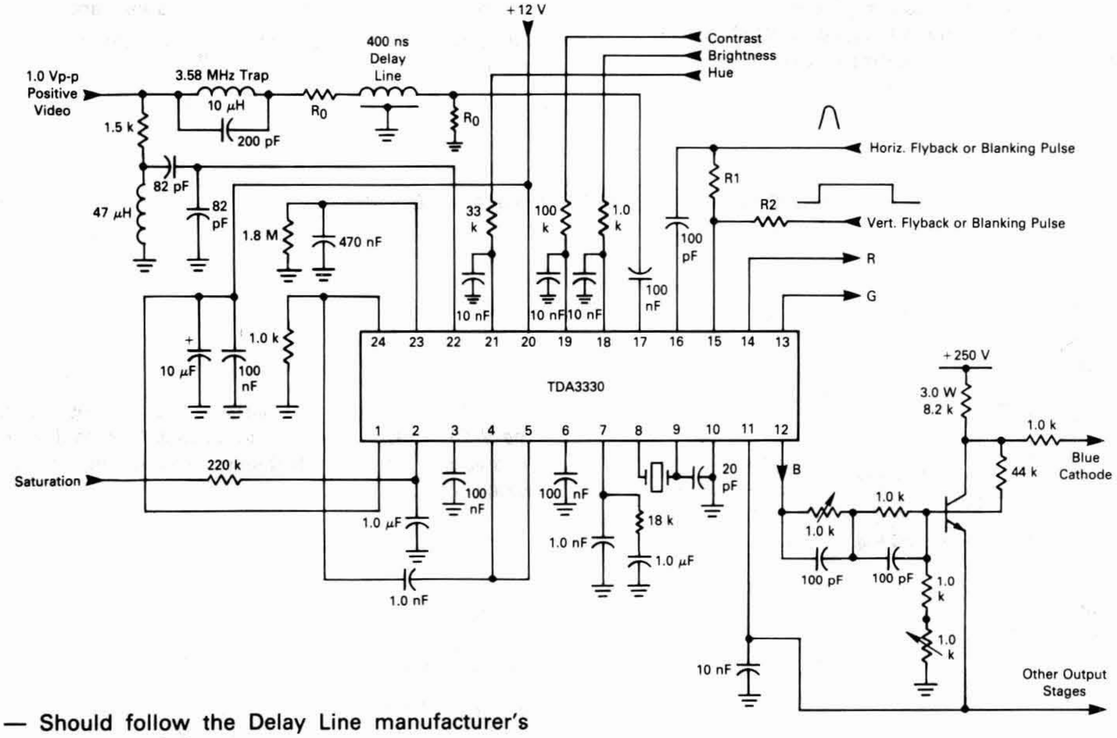

+12 V
Contrast
Brightness
1.0 V Positive Video
4.43 MHz Trap
10 µH
R0
R0
1.5 k
47 pF
120 pF
47 pF
47 µH
Horiz. Flyback
R1
R2
Vert. Flyback
R
G
1.8 M
470 nF
100 k
1.0 k
100 pF
10 nF
10 nF
100 nF
82 pF
10 µF
100 nF
1.0 k
82
24
23
22
21
20
19
18
17
16
15
14
13
TDA3330
1
2
3
4
5
6
7
8
9
10
11
12
+250 V
3.0 W 8.2 k
1.0 k
Blue Cathode
44 k
B
1.0 k
1.0 k
Saturation
220 k
100 nF
1.0 µF
100 nF
18 k
1.0 nF
1.0 µF
12 pF
100 pF
100 pF
1.0 k
1.0 k
10 µH
400
BAL
64 µs Delay Line
430
1.0 nF
10 nF
Other Output Stages

FIGURE 16 — TYPICAL NTSC APPLICATION


+12 V
Contrast
Brightness
Hue
400 ns Delay Line
1.0 Vp-p Positive Video
3.58 MHz Trap
10 µH
R0
R0
1.5 k
200 pF
82 pF
82 pF
47 µH
Horiz. Flyback or Blanking Pulse
R1
R2
Vert. Flyback or Blanking Pulse
R
G
1.8 M
470 nF
33 k
100 k
1.0 k
100 pF
10 nF
10 nF
10 nF
100 nF
1.0 k
10 µF
100 nF
24
23
22
21
20
19
18
17
16
15
14
13
TDA3330
1
2
3
4
5
6
7
8
9
10
11
12
+250 V
3.0 W 8.2 k
1.0 k
Blue Cathode
44 k
B
1.0 k
1.0 k
Saturation
220 k
1.0 µF
100 nF
1.0 nF
100 nF
18 k
1.0 nF
1.0 µF
20 pF
100 pF
100 pF
1.0 k
1.0 k
10 nF
Other Output Stages

$R_0$ — Should follow the Delay Line manufacturer's recommendations.

$R_1$ — Should be selected to give approximately 10–12 V pulse at Pin 15 (approximately 5.0 k internal resistance).

$R_2$ — Should be selected to give approximately 4.0 to 5.0 V pulse at Pin 15 (approximately 10 k internal resistance).

**MOTOROLA**

# TDA3333

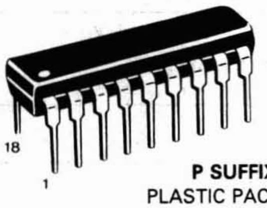
## TV COLOR DIFFERENCE DEMODULATOR

This device is designed to demodulate a typical chroma input signal and output the two color difference signals, R – Y and B – Y.

- Decodes PAL or NTSC
- Uses Inexpensive 4.43/3.58 MHz Crystal
- No Oscillator Adjustment Required
- On-Chip Hue Control for NTSC
- Interfaces with TDA3030B SECAM Adaptor
- Single 12 V Supply
- Low Dissipation

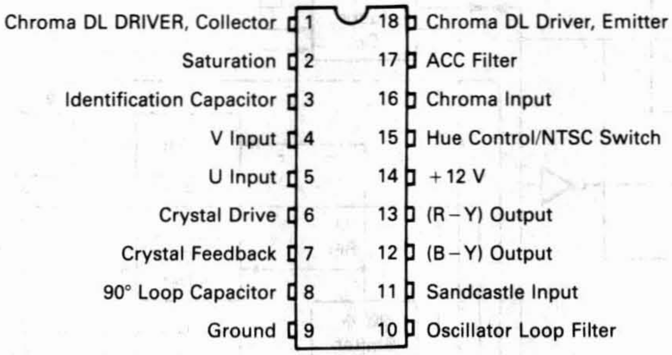
## TV COLOR DIFFERENCE DEMODULATOR

**SILICON MONOLITHIC INTEGRATED CIRCUIT**



**P SUFFIX**
PLASTIC PACKAGE
CASE 707-02

FIGURE 1 — PIN ASSIGNMENT


Chroma DL DRIVER, Collector 1
Saturation 2
Identification Capacitor 3
V Input 4
U Input 5
Crystal Drive 6
Crystal Feedback 7
90° Loop Capacitor 8
Ground 9
18 Chroma DL Driver, Emitter
17 ACC Filter
16 Chroma Input
15 Hue Control/NTSC Switch
14 +12 V
13 (R – Y) Output
12 (B – Y) Output
11 Sandcastle Input
10 Oscillator Loop Filter

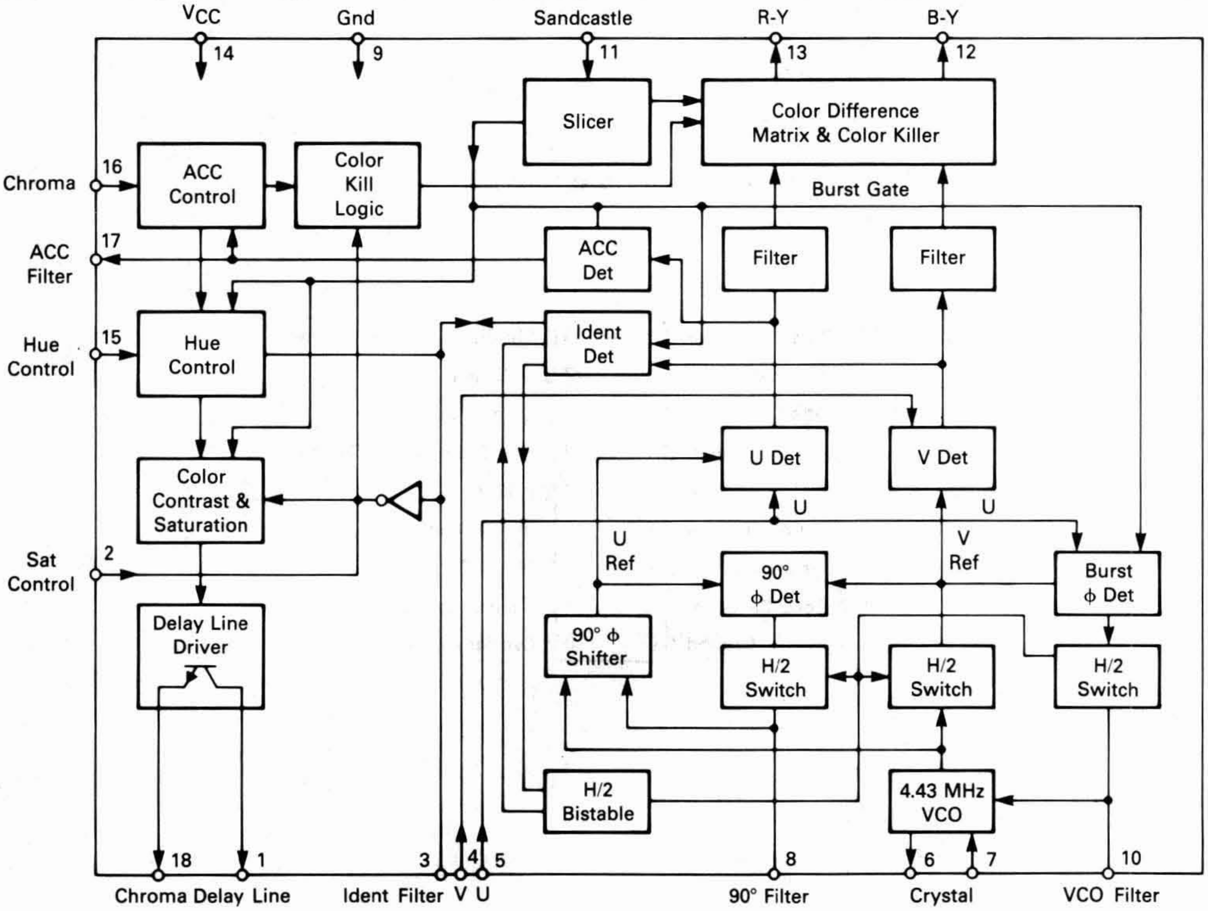
**MAXIMUM RATINGS** ($T_A$ = +25°C unless otherwise stated)

| Rating | Pin | Value | Unit |
|---|---|---|---|
| Supply Voltage | 39 | 14 | Vdc |
| Operating Temperature Range | | 0 to +70 | °C |
| Storage Temperature Range | | −65 to +150 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, $V_{CC}$ = 12 V)

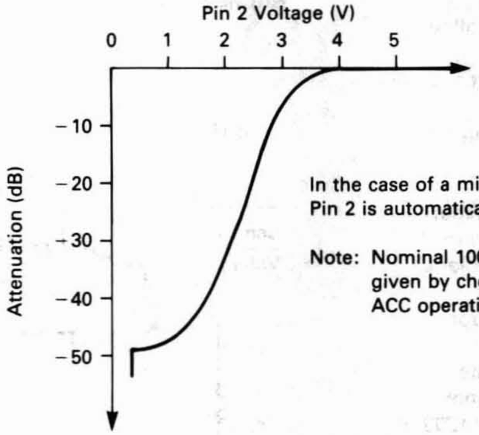
| Characteristic | | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | | 14 | 10.8 | 12 | 13.2 | V |
| Chroma Input | | 16 | 10 | 100 | 200 | mVp-p (burst) |
| ACC Effectiveness | | 1 | — | 1.2 | 3.0 | dB |
| Matrix Error | | | — | — | 10 | % |
| Oscillator Capture Range | | | 350 | — | — | Hz |
| U Ref. Phase Error | | | — | — | 5.0 | ° |
| V Ref. Phase Error | | | — | — | 5.0 | ° |
| U Input Sensitivity for 1.0 Vp-p | (B-Y) Output | 5 | — | 70 | — | mVp-p |
| Max Output (Limiting) | B-Y<br>R-Y | 12<br>13 | —<br>— | 4.2<br>2.4 | —<br>— | Vp-p<br>Vp-p |
| DC Output | B-Y<br>R-Y | 12<br>13 | —<br>— | 9.2<br>10.1 | —<br>— | V<br>V |
| Output Resistance | B-Y<br>R-Y | 12<br>13 | —<br>— | 100<br>80 | —<br>— | Ω<br>Ω |

FIGURE 2 — BLOCK DIAGRAM



$V_{CC}$
14
Gnd
9
Sandcastle
11
R-Y
13
B-Y
12
Slicer
Color Difference Matrix & Color Killer
Chroma
16
ACC Control
Color Kill Logic
Burst Gate
ACC Filter
17
ACC Det
Filter
Filter
Hue Control
15
Hue Control
Ident Det
U Det
V Det
Color Contrast & Saturation
U
U
U Ref
V
V Ref
Sat Control
2
90° ϕ Det
Burst ϕ Det
Delay Line Driver
90° ϕ Shifter
H/2 Switch
H/2 Switch
H/2 Switch
H/2 Bistable
4.43 MHz VCO
18
1
3
4
5
8
6
7
10
Chroma Delay Line
Ident Filter
V
U
90° Filter
Crystal
VCO Filter

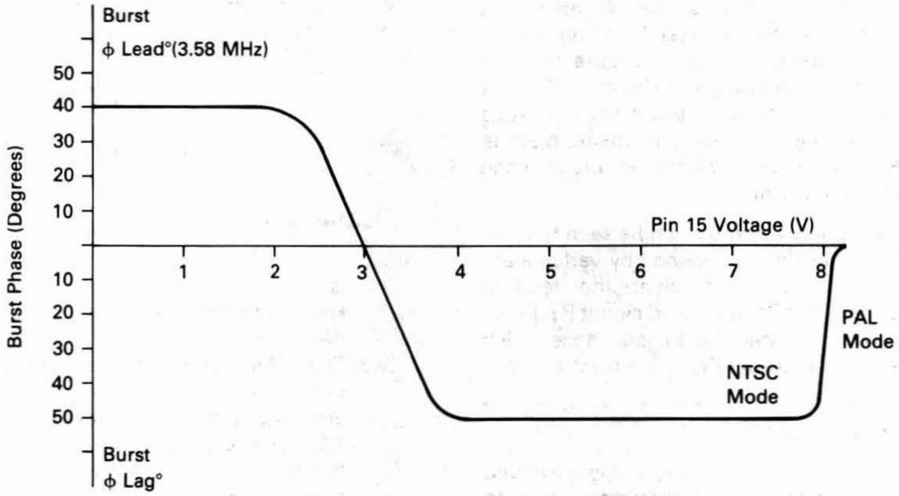
FIGURE 3 — SATURATION CONTROL VOLTAGE



In the case of a misidentified PAL signal Pin 2 is automatically pulled to ground.

Note: Nominal 100% saturation point is given by choice of $R_{17}$ which sets ACC operating point.

FIGURE 4 — HUE CONTROL



Note: Hue control acts only during burst gating with $V_{15}<8$ Volts.

This condition also selects NTSC mode

## CIRCUIT OPERATION

### CHROMINANCE DECODER SECTION

The chrominance decoder consists of the following blocks:

Phase-locked reference oscillator — Figures 5, 6, and 7

Phase-locked 90 degree servo loop — Figures 7 and 8

U and V axis decoders

ACC detector and identification detector — Figure 9

Identification circuits and PAL bistable — Figure 10

Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

- a minimum number of factory adjustments
- a minimum number of external components
- compatibility with the SECAM adapter TDA3030B
- low dissipation
- use of a standard 4.433618 MHz Crystal rather than a 2.0 fc Crystal with divider.

FIGURE 5 — VOLTAGE CONTROLLED OSCILLATOR (VCO)

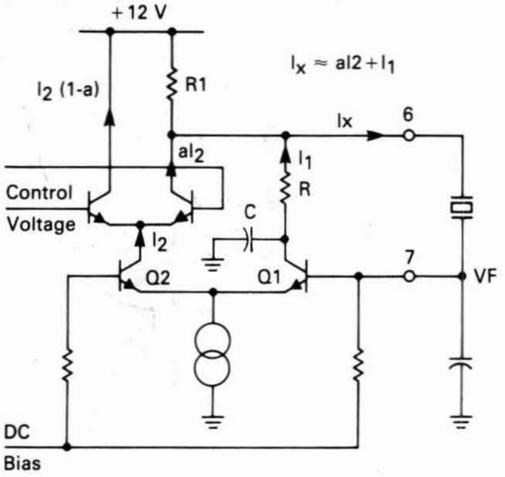
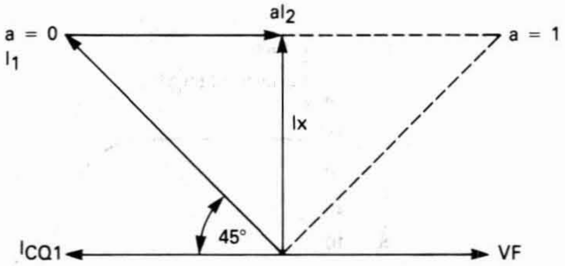


FIGURE 6 — VECTOR DIAGRAM FOR VCO



### REFERENCE REGENERATION

The Crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. A great deal of care was taken to ensure that the oscillator loop gain and the Crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade Crystals (Crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

By referring to Figures 5 and 6 it can be seen that the necessary ±45° phase shift is obtained by variable addition of two currents $I_1$ and $I_2$ which are then fed into the load resistance of the Crystal tuned circuit $R_1$. Feedback is taken from the Crystal load capacitance which gives a voltage VF lagging the Crystal current by 90°.

The RC network in $T_1$ collector causes $I_1$ to lag the collector current of $T_1$ by 45°.

For SECAM operation the currents $I_1$ and $I_2$ are added together in a fixed ratio giving a frequency close to nominal.

When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal/noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not dc. A commutator at the phase detector output also driven from the PAL bistable converts this ac signal to a dc prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC, this cannot be considered to be a serious disadvantage.

## 90° REFERENCE GENERATION

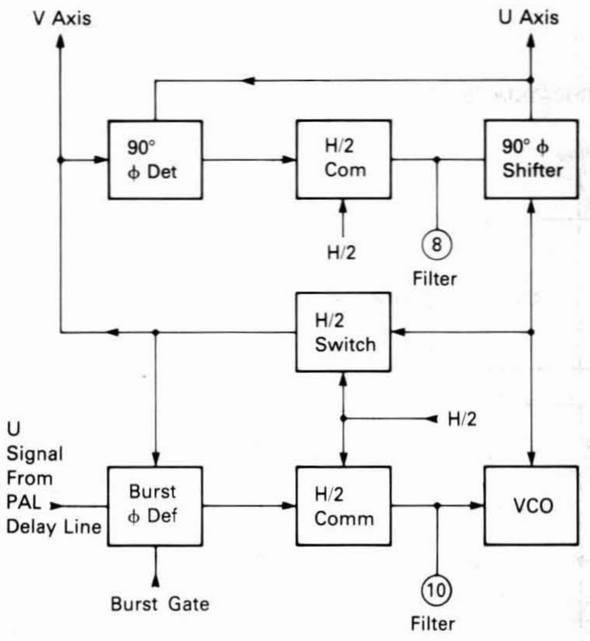


FIGURE 7 — BLOCK DIAGRAM OF REFERENCE SECTION

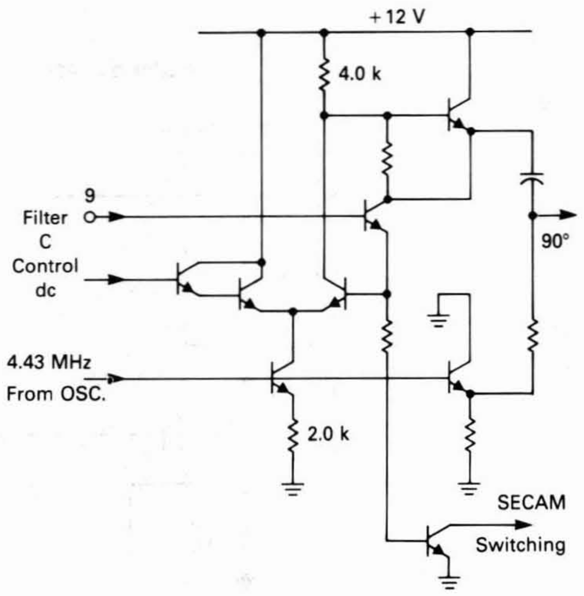


FIGURE 8 — VARIABLE ALL-PASS NETWORK

To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the varible all-pass network (see Figure 8).

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B Adapter.

### ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push-pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

### IDENTIFICATION

| | | | |
|---|---|---|---|
| Monochrome | $I_1 > I_2$ | PAL ident. X | $I_1 > I_2$ |
| PAL ident. OK | $I_1 < I_2$ | NTSC | $I_3 > I_2$ |

Only for correctly identified PAL signal is the capacitor voltage held low since $I_2$ is then greater than $I_1$.

For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage $V_C$ rises with each burst gate pulse.

When $V_{ref}$ is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by $R_1$.

When $V_{ref}$ is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current injected externally on the filter capacitor.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

FIGURE 9 — ACC AND IDENTIFICATION DETECTORS

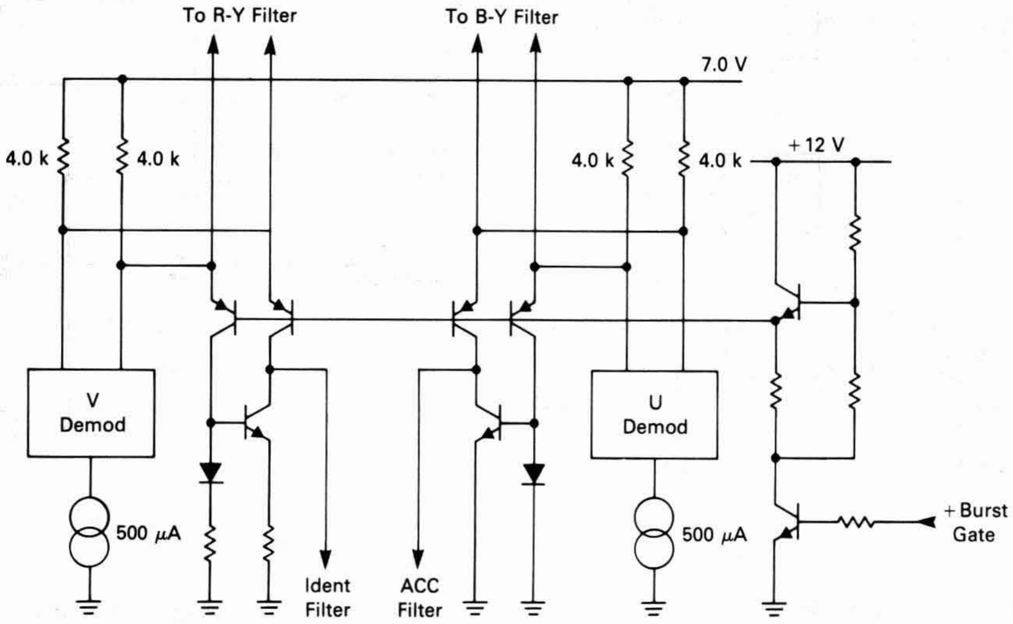
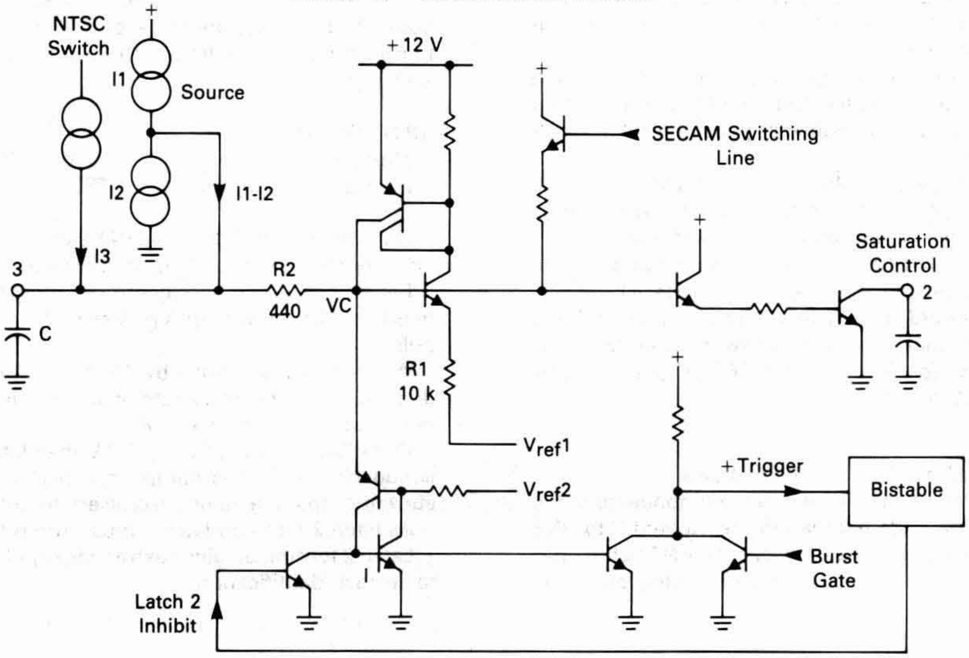

To R-Y Filter
To B-Y Filter
7.0 V
4.0 k
4.0 k
4.0 k
4.0 k
+12 V
V Demod
U Demod
500 μA
500 μA
Ident Filter
ACC Filter
+Burst Gate

FIGURE 10 — IDENTIFICATION CIRCUIT


NTSC Switch
I1
Source
I2
I1-I2
I3
3
C
R2
440
VC
+12 V
R1
10 k
Vref1
Vref2
SECAM Switching Line
Saturation Control
2
+Trigger
Bistable
Burst Gate
Latch 2 Inhibit
I

NTSC switch operates when $V_{15}$<8.0 V.

## COLOR DIFFERENCE MATRIXING, COLOR KILLING, AND CHROMA BLANKING

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

The R-Y and B-Y demodulators have equal conversion gains. The demodulated signals are therefore fed through differential amplifiers with a gain ratio G (B-Y)/G (R-Y) = 1.78 in order to give correctly proportioned B-Y and R-Y signals at the output.

FIGURE 11 — COLOR DIFFERENCE STAGES

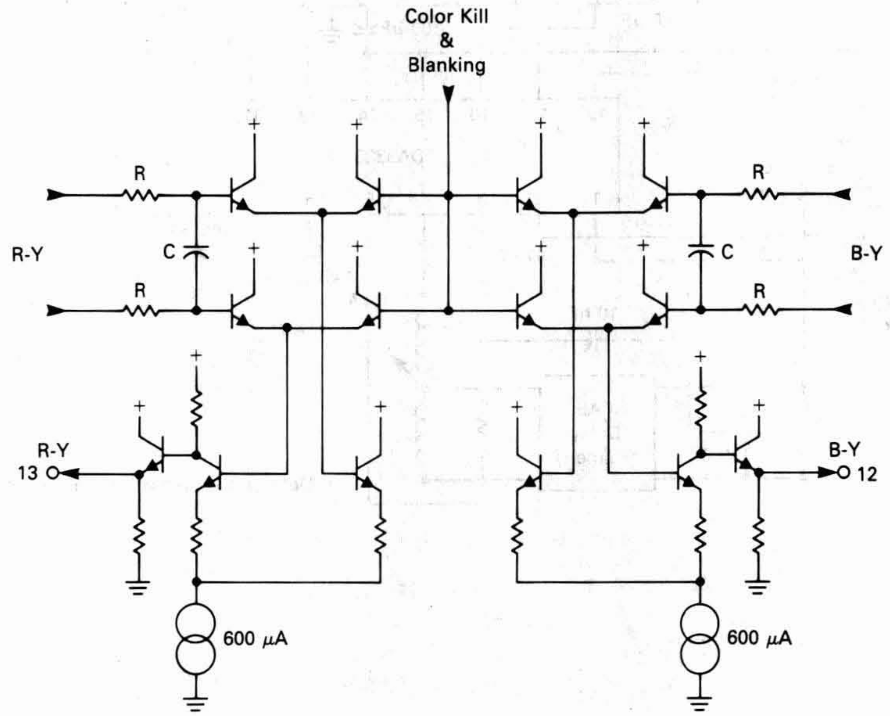
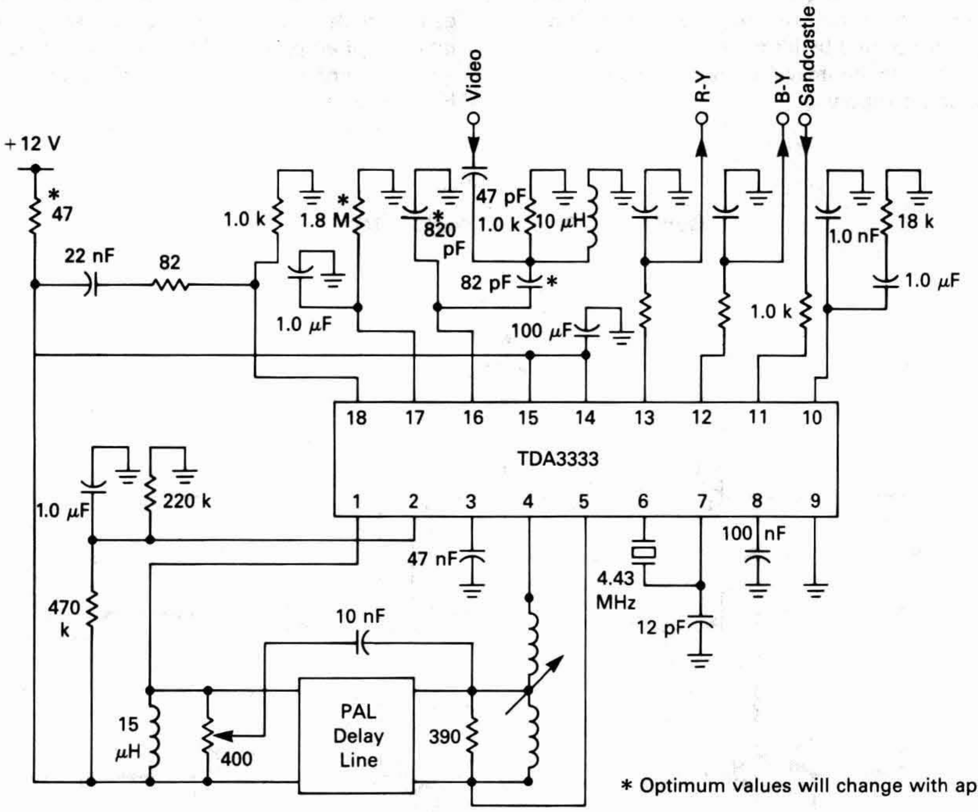
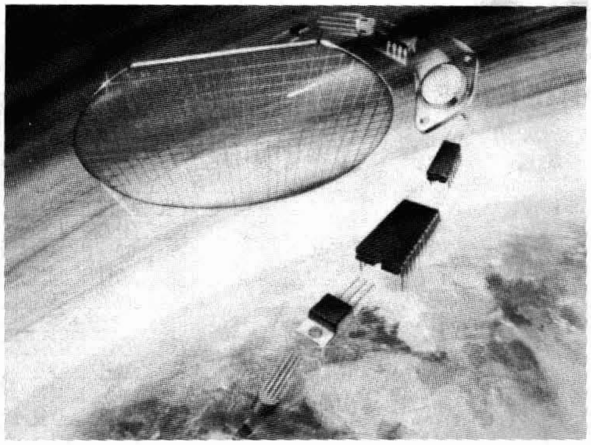


**FIGURE 12 — TYPICAL PAL APPLICATION**


Video
R-Y
B-Y
Sandcastle
+12 V
*
47
22 nF
82
1.0 k
*
1.8 M
*
820 pF
47 pF
1.0 k
10 µH
82 pF
*
1.0 µF
100 µF
1.0 k
1.0 nF
18 k
1.0 µF
18
17
16
15
14
13
12
11
10
TDA3333
1
2
3
4
5
6
7
8
9
1.0 µF
220 k
47 nF
4.43 MHz
100 nF
12 pF
470 k
10 nF
15 µH
400
PAL Delay Line
390

* Optimum values will change with application.

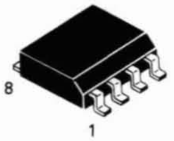


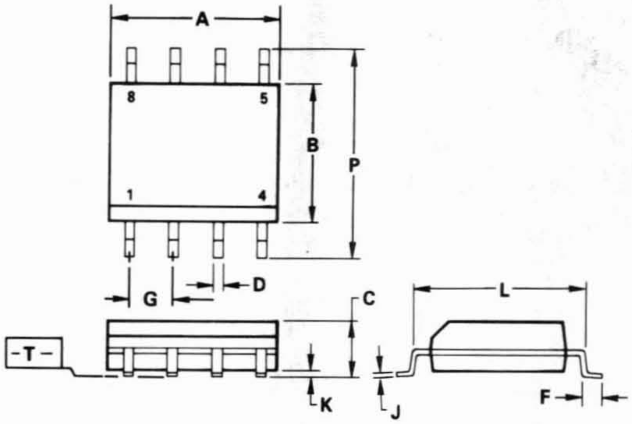
# Packaging Information

## Including Surface Mount Devices (SMD)

# Surface Mount Devices (SMD) Outline Dimensions

**CASE 751-01**
S0-8
Plastic Package
$R_{\theta JA}$ = 180° C/W



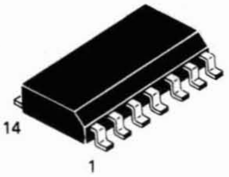


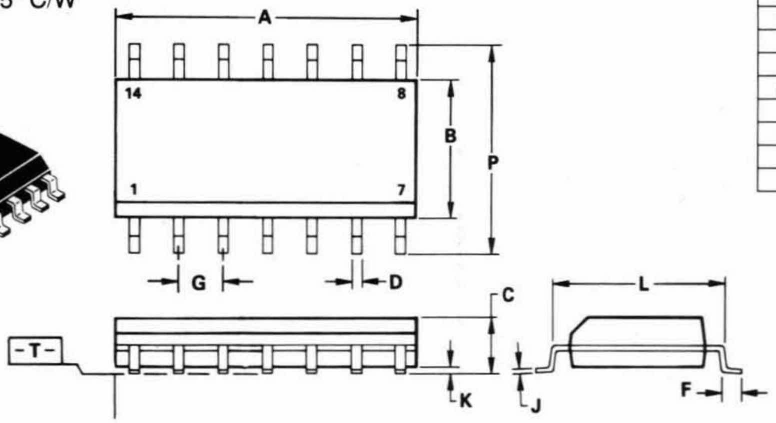
| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 4.78 | 5.00 | 0.188 | 0.197 |
| B | 3.81 | 4.01 | 0.150 | 0.158 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.35 | 0.46 | 0.014 | 0.018 |
| F | 0.67 | 0.77 | 0.026 | 0.030 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.22 | 0.007 | 0.009 |
| K | 0.10 | 0.20 | 0.004 | 0.008 |
| L | 4.82 | 5.21 | 0.189 | 0.205 |
| P | 5.79 | 6.20 | 0.228 | 0.244 |

NOTES:
1. -T- IS SEATING PLANE.
2. DIMENSION A IS DATUM.
3. POSITIONAL TOLERANCE FOR LEADS:

⌖ 0.25 (0.010) Ⓜ A Ⓢ

**CASE 751A-01**
S0-14
Plastic Package
$R_{\theta JA}$ = 145° C/W



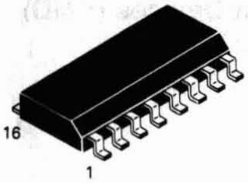


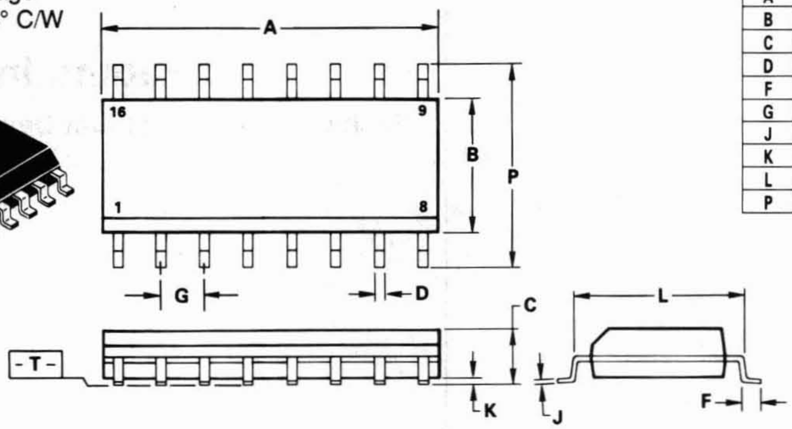
| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 8.54 | 8.74 | 0.336 | 0.344 |
| B | 3.81 | 4.01 | 0.150 | 0.158 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.35 | 0.46 | 0.014 | 0.018 |
| F | 0.67 | 0.77 | 0.026 | 0.030 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.22 | 0.007 | 0.009 |
| K | 0.10 | 0.20 | 0.004 | 0.008 |
| L | 4.82 | 5.21 | 0.189 | 0.205 |
| P | 5.79 | 6.20 | 0.228 | 0.244 |

NOTES:
1. -T- IS SEATING PLANE.
2. DIMENSION A IS DATUM.
3. POSITIONAL TOLERANCE FOR LEADS:

⌖ 0.25 (0.010) Ⓜ A Ⓢ

**CASE 751B-01**
S0-16
Plastic Package
$R_{\theta JA}$ = 135° C/W





| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 9.78 | 10.01 | 0.385 | 0.394 |
| B | 3.81 | 4.01 | 0.150 | 0.158 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.35 | 0.46 | 0.014 | 0.018 |
| F | 0.67 | 0.77 | 0.026 | 0.030 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.22 | 0.007 | 0.009 |
| K | 0.10 | 0.20 | 0.004 | 0.008 |
| L | 4.82 | 5.21 | 0.189 | 0.205 |
| P | 5.79 | 6.20 | 0.228 | 0.244 |

NOTES:
1. -T- IS SEATING PLANE.
2. DIMENSION A IS DATUM.
3. POSITIONAL TOLERANCE FOR LEADS:

⌖ 0.25 (0.010) Ⓜ A Ⓢ

# SMD THERMAL INFORMATION

THE MAXIMUM POWER CONSUMPTION AN INTEGRATED CIRCUIT CAN TOLERATE AT A GIVEN OPERATING AMBIENT TEMPERATURE, CAN BE FOUND FROM THE EQUATION:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)}$$

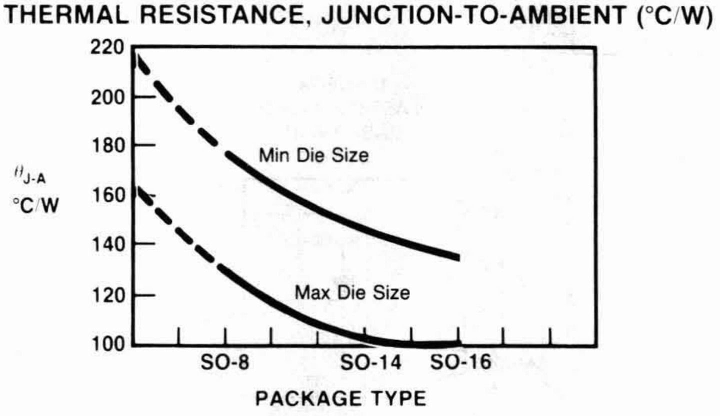
WHERE: $P_{D(T_A)}$ = POWER DISSIPATION ALLOWABLE AT A GIVEN OPERATING AMBIENT TEMPERATURE.

$T_{J(max)}$ = MAXIMUM OPERATING JUNCTION TEMPERATURE AS LISTED IN THE MAXIMUM RATINGS SECTION

$T_A$ = DESIRED OPERATING AMBIENT TEMPERATURE

$R_{\theta JA(Typ)}$ = TYPICAL THERMAL RESISTANCE JUNCTION TO AMBIENT

| RATING | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| OPERATING AMBIENT TEMPERATURE RANGES | $T_A$ | 0 TO +70<br>−40 TO +85 | °C<br>°C |
| OPERATING JUNCTION TEMPERATURE | $T_J$ | +150 | °C |
| STORAGE TEMPERATURE RANGE | $T_{Stg}$ | −55 TO +150 | °C |



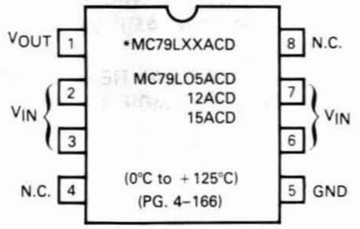
THERMAL RESISTANCE OF SOIC PACKAGES. MEASUREMENT SPECIMENS ARE SOLDER MOUNTED ON PRINTED CIRCUIT CARD 20mm X 32mm X 1.7mm IN STILL AIR. NO AUXILIARY THERMAL CONDUCTION AIDS ARE USED. AS THERMAL RESISTANCE VARIES INVERSELY WITH DIE AREA, A GIVEN PACKAGE TAKES VALUES BETWEEN THE MAX AND MIN VALUES SHOWN WHICH REPRESENT SMALLEST ( 2000 SQUARE MILS) AND LARGEST ( 8000 SQUARE MILS) EXPECTED TO BE ASSEMBLED IN THE SOIC PACKAGE.

# Special Pin Connections

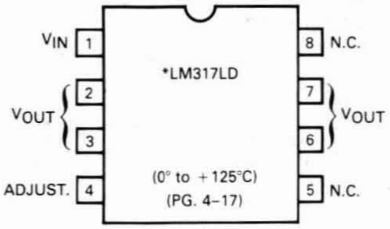
## For Surface Mount Devices (SMD) and Leadless Chip Carriers

### Surface Mount pin-out is different than standard package pin-out for these devices:

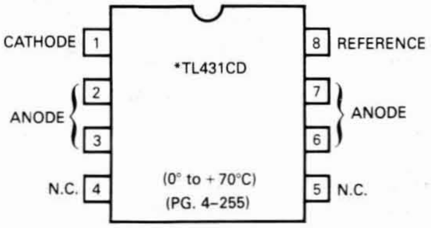
**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SOP-8


VOUT
1
VIN
2
3
N.C.
4
*MC79LXXACD
MC79LO5ACD
12ACD
15ACD
(0°C to +125°C)
(PG. 4–166)
8
N.C.
7
VIN
6
5
GND

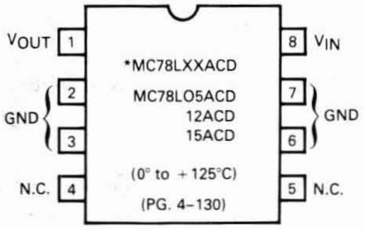
**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SOP-8


VIN
1
VOUT
2
3
ADJUST.
4
*LM317LD
(0° to +125°C)
(PG. 4–17)
8
N.C.
7
VOUT
6
5
N.C.

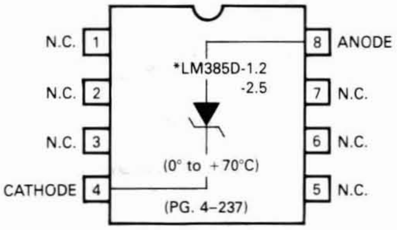
SOP-8


CATHODE
1
ANODE
2
3
N.C.
4
*TL431CD
(0° to +70°C)
(PG. 4–255)
8
REFERENCE
7
ANODE
6
5
N.C.

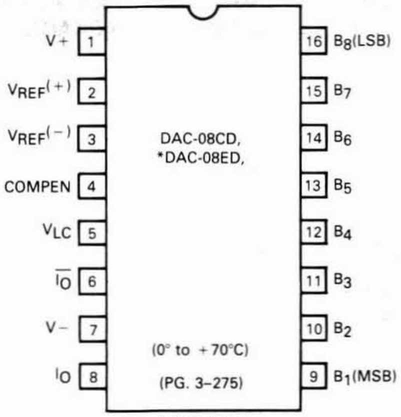
SOP-8


VOUT
1
GND
2
3
N.C.
4
*MC78LXXACD
MC78LO5ACD
12ACD
15ACD
(0° to +125°C)
(PG. 4–130)
8
VIN
7
GND
6
5
N.C.

**D SUFFIX**
PLASTIC PACKAGE
CASE 751-01
SOP-8

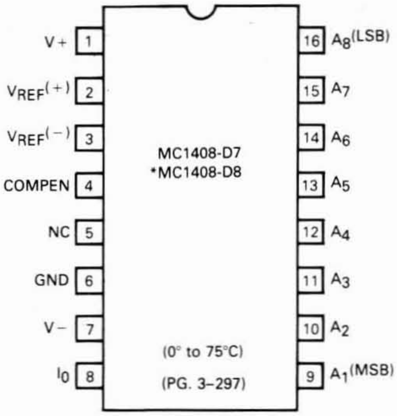

N.C.
1
N.C.
2
N.C.
3
CATHODE
4
*LM385D-1.2
-2.5
(0° to +70°C)
(PG. 4–237)
8
ANODE
7
N.C.
6
N.C.
5
N.C.

**D SUFFIX**
PLASTIC PACKAGE
CASE 751B-01
SO-16


V+
1
VREF(+)
2
VREF(−)
3
COMPEN
4
VLC
5
IO
6
V−
7
IO
8
DAC-08CD,
*DAC-08ED,
(0° to +70°C)
(PG. 3–275)
16
B8(LSB)
15
B7
14
B6
13
B5
12
B4
11
B3
10
B2
9
B1(MSB)

(TOP VIEW)

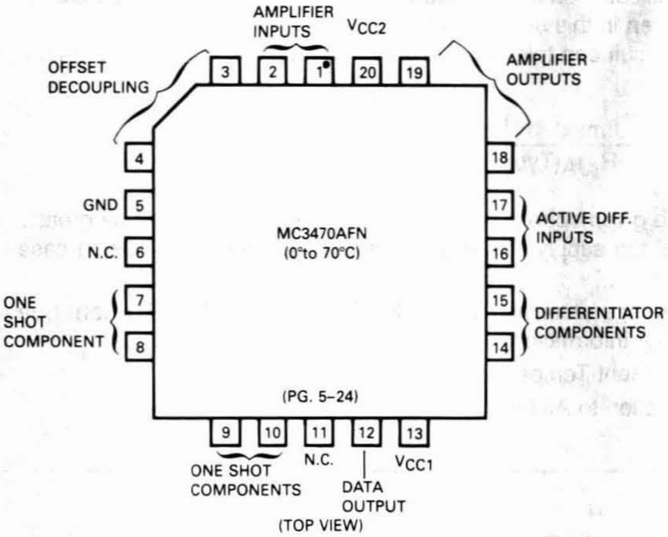
**D SUFFIX**
PLASTIC PACKAGE
CASE 751B-01
SO-16


V+
1
VREF(+)
2
VREF(−)
3
COMPEN
4
NC
5
GND
6
V−
7
IO
8
MC1408-D7
*MC1408-D8
(0° to 75°C)
(PG. 3–297)
16
A8(LSB)
15
A7
14
A6
13
A5
12
A4
11
A3
10
A2
9
A1(MSB)

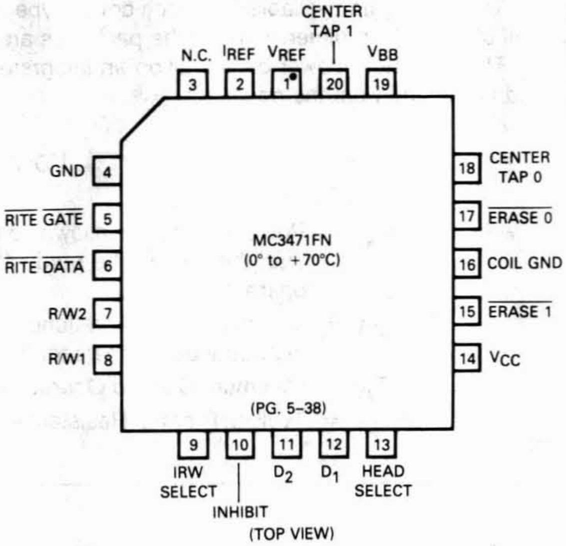
(TOP VIEW)

# SMD OUTLINE DIMENSIONS (continued)

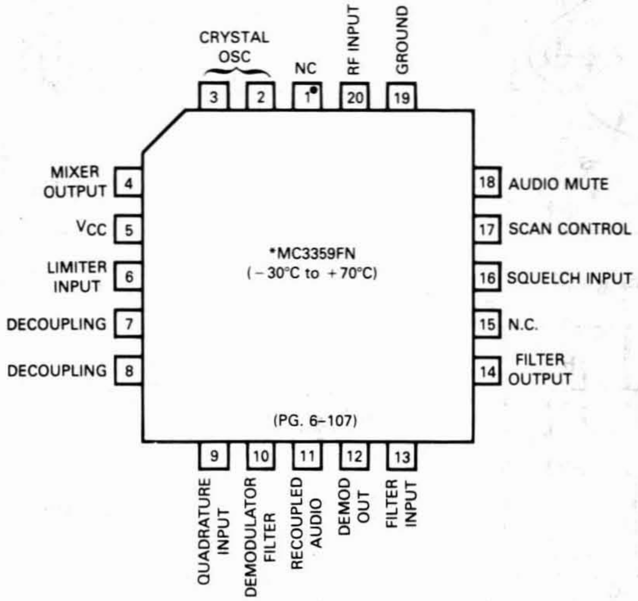
**FN SUFFIX**
PLASTIC PACKAGE
CASE 775-01
PLCC-20


AMPLIFIER INPUTS
$V_{CC2}$
OFFSET DECOUPLING
AMPLIFIER OUTPUTS
3
2
1
20
19
4
GND 5
N.C. 6
ONE SHOT COMPONENT
7
8
18
17
16
ACTIVE DIFF. INPUTS
15
14
DIFFERENTIATOR COMPONENTS
MC3470AFN
(0°to 70°C)
(PG. 5–24)
9
10
11
12
13
ONE SHOT COMPONENTS
N.C.
DATA OUTPUT
$V_{CC1}$
(TOP VIEW)

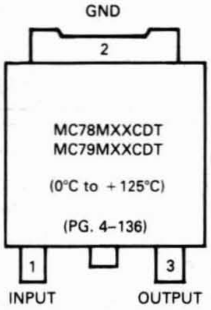
**FN SUFFIX**
PLASTIC PACKAGE
CASE 775-01
PLCC-20


CENTER TAP 1
N.C.
$I_{REF}$
$V_{REF}$
$V_{BB}$
3
2
1
20
19
GND 4
RITE GATE 5
RITE DATA 6
R/W2 7
R/W1 8
18 CENTER TAP 0
17 ERASE 0
16 COIL GND
15 ERASE 1
14 $V_{CC}$
MC3471FN
(0° to +70°C)
(PG. 5–38)
9
10
11
12
13
IRW SELECT
INHIBIT
$D_2$
$D_1$
HEAD SELECT
(TOP VIEW)

**FN SUFFIX**
PLASTIC PACKAGE
CASE 775-01
PLCC-20


CRYSTAL OSC
NC
RF INPUT
GROUND
3
2
1
20
19
MIXER OUTPUT 4
$V_{CC}$ 5
LIMITER INPUT 6
DECOUPLING 7
DECOUPLING 8
18 AUDIO MUTE
17 SCAN CONTROL
16 SQUELCH INPUT
15 N.C.
14 FILTER OUTPUT
*MC3359FN
(−30°C to +70°C)
(PG. 6–107)
9
10
11
12
13
QUADRATURE INPUT
DEMODULATOR FILTER
RECOUPLED AUDIO
DEMOD OUT
FILTER INPUT

**DT SUFFIX**
PLASTIC PACKAGE
CASE 369A-01
D-PAK


GND
2
MC78MXXCDT
MC79MXXCDT
(0°C to +125°C)
(PG. 4–136)
1
3
INPUT
OUTPUT

# Case Outline Dimensions

The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)}$$

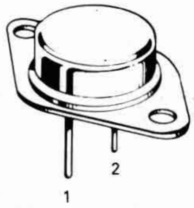
where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

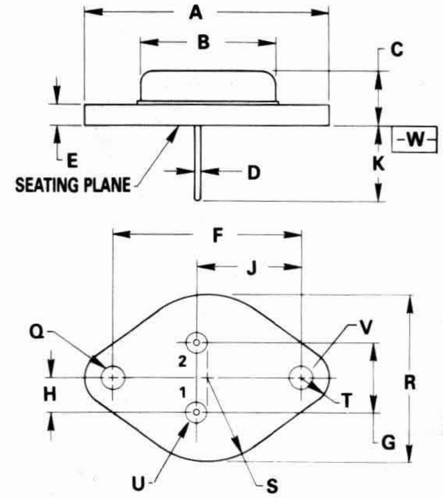
$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for $T_{J(max)}$ information.

$T_A$ = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

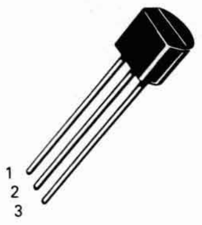
**CASE 1-03**
TO-204AA
(TO-3)
Metal Package
$R_{\theta JA}$ = 45° C/W(Typ)
$R_{\theta JC}$ = See Data Sheet

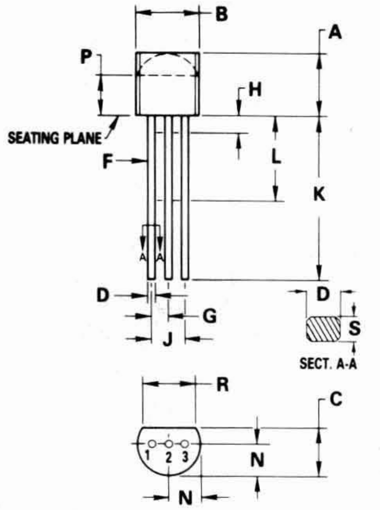




| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| B | — | 22.23 | — | 0.875 |
| C | 6.35 | 11.43 | 0.250 | 0.450 |
| D | 0.97 | 1.09 | 0.038 | 0.043 |
| E | — | 3.43 | — | 0.135 |
| F | 30.15 BSC | | 1.187 BSC | |
| G | 10.92 BSC | | 0.430 BSC | |
| H | 5.46 BSC | | 0.215 BSC | |
| J | 16.89 BSC | | 0.665 BSC | |
| K | 7.92 | — | 0.312 | — |
| Q | 3.84 | 4.09 | 0.151 | 0.161 |
| S | — | 13.34 | — | 0.525 |
| T | — | 4.78 | — | 0.188 |
| V | 3.84 | 4.09 | 0.151 | 0.161 |

**CASE 29-02**
TO-226AA
(TO-92)
Plastic Package
$R_{\theta JA}$ = 200° C/W



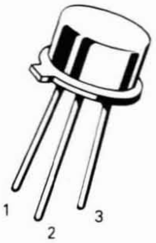


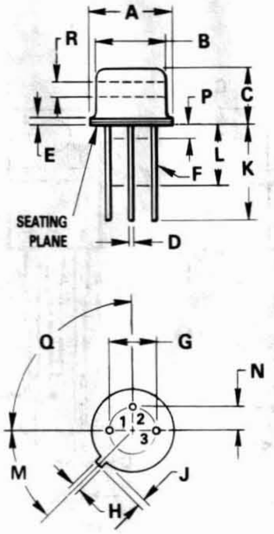
| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.32 | 5.33 | 0.170 | 0.210 |
| B | 4.44 | 5.21 | 0.175 | 0.205 |
| C | 3.18 | 4.19 | 0.125 | 0.165 |
| D | 0.41 | 0.56 | 0.016 | 0.022 |
| F | 0.41 | 0.48 | 0.016 | 0.019 |
| G | 1.14 | 1.40 | 0.045 | 0.055 |
| H | — | 2.54 | — | 0.100 |
| J | 2.41 | 2.67 | 0.095 | 0.105 |
| K | 12.70 | — | 0.500 | — |
| L | 6.35 | — | 0.250 | — |
| N | 2.03 | 2.67 | 0.080 | 0.105 |
| P | 2.92 | — | 0.115 | — |
| R | 3.43 | — | 0.135 | — |
| S | 0.36 | 0.41 | 0.014 | 0.016 |

# CASE OUTLINE DIMENSIONS (continued)

## CASE 79-02

TO-205AD
(TO-39)
Metal Package
$R_{\theta JA}$ = 185° C/W(Typ)

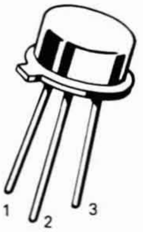


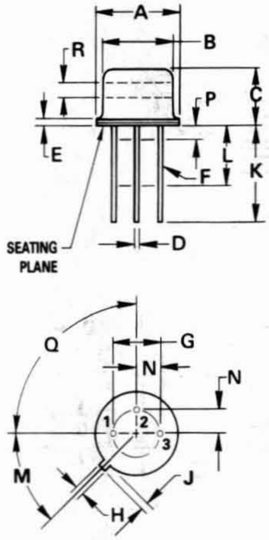

A
R
B
P
C
E
L
K
F
SEATING PLANE
D
Q
G
N
1
2
3
M
J
H

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 8.89 | 9.40 | 0.350 | 0.370 |
| B | 8.00 | 8.51 | 0.315 | 0.335 |
| C | 6.10 | 6.60 | 0.240 | 0.260 |
| D | 0.406 | 0.533 | 0.016 | 0.021 |
| E | 0.229 | 3.18 | 0.009 | 0.125 |
| F | 0.406 | 0.483 | 0.016 | 0.019 |
| G | 4.83 | 5.33 | 0.190 | 0.210 |
| H | 0.711 | 0.864 | 0.028 | 0.034 |
| J | 0.737 | 1.02 | 0.029 | 0.040 |
| K | 12.70 | — | 0.500 | — |
| L | 6.35 | — | 0.250 | — |
| M | 45° NOM | | 45° NOM | |
| P | — | 1.27 | — | 0.050 |
| Q | 90° NOM | | 90° NOM | |
| R | 2.54 | — | 0.100 | — |

## CASE 79-03

TO-205AD
(TO-39)
Metal Package
$R_{\theta JA}$ = 185° C/W (Typ)

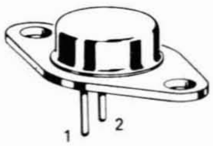


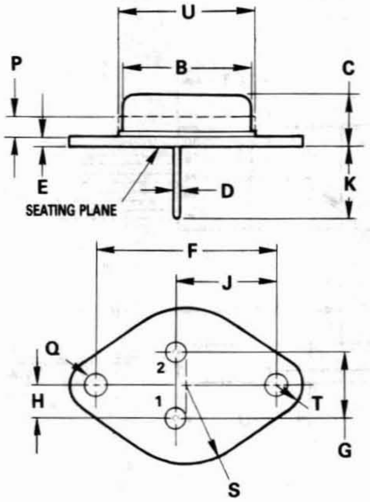

A
R
B
P
C
E
L
K
F
SEATING PLANE
D
Q
G
N
N
1
2
3
M
J
H

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 9.02 | 9.30 | 0.355 | 0.366 |
| B | 8.00 | 8.51 | 0.315 | 0.335 |
| C | 4.19 | .57 | 0.165 | 0.180 |
| D | 0.43 | 0.53 | 0.017 | 0.021 |
| E | 0.43 | 0.89 | 0.017 | 0.035 |
| F | 0.41 | 0.48 | 0.016 | 0.019 |
| G | 4.83 | 5.33 | 0.190 | 0.210 |
| H | 0.71 | 0.86 | 0.028 | 0.034 |
| J | 0.74 | 1.02 | 0.029 | 0.040 |
| K | 12.70 | — | 0.500 | — |
| M | 45°NOM | | 45°NOM | |
| N | 2.54 TYP | | 0.100 TYP | |
| Q | 90° NOM | | 90° NOM | |

## CASE 80-02

TO-213AA
(TO-66)
Metal Package
$R_{\theta JA}$ = 45°C/W(Typ)
$R_{\theta JC}$ = See Data Sheet



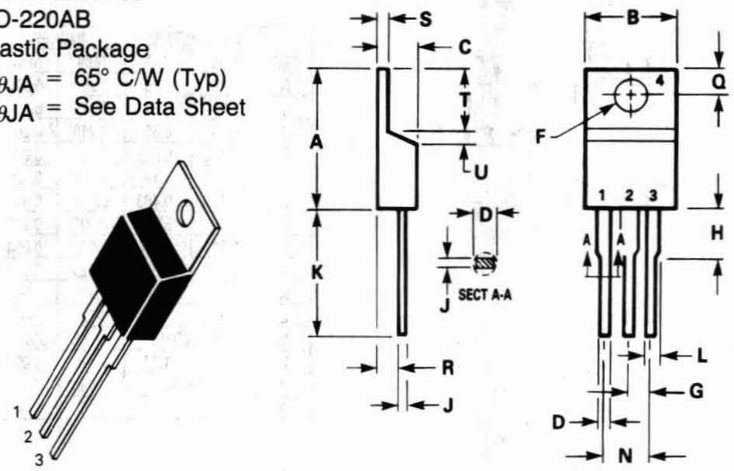

U
P
B
C
E
SEATING PLANE
D
K
F
J
Q
2
1
H
T
G
S

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| B | 11.94 | 12.70 | 0.470 | 0.500 |
| C | 6.35 | 8.64 | 0.250 | 0.340 |
| D | 0.71 | 0.86 | 0.028 | 0.034 |
| E | 1.27 | 1.91 | 0.050 | 0.075 |
| F | 24.33 | 24.43 | 0.958 | 0.962 |
| G | 4.83 | 5.33 | 0.190 | 0.210 |
| H | 2.41 | 2.67 | 0.095 | 0.105 |
| J | 14.48 | 14.99 | 0.570 | 0.590 |
| K | 9.14 | — | 0.360 | — |
| P | — | 1.27 | — | 0.050 |
| Q | 3.61 | 3.86 | 0.142 | 0.152 |
| S | — | 8.89 | — | 0.350 |
| T | — | 3.68 | — | 0.145 |
| U | — | 15.75 | — | 0.620 |

## CASE OUTLINE DIMENSIONS (continued)

### CASE 221A-03

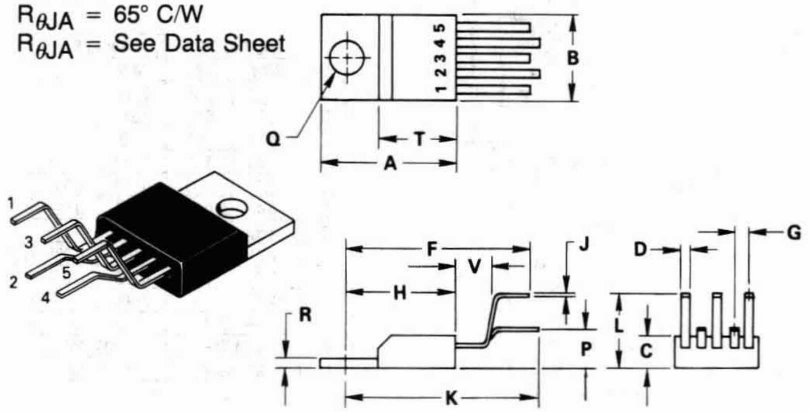
TO-220AB
Plastic Package
$R_{\theta JA}$ = 65° C/W (Typ)
$R_{\theta JA}$ = See Data Sheet



| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 14.23 | 15.87 | 0.560 | 0.625 |
| B | 9.66 | 10.66 | 0.380 | 0.420 |
| C | 3.56 | 4.82 | 0.140 | 0.190 |
| D | 0.51 | 1.14 | 0.020 | 0.045 |
| F | 3.531 | 3.937 | 0.139 | 0.155 |
| G | 2.29 | 2.79 | 0.090 | 0.110 |
| H | — | 7.11 | — | 0.280 |
| J | 0.31 | 1.14 | 0.012 | 0.045 |
| K | 12.70 | 14.73 | 0.500 | 0.580 |
| L | 1.14 | 1.77 | 0.045 | 0.070 |
| N | 4.83 | 5.33 | 0.190 | 0.210 |
| Q | 2.54 | 3.04 | 0.100 | 0.135 |
| R | 2.04 | 2.92 | 0.080 | 0.115 |
| S | 0.51 | 1.39 | 0.020 | 0.055 |
| T | 5.59 | 6.85 | 0.220 | 0.270 |
| U | 0.00 | 1.27 | 0.000 | 0.050 |

### CASE 314B-01

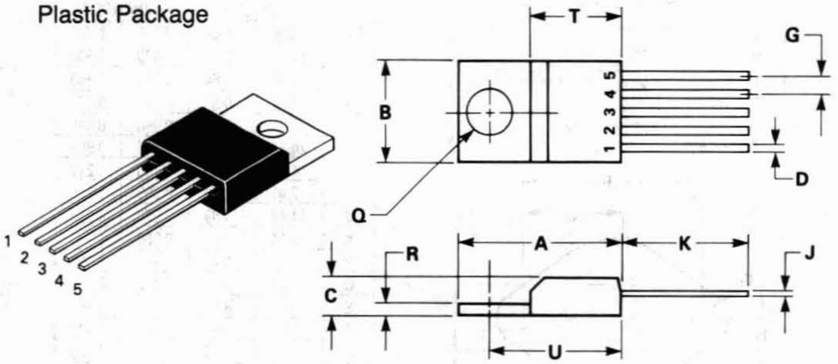
Plastic Package
$R_{\theta JA}$ = 65° C/W
$R_{\theta JA}$ = See Data Sheet



| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 15.49 | 15.88 | 0.610 | 0.625 |
| B | 9.91 | 10.41 | 0.390 | 0.410 |
| C | 4.32 | 4.57 | 0.170 | 0.180 |
| D | 0.71 | 0.81 | 0.028 | 0.032 |
| F | 20.83 | 21.59 | 0.820 | 0.850 |
| G | 1.45 | 1.96 | 0.057 | 0.077 |
| H | 12.70 | 13.69 | 0.500 | 0.539 |
| J | 0.38 | 0.64 | 0.015 | 0.025 |
| K | 21.46 | 23.50 | 0.845 | 0.925 |
| L | 8.00 | 8.38 | 0.315 | 0.330 |
| P | 4.32 | 4.70 | 0.170 | 0.185 |
| Q | 3.53 | 3.73 | 0.139 | 0.147 |
| R | 0.89 | 1.40 | 0.035 | 0.055 |
| T | 9.02 | 9.40 | 0.355 | 0.370 |
| V | 4.70 | 5.46 | 0.185 | 0.215 |

### CASE 314D-01

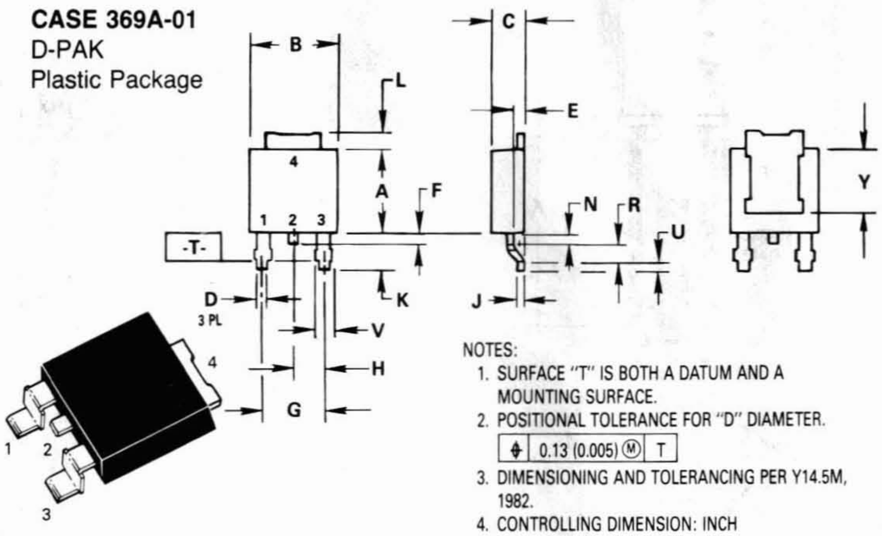
TO-220AB
Plastic Package



| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 15.49 | 15.87 | 0.610 | 0.625 |
| B | 9.91 | 10.41 | 0.390 | 0.410 |
| C | 4.32 | 4.57 | 0.170 | 0.180 |
| D | 0.51 | 1.01 | 0.020 | 0.040 |
| G | 1.45 | 1.96 | 0.057 | 0.077 |
| J | 0.38 | 0.63 | 0.015 | 0.025 |
| K | 12.70 | — | 0.500 | — |
| Q | 3.53 | 3.73 | 0.139 | 0.147 |
| R | 0.89 | 1.39 | 0.035 | 0.055 |
| T | 9.02 | 9.39 | 0.355 | 0.370 |
| U | 12.70 | 13.69 | 0.500 | 0.539 |

## CASE OUTLINE DIMENSIONS (continued)

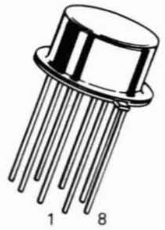
**CASE 369A-01**
D-PAK
Plastic Package

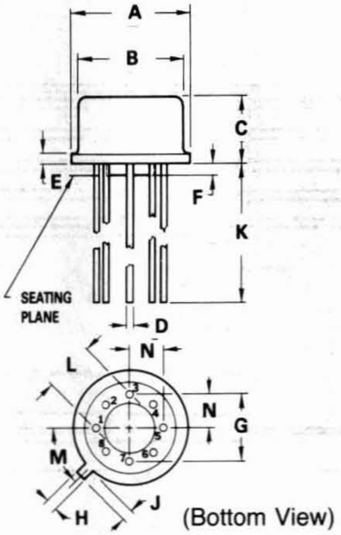


NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
⌖ | 0.13 (0.005) Ⓜ | T
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 5.97 | 6.19 | 0.235 | 0.245 |
| B | 6.35 | 6.73 | 0.250 | 0.265 |
| C | 2.18 | 2.38 | 0.086 | 0.094 |
| D | 0.69 | 0.88 | 0.027 | 0.035 |
| E | 0.89 | 1.14 | 0.035 | 0.045 |
| F | 0.64 | 0.88 | 0.025 | 0.035 |
| G | 4.57 BSC | | 0.180 BSC | |
| H | 2.87 BSC | | 0.090 BSC | |
| J | 6.46 | 0.58 | 0.018 | 0.023 |
| K | 2.59 | 2.89 | 0.102 | 0.114 |
| L | 0.89 | 1.27 | 0.035 | 0.050 |
| N | 0.81 | 1.11 | 0.032 | 0.044 |
| R | 1.07 | 1.37 | 0.042 | 0.054 |
| S | 5.21 | 5.46 | 0.205 | 0.215 |
| U | 0.51 | — | 0.020 | — |
| V | 0.76 | 1.14 | 0.030 | 0.045 |
| W | 0.48 | 0.55 | 0.019 | 0.022 |
| Y | 4.32 | — | 0.170 | — |

**CASE 601-04**
Metal Package
$R_{\theta JA}$ = 160° C/W(Typ)

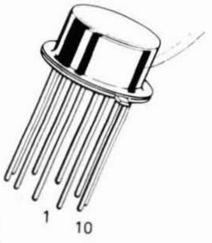


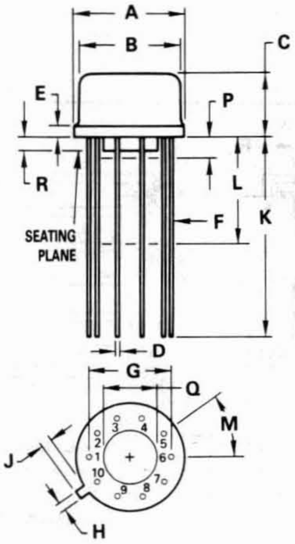


(Bottom View)

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 8.51 | 9.40 | 0.335 | 0.370 |
| B | 7.75 | 8.51 | 0.305 | 0.335 |
| C | 4.19 | 4.70 | 0.165 | 0.185 |
| D | 0.41 | 0.48 | 0.016 | 0.019 |
| E | 0.25 | 1.02 | 0.010 | 0.040 |
| F | 0.25 | 1.02 | 0.010 | 0.040 |
| G | 5.08 BSC | | 0.200 BSC | |
| H | 0.71 | 0.86 | 0.028 | 0.034 |
| J | 0.74 | 1.14 | 0.029 | 0.045 |
| K | 12.70 | — | 0.500 | — |
| L | 3.05 | 4.06 | 0.120 | 0.160 |
| M | 45° BSC | | 45° BSC | |
| N | 2.41 | 2.67 | 0.095 | 0.105 |

**CASE 603-04**
TO-100
Metal Can
$R_{\theta JA}$ = 160° C/W

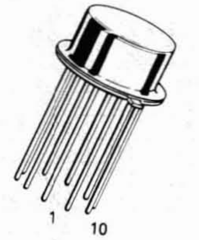


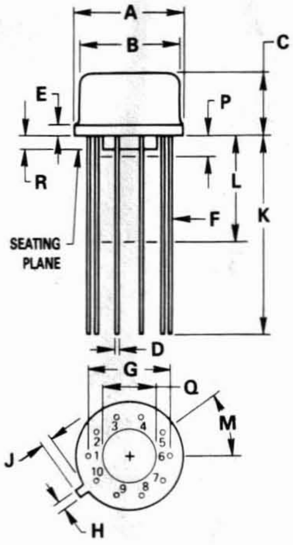


| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 8.51 | 9.39 | 0.335 | 0.370 |
| B | 7.75 | 8.51 | 0.305 | 0.335 |
| C | 4.19 | 4.70 | 0.165 | 0.185 |
| D | 0.407 | 0.533 | 0.016 | 0.021 |
| E | — | 1.02 | — | 0.040 |
| F | 0.406 | 0.483 | 0.016 | 0.019 |
| G | 5.84 BSC | | 0.230 BSC | |
| H | 0.712 | 0.864 | 0.028 | 0.034 |
| J | 0.737 | 1.14 | 0.029 | 0.045 |
| K | 12.70 | — | 0.500 | — |
| L | 6.35 | 12.70 | 0.250 | 0.500 |
| M | 36° BSC | | 36° BSC | |
| P | — | 1.27 | — | 0.050 |
| Q | 3.56 | 4.06 | 0.140 | 0.160 |
| R | 0.254 | 1.02 | 0.010 | 0.040 |

# CASE OUTLINE DIMENSIONS (continued)

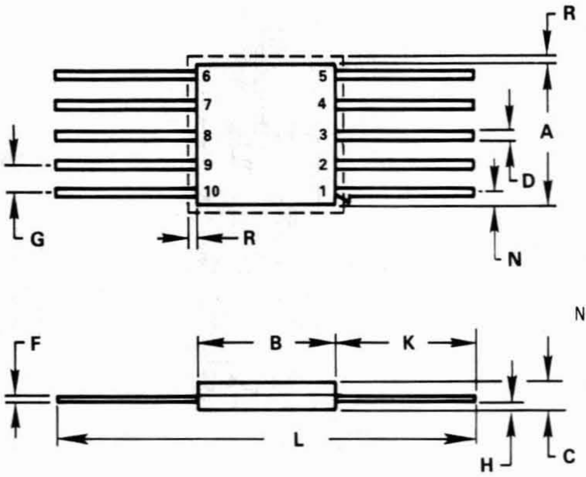
## CASE 603C-01
TO-100 Type
$R_{\theta JA}$ = 150° C/W(Typ)

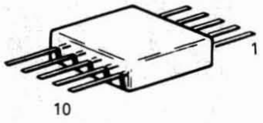




| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 8.51 | 9.39 | 0.335 | 0.370 |
| B | 7.75 | 8.51 | 0.305 | 0.335 |
| C | 4.19 | 6.73 | 0.165 | 0.265 |
| D | 0.407 | 0.533 | 0.016 | 0.021 |
| E | — | 1.02 | — | 0.040 |
| F | 0.406 | 0.483 | 0.016 | 0.019 |
| G | 5.84 BSC |  | 0.230 BSC |  |
| H | 0.712 | 0.864 | 0.028 | 0.034 |
| J | 0.737 | 1.14 | 0.029 | 0.045 |
| K | 12.70 | — | 0.500 | — |
| L | 6.35 | 12.70 | 0.250 | 0.500 |
| M | 36° BSC |  | 36° BSC |  |
| P | — | 1.27 | — | 0.050 |
| Q | 3.56 | 4.06 | 0.140 | 0.160 |
| R | 0.254 | 1.02 | 0.010 | 0.040 |

## CASE 606-04
TO-91
Ceramic Package
$R_{\theta JA}$ = 165° C/W(Typ)

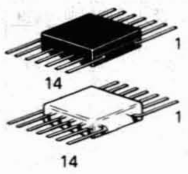


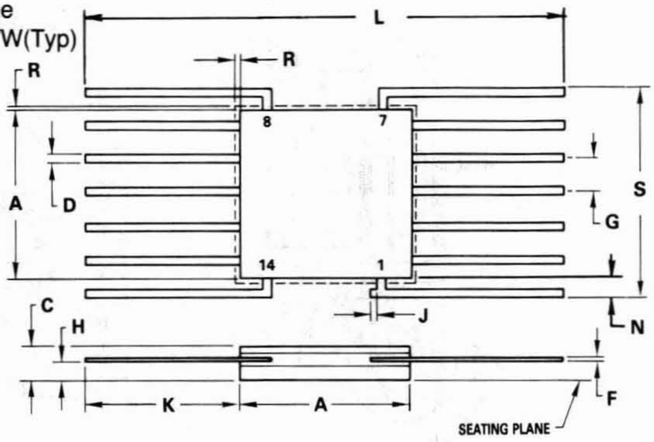


| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 6.10 | 7.36 | 0.240 | 0.290 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 0.762 | 1.77 | 0.030 | 0.070 |
| D | 0.254 | 0.482 | 0.010 | 0.019 |
| F | 0.077 | 0.152 | 0.003 | 0.006 |
| G | 1.15 | 1.39 | 0.045 | 0.055 |
| H | 0.127 | 0.889 | 0.005 | 0.035 |
| K | 1.78 | — | 0.070 | — |
| R | — | 0.381 | — | 0.015 |

NOTE:
1. ALL RULES & NOTES ASSOCIATED WITH TO-91 OUTLINE SHALL APPLY.
2. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION (AT BODY)

## CASE 607-05
TO-86 Type
Ceramic Package
$R_{\theta JA}$ = 165° C/W(Typ)





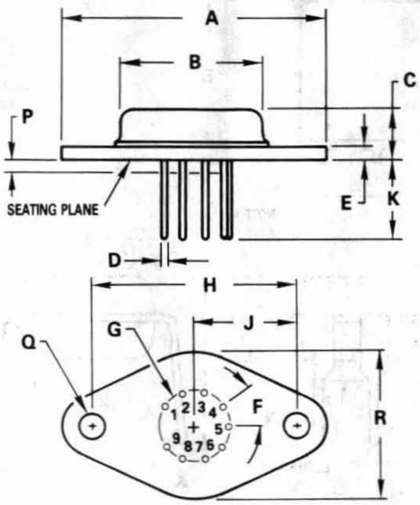
| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 0.76 | 1.78 | 0.030 | 0.070 |
| D | 0.33 | 0.48 | 0.013 | 0.019 |
| F | 0.08 | 0.15 | 0.003 | 0.006 |
| G | 1.27 BSC |  | 0.050 BSC |  |
| H | 0.30 | 0.89 | 0.012 | 0.035 |
| J | — | 0.38 | — | 0.015 |
| K | 6.35 | 9.40 | 0.250 | 0.370 |
| L | 18.80 | — | 0.740 | — |
| N | 0.25 | — | 0.010 | — |
| R | — | 0.38 | — | 0.015 |
| S | 7.62 | 8.38 | 0.300 | 0.330 |

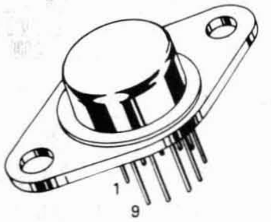
NOTES:
1. "R" DIMENSIONS DETERMINE ZONE WITHIN WHICH ALL BODY AND LEAD IRREGULARITIES LIE.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION RELATIVE TO "A" AT MAXIMUM MATERIAL CONDITION.

## CASE OUTLINE DIMENSIONS (continued)

### CASE 614-02

(TO-66 Type)
Metal Package
$R_{\theta JA}$ = 35° C/W(Typ)
$R_{\theta JC}$ = See Data Sheet





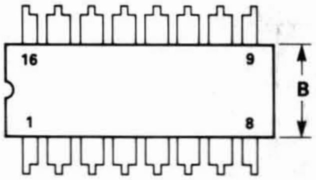
| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | — | 31.80 | — | 1.252 |
| B | 11.94 | 12.70 | 0.470 | 0.500 |
| C | 6.35 | 8.64 | 0.250 | 0.340 |
| D | 0.71 | 0.81 | 0.028 | 0.032 |
| E | 1.27 | 1.90 | 0.050 | 0.075 |
| F | 36° BSC |  | 36° BSC |  |
| G | 8.26 BSC |  | 0.325 BSC |  |
| H | 24.33 | 24.43 | 0.958 | 0.962 |
| J | 12.17 | 12.22 | 0.479 | 0.481 |
| K | 9.14 | — | 0.360 | — |
| P | 1.40 BSC |  | 0.055 BSC |  |
| Q | 3.61 | 3.86 | 0.142 | 0.152 |
| R | — | 17.78 | — | 0.700 |

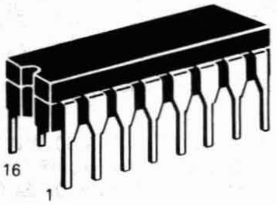
NOTE:

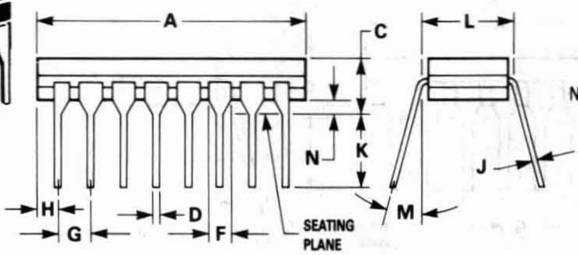
1. LEADS TRUE POSITIONED WITHIN 0.36 mm (0.014) DIA. to DIM. "A" & "H" AT MAX. MATERIAL CONDITIONS AND DIM. "P"
2. LEAD DIAMETERS ARE UNCONTROLLED BEYOND 12.70 mm (0.500) FROM BASE PLANE.

### CASE 620-02

Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)







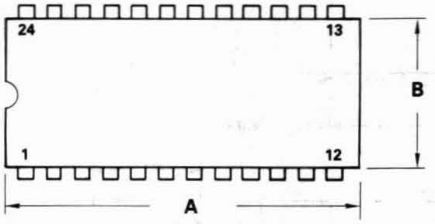
| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 19.05 | 19.81 | 0.750 | 0.780 |
| B | 6.22 | 6.98 | 0.245 | 0.275 |
| C | 4.06 | 5.08 | 0.160 | 0.200 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.40 | 1.65 | 0.055 | 0.065 |
| G | 2.54 BSC |  | 0.100 BSC |  |
| H | 0.51 | 1.14 | 0.020 | 0.045 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 4.06 | 0.125 | 0.160 |
| L | 7.37 | 7.87 | 0.290 | 0.310 |
| M | — | 15° | — | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

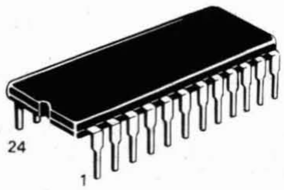
NOTES:

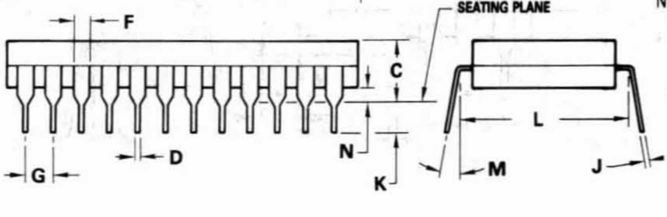
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

### CASE 623-05

Ceramic Package
$R_{\theta JA}$ = 53° C/W(Typ)







| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 31.24 | 32.77 | 1.230 | 1.290 |
| B | 12.70 | 15.49 | 0.500 | 0.610 |
| C | 4.06 | 5.59 | 0.160 | 0.220 |
| D | 0.41 | 0.51 | 0.016 | 0.020 |
| F | 1.27 | 1.52 | 0.050 | 0.060 |
| G | 2.54 BSC |  | 0.100 BSC |  |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 4.06 | 0.125 | 0.160 |
| L | 15.24 BSC |  | 0.600 BSC |  |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.27 | 0.020 | 0.050 |

NOTES:

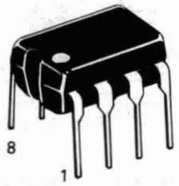
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

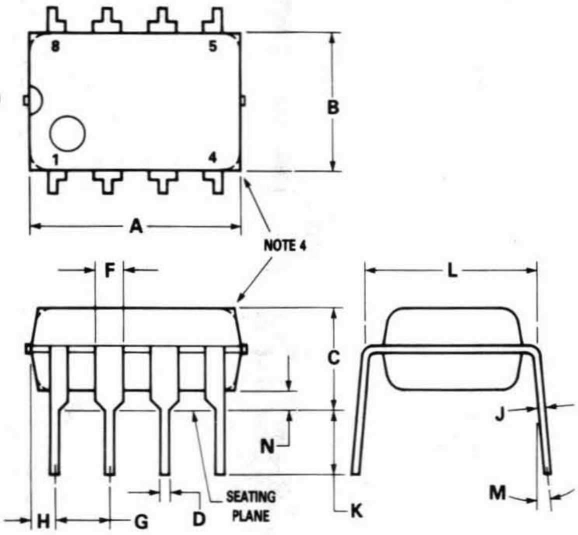
# CASE OUTLINE DIMENSIONS (continued)

### CASE 626-04

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 9.40 | 10.16 | 0.370 | 0.400 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.94 | 4.45 | 0.155 | 0.175 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.76 | 1.27 | 0.030 | 0.050 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | — | 10° | — | 10° |
| N | 0.51 | 0.76 | 0.020 | 0.030 |

NOTES:

1. LEAD POSITIONAL TOLERANCE:
   ⊕ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

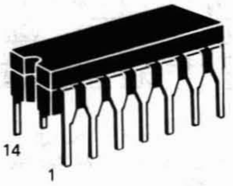
### CASE 632-02

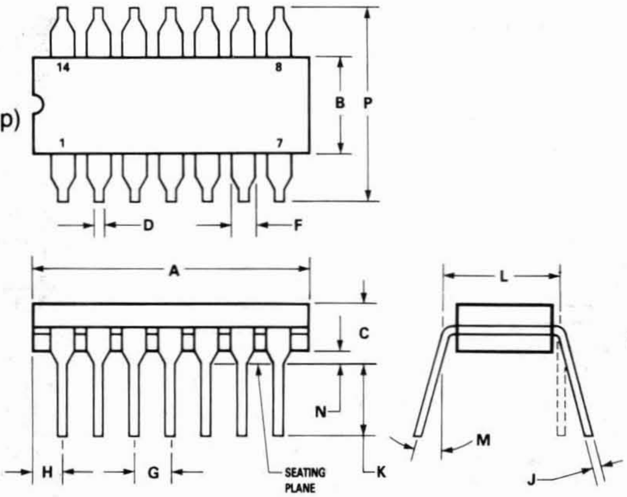
MO-001AA

(TO-116)

Ceramic Package

$R_{\theta JA}$ = 100° C/W(Typ)





| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 16.8 | 19.9 | 0.660 | 0.785 |
| B | 5.59 | 7.11 | 0.220 | 0.280 |
| C | — | 5.08 | — | 0.200 |
| D | 0.381 | 0.584 | 0.015 | 0.023 |
| F | 0.77 | 1.77 | 0.030 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.203 | 0.381 | 0.008 | 0.015 |
| K | 2.54 | — | 0.100 | — |
| L | 7.62 BSC | | 0.300 BSC | |
| M | — | 15° | — | 15° |
| N | 0.51 | 0.76 | 0.020 | 0.030 |
| P | — | 8.25 | — | 0.325 |

All JEDEC dimensions and notes apply.

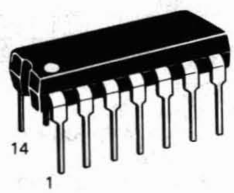
NOTES:

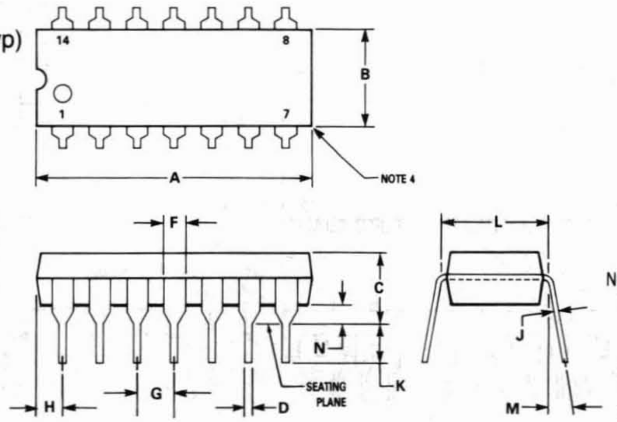
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

### CASE 646-05

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





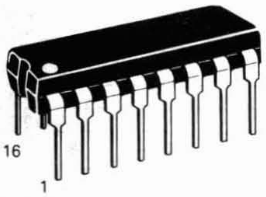
| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 18.16 | 19.56 | 0.715 | 0.770 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 4.06 | 5.08 | 0.160 | 0.200 |
| D | 0.38 | 0.53 | 0.015 | 0.021 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.32 | 2.41 | 0.052 | 0.095 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 10° | 0° | 10° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

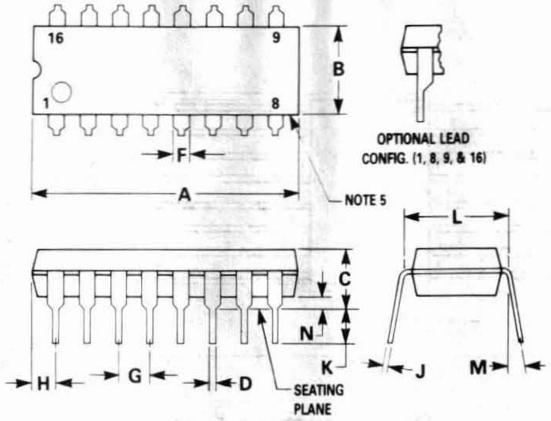
NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL; AS SHOWN IN PREVIOUS ISSUE.

# CASE OUTLINE DIMENSIONS (continued)

**CASE 648-05**
Plastic Package
$R_{\theta JA}$ = 100° C/W(Typ)

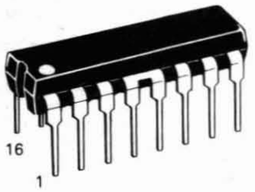


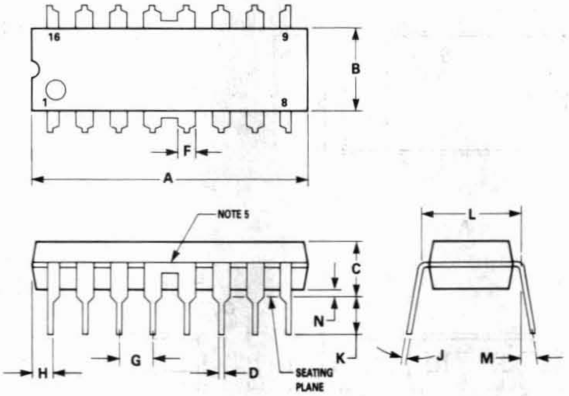


| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 18.80 | 21.34 | 0.740 | 0.840 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 4.06 | 5.08 | 0.160 | 0.200 |
| D | 0.38 | 0.53 | 0.015 | 0.021 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 BSC |  | 0.100 BSC |  |
| H | 0.38 | 2.41 | 0.015 | 0.095 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC |  | 0.300 BSC |  |
| M | 0° | 10° | 0° | 10° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9 AND 16).
5. ROUNDED CORNERS OPTIONAL; AS SHOWN IN PREVIOUS ISSUE.

**CASE 648C-01**
Plastic Package
$R_{\theta JA}$ = 52° C/W
$R_{\theta JA}$ = See Data Sheet



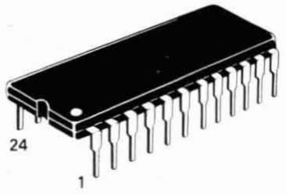


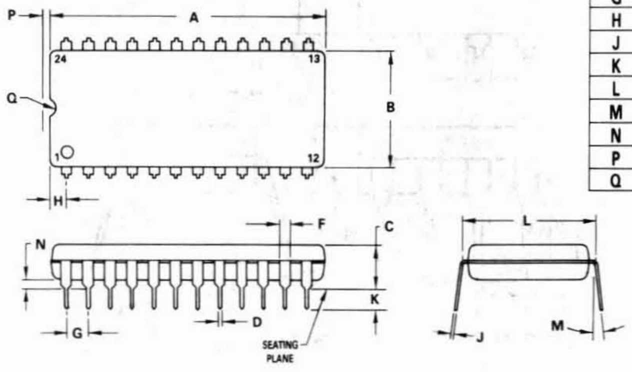
| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 18.80 | 21.34 | 0.740 | 0.840 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 4.06 | 5.08 | 0.160 | 0.200 |
| D | 0.38 | 0.53 | 0.015 | 0.021 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 BSC |  | 0.100 BSC |  |
| H | 0.38 | 2.41 | 0.015 | 0.095 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC |  | 0.300 BSC |  |
| M | 0° | 10° | 0° | 10° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.
5. EXTERNAL LEAD CONNECTION, BETWEEN 4 AND 5, 12 AND 13 AS SHOWN.

**CASE 649-03**
Plastic Package
$R_{\theta JA}$ = 90° C/W(Typ)

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

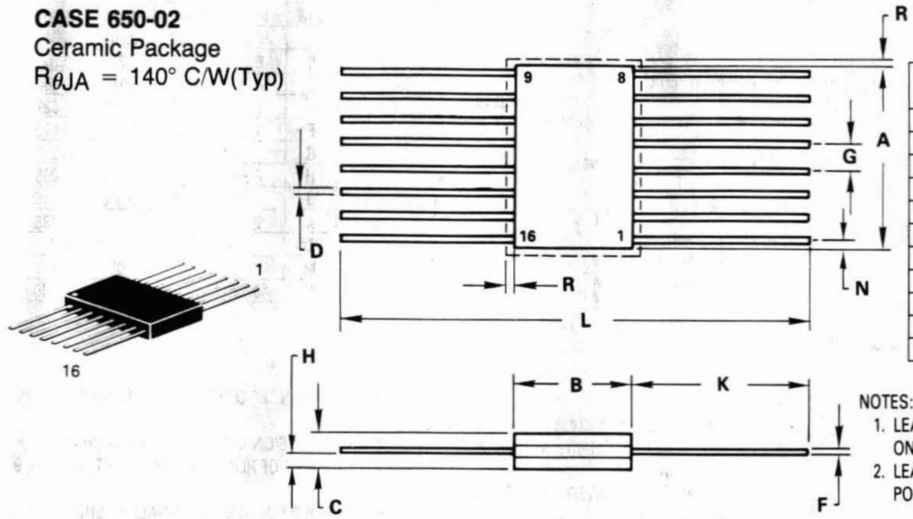




| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 31.50 | 32.13 | 1.240 | 1.265 |
| B | 13.21 | 13.72 | 0.520 | 0.540 |
| C | 4.70 | 5.21 | 0.185 | 0.205 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC |  | 0.100 BSC |  |
| H | 1.65 | 2.16 | 0.065 | 0.085 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 14.99 | 15.49 | 0.590 | 0.610 |
| M | — | 10° | — | 10° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |
| P | 0.13 | 0.38 | 0.005 | 0.015 |
| Q | 0.51 | 0.76 | 0.020 | 0.030 |

## CASE OUTLINE DIMENSIONS (continued)

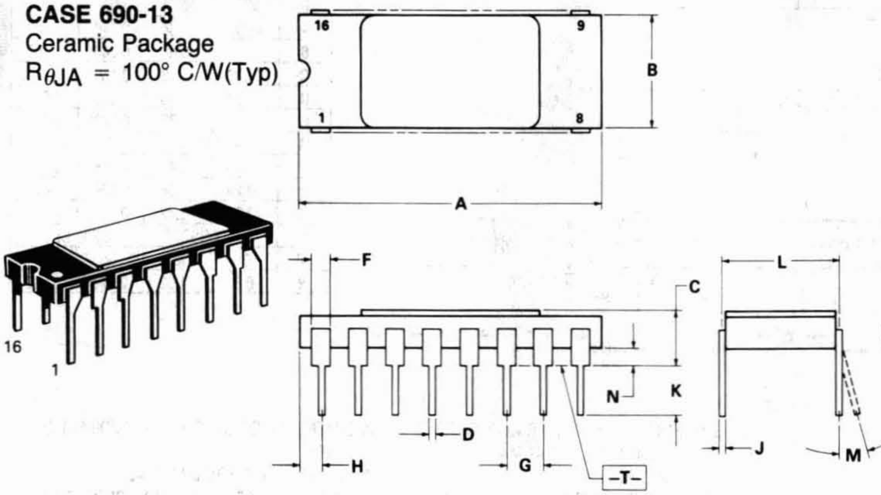
**CASE 650-02**
Ceramic Package
$R_{\theta JA}$ = 140° C/W(Typ)



| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 9.40 | 10.16 | 0.370 | 0.400 |
| B | 6.22 | 6.60 | 0.245 | 0.260 |
| C | 1.52 | 2.03 | 0.060 | 0.080 |
| D | 0.38 | 0.48 | 0.015 | 0.019 |
| F | 0.08 | 0.15 | 0.003 | 0.006 |
| G | 1.27 BSC |  | 0.050 BSC |  |
| H | 0.64 | 0.89 | 0.025 | 0.035 |
| K | 6.35 | 9.40 | 0.250 | 0.370 |
| L | 18.92 | — | 0.745 | — |
| N | — | 0.51 | — | 0.020 |
| R | — | 0.38 | — | 0.015 |

NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

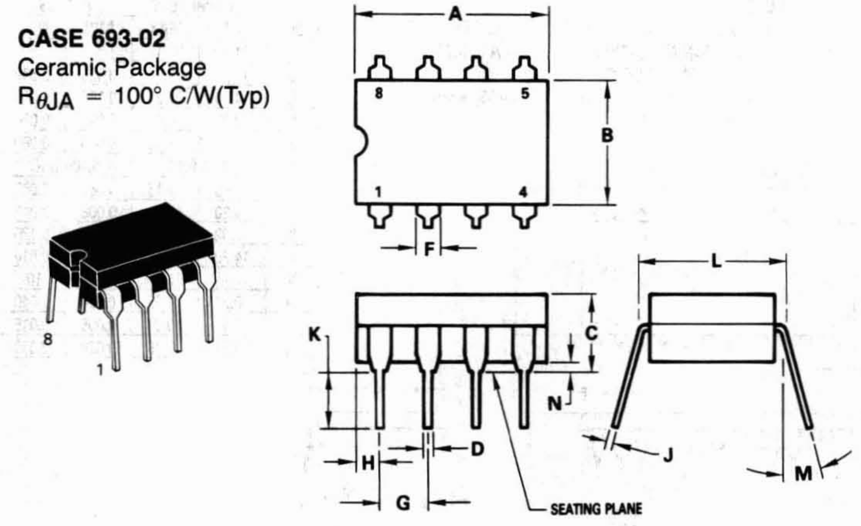
**CASE 690-13**
Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)



| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 20.07 | 20.57 | 0.790 | 0.810 |
| B | 7.11 | 7.74 | 0.280 | 0.305 |
| C | 2.67 | 4.19 | 0.105 | 0.165 |
| D | 0.38 | 0.53 | 0.015 | 0.021 |
| F | 0.76 | 1.52 | 0.030 | 0.060 |
| G | 2.54 BSC |  | 0.100 BSC |  |
| H | 0.76 | 1.78 | 0.030 | 0.070 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 5.08 | 0.125 | 0.200 |
| L | 7.62 BSC |  | 0.300 BSC |  |
| M | — | 10° | — | 10° |
| N | 0.38 | 1.52 | 0.015 | 0.060 |

NOTES:
1. -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE
3. POSITIONAL TOLERANCE FOR LEADS (D).
   ⌖ | ϕ 0.25 (0.010) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

**CASE 693-02**
Ceramic Package
$R_{\theta JA}$ = 100° C/W(Typ)



| DIM | MILLIMETERS |  | INCHES |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 9.91 | 10.92 | 0.390 | 0.430 |
| B | 6.22 | 6.99 | 0.245 | 0.275 |
| C | 4.32 | 5.08 | 0.170 | 0.200 |
| D | 0.41 | 0.51 | 0.016 | 0.020 |
| F | 1.40 | 1.65 | 0.055 | 0.065 |
| G | 2.54 BSC |  | 0.100 BSC |  |
| H | 1.14 | 1.65 | 0.045 | 0.065 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 4.06 | 0.125 | 0.160 |
| L | 7.37 | 7.87 | 0.290 | 0.310 |
| M | — | 15° | — | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

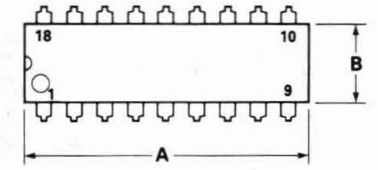
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

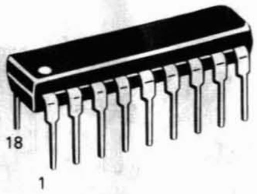
# CASE OUTLINE DIMENSIONS (continued)

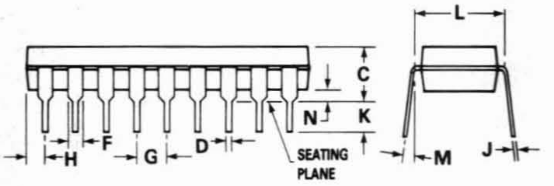
## CASE 707-02

Plastic Package

R$_{\theta JA}$ = 100° C/W(Typ)







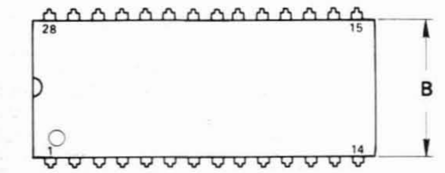
NOTES:

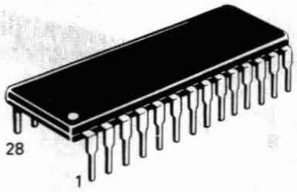
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

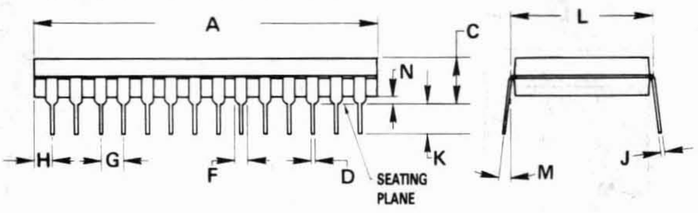
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 22.22 | 23.24 | 0.875 | 0.915 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.56 | 4.57 | 0.140 | 0.180 |
| D | 0.36 | 0.56 | 0.014 | 0.022 |
| F | 1.27 | 1.78 | 0.050 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.02 | 1.52 | 0.040 | 0.060 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

## CASE 710-02

Plastic Package







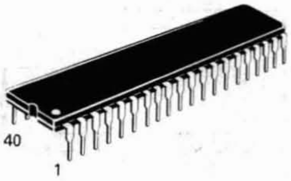
NOTES:

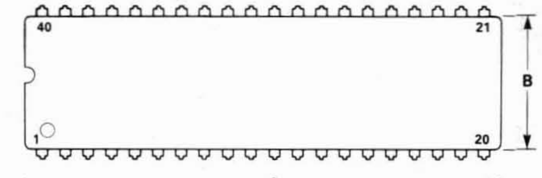
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

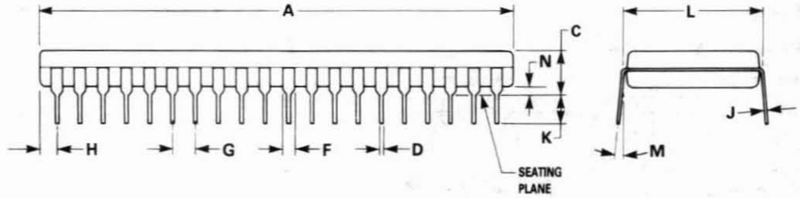
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 36.45 | 37.21 | 1.435 | 1.465 |
| B | 13.72 | 14.22 | 0.540 | 0.560 |
| C | 3.94 | 5.08 | 0.155 | 0.200 |
| D | 0.36 | 0.56 | 0.014 | 0.022 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.65 | 2.16 | 0.065 | 0.085 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

## CASE 711-03

Plastic Package







NOTES:

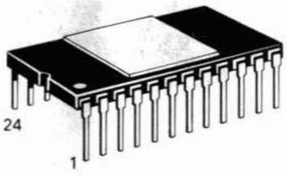
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

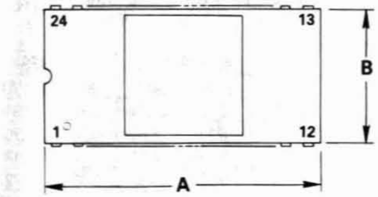
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 51.69 | 52.45 | 2.035 | 2.065 |
| B | 13.72 | 14.22 | 0.540 | 0.560 |
| C | 3.94 | 5.08 | 0.155 | 0.200 |
| D | 0.36 | 0.56 | 0.014 | 0.022 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.65 | 2.16 | 0.065 | 0.085 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

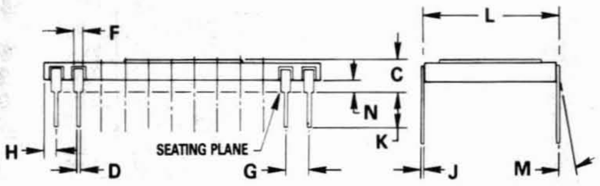
## CASE OUTLINE DIMENSIONS (continued)

### CASE 716-06

Ceramic Package
$R_{\theta JA} = 55° C/W$
$R_{\theta JC} = 15° C/W(Typ)$





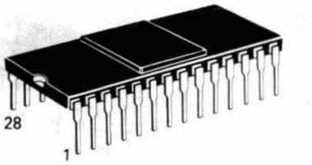


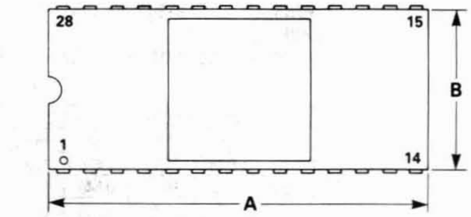
NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

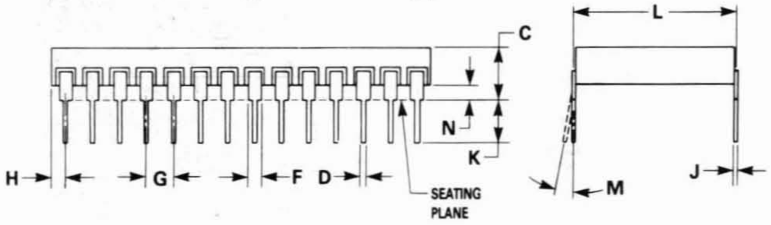
| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 27.64 | 30.99 | 1.088 | 1.220 |
| B | 14.73 | 15.34 | 0.580 | 0.604 |
| C | 2.67 | 4.32 | 0.105 | 0.170 |
| D | 0.38 | 0.53 | 0.015 | 0.021 |
| F | 0.76 | 1.40 | 0.030 | 0.055 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.76 | 1.78 | 0.030 | 0.070 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.54 | 4.57 | 0.100 | 0.180 |
| L | 14.99 | 15.49 | 0.590 | 0.610 |
| M | — | 10° | — | 10° |
| N | 1.02 | 1.52 | 0.040 | 0.060 |

### CASE 719-03

Ceramic Package
$R_{\theta JA} = 55° C/W$
$R_{\theta JC} = 15° C/W(Typ)$





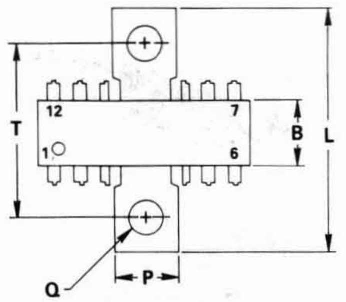


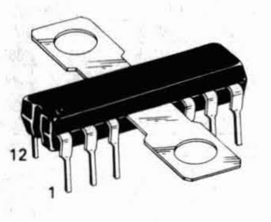
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIAMETER (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

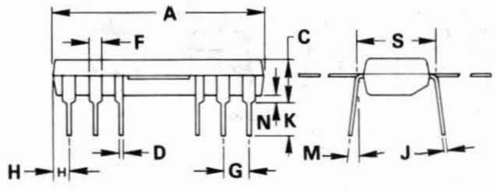
| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 35.20 | 35.92 | 1.386 | 1.414 |
| B | 14.73 | 15.34 | 0.580 | 0.604 |
| C | 3.05 | 4.19 | 0.120 | 0.165 |
| D | 0.38 | 0.53 | 0.015 | 0.021 |
| F | 0.76 | 1.40 | 0.030 | 0.055 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.76 | 1.78 | 0.030 | 0.070 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.54 | 4.19 | 0.100 | 0.165 |
| L | 14.99 | 15.49 | 0.590 | 0.610 |
| M | — | 10° | — | 10° |
| N | 0.51 | 1.52 | 0.020 | 0.060 |

### CASE 721-02

Plastic Package
$R_{\theta JA} = 52° C/W$
$R_{\theta JC}$ = See Data Sheet







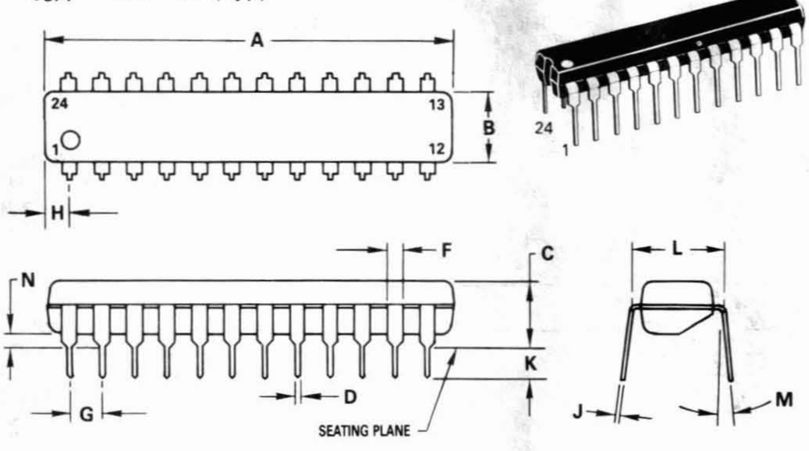
NOTES:
1. DIMENSION "S" TO CENTER OF LEADS WHEN FORMED PARALLEL.

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 20.70 | 21.34 | 0.815 | 0.840 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 4.06 | 4.57 | 0.160 | 0.180 |
| D | 0.43 | 0.56 | 0.017 | 0.022 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.41 | 2.67 | 0.095 | 0.105 |
| H | 1.32 | 1.83 | 0.052 | 0.072 |
| J | 0.33 | 0.46 | 0.013 | 0.018 |
| K | 3.30 | 3.94 | 0.130 | 0.155 |
| L | 25.15 | 27.94 | 0.990 | 1.100 |
| M | — | 10° | — | 10° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |
| P | 6.27 | 6.53 | 0.247 | 0.257 |
| Q | 3.48 | 3.73 | 0.137 | 0.147 |
| S | 7.37 | 7.87 | 0.290 | 0.310 |
| T | 16.26 | 16.76 | 0.640 | 0.660 |

## CASE 724-02

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)



NOTE:

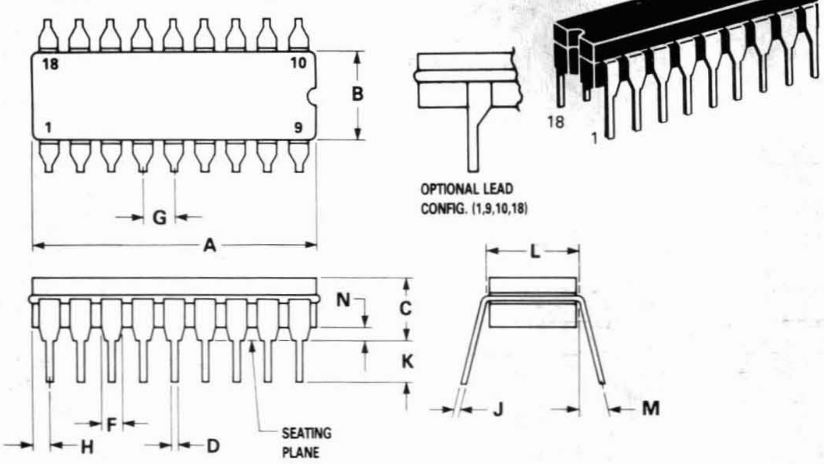
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D).

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 31.24 | 32.13 | 1.230 | 1.265 |
| B | 6.35 | 6.86 | 0.250 | 0.270 |
| C | 4.06 | 4.57 | 0.160 | 0.180 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.60 | 2.11 | 0.063 | 0.083 |
| J | 0.18 | 0.30 | 0.007 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.37 | 7.87 | 0.290 | 0.310 |
| M | — | 10° | — | 10° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

## CASE 726-01

Ceramic Package

$R_{\theta JA}$ = 100° C/W(Typ)



NOTES:

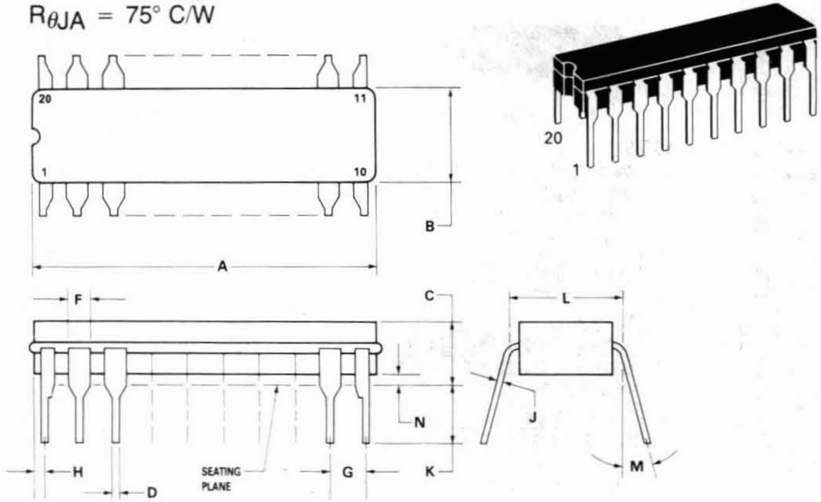
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 22.35 | 23.11 | 0.880 | 0.910 |
| B | 6.63 | 7.24 | 0.261 | 0.285 |
| C | — | 5.08 | — | 0.200 |
| D | 0.41 | 0.51 | 0.016 | 0.020 |
| F | 1.40 | 1.65 | 0.055 | 0.065 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.76 | 1.02 | 0.030 | 0.040 |
| J | 0.13 | 0.38 | 0.005 | 0.015 |
| K | — | 4.44 | — | 0.175 |
| L | 7.37 | 8.00 | 0.290 | 0.315 |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 0.76 | 0.020 | 0.030 |

## CASE 732-03

Ceramic Package

$R_{\theta JA}$ = 75° C/W



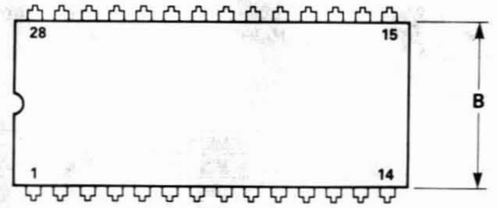
NOTES:

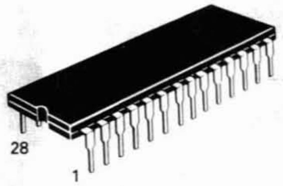
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

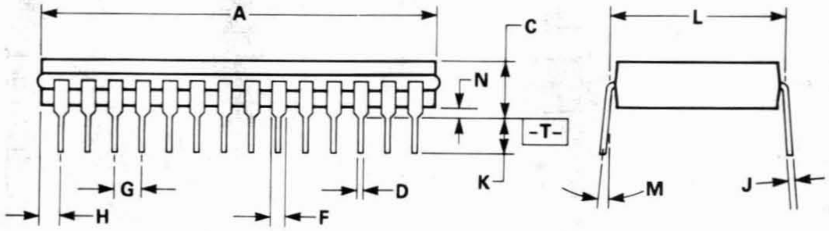
| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 23.88 | 25.15 | 0.940 | 0.990 |
| B | 6.60 | 7.49 | 0.260 | 0.295 |
| C | 3.81 | 5.08 | 0.150 | 0.200 |
| D | 0.38 | 0.56 | 0.015 | 0.022 |
| F | 1.40 | 1.65 | 0.055 | 0.065 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.51 | 1.27 | 0.020 | 0.050 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 4.06 | 0.125 | 0.160 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.25 | 1.02 | 0.010 | 0.040 |

## CASE 733-03

Ceramic Package







NOTES:

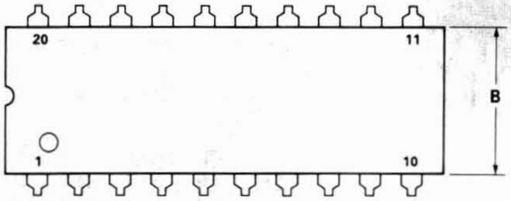
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   | ⌖ | ϕ 0.25 (0.010) Ⓜ | T | A Ⓜ |
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

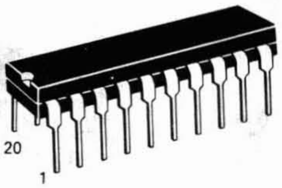
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 36.45 | 37.85 | 1.435 | 1.490 |
| B | 12.70 | 15.37 | 0.500 | 0.605 |
| C | 4.06 | 5.84 | 0.160 | 0.230 |
| D | 0.38 | 0.56 | 0.015 | 0.022 |
| F | 1.27 | 1.65 | 0.050 | 0.065 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 4.06 | 0.125 | 0.160 |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 5° | 15° | 5° | 15° |
| N | 0.51 | 1.27 | 0.020 | 0.050 |

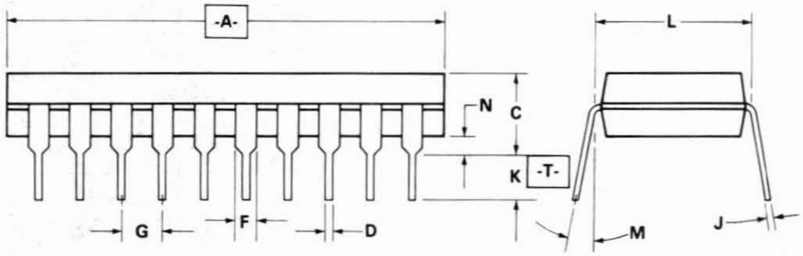
## CASE 738-02

Plastic Package

$R_{\theta JA} = 75° C/W$





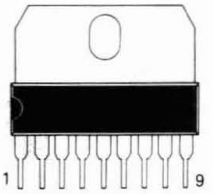


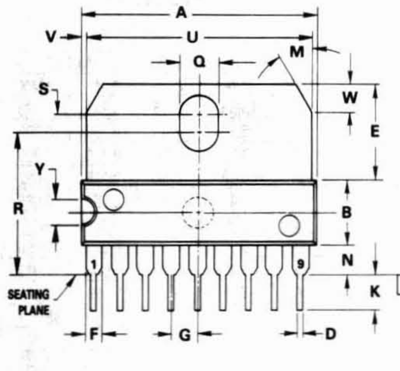
NOTES:

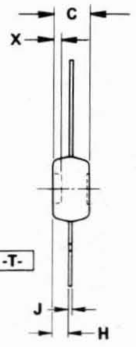
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   | ⌖ | ϕ 0.25 (0.010) Ⓜ | T | A Ⓜ |
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 25.65 | 27.18 | 1.010 | 1.070 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.94 | 4.57 | 0.155 | 0.180 |
| D | 0.38 | 0.56 | 0.015 | 0.022 |
| F | 1.27 | 1.78 | 0.050 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.79 | 3.56 | 0.110 | 0.140 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

## CASE 762-01







NOTES:

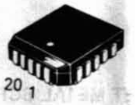
1. DIMENSIONS A, AND C ARE DATUMS. AND -T- IS A DATUM PLANE.
2. POSITIONAL TOLERANCE FOR LEAD DIMENSION D:
   | 0 | ϕ 0.25 (0.010) Ⓜ | -T- | A Ⓜ |
3. POSITIONAL TOLERANCE FOR LEAD DIMENSION J:
   | 0 | ϕ 0.25 (0.010) Ⓜ | -T- | C Ⓜ |
4. POSITIONAL TOLERANCE FOR LEAD DIMENSION Q:
   | 0 | ϕ 0.25 (0.010) Ⓜ | -T- | A Ⓜ |
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
6. CONTROLLING DIMENSION: MILLIMETER.

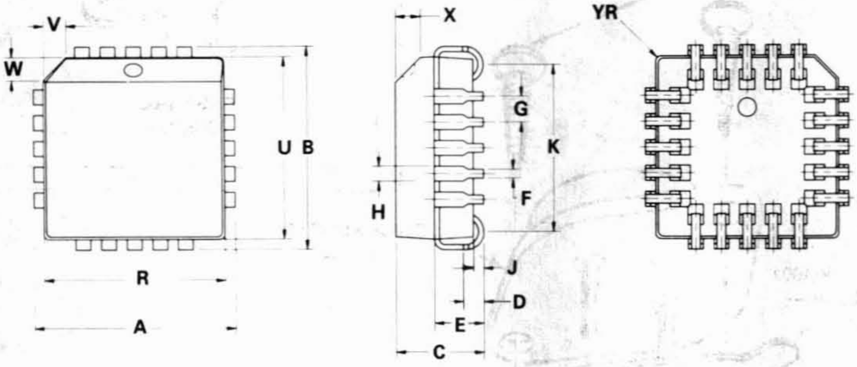
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 22.40 | 23.00 | 0.873 | 0.897 |
| B | 6.40 | 6.60 | 0.252 | 0.260 |
| C | 3.45 | 3.65 | 0.135 | 1.143 |
| D | 0.40 | 0.55 | 0.015 | 0.021 |
| E | 9.35 | 9.60 | 0.368 | 0.377 |
| F | 1.40 | 1.60 | 0.055 | 0.062 |
| G | 2.54 BSC | | 0.100BSC | |
| H | 1.51 | 1.71 | 0.059 | 0.067 |
| J | 0.360 | 0.400 | 0.014 | 0.015 |
| K | 3.95 | 4.20 | 0.155 | 0.165 |
| M | 30° BSC | | 30° BSC | |
| N | 2.50 | 2.70 | 0.099 | 0.106 |
| Q | 3.15 | 3.45 | 0.124 | 0.135 |
| R | 13.60 | 13.90 | 0.535 | 0.547 |
| S | 1.65 | 1.95 | 0.064 | 0.076 |
| U | 22.00 | 22.20 | 0.866 | 0.874 |
| V | 0.55 | 0.75 | 0.021 | 0.029 |
| W | 2.89 BSC | | 0.113 BSC | |
| X | 0.65 | 0.75 | 0.025 | 0.029 |
| Y | 2.70 | 2.80 | 0.106 | 0.110 |

## CASE 775-01

PLCC-20

Plastic Package





NOTES:

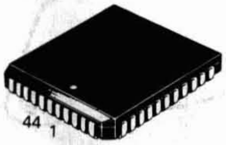
1. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH

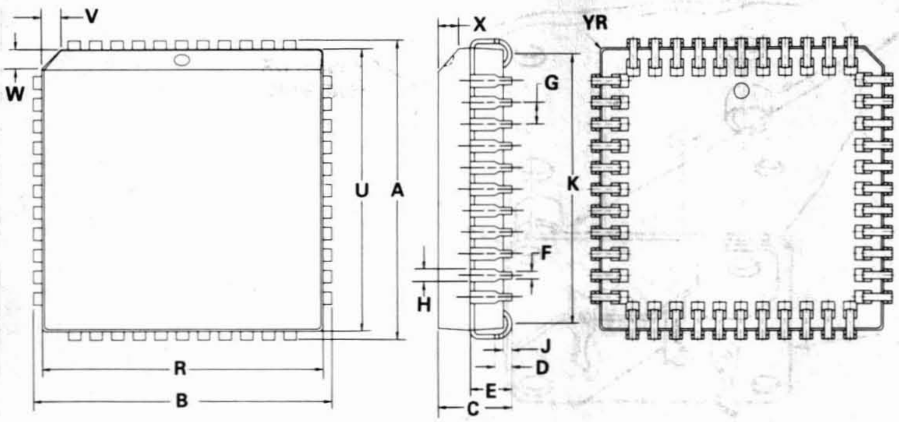
| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 9.78 | 10.02 | 0.385 | 0.395 |
| B | 9.78 | 10.02 | 0.385 | 0.395 |
| C | 4.19 | 4.57 | 0.165 | 0.180 |
| D | 0.64 | 1.01 | 0.025 | 0.040 |
| E | 2.16 | 2.79 | 0.085 | 0.110 |
| F | 0.33 | 0.53 | 0.013 | 0.021 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.66 | 0.81 | 0.026 | 0.032 |
| J | 0.38 | 0.63 | 0.015 | 0.025 |
| K | 7.37 | 8.38 | 0.290 | 0.330 |
| R | 8.89 | 9.04 | 0.350 | 0.356 |
| U | 8.89 | 9.04 | 0.350 | 0.356 |
| V | 1.07 | 1.21 | 0.042 | 0.048 |
| W | 1.07 | 1.21 | 0.042 | 0.048 |
| X | 1.07 | 1.42 | 0.042 | 0.056 |
| Y | 0.00 | 0.50 | 0.000 | 0.020 |

## CASE 777-01

PLCC-44

Plastic Package





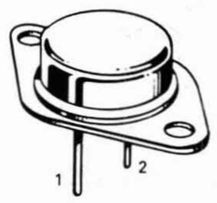
NOTES:

1. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH

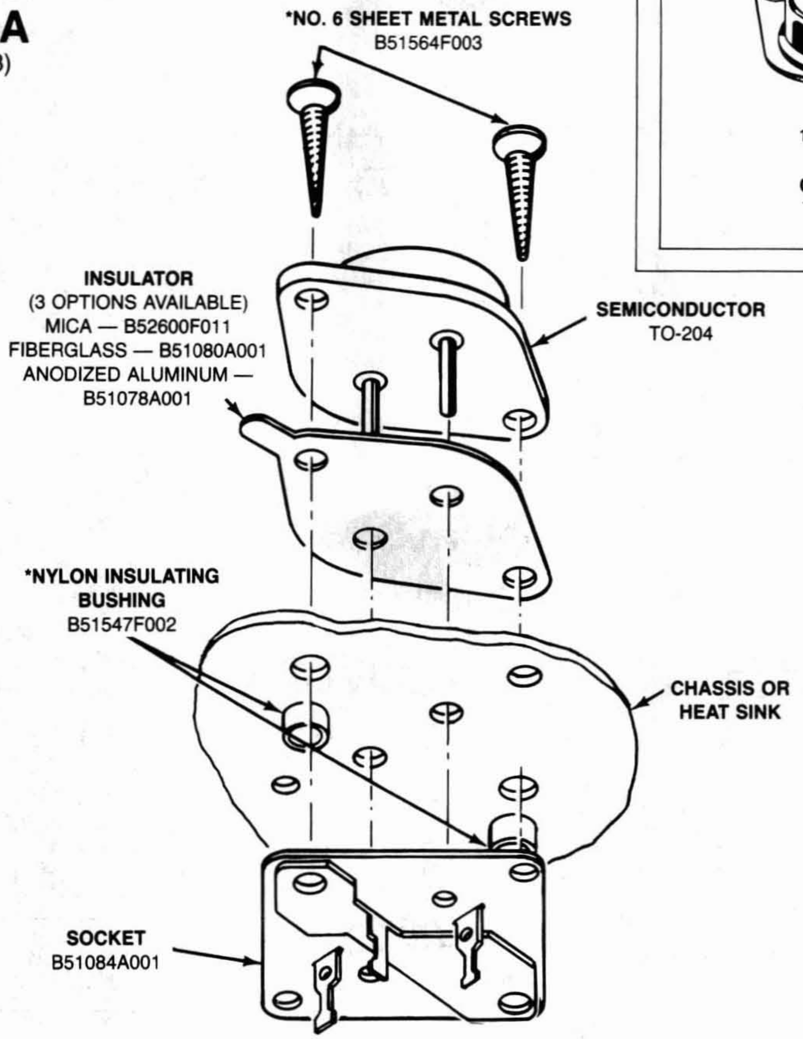
| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 17.40 | 17.65 | 0.685 | 0.695 |
| B | 17.40 | 17.65 | 0.685 | 0.695 |
| C | 4.19 | 4.57 | 0.165 | 0.180 |
| D | 0.64 | 1.01 | 0.025 | 0.040 |
| E | 2.16 | 2.79 | 0.085 | 0.110 |
| F | 0.33 | 0.53 | 0.013 | 0.021 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.66 | 0.81 | 0.026 | 0.032 |
| J | 0.38 | 0.63 | 0.015 | 0.025 |
| K | 14.99 | 16.00 | 0.590 | 0.630 |
| R | 16.51 | 16.66 | 0.650 | 0.656 |
| U | 16.51 | 16.66 | 0.650 | 0.656 |
| V | 1.07 | 1.21 | 0.042 | 0.048 |
| W | 1.07 | 1.21 | 0.042 | 0.048 |
| X | 1.07 | 1.42 | 0.042 | 0.056 |
| Y | 0.00 | 0.50 | 0.000 | 0.020 |

# Mounting Hardware TO-204AA

(Formerly TO-3)

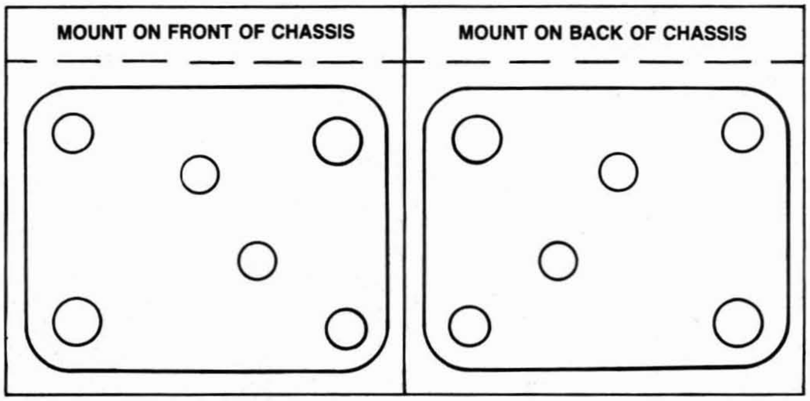


CASE 1-03
TO-204AA


*NO. 6 SHEET METAL SCREWS
B51564F003
INSULATOR
(3 OPTIONS AVAILABLE)
MICA — B52600F011
FIBERGLASS — B51080A001
ANODIZED ALUMINUM —
B51078A001
SEMICONDUCTOR
TO-204
*NYLON INSULATING
BUSHING
B51547F002
CHASSIS OR
HEAT SINK
SOCKET
B51084A001

*Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

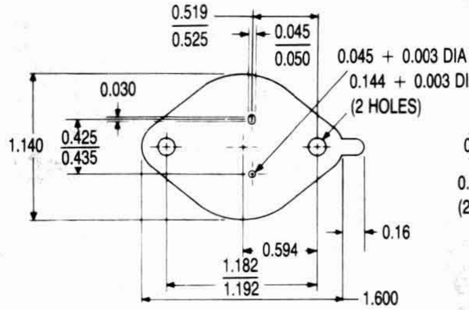
**DRAWINGS NOT TO SCALE**


MOUNT ON FRONT OF CHASSIS
MOUNT ON BACK OF CHASSIS

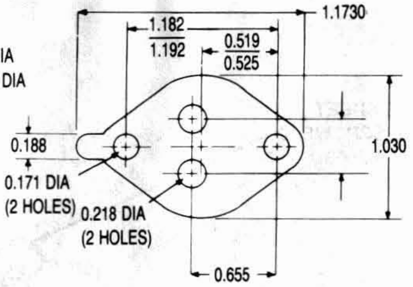
**FRONT TEMPLATE**
B51087A001

**BACK TEMPLATE**
B51087A002

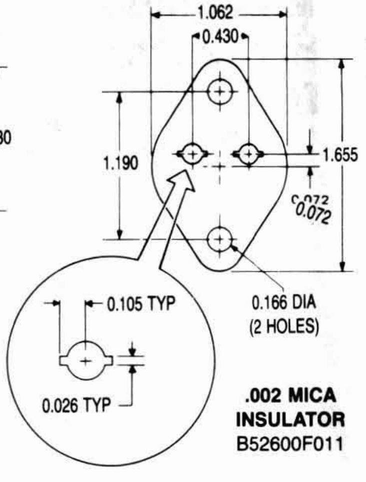
# MOUNTING HARDWARE TO-204AA


0.519
0.525
0.045
0.050
0.045 + 0.003 DIA
0.144 + 0.003 DIA
(2 HOLES)
0.030
1.140
0.425
0.435
0.16
0.594
1.182
1.192
1.600

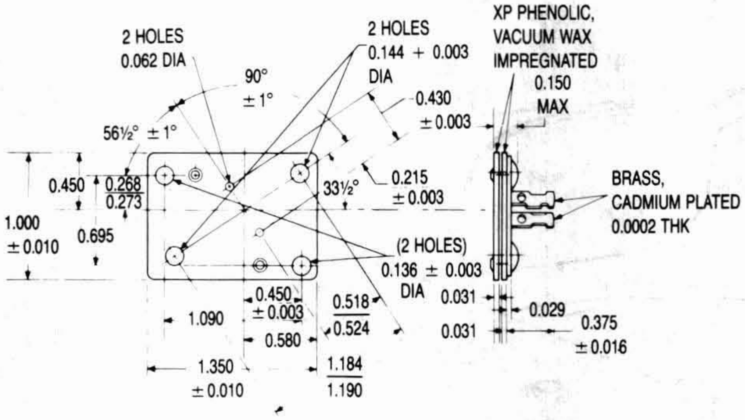
**0.003 TEFLON-COATED FIBERGLASS INSULATOR**
B51080A001


1.1730
1.182
1.192
0.519
0.525
0.188
1.030
0.171 DIA
(2 HOLES)
0.218 DIA
(2 HOLES)
0.655

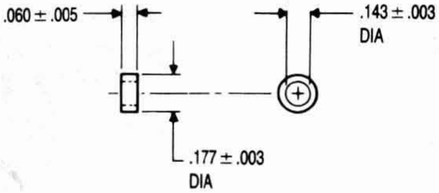
**.020 ALUMINUM INSULATOR**
B51078A001


1.062
0.430
1.190
1.655
0.072
0.105 TYP
0.026 TYP
0.166 DIA
(2 HOLES)

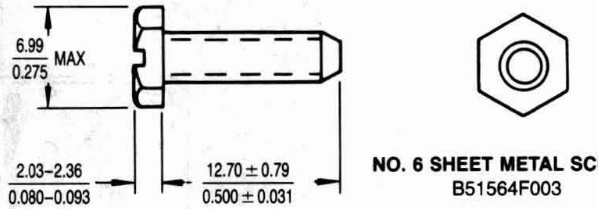
**.002 MICA INSULATOR**
B52600F011


2 HOLES
0.062 DIA
90°
± 1°
56½° ± 1°
2 HOLES
0.144 + 0.003
DIA
0.430
± 0.003
XP PHENOLIC,
VACUUM WAX
IMPREGNATED
0.150
MAX
0.450
0.268
0.273
33½°
0.215
± 0.003
BRASS,
CADMIUM PLATED
0.0002 THK
1.000
± 0.010
0.695
(2 HOLES)
0.136 ± 0.003
DIA
0.031
0.031
0.029
0.375
± 0.016
0.450
± 0.003
0.518
0.524
1.090
0.580
1.350
± 0.010
1.184
1.190

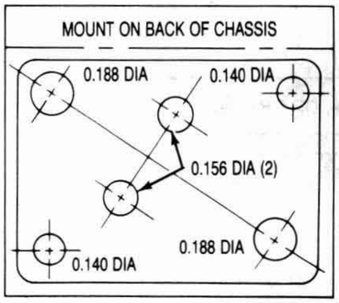
**TRANSISTOR SOCKET**
B51084A001


.060 ± .005
.143 ± .003
DIA
.177 ± .003
DIA

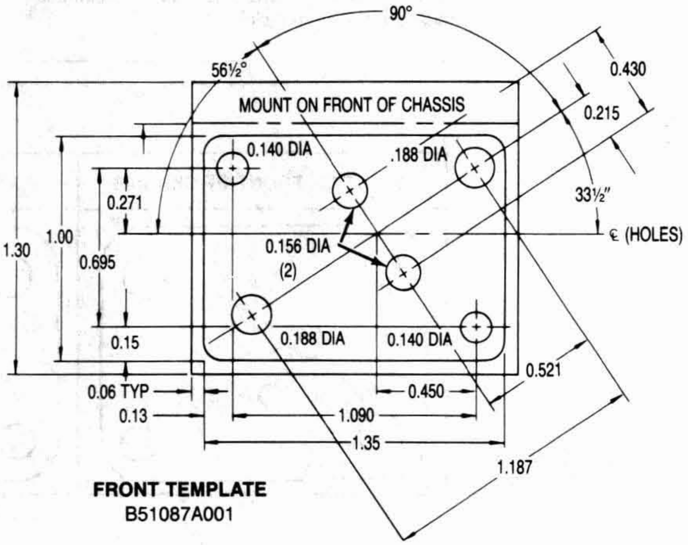
**NYLON INSULATING BUSHING**
B51547F002


6.99
0.275
MAX
2.03–2.36
0.080–0.093
12.70 ± 0.79
0.500 ± 0.031

**NO. 6 SHEET METAL SCREW**
B51564F003


MOUNT ON BACK OF CHASSIS
0.188 DIA
0.140 DIA
0.156 DIA (2)
0.188 DIA
0.140 DIA

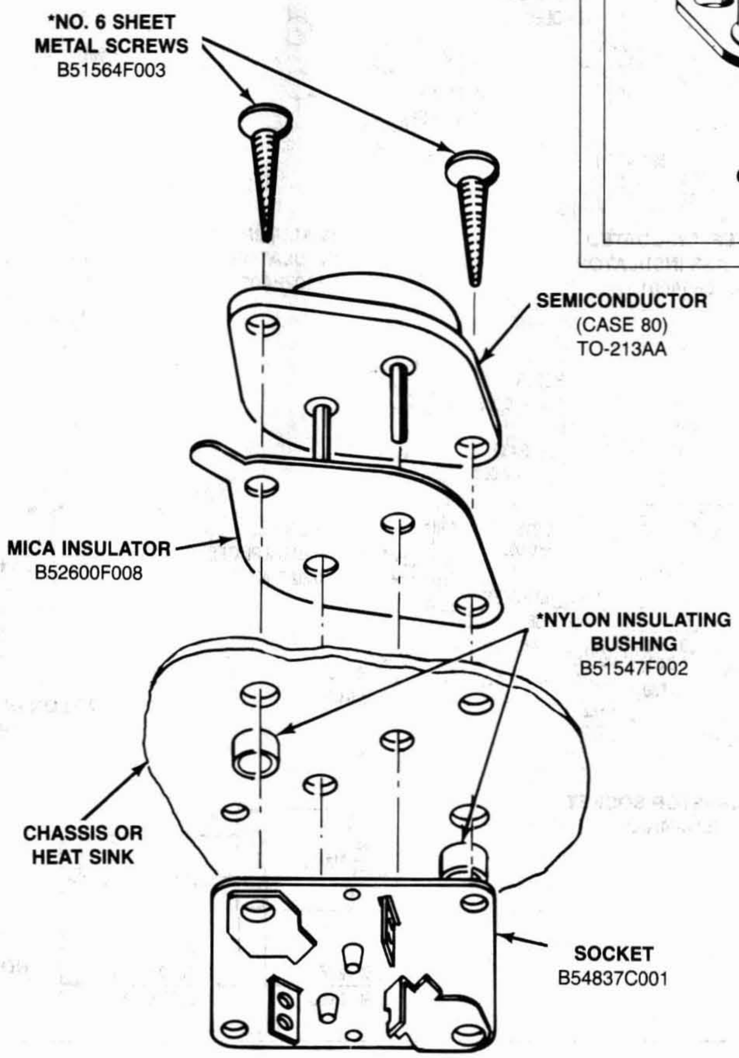
**BACK TEMPLATE**
B51087A002

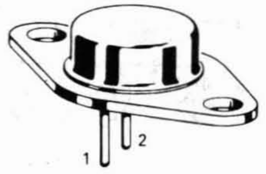

90°
56½°
0.430
0.215
MOUNT ON FRONT OF CHASSIS
0.140 DIA
.188 DIA
33½"
0.271
℄ (HOLES)
1.30
1.00
0.695
0.156 DIA
(2)
0.15
0.188 DIA
0.140 DIA
0.521
0.06 TYP
0.13
0.450
1.090
1.35
1.187

**FRONT TEMPLATE**
B51087A001

# Mounting Hardware TO-213AA

(Formerly TO-66)

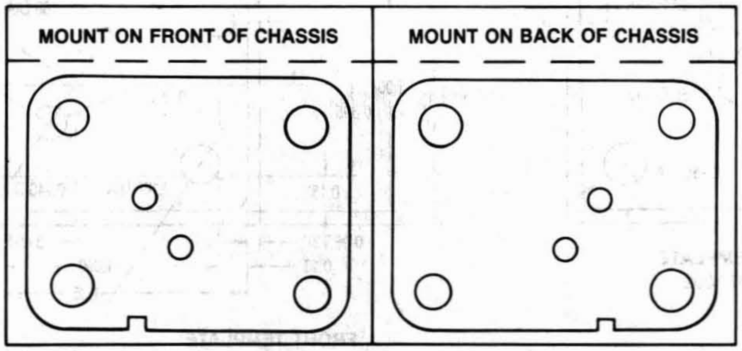

*NO. 6 SHEET METAL SCREWS
B51564F003
SEMICONDUCTOR
(CASE 80)
TO-213AA
MICA INSULATOR
B52600F008
*NYLON INSULATING BUSHING
B51547F002
CHASSIS OR HEAT SINK
SOCKET
B54837C001



CASE 80-02
TO-213AA

*Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

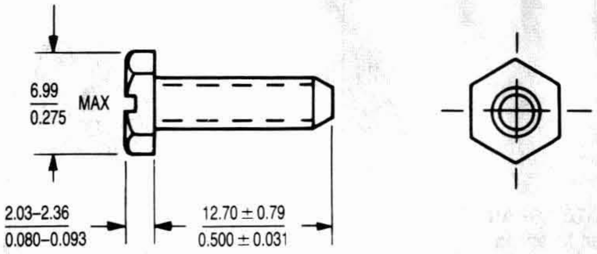
**(DRAWINGS NOT TO SCALE)**


MOUNT ON FRONT OF CHASSIS
MOUNT ON BACK OF CHASSIS

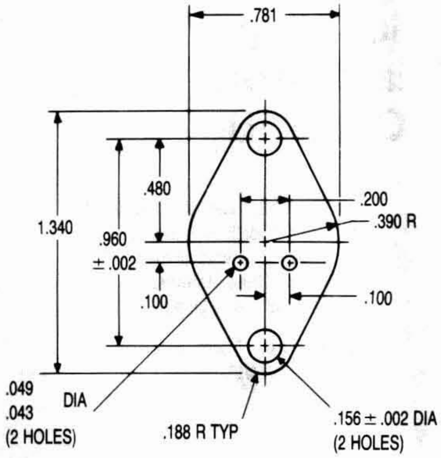
**FRONT TEMPLATE**
B54879C001

**BACK TEMPLATE**
B54879C002

# MOUNTING HARDWARE TO-213AA

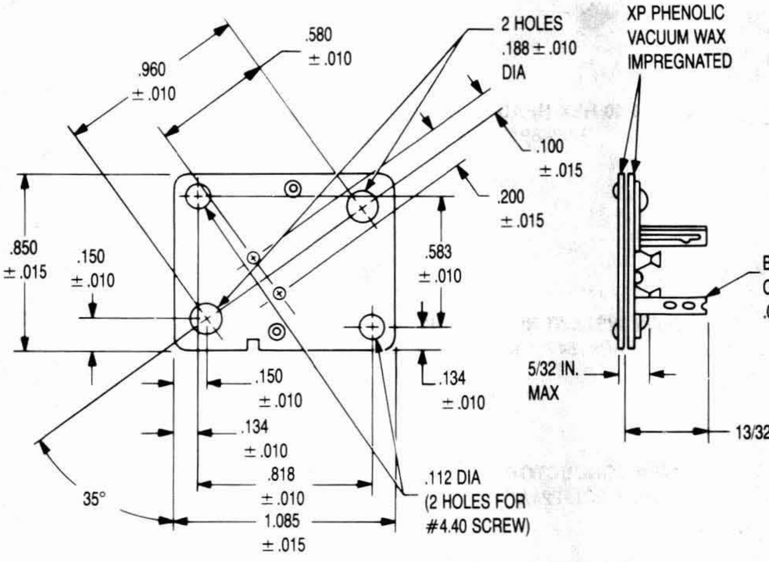

6.99
0.275
MAX
2.03–2.36
0.080–0.093
12.70 ± 0.79
0.500 ± 0.031

**NO. 6 SHEET METAL SCREW**
B51564F003

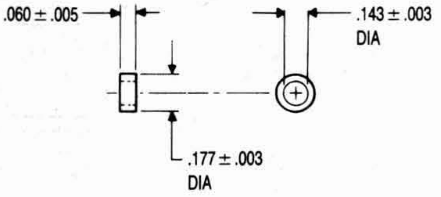

.781
1.340
.960
± .002
.480
.100
.200
.390 R
.100
.049
.043
(2 HOLES)
DIA
.188 R TYP
.156 ± .002 DIA
(2 HOLES)

**0.005 MICA INSULATOR**
B52600F008

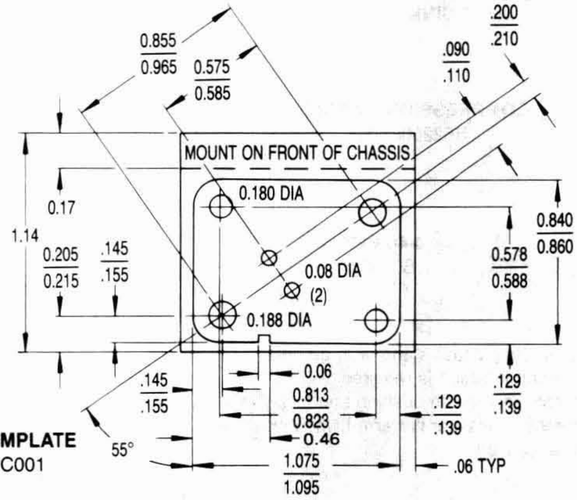
**0.003 MICA INSULATOR**
B52600F009


.960
± .010
.580
± .010
2 HOLES
.188 ± .010
DIA
XP PHENOLIC
VACUUM WAX
IMPREGNATED
.100
± .015
.200
± .015
.850
± .015
.150
± .010
.583
± .010
.150
± .010
.134
± .010
.134
± .010
.818
± .010
1.085
± .015
35°
.112 DIA
(2 HOLES FOR
#4.40 SCREW)
5/32 IN.
MAX
13/32 IN.
BRASS
CADMIUM PLATED
.030 THK

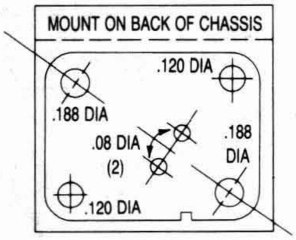
**TRANSISTOR SOCKET**
B54837C001


.060 ± .005
.143 ± .003
DIA
.177 ± .003
DIA

**NYLON INSULATING BUSHING**
B51547F002


0.855
0.965
0.575
0.585
.090
.110
.200
.210
MOUNT ON FRONT OF CHASSIS
0.180 DIA
0.17
1.14
0.205
0.215
.145
.155
0.08 DIA
(2)
0.188 DIA
0.578
0.588
0.840
0.860
.145
.155
0.06
0.813
0.823
0.46
.129
.139
.129
.139
55°
1.075
1.095
.06 TYP

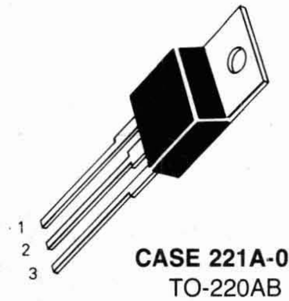
**FRONT TEMPLATE**
B54879C001


MOUNT ON BACK OF CHASSIS
.120 DIA
.188 DIA
.08 DIA
(2)
.188
DIA
.120 DIA

**BACK TEMPLATE**
B54879C002

7

# Mounting Hardware TO-220AB



**CASE 221A-03**
TO-220AB

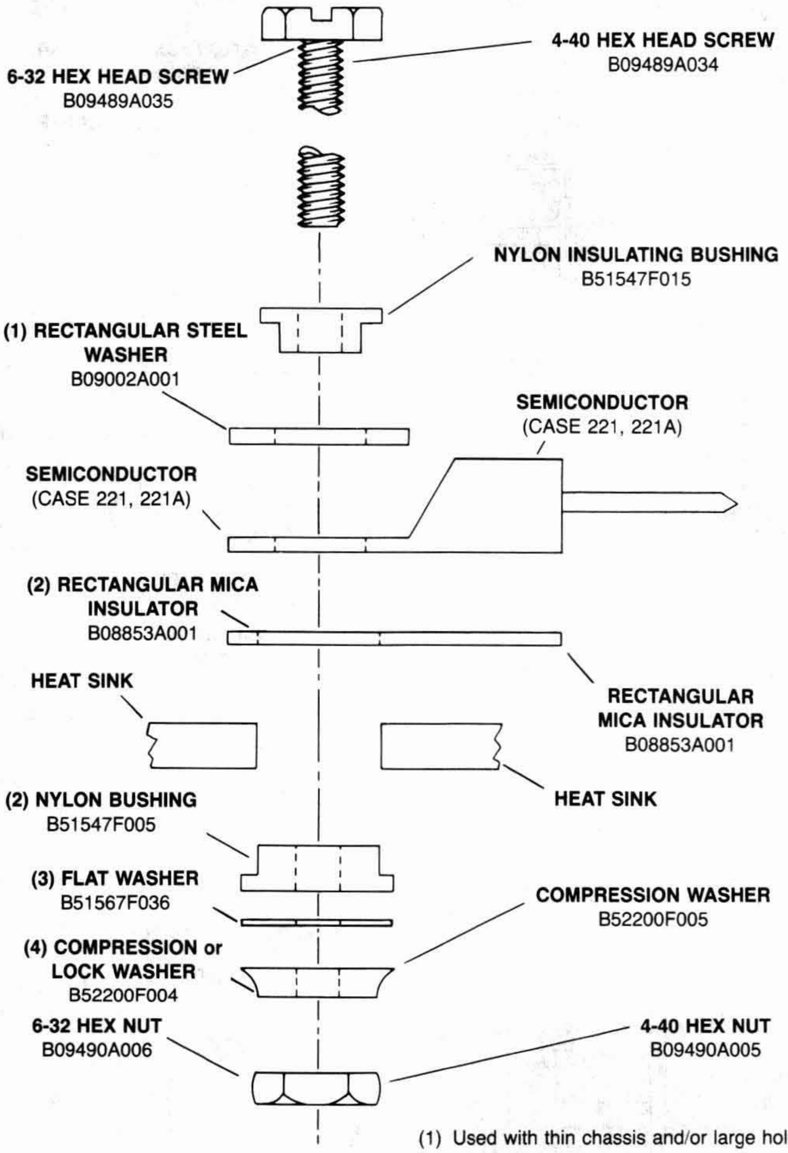
All JEDEC dimensions and notes apply

**PREFERRED ARRANGEMENT**
for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential.
6-32 Hardware is Used.

Choose from Parts Listed Below.

**ALTERNATE ARRANGEMENT**
for Isolated Mounting when Screw must be at Heat-Sink Potential.
4-40 Hardware is Used.

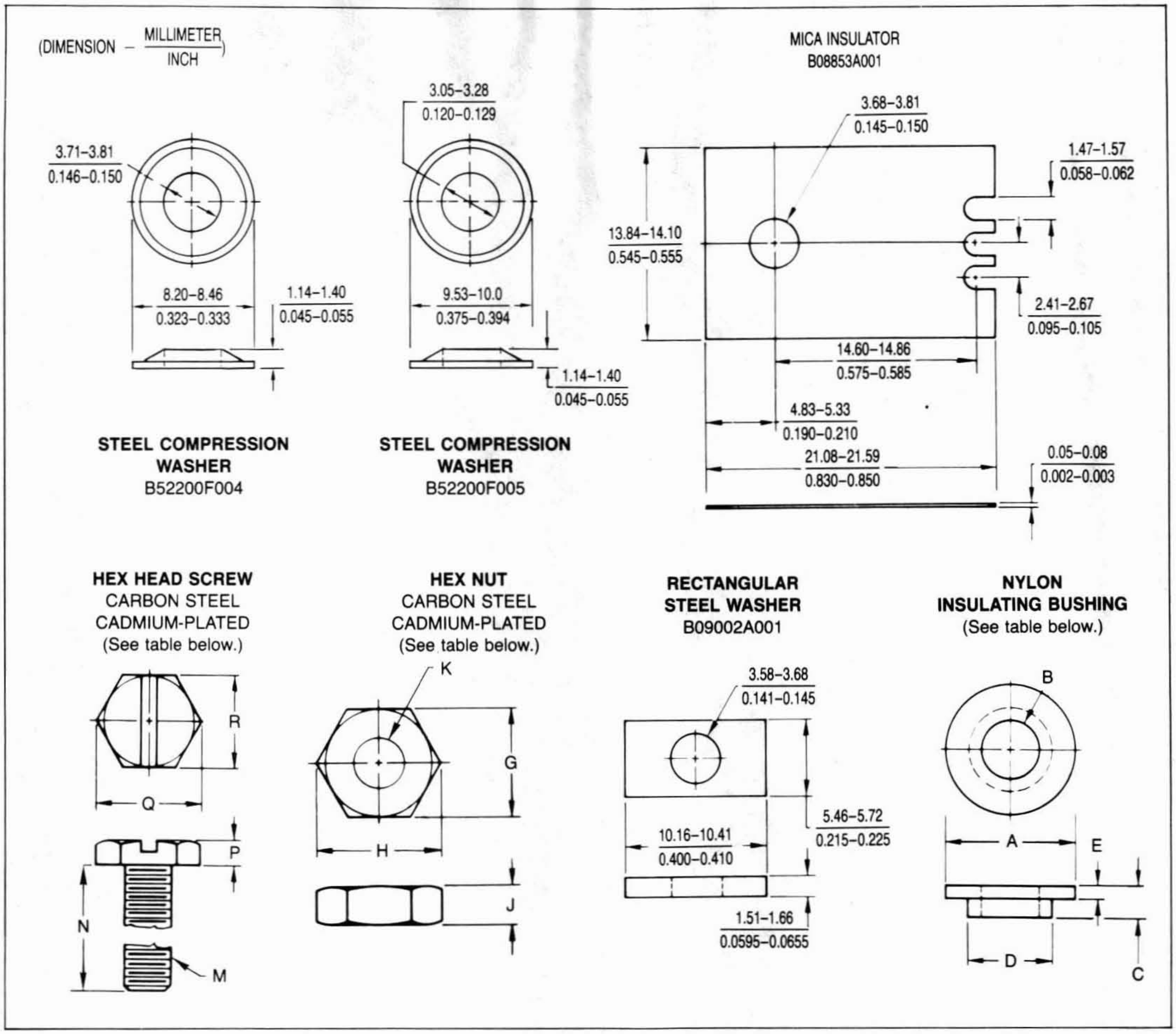
Use Parts Listed Below.


6-32 HEX HEAD SCREW
B09489A035
4-40 HEX HEAD SCREW
B09489A034
NYLON INSULATING BUSHING
B51547F015
(1) RECTANGULAR STEEL WASHER
B09002A001
SEMICONDUCTOR
(CASE 221, 221A)
SEMICONDUCTOR
(CASE 221, 221A)
(2) RECTANGULAR MICA INSULATOR
B08853A001
HEAT SINK
RECTANGULAR MICA INSULATOR
B08853A001
HEAT SINK
(2) NYLON BUSHING
B51547F005
(3) FLAT WASHER
B51567F036
COMPRESSION WASHER
B52200F005
(4) COMPRESSION or LOCK WASHER
B52200F004
6-32 HEX NUT
B09490A006
4-40 HEX NUT
B09490A005

(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing and lock washer are used.
(4) Compression washer preferred when plastic insulating material is used.

TORQUE REQUIREMENTS
Insulated 0.68 N-M (6 in.-lbs.) max
Noninsulated 0.9 N-M (8 in.-lbs.) max

# MOUNTING HARDWARE TO-220AB


(DIMENSION – MILLIMETER / INCH)
3.71–3.81 / 0.146–0.150
8.20–8.46 / 0.323–0.333
1.14–1.40 / 0.045–0.055
STEEL COMPRESSION WASHER
B52200F004
3.05–3.28 / 0.120–0.129
9.53–10.0 / 0.375–0.394
1.14–1.40 / 0.045–0.055
STEEL COMPRESSION WASHER
B52200F005
MICA INSULATOR
B08853A001
3.68–3.81 / 0.145–0.150
13.84–14.10 / 0.545–0.555
1.47–1.57 / 0.058–0.062
2.41–2.67 / 0.095–0.105
14.60–14.86 / 0.575–0.585
4.83–5.33 / 0.190–0.210
21.08–21.59 / 0.830–0.850
0.05–0.08 / 0.002–0.003
HEX HEAD SCREW
CARBON STEEL
CADMIUM-PLATED
(See table below.)
R
Q
P
N
M
HEX NUT
CARBON STEEL
CADMIUM-PLATED
(See table below.)
K
G
H
J
RECTANGULAR STEEL WASHER
B09002A001
3.58–3.68 / 0.141–0.145
10.16–10.41 / 0.400–0.410
5.46–5.72 / 0.215–0.225
1.51–1.66 / 0.0595–0.0655
NYLON INSULATING BUSHING
(See table below.)
B
A
E
D
C

## DIMENSIONS — MILLIMETER (INCH)

### NYLON BUSHING

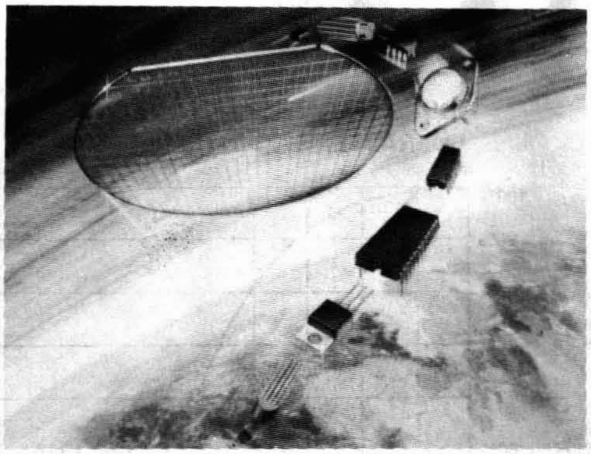
| PART NO. | DIM A | DIM B | DIM C | DIM D | DIM E |
|---|---|---|---|---|---|
| B51547F005 | 9.40–9.65<br>(0.370–0.380) | 3.84–4.09<br>(0.151–0.161) | 2.16–2.41<br>(0.085–0.095) | 6.10–6.35<br>(0.240–0.250) | 1.02–1.27<br>(0.040–0.050) |
| B51547F015 | 5.59–6.10<br>(0.220–0.240) | 3.05–3.15<br>(0.120–0.124) | 1.57–1.68<br>(0.062–0.066) | 3.56–3.66<br>(0.140–0.144) | 0.51–0.64<br>(0.020–0.025) |

### HEX NUT

| TYPE | PART NO. | DIM G | DIM H | DIM J | DIM K |
|---|---|---|---|---|---|
| 4-40 | B09490A005 | 6.12–6.35<br>(0.241–0.250) | 6.98–7.34<br>(0.275–0.289) | 2.21–2.49<br>(0.087–0.098) | 2.84 NOM<br>(0.112 NOM) |
| 6-32 | B09490A006 | 7.67–7.92<br>(0.302–0.312) | 8.74–9.17<br>(0.344–0.361) | 2.59–2.90<br>(0.102–0.114) | 3.50 NOM<br>(0.138 NOM) |

### HEX HEAD SCREW

| TYPE | PART NO. | DIM M | DIM N | DIM P | DIM Q | DIM R |
|---|---|---|---|---|---|---|
| 4-40 | B09489A034 | 0.112–40 | 1.57 (0.62) | 1.24–1.52<br>(0.049–0.060) | 5.12 MIN<br>(0.202 MIN) | 4.60–4.75<br>(0.181–0.187) |
| 6-32 | B09489A035 | 0.138–32 | 1.57 (0.62) | 2.03–2.36<br>(0.80–0.093) | 6.91 MIN<br>(0.272 MIN) | 6.20–6.35<br>(0.244–0.250) |



# Quality and Reliability Assurance

## 8

# Quality Concepts

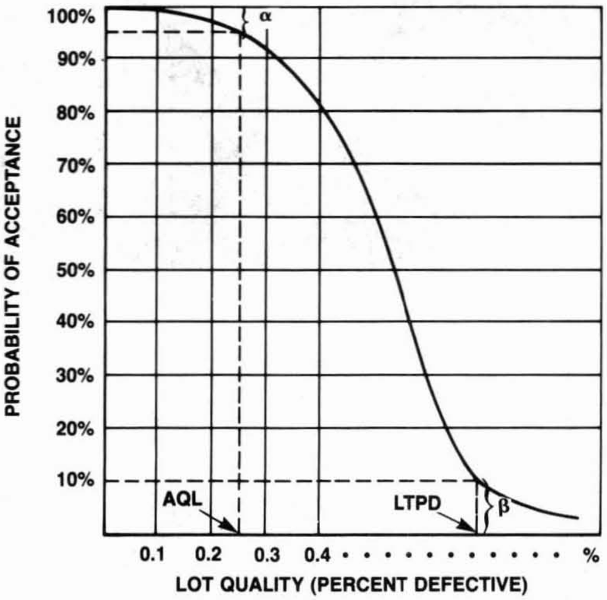
The word quality has been used to describe many things, such as fitness for use, customer satisfaction, customer enthusiasm, etc. However, when quality is used in the manufacturing environment, it has come to mean total quality as perceived by the customer. The simplest formulation that has been devised for total quality is:

$$Q = \frac{qs}{pd}$$

Where: $Q$ = Total Quality of a Supplier
$q$ = Product Quality (Technical)
$s$ = Service
$p$ = Price Competitiveness
$d$ = On Time Delivery

Product quality (q) of a linear integrated circuit from a product line is a measure that expresses the conformance of the device to a set of specifications. Such a measure is the percent rejects out of a collection of devices (lot, population). One hundred percent inspection has to be used to determine the actual quality of the lot. One characteristic of this approach is that it is expensive, and therefore, is used only where necessary. In addition, it may not be as accurate as it first appears because of operator errors due to fatigue and of course, it cannot be used where the inspection (test) is destructive. An alternative to 100% inspection is scientific acceptance sampling. Acceptance sampling is a method by which a portion (sample) of the total population is examined. On the basis of the sample quality (number of rejects that fail to conform to specifications out of a total sample is usually expressed in **parts per million percent rejects**) and by using the mathematics of probability and statistics, an estimate of the lot quality is made and the risk of an improper decision is specified. For example, a lot may be rejected because the sample quality was worse than that prescribed by the mathematics of sampling and our original goal (maximum percent rejects allowed in a lot). Yet, if the lot was one hundred percent inspected, we may find that the actual percent rejects in the lot was less than the maximum percent rejects established as a goal (Type I improper decision). In a similar way, the reverse may happen: a lot may be accepted on the basis of the sample quality (sample rejects are fewer than those prescribed by the mathematics of sampling and our goal) and yet, if a 100% inspection was performed, the actual percent rejects in the lot could be more than our established goal (Type II improper decision). A sampling plan is specified by the sample size and the maximum allowable defectives known as the acceptance number (ACCN).

**FIGURE 1 — TYPICAL OPERATING CHARACTERISTIC (O.C.) CURVE**



The risks involved in sampling are described by the operating characteristic (O.C.) curve of the sampling plan. As illustrated by Figure 1, this curve shows the probability of acceptance, on the vertical axis, versus the lot quality (percent rejects), on the horizontal axis. Each particular sampling plan will have its own O.C. curve. Two points on the curve are of interest. The AQL (Acceptable Quality Level), signifies the quality level (lot quality, in percent defective) that will be accepted most of the time (usually this is set at 95%). The risk of rejecting a lot even though the lot quality is equal to or better than the AQL is called the α Risk (5% probability shown on the curve; Type I error or Producer's Risk). The other point on the curve is the LTPD (Lot Tolerance Percent Defective) which signifies the level of rejects in a lot that is unsatisfactory and should be rejected by the plan most of the time or accepted infrequently (usually set at 10% of the time). This risk of accepting a lot when it should be rejected is known as the risk of making Type II improper decision (β Risk of Consumers Risk).

Linear integrated circuits can be produced to a variety of quality levels by combining different 100% and sample inspections and varying the criteria of acceptance and rejection. Thus, a customer can negotiate his own custom quality level if he wishes; however, this can become quite expensive in terms of time and money. That is why Motorola, in addition to the standard product level, produces Linear integrated circuits to a combination of screens which give enhanced product quality and reliability. These quality and reliability enhancement programs are the BETTER, JEDEC and JAN qualified programs and are described in this section.

# Reliability Concepts

Reliability is the probability that a Linear integrated circuit will perform its specified function in a given environment for a specified period of time. In other words, reliability is quality over time and environmental conditions.

The most frequently used reliability measure for integrated circuits is the failure rate, expressed in percent per thousand hours. The number of failures observed, taken over the number of device hours accumulated at the end of the observation period and expressed as a percent, is called the point estimate failure rate. This, however, is a number obtained from observations from a portion (sample) of all the integrated circuits. If we are to use this number to estimate the failure rate of all integrated circuits (total population), we need to say something about the risk we are taking by using this estimate. This statement is provided by the confidence level expressed together with the failure rate. For example, a 0.1% per 1000 hours failure rate at 90% confidence level means that 90% of the integrated circuits will have a failure rate below 0.1%/1000 hours — mathematically, the failure rate at a given confidence level is obtained from the point estimate and the CHI square ($X^2$) distribution. (The $X^2$ is a statistical distribution used to relate the observed and expected frequencies of an event.) In practice, a reliability calculator rule is used that gives the failure rate at the confidence level desired for the number of failures and device hours under question.

It is also important to note that, as the number of device hours increases, our confidence in the estimate increases. In integrated circuits, it is preferred to make estimates on the basis of failures per 1,000,000,000 device hours (FITS) or more. If such large numbers of device hours are not available for a particular device, then the point estimate is obtained by combining (pooling) the data from devices that are similar in process, voltage, construction, design, etc., and for which we expect to see the same failure modes in the field.

The environment is specified in terms of the temperature, electric field, relative humidity, etc., by an Eyring type of an equation of the form:

$$\lambda = Ae^{-\frac{Ø}{KT}} \ldots e^{-\frac{B}{RH}} \ldots e^{-\frac{C}{E}} \ldots$$

Where A, B, C, Ø & K are constants, T is temperature, RH is relative humidity, E is the electric field, etc.

The most familiar form of this equation deals with the first exponential which shows an Arrhenious type relationship of the failure rate versus the junction temperature of integrated circuits, while the causes of failure generally remain the same. Thus, we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then by applying known acceleration factors, estimate the failure rates for lower junction temperatures. Figure 2 shows a curve that gives estimates of typical failure rates versus temperature for integrated circuits.

Arrhenious type of equation: $\lambda = Ae^{-\frac{Ø}{KT}}$

Where:
$\lambda$ = Failure Rate
$A$ = Constant
$e$ = 2.72
$Ø$ = Activation Energy
$K$ = Botzman's Constant
$T$ = Temperature in Degrees Kelvin

$$T_J = T_A + \theta_{JA} P_D \text{ or } T_J = T_C + \theta_{JC} P_D$$

Where:
$T_J$ = Junction Temperature
$T_A$ = Ambient Temperature
$T_C$ = Case Temperature
$\theta_{JA}$ = Junction to Ambient Thermal Resistance
$\theta_{JC}$ = Junction to Case Thermal Resistance
$P_D$ = Power Dissipation

Failure rate curves for equipment and devices can be represented by an idealized graph called the Bathtub Curve (Figure 3).

There are three important regions identified on this curve. In Region A, the failure rate decreases with time and it is generally called infant mortality or early life failure region. In Region B, the failure rate has reached a relatively constant level and it is called constant failure rate or useful life region. In the third region, the failure rate increases again and it is called wearout region. Modern integrated circuits generally do not reach the wearout portion of the curve when operated under normal use conditions. The wearout portion of the curve can be seen under highly accelerated test conditions. As a matter of fact, even their useful life portion of the curve is characterized by so few failures compared to the accumulating hours, that the useful life curve looks as a continuously decreasing curve (Figure 3). From this discussion, it becomes obvious that elimination of infant mortality is of importance.

FIGURE 2 — TYPICAL FAILURE RATE
versus
JUNCTION TEMPERATURE

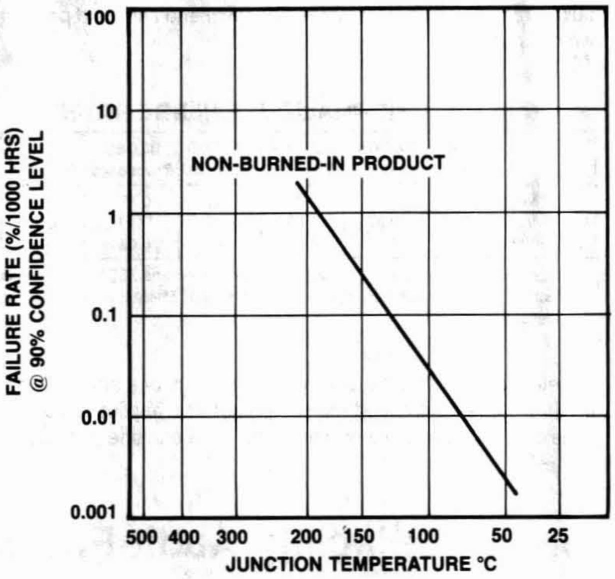
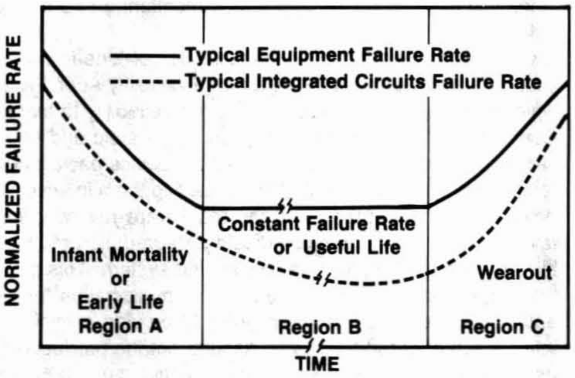


FIGURE 3 — FAILURE RATE
versus
TIME (BATHTUB CURVE)



Infant mortality in the short run is eliminated by a combination of various sample and 100% screens, with the most cost effective screen being burn-in at high temperature. These screening combinations form the various product enhancement programs such as the BETTER, JEDEC and JAN qualified, described in this section.

The most frequently asked question is which enhancement program do I need, if any at all, especially with the improvement of quality and reliability that has been achieved in integrated circuits over the last few years? The answer to this question is not simple and it depends on a number of factors such as the number of integrated circuits that will be used in a single piece of equipment, the maturity of this equipment, the environment in which the equipment will operate, the impact of a failure (safety versus entertainment), maintenance costs, etc. This question is best answered during customer-vendor interfacing, because of its' complexity and proprietary nature.

In order to obtain a feel for the effectiveness of the various programs, we will look at them on the basis of the normalized failure rate between each screening level and standard product which is used as reference.

**TABLE 1 — NORMALIZED FAILURE RATES**

| | Std Product | BETTER Level I | BETTER Level II | BETTER Level III | JEDEC Processed | JAN Qualified |
|---|---|---|---|---|---|---|
| 5–10 Volts | 1.0 | 0.67 | 0.33 | 0.25 | 0.17* | 0.17* |
| 10–25 Volts | 1.0 | 0.67 | 0.20 | 0.15 | 0.1 | 0.1 |
| 25–40 Volts | 1.0 | 0.67 | 0.1 | 0.07 | 0.05 | 0.05 |

*Note: A quality factor of 0.17 is given to JAN qualified and JEDEC processed product because of insufficient data to determine real differences between the two classes.

Determination that the quality and reliability of standard product is what is best suited for equipment and application under consideration, leads to a new question. How can one be assured that the reliability of standard product does not degrade over time? This is accomplished by periodic and strategic sampling and accelerated testing of the various integrated circuit device packaging systems known as reliability auditing. A description of this program is given later in this section.

Finally, a frequently asked question is about the reliability differences between plastic versus hermetic packaged integrated circuits. In general, for all bipolar integrated circuits including Linear, the field removal rates for plastic and hermetic ICs are the same for environments where there is not high humidity. In cases where the environment contains high humidity (such as under biased 85°C and 85% humidity), higher failure rates are to be expected from plastic encapsulated devices. The determination of the best packaging system for a given application depends on many factors, one of which is protection of the equipment from hostile environments. For example, some users have reported favorable results with plastic integrated circuits, even in relatively high humidity environments (coastal areas), by properly coating (good adherence, no contaminants) the boards containing the integrated circuits with protective materials.

# Linear Reliability Audit Program

The reliability of a product is a function of design and manufacturing. Inherent reliability is the reliability that a product would have if there were no imperfections in the materials, piece parts and manufacturing processes of the product. The presence of imperfections gives rise to the actual reliability of the product. The difference between inherent reliability and actual reliability is kept to a minimum by continuous monitoring and corrective action.

Continuous monitoring of the reliability of Linear integrated circuits is accomplished by the Linear Reliability Audit Program, which is designed to compare the actual reliability to that specified. This objective is accomplished by periodic and strategic sampling of the various integrated circuit device packaging systems. The samples are tested by subjecting them to accelerated environmental conditions and the results are reviewed for unfavorable trends that would indicate a degradation of the reliability or quality of a particular packaging system. This provides the trigger mechanism for initiating an investigation for cause and corrective action. Also, in order to provide a minimum of interruption of product flow and assure that the product is fit for use, a lot by lot sampling or a nondestructive type 100% screen is used to assure that a particular packaging system released for shipment does have the expected reliability. This rigorous surveillance is continued until there is sufficient proof (many consecutive lots) that the problem has been corrected.

The Bipolar Integrated Circuits Group has used reliability audits since the late sixties. Such programs have been identified by acronyms such as CRP (Consumer Reliability Program), EPIIC (Environmental Package Indicators for Integrated Circuits), LAPP (Linear Accelerated Punishment Program), RRAP (Rapid Reliability Assessment Program), and RAP (Reliability Audit Program).

Currently, the Linear Reliability Audit Program consists of a Weekly Reliability Audit and a Quarterly Reliability Audit. The Weekly Reliability Audit consists of rapid (short time) type of tests used to monitor the production lines on a real time basis. This type of testing is performed at the assembly/test sites and at the U.S. Linear Division Center. It provides data for use as an early warning system for identifying negative trends and triggering investigations for causes and corrective actions.

The Quarterly Reliability Audit consists of long term types of tests and is performed at the U.S. Linear Division Center. The data obtained from the Quarterly Reliability Audits is used to assure that the correlation between the short term weekly tests and long term quarterly type of tests has not changed, nor a new failure mechanism has appeared.

A large data base is established by combining the results from the Weekly Reliability Audit with the results from the Quarterly Reliability Audit. Such a data base is necessary for estimating long term failure rate and evaluating potential process improvement changes. Also, after a process improvement change has been implemented, the Linear Reliability Audit Program provides the system of monitoring the change and the past history data base for evaluating the affect of the change.

# Weekly Reliability Audit

The Weekly Reliability Audit is performed by the U.S. Linear Division Center, plus each assembly/test site which has the capability of assembling the Linear integrated circuits, performing final electrical testing, quality assurance electrical acceptance testing, reliability assurance testing and first level of failure analysis. The results are reviewed on a continuous basis and corrective action is taken when appropriate. The results are accumulated on a monthly basis and published.

The experimental test plan is as follows:

**Electrical Measuremenns:** Performed initially and after each reliability test, consists of critical parameters and functional testing at 25°C on a go-no-go basis.

**High Temperature Operating Life Test:** Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per the MIL-STD-883, Method 1015 with an ambient temperature of 145°C for 40 hours or equivalent based on a 1.0eV activation energy and the Arrhenious equation.

Approximate Accelerated Factors

| | 125°C | 50°C |
|---|---|---|
| 145°C | 4 | 4000 |
| 125°C | 1 | 1000 |

**Temperature Cycling/Thermal Shock:** Performed to detect mechanisms related to thermal expansion and contraction of dissimilar materials, etc. Procedure and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of −65°C to 150°C or −40°C to 125°C (JEDEC-STD-22-A104), minimum of 100 cycles.

**Pressure Temperature Humidity (Autoclave):** Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15psig. The duration of the test is 48 hours.

**Analysis Procedure:** Devices failing to meet the electrical criteria after being subjected to an accelerated environmental type test are verified and characterized electrically, then submitted for failure analysis.

# Quarterly Reliability Audit

The Quarterly Linear Reliability Audit Program is performed at the U.S. Linear Division Center. This testing is designed to assure that the correlation between the short term weekly tests and the longer quarterly tests has not changed and that no new failure mechanisms have appeared. It also provides additional long term information for a data base for estimating failure rates and evaluation of potential process improvement changes.

**Electrical Measurements:** Performed initially and at interim readouts, consist of all standard dc and functional parameters at 25°C, measured on a go-no-go basis.

**High Temperature Operating Life Test:** Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015, with an ambient temperature of 145°C for 40 and 250 hours or equivalent, based on 1.0eV activation energy and the Arrhenious equation.

Approximate Acceleration Factors

| | 125°C | 50°C |
|---|---|---|
| 145°C | 4 | 4000 |
| 125°C | 1 | 1000 |

**Temperature Cycling/Thermal Shock:** Performed to detect mechanisms related to thermal expansion and contraction, mismatch effects, etc. Procedure and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of −65°C to 150°C or −40°C to 125°C (JEDEC-STD-22-A104) for 100 and 1000 cycles. Temperature Cycling and Thermal Shock are used interchangeably.

**Pressure Temperature Humidity (Autoclave):** Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanism due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15psig. The duration of the test is for 96 hours, with a 48 hours interim readout.

**Pressure Temperature Humidity Bias (Biased Autoclave):** This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanism due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by the moisture and the applied electric fields. Conditions are per JEDEC-STD-22, Method 102, with bias applied. Temperature is 121°C, steam environment and 15psig. Duration is for 32 hours, with a 16 hour interim readout. This test detects the same type of failures as the Temperature Humidity Bias (85°C, 85% RH, with bias) test, only faster. The acceleration factor between PTHB and THB is between 20 and 40 times, depending on the type of corrosion mechanism, electric field and packaging system.

**Temperature, Humidity & Bias (THB):** This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by moisture and the applied electric fields. Conditions are per JEDEC-STD-22, Method 102 (85°C, 85% RH), with bias applied. The duration is for 1008 hours, with a 504 hour interim readout. The acceleration factor between THB (85°C, 85% RH and bias) and the 30°C, 90% RH is typically 40–50 times, depending on the type of corrosion mechanism, electric field and packaging system.

**Analysis Procedure:** Devices failing to meet the electrical criteria after being subjected to an accelerated environmental type test are verified and characterized electrically, then submitted for failure analysis.

# Commercial Product Processing Levels

**Motorola's reliability and quality-enhancement program was developed to provide improved levels of quality and reliability for standard commercial products.**

# The "Better" Program

**THE "BETTER" program is offered on MOS, Linear ECL, TTL, LS TTL, DTL and HTL in dual-in-line ceramic and plastic packages.**

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industry's finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing, each tailored to meet different user needs at nominal costs.

The program is designed to:

- Eliminate need for independent test labs and associated extra time and costs
- Reduce field failures
- Reduce service calls
- Reduce equipment downtime
- Reduce board and system rework
- Reduce infant mortality
- Save time and money
- Increase end-customer satisfaction

***BETTER PROCESSING — STANDARD PRODUCT PLUS:***

| 100% Screen | Level I "S" | Level II "D" | Level III "DS" |
|---|---|---|---|
| Temp. Cycle, 10 Cycles<br>−65°C to +150°C | X | | X |
| Burn-In — Mil-Std-883 | | X | X |
| Post Burn-In Electrical[1,2] | | X | X |
| 100°C Functional | X | | X |
| DC Parameter at 25°C[1,2] | X | X | X |
| Tightened, QA Sample | X | X | X |

1. ECL and LS TTL do functional and dc 100% at $T_A$ Max (Levels I and III, 25°C or $T_A$ Max optional for Level II.)
2. NMOS does functional and dc 100% at 100°C.
3. Additional standardized flows, when available, will be added as BETTER Level IV, V, etc.

## "BETTER" AQL GUARANTEES

| Test | Condition | AQL | | |
|---|---|---|---|---|
| | | Level I | Level II | Level III |
| High Temperature Functional | $T_A$ = 100°C or $T_A$ Max | 0.061 | * | 0.061 |
| DC Parametric | $T_A$ = 25°C | 0.061 | 0.061 | 0.061 |
| DC Parametric | $T_A$ Min, $T_A$ Max | 0.30 | 0.30 | 0.30 |
| AC Parametric | $T_A$ = 25°C* | 0.061 | 0.061 | 0.061 |
| Dynamic Test (Linear and NMOS) | $T_A$ = 25°C* | 0.061 | 0.061 | 0.061 |
| External Visual and Mechnical | Major/Minor | 0.061 | 0.061 | 0.061 |
| Hermeticity<br>(Not Applicable to Plastic Packages) | Gross/Fine | 0.15 | 0.15 | 0.15 |

"AQL" values shown are for reference only. "LTPD" type sampling plans that are equal to or tighter than values indicated may be used. Also, the guaranteed electrical and visual/mechanical AQL levels will be progressively tightened. Contact your nearest Motorola sales office for current values.

*Some products are also AC specified at $T_A$ Min and $T_A$ Max. In those instances, AQL guarantees will be per Motorola standard. The AQL guarantee for Functional on "LEVEL II" processing will also be per Motorola standard.

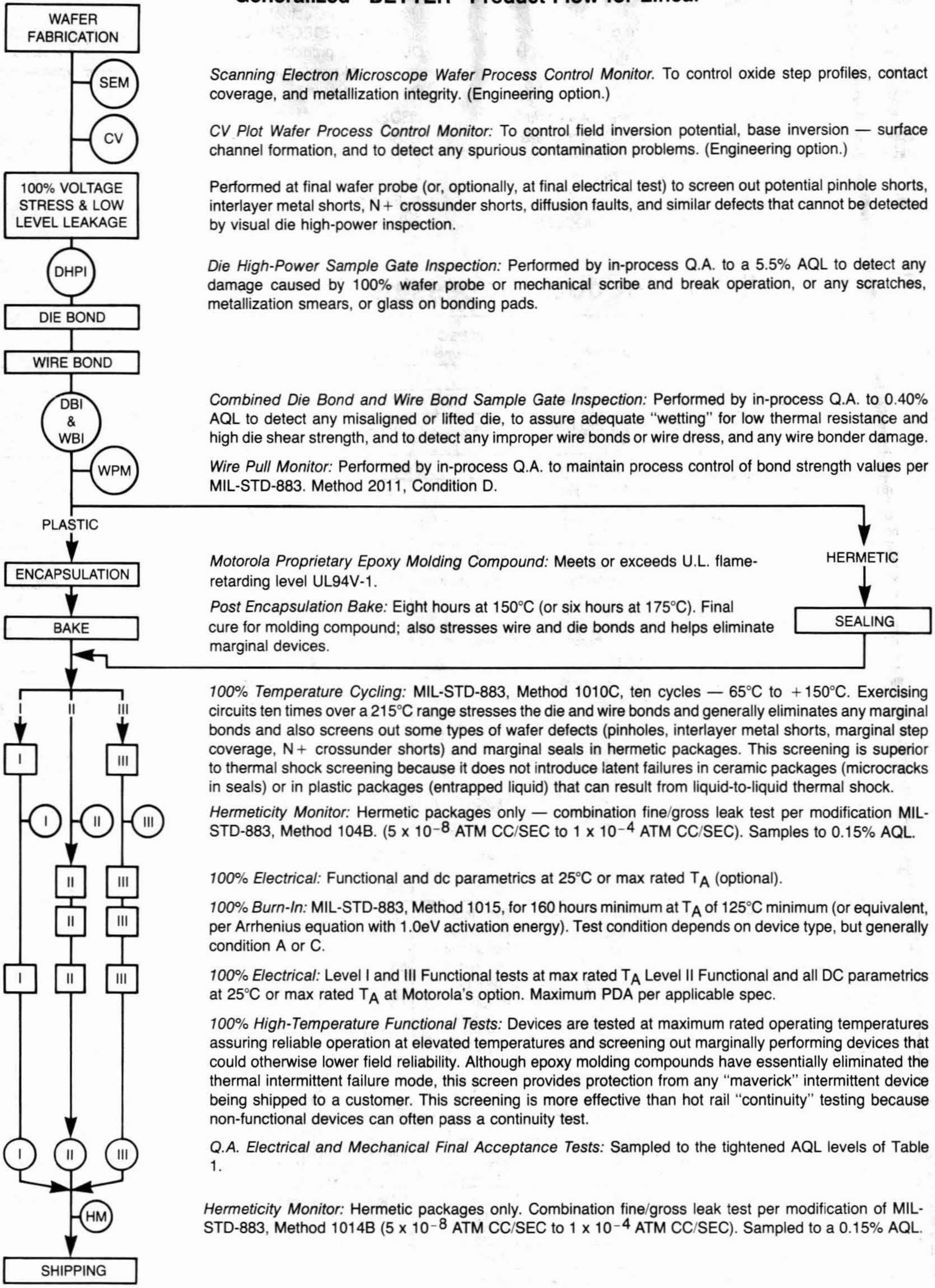
## How to Order

| **MC34004** | **P** | **D** |
|---|---|---|
| Part Identification | Standard Package Suffix | BETTER PROCESSING<br>LEVEL I = SUFFIX S<br>LEVEL II = SUFFIX D<br>LEVEL III = SUFFIX DS |

## Part Marking

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

## Generalized "BETTER" Product Flow for Linear



*Scanning Electron Microscope Wafer Process Control Monitor.* To control oxide step profiles, contact coverage, and metallization integrity. (Engineering option.)

*CV Plot Wafer Process Control Monitor:* To control field inversion potential, base inversion — surface channel formation, and to detect any spurious contamination problems. (Engineering option.)

Performed at final wafer probe (or, optionally, at final electrical test) to screen out potential pinhole shorts, interlayer metal shorts, N+ crossunder shorts, diffusion faults, and similar defects that cannot be detected by visual die high-power inspection.

*Die High-Power Sample Gate Inspection:* Performed by in-process Q.A. to a 5.5% AQL to detect any damage caused by 100% wafer probe or mechanical scribe and break operation, or any scratches, metallization smears, or glass on bonding pads.

*Combined Die Bond and Wire Bond Sample Gate Inspection:* Performed by in-process Q.A. to 0.40% AQL to detect any misaligned or lifted die, to assure adequate "wetting" for low thermal resistance and high die shear strength, and to detect any improper wire bonds or wire dress, and any wire bonder damage.

*Wire Pull Monitor:* Performed by in-process Q.A. to maintain process control of bond strength values per MIL-STD-883. Method 2011, Condition D.

*Motorola Proprietary Epoxy Molding Compound:* Meets or exceeds U.L. flame-retarding level UL94V-1.

*Post Encapsulation Bake:* Eight hours at 150°C (or six hours at 175°C). Final cure for molding compound; also stresses wire and die bonds and helps eliminate marginal devices.

*100% Temperature Cycling:* MIL-STD-883, Method 1010C, ten cycles — 65°C to +150°C. Exercising circuits ten times over a 215°C range stresses the die and wire bonds and generally eliminates any marginal bonds and also screens out some types of wafer defects (pinholes, interlayer metal shorts, marginal step coverage, N+ crossunder shorts) and marginal seals in hermetic packages. This screening is superior to thermal shock screening because it does not introduce latent failures in ceramic packages (microcracks in seals) or in plastic packages (entrapped liquid) that can result from liquid-to-liquid thermal shock.

*Hermeticity Monitor:* Hermetic packages only — combination fine/gross leak test per modification MIL-STD-883, Method 104B. (5 x $10^{-8}$ ATM CC/SEC to 1 x $10^{-4}$ ATM CC/SEC). Samples to 0.15% AQL.

*100% Electrical:* Functional and dc parametrics at 25°C or max rated $T_A$ (optional).

*100% Burn-In:* MIL-STD-883, Method 1015, for 160 hours minimum at $T_A$ of 125°C minimum (or equivalent, per Arrhenius equation with 1.0eV activation energy). Test condition depends on device type, but generally condition A or C.

*100% Electrical:* Level I and III Functional tests at max rated $T_A$ Level II Functional and all DC parametrics at 25°C or max rated $T_A$ at Motorola's option. Maximum PDA per applicable spec.

*100% High-Temperature Functional Tests:* Devices are tested at maximum rated operating temperatures assuring reliable operation at elevated temperatures and screening out marginally performing devices that could otherwise lower field reliability. Although epoxy molding compounds have essentially eliminated the thermal intermittent failure mode, this screen provides protection from any "maverick" intermittent device being shipped to a customer. This screening is more effective than hot rail "continuity" testing because non-functional devices can often pass a continuity test.

*Q.A. Electrical and Mechanical Final Acceptance Tests:* Sampled to the tightened AQL levels of Table 1.

*Hermeticity Monitor:* Hermetic packages only. Combination fine/gross leak test per modification of MIL-STD-883, Method 1014B (5 x $10^{-8}$ ATM CC/SEC to 1 x $10^{-4}$ ATM CC/SEC). Sampled to a 0.15% AQL.

# Standard HIGH REL Programs

Motorola, a pioneer in the manufacture of *high-reliability* integrated circuits, now offers you a two-way program for Hi Rel products.

**JAN-QUALIFIED**

Motorola stocks many circuits which meet JAN-QUALIFIED specifications, and is actively pursuing an expansion of this qualification listing with product in all IC categories — encompassing Bipolar Digital, Linear and MOS technologies.

**JEDEC PROCESSED**

An extensive program supplying JEDEC PROCESSED devices approach Qualified Reliability goals without the delay and high cost of the actual qualification program.

Motorola JEDEC PROCESSED products complement JAN-QUALIFIED products by making available hi-rel versions of nearly all Motorola full-temperature range circuits, while adding the advantage of hi-rel standardization.

**JEDEC BENEFITS**

1. Standardization of environmental and electrical test procedures.
2. Less specification writing required.
3. Less time required in negotiating specifications.
4. Fast delivery.
5. Lower costs.

# Standard Military Product Processing Programs

| Screen | Method | JEDEC Requirements | JAN Qualified | Motorola 883 S | |
|---|---|---|---|---|---|
| | | | | Method | Requirements |
| Wafer Acceptance | | | | 5007 | |
| Internal Visual (Precap) | 2010 Condition B and 38510 | 100% | 100% | 2010 Condition A and 38510 | 100% |
| Stabilization Bake | 1008, 24 Hrs. Test Condition C or Equivalent | 100% | 100% | 1008 24 Hrs. min Condition C | 100% |
| Temperature Cycling | 1010 Condition C | 100% | 100% | 1010 Condition C | 100% |
| Constant Acceleration | 2001 Condition E min in $Y_1$ plane | 100% | 100% | 2001 Condition E min in $Y_1$ plane | 100% |
| Pind Testing | | | | 2020 Ceramic Pkgs. | 100% |
| Seal Fine & Gross | 1014 | 100% | 100% | 1014 | 100% |
| Interim Electrical | As Applicable Device Note 1 | As Applicable | As Applicable | JAN slash sheet elec. spec. Serialization R&R. Variable data. Note 1 | As Applicable |
| Burn-In Test | 1015 @ 125°C or Equivalent PDA = 10% | 100% | 100% | 1015 125°C min 240 Hrs. PDA = 5% | 100% |
| Final Electrical Tests<br>(a) Static Tests | Per Applicable Device Specification | | | JAN slash sheet elec. spec. Read and Record 25°C Note 1 | |
| 1. 25°C (Subgroup 1, Table 1, 5005) | | 100% | 100% | | 100% |
| 2. Max and min rated operating temperature (Subgroups 2 and 3 Table 1, 5005) | | 100% | 100% | | 100% |
| (b) Dynamic Tests and Switching Tests 25°C (Subgroup 4 and 9 Table 1, 5005) | | 100% | 100% | | 100% |
| (c) Functional Test 25°C (Subgroup 7, Table 1, 5005) | | 100% | 100% | 25°C, −55°C, 125°C | 100% |
| Quality Conformance Inspection: Group A | 5005 Class B | Sample per Applicable Specification (Provision) Equal to or tighter than 883 | LTPD | 5005 Class S | LTPD |
| (a) Static | | | | | |
| 1. 25°C (Subgroup 1) | | | 5% | | 3% |
| 2. Temperature (Subgroup 2&3) | | | 7% | | 5% |
| (b) Switching | | | | | |
| 1. 25°C (Subgroup 9) | | | 7% | | 5% |
| 2. Temperature (Subgroup 10&11) | | | 10% | | |
| (c) Functional | | | | | |
| 1. 25°C (Subgroup 7) | | | 5% | | 3% |
| RadioGraphic | | | | 2012 | 100% |
| Group B | 5005 Class B | Insp. Lot | Insp. Lot | 5005 Class S | Insp. Lot |
| Group C | 5005 Class B | 52 Wks. Prod. | 13 Wks. Prod. | | |
| Group D | 5005 Class B | 12 Mos. Package Production | 6 Mos. Package Production | 5005 Class S | Generic or Insp. Lot |
| External Visual | 2009 | 100% | 100% | 2009 | 100% |

NOTE 1: Motorola data sheet electricals where JAN slash sheets are not available.

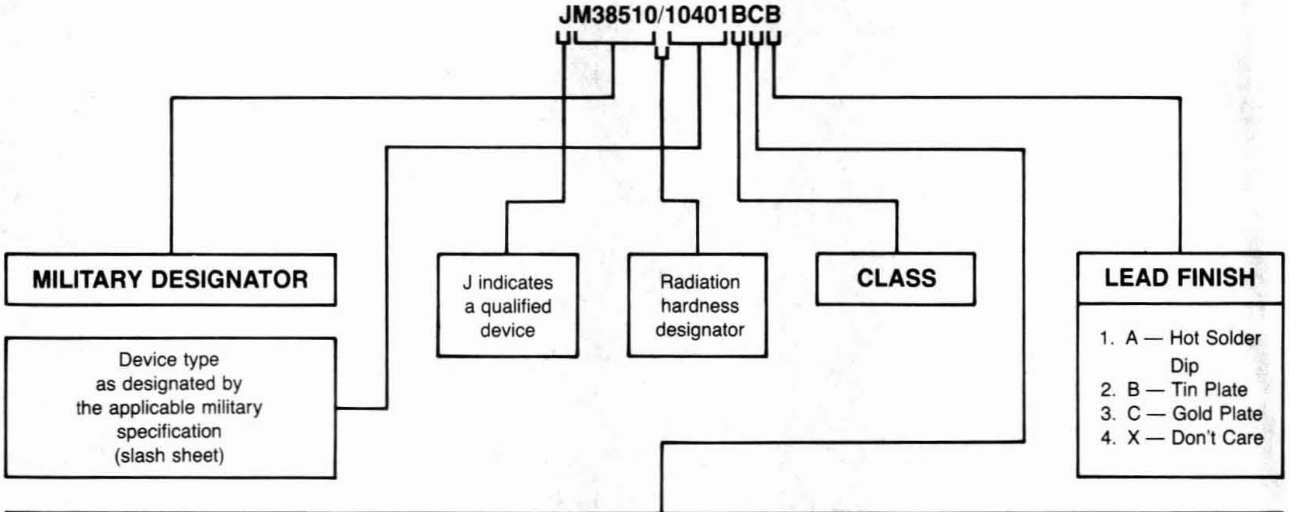
# Ordering and Marking for Better Level Product

| MC34004 | P | D |
|---|---|---|
| Part Identification | Standard Package Suffix | Better Processing<br>Level I = Suffix S<br>Level II = Suffix D<br>Level III = Suffix DS |

## Ordering & Marking for JEDEC Hi-Rel Processing Program

| 139 | / | B | C | B | JC |
|---|---|---|---|---|---|
| **Motorola Device Type (Without letter prefix)** | **Slash** | **Device Class (See Table)** | **Case Outline (Same as JAN Qualified Product, See Table Below)** | **Lead Finish Same as JAN Qualified Product, See Table Below** | **JEDEC Designator** |

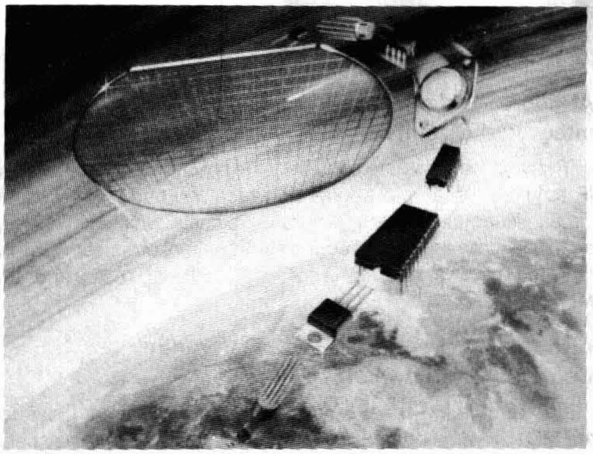
## Ordering & Marking for JAN Qualified Program


JM38510/10401BCB
MILITARY DESIGNATOR
J indicates a qualified device
Radiation hardness designator
CLASS
LEAD FINISH
1. A — Hot Solder Dip
2. B — Tin Plate
3. C — Gold Plate
4. X — Don't Care
Device type as designated by the applicable military specification (slash sheet)

**CASE OUTLINE**

1. A — ¼" x ¼+ flat pack, 14-pin
2. B — 3⁄16" x ¼" flat pack, 14-pin
3. C — ¼" x ¾" dual-in-line, 14-pin
4. D — ¼" x ⅜" flat pack, 14-pin
5. E — ¼" x ⅞" dual-in-line, 16-pin
6. F — ¼" x ⅜" flat pack, 16-pin
7. G — 8-lead can
8. H — ¼" x ¼" flat pack, 10-lead
9. I — 10-lead can
10. J — ½" x 1¼" dual-in-line, 24-pin
11. K — ⅜" x ⅝" flat pack, 24-pin
12. L — ⅜" x ½" flat pack, 24-pin
13. M — 12-lead can
14. N — (Size *N/D) flat pack, 24-pin
15. P — ¼" x ⅜" dual-in-line, 8-pin
16. Q — 0.60" x 2.00" dual-in-line, 40-pin
17. R — ¼" x 1 1⁄16" dual-in-line, 20-pin
18. S — ¼" x ½" flat pack, 20-pin
19. T — (Size *N/D) flat pack, 22-pin
20. U — 0.40" x 0.40" leadless flat pack, 24-pin
21. V — 0.30" x 1.00" dual-in-line, 18-pin
22. W — 0.40" x 1.10" dual-in-line, 22-pin
23. X
24. Y Variable per applicable slash sheet
25. Z

*N/D — NOT DEFINED



# Applications Literature

# Applications Literature

The application literature listed in this section has been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications. To obtain copies of the notes, simply list the publication number or numbers and send your request on your company letterhead to: Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

## Application Note Abstracts

### AN401 The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier

This application note discusses four different applications for the MC1554, along with a circuit description including dc characteristics, frequency response, and distortion. A section of the note is also devoted to package power dissipation calculations including the use of the curves on the power amplifier data sheet.

### AN471 Analog-to-Digital Conversion Techniques

The subject of analog-to-digital conversion and many of the techniques that can be used to accomplish it are discussed. The paper is written in general terms from a system point of view and is intended to assist the reader in determining which conversion technique is best suited for a given application.

### AN489 Analysis and Basic Operation of the MC1595

The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given along with performance that is characteristic of the device. A few basic applications are given to assist the designer in system design.

### AN491 Gated Video Amplifier Applications Using The MC1545

This application note reviews the basic operation of the MC1545 and discusses some of the more popular applications for the MC1545. Included are several modulator types, temperature compensation of the active gate, AGC, gated oscillators, FSK systems, and single supply operation.

### AN513 A High Gain Integrated Circuit RF-IF Amplifier with Wide Range AGC

This note describes the operation and application of the MC1590G, a monolithic RF-IF amplifier. Included are several applications for IF amplifiers, a mixer, video amplifiers, single and two-stage RF amplifiers.

### AN531 MC1596 Balanced Modulator

The MC1596 monolithic circuit is a highly versatile communications building block. In this note, both theoretical and practical information are given to aid the designer in the use of this part. Applications include modulators/demodulators for AM, SSB, and suppressed carrier AM; frequency doublers and HF/VHF double balanced mixers.

### AN543A Integrated Circuit IF Amplifiers for AM/FM and FM Radios

This application note discusses the design and performance of four IF amplifiers using integrated circuits. The IF amplifiers discussed include a high performance circuit, a circuit utilizing a quadrature detector, a composite AM/FM circuit, and an economy model for use with an external discriminator.

### AN545A Television Video IF Amplifier Using Integrated Circuits

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, and the MC1330.

### AN547 A High-Speed Dual Differential Comparator, The MC1514

This application note discusses a few of the many uses for the MC1514 dual comparator. Many applications such as sense amplifiers, multivibrators, and peak level detectors are presented.

### AN587 Analysis and Design of the Op Amp Current Source

A voltage controlled current source utilizing an operational amplifier is discussed. Expressions for the transfer function and output impedances are developed using both the ideal and non-ideal op amp models. A section on analysis of the effects of op amp parameters and temperature variations on circuit performance is presented.

### AN599 Mounting Techniques for Metal Packaged Power Semiconductors

For cooler, more reliable operation, proper mounting procedures must be followed if the interface thermal resistance between the semiconductor package and heat sink is to be minimized. Discussed are aspects of preparing the mounting surface, using thermal compounds, and fastening techniques. Typical interface thermal resistance is given for a number of packages.

### AN702 High Speed Digital-To-Analog and Analog-To-Digital Techniques

A brief overview of some of the more popular techniques for accomplishing D/A and A/D techniques. In particular those techniques which lead themselves to high speed conversion.

### AN703 Designing Digitally-Controlled Power Supplies

This application note shows two design approaches; a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in an application.

### AN708A Line Driver and Receiver Considerations

This report discusses many line driver and receiver design considerations such as system description, definition of terms, important parameter measurements, design procedures and application examples. An extensive line of devices is available from Motorola to provide the designer with the tools to implement the data transmission requirements necessary for almost every type of transmission system.

### AN713 Binary D/A Converters can Provide BCD-Coded Conversion

This note describes the application and use of integrated circuit D/A converters for use in providing a BCD-coded conversion. The technique is illustrated using a 2-1/2 digit digital voltmeter.

### AN714 A Personalized Heart-Rate Monitor with Digital Readout

Using the micropower operational amplifier MC1776 and CMOS digital integrated circuits, entirely self-contained portable electro-medical monitoring equipment can be built. This note details the construction of a heart-rate monitor giving a digital indication, beat-by-beat.

### AN716 Successive Approximation A/D Conversion

Recent advances in integrated circuit design and technology have resulted in reduced cost of high performance successive approximation analog to digital converters. This note describes and illustrates two examples of how modern IC components have changed this well known technique.

### AN719 A New Approach to Switching Regulators

This article describes a 24-Volt, 3-Ampere switching mode supply. It operates at 20 kHz from a 120 Vac line with an overall efficiency of 70%. New techniques are used to shape the load line. The control portion uses a quad comparator and an opto coupler and features short circuit protection.

### AN720 Interfacing with MECL 10,000

This article describes some of the MECL circuits used to interface with signals not meeting MECL input or output requirements. The characteristics of these circuits such as input impedance, output drive, gain and bandwidth allow the system designer to use these parts to optimize his system. MECL interface circuits overcome a problem area of many system designs, which is the efficient coupling of non-compatible signals.

### AN727 Television Horizontal APC/AFC Loops: The Last 10 Percent

A discussion of some common problems that may be encountered with the design of Horizontal APC/AFC loops and methods to avoid or overcome them.

### AN737A Switched Mode Power Supplies — Highlighting A 5.0-V, 40-A Inverter Design

This application note identifies the features of various regulator circuits that are in use today in ac to dc power supplies. The note also illustrates how these circuits may be used as complementary building blocks in a system design. Primary emphasis is on switched mode regulators because they fill the present need for energy and space savings.

A complete 5.0-V, 40-A line operated inverter supply is described in detail including design procedures for the magnetic components. The inverter itself is a "state-of-the-art" design which features CMOS logic, high voltage power transistors, Schottky rectifiers and an optoelectronic coupler. It operates with a full load efficiency of 80% at a frequency of 20 kHz.

### AN752 An 80-Watt Switching Regulator for CATV and Industrial Applications

This application note describes a 24-Volt, 3.0-Ampere switching, regulated power supply that operates above 18 kHz from a 40-to 60-Volt, 60-Hz square wave source (CATV power line from a feroresonant transformer) or a dc standby source with input output isolation. The control circuit consists of a dual operational amplifier and a linear integrated circuit timer which are used to vary the on time of a new high-speed power transistor. The circuit provides good efficiency, good regulation, low output ripple and incorporates input and output voltage over shutdown protection.

### AN760 Application of The MC3416 Crosspoint Switch

The operation and application of the MC3416 4 x 4 balanced crosspoint switch is described in detail. Special emphasis is given to balanced switching systems like those in space division PABX. Discussion of the total system design using the MC3416 is also included.

### AN767 A Line Operated, Regulated 5.0 V/50 A Switching Power Supply

This application note describes a regulated 220 Vac to 5.0 Vdc converter using high voltage switching transistors and Schottky barrier rectifiers. The control functions are all performed by integrated circuits.

### AN775 M6800 Systems Utilizing the MC6875 Clock Generator/Driver

This application note describes the use of the MC6875 clock generator/driver in M6800 based systems. Design examples will demonstrate the capabilities of the driver in systems using slow and/or dynamic memories. Multiprocessing and DMA methods are also covered.

### AN778 Mounting Techniques for Power Semiconductors

For reliable operation, semiconductors must be properly mounted. Discussed are aspects of preparing the mounting surface, using thermal compounds, insulation techniques, fastening techniques, handling of leads and pins, and evaluation methods for the thermal system.

### AN781A Revised Data Interface Standards

This application note provides a brief overview and comparison of communication interface standards RS-232-C, RS-422A, RS-423, RS-449 and RS-485 for the hardware designer. A listing of the standard's specifications and appropriate Motorola devices are included.

### AN787 An M6800 Clock System That Handles DMA and Memory Refresh Cycle Stealing

Dynamic memory and three-state cycle stealing for Direct Memory Access transfers require a clock generator and priority logic to maintain proper refresh times of the dynamic MPU and dynamic memory. The design presented here demonstrates use of the MC6875 clock generator with an MC6800 MPU.

### AN829 Application of the MC1374 TV Modulator

The MC1374 was designed for use in applications where separate audio and composite video signals are available, which need converting to a high quality VHF television signal. It's idealy suited as an output device for subscription TV decoders, video disk and video tape players.

### AN842 Microprocessor-Compatible DACs and the MC6890

As the range of applications and consequently the usage, of microprocessors steadily increases, the need for more efficient interfacing also increases. There has been developed a class of DACs which incorporate the commonly used circuits necessary for microprocessor interfacing, thus easing the design problems involved.

### AN844 Extending the Capabilities of the MC10315/MC10317 Flash A/D Converters

Recent advances in manufacturing capabilities have provided the means to produce 7-bit flash converters in monolithic form. This application note will discuss some of the means whereby the user may extend the resolution and speed of the basic devices.

### AN848 An Evaluation System for High-Speed A-D and D-A Converters

The purpose of this application note is to describe the capabilities and operation of the MC10315 and MC10317 flash A-D converter, as well as their application in an Evaluation Board designed for their use at frequencies which include video rates.

### AN877 Precision Voltage References for the MC10315/MC10317 Flash A-D Converters

In order to produce a digital representation of an analog signal, all analog-to-digital converters require a reference voltage. The digital output word is the result of a comparison of that analog voltage versus the reference voltage.

While most analog-to-digital converters have a high input impedance for the reference voltage, the MC10315/10317 flash A-D converters have a reference input resistance of (typically) 64 ohms, thus requiring a significant current be supplied from a precision source. This application note describes several circuit configurations which can be used to supply the reference voltage, and current, at the stability by the A-D converters.

### AN879 Monomax — Application of the MC13001 Monochrome Television Integrated Circuit

This application note presents a complete 12″ black and white line-operated television receiver, including artwork for the printed circuit board. It is intended to provide a good starting point for the first-time user. Some of the most common pitfalls are overcome, and the significance of component selections and locations are discussed.

### AN917 Reading and Writing in Floppy Disk Systems Using Motorola Integrated Circuits

The floppy disk system has become a widely used means for storing and retrieving both programs and data. A floppy disk drive requires precision controls to position and load the head as well as defined read/write signals in order to be a viable system. This application note describes the use of the MC3469 and MC3471 Write Control ICs and the MC3470 Read Amplifier which provide the necessary head and erase control, timing functions, and filtering.

### AN920A Theory and Applications of the MC34063 and μA78S40 Switching Regulator Control Circuits

This paper describes in detail the principle of operation of the MC34063 and μA78S40 switching regulator subsystems. Several converter design examples and numerous applications circuits with test data are included.

### AN926 Techniques for Improving the Settling Time of a DAC & Op-Amp Combination

This application note describes some techniques which were tested for the purpose of optimizing settling time of a DAC/op-amp combination. The objective of the experimentation was to obtain a settling time of under 1.0 μs for 12 bit (±0.012%) accuracy. Op-amps chosen for this exercise are high speed, yet inexpensive monolithic devices.

### AN932 Application of the MC1377 Color Encoder

The MC1377 is an economical, high quality, RGB encoder for NTSC or PAL applications. It accepts red, green, blue, and composite sync inputs and delivers 1Vpp composite NTSC or PAL video output into a 75 ohm load. It can provide its own color oscillator and burst gating, or it can be easily driven from external sources. Performance virtually equal to high cost studio equipment is possible with common color receiver components. The following note is intended to explain the operation of the device and guide the prospective user in selecting the optimum circuit for his needs.

### AN954 A Unique Converter Configuration Provides Step-Up/Down Functions

The use of switching regulators in new portable equipment designs is becoming more pronounced over that of linear regulators. This is primarily due to the need for reductions in size and weight which dictate an ever increasing demand for higher power conversion efficiency from a battery pack. When designing at the board level it sometimes becomes necessary to generate a constant output voltage that is less than that of the battery. The step-down circuit will perform this function efficiently. However, as the battery discharges, its terminal voltage will eventually fall below the desired output, and in order to utilize the remaining battery energy, the step-up circuit will be required.

## Engineering Bulletin Abstracts

### EB20 Multiplier/OP Amp Circuit Detects True RMS

Two op amps and two multipliers are used in the circuit described by EB-20 to obtain the true rms of an input voltage ranging from 2 to 10 Vpk.

### EB51 Successive Approximation BCD A/D Converter

A successive approximation A/D converter in which a digital-to-analog converter in a feedback loop produces a BCD digital output from an analog input is described in EB-51.

### EB57 An Economical FM Transmitter Voice Processor from a Single IC

An MC3401 Quad Op-Amp is used as a Microphone/Modulation interface in an FM transmitter.

### EB66A A Symmetry Correcting Circuit for Use with the MC3420

EB-66 shows a method of implementing an external symmetry-correction circuit with the MC3420 Switchmode Regulator Control IC to insure balanced operation of the power transformer in push-pull inverter configurations.

### EB78 New ICs Perform Control and Ancillary Functions in High Performance Switching Supplies

This bulletin discusses the MC3420 and MC3423. The MC3420 performs a great number of functions required for the control of inverter type Switchmode power supplies. The MC3423 is for the overvoltage protection of power supplies.

### EB85A Full-Bridge Switching Power Supplies

This bulletin provides information for the preliminary selection of devices required for implementation of a full-bridge-configuration supply from 500 to 1000 watts.

### EB86 Half-Bridge Switching Power Supplies

This bulletin provides information for the preliminary selection of devices required for implementation of a half-bridge-configuration supply from 100 to 500 watts.

### EB87A Flyback Switching Power Supplies

This bulletin provides information for the preliminary selection of devices required for implementation of a flyback-configuration supply from 100 to 250 watts.

### EB88 Push-Pull Switching Power Supplies

This bulletin provides information for the preliminary selection of devices required for implementation of a push-pull-configuration supply from 100 to 500 watts.

### EB100 A Simplified Power-Supply Design Using the TL494 Control Circuit

This bulletin describes the operation and characteristics of the TL494 Switchmode Voltage Regulator and shows its application in a 400-watt off-line power supply.

## TMOS Design Tip Abstracts

### TDT101B A 100 kHz FET Switcher

This note describes a circuit for a 60 W, 100 kHz FET switcher with four output voltages, operating from 120 Vac.

## Alphanumeric Index and Cross Reference

**Including Surface Mount Devices (SMD)**

## Selector Guide

## Analog Circuits

**Amplifiers**

**Data Converters**

**Comparators**

**Special Circuits**

## Power Supply Circuits

**Voltage/Switching Regulators**

**Voltage References**

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**Memory Interface and Control**

**Bus Interface**

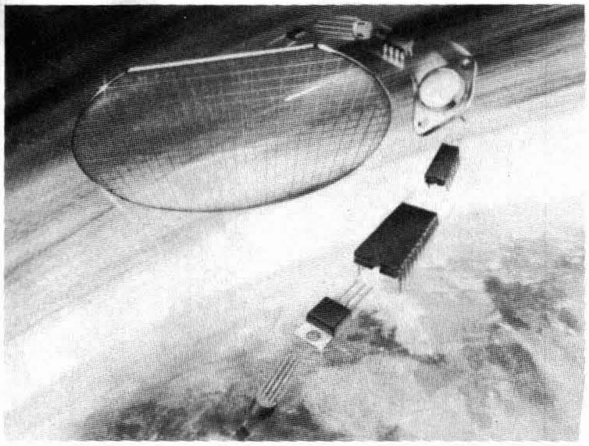
**Line Drivers and Receivers**

## Consumer and Automotive Circuits

## Packaging Information

**Including Surface Mount Devices (SMD)**

## Quality and Reliability Assurance

## Applications Literature